QUALITY
SEMICONDUCTOR, INC.

High-Speed CMOS 3.3V 8-Bit Register

QS74LVC574A

FEATURES/BENEFITS

- 5V tolerant inputs and outputs
- 10µA I_{CCQ} quiescent power supply current
- Hot insertable
- 2.0V–3.6V V_{CC} supply operation
- ±24mA balanced output drive
- Power down high impedance inputs and outputs
- Input hysteresis for noise immunity
- Meets or exceeds JEDEC Standard 36 specifications
- Multiple power and ground pins for low noise
- Operating temperature range:
  –40°C to 85°C
- Latch-up performance exceeds 500mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V
- Packages available:
  20-pin QSOP
  20-pin SOIC

DESCRIPTION

The LVC574A is an 8-bit buffered register with three-state outputs that is ideal for driving high capacitance loads such as memory address and data buses. The 3.3V LVC family features low power, low switching noise, and fast switching speeds for low power portable applications as well as high-end, advanced workstation applications. 5V tolerant inputs and outputs allow this LVC product to be used in mixed 5V and 3.3V applications. To accomodate hot-plug or live insertion applications, this product is designed not to load an active bus when V_{CC} is removed.

Figure 1. Functional Block Diagram

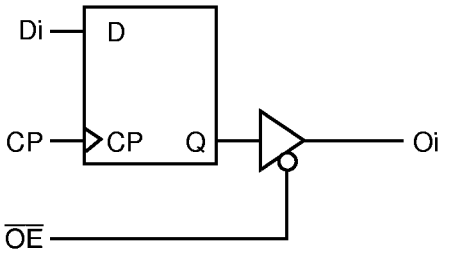


Figure 2. Pin Configurations
(All Pins Top View)

SOIC, QSOP

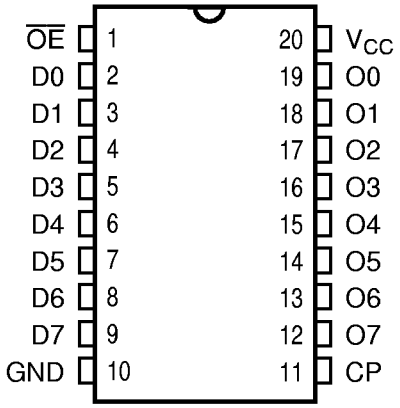


Table 1. Pin Description

Name	I/O	Description
Di	I	Data Inputs
Oi	O	Data Outputs
CP	I	Clock Input
$\overline{OE}$	I	Output Enable

Table 2. Function Table

Inputs			Internal	Outputs	
$\overline{OE}$	CP	Di	Q Value	Oi	Function
H	X	X	X	Hi-Z	Disable Outputs
L	↑	X	L	L	Enable Outputs
L	↑	X	H	H	
X	↑	L	L	X	Load Input Data
X	↑	H	H	X	

Table 3. Absolute Maximum Ratings

Supply Voltage to Ground ..... –0.5V to 7.0V
DC Output Voltage V_{OUT}
Outputs HIGH-Z ..... –0.5V to 7.0V
Outputs Active ..... –0.5V to V_{CC} + 0.5V
DC Input Voltage V_{IN} ..... –0.5V to 7.0V
DC Input Diode Current with $V_{IN} < 0$ ..... –50mA
DC Output Diode Current
$V_O < 0$ ..... –50mA
$V_O > V_{CC}$ 50mA
DC Output Source/Sink Current (I_{OH}/I_{OL}) ..... ±50mA
DC Supply Current per Supply Pin ..... ±100mA
DC Ground Current per Ground Pin ..... ±100mA
T_{STG} Storage Temperature ..... –65°C to 150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

Table 4. Recommended Operating Conditions

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage, Operating		2.0	3.6	V
	Supply Voltage, Data Retention Only		1.5	3.6	
V_{IH}	Input HIGH Voltage	V_{OL} = 2.7 to 3.6V	2.0	—	V
V_{IL}	Input LOW Voltage	V_{CC} = 2.7 to 3.6V	—	0.8	V
V_{IN}	Input Voltage		0	5.5	V
V_{OUT}	Output Voltage in Active State		0	V_{CC}	V
	Output Voltage in "OFF" State		0	5.5	
I_{OH}	Output Current HIGH	V_{CC} = 3.0–3.6V	—	–24	mA
		V_{CC} = 2.7V		–12	
I_{OL}	Output Current LOW	V_{CC} = 3.0–3.6V	—	24	mA
		V_{CC} = 2.7V	—	12	
$\Delta t/\Delta v$	Input Transition Slew Rate		—	10	ns/V
T_A	Operating Free Air Temperature		–40	85	°C

Table 5. DC Electrical Characteristics Over Operating Range

Industrial Temperature Range, T_A = –40°C to 85°C

Symbol	Parameter	Test Conditions	Min	Typ(1)	Max	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 2.7V, I_{OH} = –100µA V_{CC} = 2.7V, I_{OH} = –12mA V_{CC} = 3.0V, I_{OH} = –12mA V_{CC} = 3.0V, I_{OH} = –24mA	V_{CC} –0.2 2.2 2.4 2.2	— — — —	— — — —	V
V_{OL}	Output LOW Voltage	V_{CC} = 2.7V, I_{OL} = 100µA V_{CC} = 2.7V, I_{OL} =12mA V_{CC} = 3.0V, I_{OL} = 24mA	— — —	— — —	0.2 0.4 0.55	V
V_{IK}	Input Clamp Voltage	V_{CC} = 2.7V, I_{IN} = –18mA	—	–0.7	–1.2	V
I_I	Input Leakage Current	V_I = 0V, V_I = 5.5V, V_{CC} = 3.6V	—	—	±1.0	µA
I_{OZ}	High-Z I/O Leakage	V_O = 0V, V_O = 5.5V, V_I = V_{IH} or V_{IL}, V_{CC} = 3.6V	—	—	±1.0	µA
I_{OFF}	Power Off Leakage	V_{CC} = 0V, V_I or V_O = 5.5V	—	—	10	µA
I_{CC}	Quiescent Power Supply Current	V_{CC} = 3.6V, V_{IN} = V_{CC} or GND	—	0.1	10	µA
ΔI_{CC}	Quiescent Power Supply Current per Inputs at TTL HIGH	V_{CC} = 3.6V, V_{IN} = V_{CC} – 0.6V(2)	—	2.0	3.0	µA

Notes:
1. Typical values are at V_{CC} = 3.3V and T_A = 25°C.
2. Per TTL driven input. All other inputs at V_{CC} or GND.

Table 6. Dynamic Switching Characteristics

Symbol	Parameter	Test Conditions		Typ(1)	Unit
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	C_L = 50pF, V_{CC} = 3.3V	V_{IH} = 3.3V, V_{IL} = 0V	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	C_L = 50pF, V_{CC} = 3.3V	V_{IH} = 3.3V, V_{IL} = 0V	0.8	V
C_{PD}	Power Dissipation	C_L = 50pF, f = 10MHz,	Output Enable	20	pF
		V_{CC} = 3.3 ±0.3V	Output Disable	4	

Note:
1. Typical values are at V_{CC} = 3.3V, 25°C ambient.

Table 7. Capacitance(1)

Symbol	Pins	Conditions	Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V, V_{OUT} = 0V, f = 1MHz	7.0	pF
$C_{I/O}$	I/O Capacitance	V_{IN} = 0V, V_{OUT} = 0V, f = 1MHz	8.0	pF

Note:
1. Capacitance is characterized but not production tested.

Table 8. Switching Characteristics Over Operating Range

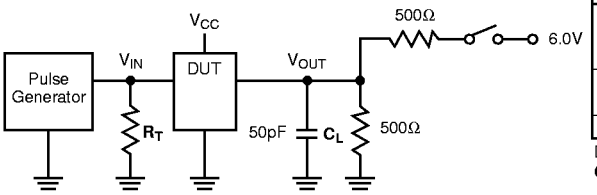
Industrial Temperature Range, T_A = –40°C to 85°C.
C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description(1)	V_{CC} = 3.3 ±0.3V		V_{CC} = 2.7V(2)		Unit
		Min	Max	Min	Max	
f_{MAX}	Clock Pulse Frequency(2)	150	—	150	—	MHz
t_{PD}	Propagation Delay CP to Oi	1.5	7.0	1.5	8.0	ns
t_{EN}	Output Enable Time $\overline{OE}$ to Oi	1.5	7.5	1.5	8.5	ns
t_{DIS}	Output Disable Time(2) $\overline{OE}$ to Oi	1.5	6.4	1.5	7.0	ns
t_S	Data Setup Time Di to CP	2.0	—	2.0	—	ns
t_H	Data Hold Time Di to CP	1.5	—	1.5	—	ns
t_W	Clock Pulse Width(2) HIGH or LOW	3.3	—	3.3	—	ns
$t_{SK(O)}$	Output Skew(3)	—	0.5	—	—	ns

Notes:
1. Minimums guaranteed but not tested. See Test Circuit and Waveforms.
2. Guaranteed by characterization.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by characterization but not production tested.

TEST CIRCUIT AND WAVEFORMS

Figure 3. Test Circuit



SWITCH POSITION

Test	Switch
Open Drain Disable LOW Enable LOW	6V
Disable HIGH Enable HIGH	GND
All Other Inputs	Open

DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

Figure 4. Setup, Hold, and Release Timing

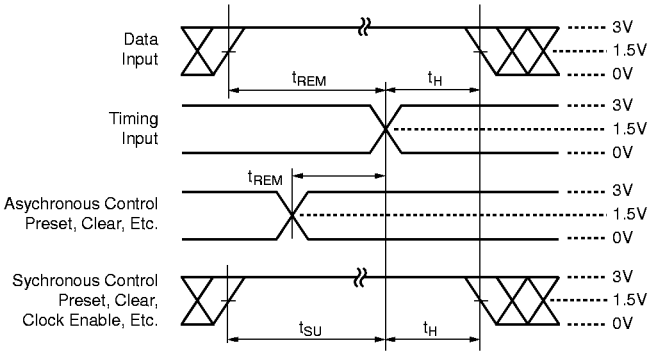


Figure 6. Pulse Width

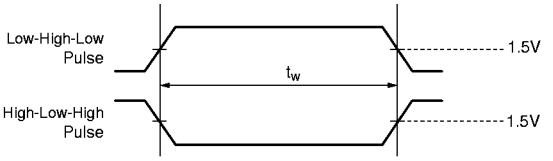


Figure 5. Enable and Disable Timing

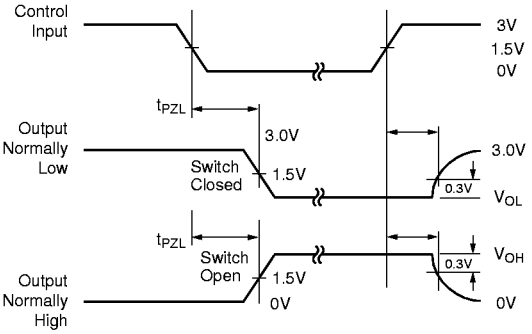
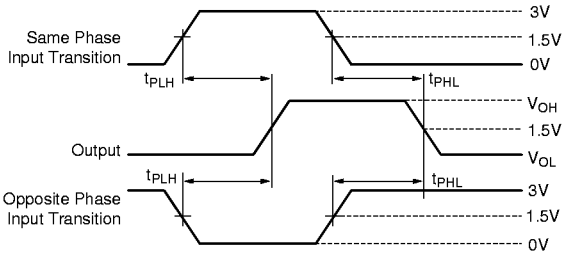
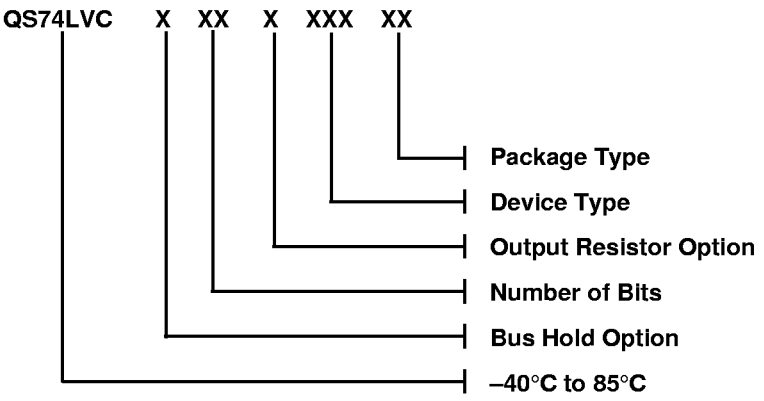


Figure 7. Propagation Delay



Notes:
1. Input Control Enable = LOW and Input Control Disable = HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_{OUT} \leq 50\Omega$; t_F, $t_R \leq 2.5$ns.

ORDERING INFORMATION



Bus Hold Option:
Blank – No Bus Hold

Number of Bits:
Blank – 8-Bit

Output Resistor Option:
Blank – No Output Resistor

Device Type:
574

Package Type:
Q – QSOP, 150 mil
SO – SOIC, 300 mil