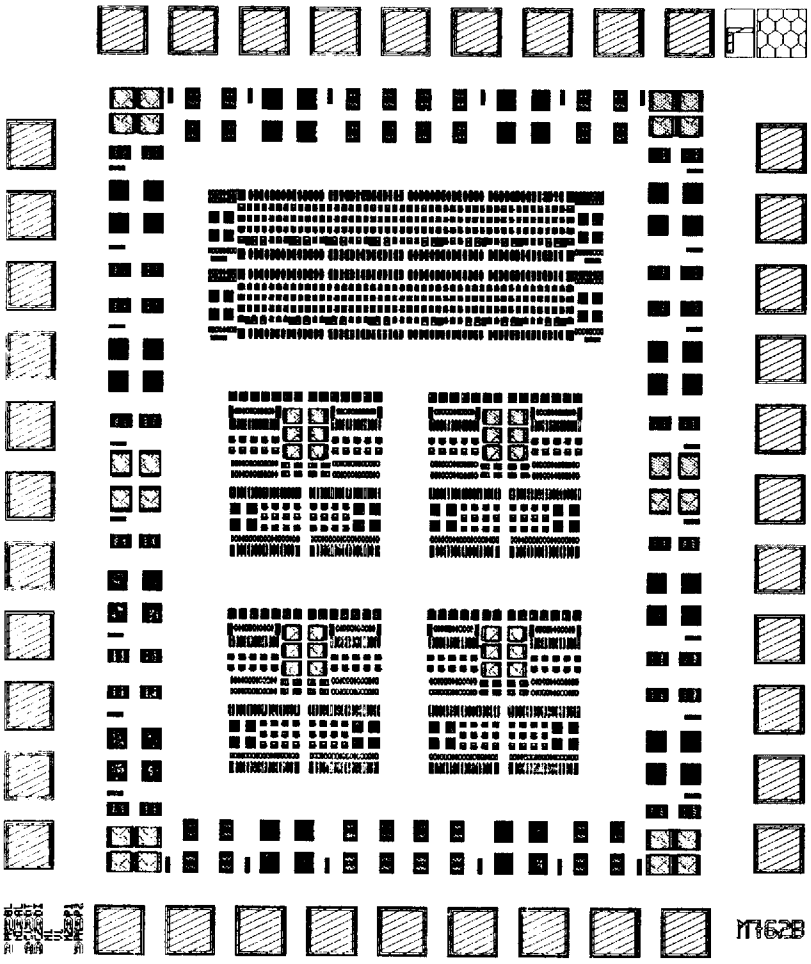
T-42-31

# QuickChip™ 7 Integrated Circuit Array

Tektronix
Test and Measurement



The *QuickChip™* 7 Integrated Circuit Array combines an entirely new generation polysilicon wafer fabrication process with our *QuickCustom™* Design System to produce a powerful tool for analog or mixed analog/digital applications.

Our new process (GST-1), offers the following features:

- 2x density improvement over SHPi (QC6)
- Trench isolation (poly filled)
- $f_T$ > 12 GHz @ $V_{CE}$ = 4 V, NPN
- 200 Ω/□ poly resistors
- 4 μm metal pitch, 2 layers of Au
- Trimmable nichrome resistors (50 Ω/□)
- Schottky diodes
- Low power ( $f_T$ peak at 600 μA for G11M02)

QuickChip 7 is an uncommitted array of very high speed bipolar transistors, capacitors, resistors, and Schottky diodes that the analog circuit designer can quickly interconnect to meet application requirements using the Tektronix QuickCustom Design Process. Typical applications include:

- RF amplifiers and mixers
- Sample and hold circuits
- High-speed comparators
- Voltage-controlled oscillators
- Prescalers
- High speed logic/interface functions

## Process Description

The QuickChip 7 IC is designed on a wafer fabrication process known as Giga-Speed Si-Bipolar Technology (GST-1). GST-1 is a self-aligned, double-polysilicon process. To isolate devices this process uses a deep trench that increases density and reduces parasitics. All devices except resistors are completely trench isolated. GST-1 has a thin base with a highly doped emitter which yields high speed with good DC parameters.

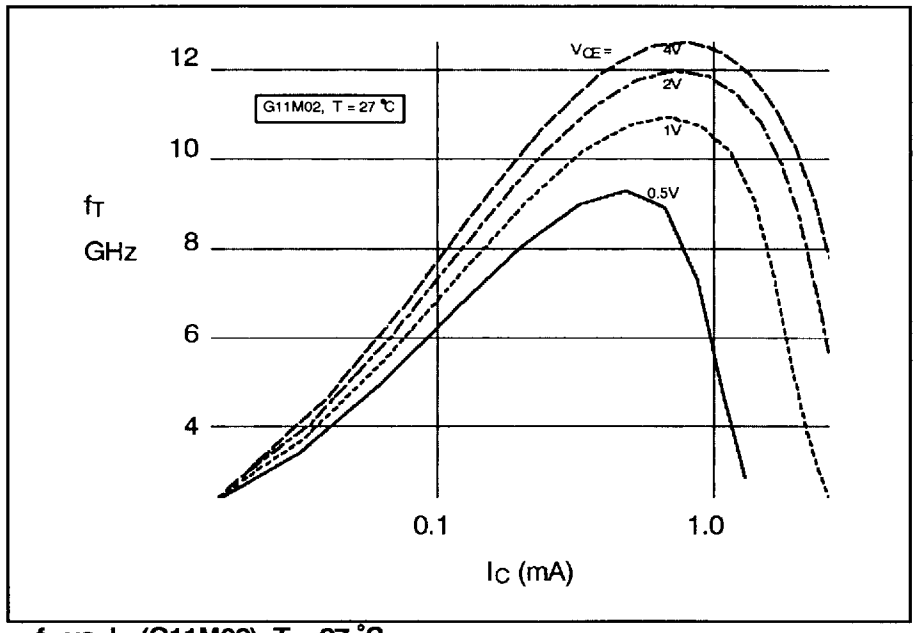
## Chip Description

The QuickChip 7 consists of an array that is 90 mils (2.28 mm) by 76 mils (1.93 mm). Since the GST-1 process is well suited for mixed analog/digital designs, the QuickChip 7 array is divided into a section that is optimized for analog design and a section that is optimized for digital (ECL) design. The analog section consists of 4 symmetrical macro-tiles, occupying the lower two-thirds of the central portion of the array. These 4 macro-tiles contain 208 NPN transistors, 56 PNP transistors, 32 Schottky

diodes, 24 capacitors and 848 resistors. The top third of the central portion of the array is occupied by the digital section, one large macro-tile, constructed from 8 full tiles (each sufficient to design a clocked master-slave data latch) and 4 half tiles. The digital area is designed for easy implementation of ECL logic with 200 mV to 600 mV internal logic swings. Collectively, this area contains 336 NPN transistors, 32 Schottky diodes, and 560 resistors. The periphery of the chip contains 48 large NPN transistors for I/O applications, 64 ESD diodes, and 24 [1.35 pF (max.)] capacitors. The complete array is surrounded by 40 bond pads.

| Device Type | Name | Analog Area | Digital Area | Periphery | Total |
|---|---|---|---|---|---|
| small NPN | G11M02 | 0 | 304 | 0 | 304 |
| small NPN | G11M032 | 176 | 16 | 0 | 192 |
| medium NPN | G12U05 | 32 | 16 | 0 | 48 |
| large NPN | G14V102 | 0 | 0 | 48 | 48 |
| PNP | PLAT | 56 | 0 | 0 | 56 |
| Schottky diode | DSU2 | 32 | 32 | 0 | 64 |
| ESD diode | DESD7 | 0 | 0 | 64 | 64 |
| 2 kΩ resistor | RY2KA | 400 | 0 | 0 | 400 |
| 2 kΩ resistor | RY2KD | 0 | 464 | 0 | 464 |
| 400 Ω resistor | RY400 | 448 | 96 | 0 | 544 |
| MOS capacitor | CMOS | 24 | 0 | 0 | 24 |
| MOS/junction capacitor | CSW | 0 | 0 | 24 | 24 |
| pad | PAD | 0 | 0 | 0 | 40 |

**The QuickChip 7 IC Devices**




**$f_T$ vs. $I_C$ (G11M02), T = 27 °C**

## Design Tools

The QuickCustom approach leads smoothly through all the steps required to design an IC. The QuickChip 7 Design Guide provides the necessary information to use the process, enabling even the first-time user to complete a design with minimal one-on-one coaching. The startup package includes 2½ days of training at Tektronix which provides all the necessary design and process information plus training on our CAD tools. A library of SPICE models for the QuickChip transistors, resistors, capacitors, diodes, and bonding pads accurately predicts the speed and performance of the design. Models are available for –55 °C to 125 °C operation.

*QuickKic™*, a comprehensive design tool, is included with the QuickCustom start-up package. QuickKic provides schematic capture, netlist extraction, design rule checking, and a grid-based graphics editor to greatly simplify the design and layout process. Quickic can also be used to extract metal run parasitic capacitance and resistance.

*QuickChip™* Terminology:

**Tile** -- an area on the array which contains various unconnected devices in a basic layout pattern. [On QuickChip 7, a full tile is 176 μm x 176 μm.]

**Macro-tile** -- a grouping of tiles, half tiles, and/or quarter tiles. QuickChip 7 contains a digital macro-tile and four analog macro-tiles.

**Array** -- a fixed configuration of macro-tiles and/or tiles, with added perimeter devices, placed in a way that is optimum for construction of integrated circuits.

| Parameter | Symbol | Measurement Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| Collector-Base Breakdown Voltage | $BV_{CBO}$ | $I_C$=1 µA | 12 | | V |
| Collector-Emitter Punch-through Voltage | $BV_{CES}$ | $I_C$=1 µA | 10 | | V |
| Collector-Emitter Sustaining Voltage | $LV_{CEO}$ | $I_C$=400 µA | 5 | | V |
| Collector-Emitter Breakdown Voltage | $BV_{CEO}$ | $I_C$=1 µA | 4 | | V |
| Emitter-Base Breakdown Voltage | $BV_{EBO}$* | $I_E$=1 µA | 4 | | V |
| Emitter-Collector Punch-through Voltage | $BV_{ECS}$ | $I_E$=1 µA | 1.5 | | V |
| Collector-Substrate Breakdown Voltage | $BV_{CS}$ | $I_C$=1 µA | 25 | | V |
| Collector-Collector Breakdown Voltage | $BV_{CCS}$ | $I_C$=1 µA | 20 | | V |
| Emitter-Base Forward Voltage | $V_{BES}$ | $I_C$=400 µA | 0.80 | 0.90 | V |
| Collector-Emitter Saturation Voltage | $V_{CE}$(sat) | $I_C$=400 µA, $I_B$=40 µA | | 0.15 | V |
| Early Voltage | $V_A$ | $V_{BE}$=0.89V, $V_{CE}$=2, 3V | 15 | | V |
| DC Current Gain | $\beta_F$ | $V_{CB}$=2V, $I_C$=40 µA<br>$V_{CB}$=2V, $I_C$=100 µA<br>$V_{CB}$=2V, $I_C$=400 µA | 40<br>40<br>40 | | |
| Collector-Emitter Leakage Current | $I_{CEO}$ | $V_{CE}$=3V | | 1 | nA |
| Emitter-Base Leakage Current | $I_{EBO}$ | $V_{EB}$=2.5V* | | 50 | nA |
| Emitter Resistance | $R_E$ | $I_E$=60, 90 µA | 50 | 120 | Ω |
| Common Emitter Unity Gain Frequency | $f_T$ | $V_{CE}$=4V, $I_C$=600 µA | 12 | | GHz |
| Voltage Mismatch | $\Delta V_{BE}$ (3 σ) | $I_C$ = 1 mA | | 2.5 | mV |

*Note: There may be a degradation of β for $V_{EB}$ > 3V

**NPN Electrical Specifications (G11M02), T= 27 °C**

| Parameter | Symbol | Measurement Conditions | Nom | Min | Max | Units |
|---|---|---|---|---|---|---|
| Forward Diode Voltage | $V_F$ | $I_F$= 75 µA | 375 | | | mV |
| | | $I_F$=750 µA | 458 | 300 | 550 | mV |
| Reverse Diode Leakage Current | $I_R$ | $V_R$= 1 V | 30 | | 50 | nA |
| | | $V_R$= 3 V | 100 | | 200 | nA |

**Schottky Diode (DSU2) Electrical Specifications, T= 27 ° C.**

A recent addition to QuicKic permits real-time verification between the netlist and layout. QuicKic reads the netlist and permits only the correct combination of devices to be interconnected on the layout. The combination of real-time Design Rule Checking and Verification has greatly increased the productivity of the designer and reduced development time and cost.

The startup package also includes QuERC™, a proprietary electrical rules checker which examines the DC bias conditions as provided by the circuit simulator. Using a data base of process and device limitations, QuERC identifies design problems early in the development process.

After receipt of the completed layout, Tektronix performs an extensive connectivity check between the SPICE netlist and QuicKic layout to confirm layout accuracy. Tektronix Microelectronics also performs a design rule check (DRC) to verify conformance to the layout rules.

## Design Support

A Product Engineer will be assigned to provide guidance through the QuickCustom design process, through prototype fabrication, and into production. Also available are Tektronix experienced designers to provide design consultation as required. (Up to eight hours of design consultation is included in the startup package.)

| Parameter | Symbol | Measurement Conditions | Min | Units |
|---|---|---|---|---|
| Collector-Emitter Punch-through Voltage | $BV_{CES}$ | $I_C$=1 µA | 12 | V |
| Emitter-Collector Punch-through Voltage | $BV_{ECS}$ | $I_C$=1 µA | 12 | V |
| Collector-Base Breakdown Voltage | $BV_{CBO}$ | $I_C$=1 µA | 12 | V |
| Emitter-Base Breakdown Voltage | $BV_{EBO}$ | $I_C$=1 µA | 12 | V |
| Base-Substrate Breakdown Voltage | $BV_{BS}$ | $I_C$=1 µA | 25 | V |
| Collector-Emitter Sustaining Voltage | $LV_{CEO}$ | $I_C$=100 µA | 8 | V |
| Early Voltage | $V_A$ | $V_{BE}$= -0.8 V, $V_{CE}$= -3 V | 80 | V |
| DC Current Gain | $\beta_F$ | $I_C$= 10 µA, $V_{CB}$= -1 V<br>$I_C$=200 µA, $V_{CB}$= -1 V<br>$I_C$=500 µA, $V_{CB}$= -1 V | 10<br>4<br>2 | |

**Lateral PNP (PLAT) Electrical Specifications, T=27 °C**

| CHARACTERISTICS | RY400 | RY2KA | RY2KD | NI | UNITS |
|---|---|---|---|---|---|
| Resistor Value | 400 | 2000 | 2000 | (note a) | Ω |
| Sheet Resistance | 200 | 200 | 200 | 50 | Ω/□ |
| Tolerance | ± 17 | ± 17 | ± 20 | ± 10 (note b) | % |
| Drawn Width | 3.6 | 2.2 | 1.6 | 4.8 min | µm |
| Temperature Coefficient | -1250 | -1250 | -1250 | <200 | ppm/°C |
| Extra Mask Step | no | no | no | yes | (n.a.) |
| Usable as M1 Cross Under | yes | yes | yes | no | (n.a.) |
| Max Current | 3.6 mA | 2.2 mA | 1.6 mA | 1 mA/ µm of width | (n.a.) |

**Resistor Notes:**

(a) Thin film NiCr resistors can be designed for values ranging from 5 ohms to several thousand ohms.

(b) Tolerance and matching depend on the design of specific NiCr resistors. On-chip laser trimming is available to achieve tolerances as low as ± 0.1% and matching as low as ± 0.02%.

**QuickChip 7 Resistors**

## Quality Assurance

For more than 40 years, the Tektronix commitment to excellence has earned the company a reputation for making instruments of the highest quality. The products of Tektronix Microelectronics have contributed to the performance and reliability of Tektronix instrumentation for more than 20 years.

Our goal is to ship 100 percent quality products on time--every time.

Tektronix Microelectronics' Quality Assurance program consists of quality systems and inspections designed to achieve those goals.

The program consists of:

- Documentation control system including engineering change control.
- Vendor qualification procedure including vendor audits, first article inspections, and vendor product certification.
- Statistical process control (SPC program)
- Lot traceability.
- Independent quality and reliability audits.
- Operator training and certification.
- Preventive maintenance programs.
- Static and environmental control.
- Closed loop corrective action system.

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