

APT5040BN	500V	16.0A	0.40Ω
APT4540BN	450V	16.0A	0.40Ω
APT5050BN	500V	14.0A	0.50Ω
APT4550BN	450V	14.0A	0.50Ω

POWER MOS IV®

N-CHANNEL ENHANCEMENT MODE HIGH VOLTAGE POWER MOSFETS

MAXIMUM RATINGS

All Ratings: $T_C = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	APT				UNIT
		4540BN	5040BN	4550BN	5050BN	
V _{DSS}	Drain-Source Voltage	450	500	450	500	Volts
I _D	Continuous Drain Current	16		14		Amps
I _{DM}	Pulsed Drain Current ①	64		56		Amps
V _{GS}	Gate-Source Voltage	±30				Volts
P _D	Total Power Dissipation @ T _C = 25°C, Derate Above 25°C	240				Watts
T _J , T _{STG}	Operating and Storage Junction Temperature Range	- 55 to 150				°C

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions / Part Number	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage ($V_{GS} = 0V, I_D = 250 \mu A$)	APT5040BN / APT5050BN		500	Volts
		APT4540BN / APT4550BN		450	Volts
I_{DSS}	Zero Gate Voltage Drain Current ($V_{DS} = V_{DSS}, V_{GS} = 0V$)			250	μA
	($V_{DS} = 0.8 V_{DSS}, V_{GS} = 0V, T_C = 125^\circ\text{C}$)			1000	
I_{GSS}	Gate-Source Leakage Current ($V_{GS} = \pm 30V, V_{DS} = 0V$)			± 100	nA
$I_{D(ON)}$	On State Drain Current ②	APT5040BN / APT4540BN		16	Amps
	($V_{DS} > I_{D(ON)} \times R_{DS(ON)} \text{ Max}, V_{GS} = 10V$)	APT5050BN / APT4550BN		14	Amps
$V_{GS(TH)}$	Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 1mA$)	2		4	Volts
$R_{DS(ON)}$	Static Drain-Source On-State Resistance ②	APT5040BN / APT4540BN		0.40	Ohms
	($V_{GS} = 10V, I_D = 0.5 I_D \text{ [Cont.]}$)	APT5050BN / APT4550BN		0.50	Ohms

THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction to Case			0.51	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction to Ambient			40	$^\circ\text{C/W}$
T_L	Max. Lead Temp. for Soldering Conditions: 0.063" from Case for 10 Sec.			300	$^\circ\text{C}$



CAUTION: These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

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Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C_{iss}	Input Capacitance	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1\text{ MHz}$		1430	1800	pF
C_{oss}	Output Capacitance			330	465	pF
C_{rss}	Reverse Transfer Capacitance			130	200	pF
Q_g	Total Gate Charge ^③	$V_{GS} = 10V, I_D = I_D[\text{Cont.}]$ $V_{DD} = 0.5 V_{DSS}$		64	105	nC
Q_{gs}	Gate-Source Charge			8.7	12	nC
Q_{gd}	Gate-Drain ("Miller") Charge			34	51	nC
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 0.5 V_{DSS}$ $I_D = I_D[\text{Cont.}], V_{GS} = 15V$ $R_G = 1.8\Omega$		12	24	ns
t_r	Rise Time			21	42	ns
$t_{d(off)}$	Turn-off Delay Time			51	77	ns
t_f	Fall Time			27	54	ns

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic / Test Conditions / Part Number	MIN	TYP	MAX	UNIT
I_S	Continuous Source Current (Body Diode)	APT5040BN / APT4540BN		16	Amps
		APT5050BN / APT4550BN		14	Amps
I_{SM}	Pulsed Source Current ^① (Body Diode)	APT5040BN / APT4540BN		64	Amps
		APT5050BN / APT4550BN		56	Amps
V_{SD}	Diode Forward Voltage ^② ($V_{GS} = 0V, I_S = -I_D[\text{Cont.}]$)			1.3	Volts
t_{rr}	Reverse Recovery Time ($I_S = -I_D[\text{Cont.}], di_S/dt = 100A/\mu s$)	148	296	592	ns
Q_{rr}	Reverse Recovery Charge	2.2	4.4	8.8	μC

SAFE OPERATING AREA CHARACTERISTICS

Symbol	Characteristic	Test Conditions / Part Number	MIN	TYP	MAX	UNIT
SOA1	Safe Operating Area	$V_{DS} = 0.4 V_{DSS}, I_{DS} = P_D / 0.4 V_{DSS}, t = 1\text{ Sec.}$	240			Watts
SOA2	Safe Operating Area	$I_{DS} = I_D[\text{Cont.}], V_{DS} = P_D / I_D[\text{Cont.}], t = 1\text{ Sec.}$	240			Watts
I_{LM}	Inductive Current Clamped	APT5040BN / APT4540BN	64			Amps
		APT5050BN / APT4550BN	56			Amps

① Repetitive Rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve. (Fig.1)

② Pulse Test: Pulse width < 380 μs , Duty Cycle < 2%

③ See MIL-STD-750 Method 3471

APT Reserves the right to change, without notice, the specifications and information contained herein.

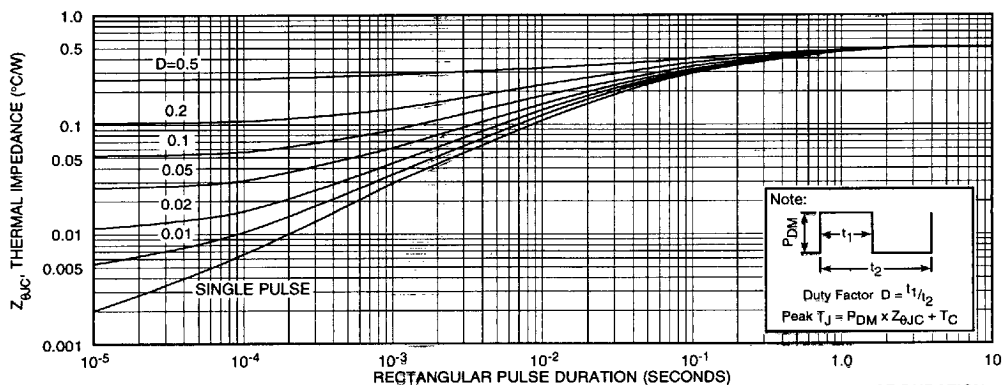
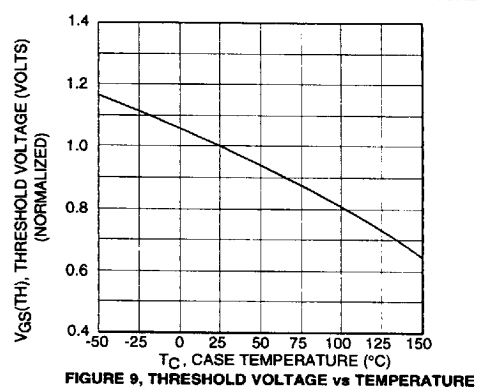
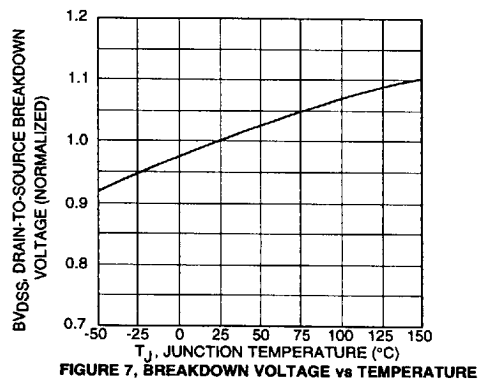
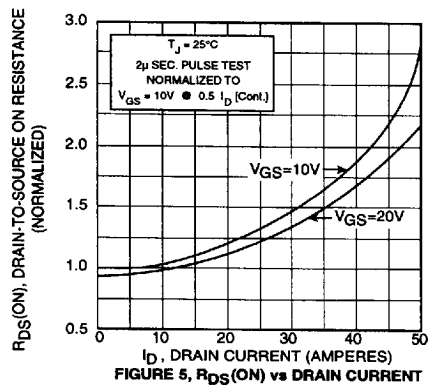
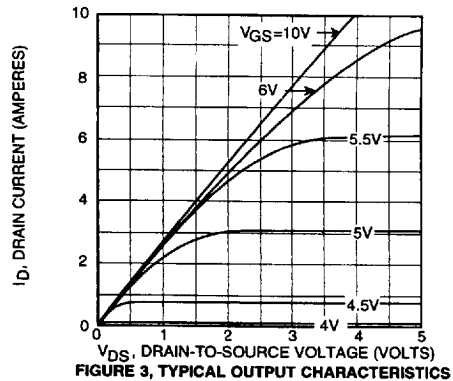
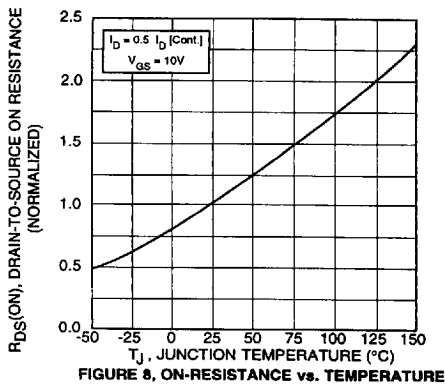
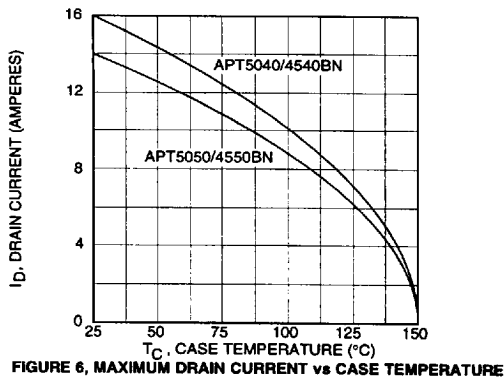
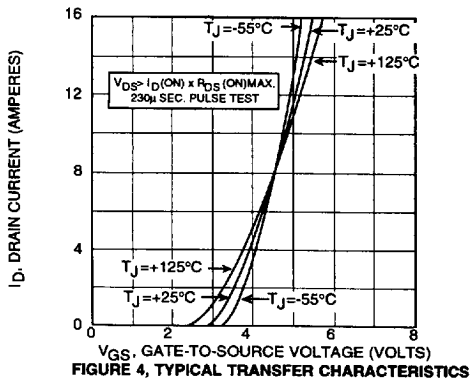
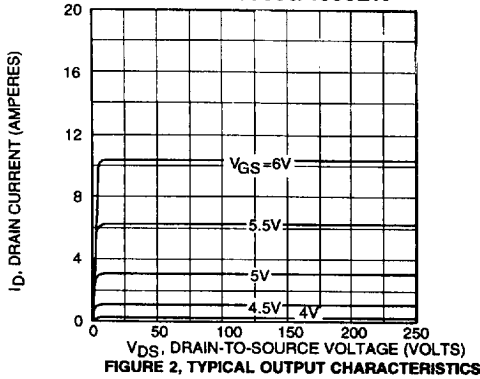


FIGURE 1, MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION
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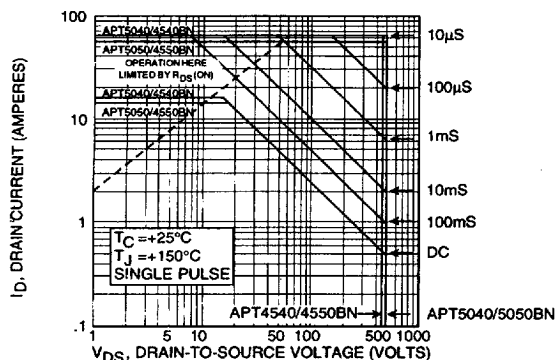


FIGURE 10, MAXIMUM SAFE OPERATING AREA

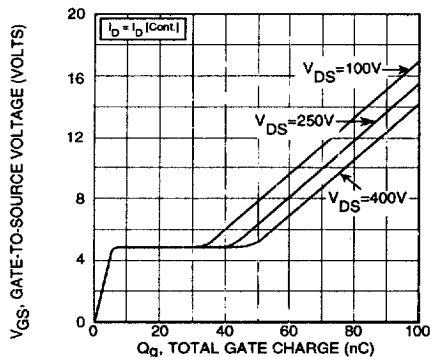


FIGURE 12, GATE CHARGES vs GATE-TO-SOURCE VOLTAGE

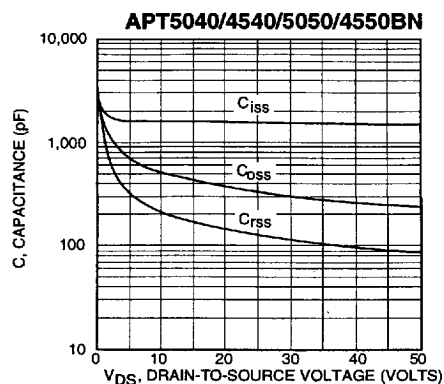


FIGURE 11, TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

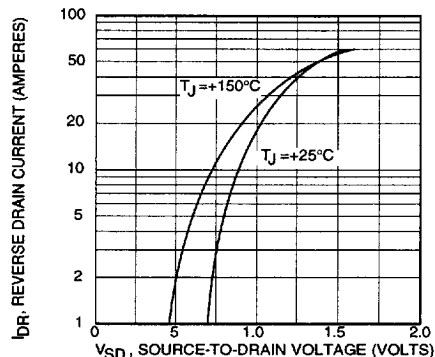
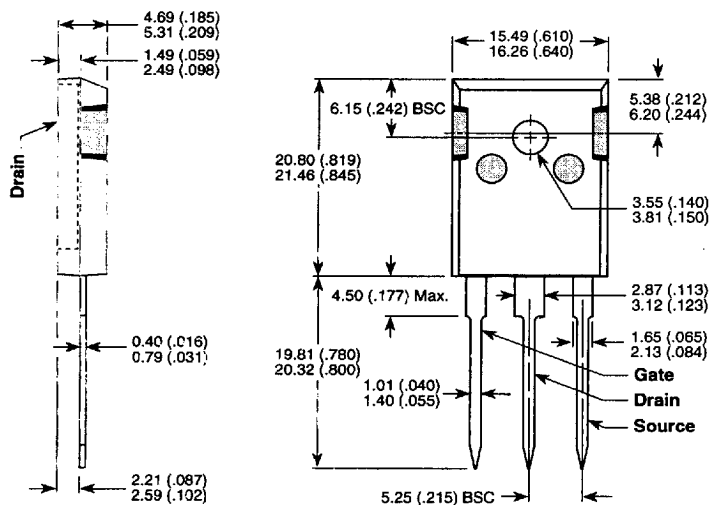


FIGURE 13, TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

TO-247AD Package Outline



Dimensions in Millimeters and (Inches)

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