Preliminary information

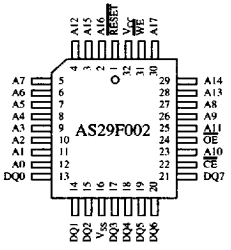
Features

- Organization: 256K×8
- Sector architecture
  - One 16K; two 8K; one 32K; and three 64K byte sectors
  - Boot code sector architecture—T (top) or B (bottom)
  - Erase any combination of sectors or full chip
- Single 5.0±0.5V power supply for read/write operations
- Sector protection
- High speed 55/70/90/120 ns address access time
- Automated on-chip programming algorithm
  - Automatically programs/verifies data at specified address
- Automated on-chip erase algorithm
  - Automatically preprograms/erases chip or specified sectors
- 10,000 write/erase cycle endurance
- Hardware $\overline{\text{RESET}}$ pin
  - Resets internal state machine to read mode
- Low power consumption
  - 40 mA maximum read current
  - 60 mA maximum program current
  - 2 mA maximum standby current
  - 10 µA standby current ($\overline{\text{RESET}}$ = 0)
- JEDEC standard software, packages and pinouts
  - 40-pin TSOP
  - 32-pin PLCC
  - 32-pin TSOP
  - 32-pin PDIP
  - 44-pin PSOP
- Detection of program/erase cycle completion
  - DQ7 $\overline{\text{DATA}}$ polling
  - DQ6 toggle bit
- Erase suspend/resume
  - Supports reading data from a sector not being erased
- Low V_{CC} write lock-out below 3.2V

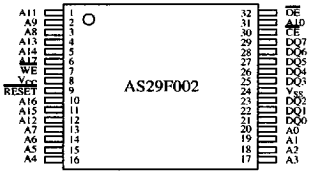
Pin arrangement

40-pin TSOP

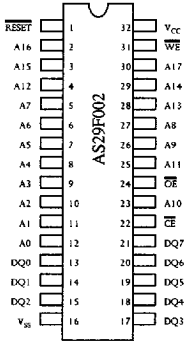
32-pin PLCC



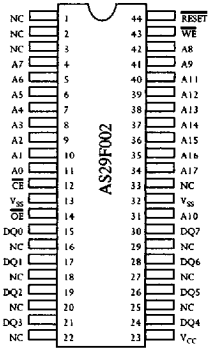
32-pin TSOP



32-pin PDIP



44-pin SO



Selection guide

		29F002-55	29F002-70	29F002-90	29F002-120	Unit
Maximum access time	t_{AA}	55	70	90	120	ns
Maximum chip enable access time	t_{CE}	55	70	90	120	ns
Maximum output enable access time	t_{OE}	30	30	35	50	ns

Functional description

The AS29F002 is a 2 megabit, 5 volt only Flash memory organized as 256K bytes of 8 bits each. For flexible erase and program capability, the 2 megabits of data is divided into 7 sectors: one 16K byte, two 8K byte, one 32K byte, and three 64K bytes. The data appears on DQ0–DQ7. The AS29F002 is offered in JEDEC standard 40-pin TSOP, 32-pin PLCC, 32-pin TSOP, 32-pin PDIP, and 44-pin PSOP packages. This device is designed to be programmed and erased in-sytem with a single 5.0V V_{CC} supply. The device can also be reprogrammed in standard EPROM programmers.

The AS29F002 offers access times of 55/70/90/120 ns, allowing 0-wait state operation of high speed microprocessors. To eliminate bus contention the device has separate chip enable ($\overline{CE}$), write enable ($\overline{WE}$), and output enable ($\overline{OE}$) controls.

The AS29F002 is fully compatible with the JEDEC single power supply Flash standard. Write commands to the command register using standard microprocessor write timings. An internal state-machine uses register contents to control the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Read data from the device in the same manner as other Flash or EPROM devices. Use the program command sequence to invoke the automated on-chip programming algorithm that automatically times the program pulse widths and verifies proper cell margin. Use the erase command sequence to invoke the automated on-chip erase algorithm that preprograms the sector if it is not already programmed before executing the erase operation, times the erase pulse widths, and verifies proper cell margin.

Boot sector architecture enables the device to boot from either the top (AS29F002T) or bottom (AS29F002B) sector. Sector erase architecture allows specified sectors of memory to be erased and reprogrammed without altering data in other sectors. A sector typically erases and verifies within 1.6 seconds. Hardware sector protection disables both program and erase operations in all or any combination of the seven sectors. The device provides background erase with Erase Suspend, which puts erase operations on hold to read data from a sector that is not being erased. The chip erase command will automatically erase all unprotected sectors.

A factory shipped AS29F002 is fully erased (all bits = 1). The programming operation sets bits to 0. Data is programmed into the array one byte at a time in any sequence and across sector boundaries. A sector must be erased to change bits from 0 to 1. Erase returns all bytes in a sector to the erased state (all bits = 1). Each sector is erased individually with no effect on other sectors.

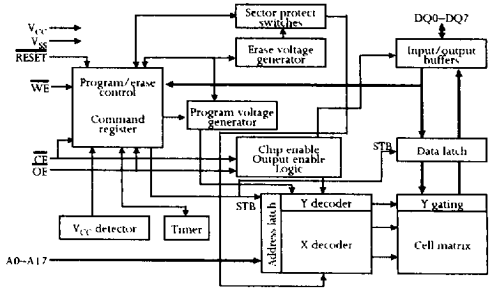
The device features single 5.0V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations during power transtitions. $\overline{DATA}$ polling of DQ7 or toggle bit (DQ6) may be used to detect end of program or erase operations. The device automatically resets to the read mode after program/erase operations are completed.

The AS29F002 resists accidental erasure or spurious programming signals resulting from power transitions. Control register architecture permits alteration of memory contents only after successful completion of specific command sequences. During power up, the device is set to read mode with all program/erase commands disabled when V_{CC} is less than V_{LKO} (lockout voltage). The command registers are not affected by noise pulses of less than 5 ns on $\overline{OE}$, $\overline{CE}$, or $\overline{WE}$. $\overline{CE}$ and $\overline{WE}$ must be logical zero and $\overline{OE}$ a logical one to initiate write commands.

When the device's hardware $\overline{RESET}$ pin is driven low, any program/erase operation in progress will be terminated and the internal state machine will be reset to read mode. If the $\overline{RESET}$ pin is tied to the system reset circuitry and a system reset occurs during an automated on-chip program/erase algorithm, data in address locations being operated on will become corrupted and require rewriting. Resetting the device enables the system's microprocessor to read boot-up firmware from the Flash memory.

The AS29F002 uses Fowler-Nordheim tunnelling to electrically erase all bits within a sector simultaneously. Bytes are programmed one at a time using EPROM programming mechanism of hot electron injection.

Logic block diagram



Flexible sector architecture

Sector	Bottom boot sector architecture (AS29F002B)		Top boot sector architecture (AS29F002T)	
		Size (Kbytes)		Size (Kbytes)
0	00000h–03FFFh	16	00000h–0FFFFh	64
1	04000h–05FFFh	8	10000h–1FFFFh	64
2	06000h–07FFFh	8	20000h–2FFFFh	64
3	08000h–0FFFFh	32	30000h–37FFFh	32
4	10000h–1FFFFh	64	38000h–39FFFh	8
5	20000h–2FFFFh	64	3A000h–3BFFFh	8
6	30000h–3FFFFh	64	3C000h–3FFFFh	16

ID Sector address table

Sector	Bottom boot sector address (AS29F002B)					Top boot sector address (AS29F002T)				
	A17	A16	A15	A14	A13	A17	A16	A15	A14	A13
0	0	0	0	0	X	0	0	X	X	X
1	0	0	0	1	0	0	1	X	X	X
2	0	0	0	1	1	1	0	0	X	X
3	0	0	1	X	X	1	1	0	X	X
4	0	1	X	X	X	1	1	1	0	0
5	1	0	X	X	X	1	1	1	0	1
6	1	1	X	X	X	1	1	1	1	X

Operating modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0	A1	A6	A9	$\overline{RESET}$	DQ
ID read MFR code	L	L	H	L	L	L	V_{ID}	H	Code
ID read device code	L	L	H	H	L	L	V_{ID}	H	Code
Read	L	L	H	A0	A1	A6	A9	H	D_{OUT}
Standby	H	X	X	X	X	X	X	H	High Z
Output disable	L	H	H	X	X	X	X	H	High Z
Write	L	H	L	A0	A1	A6	A9	H	D_{IN}
Enable sector protect	L	V_{ID}	Pulse/L	L	H	L	V_{ID}	H	X
Sector unprotect	L	V_{ID}	Pulse/L	L	H	H	V_{ID}	H	X
Verify sector protect	L	L	H	L	H	L	V_{ID}	H	Code
Temporary sector unprotect	X	X	X	X	X	X	X	V_{ID}	X
Hardware reset	X	X	X	X	X	X	X	L	High Z

L = Low ($<V_{IL}$); H = High ($>V_{IH}$); V_{ID} = 12.0 ± 0.5V; X = Don't care.

Mode definitions

Item	Description
ID MFR code, device code	Selected by A9 = V_{ID}(11.5–12.5V), $\overline{CE}$ = $\overline{OE}$ = A1 = A6 = L, enabling outputs. When A0 is low (V_{IL}) the output data = 52h, a unique Mfr. code for Alliance Semiconductor Flash products. When A0 is high (V_{IH}), D_{OUT} represents the device code for the 29F002.
Read mode	Selected with $\overline{CE}$ = $\overline{OE}$ = L, $\overline{WE}$ = H. Data is valid in t_{ACC} time after addresses are stable, t_{CE} after $\overline{CE}$ is low and t_{OE} after $\overline{OE}$ is low.
Standby	Selected with $\overline{CE}$ = H. Part is powered down, and I_{CC} reduced to <2.0 mA for TTL input levels. If activated during an automated on-chip algorithm, the device completes the operation before entering standby.
Output disable	Part remains powered up; but outputs disabled with $\overline{OE}$ pulled high.
Write	Selected with $\overline{CE}$ = $\overline{WE}$ = L, $\overline{OE}$ = H. Accomplish all Flash erasure and programming through the command register. Contents of command register serve as inputs to the internal state machine. Address latching occurs on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs later. Data latching occurs on the rising edge $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Filters on $\overline{WE}$ prevent spurious noise events from appearing as write commands.
Enable sector protect	Hardware protection circuitry implemented with external programming equipment causes the device to disable program and erase operations for specified sectors.
Sector unprotect	Disables sector protection using external programming equipment.
Verify sector protect	Verifies write protection for sector. Sectors are protected from program/erase operations on commercial programming equipment. Determine if sector protection exists in a system by writing the ID read command sequence and reading location XXX02h, where address bits A13–17 select the defined sector addresses. A logical 1 on DQ0 indicates a protected sector; a logical 0 indicates an unprotected sector.
Temporary sector unprotect	Temporarily disables sector protection for in-system data changes to protected sectors. Apply +12V to $\overline{RESET}$ to activate sector unprotect mode. During sector unprotect mode, program protected sectors by selecting the appropriate sector address. All protected sectors revert to protected state on removal of +12V from $\overline{RESET}$.
$\overline{RESET}$	Resets the write and erase state machine to read mode. If device is programming or erasing when $\overline{RESET}$ = L, data may be corrupted.
Deep power down	Hold $\overline{RESET}$ low to enter deep power down mode (<10 µA CMOS). Recovery time to active mode is 1.5 µs.

READ codes

Mode		A17–A13	A6	A1	A0	Code
MFR code (Alliance Semiconductor)		X	L	L	L	52h
Device code	Top boot	X	L	L	H	B0h
	Bottom boot	X	L	L	H	34h
Sector protection		Sector address	L	H	L	01h protected 00h unprotected

Key: L =Low (<V_{IL}); H = High (>V_{IH}); X =Don't care.

Write operation status

	Status	DQ7	DQ6	DQ5	DQ3
In progress	Auto programming	$\overline{DQ7}$	Toggle	0	0
	Program/erase in auto erase	0	Toggle	0	1
Exceeded time limits	Auto programming	DQ7	Toggle	1	1
	Program erase in auto erase	0	Toggle	1	1

Command definitions

Item	Description
Reset/Read	Initiate read or reset operations by writing the Read/Reset command sequence into the command register. This allows the microprocessor to retrieve data from the memory. Device remains in read mode until command register contents are altered. Device automatically powers up in read/reset state. This feature allows only reads, therefore ensuring no spurious memory content alterations during power up.
ID Read	AS29F002 provides manufacturer and device codes in two ways. External PROM programmers typically access the device codes by driving +12V on A9. AS29F002 also contains an ID read command to read the device code with only +5V, since multiplexing +12V on address lines is generally undesirable. Initiate device ID read by writing the ID Read command sequence into the command register. Follow with a read sequence from address XX00h to return MFG code. Follow ID read command sequence with a read sequence from address XX01h to return device code. To verify write protect status on sectors, read address XX02h. Sector addresses A17–A13 produce a 1 on DQ0 for protected sector and a 0 for unprotected sector. Exit from ID read mode with Read/Reset command sequence.
Hardware reset	Holding $\overline{RESET}$ low for 500 ns resets the device, terminating any operation in progress; data handled in the operation is corrupted. The internal state machine resets 20 µs after $\overline{RESET}$ is driven low. After $\overline{RESET}$ is set high, there is a delay of 1.5 µs for the device to permit read operations.

Item	Description
Byte Programming	Programming the AS29F002 is a four bus cycle operation performed on a byte-by-byte basis. Two unlock write cycles precede the Program Setup command and program data write cycle. Upon execution of the program command, no additional CPU controls or timings are necessary. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$ (whichever is last); data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, (whichever is first). The AS29F002's automated on-chip program algorithm provides adequate internally-generated programming pulses and verifies the programmed cell margin. Check programming status by sampling data on $\overline{DATA}$ polling (DQ7) or the toggle bit (DQ6). The AS29F002 returns the equivalent data that was written to it (as opposed to complemented data), to complete the programming operation. The AS29F002 ignores commands written during programming. A hardware reset occurring during programming may corrupt the data at the programmed location. AS29F002 allows programming in any sequence and across any sector boundary. Changing data from 0 to 1 requires an erase operation. Attempting to program data 0 to 1 results in either DQ5 = 1 (exceeded programming time limits) or success according to $\overline{DATA}$ polling; reading this data after a Read/reset operation returns a 0. When programming time limit is exceeded, DQ5 reads high, and DQ6 continues to toggle. In this state, a reset command returns the device to read mode.
Chip Erase	Chip erase requires six bus cycles: two unlock write cycles; a setup command, two additional unlock write cycles; and finally the Chip Erase command. Chip erase does not require logical 0s written prior to erasure. When the automated on-chip erase algorithm is invoked with the Chip Erase command sequence, AS29F002 automatically programs and verifies the entire memory array for an all-zero pattern prior to erase. The AS29F002 returns to read mode upon completion of chip erase unless DQ5 is set high as a result of exceeding time limit.
Sector Erase	Sector erase requires six bus cycles: two unlock write cycles, a setup command, two additional unlock write cycles, and finally the Sector Erase command. Determine the sector to be erased by addressing any location in the sector. This address is latched on the falling edge of $\overline{WE}$; the command, 30H is latched on the rising edge of $\overline{WE}$. The sector erase operation begins after a 80 µs time-out. To erase multiple sectors, write the sector erase command to each of the addresses of sectors to erase after following the six bus cycle operation above. Timing between writes of additional sectors must be <80 µs, or the AS29F002 ignores the command and erasure begins. During the 80 µs time-out period any falling edge of $\overline{WE}$ resets the time-out. Any command (other than Sector Erase or Erase Suspend) during time-out resets the AS29F002 to read mode, and the device ignores the sector erase command string. Erase such ignored sectors by restarting the Sector Erase command on the ignored sectors. The entire array need not be written with 0s prior to erasure. AS29F002 writes 0s to the entire sector prior to electrical erase; writing of 0s affects only selected sectors, leaving non-selected sectors unaffected. AS29F002 requires no CPU control or timing signals during sector erase operations. Automatic sector erase begins after 80 µs time-out from the last rising edge of $\overline{WE}$ from the sector erase command stream and ends when the $\overline{DATA}$ polling (DQ7) is logical 1. $\overline{DATA}$ polling address must be performed on addresses that fall within the sectors being erased. AS29F002 returns to read mode after sector erase unless DQ5 is set high by exceeding the time limit.

Item	Description
Erase Suspend	Erase suspend allows interruption of sector erase operations to perform data reads from a sector not being erased. Erase suspend applies only during sector erase operations, including the time-out period. Writing an Erase Suspend command during sector erase time-out results in immediate termination of time-out period and suspension of erase operation. AS29F002 ignores any commands during erase suspend other than the Reset or Erase Resume commands. Writing erase resume continues erase operations. Addresses are DON'T CARE when writing Erase Suspend or Erase Resume commands. AS29F002 takes 0.1–15 µs to suspend erase operations after receiving Erase Suspend command. Check completion of erase suspend by polling DQ7 and/or DQ6. AS29F002 ignores redundant writes of erase suspend. AS29F002 defaults to erase-suspend-read mode while an erase operation has been suspended. While in erase-suspend-read mode AS29F002 allows reading data in any sector not undergoing sector erase, treated as standard read mode. Write the Resume command 30h to continue operation of sector erase. AS29F002 ignores redundant writes of the Resume command. AS29F002 permits multiple suspend/resume operations during sector erase.
Sector Protect	When attempting to write to a protected sector, $\overline{\text{DATA}}$ polling and Toggle Bit 1 (DQ6) are activated for about <1 µs. When attempting to erase a protected sector, $\overline{\text{DATA}}$ polling and Toggle Bit 1 (DQ6) are activated for about <5 µs. In both cases, the device returns to read mode without altering the specified sectors.

Status operations

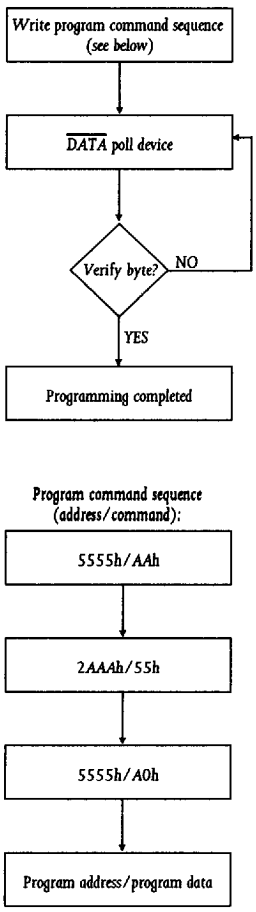
$\overline{\text{DATA}}$ polling (DQ7)	Only active during automated on-chip algorithms or sector erase time outs. DQ7 reflects complement of data last written when read during the automated on-chip algorithm (0 during erase algorithm); reflects true data when read after completion of an automated on-chip algorithm (1 after completion of erase agorithm).
Toggle bit (DQ6)	Active during automated on-chip algorithms or sector time outs. DQ6 toggles when $\overline{\text{CE}}$ or $\overline{\text{OE}}$ toggles, or an Erase Resume command is invoked. DQ6 is valid after the rising edge of the fourth pulse of $\overline{\text{WE}}$ during programming; after the rising edge of the sixth $\overline{\text{WE}}$ pulse during chip erase; after the last rising edge of the sector erase $\overline{\text{WE}}$ pulse for sector erase. For protected sectors, DQ6 toggles for only <1 µs during writes, and <5 µs during erase (if all selected sectors are protected); in both cases, data is unaffected.
Exceeding time limit (DQ5)	Indicates unsuccessful completion of program/erase operation (DQ5 = 1). $\overline{\text{DATA}}$ polling remains active; $\overline{\text{CE}}$ powers the device down to 2 mA. If DQ5 = 1 during chip erase, all or some sectors are defective; during byte programming, the entire sector is defective; during sector erase, the sector is defective (in this case, reset the device and execute a program or erase command sequence to continue working with functional sectors). Attempting to program 0 to 1 will set DQ5 = 1.
Sector erase timer (DQ3)	Checks whether sector erase timer window is open. If DQ3 = 1, erase is in progress; no commands will be accepted. If DQ3 = 0, the device will accept sector erase commands. Check DQ3 before and after each sector erase command to verify that the command was accepted.

Command format

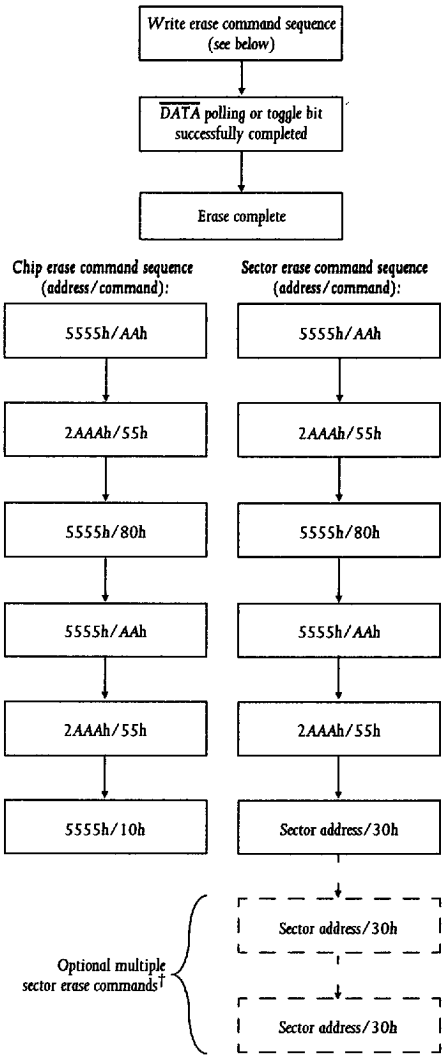
Command sequence	Required bus cycles	1st bus write cycle		2nd bus write cycle		3rd bus write cycle		4th bus write cycle		5th bus write cycle		6th bus write cycle	
		Address	Data	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data
Reset/Read	1	XXXXh	F0h	Read Address	Read Data								
Reset/Read	4	5555h	AAh	2AAAh	55h	5555h	F0h	Read Address	Read Data				
Autoselect ID Read	4	5555h	AAh	2AAAh	55h	5555h	90h	00h MFR code	52h				
top boot								01h Device code	B0h				
bottom boot									34h				
								XXX02h Sector protection	01h = protected 00h = unprotected				
Program	4	5555h	AAh	2AAAh	55h	5555h	A0h	Program Address	Program Data				
Chip Erase	6	5555h	AAh	2AAAh	55h	5555h	80h	5555h	AAh	2AAAh	55h	5555h	10h
Sector Erase	6	5555h	AAh	2AAAh	55h	5555h	80h	5555h	AAh	2AAAh	55h	Sector Address	30h
Sector Erase Suspend	1	XXXXh	B0h										
Sector Erase Resume	1	XXXXh	30h										

1 Bus operations defined in "Mode definitions," on page 250.
2 Reading from non-erasing sectors allowed in Erase Suspend mode.
3 Address bit A12–A17 = X = Don't care for all address commands except Program Address and Sector Address.
4 System should generate address patterns: 5555h or 2AAAh to address A0–A11.
5 A_{IN} for sector protect verify has A_1 = 1, sector selected on A17-A13.

Automated on-chip programming algorithm

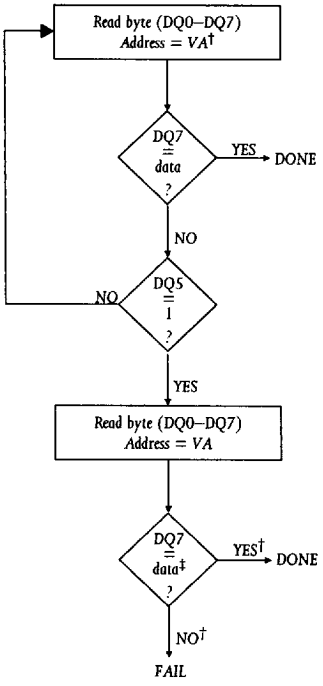


Automated on-chip erase algorithm



† The system software should check the status of DQ3 prior to and following each subsequent sector erase command to ensure command completion. The device may not have accepted the command if DQ3 is high on second status check.

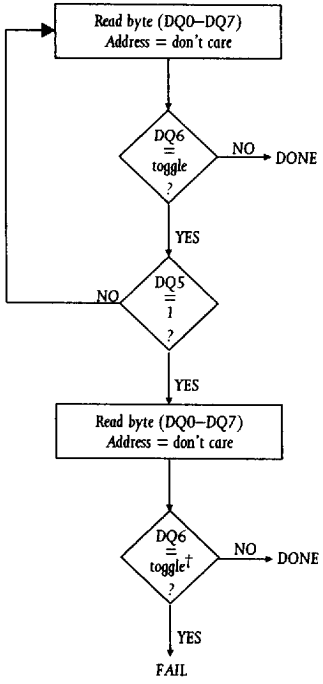
$\overline{DATA}$ polling algorithm



† VA = Byte address for programming. VA = any of the sector addresses within the sector being erased during Sector Erase. VA = valid address equals any non-protected sector group address during Chip Erase.

‡ DQ7 rechecked even if DQ5 = 1 because DQ5 and DQ7 may not change simultaneously.

Toggle bit algorithm



†DQ6 rechecked even if DQ5 = 1 because DQ6 may stop toggling when DQ5 changes to 1.

Flash

DC electrical characteristics

V_{CC} = 5.0±0.5V

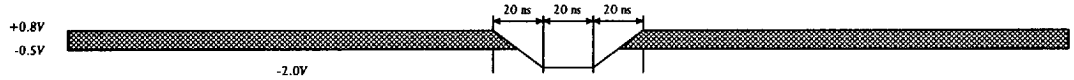
Parameter	Symbol	Test conditions	Min	Max	Unit
Input load current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CCMAX}$	-	±1	µA
A9 Input load current	I_{LIT}	$V_{CC} = V_{CCMAX}$, A9 = 12.5V		90	µA
Output leakage current	I_{LO}	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CCMAX}$	-	±1	µA
Output short circuit current[1]	I_{OS}	V_{OUT} = 0.5V	-	200	mA
Active current, read @ 6MHz[2]	I_{CC}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	-	40	mA
Active current, program/erase[3]	I_{CC2}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	-	60	mA
Standby current (TTL compatible)	I_{SB1}	$\overline{CE} = \overline{OE} = V_{IH}$, $V_{CC} = V_{CCMAX}$	-	2.0	mA
Deep power down	I_{SB2}	$\overline{RP}$ = 0V	-	10	µA
Input low voltage	V_{IL}		-0.5	0.8	V
Input high voltage	V_{IH}		2.0	V_{CC} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 5.8mA, $V_{CC} = V_{CC\ MIN}$	-	0.45	V
Output high level	V_{OH1}	I_{OH} = -2.5 mA, $V_{CC} = V_{CC\ MIN}$	2.4	-	V
	V_{OH2}	I_{OH} = -100 µA, $V_{CC} = V_{CC\ MIN}$	V_{CC} - 0.4	-	V
Low V_{CC} lock out voltage	V_{LKO}		3.2	4.2	V
Input HV select voltage	V_h		11.5	12.5	V

1 Not more than one output tested simultaneously. Duration of the short circuit must not be >1 second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation. (This parameter is sampled and not 100% tested, but guaranteed by characterization.)

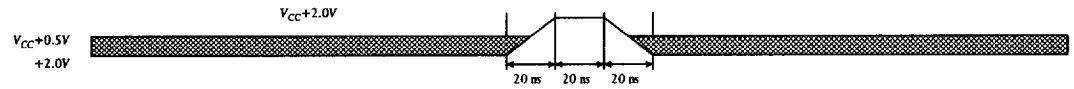
2 The I_{CC} current listed includes both the DC operating current and the frequency dependent component (@ 6 MHz). The frequency component typically is less than 2 mA/MHz with $\overline{OE}$ at V_{IH}.

3 I_{CC} active while program or erase operations are in progress.

Maximum negative overshoot waveform



Maximum positive overshoot waveform



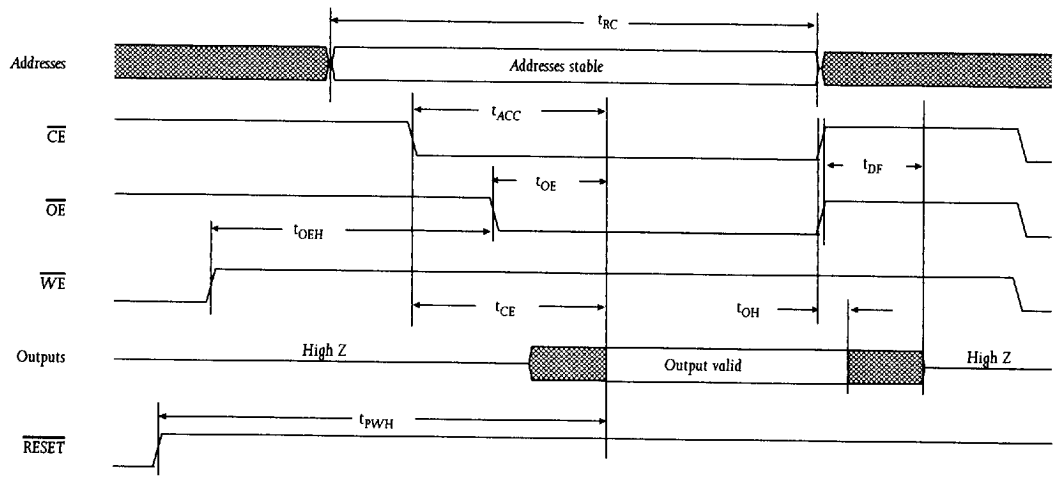
AC parameters: read cycle

JEDEC Symbol	Std Symbol	Parameter	-55 Min	-55 Max	-70 Min	-70 Max	-90 Min	-90 Max	-120 Min	-120 Max	Unit
t_{AVAV}	t_{RC}	Read cycle time	55	-	70	-	90	-	120	-	ns
t_{AVQV}	t_{ACC}	Address to output delay	-	55	-	70	-	90	-	120	ns
t_{ELQV}	t_{CE}	Chip enable to output	-	55	-	70	-	90	-	120	ns
t_{GLQV}	t_{OE}	Output enable to output	-	30	-	30	-	35	-	50	ns
t_{EHQZ}	t_{DF}	Chip enable to output High Z	-	15	-	20	-	20	-	30	ns
t_{GHQZ}	t_{DF}	Output enable to output High Z	-	15	-	20	-	20	-	30	ns
t_{AXQX}	t_{OH}	Output hold time from addresses, first occurrence of $\overline{CE}$ or $\overline{OE}$	0	-	0	-	0	-	0	-	ns
t_{PHQV}	t_{PWH}	$\overline{RESET}$ high to output delay	-	1.5	-	1.5	-	1.5	-	1.5	µs

Key to switching waveforms

Rising input Falling input Undefined output/don't care

Read waveform



Flash

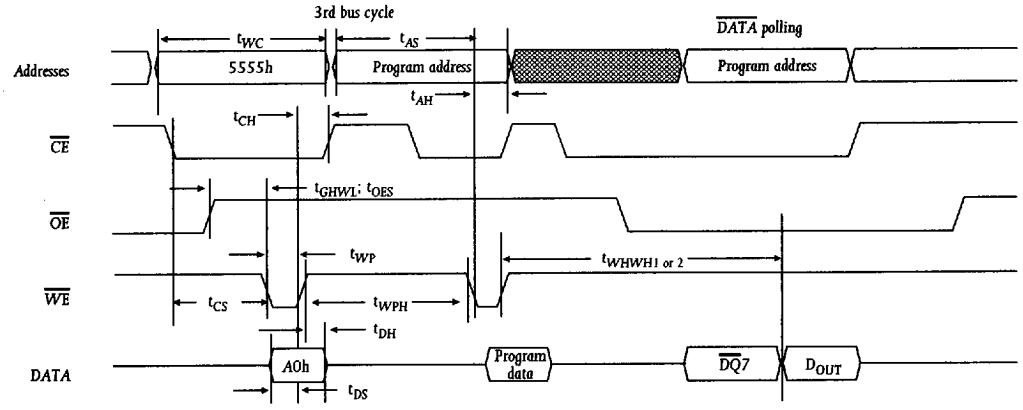
AC parameters — write cycle

$\overline{WE}$ controlled

JEDEC Symbol	Std Symbol	Parameter	-55 Min	-55 Max	-70 Min	-70 Max	-90 Min	-90 Max	-120 Min	-120 Max	Unit
t_{AVAV}	t_{WC}	Write cycle time	55	-	70	-	90	-	120	-	ns
t_{AVWL}	t_{AS}	Address setup time	0	-	0	-	0	-	0	-	ns
t_{WLAX}	t_{AH}	Address hold time	40	-	45	-	45	-	50	-	ns
t_{DVWH}	t_{DS}	Data setup time	25	-	30	-	45	-	50	-	ns
t_{WHDX}	t_{DH}	Data hold time	0	-	0	-	0	-	0	-	ns
	t_{OES}	Output enable setup time	0	-	0	-	0	-	0	-	ns
		Output enable hold time: Read	0	-	0	-	0	-	0	-	ns
	t_{OEH}	Output enable hold time: Toggle and $\overline{DATA}$ polling	10	-	10	-	10	-	10	-	ns
	t_{READY}	$\overline{RESET}$ pin low to read mode	20	-	20	-	20	-	20	-	µs
	t_{RP}	$\overline{RESET}$	500	-	500	-	500	-	500	-	ns
t_{GHWL}	t_{GHWL}	Read recover time before write	0	-	0	-	0	-	0	-	ns
t_{ELWL}	t_{CS}	$\overline{CE}$ setup time	0	-	0	-	0	-	0	-	ns
t_{WHEH}	t_{CH}	$\overline{CE}$ hold time	0	-	0	-	0	-	0	-	ns
t_{WLWH}	t_{WP}	Write pulse width	35	-	35	-	45	-	50	-	ns
t_{WHWL}	t_{WPH}	Write pulse width high	20	-	20	-	20	-	20	-	ns
t_{WHWH1}	t_{WHWH1}	Programming pulse time Byte	50	-	50	-	50	-	50	-	µs
t_{WHWH2}	t_{WHWH2}	Erase pulse time	0.3	-	0.3	-	0.3	-	0.3	-	sec

Write waveform

$\overline{WE}$ controlled



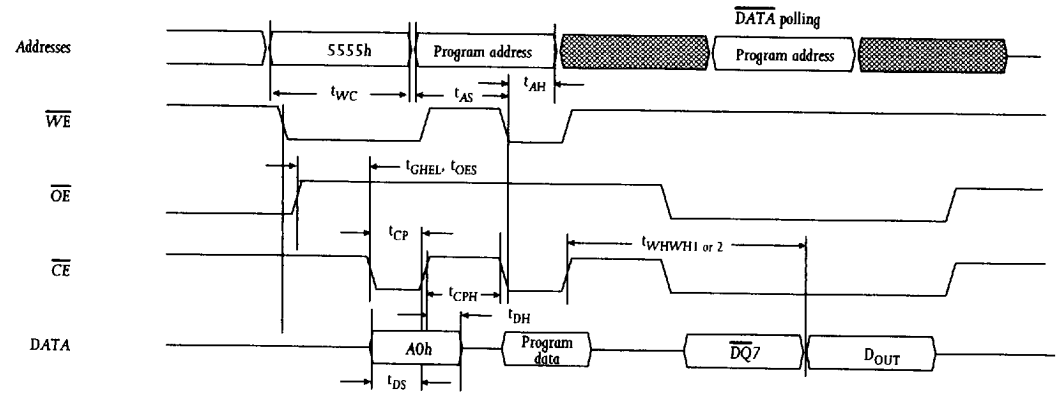
AC parameters—write cycle 2

$\overline{CE}$ controlled

JEDEC Symbol	Std Symbol	Parameter	-55 Min	-55 Max	-70 Min	-70 Max	-90 Min	-90 Max	-120 Min	-120 Max	Unit
t_{AVAV}	t_{WC}	Write cycle time	55	-	70	-	90	-	120	-	ns
t_{AVEL}	t_{AS}	Address setup time	0	-	0	-	0	-	0	-	ns
t_{ELAX}	t_{AH}	Address hold time	40	-	45	-	45	-	50	-	ns
t_{DVEH}	t_{DS}	Data setup time	25	-	30	-	45	-	50	-	ns
t_{EHDX}	t_{DH}	Data hold time	0	-	0	-	0	-	0	-	ns
	t_{OES}	Output enable setup time	0	-	0	-	0	-	0	-	ns
	t_{OEH}	Output enable hold time: Read	0	-	0	-	0	-	0	-	ns
		Output enable hold time: Toggle and $\overline{DATA}$ polling	10	-	10	-	10	-	10	-	ns
t_{GHEL}	t_{GHEL}	Read recover time before write	0	-	0	-	0	-	0	-	ns
t_{WLEL}	t_{WS}	$\overline{WE}$ setup time	0	-	0	-	0	-	0	-	ns
t_{EHWH}	t_{WH}	$\overline{WE}$ hold time	0	-	0	-	0	-	0	-	ns
t_{ELEH}	t_{CP}	$\overline{CE}$ pulse width	35	-	35	-	45	-	50	-	ns
t_{EHEL}	t_{CPH}	$\overline{CE}$ pulse width high	20	-	20	-	20	-	20	-	ns
t_{WHWH1}	t_{WHWH1}	Programming pulse time	50	-	50	-	50	-	50	-	µs
t_{WHWH2}	t_{WHWH2}	Erase pulse time	0.3	-	0.3	-	0.3	-	0.3	-	sec

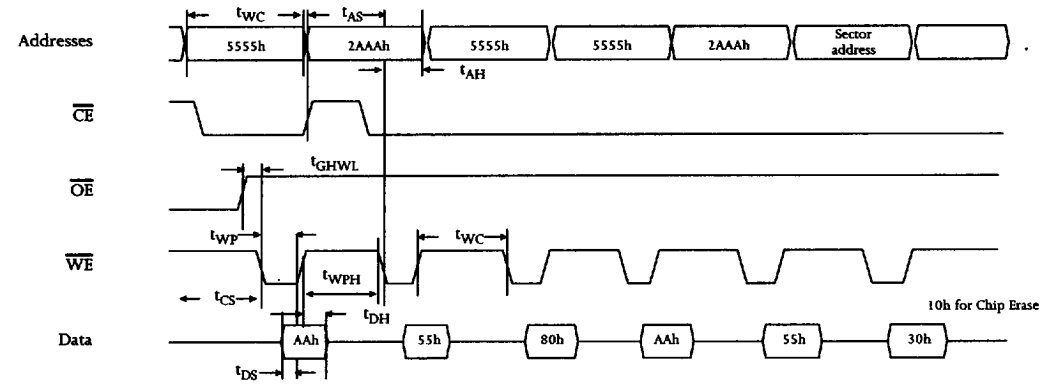
Write waveform 2

$\overline{CE}$ controlled

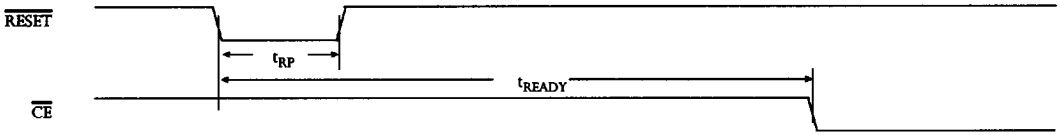


Erase waveform

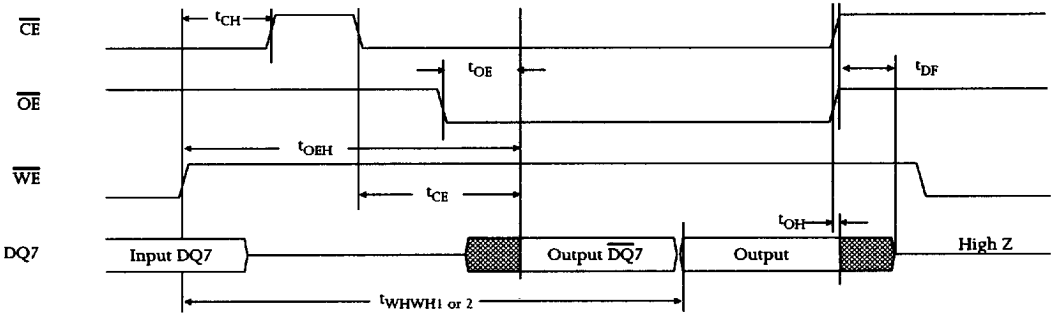
×16 mode only



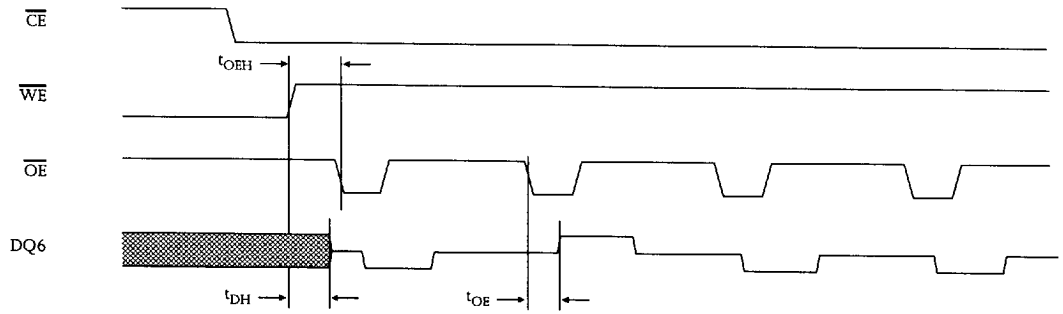
RESET waveform



DATA polling waveform



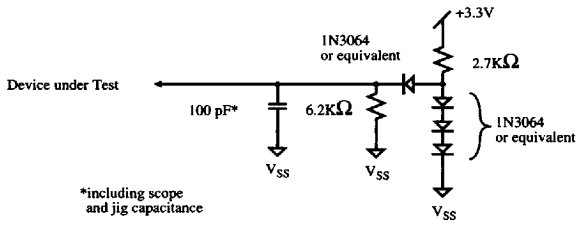
Toggle bit waveform



Erase and programming performance

Parameter	Limits			Unit
	Min	Typical	Max	
Sector erase and verify-1 time (excludes 00h programming prior to erase)	-	1.6	15	sec
Byte program time	50	120	5200	µs
Chip programming time	-	120	240	sec
Erase program cycles	-	-	10,000	cycles

AC test conditions



Recommended operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	+4.5	5.0	+5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.0	-	V_{CC} + 0.5	V
	V_{IL}	−0.5	-	0.8	V

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Input voltage (Input or DQ pin)	V_{IN}	−2.0	+7.0	V
Input voltage (A9 pin, $\overline{OE}$, $\overline{RESET}$)	V_{IN}	−2.0	+13.0	V
Power supply voltage	V_{CC}	-0.5	+5.5	V
Operating temperature	T_{OPR}	−55	+125	°C
Storage temperature (plastic)	T_{STG}	−65	+150	°C
Short circuit output current	I_{OUT}	-	200	mA

Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Latchup tolerance

Parameter	Min	Max	Unit
Input voltage with respect to V_{SS} on A9, $\overline{OE}$, and $\overline{RESET}$ pin	-1.0	+13.0	V
Input voltage with respect to V_{SS} on all DQ, address and control pins	-1.0	V_{CC}+1.0	V
Current	-100	+100	mA

Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0V, one pin at a time.

TSOP pin capacitance

Symbol	Parameter	Test setup	Typ	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control pin capacitance	V_{IN} = 0	8	10	µF

SO pin capacitance

Symbol	Parameter	Test setup	Typ	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control pin capacitance	V_{IN} = 0	8	10	µF

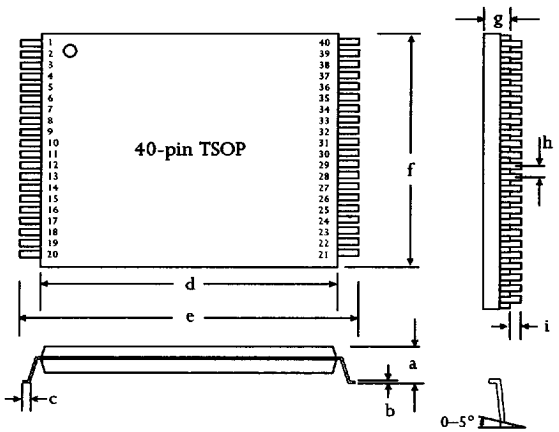
PLCC pin capacitance

Symbol	Parameter	Test setup	Typ	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control pin capacitance	V_{IN} = 0	7.5	9	pF

Data retention

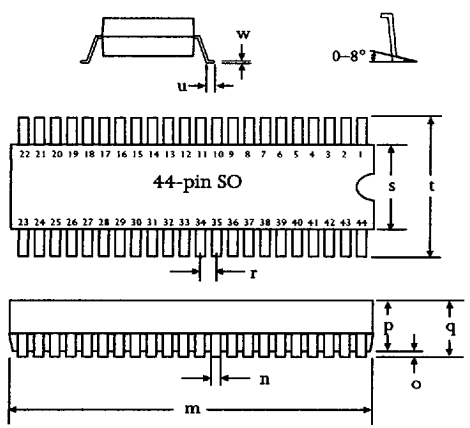
Parameter	Temp. (°C)	Min	Unit
Minimum pattern data retention time	150°	10	years
	125°	20	years

Package dimensions



40-pin TSOP

	Min (mm)	Max (mm)
a		1.20
b	0.120	0.134
c	0.30	0.35
d	18.20	18.60
e	19.80	20.20
f	9.8	10.2
g	0.96	1.02
h		0.5
i	0.05	0.15

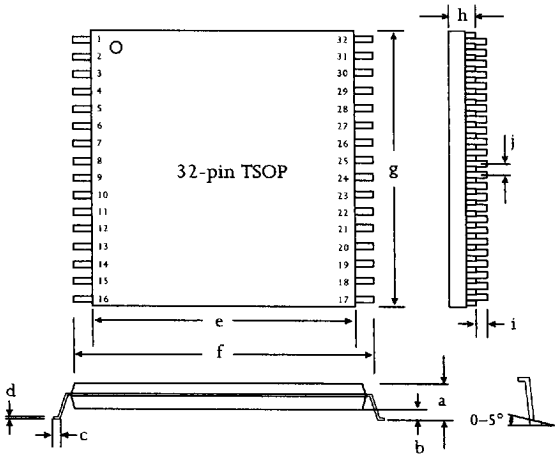


44-pin SO

	Min (mm)	Max (mm)
m	28.00	28.40
n	0.35	0.50
o	0.10	0.35
p	2.17	2.45
q		2.80
r	1.27	
s	13.10	13.50
t	15.70	16.30
u	0.06	1.00
w	0.10	0.21

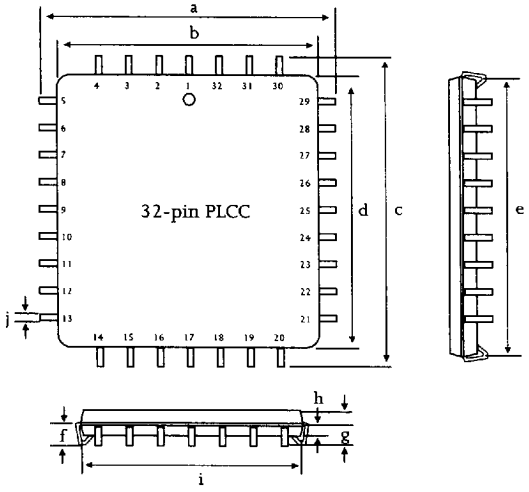
Flash

Package dimensions (continued)



32-pin TSOP

	min (mm)	max (mm)
a		1.20
b		0.25
c	0.5	0.7
d	0.1	0.21
e	18.30	18.50
f	19.80	20.20
g	7.90	8.10
h	0.95	1.05
i	0.05	0.15
j		0.50



32-pin PLCC

	typical (inch)
a	0.49
b	0.45
c	0.59
d	0.55
e	0.51
f	0.09
g	0.14
h	0.11
i	0.41
j	0.004

JEDEC outline	MS-016 AE
Body size	0.450 in. × 0.550 in.
Package thickness	0.110 in.
Board standoff	0.020 in. (min)
Lead pitch	0.050 in.
Coplanarity	0.004 in. (max)

AS29F002 ordering codes

Package \ Access time	55 ns	70 ns	90 ns	120 ns
TSOP, 10×20 mm, 40-pin	AS29F002B-55TC	AS29F002B-70TC AS29F002B-70TI	AS29F002B-90TC AS29F002B-90TI	AS29F002B-120TC AS29F002B-120TI
	AS29F002T-55TC	AS29F002T-70TC AS29F002T-70TI	AS29F002T-90TC AS29F002T-90TI	AS29F002T-120TC AS29F002T-120TI
PLCC, 0.55''×0.45'', 32-pin	AS29F002B-55LC	AS29F002B-70LC AS29F002B-70LI	AS29F002B-90LC AS29F002B-90LI	AS29F002B-120LC AS29F002B-120LI
	AS29F002T-55LC	AS29F002T-70LC AS29F002T-70LI	AS29F002T-90LC AS29F002T-90LI	AS29F002T-120LC AS29F002T-120LI
TSOP, 8×20 mm, 32-pin	AS29F002B-55T1C	AS29F002B-70T1C AS29F002B-70T1I	AS29F002B-90T1C AS29F002B-90T1I	AS29F002B-120T1C AS29F002B-120T1I
	AS29F002T1-55T1C	AS29F002T1-70T1C AS29F002T1-70T1I	AS29F002T1-90T1C AS29F002T1-90T1I	AS29F002T1-120T1C AS29F002T1-120T1I
PDIP, 600 mil wide, 32-pin	AS29F002B-55PC	AS29F002B-70PC AS29F002B-70PI	AS29F002B-90PC AS29F002B-90PI	AS29F002B-120PC AS29F002B-120PI
	AS29F002T-55PC	AS29F002T-70PC AS29F002T-70PI	AS29F002T-90PC AS29F002T-90PI	AS29F002T-120PC AS29F002T-120PI
SO, 600 mil wide, 44-pin	AS29F002B-55SC	AS29F002B-70SC AS29F002B-70SI	AS29F002B-90SC AS29F002B-90SI	AS29F002B-120SC AS29F002B-120SI
	AS29F002T-55SC	AS29F002T-70SC AS29F002T-70SI	AS29F002T-90SC AS29F002T-90SI	AS29F002T-120SC AS29F002T-120SI

AS29F002 part numbering system

AS29F	002	X	-XXX	X	C
Flash EEPROM prefix	Device number	B (bottom) or T (top) boot block	Address access time	Package: T = 40-pin TSOP L = 32-pin PLCC T1 = 32-pin TSOP P = 32-pin PDIP S = 44-pin SO	Temperature range C = Commercial, 0°C to 70 °C I = Industrial, -40°C to 85°C