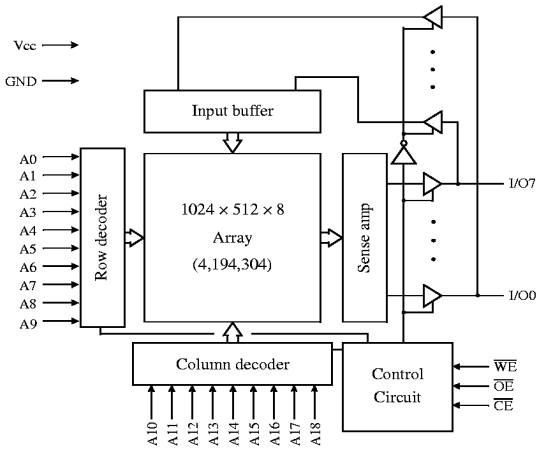
5V/3.3V 512K×8 CMOS SRAM

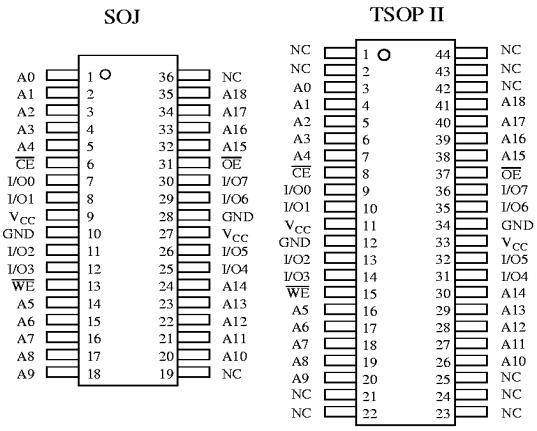
Features

- Organization: 524,288 words × 8 bits
- High speed
  - 12/15/20/25 ns address access time
  - 5/5/6/7 ns output enable access time
- Low power consumption
  - Active: 990 mW max (20 ns cycle, 5V)
  - Standby: 55 mW max (CMOS inputs)
  - Very low DC component in active power
- 2.0V data retention
- Equal access and cycle times
- Easy memory expansion with $\overline{CE}$, $\overline{OE}$ inputs
- TTL-compatible, three-state I/O
- JEDEC standard packages
  - 400 mil 36-pin SOJ
  - 400 mil 44-pin TSOP II
- Center power and ground pins for low noise
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA
- Industrial temperature range available (-40 to +85 ℃)
- 3.3V LVTTL version available (AS7C34096)

Logic block diagram



Pin arrangement



Selection guide

		7C4096-12 7C34096-12	7C4096-15 7C34096-15	7C4096-20 7C34096-20	7C4096-25 7C34096-25	Unit
Maximum address access time		12	15	20	25	ns
Maximum output enable access time		6	4	5	6	ns
Maximum operating current	AS7C4096	250	220	180	170	mA
	AS7C34096	200	170	120	110	mA
Maximum CMOS standby current		10	10	10	10	mA

Shaded areas indicate preliminary information.

Functional description

The AS7C4096 and AS7C34096 are high performance CMOS 4,194,304-bit Static Random Access Memories (SRAM) organized as 524,288 words × 8 bits. They are designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times (t_{AA}, t_{RC}, t_{WC}) of 12/15/20/25 ns with output enable access times (t_{OE}) of 5/5/6/7 ns are ideal for high performance applications. The chip enable input $\overline{CE}$ permits easy memory expansion with multiple-bank memory systems.

When $\overline{CE}$ is HIGH the device enters standby mode. The AS7C4096 is guaranteed not to exceed 55 mW power consumption in CMOS standby mode. Both devices offer 2.0V data retention.

A write cycle is accomplished by asserting write enable ($\overline{WE}$) and chip enable ($\overline{CE}$). Data on the input pins I/O0-I/O7 is written on the rising edge of $\overline{WE}$ (write cycle 1) or $\overline{CE}$ (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting output enable ($\overline{OE}$) and chip enable ($\overline{CE}$), with write enable ($\overline{WE}$) HIGH. The chip drives I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

All chip inputs and outputs are TTL-compatible, and operation is from a single supply voltage. Both devices are available in the industry standard 400-mil 36-pin SOJ and 44-pin TSOP II packages.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Voltage on any input pin relative to GND (7C4096)	V_t	–0.5	+7.0	V
Voltage on any input pin relative to GND (7C34096)	V_t	–0.5	+5.5	V
Voltage on any I/O pin	V_t	–0.5	V_{CC} + 0.5	V
Power dissipation	P_D	–	1.0	W
Storage temperature	T_{stg}	–55	+150	°C
DC output current	I_{out}	–	20	mA

Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Data	Mode
H	X	X	High-Z	Standby (I_{SB}, I_{SB1})
L	H	H	High-Z	Output disable
L	H	L	D_{out}	Read
L	L	X	D_{in}	Write

Key: X = Don't Care, L = Low, H = High

Capacitance

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	A, $\overline{CE}$, $\overline{WE}$, $\overline{OE}$	V_{in} = 0V	5	pF
I/O capacitance	$C_{I/O}$	I/O	V_{in} = V_{out} = 0V	7	pF

Recommended operating condition

Parameter		Symbol	Min	Nominal	Max	Unit
Supply voltage	AS7C4096	V_{CC}	4.5	5.0	5.5	V
	AS7C34096	V_{CC}	3.0	3.3	3.6	V
		GND	0.0	0.0	0.0	V
Input voltage	AS7C4096	V_{IH}	2.2	–	V_{CC} + 0.5	V
	AS7C34096	V_{IH}	2.0	–	V_{CC} + 0.5	V
		V_{IL}	–0.5†	–	0.8	V
Ambient operating temperature	Commercial	T_A	0	–	70	℃
	Industrial	T_A	-40	–	85	℃

† V_{IL} min = –3.0V for pulse width less than $t_{RC}/2$.

DC operating characteristics

				-12		-15		-20		-25		
Parameter	Symbol	Test conditions		Min	Max	Min	Max	Min	Max	Min	Max	Unit
Input leakage current	$\lvert I_{LI} \rvert$	V_{CC} = Max, V_{in} = GND to V_{CC}		–	2	–	2	–	2	–	2	µA
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CE}$ = V_{IH}, V_{CC} = Max, V_{out} = GND to V_{CC}		–	5	–	5	–	5	–	5	µA
Operating power supply current	I_{CC}	$\overline{CE}$ = V_{IL} f = f_{max}, I_{out} = 0 mA	AS7C4096	–	250	–	220	–	180	–	170	mA
			AS7C34096	–	200	–	170	–	120	–	110	
Standby power supply current	I_{SB}	$\overline{CE}$ = V_{IH} f = f_{max}		–	60	–	60	–	60	–	60	mA
	I_{SB1}	$\overline{CE}$ ≥ V_{CC}–0.2V, V_{in} ≤ 0.2V or V_{in} ≥ V_{CC}–0.2V, f = 0		–	10	–	10	–	10	–	10	mA
Output voltage	V_{OL}	I_{OL} = 8 mA, V_{CC} = Min		–	0.4	–	0.4	–	0.4	–	0.4	V
	V_{OH}	I_{OH} = –4 mA, V_{CC} = Min		2.4	–	2.4	–	2.4	–	2.4	–	V

Shaded areas indicate preliminary information.

SRAM

Read cycle [3,9]

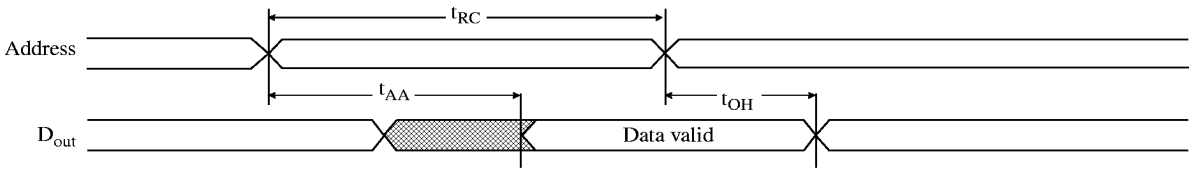
		-12		-15		-20		-25			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Read cycle time	t_{RC}	12	–	15	–	20	–	25	–	ns	
Address access time	t_{AA}	–	12	–	15	–	20	–	25	ns	3
Chip enable ($\overline{CE}$) access time	t_{ACE}	–	12	–	15	–	20	–	25	ns	3
Output enable ($\overline{OE}$) access time	t_{OE}	–	5	–	5	–	6	–	7	ns	
Output hold from address change	t_{OH}	3	–	3	–	3	–	3	–	ns	5
$\overline{CE}$ Low to output in Low Z	t_{CLZ}	0	–	0	–	0	–	0	–	ns	4, 5
$\overline{CE}$ High to output in High-Z	t_{CHZ}	–	3	–	4	–	5	–	6	ns	4, 5
$\overline{OE}$ Low to output in Low Z	t_{OLZ}	0	–	0	–	0	–	0	–	ns	4, 5
$\overline{OE}$ High to output in High-Z	t_{OHZ}	–	3	–	4	–	5	–	6	ns	4, 5
Power up time	t_{PU}	0	–	0	–	0	–	0	–	ns	4, 5
Power down time	t_{PD}	–	12	–	15	–	20	–	25	ns	4, 5

Shaded areas indicate preliminary information.

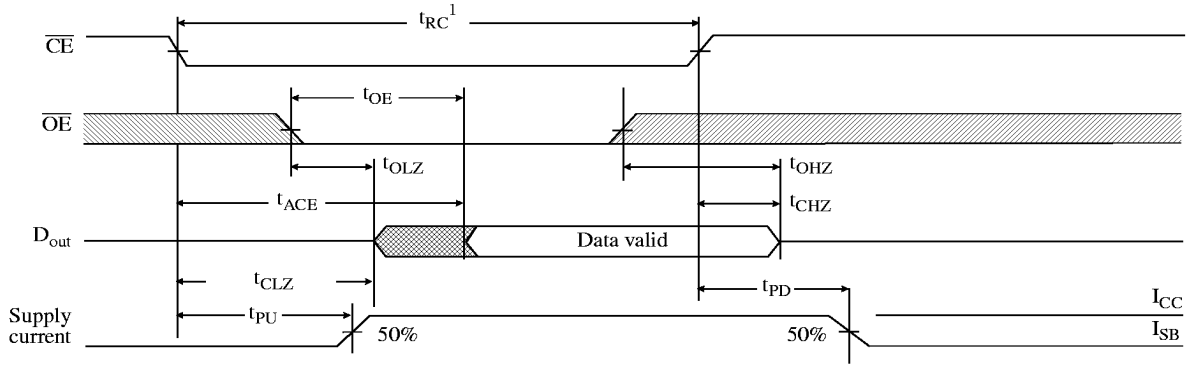
Key to switching waveforms

Rising input Falling input Undefined output/don't care

Read waveform 1 [3,6,7,9]



Read waveform 2 [3,6,8,9]

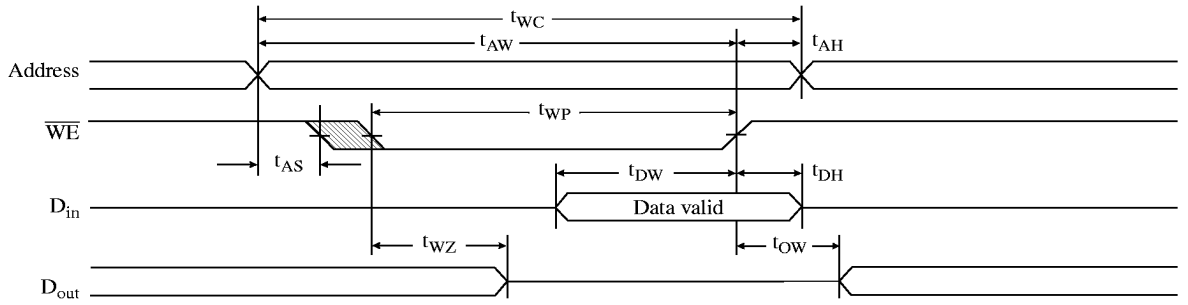


Write cycle [11]

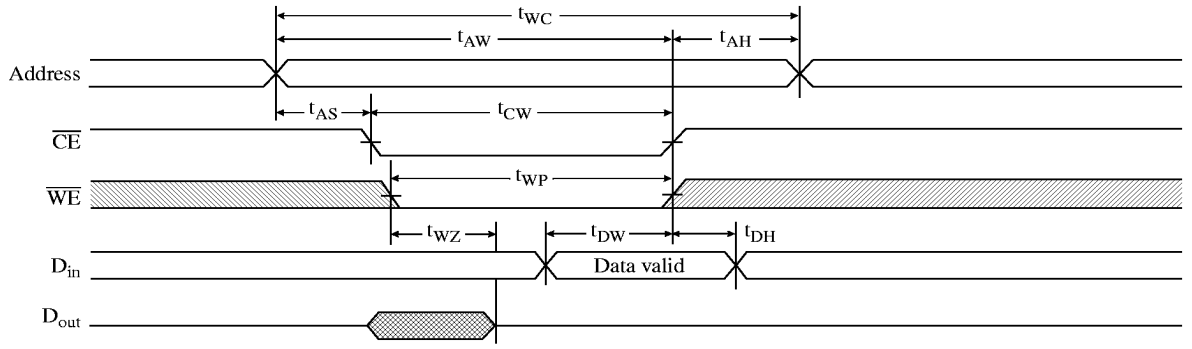
		-12		-15		-20		-25			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Write cycle time	t_{WC}	12	–	15	–	20	–	20	–	ns	
Chip enable ($\overline{CE}$) to write end	t_{CW}	10	–	12	–	12	–	15	–	ns	
Address setup to write end	t_{AW}	10	–	12	–	12	–	15	–	ns	
Address setup time	t_{AS}	0	–	0	–	0	–	0	–	ns	
Write pulse width	t_{WP}	8	–	9	–	12	–	15	–	ns	
Address hold from end of write	t_{AH}	0	–	0	–	0	–	0	–	ns	
Data valid to write end	t_{DW}	6	–	9	–	10	–	10	–	ns	
Data hold time	t_{DH}	0	–	0	–	0	–	0	–	ns	4, 5
Write enable to output in High-Z	t_{WZ}	–	5	–	5	–	5	–	5	ns	4, 5
Output active from write end	t_{OW}	1	–	1	–	1	–	1	–	ns	4, 5

Shaded areas indicate preliminary information.

Write waveform 1 [10,11]



Write waveform 2 [10,11]

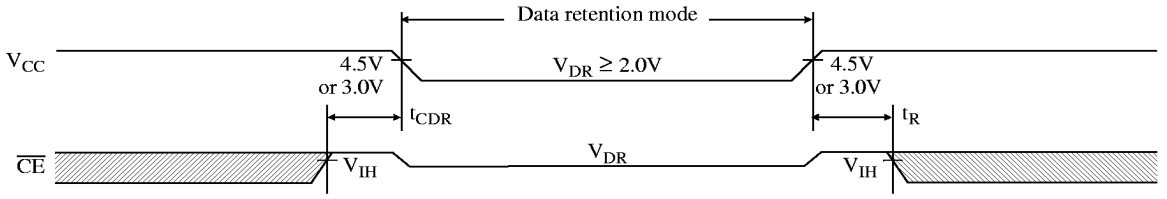


SRAM

Data retention characteristics [13]

Parameter	Symbol	Test conditions	Min	Max	Unit
V_{CC} for data retention	V_{DR}	V_{CC} = 2.0V $\overline{CE} \geq V_{CC}-0.2V$ $V_{in} \geq V_{CC}-0.2V$ or $V_{in} \leq 0.2V$	2.0	–	V
Data retention current	I_{CCDR}		–	500	µA
Chip deselect to data retention time	t_{CDR}		0	–	ns
Operation recovery time	t_R		t_{RC}	–	ns
Input leakage current	$\lvert I_{LI} \rvert$		–	1	µA

Data retention waveform



AC test conditions

- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 5 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

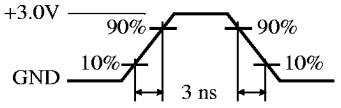


Figure A: Input pulse

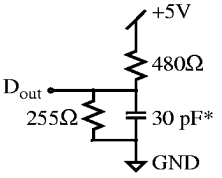


Figure B: 5V Output load

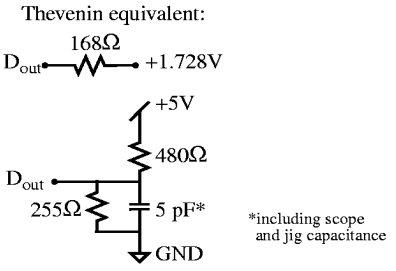


Figure C: 5V Output load for t_{CLZ}, t_{CHZ}, t_{OLZ}, t_{OHZ}, t_{WZ}

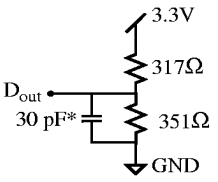


Figure D: 3.3V Output load

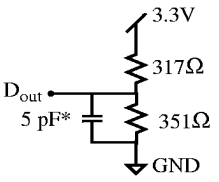


Figure E: 3.3V Output load for t_{CLZ}, t_{CHZ}, t_{OLZ}, t_{OHZ}, t_{WZ}

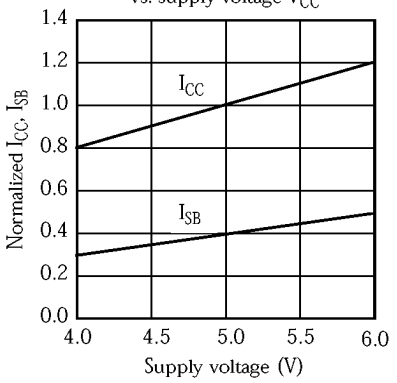
Notes

1 During V_{CC} power-up, a pull-up resistor to V_{CC} on $\overline{CE}$ is required to meet I_{SB} specification.
2 This parameter is sampled and not 100% tested.
3 For test conditions, see AC *Test Conditions*.
4 t_{CLZ} and t_{CHZ} are specified with C_L = 5pF as in Figure C. Transition is measured ±500mV from steady-state voltage.
5 This parameter is guaranteed but not tested.
6 $\overline{WE}$ is HIGH for read cycle.
7 $\overline{CE}$ and $\overline{OE}$ are LOW for read cycle.
8 Address valid prior to or coincident with $\overline{CE}$ transition Low.
9 All read cycle timings are referenced from the last valid address to the first transitioning address.
10 $\overline{CE}$ or $\overline{WE}$ must be HIGH during address transitions.
11 All write cycle timings are referenced from the last valid address to the first transitioning address.
12 This data is applicable to the AS7C4096 only. the AS7C34096 functions similarly.
13 2V data retention applies to commercial temperature range operation only.

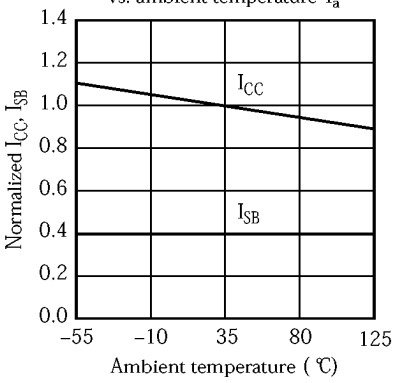
SRAM

Typical DC and AC characteristics [12]

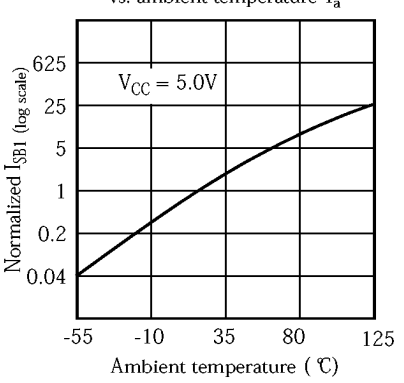
Normalized supply current I_{CC}, I_{SB} vs. supply voltage V_{CC}



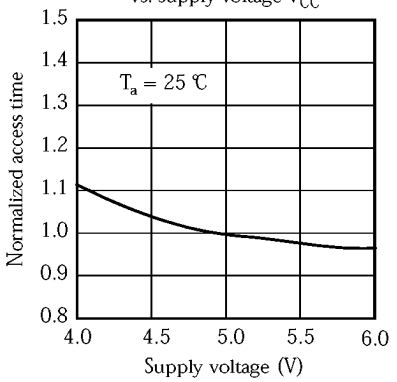
Normalized supply current I_{CC}, I_{SB} vs. ambient temperature T_a



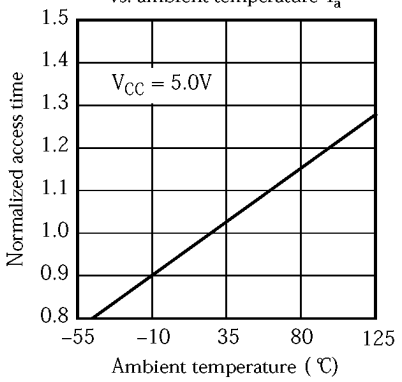
Normalized supply current I_{SB1} vs. ambient temperature T_a



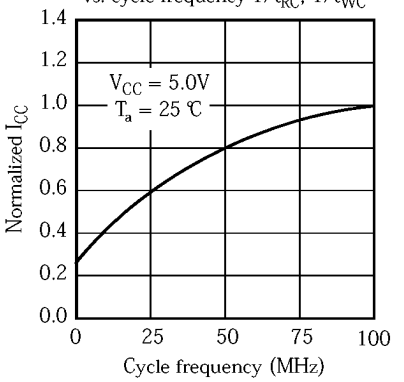
Normalized access time t_{AA} vs. supply voltage V_{CC}



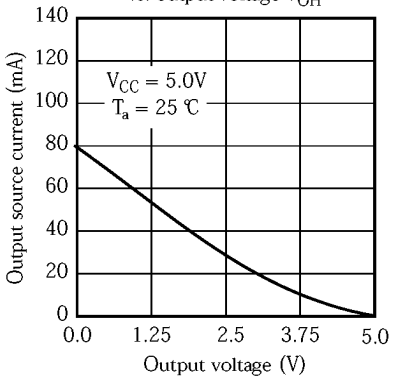
Normalized access time t_{AA} vs. ambient temperature T_a



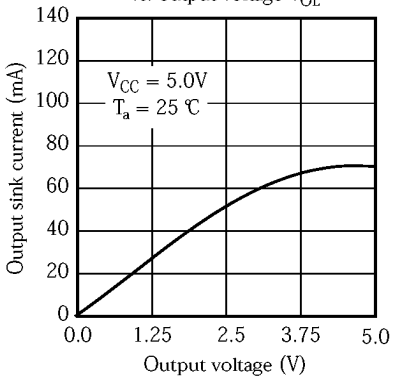
Normalized supply current I_{CC} vs. cycle frequency $1/t_{RC}$, $1/t_{WC}$



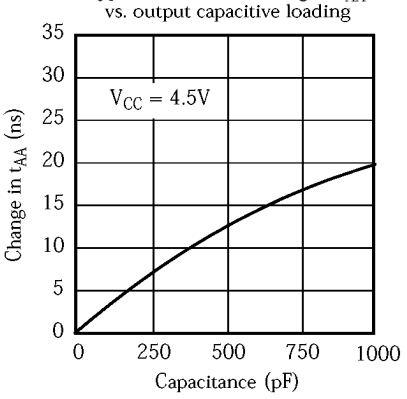
Output source current I_{OH} vs. output voltage V_{OH}



Output sink current I_{OL} vs. output voltage V_{OL}



Typical access time change Δt_{AA} vs. output capacitive loading



AS7C4096 ordering codes

Package	Version		12 ns	15 ns	20 ns	25 ns
SOJ	Commercial temperature	5V	AS7C4096-12JC	AS7C4096-15JC	AS7C4096-20JC	AS7C4096-25JC
		3.3V	AS7C34096-12JC	AS7C34096-15JC	AS7C34096-20JC	AS7C34096-25JC
	Industrial temperature	5V	AS7C4096-12JI	AS7C4096-15JI	AS7C4096-20JI	AS7C4096-25JI
		3.3V	AS7C34096-12JI	AS7C34096-15JI	AS7C34096-20JI	AS7C34096-25JI
TSOP II	Commercial temperature	5V	AS7C4096-12TC	AS7C4096-15TC	AS7C4096-20TC	AS7C4096-25TC
		3.3V	AS7C34096-12TC	AS7C34096-15TC	AS7C34096-20TC	AS7C34096-25TC
	Industrial temperature	5V	AS7C4096-12TI	AS7C4096-15TI	AS7C4096-20TI	AS7C4096-25TI
		3.3V	AS7C34096-12TI	AS7C34096-15TI	AS7C34096-20TI	AS7C34096-25TI

Shaded areas indicate preliminary information.

AS7C4096 part numbering system

AS7C	X	4096	–XX	X	X
SRAM prefix	Blank = 5V CMOS 3 = 3.3V CMOS	Device number	Access time	Package: J = SOJ 400 mil T = TSOP II 400 mil	Temperature range, C = Commercial: 0 ℃ to 70 ℃ I = Industrial: -40 ℃ to 85 ℃