

AT209S
PCI Arbiter and Clock Buffer

Preliminary Specification

Release Date: Dec. 2000

1. General Description

The AT209S is an integrated device that contains a PCI Arbiter and a Clock Buffer. PCI Arbiter extends system PCI devices without piecing other circuit to simplify design complexity and increase system's stability.

PCI Arbiter also provides STOP# input pin with that extended PCI devices instruct the master to prematurely end the transaction on the current data phase same as one in PCI specification.

Clock Buffer is a high performance and low jitter zero delay buffer that provides synchronization between the input and output. The synchronization is established via CLK0 feed back to the input of a build-in PLL.

PCICLK1 is the clock input of the Clock Buffer. In the absence of PCICLK1 input, will be in the power down mode. In this mode, the PLL is turned off and the output buffers are pulled low. Power down mode provides the lowest power consumption for a standby condition.

2. Features

- PCI Arbiter
 - Extend PCI Devices from one to three
- PCI Clock Frequency
 - Support PCI Clock range from 25MHz to 66MHz
- Zero delay buffer
 - Generate four zero delay clock sources
 - Support frequency range from 25MHz to 66MHz

3. Pin Configuration

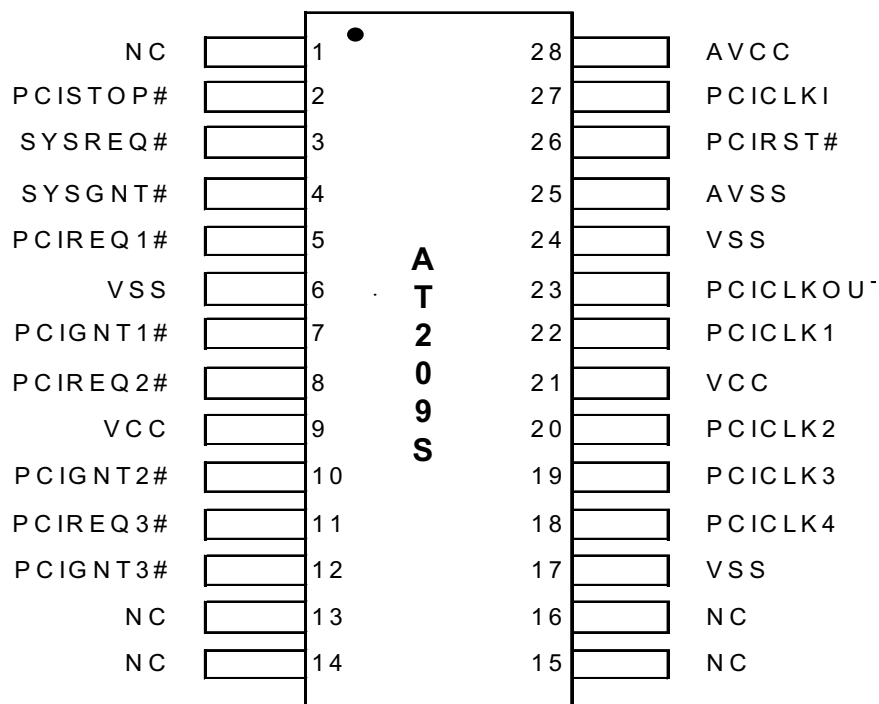
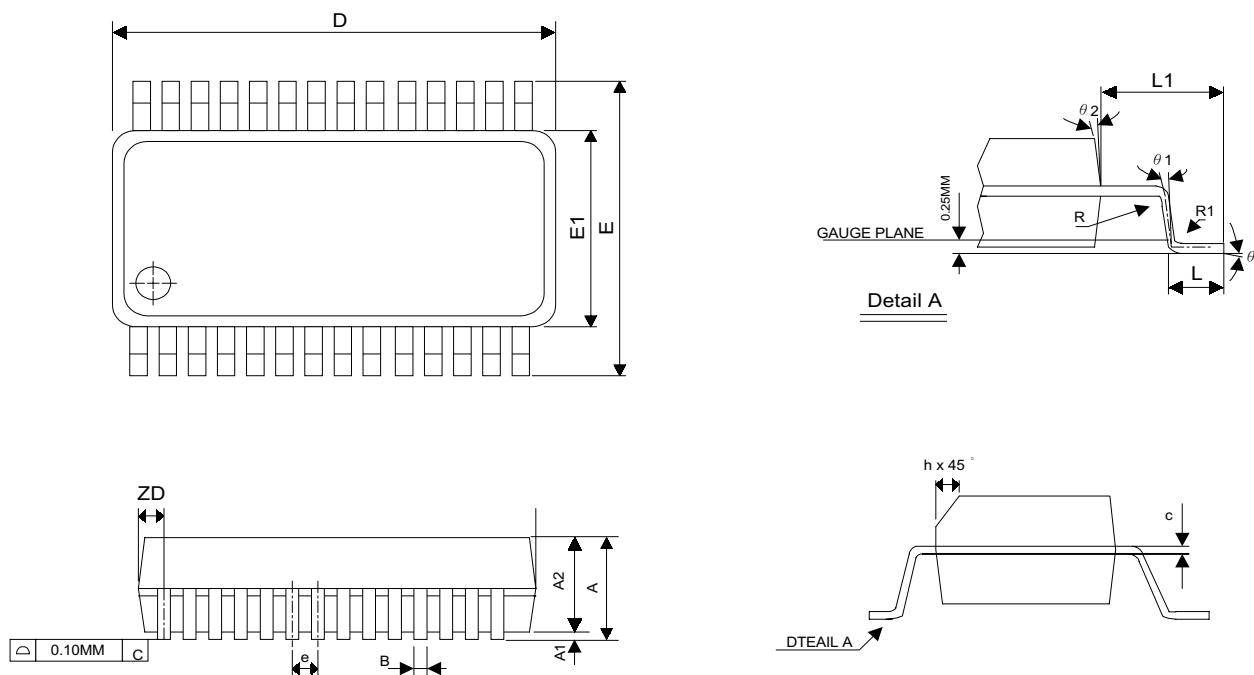


Figure 1. AT209S Pin Diagram (Top View)

4. Package Information SSOP28pin Outline Dimension



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	1.35	1.63	1.75	0.053	0.064	0.069
A1	0.10	0.15	0.25	0.004	0.006	0.010
A2			0.50			0.059
B	0.20		0.30	0.008		0.012
c	0.18		0.25	0.007		0.010
E	0.635 BASIC			0.025 BASIC		
D	9.80	9.91	10.01	0.386	0.390	0.394
E	5.79	5.99	6.20	0.228	0.236	0.244
E1	3.81	3.91	3.99	0.150	0.154	0.157
L	0.41	0.635	1.27	0.016	0.025	0.050
H	0.25		0.50	0.010		0.020
ZD	0.838 REF			0.033 REF		
R1	0.20		0.33	0.008		0.013
R	0.20			0.008		
θ	0°		8°	0°		8°
$\theta 1$	0°			0°		
$\theta 2$	5°	10°	15°	5°	10°	15°
JEDEC	MO-137 (AF)					



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