Rockwell

R68C552 Dual Asynchronous Communications Interface Adapter (DACIA)

DESCRIPTION

The Rockwell CMOS R68C552 Dual Asynchronous Communications Interface Adapter (DACIA) provides an easily implemented, program controlled two-channel interface between 16-bit microprocessor-based systems and serial communication data sets and modems.

The DACIA is designed for maximum programmed control from the microprocessor (MPU) to simplify hardware implementation. Dual sets of registers allow independent control and monitoring of each channel.

Transmitter and Receiver bit rates may be controlled by an internal baud rate generator or external times 16 clocks. The baud rate generator accepts either a crystal or a clock input, and provides 15 programmable baud rates. When a 3.6864 MHz crystal is used, the baud rates range from 50 bps to 38,400 bps.

The DACIA may be programmed to transmit and receive frames having word lengths of 5, 6, 7 or 8 bits; even, odd, space, mark or no parity; and 1 or 2 stop bits.

A Compare Register, and the ability to detect address frames, facilitate address recognition in a multidrop mode.

FEATURES

- Low power CMOS N-well silicon gate technology
- Two independent full duplex channels with buffered receivers and transmitters.
- Data set/modem control functions
- Internal baud rate generator with 15 programmable baud rates (50 bps to 38,400 bps)
- Program-selectable internally or externally controlled receiver and transmitter bit rates
- Programmable word lengths, number of stop bits, and parity bit generation and detection
- Programmable interrupt control
- Edge detect for $\overline{DCD}$, $\overline{DSR}$, and $\overline{CTS}$
- Program-selectable echo mode for each channel
- Compare Register
- Address/Data frame recognition
- 5.0 Vdc ±5% supply requirements
- 40-pin plastic or ceramic DIP or 44-pin PLCC
- Full TTL or CMOS input/output compatibility
- Compatible with R68000 microprocessors

ORDERING INFORMATION

Part Number:
R68C552 _ _

- Temperature Range (T_L to T_H):
  - Blank = 0°C to +70°C
  - E = −40°C to +85°C
- Package:
  - C = 40-Pin Ceramic DIP
  - P = 40-Pin Plastic DIP
  - J = 44-Pin Plastic Leaded Chip Carrier (PLCC)

INTERFACE SIGNALS

The DACIA is available in a 40-pin DIP or a 44-pin PLCC. Figure 1 shows the pin assignments for each package. The DACIA interface signals are shown in Figure 2. Table 1 contains a description of each signal.

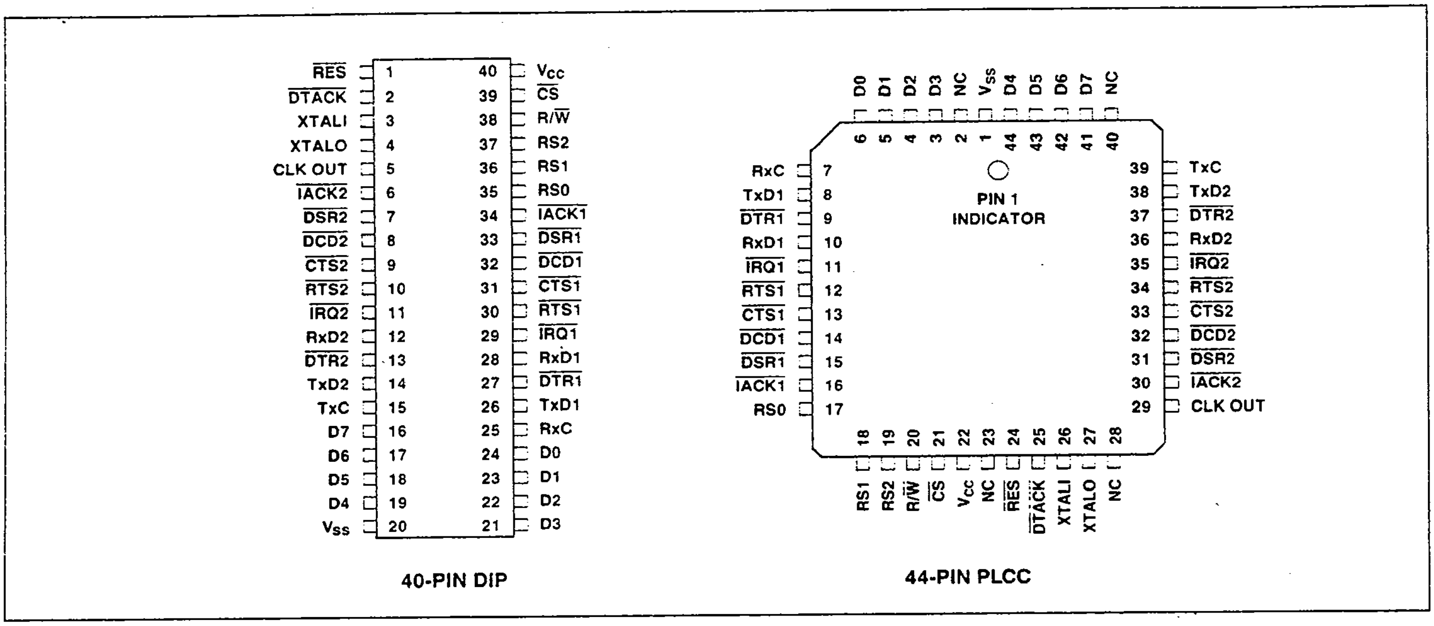


Figure 1. R68C552 Pin Assignments

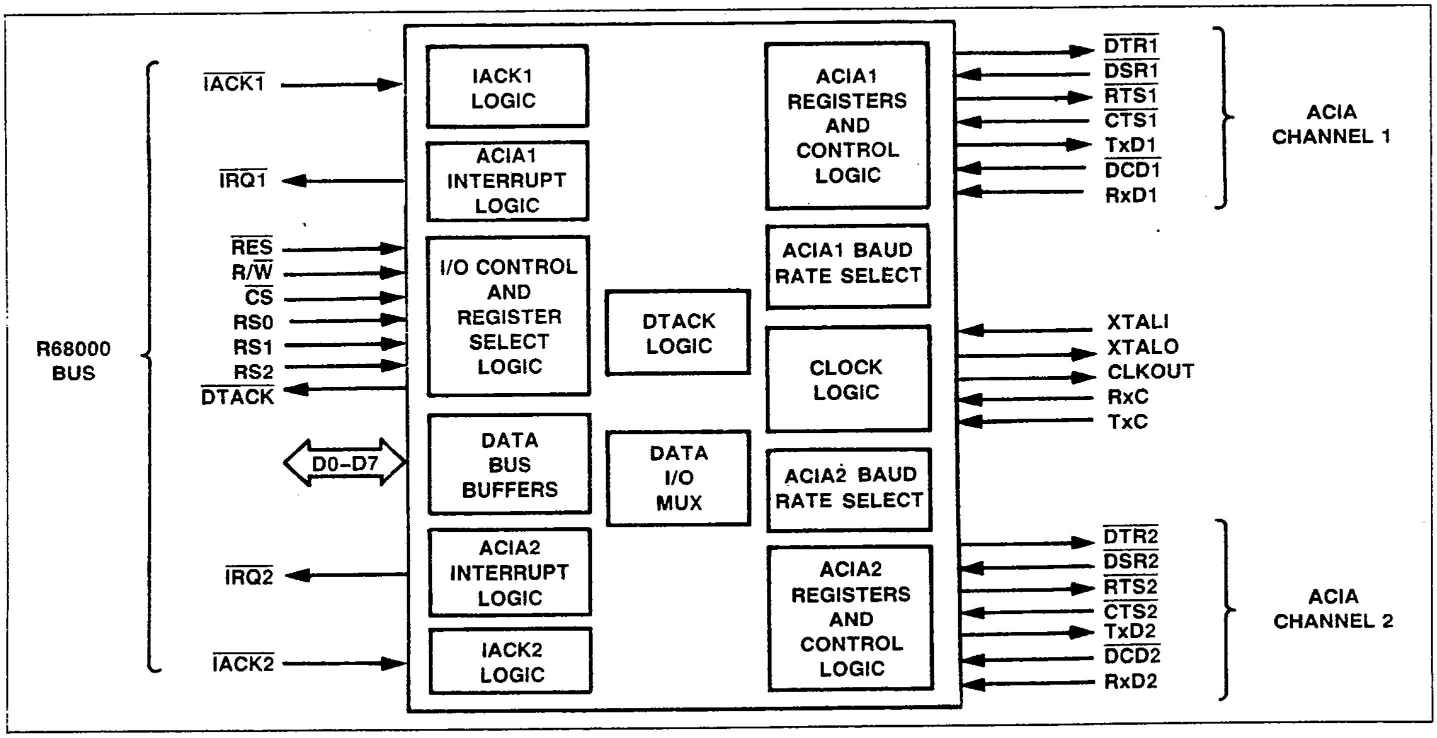


Figure 2. R68C552 DACIA Interface Signals

7811073 0017444 854 RKW

Table 1. DACIA Interface Signal Definitions

Signal	Pin No. DIP	Pin No. PLCC	I/O	Name/Description
Host Interface				
$\overline{RES}$	1	24	I	**Reset.** Active low input controlling the reset function. This signal must be driven low for a minimum of 4 μs for a valid reset to occur. It is driven high during normal operation.
R/$\overline{W}$	38	20	I	**Read/Write.** Input controlling the direction of data transfer. It is driven low during write cycles, and is driven high at all other times.
$\overline{CS}$	39	21	I	**Chip Select.** Active low input enabling data transfers between the host CPU and the DACIA. The DACIA latches register selects and the R/$\overline{W}$ input on the falling edge of $\overline{CS}$. It latches input data on the rising edge of $\overline{CS}$.
RS0-RS3	35-37	17-19	I	**Register Select.** Three inputs controlling access to the DACIA internal registers. Table 3 lists the coding for each register.
D0-D3 D4-D7	24-21 19-16	6-3 44-41	I/O	**Data Bus.** Eight bidirectional lines used to transfer data between the host and the DACIA. These lines output data during READ cycles when $\overline{CS}$ is low and they output the interrupt vector during INTERRUPT ACKNOWLEDGE cycles when $\overline{IACK1}$ or $\overline{IACK2}$ is low. At all other times, they are in the high impedence state.
$\overline{DTACK}$	2	25	O	**Data Transfer Acknowledge.** Active low open drain output generated in response to $\overline{CS}$, $\overline{IACK1}$ and $\overline{IACK2}$ during asynchronous data transfers. $\overline{DTACK}$ goes to the high impedence state when $\overline{CS}$, $\overline{IACK1}$ and $\overline{IACK2}$ are high.
$\overline{IRQ1}$ $\overline{IRQ2}$	29 11	11 35	O	**Interrupt Request.** Two active low, open-drain outputs from the interrupt control logic. These outputs are normally high. An $\overline{IRQ}$ line goes low when one of the flags of the associated ISR is set if the corresponding enable bit is set in the IER.
$\overline{IACK1}$ $\overline{IACK2}$	34 6	16 30	I	**Interrupt Acknowledge.** Two active low inputs indicating that an INTERRUPT ACKNOWLEDGE cycle is in progress. When an $\overline{IACK}$ goes low, the DACIA places the interrupt vector for the associated channel on the data bus and issues $\overline{DTACK}$.
Clock Interface				
XTALI XTALO	3 4	26 27	I O	**Crystal Input/Output.** One input and one output through which the reference signal for the internal clock oscillator is supplied. A parallel resonant crystal may be connected across the pins or a clock may be input at XTALI. When a clock is used, XTALO must be left open.
CLK OUT	5	29	O	**Clock Out.** A buffered output from the internal clock oscillator which is in phase with XTALI. This output may be used to drive the XTALI input of another DACIA. Therefore, several DACIA chips may be driven with one crystal.
RxC	25	7	I	**Receiver Clock.** Input for external 16x receiver clock.
TxC	15	39	I	**Transmitter Clock.** Input for external 16x transmitter clock.
Serial Channel Interface				
$\overline{DTR1}$ $\overline{DTR2}$	27 13	9 37	O	**Data Terminal Ready.** Two general purpose outputs which are set high upon reset. The output level is programmed by setting the appropriate bit in the associated Format Register (FR) high or low. The state of each $\overline{DTR}$ line is reflected by the $\overline{DTR}$ LVL bit in the associated Control Status Register (CSR).
$\overline{DSR1}$ $\overline{DSR2}$	33 7	15 31	I	**Data Set Ready.** Two general purpose inputs. An active transition sets the $\overline{DSRT}$ bit in the Interrupt Status Register (ISR). The $\overline{DSR}$ LVL bit in the associated CSR reflects the current state of a $\overline{DSR}$ line.
$\overline{RTS1}$ $\overline{RTS2}$	30 10	12 34	O	**Request To Send.** Two general purpose outputs which are set high upon reset. The output level is programmed by setting the appropriate bit in the associated FR high or low. The state of an $\overline{RTS}$ line is reflected by the $\overline{RTS}$ LVL bit in the associated CSR.
$\overline{CTS1}$ $\overline{CTS2}$	31 9	13 33	I	**Clear To Send.** The $\overline{CTS}$ control line inputs allow handshaking by the transmitters. When $\overline{CTS}$ is low, the data is transmitted continuously. When $\overline{CTS}$ is high, the Transmit Data Register Empty bit (TDRE) in the associated ISR is not set. The word presently in the Transmit Shift Register is sent normally. Any active transition on a $\overline{CTS}$ line sets the $\overline{CTST}$ bit in the appropriate ISR. The $\overline{CTS}$ LVL bit in the associated CSR reflects the current state of $\overline{CTS}$.
TxD1 TxD2	26 14	8 38	O	**Transmit Data.** The TxD outputs transfer serial non-return to zero (NRZ) data to the data communications equipment (DCE). The data is transferred, LSB first, at a rate determined by the baud rate generator or external clock.
$\overline{DCD1}$ $\overline{DCD2}$	32 8	14 32	I	**Data Carrier Detect.** Two general purpose inputs. An active transition sets the $\overline{DCDT}$ bit in the appropriate ISR. The $\overline{DCD}$ LVL bit in the associated CSR reflects the current state of a $\overline{DCD}$ line.
RxD1 RxD2	28 12	10 36	I	**Receive Data.** The RxD inputs transfer serial NRZ data into the DACIA from the DCE, LSB first. The receiver baud rate is determined by the baud rate generator or external clock.
Power				
VCC	40	22	I	**DC Power Input.** 5.0V ± 5%.
VSS	20	1	I	**Power and Signal Reference.**

FUNCTIONAL DESCRIPTION

Figure 3 is a block diagram of the DACIA which consists of two asynchronous communications interface adapters with common microprocessor interface control logic and data bus buffers. The individual functional elements of the DACIA are described in the following paragraphs.

RESET LOGIC

The Reset Logic sets various internal registers, status bits and control lines to a known state. The $\overline{\text{RES}}$ input must be driven low for a minimum of 4 μs for a valid reset to occur. At this time, the IERs are set to \$80, the RDRs and ACRs are cleared, and the compare mode is disabled. Also, the $\overline{\text{DTR}}$ and $\overline{\text{RTS}}$ outputs are driven high and the $\overline{\text{CTS}}$, $\overline{\text{DCD}}$ and $\overline{\text{DSR}}$ transition detect flags are cleared. No other bits are affected.

DATA BUS BUFFER

The Data Bus Buffer is a bidirectional interface between the data lines and the internal data bus. The state of the Data Bus Buffer is controlled by the I/O Control Logic and the Interrupt Logic. Table 2 summarizes the Data Bus Buffer states.

I/O CONTROL LOGIC

The I/O Control Logic controls data transfers between the Internal Registers and the Data Bus Buffer. Internal Register selection is determined by the Register Select inputs as shown in Table 3. When R/$\overline{\text{W}}$ is high and $\overline{\text{CS}}$ is low, data from the selected register is transferred from the internal data bus to the data lines and $\overline{\text{DTACK}}$ is asserted. When $\overline{\text{CS}}$ is high, the DACIA is deselected if the $\overline{\text{IACK}}$ inputs are high and the data lines are tri-stated.

INTERRUPT LOGIC

The interrupt logic causes the $\overline{\text{IRQ}}$ lines ($\overline{\text{IRQ1}}$ or $\overline{\text{IRQ2}}$) to go low when conditions are met that require the attention of the MPU. There are two registers (the Interrupt Enable Register and the Interrupt Status Register) involved in the control of interrupts in the DACIA. An $\overline{\text{IRQ}}$ will be asserted *on the transition* of one of the flags in an ISR from 0 to 1 if the corresponding bit in the associated IER is set. The $\overline{\text{IRQ}}$ line is negated when the ISR is read or when the interrupting condition is cleared. CAUTION: When the interrupt is generated by TDRE, 1/16 of a bit time must elapse before $\overline{\text{IRQ}}$ can be cleared by reading the ISR.

When an $\overline{\text{IACK}}$ input goes low in response to an $\overline{\text{IRQ}}$, the following occurs if $\overline{\text{CS}}$ and R/$\overline{\text{W}}$ are high: D0 goes low if the $\overline{\text{IRQ}}$ is generated by TDR empty or RDR full. D0 goes high for all other interrupt sources. TDRE and RDRF interrupts have priority over all other interrupt sources. D1 goes low when the interrupt request is from Channel 1. It goes high if the $\overline{\text{IRQ}}$ is from Channel 2. D2 through D7 outputs the Interrupt Vector Number stored in bits 2 through 7 of the Auxiliary Control Register. $\overline{\text{DTACK}}$ is asserted.

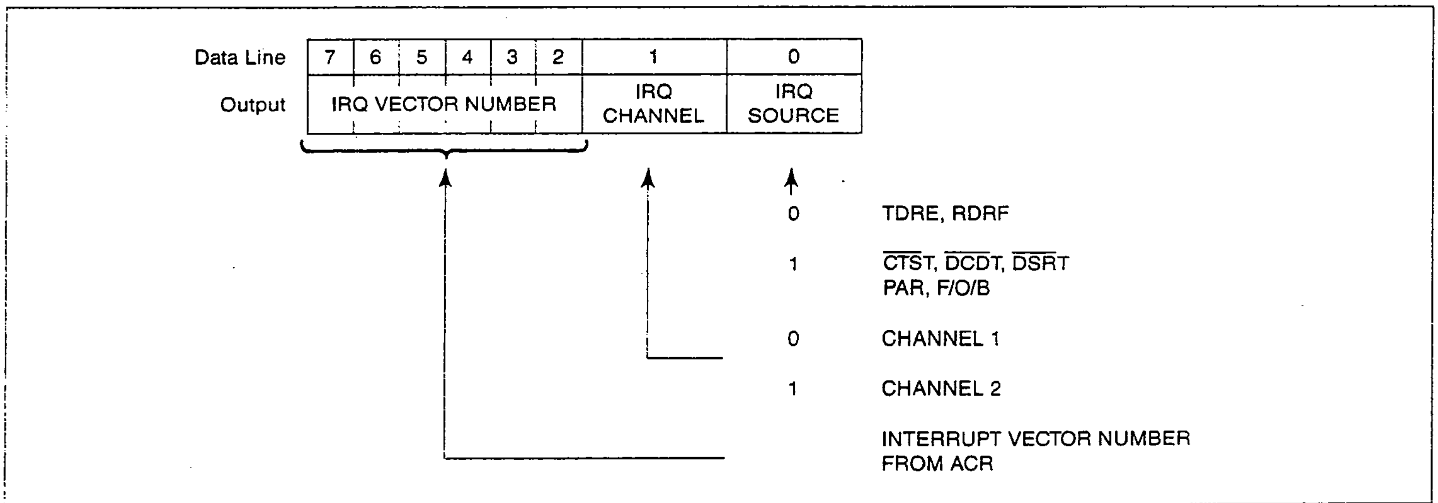
CLOCK OSCILLATOR LOGIC

The internal clock oscillator supplies the time base for the baud rate generator. The oscillator can be driven by a crystal or an external clock.

The baud rate generator may be disabled by connecting XTALI to ground and leaving XTALO open. When this is done, a transmitter times 16 clock must be input at TxC, a receiver times 16 clock must be input at RxC and the Control Registers must be programmed to select TxC and RxC clocks.

Table 2. Data Bus Buffer Summary

Control Signals R/$\overline{\text{W}}$	$\overline{\text{CS}}$	$\overline{\text{IACK1}}$	$\overline{\text{IACK2}}$	Data Bus Buffer State
L	L	L	L	Illegal Mode — Tri-State
L	L	L	H	Illegal Mode — Tri-State
L	L	H	L	Illegal Mode — Tri-State
L	L	H	H	Write Mode — Tri-State
L	H	L	L	Illegal Mode — Tri-State
L	H	L	H	Illegal Mode — Tri-State
L	H	H	L	Illegal Mode — Tri-State
L	H	H	H	Tri-State
H	L	L	L	Illegal Mode — Output \$0F
H	L	L	H	Illegal Mode — Output \$0F
H	L	H	L	Illegal Mode — Output \$0F
H	L	H	H	Read Mode — Output Data
H	H	L	L	Illegal Mode — Output \$0F
H	H	L	H	Output IRQ Vector 1
H	H	H	L	Output IRQ Vector 2
H	H	H	H	Tri-State



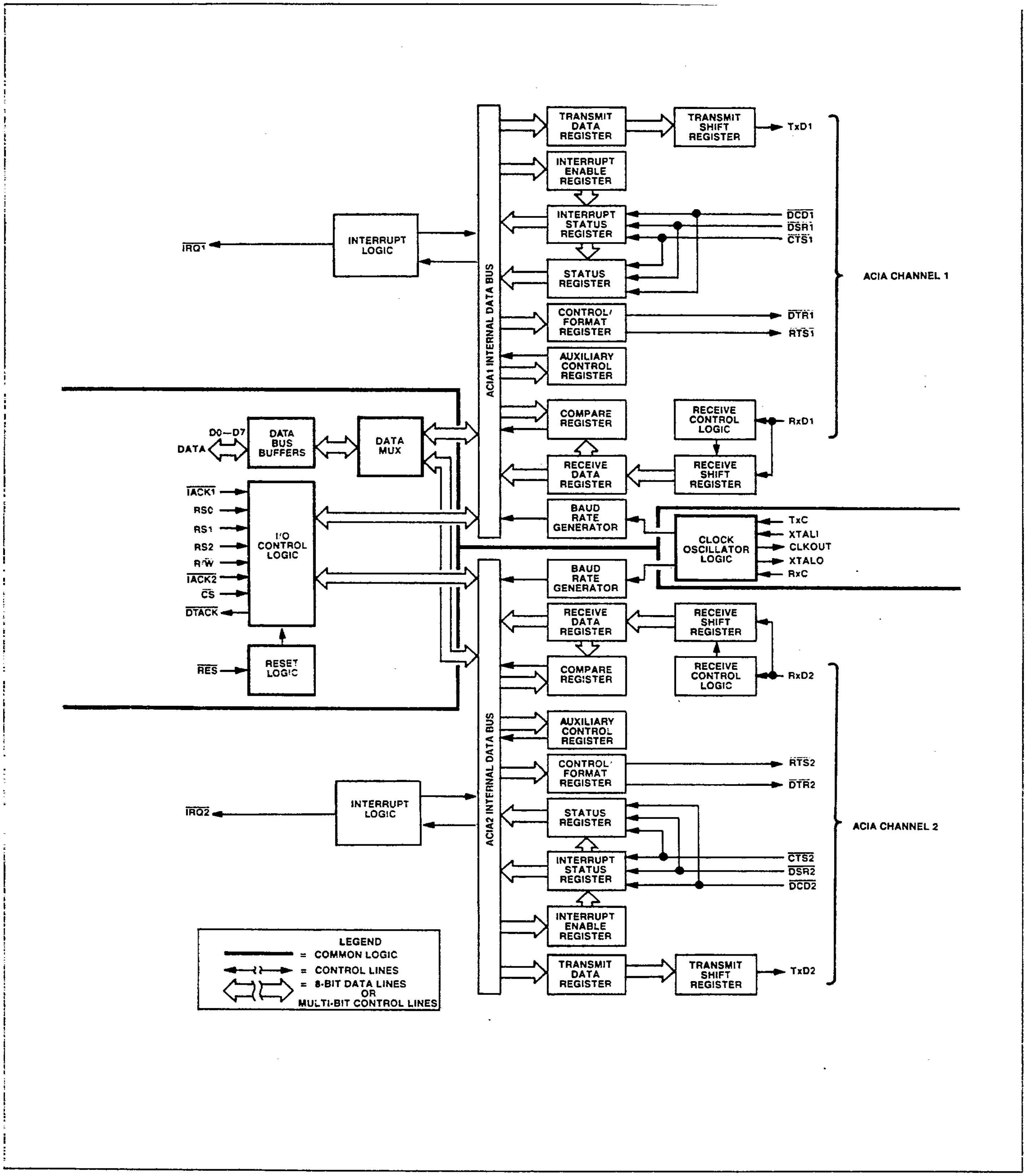


Figure 3. DACIA Block Diagram

Table 3. DACIA Register Selection

Register Select Lines				Register Accessed			
				Write		Read	
HEX	RS2	RS1	RS0	Symbol	Name	Symbol	Name
0	L	L	L	IER1	Interrupt Enable Register 1	ISR1	Interrupt Status Register 1
1	L	L	H	CR1	Control Register 1[1]	CSR1	Control Status Register 1
				FR1	Format Register 1[2]		
2	L	H	L	CDR1	Compare Data Register 1[3]		Not Used
				ACR1	Auxiliary Control Register 1[4]		
3	L	H	H	TDR1	Transmit Data Register 1	RDR1	Receive Data Register 1
4	H	L	L	IER2	Interrupt Enable Register 2	ISR2	Interrupt Status Register 2
5	H	L	H	CR2	Control Register 2[1]	CSR2	Control Status Register 2
				FR2	Format Register 2[2]		
6	H	H	L	CDR2	Compare Data Register 2[3]		Not Used
				ACR2	Auxiliary Control Register 2[4]		
7	H	H	H	TDR2	Transmit Data Register 2	RDR2	Receive Data Register 2

Notes:
1. D7 must be set low to write to the Control Registers.
2. D7 must be set high to write to the Format Registers.
3. Control Register bit 6 must be set to 0 to access the Compare Register.
4. Control Register bit 6 must be set to 1 to access the Auxiliary Control Register.

SERIAL DATA CHANNELS

Two independent serial data channels are available for the full duplex (simultaneous transmit and receive) transfer of asynchronous frames. Separate internal registers are provided for each channel for the selection of frame parameters (number of bits per character, parity options, etc.), status flags, interrupt control and handshake. The asynchronous frame format is shown in Figure 4.

Transmit data from the host system is loaded into the Transmit Data Register. From there, it is transferred to the Transmit Shift Register where it is shifted, LSB first, onto the TxD line. All transmissions begin with a start bit and end with the user selected number of stop bits. A parity bit is transmitted before the stop bit(s) if parity is enabled.

Receive data is shifted into the Receive Shift Register from the associated RxD line. Start and stop bits are stripped from the frame and the data is transferred to the Receive Data Register. Parity bits may be discarded or stored in the ISR.

Five I/O lines are provided for each channel for handshake with the data communications equipment (DCE). Four of these signals ($\overline{\text{RTS}}$, $\overline{\text{DTR}}$, $\overline{\text{DSR}}$ and $\overline{\text{DCD}}$) are general purpose inputs or outputs. The fifth signal, $\overline{\text{CTS}}$, enables/disables the transmitter. When $\overline{\text{CTS}}$ is high and the Transmit Shift Register is empty, the transmitter (except for Echo Mode) is inhibited. When $\overline{\text{CTS}}$ is low, the transmitter is enabled.

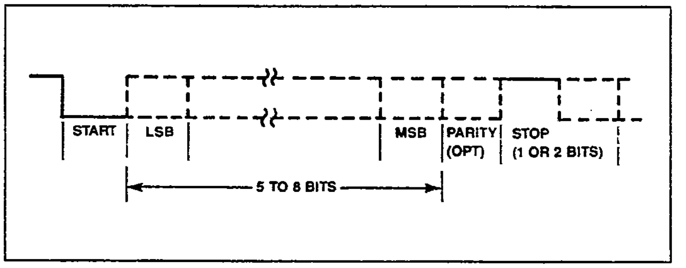


Figure 4. Asynchronous Frame Format

INTERNAL REGISTERS

The DACIA contains ten control registers and four status registers in addition to the transmit and receive registers. The Control Registers provide for control of frame parameters, baud rate, interrupt generation, handshake lines, transmission and reception. The status registers provide status information on transmit and receive registers, error conditions and interrupt sources. Table 4 summarizes the bit definitions of these registers. A detailed description follows.

Table 4. Register Formats

Register Select (Hex)	Register	R/$\overline{\text{W}}$	Bit 7	6	5	4	3	2	1	0	Reset Value 76543210
0 4	ISR1 ISR2	R	ANY BIT SET	TDRE	$\overline{\text{CTST}}$	$\overline{\text{DCDT}}$	$\overline{\text{DSRT}}$	PAR	F/O/B	RDRF	1 - 00000 -
0 4	IER1 IER2	W	CLR/SET BITS	TDRE IE	$\overline{\text{CTST}}$ IE	$\overline{\text{DCDT}}$ IE	$\overline{\text{DSRT}}$ IE	PAR IE	F/O/B IE	RDRF IE	- 0000000
1 5	CSR1 CSR2	R	FE	TUR	$\overline{\text{CTS}}$ LVL	$\overline{\text{DCD}}$ LVL	$\overline{\text{DSR}}$ LVL	BRK	$\overline{\text{DTR}}$ LVL	$\overline{\text{RTS}}$ LVL	1 - - - - 011
1 5	CR1 CR2	W	0	CDR/ ACR	STOP BITS	ECHO	BIT RATE SEL				0 - - - - - - -
1 5	FR1 FR2	W	1	DATA BITS		PAR SEL		PAR EN	$\overline{\text{DTR}}$ CNTL	$\overline{\text{RTS}}$ CNTL	1 - - - - - - -
2 6	CDR1 CDR2	W (CR6 = 0)	COMPARE DATA								- - - - - - - -
2 6	ACR1 ACR2	W (CR6 = 1)	IRQ VECTOR NUMBER						TRNS BRK	PAR ERR/ST	- - - - - - 00
3 7	RDR1 RDR2	R	RECEIVE DATA REGISTER								00000000
3 7	TDR1 TDR2	W	TRANSMIT DATA REGISTER								- - - - - - - -

INTERRUPT STATUS REGISTERS (ISR1, ISR2)

The Interrupt Status Registers are read-only registers indicating the status of each interrupt source. Bits 6 through 0 are set when the indicated $\overline{IRQ}$ condition has occurred. Bit 7 is set to a 1 when any $\overline{IRQ}$ source bit is set, or if Echo Mode is disabled, when $\overline{CTS}$ is high.

7	6	5	4	3	2	1	0
ANY BIT SET	TDRE	$\overline{CTS}$T	$\overline{DCD}$T	$\overline{DSR}$T	PAR	F/O/B	RDRF

Address = 0,4   Reset Value = 1 - 00000 -

Bit 7 **Any Bit Set**
- 1 Any bit (6 through 0) has been set to a 1 or $\overline{CTS}$ is high with echo disabled
- 0 No bits have been set to a 1 or echo is enabled

Bit 6 **Transmit Data Register Empty (TDRE)**
- 1 Transmit Data Register is empty and $\overline{CTS}$ is low
- 0 Transmit Data Register is full or $\overline{CTS}$ is high

Bit 5 **Transition On $\overline{CTS}$ Line ($\overline{CTS}$T)**
- 1 A positive or negative transition has occurred on $\overline{CTS}$
- 0 No transition has occurred on $\overline{CTS}$, or ISR has been Read

Bit 4 **Transition On $\overline{DCD}$ Line ($\overline{DCD}$T)**
- 1 A positive or negative transition has occurred on $\overline{DCD}$
- 0 No transition has occurred on $\overline{DCD}$, or ISR has been Read

Bit 3 **Transition On $\overline{DSR}$ Line ($\overline{DSR}$T)**
- 1 A positive or negative transition has occurred on $\overline{DSR}$
- 0 No transition has occurred on $\overline{DSR}$, or ISR has been Read

Bit 2 **Parity Status (PAR)**

ACR bit 0 = 0
- 1 A parity error has occurred in received data
- 0 No parity error has occurred, or the Receive Data Register (RDR) has been Read

ACR bit 0 = 1
- 1 Parity bit = 1
- 0 Parity bit = 0

Bit 1 **Frame Error, Overrun, Break**
- 1 A framing error, receive overrun, or receive break has occurred or has been detected
- 0 No error, overrun, break has occurred or RDR has been Read

Bit 0 **Receive Data Register Full (RDRF)**
- 1 Receive Data Register is full
- 0 Receive Data Register is empty

Note: To reset ISR:
(a) Bits 0,1,2: Read Receive Data Register
(b) Bits 3,4,5: Read ISR
(c) Bit 6: Write Transmit Data Register

INTERRUPT ENABLE REGISTERS (IER1, IER2)

The Interrupt Enable Registers are write-only registers that enable/disable the $\overline{IRQ}$ sources. $\overline{IRQ}$ sources are enabled by writing to an IER with bit 7 set to a 1 and the bit for every $\overline{IRQ}$ source to be enabled set to a 1. $\overline{IRQ}$ sources are disabled by writing to an IER with bit 7 reset to a 0 and the bit for every source to be disabled set to a 1. Any source bit reset to 0 is unaffected and remains in its original state. Thus, writing $7F to an IER disables all of that channel's interrupts and writing an $FF to an IER enables all of that channel's interrupts.

7	6	5	4	3	2	1	0
SET BITS	TDRE IE	$\overline{CTS}$T IE	$\overline{DCD}$T IE	$\overline{DSR}$T IE	PAR IE	F/O/B IE	RDRF IE

Address = 0,4   Reset Value = - 0000000

Bit 7 **Enable/Disable**
- 1 Enable selected IRQ source
- 0 Disable selected IRQ source

Bits 0-6
- 1 Select for enable/disable
- 0 No change

CONTROL STATUS REGISTERS (CSR1, CSR2)

The Control Status Registers are read-only registers that provide I/O status and error condition information. A CSR is normally read after an $\overline{IRQ}$ has occurred to determine the exact cause of the interrupt condition.

7	6	5	4	3	2	1	0
FE	TUR	$\overline{CTS}$ LVL	$\overline{DCD}$ LVL	$\overline{DSR}$ LVL	BRK	$\overline{DTR}$ LVL	$\overline{RTS}$ LVL

Address = 1,5   Reset Value = 1 - - - - 011

Bit 7 **Framing Error (FE)**
- 1 A framing error occurred in receive data
- 0 No framing error occurred, or the RDR was read

Bit 6 **Transmitter Underrun (TUR)**
- 1 Transmit Shift Register is empty and TDRE is set
- 0 Transmitter Shift Register is not empty

Bit 5 **$\overline{CTS}$ Level ($\overline{CTS}$ LVL)**
- 1 $\overline{CTS}$ line is high
- 0 $\overline{CTS}$ line is low

Bit 4 **$\overline{DCD}$ Level ($\overline{DCD}$ LVL)**
- 1 $\overline{DCD}$ line is high
- 0 $\overline{DCD}$ line is low

Bit 3 **$\overline{DSR}$ Level ($\overline{DSR}$ LVL)**
- 1 $\overline{DSR}$ line is high
- 0 $\overline{DSR}$ line is low

Bit 2 **Receive Break (BRK)**
- 1 A Receive Break has occurred
- 0 No Receive Break occurred, or RDR was read

Bit 1 **$\overline{DTR}$ Level ($\overline{DTR}$ LVL)**
- 1 $\overline{DTR}$ line is high
- 0 $\overline{DTR}$ line is low

Bit 0 **$\overline{RTS}$ Level ($\overline{RTS}$ LVL)**
- 1 $\overline{RTS}$ line is high
- 0 $\overline{RTS}$ line is low

CONTROL REGISTERS (CR1, CR2)

The Control Registers are write-only registers. They control access to the Auxiliary Control Register and the Compare Data Register. They select the number of stop bits, control Echo Mode, and select the data rate.

(Accessed when Bit 7 = 0)

7	6	5	4	3	2	1	0
0	CDR/ACR	STOP BITS	ECHO	BAUD RATE SEL			

Address = 1,5 Reset Value = 0-------

Bit 7 — Control or Format Register
- 0 — Access Control Register

Bit 6 — CDR/ACR
- 1 — Access the Auxiliary Control Register (ACR)
- 0 — Access the Compare Data Register (CDR)

Bit 5 — Number of Stop Bits Per Character
- 1 — Two stop bits
- 0 — One stop bit

Bit 4 — Echo Mode Selection
- 1 — Echo Mode enabled
- 0 — Echo Mode disabled

Bits 3-0 — Baud Rate Selection

3	2	1	0	(bits per second with 3.6864 MHz crystal)
0	0	0	0	50
0	0	0	1	109.2
0	0	1	0	134.58
0	0	1	1	150
0	1	0	0	300
0	1	0	1	600
0	1	1	0	1200
0	1	1	1	1800
1	0	0	0	2400
1	0	0	1	3600
1	0	1	0	4800
1	0	1	1	7200
1	1	0	0	9600
1	1	0	1	19200
1	1	1	0	38400
1	1	1	1	External TxC and RxC X16 Clocks

FORMAT REGISTERS (FR1, FR2)

The Format Registers are write-only registers. They select the number of data bits per character and parity generation/checking options. They also control $\overline{RTS}$ and $\overline{DTR}$.

(Accessed when Bit 7 = 1)

7	6	5	4	3	2	1	0
1	DATA BITS		PAR SEL		PAR EN	$\overline{DTR}$ CNTL	$\overline{RTS}$ CNTL

Address = 1,5 Reset Value = 1-------

Bit 7 — Control or Format Register
- 1 — Access Format Register

Bits 6-5 — Number of Data Bits Per Character

6	5	
0	0	5
0	1	6
1	0	7
1	1	8

Bits 4-3 — Parity Mode Selection

4	3	
0	0	Odd Parity
0	1	Even Parity
1	0	Mark in Parity bit
1	1	Space in Parity bit

Bit 2 — Parity Enable
- 1 — Parity as specified by bits 4-3
- 0 — No Parity

Bit 1 — $\overline{DTR}$ Control
- 1 — Set $\overline{DTR}$ high
- 0 — Set $\overline{DTR}$ low

Bit 0 — $\overline{RTS}$ Control
- 1 — Set $\overline{RTS}$ high
- 0 — Set $\overline{RTS}$ low

COMPARE DATA REGISTERS (CDR1, CDR2)

The Compare Data Registers are write-only registers which can be accessed when CR bit 6 = 0. By writing a value into the CDR, the DACIA is put in the compare mode. In this mode, setting of the RDRF bit is inhibited until a character is received which matches the value in the CDR. The next character is then received and the RDRF bit is set. The receiver will now operate normally until the CDR is again loaded.

(Control Register bit 6 = 0)

7	6	5	4	3	2	1	0
COMPARE DATA							

Address = 2,6 Reset Value = - - - - - - - -

AUXILIARY CONTROL REGISTERS (ACR1, ACR2)

The Auxiliary Control Registers are write-only registers. Bits 7-2 hold the user selected interrupt vector number to be output on data lines 7-2 during interrupt acknowledge. Bit 1 causes the transmitter to transmit a BREAK. Bit 0 determines whether parity error or the parity bit is displayed in ISR bit 2.

(Control Register bit 6 = 1)

7	6	5	4	3	2	1	0
IRQ VECTOR ADDRESS						TRNS BRK	PAR ERR/ST

Address = 2,6 Reset Value = - - - - - - 00

Bits 7-2 **IRQ Vector Address**

Bit 1 **Transmit Break (TRNS BRK)**
- 1 Transmit continuous Break
- 0 Normal transmission

Bit 0 **Parity Error/State (PAR ERR/ST)**
- 1 Send value of parity bit to ISR bit 2 (Address Recognition mode)
- 0 Send Parity Error status to ISR bit 2

RECEIVE DATA REGISTERS (RDR1, RDR2)

The Receive Data Registers are read-only registers which are loaded with the received data character of each frame. Start bits, stop bits and parity bits are stripped off of incoming frames before the data is transferred from the Receive Shift Register to the Receive Data Register. For characters of less than eight bits, the unused bits are the high order bits which are set to 0.

MSB **LSB**

7	6	5	4	3	2	1	0
RECEIVE DATA							

Address = 3,7 Reset Value = 00000000

TRANSMIT DATA REGISTERS (TDR1, TDR2)

The Transmit Data Registers are write-only registers which are loaded from the CPU with data to be transmitted. For data characters of less than eight bits, the unused bits are the high order bits which are "don't care".

MSB **LSB**

7	6	5	4	3	2	1	0
TRANSMIT DATA							

Address = 3,7 Reset Value = - - - - - - - -

OPERATION

TERMINATION OF UNUSED INPUTS

Noise on floating inputs can affect chip operation. All unused inputs must be terminated. If unused, $\overline{\text{IACK1}}$ and $\overline{\text{IACK2}}$ must be tied high. If the baud rate generator is bypassed, XTALI must be connected to ground (XTALO is an output and must be left open). If the external clock mode is not used, RxC and TxC may be tied either to +5V or to ground. If the handshake inputs are not needed, the $\overline{\text{CTS}}$ inputs should be tied low to enable the transmitters. The $\overline{\text{DCD}}$ and $\overline{\text{DSR}}$ inputs may either be tied high or low.

TERMINATION OF $\overline{\text{DTACK}}$

A current limiting resistor with a minimum value of 3.6 KΩ should be connected between $\overline{\text{DTACK}}$ and +5V.

RESET INITIALIZATION

During power on initialization, all readable registers should be read to assure that the status registers are initialized. Specifically, the RDRF bit of the Interrupt Status Registers is not initialized by reset. The Receiver Data Registers must be read to clear this bit.

TDRE $\overline{\text{IRQ}}$ is generated only on the transition of the corresponding TDR from full to empty. Initialization software must account for this occurrence.

BAUD RATE CLOCK OPTIONS

The receiver and transmitter clocks may be supplied either by the internal Baud Rate Generator or by user supplied external clocks. Both channels may use the same clock source or one may use the Baud Rate Generator and the other channel external clocks. If both channels use the Baud Rate Generator, each channel may have a different bit rate. The options are shown in Figure 5.

An internal clock oscillator supplies the time base for the Baud Rate Generator. The oscillator can be driven by a crystal or an external clock.

If the on-chip oscillator is driven by a crystal, a parallel resonant crystal is connected between the XTALI and XTALO pins. The equivalent oscillator circuit is shown in Figure 6.

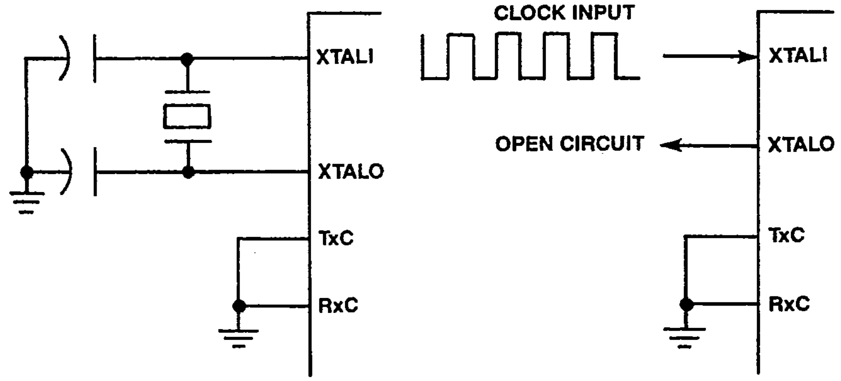
A parallel resonant crystal is specified by its load capacitance and series resonant resistance. For proper oscillator operation, the load capacitance (C_L), series resistance (R_s) and the crystal resonant frequency (F) must meet the following two relations:

$$(C + 2) = 2C_L \quad \text{or} \quad C = 2C_L - 2$$

$$R_s \leq R_{smax} = \frac{2 \times 10^6}{(F \text{ [illegible]})^2}$$

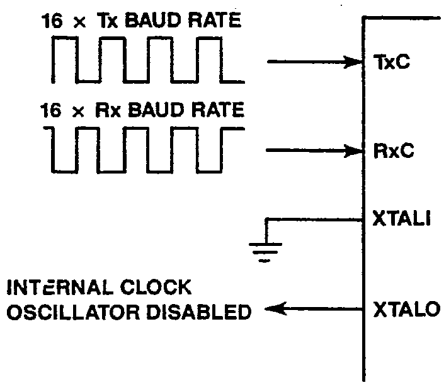
where: F is in MHz; C and C_L are in pF; R is in ohms.

To select a parallel resonant crystal for the oscillator, first select the load capacitance from a crystal manufacturer's catalog. Next, calculate R_{smax} based on F and C_L. The selected crystal must have a R_s less than the R_{smax}.



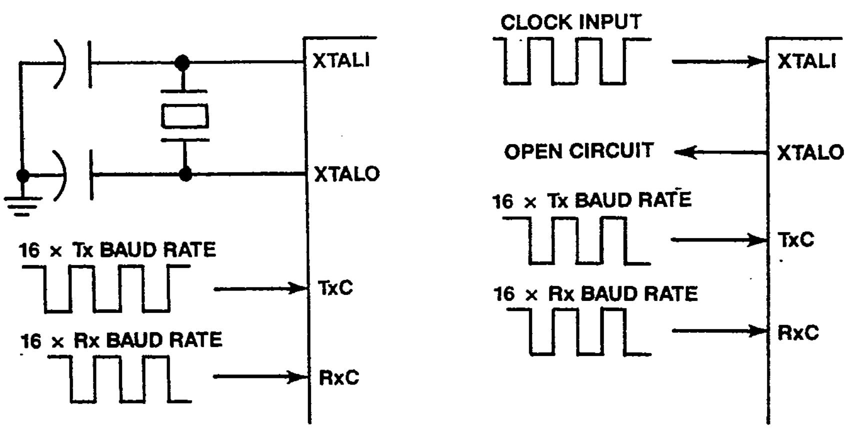
- Baud rate determined by XTALI frequency and 1 of 15 divisors selected in CR1 and CR2. CR1 and CR2 must not be set to all ones.
- Channel 1 baud rate may be different from channel 2 baud rate.
- Receiver baud rate must be the same as transmitter baud rate.

A. Both Channels Use Internal Baud Rate Generator



- Transmitter baud rate 1/16 TxC input frequency.
- Receiver baud rate 1/16 RxC input frequency.
- Channel 1 baud rate is the same as channel 2 baud rate.
- Receiver baud rate may be different from transmitter baud rate.
- Bits 3-0 of CR1 and CR2 must be set to all ones.

B. Both Channels Use External Clocks



- Channel 1 baud rate may be different from channel 2 baud rate.
- Transmitter baud rate may be different from receiver baud rate on channel using external clock.

C. One Channel Uses Internal Baud Rate Generator;
One Channel Uses External Clocks

Figure 5. Baud Rate Clock Options

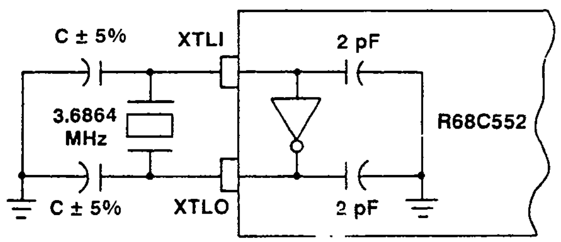


Figure 6.

For example, if C_L = 22 pF for a 3.6864 MHz parallel resonant crystal, then

$$C = (2 \times 22) - 2 = 42 \text{ pF (use standard value of 43 pF)}$$

The series resistance of the crystal must be less than

$$R_{smax} = \frac{2 \times 10^6}{(3.6864 \times 22)^2} = 304 \text{ ohms}$$

If the on-chip oscillator is driven by an external clock, the clock is input at XTALI and XTALO is left open.

An internal counter/divider circuit divides the frequency input at XTALI by the divisor selected in bits 3 through 0 of the Control Registers. Table 5 lists the divisors that may be selected and shows the bit rates generated with a 3.6864 MHz crystal or clock input. Other bit rates may be generated by changing the clock or crystal frequency. However, the input frequency must not exceed 4 MHz.

For external clock operation, a transmitter times 16 clock must be supplied at TxC and a receiver times 16 clock must be input at RxC. Since there are separate receiver and transmitter clock inputs, the receiver data rate may be different from the transmitter data rate.

Table 5. Baud Rate Generator Divisor Selection

Control Register Bits				Divisor Selected For The Internal Counter	Baud Rate Generated With 3.6864 MHz Crystal or Clock	Baud Rate Generated* With a Crystal or Clock of Frequency (f)
3	2	1	0			
0	0	0	0	73,728	$(3.6864 \times 10^6)/73{,}728 = 50$	f/73,728
0	0	0	1	33,538	$(3.6864 \times 10^6)/33{,}538 = 109.92$	f/33,538
0	0	1	0	27,408	$(3.6864 \times 10^6)/27{,}408 = 134.58$	f/27,408
0	0	1	1	24,576	$(3.6864 \times 10^6)/24{,}576 = 150$	f/24,576
0	1	0	0	12,288	$(3.6864 \times 10^6)/12{,}288 = 300$	f/12,288
0	1	0	1	6,144	$(3.6864 \times 10^6)/6{,}144 = 600$	f/6,144
0	1	1	0	3,072	$(3.6864 \times 10^6)/3{,}072 = 1{,}200$	f/3,072
0	1	1	1	2,048	$(3.6864 \times 10^6)/2{,}048 = 1{,}800$	f/2,048
1	0	0	0	1,536	$(3.6864 \times 10^6)/1{,}536 = 2{,}400$	f/1,536
1	0	0	1	1,024	$(3.6864 \times 10^6)/1{,}024 = 3{,}600$	f/1,024
1	0	1	0	768	$(3.6864 \times 10^6)/768 = 4{,}800$	f/768
1	0	1	1	512	$(3.6864 \times 10^6)/512 = 7{,}200$	f/512
1	1	0	0	384	$(3.6864 \times 10^6)/384 = 9{,}600$	f/384
1	1	0	1	192	$(3.6864 \times 10^6)/192 = 19{,}200$	f/192
1	1	1	0	96	$(3.6864 \times 10^6)/96 = 38{,}400$	f/96
1	1	1	1	16	Transmitter Baud Rate = TxC/16	Receiver Baud Rate = RxC/16

$$\text{*Baud Rate} = \frac{\text{Frequency}}{\text{Divisor}}$$

CONTINUOUS DATA TRANSMIT

In the normal operating mode, the TDRE bit in the ISR signals the MPU that the DACIA is ready to accept the next data word. An $\overline{IRQ}$ occurs on the transition of the TDR from full to empty if the corresponding TDRE IRQ enable bit is set in the IER. The TDRE bit is set at the beginning of the start bit. When the MPU writes a word to the TDR the TDRE bit is cleared. In order to maintain continuous transmission the TDR must be loaded before the stop bit(s) are ended. 1/16 of a bit time after $\overline{IRQ}$ goes low, the $\overline{IRQ}$ line may be reset by reading the IRS. $\overline{IRQ}$ will always reset when data is written to the TDR. Figure 7 shows the relationship between $\overline{IRQ}$ and TxD for the Continuous Data Transmit mode.

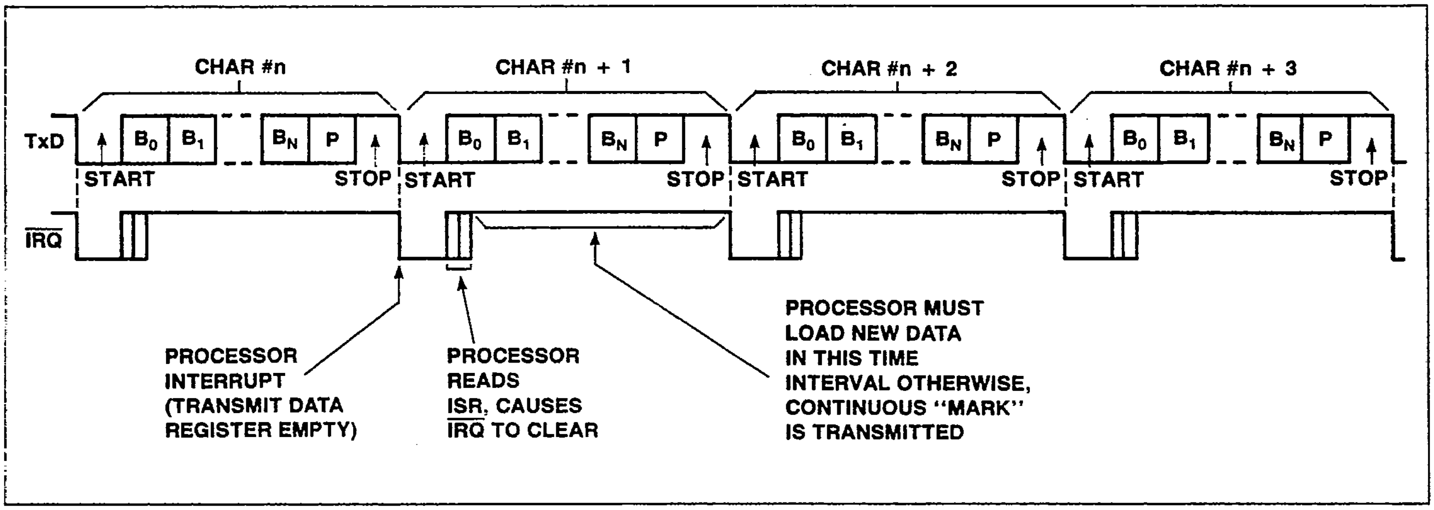


Figure 7. Continuous Data Transmit

TRANSMIT UNDERRUN CONDITION

If the MPU is unable to load the TDR before the last stop bit is sent, the TxD line goes to the MARK condition and the underrun flag (TUR) is set. This condition persists until the TDR is loaded with a new word. Figure 8 shows the relation between $\overline{IRQ}$ and TxD for the Transmit Underrun Condition.

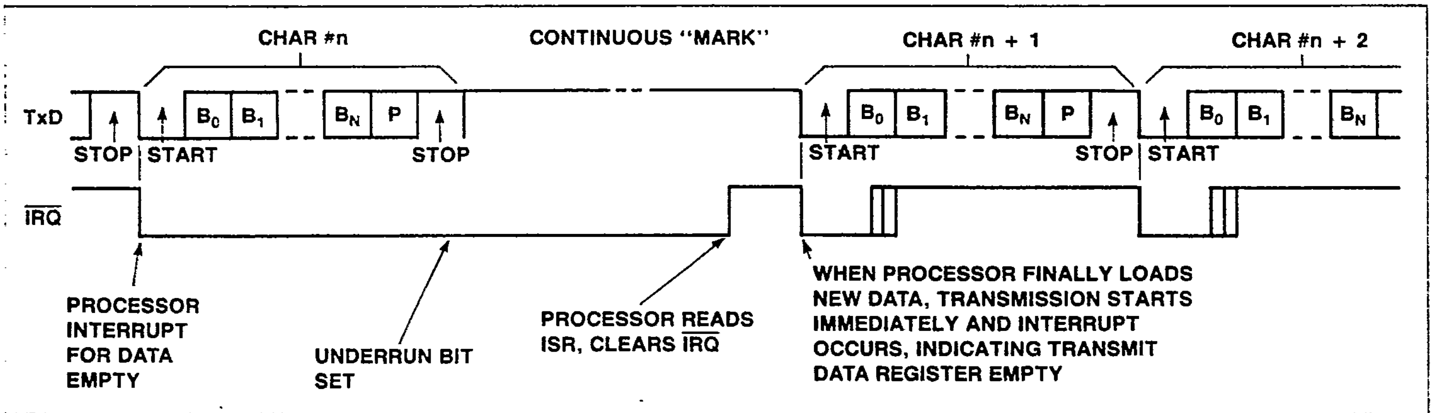


Figure 8. Transmit Underrun Condition Relationship

TRANSMIT BREAK CHARACTER

A BREAK may be transmitted by setting bit 1 of the ACR (Transmit Break bit) to a 1. The BREAK is transmitted after the character in the Transmit Shift Register is sent. If there is a character in the Transmit Data Register, it will be transmitted after the BREAK is terminated. The Transmit Break bit must remain set for at least one character time to assure that a proper BREAK is transmitted. If the Transmit Break bit is cleared before one character time of BREAK has been transmitted, the BREAK will be terminated after one character time has elapsed. If the Transmit Break bit is cleared after one character time of BREAK has been transmitted, the BREAK will be terminated immediately. Figure 9 shows the relationship of TxD, $\overline{IRQ}$ and ACR bit 1 for various BREAK options.

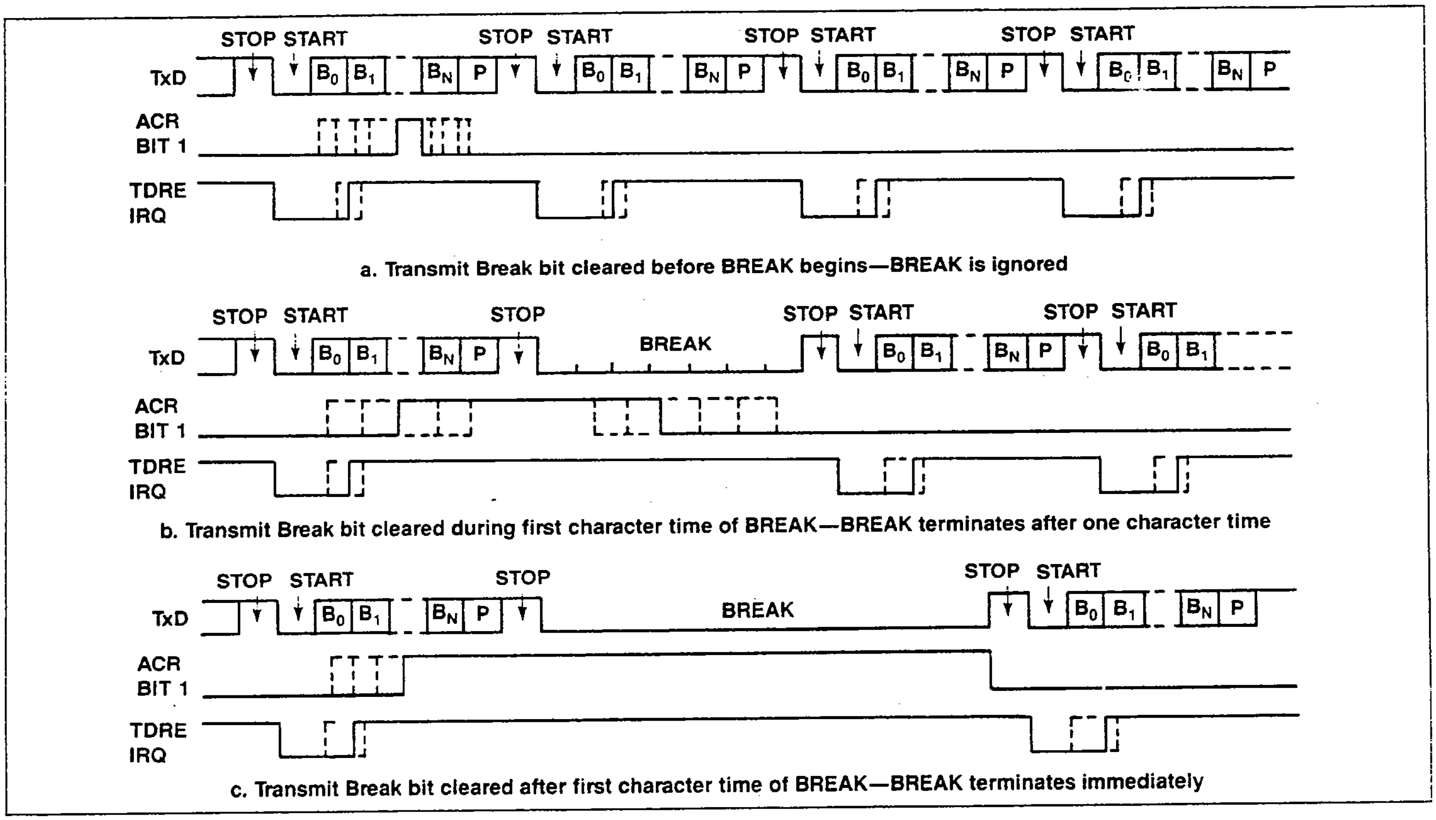


Figure 9. Transmit BREAK

EFFECTS OF $\overline{CTS}$ ON TRANSMITTER

The $\overline{CTS}$ control line controls the transmission of data or the handshaking of data to a "busy" device (such as a printer). When the $\overline{CTS}$ line is low, the transmitter operates normally. A high condition inhibits the TDRE bit in the ISR from becoming set. Transmission of the word currently in the shift register is completed but any word in the TDR is held until $\overline{CTS}$ goes low.

Any transition on $\overline{CTS}$ sets bit 5 ($\overline{CTST}$) of the ISR. A high on $\overline{CTS}$ forces bit 6 ($\overline{TDRE}$) of the ISR to a 0. Bit 7 of the ISR also goes to a 1 when $\overline{CTS}$ is high, if Echo Mode is disabled. Thus, when the ISR is \$80, it means that $\overline{CTS}$ is high and no interrupt source requires service. A processor interrupt will not be generated under these circumstances, but an ISR polling routine should accommodate this.

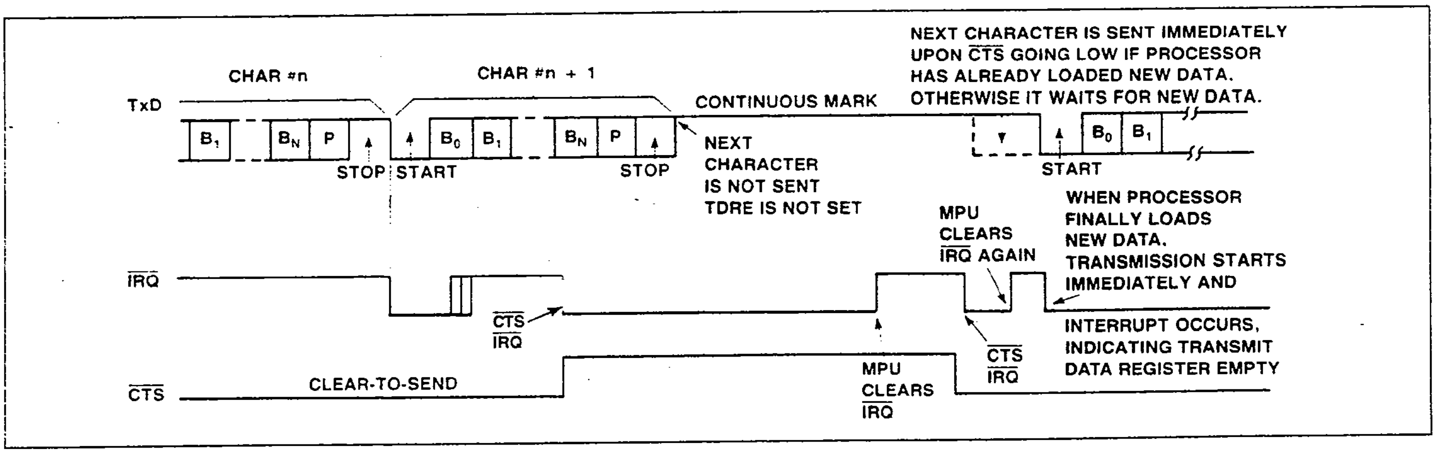


Figure 10. Effects of $\overline{CTS}$ on Transmitter

ECHO MODE TIMING

In the Echo Mode, the TxD line re-transmits the data received on the RxD line, delayed by 1/2 of a bit time. An internal underrun mode must occur before Echo Mode will start transmitting. In normal transmit mode if TDRE occurs (indicating end of data) an underflow flag would be set and continuous Mark transmitted. If Echo is initiated, the underflow flag will not be set at end of data and continuous Mark will not be transmitted. Figure 11 shows the relationship of RxD and TxD for Echo Mode.

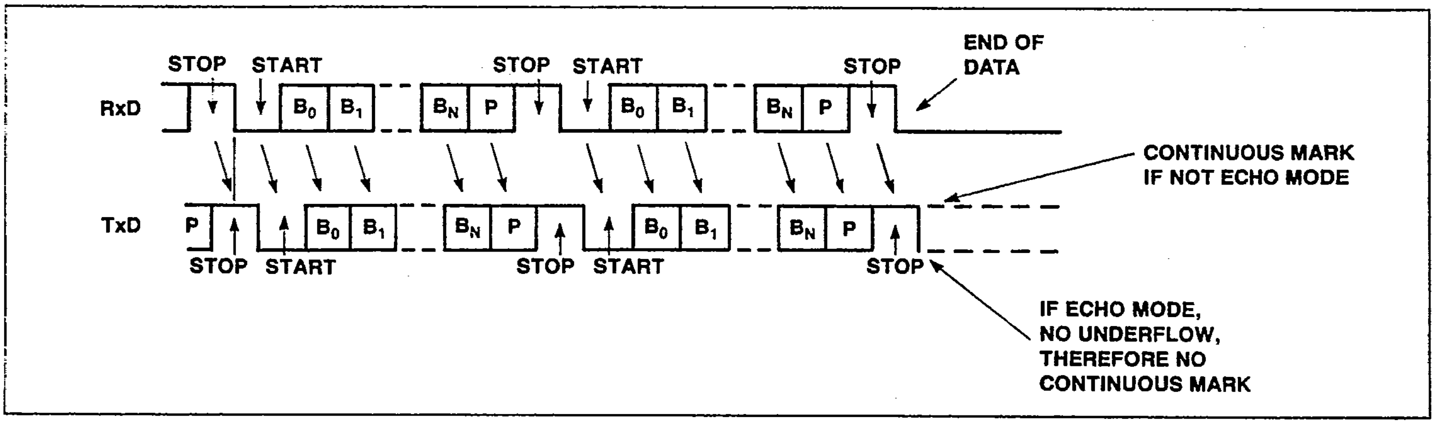


Figure 11. Echo Mode Timing

CONTINUOUS DATA RECEIVE

The normal receive mode sets the RDRF bit in the ISR when the DACIA channel has received a full data word. This occurs at about the 9/16 point through the stop bit. The processor must read the RDR before the next stop bit, or an overrun error occurs. Figure 12 shows the relationship between $\overline{IRQ}$ and RxD for the continuous Data Receive mode.

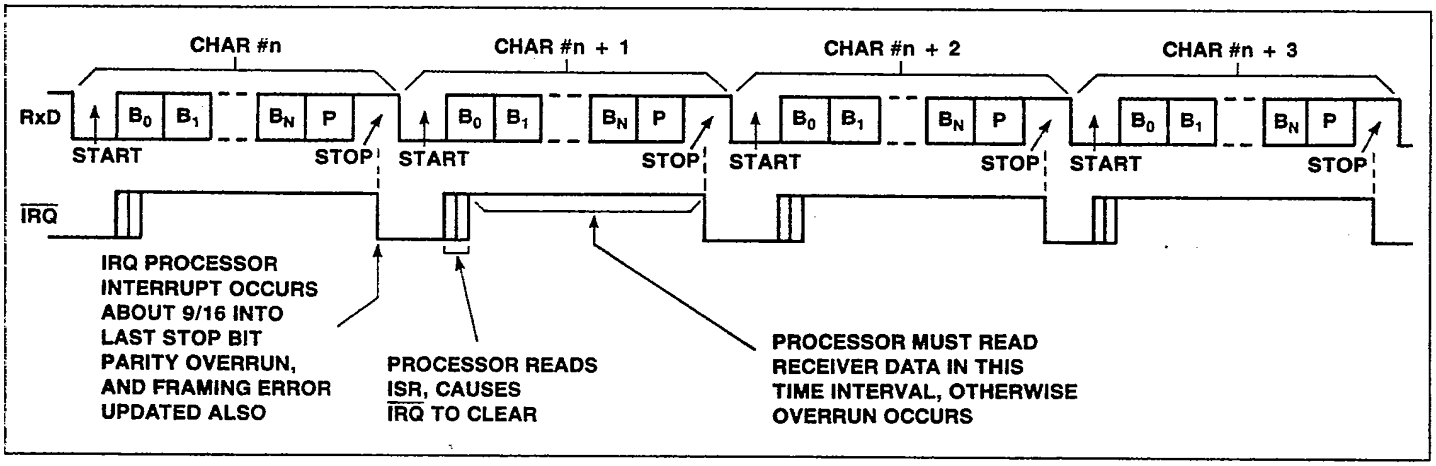


Figure 12. Continuous Data Receive

EFFECTS OF OVERRUN ON RECEIVER

If the processor does not read the RDR before the stop bit of the next word, an overrun error occurs, the overrun bit is set in the ISR, and the new data word is not transferred to the RDR. The RDR contains the last word not read by the MPU and all following data is lost. The receiver will return to normal operation when the RDR is read. Figure 13 shows the relationship of $\overline{IRQ}$ and RxD when overrun occurs.

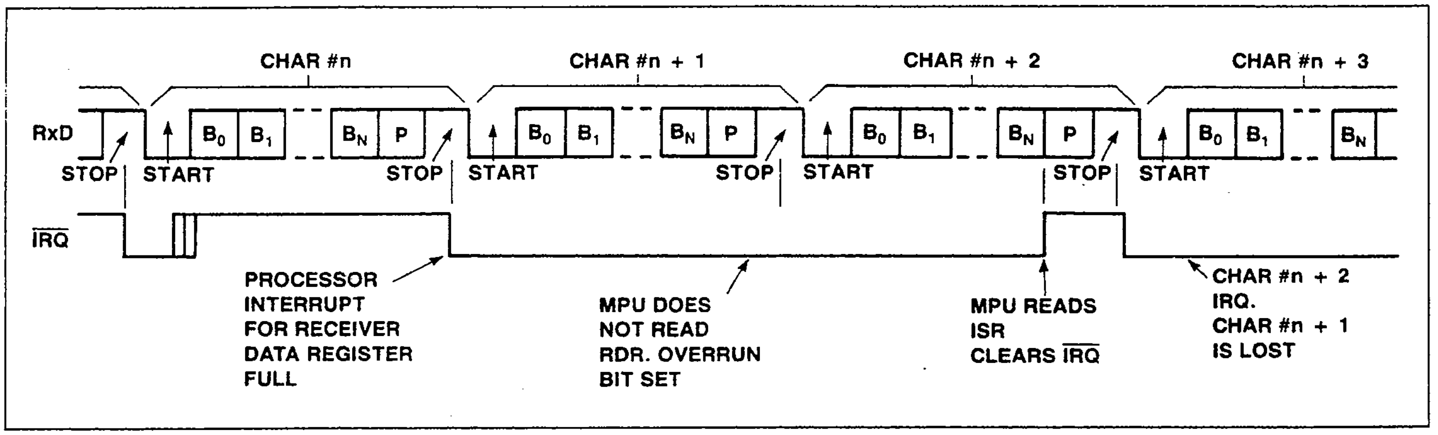


Figure 13. Effects of Overrun on Receiver

RECEIVE BREAK CHARACTER

When a Break character is received, the Break bit is set. The receiver does not set the RDRF bit and remains in this state until a stop bit is received. At this time the next character is received normally. Figure 14 shows the relationship of $\overline{IRQ}$ and RxD for a Receive Break Character.

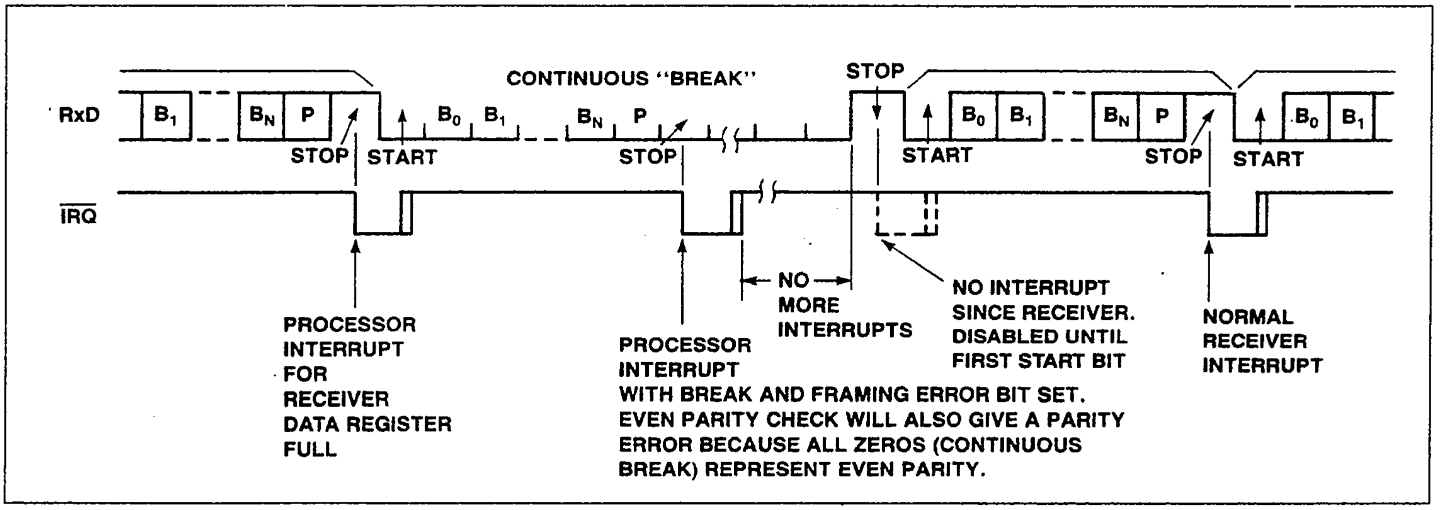


Figure 14. Receive Break Character

FRAMING ERROR

Framing error is caused by the absence of stop bit(s) on received data. The framing error bit is set when the RDRF bit is set. Subsequent data words are tested separately, so the status bit always reflects the last data word received. Figure 15 shows the relationship of $\overline{IRQ}$ and RxD when a framing error occurs.

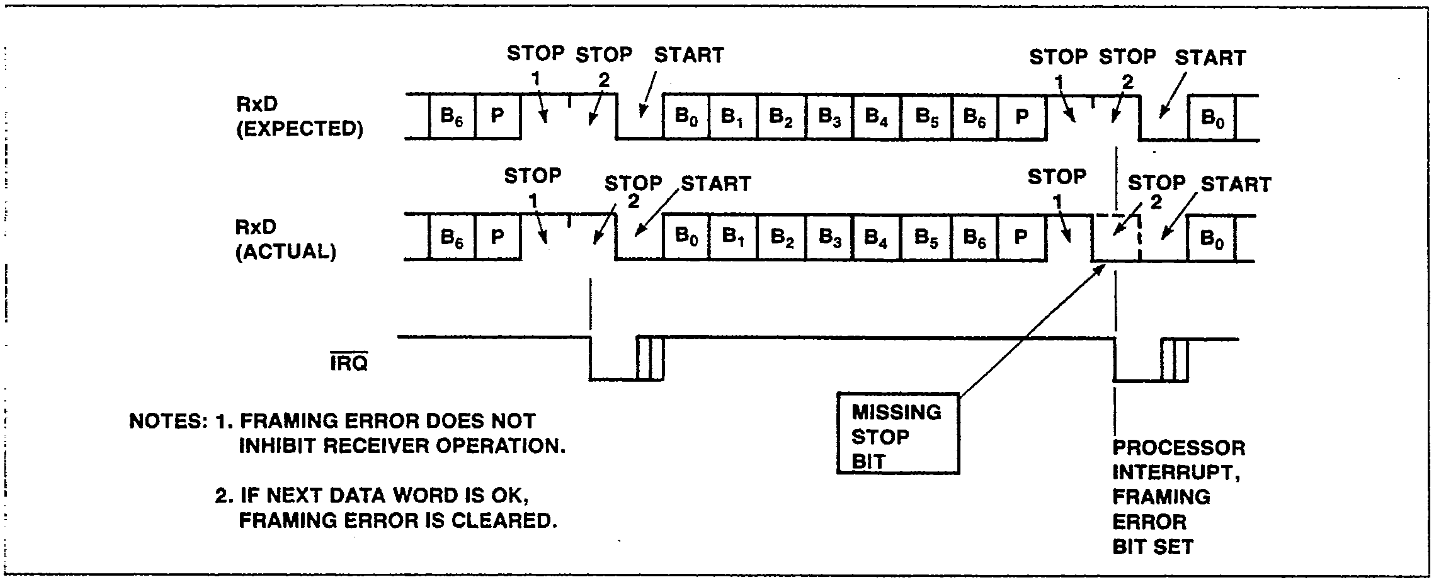


Figure 15. Framing Error

PARITY ERROR DETECT/ADDRESS FRAME RECOGNITION

The Parity Status bit (ISR bit 2) may be programmed to indicate parity errors (ACR bit 0 = 0) or to display the parity bit received (ACR bit 0 = 1).

In applications where parity checking is used, one of the parity checking modes is enabled by setting bits 2, 3 and 4 of the Format Register to the desired option and bit 0 of the Auxiliary Control Register is reset to 0. Then, when the RDRF bit (bit 0) is set in the ISR, the PAR bit (bit 2) will be set when a parity error is detected.

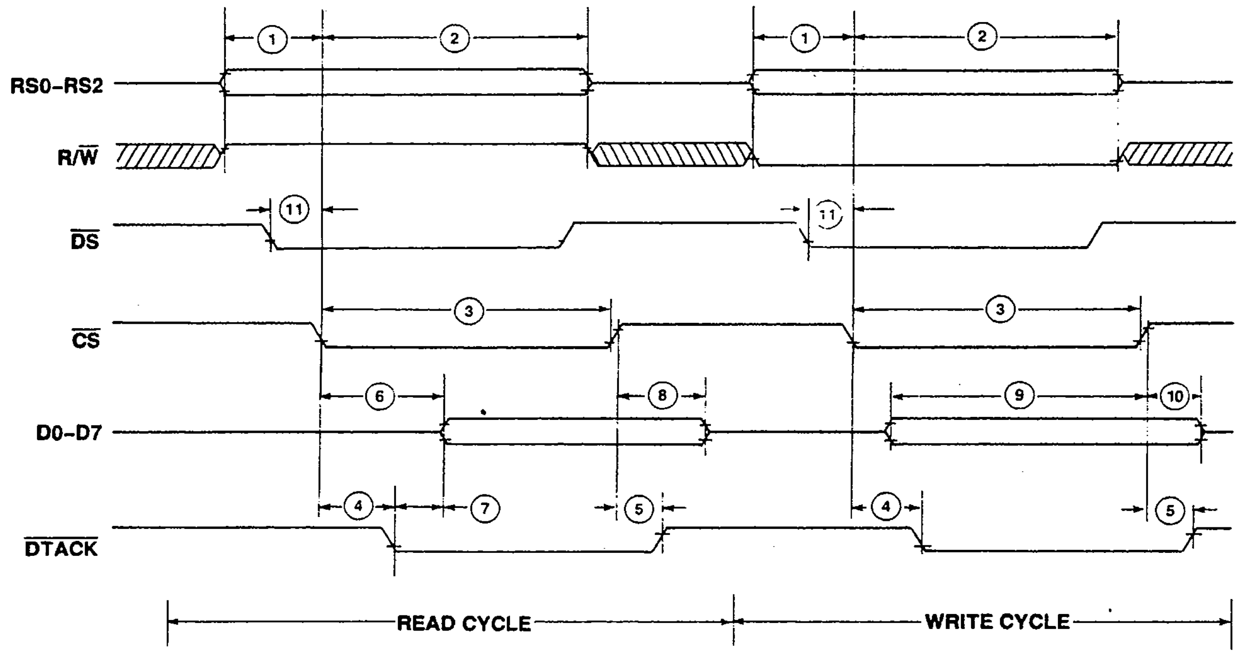
In multi-drop applications, the parity bit is used as an address/data flag. It is set to 1 for address frames and is 0 on data frames. For this type of operation, bit 0 of the ACR is set to a 1 and bits 2, 3 and 4 of the FR select a parity checking mode. Then, ISR bit 2 will be set to a 1 by incoming address frames and it will be a 0 on data frames.

COMPARE MODE

The Compare Mode is automatically enabled, i.e., the channel is put to sleep, whenever data is written to the Compare Data Register. NOTE: Bit 6 of the Control Register must be set to 0 to enable access to the Compare Data Register. When the channel is in the compare mode, the RDRF bit (bit 0 of the ISR) is forced to a 0. Upon receipt of a matching character, normal receiver operation resumes and the RDRF bit (bit 0 of the ISR) will be set upon receipt of the *next* character.

SPECIFICATIONS

DACIA READ/WRITE WAVEFORMS



NOTE: TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8V AND A HIGH VOLTAGE OF 2.0V, UNLESS OTHERWISE NOTED.

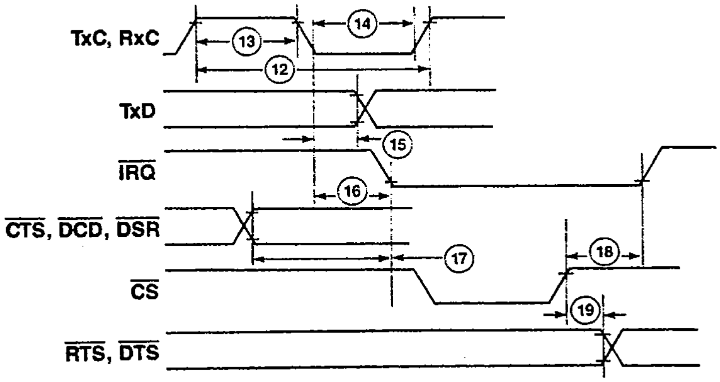
DACIA READ/WRITE CYCLE TIMING

(V_{CC} = 5 Vdc ±5%, V_{SS} = 0 Vdc, T_A = T_L to T_H, unless otherwise noted)

Number	Characteristic	Symbol	Min.	Typ.	Max.	Unit
1	R/W̄, RS0-RS2 Valid to C̄S̄ Low (Setup)	T_{RSU}	5		—	ns
2	C̄S̄ Low to R/W̄, RS0-RS2 Invalid (Hold)	T_{RH}	45		—	ns
3	C̄S̄ Pulse Width	T_{CP}	210		—	ns
4	C̄S̄ Low to D̄T̄ĀC̄K̄ Low	T_{CTL}	—		55	ns
5	C̄S̄ High to D̄T̄ĀC̄K̄ High	T_{CTH}	0		170	ns
6	C̄S̄ Low to Data Valid (Read)	T_{CDV}	—		170	ns
7	D̄T̄ĀC̄K̄ Low to Data Valid (Read)	T_{TDV}	—		110	ns
8	C̄S̄ High to Data Invalid (Read)	T_{CDR}	10		50	ns
9	Data Valid to C̄S̄ High (Write, Setup)	T_{DSU}	30		—	ns
10	C̄S̄ High to Data Invalid (Write Hold)	T_{CDW}	10		—	ns
11	D̄S̄ Low to C̄S̄ Low (Delay for C̄S̄ derived from Data Strobe)	T_{DSC}		20		ns

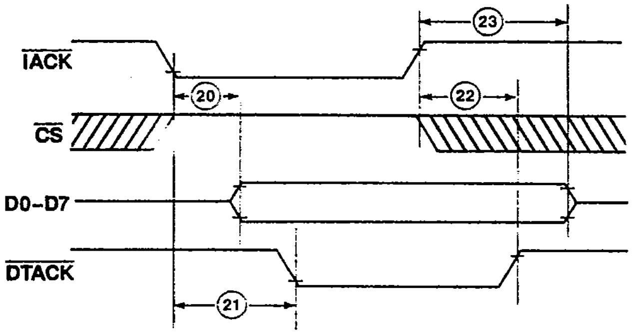
7811073 0017460 TT7 RKW

DACIA TRANSMIT/RECEIVER WAVEFORMS



NOTE: TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8V AND A HIGH VOLTAGE OF 2.0V, UNLESS OTHERWISE NOTED.

DACIA INTERRUPT ACKNOWLEDGE WAVEFORMS



NOTE: TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8V AND A HIGH VOLTAGE OF 2.0V, UNLESS OTHERWISE NOTED.

NOTE: CS MUST BE HIGH DURING IACK CYCLE.

TRANSMIT/RECEIVE AND INTERRUPT ACKNOWLEDGE TIMING

(V_{CC} = 5 Vdc ± 5%, V_{SS} = 0 Vdc, T_A = T_L to T_H, unless otherwise noted)

Number	Characteristic	Symbol	Min.	Max.	Unit
TRANSMIT/RECEIVE TIMING					
12	Transmit/Receive Clock Rate	t_{CY}	300	—	ns
13	Transmit/Receive Clock High	t_{CH}	125	—	ns
14	Transmit/Receive Clock Low	t_{CL}	125	—	ns
15	TxC, RxC to TxD Propagation Delay	t_{DD}	—	285	ns
16	TxC, RxC to IRQ Propagation Delay	t_{DI}	—	285	ns
17	CTS, DCD, DSR Valid to IRQ Low	t_{CTI}	—	150	ns
18	IRQ Propagation Delay (Clear)	t_{IRQ}	—	150	ns
19	RTS, DTR Propagation Delay	t_{DLY}	—	150	ns
INTERRUPT ACKNOWLEDGE TIMING					
20	IACK Low to Data Valid	t_{IDV}	—	170	ns
21	IACK Low to DTACK Low	t_{ITL}	—	62	ns
22	IACK High to DTACK High	t_{ITH}	—	170	ns
23	IACK High to Data Invalid	t_{IDZ}	10	40	ns

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to V_{CC} +0.3	Vdc
Output Voltage	V_{OUT}	−0.3 to V_{CC} +0.3	Vdc
Operating Temperature Commercial Industrial	T_A	 0 to +70 −40 to +85	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V ± 5%
Temperature Range Commercial Industrial	T_A	 0 to 70°C −40°C to +85°C

DC CHARACTERISTICS

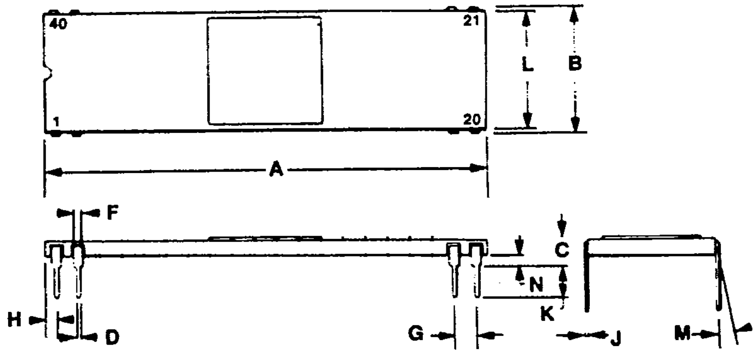
(V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input High Voltage Except XTALI XTALI	V_{IH}	 +2.0 +3.0	 — —	 V_{CC} + 0.3 V_{CC} + 0.3	V	
Input Low Voltage Except XTALI XTALI	V_{IL}	 −0.3 −0.3	 — —	 +0.8 +0.4	V	
Input Leakage Current R/$\overline{W}$, $\overline{RES}$, RS0, RS1, RS2, RxD, $\overline{CTS}$, $\overline{DCD}$, $\overline{DSR}$, RxC, TxC, $\overline{CS}$, $\overline{IACK}$	I_{IN}	—	10	50	µA	V_{IN} = 0V to 5.0V V_{CC} = 5.25V
Input Leakage Current for Three-State Off D0–D7	I_{TSI}	—	±2	10	µA	V_{IN} = 0.4V to 2.4V V_{CC} = 5.25V
Output High Voltage D0–D7, TxD, CLK OUT, $\overline{RTS}$, $\overline{DTR}$	V_{OH}	+2.4	—	—	V	V_{CC} = 4.75V I_{LOAD} = −100 µA
Output Low Voltage D0–D7, TxD, CLK OUT, $\overline{RTS}$, $\overline{DTR}$	V_{OL}	—	—	+0.4	V	V_{CC} = 4.75V I_{LOAD} = 1.6 mA
Output Leakage Current (Off State) $\overline{IRQ}$, $\overline{DTACK}$	I_{OFF}	—	±2	±10	µA	V_{CC} = 5.25V V_{OUT} = 0 to 2.4V
Power Dissipation	P_D	—	—	10	mW/MHz	
Input Capacitance Except XTALI XTALI	C_{IN}	 — —	 — —	 5 10	 pF pF	V_{CC} = 5.0V V_{IN} = 0V f = 2 MHz T_A = 25°C
Output Capacitance	C_{OUT}	—		10	pF	

Notes:
1. All units are direct current (dc) except for capacitance.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. Typical values are shown for V_{CC} = 5.0V and T_A = 25°C.

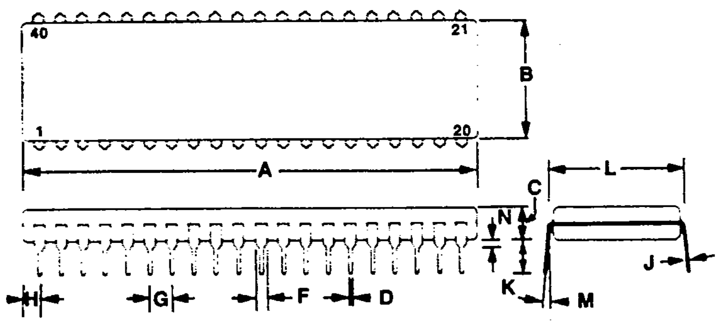
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



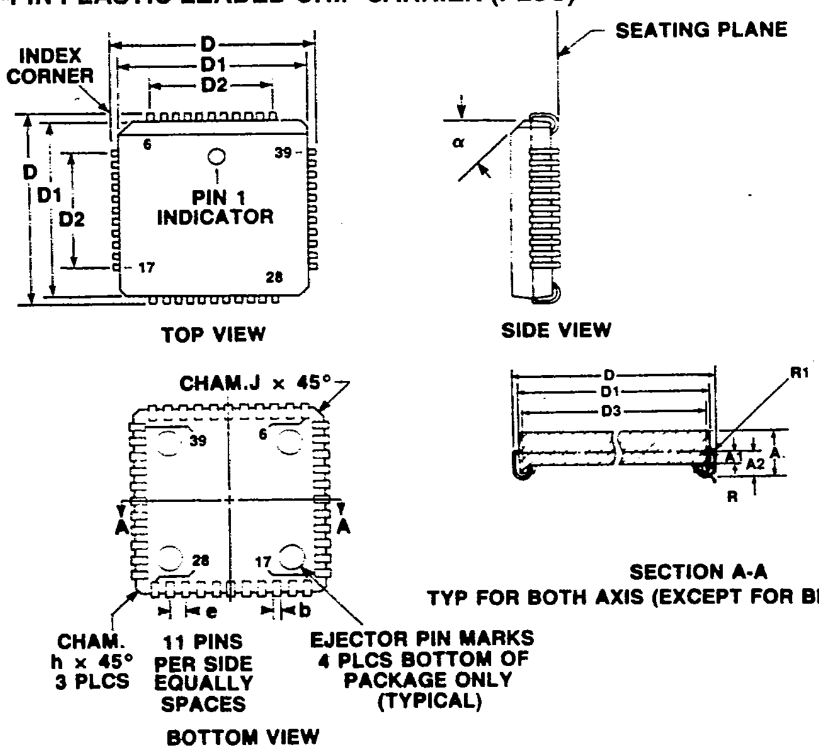
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50.29	51.31	1.980	2.020
B	15.11	15.88	0.595	0.625
C	2.54	4.19	0.100	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.27	0.030	0.050
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.60	15.37	0.575	0.605
M	0°	10°	0°	10°
N	0.51	1.52	0.020	0.060

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.82	52.32	2.040	2.060
B	13.46	13.97	0.530	0.550
C	3.56	5.08	0.140	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.30	4.32	0.130	0.170
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040

44-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



SECTION A-A
TYP FOR BOTH AXIS (EXCEPT FOR BEVELED EDGE)

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.14	4.39	0.163	0.173
A1	1.37	1.47	0.054	0.058
A2	2.31	2.46	0.091	0.097
b	0.457 TYP		0.018 TYP	
D	17.45	17.60	0.687	0.693
D1	16.46	16.56	0.648	0.652
D2	12.62	12.78	0.497	0.503
D3	15.75 REF		0.620 REF	
e	1.27 BSC		0.050 BSC	
h	1.15 TYP		0.045 TYP	
J	0.25 TYP		0.010 TYP	
α	45° TYP		45° TYP	
R	0.89 TYP		0.035 TYP	
R1	0.25 TYP		0.010 TYP	