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R8069B

Rockwell

Line Interface Unit (LIU)

INTRODUCTION

The Rockwell R8069B Line Interface Unit (LIU) is a single chip CMOS device that interfaces the Rockwell R8070 T1/CEPT PCM Transceiver or RT9170 Intelligent T1 Controller to the physical T-1/CEPT PCM30 transmission medium.

The R8069B LIU device contains analog and digital circuits which are based on CMOS technology to support the line interface function required in ISDN primary rate transmission. The R8069B provides capabilities for 4-wire transmission of image, voice, or data signals; clock extraction; line equalization; bipolar violation detection; jitter accommodation; and AIS (Blue Alarm) generation and detection. In addition, the device operates at 1.544 or 2.048 Mbit/s and meets pulse shape and jitter requirements specified by T-1 or PCM30 standards, respectively.

The R8069B is ideally suited for image, voice, or data transmission required in ISDN primary rate applications. The device is highly integrated and requires minimal external components.

Internal LIU functions allow system designers to minimize their development cost and easily implement a T-1/PCM30 physical interface to primary rate lines without concern about most of the complex details normally associated with such a design. The R8069B also provides a high level of integration which increases system reliability, reduces space and achieves higher levels of performance and quality.

FEATURES

- Compatible with T-1 (1.544 Mbit/s) DSX-1 and PCM30 (2.048 Mbit/s) standards
- Selectable T-1 and PCM30 clock rates
- Directly compatible with Rockwell R8070 T-1/CEPT PCM Transceiver, RT9170 Intelligent T1 Controller, and R8071 ISDN/DMI Link Layer Controller devices
- Meets AT&T Technical Advisory No. 34 for T-1 and CCITT Recommendation G.703 for PCM30
- Meets jitter requirements specified in AT&T Publication 62411 (Oct. 1985) for T-1 and CCITT Recommendation G.823 for PCM30
- Phase locked loop for loop timing applications
- Incorporates a frequency discriminator in PLL circuitry to enhance frequency training and locking
- Provides line equalization for up to 660 feet of 100 Ω 22-gauge plastic insulated (ABAM) cable for T-1
- Accommodates pulse shape requirements for 75 Ω and 120 Ω lines in PCM30 application and 100 Ω T-1 lines
- Intrinsic jitter less than 0.05 UI
- Jitter attenuation roll off starts at 2 Hz
- Jitter tolerance above 0.4 UI for jitter frequency from 20 kHz to 100 kHz
- 8-bit transmitter (TX) elastic store for system-provided timing alignment
- 44-bit receiver (RX) elastic store for input jitter and wander accommodation
- Provision to bypass RX elastic store
- Master/slave timing option
- Local and remote loopback modes with automatic RCLK switching
- AIS (Blue Alarm) generation and detection
- Bipolar violation detector
- Automatic detection of external line-rate clock (EXCLK)
- Automatic centering of phase-lock loop when timing reference is absent
- On-chip line drivers, pulse shaping, and TX equalizer
- Analog CMOS technology
- CMOS/TTL compatible inputs and outputs
- Operates from a single +5V power supply
- Packaging options
  - 28-pin plastic DIP
  - 28-pin CERDIP
  - 44-pin PLCC

Document No. 29300N53 **Data Sheet (Preliminary)** **Order No. 353 February 1990**

ORDERING INFORMATION

Part Number:
R8069B_
- Temperature
  - Blank = 0°C to + 70°C
- Package
  - P = 28-Pin Plastic DIP
  - S = 28-Pin CERDIP
  - J = 44-Pin PLCC

INTERFACE SIGNAL DESCRIPTION

The R8069B interfaces directly to the R8070 and R8071 on one side and the DSX-1 or PCM30 demarcation point on the other, through transmit and receive transformers located external to the LIU device (Figure 1). The R8069B LIU interface signals are functionally grouped in Figure 2. Figure 3 shows the R8069B pin assignments. Table 1 describes the R8069B interface signals.

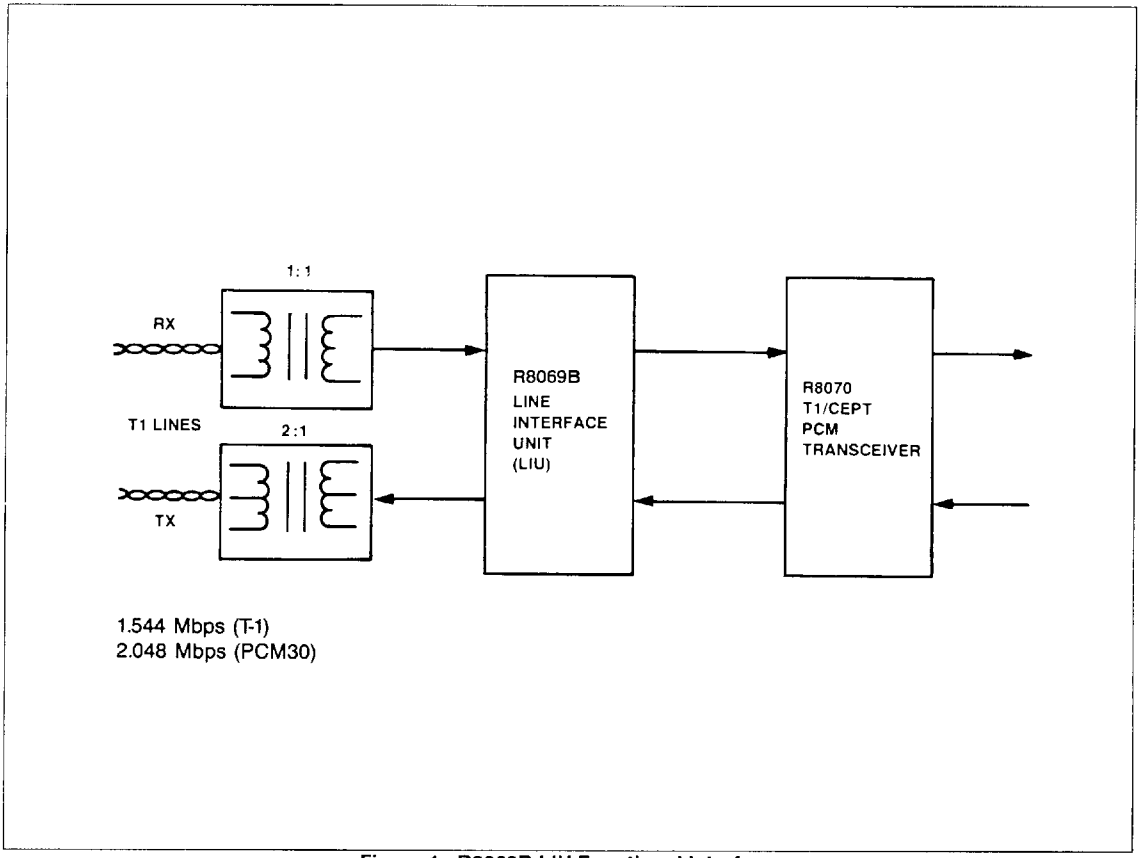


Figure 1. R8069B LIU Functional Interface

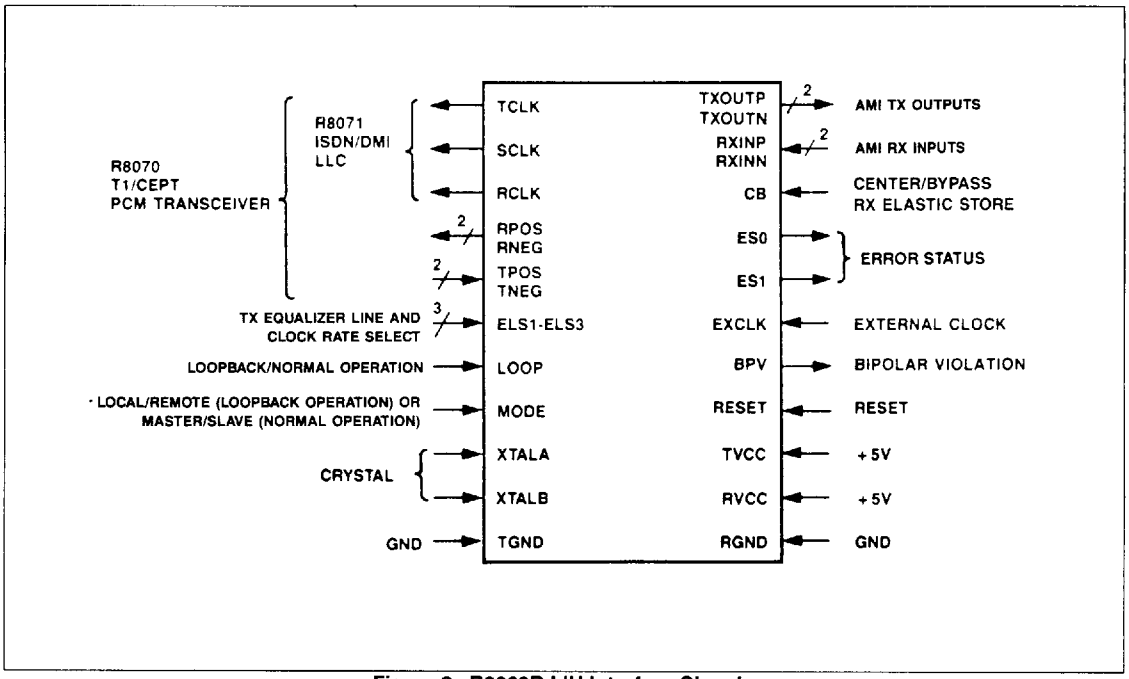


Figure 2. R8069B LIU Interface Signals

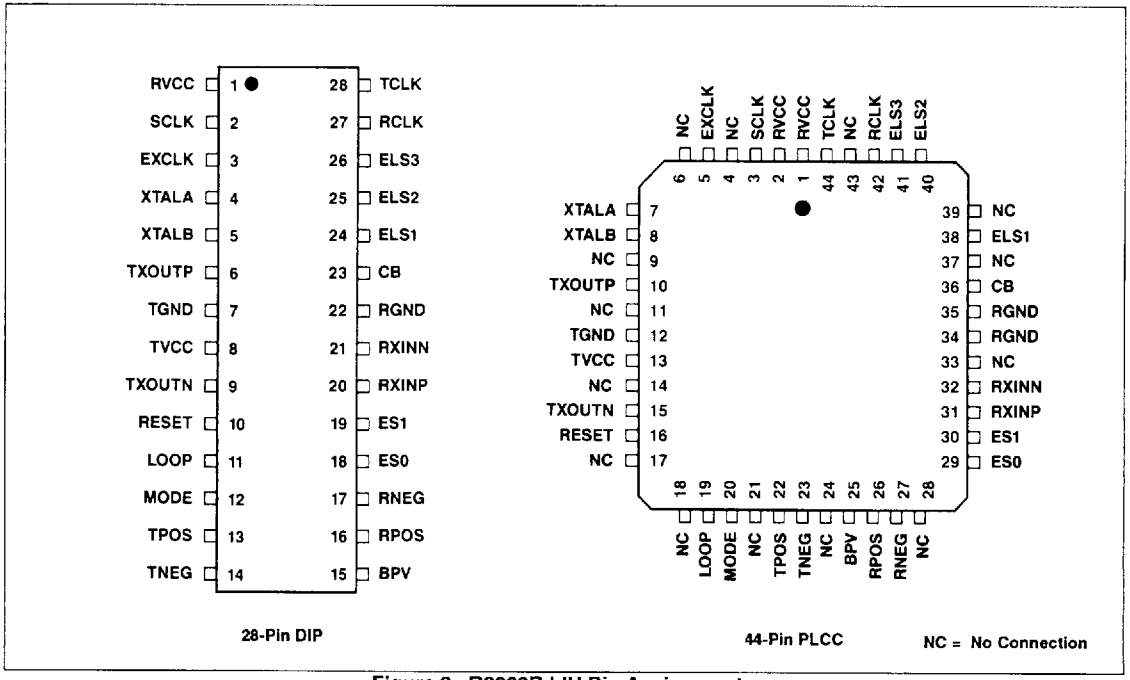


Figure 3. R8069B LIU Pin Assignments

Table 1. R8069B Interface Signal Descriptions

Symbol	I/O	Name/Function
RXINP, RXINN	I	**Receive Data Input P, Receive Data Input N.** Receive bipolar data from transmission line. A 1:1 transformer is required on these input lines.
RPOS, RNEG	O	**Receive Unipolar Positive, Receive Unipolar Negative.** RPOS and RNEG are the outputs of the received data recovered from RXINP and RXINN AMI line pulses. RPOS and RNEG have TTL levels and are alternate unipolar. (These lines can be directly connected to R8070's RPOS and RNEG inputs.) RPOS and RNEG are clocked out at the falling edge of RCLK (when elastic store bypass is enabled) or TCLK (when elastic store bypass is disabled).
RCLK	O	**Received Clock.** RCLK is the recovered clock output which is used to clock the receive data outputs, RPOS and RNEG, from the receiver at its falling edge.
EXCLK	I	**External Clock.** EXCLK is a TTL level input. The clock frequency should be 1.544 MHz ± 32 ppm for T-1 applications and 2.048 MHz ± 50 ppm for PCM30 applications.
CB	I	**Center/Bypass Elastic Store.** RX elastic store is centered on the rising edge of CB. RX elastic store is bypassed when CB is high. (Minimum pulse width is one clock cycle.)
BPV	O	**Bipolar Violation Detection.** Whenever a bipolar violation on the receive data is detected, the BPV generates a positive pulse of one clock interval at the falling edge of TCLK (CB low) or RCLK (CB high).
ES0, ES1	O	**Error Status.** The Error Status is continuously updated on the rising edge of TCLK. **ES0 ES1** 0 0 **AIS Detected.** AIS is activated by detection of a string of 2316 ones with no more than one zero. AIS is deactivated when three or more zeros are detected after the AIS detection. 0 1 **Loss of Signal.** Activated when the input signal level drops below 0.97 volts for 175 bit times; deactivated when the input signal level rises above 0.97 volts. 1 0 **Elastic Buffer Limit**. Indicates an overrun/underrun on the elastic store. It is cleared when CB or RESET is activated. 1 1 **Normal Operation.**
TPOS, TNEG	I	**Transmit Unipolar Positive, Transmit Unipolar Negative.** TPOS and TNEG are the "unipolar paired" input for transmitted data. TPOS and TNEG must have TTL levels and must be alternate unipolar. (These lines can be directly connected to R8070 TPOS and TNEG outputs.) They are clocked in at the falling edge of TCLK or EXCLK (see Table 4). There are only three valid states for TPOS/TNEG (10, 01, 00); **state 11 is not allowed**.
TXOUTP, TXOUTN	O	**Transmit Data Output P, Transmit Data Output N.** Transmit bipolar data to transmission line. A 1:2 step up transformer is needed at the output.
TCLK	O	**Transmit Clock.** TCLK is the transmit clock output which is generated by the crystal based PLL2. It normally references EXCLK or the receive data input depending on mode. In the absence of EXCLK and receive data, the TCLK reference is the on-chip crystal oscillator center frequency. (See Table 4.)
SCLK	O	**System Clock.** SCLK runs at two times the clock rate of TCLK, which is required by the R8071. This output can be directly connected to the R8071 SCLK input.
ELS1-ELS3	I	**Equalization Select.** Strap inputs that select T-1 cable length equalization or PCM30 line load impedance. (See Table 2.)
LOOP	I	**Loopback Select.** LOOP low selects either master or slave. LOOP high selects either local or remote loopback. (See "Mode and Loop Timing" section for details.)
MODE	I	**Mode Select.** Mode low selects local loopback or master timing mode. Mode high selects remote loopback or slave. (See "Mode and Loop Timing" section for details.)

Table 1. R8069B Interface Signal Descriptions (Cont'd)

Symbol	I/O	Name/Function
RESET	I	**Reset.** When Reset is asserted, the RX elastic store is centered, the VCO is trained to lock to EXCLK, or the crystal-based PLL2 if EXCLK is absent. **This resetting mechanism is disabled when both LOOP and MODE inputs are high.**
XTALA, XTALB	I	**XTAL Input pins.** Connect an external, parallel resonant, 6.176 MHz or 8.192 MHz crystal to these pins for T-1 or PCM30 application, respectively. **NOTE: Do not connect a TTL or CMOS clock source to these pins.**
TVCC	I	**Transmit Line Driver Power.** +5V power supply for the transmit line driver.
TGND	I	**Transmit Line Driver Ground.** Ground for the transmit line driver.
RVCC	I	**Power.** +5V power supply.
RGND	I	**Ground.**

FUNCTIONAL DESCRIPTION

The R8069B LIU contains both analog and digital circuitry which independently process transmit and receive primary rate voice or data information. Circuitry to provide master, slave, local loopback, remote loopback, and their derivatives is also included. A simplified block diagram of the R8069B LIU is depicted in Figure 4. Typical R8069B LIU connections in CEPT and T-1 applications are shown in Figures 5, 6, and 7.

TRANSMIT SECTION

Unipolar transmit data (TPOS and TNEG) is clocked into the R8069B by the falling edge of TCLK or EXCLK. The transmit data passes through an 8-bit transmit elastic store buffer which can accommodate up to 6 Unit Interval (UI) peak-peak jitter (fj > 10 Hz) and wander (fj < 10 Hz). The transmit data then goes to a line equalizer for pulse shaping and conditioning. The line equalizer will equalize up to 660 feet of 100 Ω ABAM cable (22-gauge plastic insulated cable with characteristics specified in Appendix B of the AT&T Technical Reference Number 34, September 1983)*.

Three encoded inputs, ELS1-ELS3, allow selection of cable length equalization and clock rates (Table 2). Equalization of cable length of 0-660 feet in increments of 110 feet is selectable for T-1 line. A 20 Ω resistor should be connected in series with 75Ω coaxial cable connector (see Figure 5 and Table 2).

The equalized data is then provided to a line driver. In T-1 applications the driver can drive a twisted pair cable of up to 660 feet. The isolated pulse template at the end of the cable (at DSX-1) meets the pulse shape requirement specified by AT&T Technical Advisory No. 34. In PCM30 mode, the R8069B LIU provides a pulse shape which meets the requirements of CCITT Recommendation G.703. The pulse shape is measured at the output of the transmit transformer. The upper and lower limits of the T-1 or PCM30 pulse template were used to qualify the pulse shape.

The DSX-1 pulse template for T-1 is specified by Table 3 and illustrated in Figure 8.

The output pulse waveform for PCM30 conforms to the template shown in Figure 9.

* The R8069B was tested using AT&T ABAM cable part no. 606-6/22 R6900.

Table 2. ELS1 - ELS3 Encoding

ELS3	ELS2	ELS1	Cable Length/ Line Impedance	Clock Rate[1]
L	L	L	0 - 110 ft	T-1
L	L	H	110 - 220 ft	T-1
L	H	L	220 - 330 ft	T-1
L	H	H	330 - 440 ft	T-1
H	L	L	440 - 550 ft	T-1
H	L	H	550 - 660 ft	T-1
H	H	L	75/120 Ω[2,3]	PCM30

NOTES:

1. T-1 = 1.544 Mbits/s; PCM30 = 2.048 Mbits/s.
2. See Figures 5 and 6.
3. If the selected equalization line code is ELS3 = H, ELS2 = H, and ELS1 = L, then a 20 Ω resistor is required at the line side of the transmit transformer (see Figure 5). This is the recommended mode in a 75 Ω PCM30 application to ensure that the pulse shape meets G.703.

   At the customer's option, the value ELS3 = H, ELS2 = H, and ELS1 = H may be selected and the 20Ω resistor can be deleted. In this configuration, the pulse shape will normally conform to G.703, but is not guaranteed in every case.

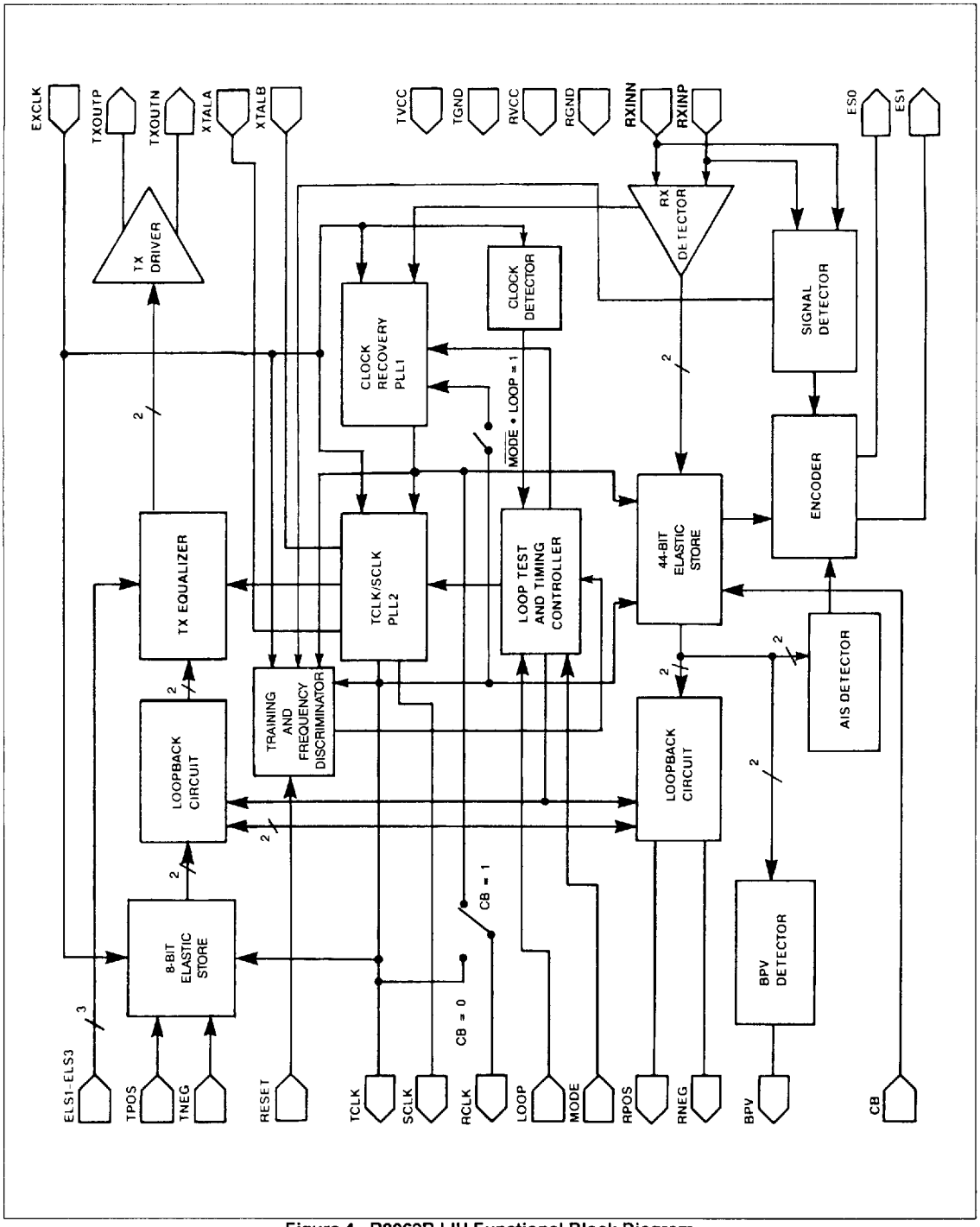


Figure 4. R8069B LIU Functional Block Diagram

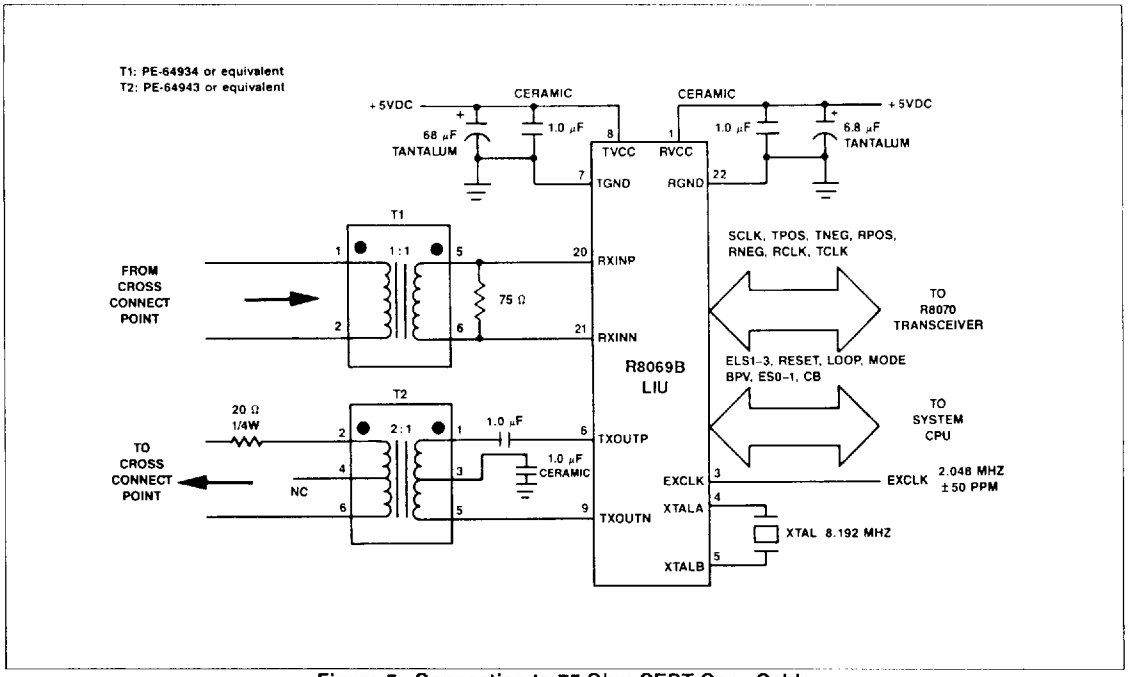


Figure 5. Connection to 75 Ohm CEPT Coax Cable

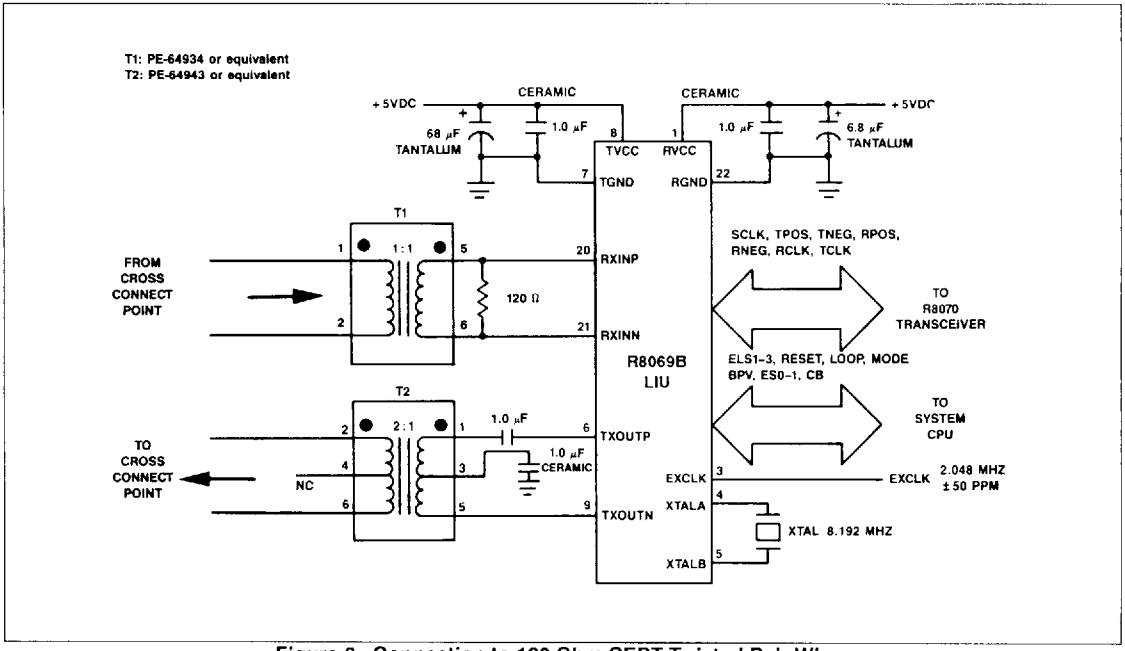


Figure 6. Connection to 120 Ohm CEPT Twisted Pair Wires

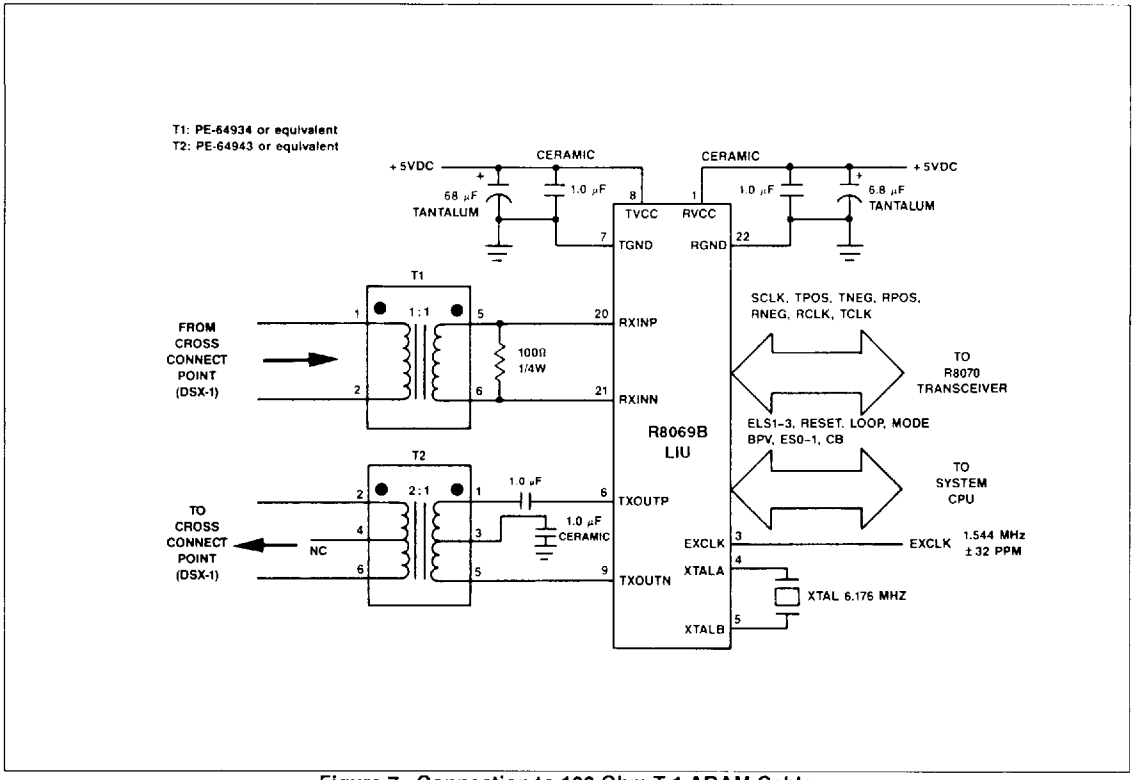


Figure 7. Connection to 100 Ohm T-1 ABAM Cable

Table 3. DSX-1 Pulse Template Corner Points (T-1)

Maximum Curve		Minimum Curve	
ns	Normalized Voltage	ns	Normalized Voltage
0	0.05	0	−0.05
250	0.05	350	−0.05
325	0.80	350	0.50
325	1.15	400	0.95
425	1.15	500	0.95
500	1.05	600	0.90
675	1.05	650	0.50
725	−0.07	650	−0.45
1100	0.05	800	−0.45
1250	0.05	925	−0.20
		1100	−0.05
		1250	−0.05

Note: Successive corner points are joined by straight lines to form the template shown in Figure 8.

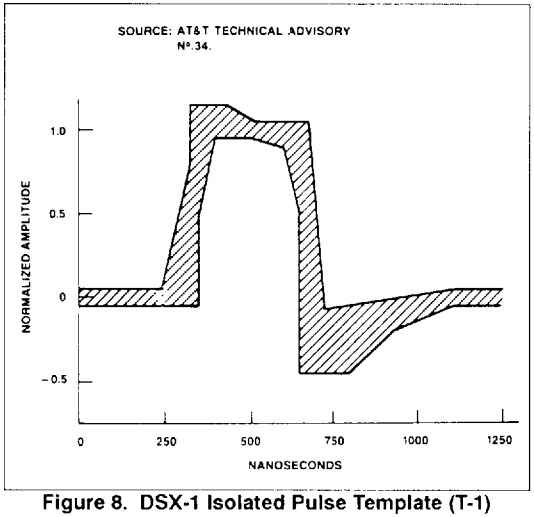
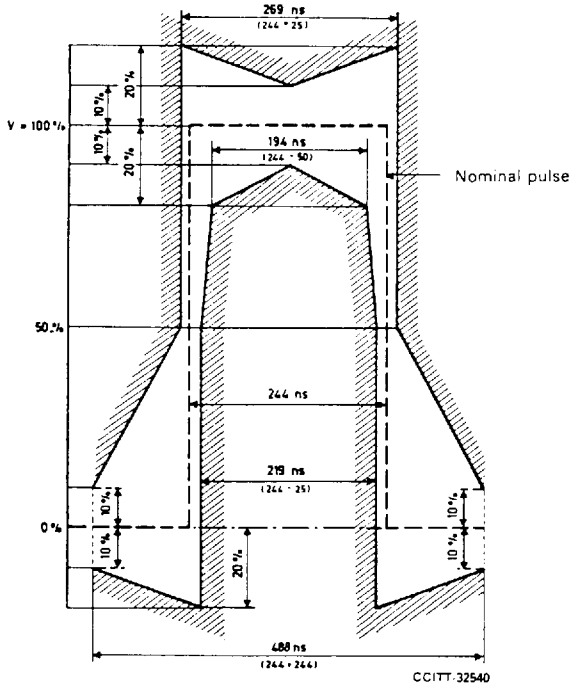


Figure 8. DSX-1 Isolated Pulse Template (T-1)



FOR
75 Ω LOAD IMPEDANCE: V = 2.37V
120 Ω LOAD IMPEDANCE: V = 3.00V
OPERATING FREQUENCY 2.048 MBPS
SOURCE: CCITT REC G.703

Figure 9. Isolated Pulse Template (PCM30)

RECEIVE SECTION

On the receive side, bipolar input data (RXINP and RXINN) is converted to unipolar signal (RPOS and RNEG). Phase locked loop 1 (PLL1) is used to recover the clock from the incoming bipolar data.

A second phase locked loop (PLL2) smooths the clock signal coming from PLL1 or the EXCLK input pin, and generates both Transmit Clock (TCLK) and System Clock (SCLK). TCLK represents the base frequency (1.544 MHz or 2.048 MHz) and SCLK is twice the base frequency. TCLK and SCLK are used as transmit clocks by the R8070 and R8071, respectively.

In master mode, PLL2 locks on the EXCLK as a reference if EXCLK is present. In the absence of EXCLK, PLL2 will reference the crystal-based clock source. In slave mode, PLL2 will use the output of PLL1 as a reference.

The receive section also contains a 44-bit elastic store buffer which can accommodate up to 40 UI peak-peak jitter and wander.

RECEIVER RESET

When the RESET input is asserted high, the clock recovery PLL1 locks to EXCLK or the crystal-based clock source for training. After RESET is switched low, PLL1 will again lock to the incoming receive data.

RECEIVER TRAINING MODE

Receiver training can be initiated by any of three ways (Figure 22 on page 22):

1. Loss of signal (receipt of 175 consecutive zeros) triggers training for a minimum period of 512 UI; 1 UI = 648 ns (T-1) or 488 ns (PCM30). If loss of signal still persists at the end of this period, the PLL1 continues to train. Training stops as soon as the received signal is a 1 bit.

2. Training is activated for 512 UI when the frequency difference of PLL1 and the reference clock exceeds 38 kHz. The frequency difference is measured by a frequency discriminator. The reference clock is the external clock at EXCLK input pin or TCLK if the external clock is absent.

3. Training is activated by asserting the RESET input and continues as long as RESET is high.

ALARM INDICATOR SIGNAL (AIS)

Alarm indicator signal (AIS) is asserted when the receive data consisting of 2316 unframed ones and less than 2 zeroes are detected. This condition is represented in the error status by ES0=L and ES1=L.

When multiple error status occurs, only the status that has the highest priority is reported. Both Loss of Signal and AIS share the highest priority. They are mutually exclusive. Elastic Buffer overflow/underflow has lower priority than AIS or Loss of Signal.

BIPOLAR VIOLATION

Bipolar violation is reported on the BPV output pin whenever any bipolar violations occur on the receive data. BPV generates a positive pulse of one unit interval at the falling edge of TCLK or RCLK. A unit interval is equivalent to 648 ns for T-1, or 488 ns for PCM30. (See Figures 15-18.)

RECEIVE ELASTIC STORE BUFFER

In order to avoid data loss due to jitter, a 44-bit elastic store is provided in the receive data path. It's function is to eliminate the effect of short term jitter resulting from transmission line impairments. The receive data is written into the elastic buffer by the Recovered Clock (RCLK) and read out from the elastic buffer by TCLK. The output of the elastic buffer drives the unipolar output signal (RPOS and RNEG).

When the receive elastic buffer is enabled (CB=L), RCLK is the same as TCLK. They will have the same phase and frequency relation. TCLK is generated from PLL2. When the receive elastic buffer is bypassed (CB=H), then RCLK is the recovered clock extracted from the receive data by PLL1, and is not in phase with TCLK. (See Figures 15 and 16.)

LOSS OF SIGNAL (LOS)

Loss of Signal indicates the received signal is less than 0.97 V for 175 bit times. It is represented by the Error Status output pins ES0=L and ES1=H. When Loss of Signal occurs, PLL2 uses either the external clock (EXCLK) or the crystal as an input to generate TCLK and SCLK. PLL1 locks onto EXCLK, if present, or onto TCLK. When receive data returns, PLL1 will lock back onto the receive data stream.

EXCLK ACTIVITY DETECTOR

The EXCLK activity detector monitors the presence of EXCLK. The absence of EXCLK is acknowledged if EXCLK has no transition for 16 consecutive TCLK periods. The EXCLK or the crystal is used as a reference by PLL2. (See Table 4.)

RECEIVE ONLY WITH TRANSMITTER FUNCTION DISABLED

The R8069B LIU transmitter is disabled and the TX line driver is put into high impedance (R_O > 10K Ω) under the following condition:

LOOP	= High	TPOS	= Low
MODE	= High	TNEG	= Low
RESET	= High		

In this mode, the receiver can be reset by asserting the MODE input low for at least 200 μs.

TEST MODE CONDITION

TPOS, TNEG, and RESET should not be set to high levels simultaneously because this will put the R8069B in a factory test mode.

MODE AND LOOP TIMING MODE

Mode and Loop modes are determined by the state of the MODE and LOOP pins. Refer to LOOP AND MODE SELECTION for selection details. For data alignment and clock sources, refer to Table 4.

MASTER TIMING MODES

Normal Operation without EXCLK

TCLK and SCLK reference the on-chip crystal oscillator nominal frequency while RCLK is based on TCLK (CB=0) or the recovered clock (CB=1). TPOS and TNEG are clocked in on the falling edge of TCLK. The source of TXOUTP/N is TPOS/TNEG. RPOS and RNEG are clocked out on the falling edge of RCLK. The source of RPOS/RNEG is RXINP/N.

Normal Operation with EXCLK

TCLK and SCLK reference EXCLK while RCLK references TCLK (CB=0) or the recovered clock (CB=1). TPOS and TNEG are clocked in on the falling edge of EXCLK. The source of TXOUTP/N is TPOS/TNEG. RPOS and RNEG are clocked out on the falling edge of RCLK. The source of RPOS/RNEG is RXINP/N.

Local Loopback without EXCLK

TCLK and SCLK reference the on-chip crystal oscillator nominal frequency while RCLK is based on TCLK. TPOS and TNEG are clocked in on the falling edge of TCLK. TXOUTP/N transmit all ones. RPOS and RNEG are clocked out on the falling edge of RCLK. The source of RPOS/RNEG is TPOS/TNEG.

Local Loopback with EXCLK

TCLK and SCLK reference EXCLK while RCLK references TCLK. TPOS and TNEG are clocked in on the falling edge of EXCLK. TXOUTP/N transmit all ones. RPOS and RNEG are clocked out on the falling edge of RCLK. The source of RPOS/RNEG is TPOS/TNEG.

Remote Loopback without EXCLK

TCLK and SCLK reference the on-chip crystal oscillator nominal frequency while RCLK is based on TCLK (CB=0) or the recovered clock (CB=1). TPOS and TNEG are clocked in on the falling edge of TCLK. The source of TXOUTP/N is RXINP/N. RPOS and RNEG are clocked out on the falling edge of RCLK. The source of RPOS/RNEG is RXINP/N.

Remote Loopback with EXCLK

TCLK and SCLK reference EXCLK while RCLK references TCLK (CB=0) or the recovered clock (CB=1). TPOS and TNEG are clocked in on the falling edge of EXCLK. The source of TXOUTP/N is RXINP/N. RPOS and RNEG are clocked out on the falling edge of RCLK. The source of RPOS/RNEG is RXINP/N.

SLAVE TIMING MODES

Normal Operation without EXCLK

TCLK and SCLK reference the recovered clock while RCLK references TCLK (CB=0) or the recovered clock (CB=1). TPOS and TNEG are clocked in on the falling edge of TCLK. The source of TXOUTP/N is TPOS/TNEG. RPOS and RNEG are clocked out on the falling edge of RCLK. The source of RPOS/RNEG is RXINP/N.

Normal Operation with EXCLK

TCLK and SCLK reference the recovered clock while RCLK references TCLK (CB=0) or the recovered clock (CB=1). TPOS and TNEG are clocked in on the falling edge of TCLK. The source of TXOUTP/N is TPOS/TNEG. RPOS and RNEG are clocked out on the falling edge of RCLK. The source of RPOS/RNEG is RXINP/N.

Table 4. Data and Clock Sources

Timing/ Operation Mode	Input Pins* M	Input Pins* L	EXCLK Supplied?	Source of TCLK and SCLK: No Data on RXINP/N	Source of TCLK and SCLK: Data on RXINP/N	TPOS/ TNEG Alignmnt	Source of TXOUTP/N	Source of RCLK: CB=0	Source of RCLK: CB=1 and Data on RXINP/N	Source of RCLK: CB=1 and NoData on RXINP/N	Source of RPOS/ RNEG	RPOS/ RNEG Alignment
Master												
Normal	L	L	N	XTAL	XTAL	TCLK	TPOS/TNEG	TCLK	RXINP/N	TCLK	RXINP/N	RCLK
Normal	L	L	Y	EXCLK	EXCLK	EXCLK	TPOS/TNEG	TCLK	RXINP/N	EXCLK	RXINP/N	RCLK
Local Loopback	L	H	N	XTAL	XTAL	TCLK	All Ones	TCLK	TCLK	TCLK	TPOS/TNEG	RCLK
Local Loopback	L	H	Y	EXCLK	EXCLK	EXCLK	All Ones	TCLK	TCLK	TCLK	TPOS/TNEG	RCLK
Remote Loopback	H	H	N	XTAL	XTAL	TCLK	RXINP/N	TCLK	RXINP/N	TCLK	RXINP/N	RCLK
Remote Loopback	H	H	Y	EXCLK	EXCLK	EXCLK	RXINP/N	TCLK	RXINP/N	EXCLK	RXINP/N	RCLK
Slave												
Normal	H	L	N	XTAL	RXINP/N	TCLK	TPOS/TNEG	TCLK	RXINP/N	TCLK	RXINP/N	RCLK
Normal	H	L	Y	EXCLK	RXINP/N	TCLK	TPOS/TNEG	TCLK	RXINP/N	EXCLK	RXINP/N	RCLK
Local Loopback	L	H	N	XTAL	RXINP/N	TCLK	All Ones	TCLK	TCLK	TCLK	TPOS/TNEG	RCLK
Local Loopback	L	H	Y	EXCLK	RXINP/N	TCLK	All Ones	TCLK	TCLK	TCLK	TPOS/TNEG	RCLK
Remote Loopback	H	H	N	XTAL	RXINP/N	TCLK	RXINP/N	TCLK	RXINP/N	TCLK	RXINP/N	RCLK
Remote Loopback	H	H	Y	EXCLK	RXINP/N	TCLK	RXINP/N	TCLK	RXINP/N	EXCLK	RXINP/N	RCLK

* M = MODE input; L = LOOP input.

Local Loopback without EXCLK

TCLK and SCLK reference the recovered clock while RCLK references TCLK. TPOS and TNEG are clocked in on the falling edge of TCLK. TXOUTP/N transmit all ones. RPOS and RNEG are clocked out on the falling edge of RCLK. The source of RPOS/RNEG is TPOS/TNEG.

Local Loopback with EXCLK

TCLK and SCLK reference the recovered clock while RCLK references TCLK. TPOS and TNEG are clocked in on the falling edge of TCLK. TXOUTP/N transmit all ones. RPOS and RNEG are clocked out on the falling edge of RCLK. The source of RPOS/RNEG is TPOS/TNEG.

Remote Loopback without EXCLK

TCLK and SCLK are based on the recovered clock while RCLK is based on TCLK (CB=0) or the recovered clock (CB=1). TPOS and TNEG are clocked in on the falling edge of TCLK. The source of TXOUTP/N is RXINP/N. RPOS and RNEG are clocked out on the falling edge of RCLK. The source of RPOS/RNEG is RXINP/N.

Remote Loopback with EXCLK

TCLK and SCLK are based on the recovered clock while RCLK is based on TCLK (CB=0) or the recovered clock (CB=1). TPOS and TNEG are clocked in on the falling edge of TCLK. The source of TXOUTP/N is RXINP/N. RPOS and RNEG are clocked out on the falling edge of RCLK. The source of RPOS/RNEG is RXINP/N.

MODE AND LOOP SELECTION

The basic modes of operation are as follows:

MODE	LOOP	Mode of Operation
Low	Low	Master Normal
High	Low	Slave Normal
Low	High	Master/Slave Local Loopback
High	High	Master/Slave Remote Loopback

MODE and LOOP signals are latched on the falling edge of EXCLK or TCLK (if no EXCLK is present) in master timing modes or on the falling edge of TCLK in slave timing modes.

The timing mode (master or slave) must be selected before local or remote loopback is selected. When a loopback mode is selected, the R8069B remembers the timing mode (master or slave) it was last in. Care must be taken while switching from one mode to another so as not to **unintentionally** change the timing mode. MODE and LOOP should not both be changed during the same clock cycle when switching from a normal timing mode to a loopback mode.

EXAMPLE 1. You are in slave normal and you want to switch to master remote loopback. Each change lasts a minimum of one clock cycle.

Current mode is slave normal	MODE = H	LOOP = L
Change to master normal	MODE = L	LOOP = L
Change to master local loopback	MODE = L	LOOP = H
Change to master remote loopback	MODE = H	LOOP = H

Final mode is master remote loopback.

EXAMPLE 2. You are in master normal and you want to switch to slave local loopback. Each change lasts a minimum of one clock cycle.

Current mode is master normal	MODE = L	LOOP = L
Change to slave normal	MODE = H	LOOP = L
Change to slave remote loopback	MODE = H	LOOP = H
Change to slave local loopback	MODE = L	LOOP = H

Final mode is slave local loopback.

R8069 JITTER CONFORMANCE

Input jitter tolerance, intrinsic output jitter and jitter transfer function of the R8069B surpasses the requirements set forth in AT&T Pub 62411 and CCITT Recommendation G.823.

Jitter is defined as a short term phase shift of a digital signal from its ideal position in time. Wander (jitter below 10 Hz) is a long term phase shift of a digital signal which may result due to change in the propagation delay of the transmission media being used.

Input jitter tolerance is the amount of jitter that the Data Terminal Equipment (DTE) can accept in its input signal and still be able to operate with specified bit error rate (BER $<10^{-8}$). The input jitter tolerance of the R8069B is shown in Figure 10. The input jitter tolerance of the R8069B PLL clock recovery circuit is shown in Figure 11.

Intrinsic output jitter is the inherent jitter generated within the individual equipment when the input signal is jitter free. The R8069B's novel PLL utilizes a parallel resonant crystal in order to achieve a very low intrinsic output jitter. The maximum intrinsic output jitter is shown in Figure 12.

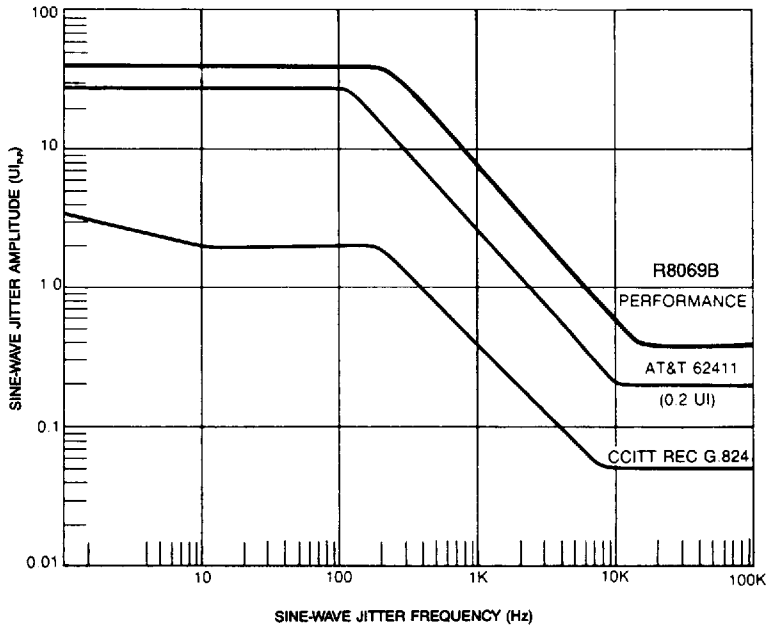
Jitter transfer function represents the amount of jitter that is carried over from the input signal to the output signal. The R8069B advanced design minimizes this transference of jitter from the input signal to the output signal as depicted in Figure 13.

The test setup to measure the DTE jitter transfer function is shown in Figure 14.

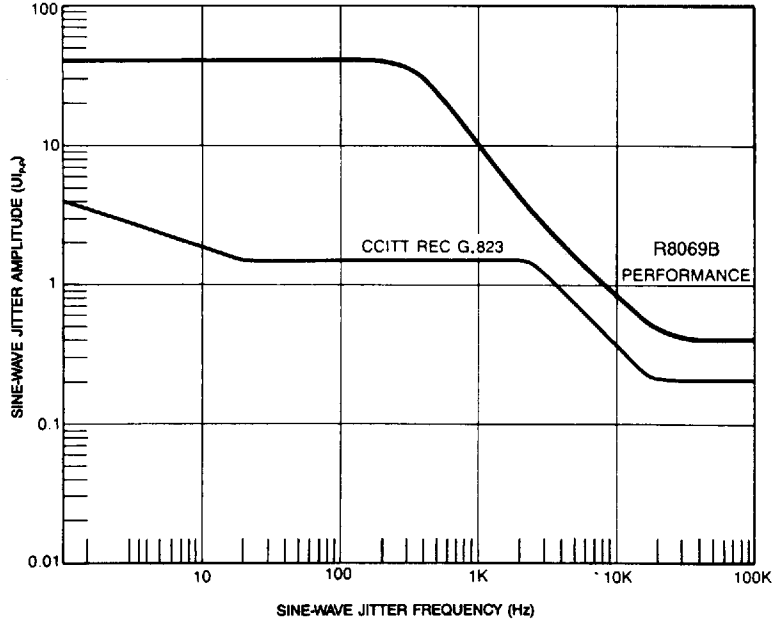
RECEIVE AND TRANSMIT WAVEFORMS

Receive waveforms with elastic store enabled and bypassed are shown in Figures 15 and 16, respectively.

Transmit waveforms for master mode with and without EXCLK source are shown in Figures 17 and 18, respectively. Transmit waveforms for slave mode are shown in Figure 19.



1.544 MHz Operation



2.048 MHz Operation

Figure 10. R8069B Input Data Jitter Tolerance

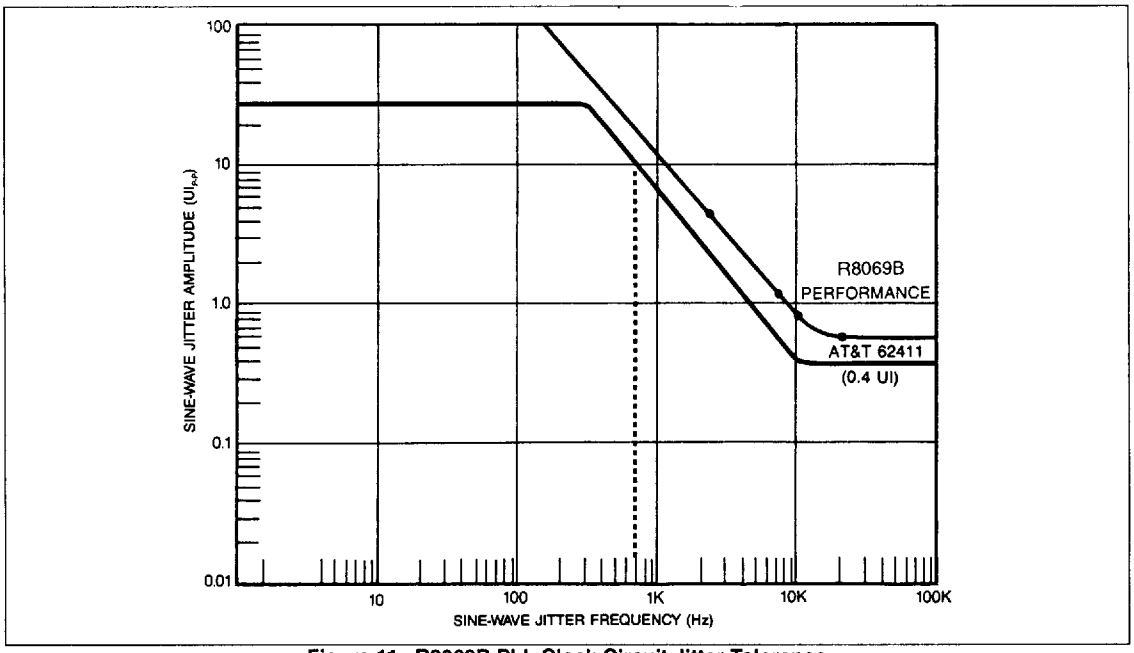


Figure 11. R8069B PLL Clock Circuit Jitter Tolerance

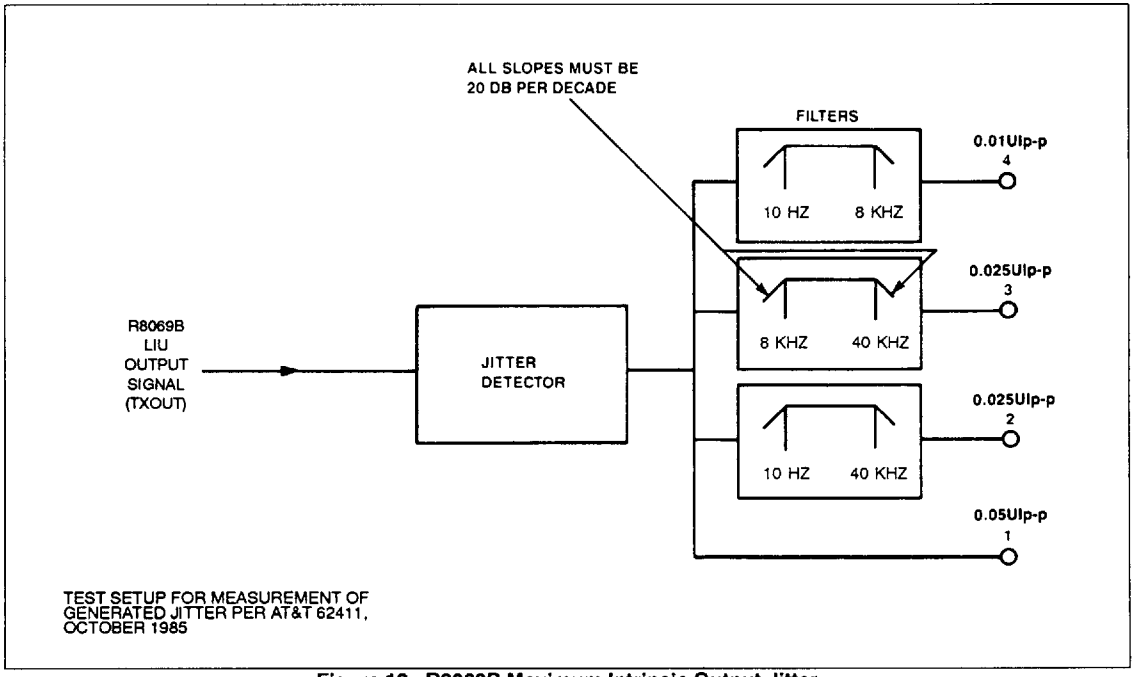


Figure 12. R8069B Maximum Intrinsic Output Jitter

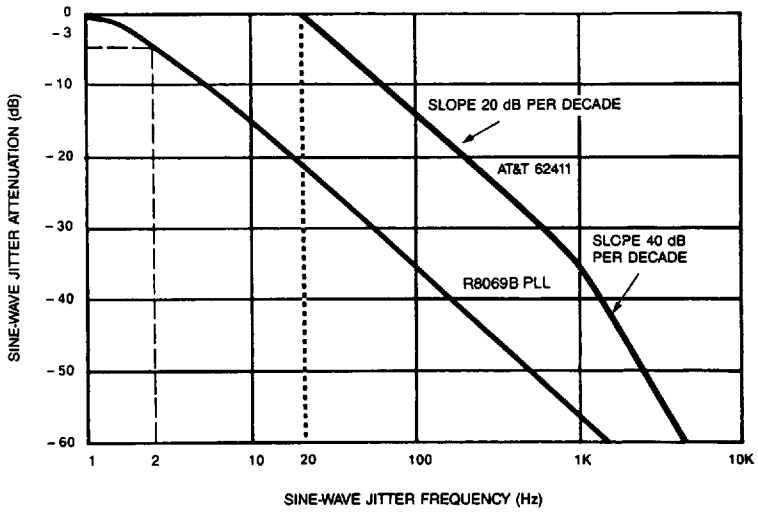


Figure 13. R8069B Jitter Transfer Function

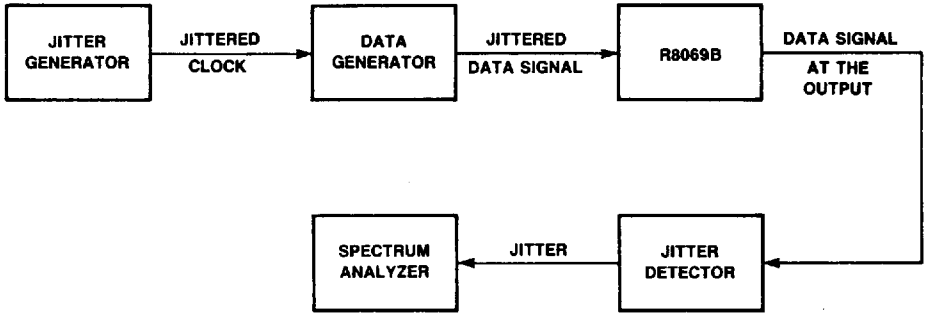


Figure 14. Measurement of DTE Jitter Transfer Function

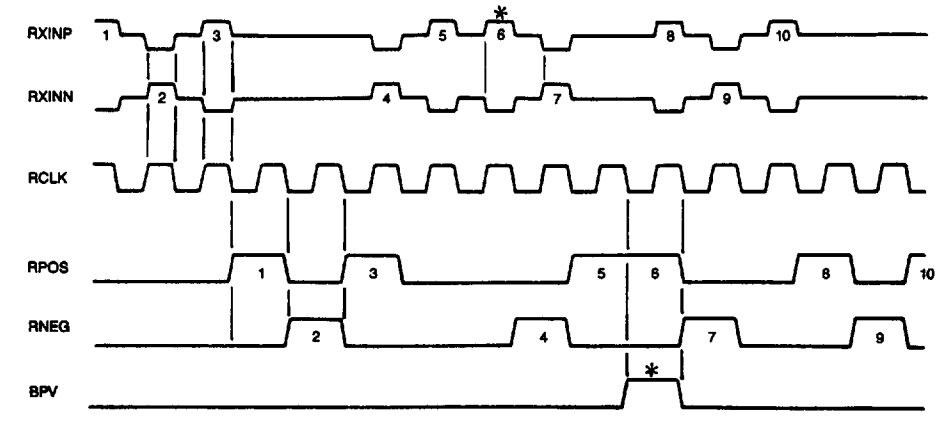


Figure 15. Receive Waveforms-Elastic Store Bypass (CB=1)

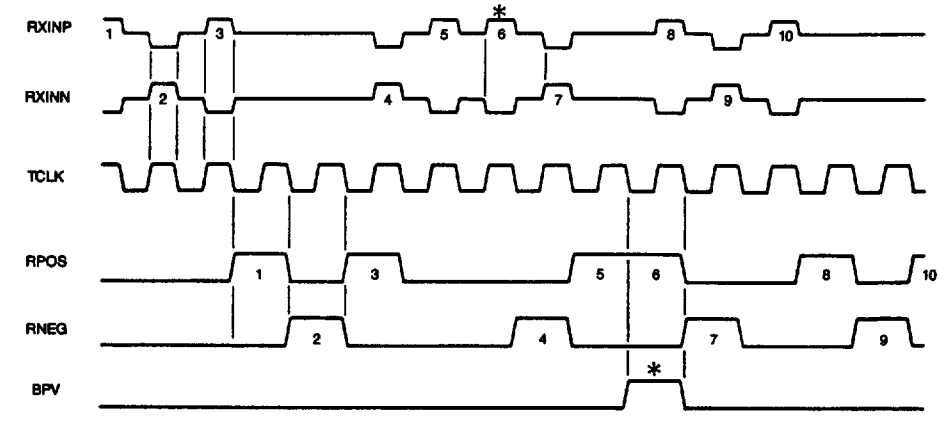


Figure 16. Receive Waveforms-Elastic Store Enable (CB=0)

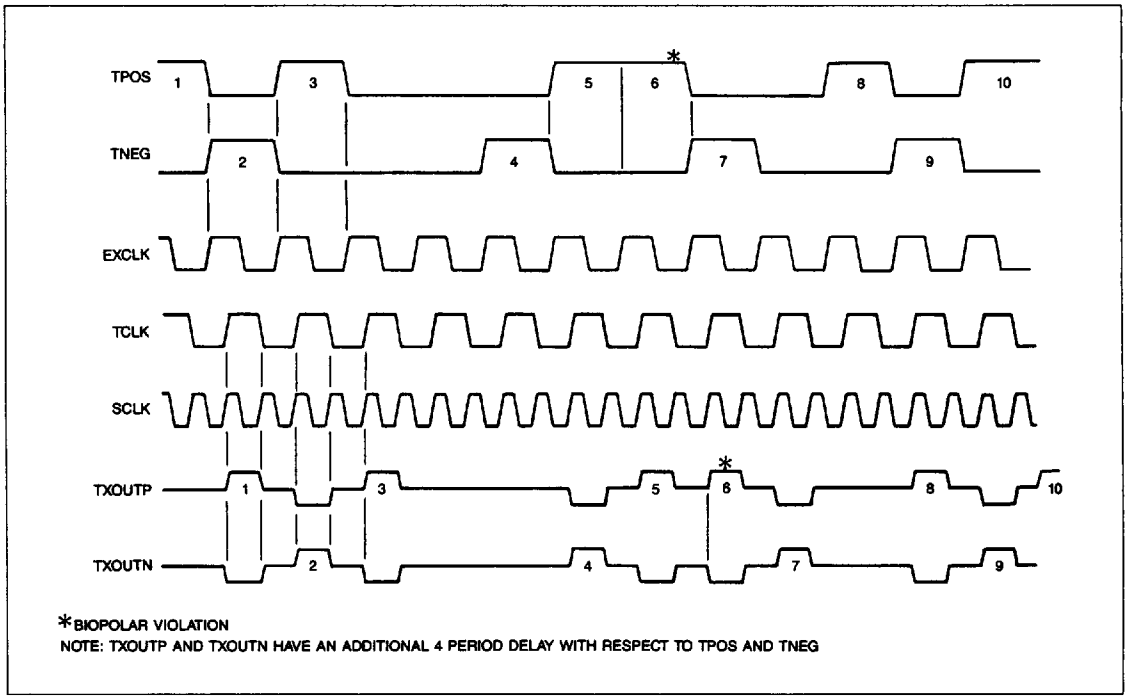


Figure 17. Transmitter Waveforms-Master with EXCLK

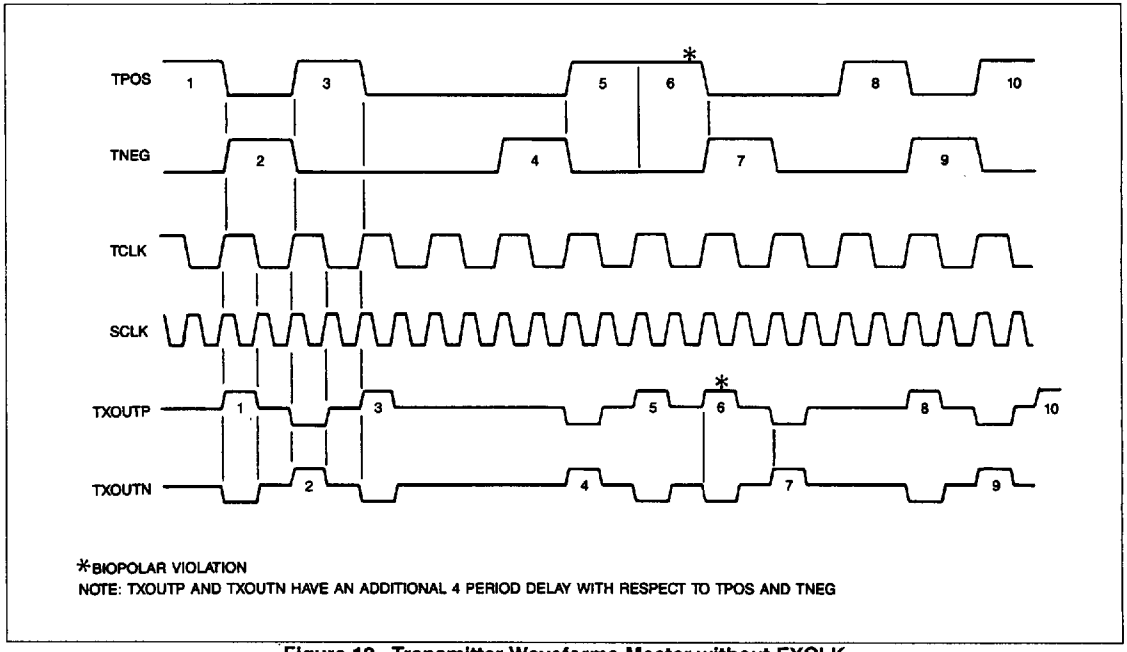
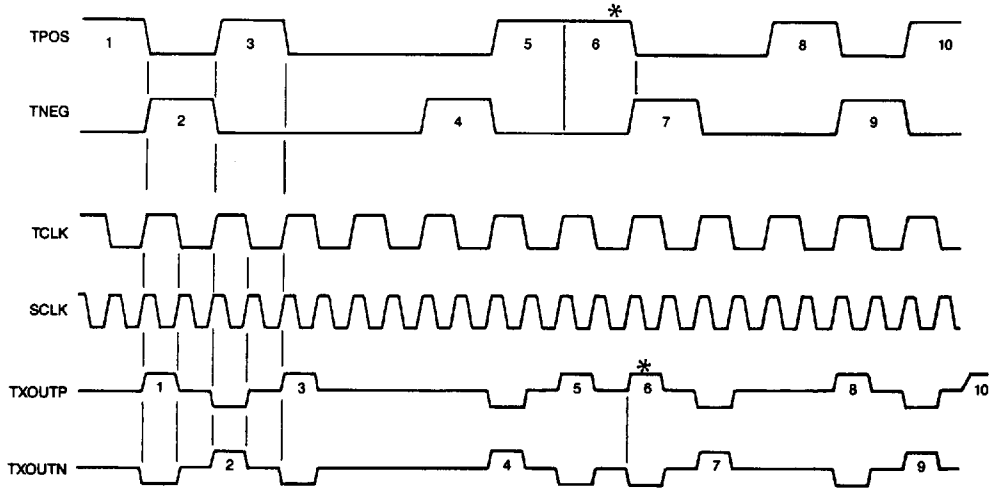


Figure 18. Transmitter Waveforms-Master without EXCLK



*BIPOLAR VIOLATION
NOTE: TXOUTP AND TXOUTN HAVE AN ADDITIONAL 4 PERIOD DELAY WITH RESPECT TO TPOS AND TNEG

Figure 19. Transmitter Waveforms-Slave Mode

SYSTEM APPLICATIONS

The R8069B can be used in a wide variety of applications for North American T-1, European PCM30, and world-wide ISDN Primary Rate Services. PBXs, Channel Banks, Computer System Interface, Network Switches, and Multiplexers are a few of the many systems in which the R8069B can be effectively used. Figures 20 and 21 illustrate two applications.

Application Note, *R8069/R8069A Interface Transformer Specifications and Connections,* Order No. 340, also applies to the R8069B.

INTERFACE REQUIREMENTS

Table 5 defines the general R8069B interface requirements.

The recommended crystal and transformer specifications are defined in Tables 6 and 7, respectively.

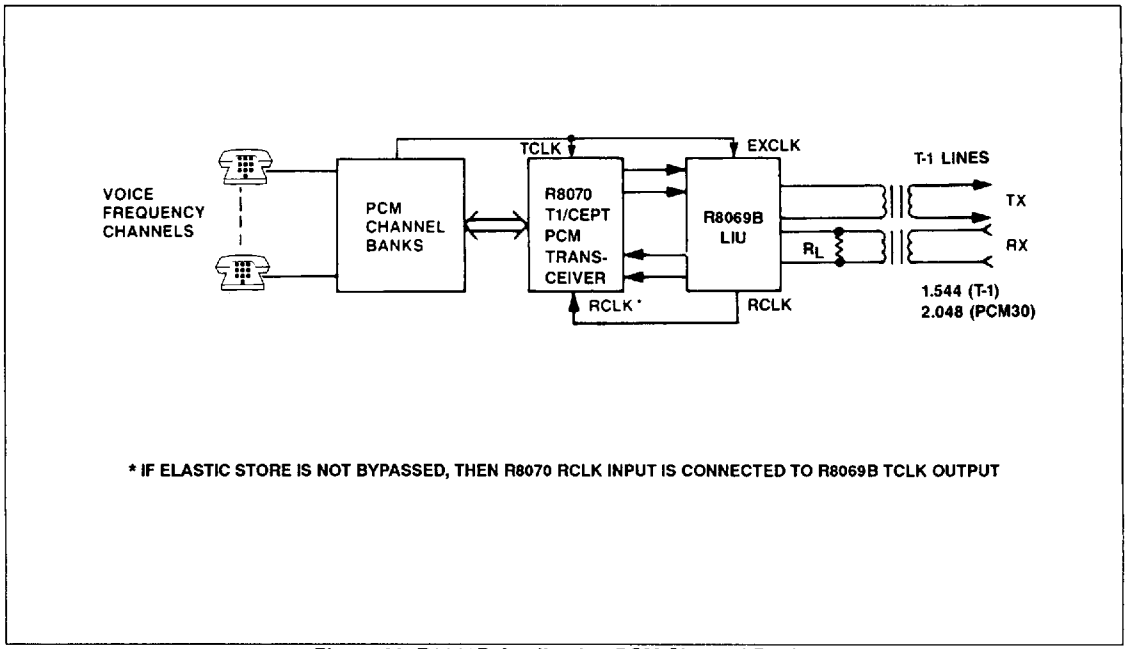


Figure 20. R8069B Application PCM Channel Banks

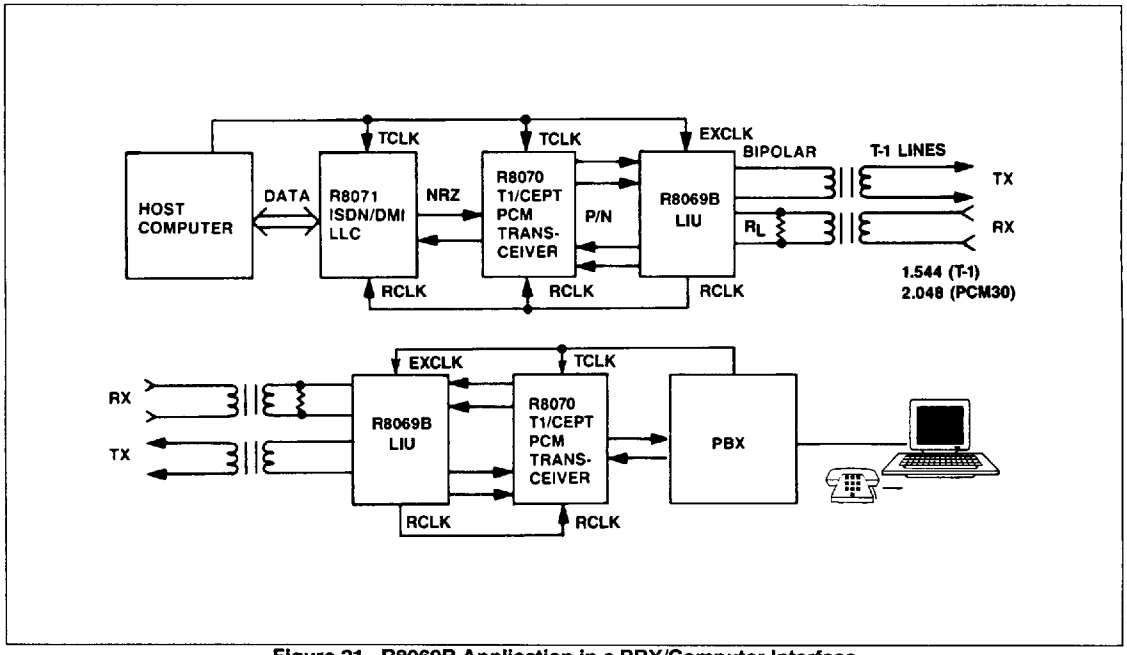


Figure 21. R8069B Application in a PBX/Computer Interface

Table 5. General Interface Requirements

Characteristic	Value
Operation	4-wire full-duplex balanced lines (T-1 or PCM30) or coax cable (PCM30)
Transmit Pulse Requirements	
Transmit Level	
1.544 Mbps (T-1)	3 V (nominal). Fits the pulse shape template in DSX-1 Interconnect Specification (T-1)
2.048 Mbps (PCM30)	3 V (nominal). Fits the pulse shape template in CCITT Rec. G.703. 2.37 V (nominal). Fits the pulse shape template in CCITT Rec. G.703.
Transmit Pulse Width	
1.544 Mbps (AT&T & CCITT)	324 ns (nominal)
2.048 Mbps (CCITT)	244 ns (nominal)
Transmit Clock Accuracy	
Meets AT&T requirement	1.544 MHz ±32 ppm *
Meets CCITT requirement	1.544 MHz ±50 ppm*
Meets CCITT requirement	2.048 MHz ±50 ppm*
	* When used with a crystal and EXCLK meeting recommended specifications.
Receive Clock Tolerance	
Meets AT&T requirement	1.544 MHz ±130 ppm**
Meets CCITT requirement	1.544 MHz ±50 ppm**
Meets CCITT requirement	2.048 MHz ±50 ppm**
	** When used with a crystal meeting recommended specifications.
Input Jitter Tolerance	40 UI_{P-P}
Receiver Sensitivity	10 dB below DSX-1 or G.703 specification
Diagnostics	Local and remote loopback
Transmitter Transformer Test Load Impedance	
1.544 Mbps (AT&T & CCITT)	100 Ω resistive
2.048 Mbps (CCITT)	120 Ω /75 Ω resistive
Interface to R8070/RT9170/R8071	
Level	CMOS/TTL compatible
Clock timing	Meets R8070/RT9170/R8071 timing specifications
Data from R8070 or RT9170	Unipolar data to be transmitted on primary rate lines (TPOS and TNEG)
Data to R8070 or RT9170	Unipolar data received from primary rate lines (RPOS and RNEG)
Clocks to R8070/RT9170/R8071	
Recovered Clock	RCLK
Transmit clock	TCLK
System Clock	SCLK (= 2 x TCLK)

Table 6. Recommended Crystal Specifications

Parameter	Value
Nominal Frequency @ 25°C	
T-1	6.176000 MHz
PCM30	8.192000 MHz
Operating Temperature	0°C to 70°C
Storage Temperature	– 40°C to 85°C
Oscillator Mode	Fundamental
Resonance Mode	Parallel
Load Capacitance (C_L)	14 pF (see note 2)
Frequency Tolerance @ 25°C	± 0.001% (±10 ppm)
Temperature Stability @ 0°C to 70°C	± 0.003% (±30 ppm)
Pullability @ 25°C and C_L = 9.8 pF	
T-1	+200 ppm min.
PCM30	+120 ppm min.
Pullability @ 25°C and C_L = 23.0 pF	
T-1	–200 ppm min.
PCM30	–120 ppm min
Maximum Drive Level	2.5 mW
Series Resistance	50 Ω max.
Maximum Aging Per Year	2 ppm

Notes:

1. This table is an example of typical crystal requirements for a system design with a pulling range of ± 130 ppm.

   For different pulling range requirements, refer to Application Note, R8069-Series Crystal Specifications, Order No. 355.

2. C_L includes typical 3.3 pF load capacitance due to board layout, crystal lead capacitance, and other stray capacitance , i.e.,
   $C_L = C_{LIU\ LOAD} + C_{OTHER}$
   = 10.7 pF + 3.3 pF = 14 pF

Table 7. Recommended R8069B Transformer

Parameter	Value
Transmit Transformer	
Turn Ratio	1CT:2CT
Rise/Fall Time	22 ns max.
Serial Resistance	0.7 Ω max.
Primary Inductance	1 mH min.
Isolation Voltage	1500 Vrms
Insulation Resistance	10,000 MΩ min.
Average Power Rating	500 mW
Leakage Inductance	0.30 µH - 0.55 µH
Receive Transformer	
Turn Ratio	1:1
Rise/Fall Time	22 ns max.
Serial Resistance	0.7 Ω max.
Primary Inductance	1 mH min.
Isolation Voltage	1500 Vrms
Insulation Resistance	10,000 MΩ min.
Average Power Rating	500 mW
Leakage Inductance	0.55 µH max.

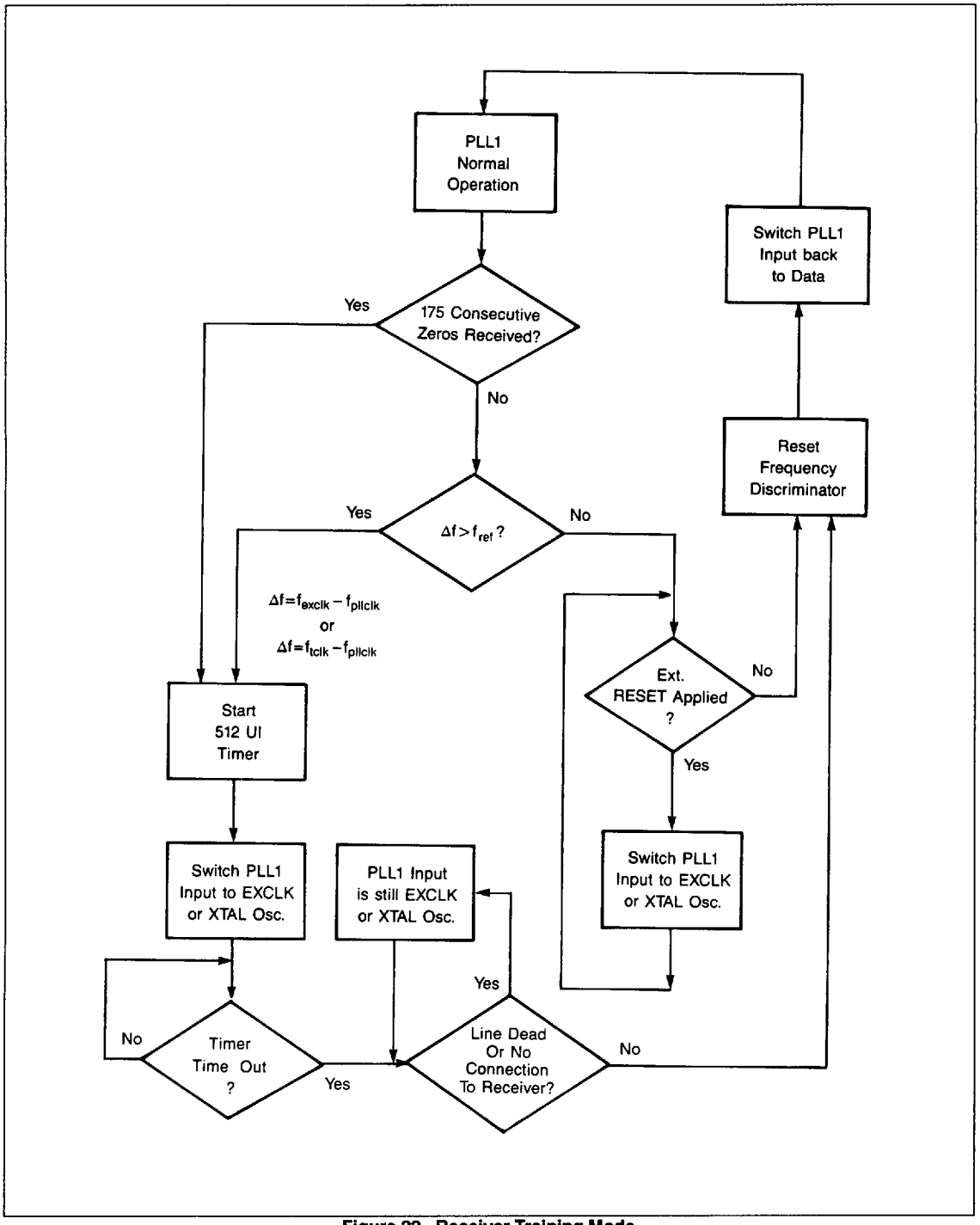
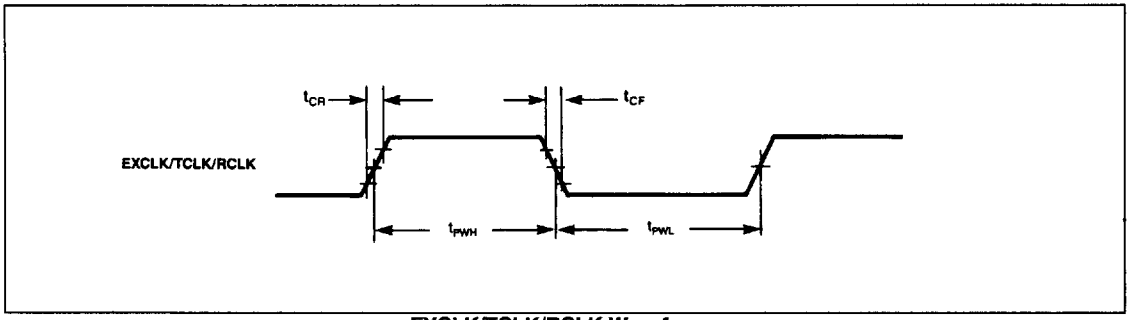
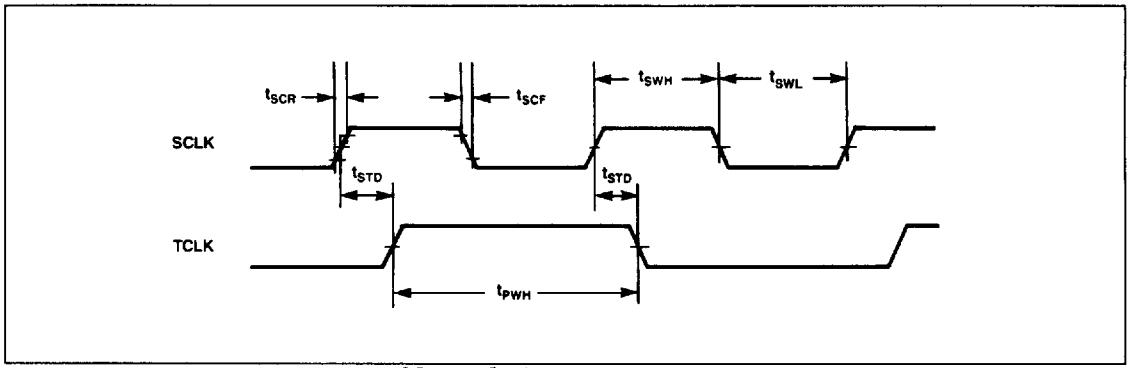


Figure 22. Receiver Training Mode

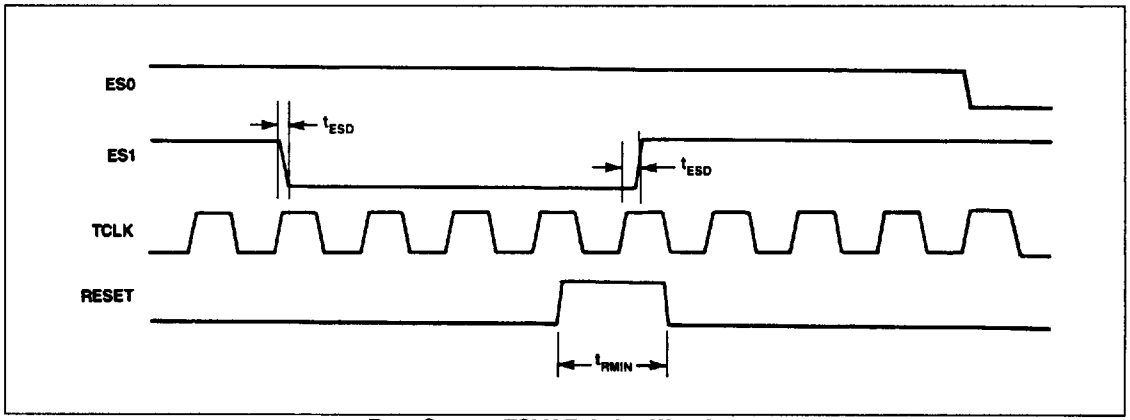
SWITCHING CHARACTERISTICS - WAVEFORMS



EXCLK/TCLK/RCLK Waveforms

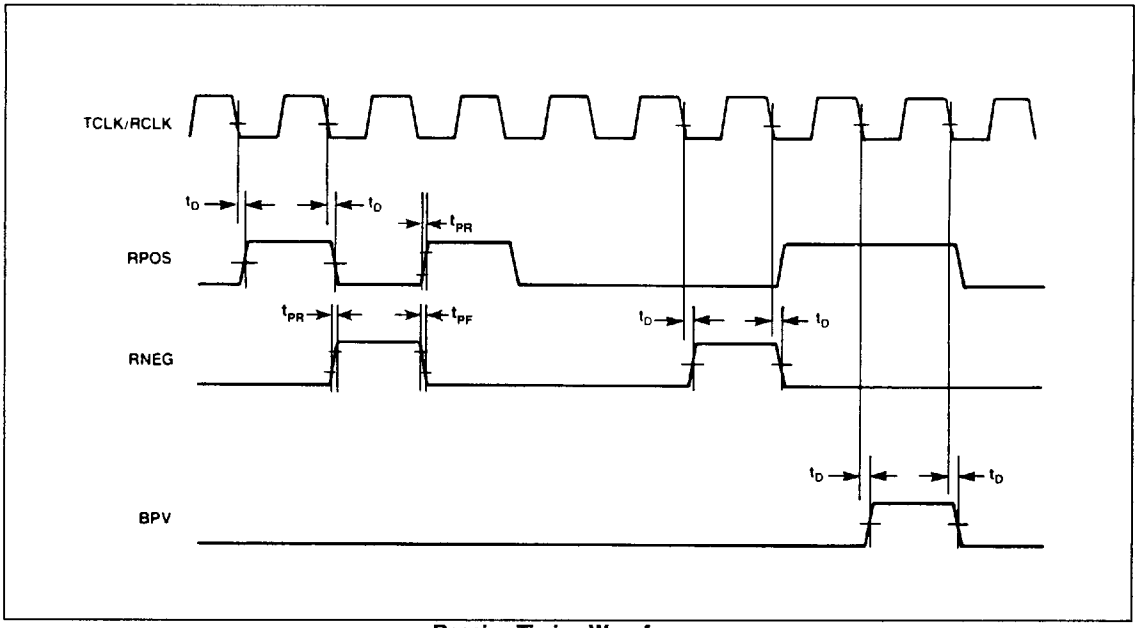


SCLK - TCLK Relation Waveforms

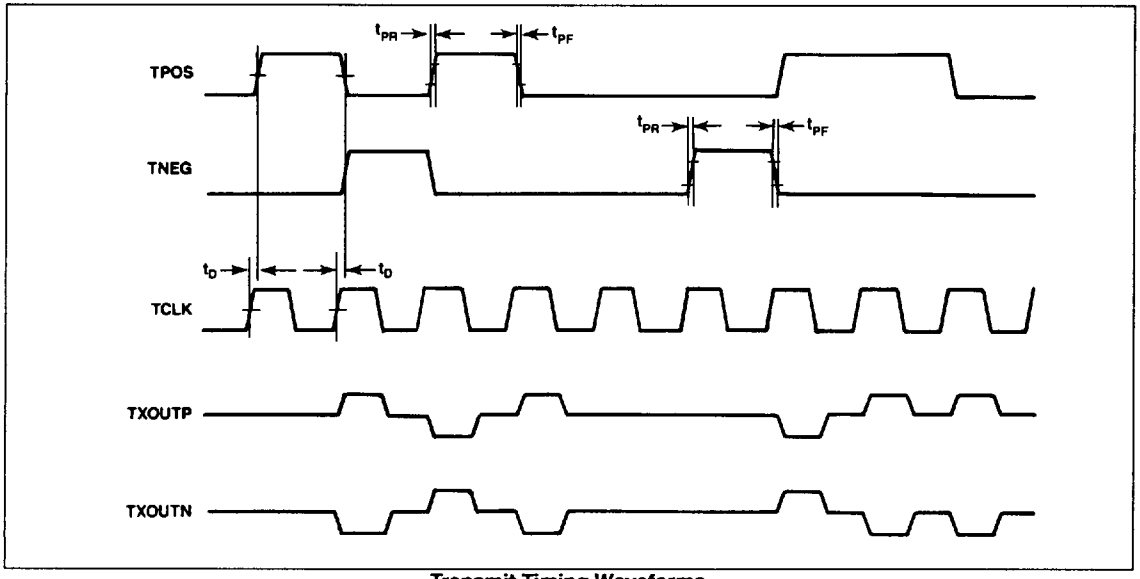


Error Status - TCLK Relation Waveforms

SWITCHING CHARACTERISTICS - WAVEFORMS (CONT'D)



Receive Timing Waveforms



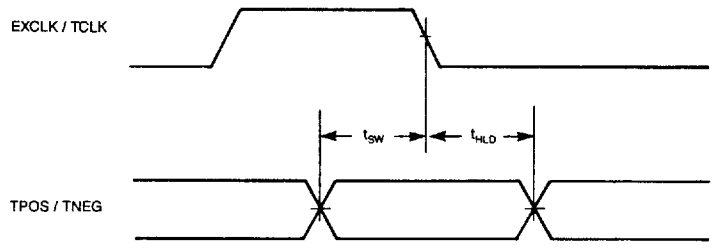
Transmit Timing Waveforms

SWITCHING CHARACTERISTICS

(V_{CC} = 5.0 Vdc ± 5%, V_{SS} = 0 Vdc, T_A= 0°C to 70°C, unless otherwise specified)

Parameter	Symbol	Min.	Max.	Units	Notes
Rise and Fall time					
RCLK, TCLK	t_{CR}, t_{CF}	–	20	ns	1
SCLK	t_{SCR}, t_{SCF}	–	10	ns	1
EXCLK	t_{CR}, t_{CF}	–	30	ns	
Rise and Fall time, TPOS, TNEG, RPOS, RNEG, BPV, ES0, ES1	t_{PR}, t_{PF}	–	60	ns	
Delay Time					
TCLK (or RCLK) to RPOS, RNEG, BPV	t_D		80	ns	
SCLK to TCLK	t_{STD}		50	ns	
TCLK to Error Status VALID	t_{ESD}		80	ns	
RESET Pulse Width	t_{RMIN}	200	–	µs	
T-1					
Pulse Width, TCLK or RCLK Low	t_{PWL}	314	334	ns	2
Pulse Width, TCLK or RCLK High	t_{PWH}	314	334	ns	2
Pulse Width, SCLK Low	t_{SWL}	157	167	ns	
Pulse Width, SCLK High	t_{SWH}	157	167	ns	
PCM30					
Pulse Width, TCLK or RCLK Low	t_{PWL}	234	254	ns	2
Pulse Width, TCLK or RCLK High	t_{PWH}	234	254	ns	2
Pulse Width, SCLK or SCLK Low	t_{SWL}	117	127	ns	
Pulse Width, SCLK or SCLK High	t_{SWH}	117	127	ns	
Set Up and Hold time for EXCLK					
TPOS, TNEG	t_{SW}	150		ns	
TPOS, TNEG	t_{HLD}	150		ns	

Notes:
1. TCLK, RCLK, and SCLK rise and fall times are defined as TTL levels.
2. The summation of t_{PWL} and t_{PWH} must meet the frequency specifications listed in the Interface Requirements table.



TPOS/TNEG Set Up and Hold Time

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Units
Supply Voltage	V_{CC}	–0.3 to +7.0	Vdc
Input Voltage	V_{IN}	–0.3 to V_{CC} + 0.3	Vdc
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{STG}	–55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

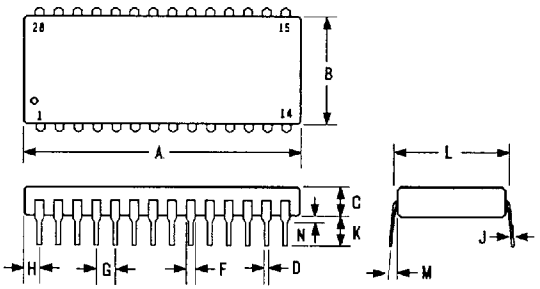
ELECTRICAL OPERATING CHARACTERISTICS[1]

(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Condition
Input Low Voltage	V_{IL}	–0.3	–	+0.8	V	
Input High Voltage	V_{IH}	+2.0	–	VCC +0.3	V	
Output Low Voltage	V_{OL}	–	–	0.4	V	I_{LOAD} = 1.6 mA
Output High Voltage						
TTL	V_{OH}	2.4	–	–	–	I_{LOAD} = –100 µA
CMOS	–	3.5	–	–	–	I_{LOAD} = –100 µA
Output Low Current	I_{OL}	+1.6	–	–	mA	V_{OL} = 0.4V
Output High Current	I_{OH}	–100	–	–	µA	V_{OH} = 3.5V
Input Capacitance	C_{IN}	–	–	5	pF	
Power Dissipation[2]	P_D				mW	
T-1 Mode						
Transmit Random Data						
330 ft.		–	270	305		
655 ft.		–	280	360		
Transmit All Ones						
330 ft.		–	350	430		
655 ft.		–	410	480		
PCM30 Mode						
Transmit Random Data		–	240	280		
Transmit All Ones		–	310	360		
Power Consumption[2]	P_C				mW	
T-1 Mode						
Transmit Random Data						
330 ft.		–	300	375		
655 ft.		–	340	410		
Transmit All Ones						
330 ft.		–	420	500		
655 ft.		–	500	570		
PCM30 Mode						
Transmit Random Data		–	260	300		
Transmit All Ones		–	350	400		
Parametric Tests						
Input High Current	I_{IH}	–	–	20	µA	V_{CC} = max., V_{IH} = 2.0V
Input Low Current	I_{IL}	–	–	20	µA	V_{CC} = max., V_{IL} = 0.8V

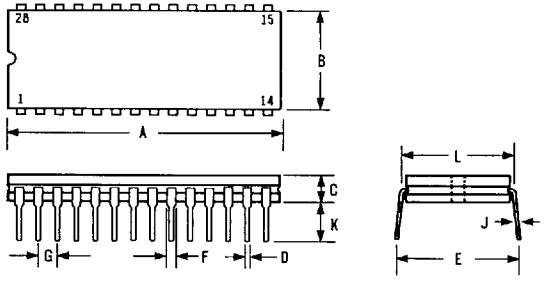
Notes: 1. Applies to all signals except TXOUTP, TXOUTN, RXINP and RXINN.
2. Power Consumption = Power dissipated in the device plus power delivered to the transmission line.

PACKAGE DIMENSIONS



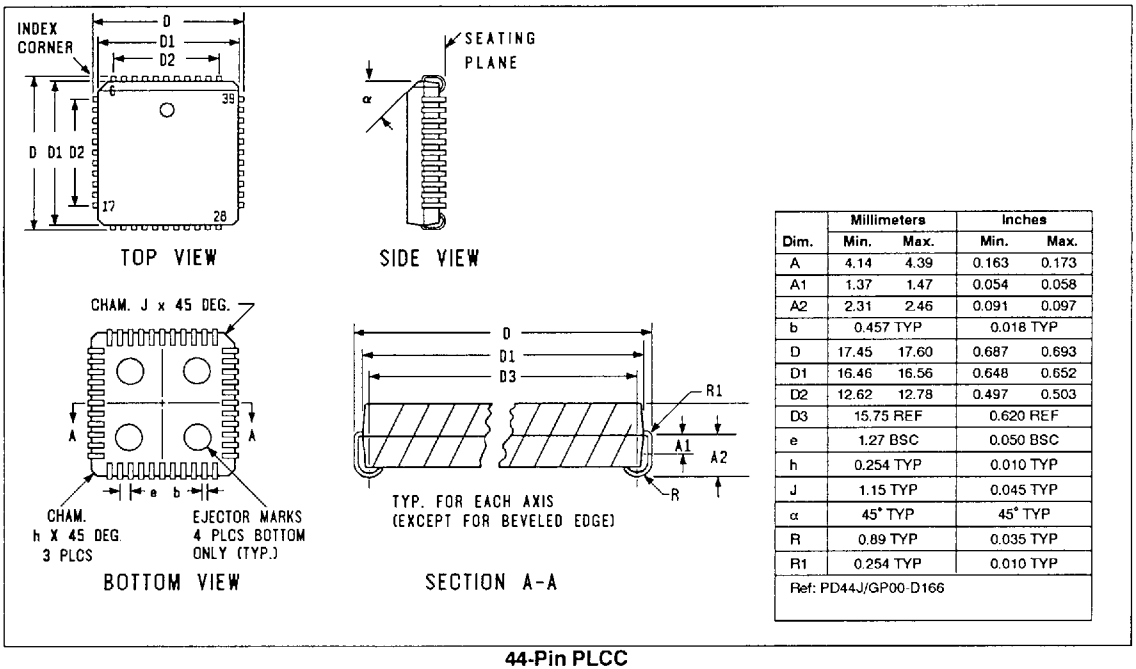
Dim.	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	36.58	37.08	1.440	1.460
B	13.46	13.97	0.530	0.550
C	3.56	4.06	0.140	0.160
D	0.38	0.53	0.015	0.021
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040
Ref: PD28P/GP00-D136				

28-Pin Plastic DIP



Dim.	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	36.32	37.34	1.430	1.470
B	12.95	13.46	0.510	0.530
C	3.68	4.19	0.145	0.165
D	0.41	0.51	0.016	0.020
E	16.26	17.27	0.640	0.680
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	4.19	4.95	0.165	0.195
L	15.24 BSC		0.600 BSC	
M	0°	10°	0°	10°
Ref: PD28S/GP00-D310				

28-Pin CERDIP



Dim.	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	4.14	4.39	0.163	0.173
A1	1.37	1.47	0.054	0.058
A2	2.31	2.46	0.091	0.097
b	0.457 TYP		0.018 TYP	
D	17.45	17.60	0.687	0.693
D1	16.46	16.56	0.648	0.652
D2	12.62	12.78	0.497	0.503
D3	15.75 REF		0.620 REF	
e	1.27 BSC		0.050 BSC	
h	0.254 TYP		0.010 TYP	
J	1.15 TYP		0.045 TYP	
α	45° TYP		45° TYP	
R	0.89 TYP		0.035 TYP	
R1	0.254 TYP		0.010 TYP	

Ref: PD44J/GP00-D166

44-Pin PLCC

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