Rockwell

R96EFX 9600 bps MONOFAX® Modem with Error Detection

INTRODUCTION

The Rockwell R96EFX MONOFAX modem is a synchronous 9600 bits per second (bps) half-duplex modem with error detection. The modem is housed in a single VLSI device package.

The modem can operate over the public switched telephone network (PSTN) through line terminations provided by a data access arrangement (DAA).

The R96EFX is designed for use in Group 3 and Group 2 facsimile machines.

The modem satisfies the requirements specified in CCITT recommendations V.29, V.27 ter, V.21 Channel 2, T.3, and T.4, and meets the binary signaling requirements of T.30.

The modem can operate at 9600, 7200, 4800, 2400, or 300 bps, and also includes the V.27 ter short training sequence option.

The modem can also perform HDLC framing according to T.30 at 9600, 7200, 4800, 2400, or 300 bps.

The voice mode allows the host computer to efficiently transmit and receive audio signals and messages.

The modem includes three programmable tone detectors which operate concurrently with the V.21 channel 2, Group 2, and voice mode receivers.

The modem is available in either a 68-pin plastic leaded chip carrier (PLCC) package or a 64-pin quad in-line package (QUIP). Figure 1 shows the modem in the PLCC. The general modem interface is illustrated in Figure 2.

Additional modem information is described in the 9600 bps MONOFAX Modem Designer's Guide (Order No. 820).

FEATURES

- Group 3 and Group 2 facsimile transmission/reception
  - CCITT V.29, V.27 ter, T.30, V.21 Channel 2 (FSK), T.3, T.4
  - HDLC Framing at all speeds
- V.27 ter short train
- Voice mode transmission/reception
- Half-duplex (2-Wire)
- Concurrent FSK and tone reception
- Maximum transmit level: 0 dBm programmable to –15 dBm
- Receive dynamic range: 0 dBm to –43 dBm
- Programmable dual tone generation
- Programmable tone detection
- Programmable turn-on and turn-off thresholds
- Programmable interface memory interrupt
- Diagnostic capability
  - Allows telephone line quality monitoring
- Equalization
  - Automatic adaptive
  - Selectable compromise cable
- DTE interface: two alternate ports
  - Selectable microprocessor bus (6500 or 8085)
  - CCITT V.24 (EIA-232-D compatible) interface
- TTL and CMOS compatible
- Low power consumption: 370 mW (typical)
- Single Package
  - 68-pin PLCC
  - 64-pin QUIP
- Compatible with R144EFX, R96MFX, R96DFX, and R96VFX modems

Document No. 29200N49 **Data Sheet** **Order No. MD49**
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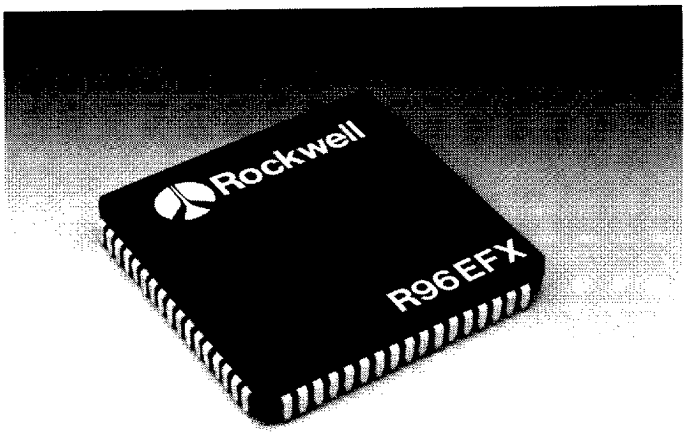


Figure 1. R96EFX MONOFAX Modem in 68-Pin PLCC

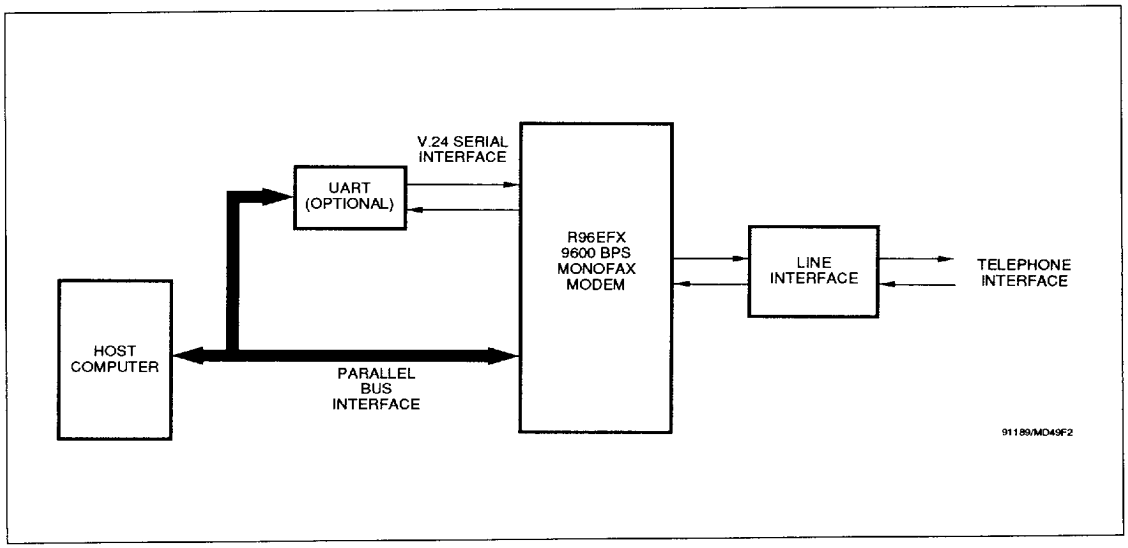


Figure 2. R96EFX MONOFAX Modem General Interface

TECHNICAL SPECIFICATIONS

Configurations, Signaling Rates And Data Rates

The selectable modem configurations, along with the corresponding signaling (baud) rates and data rates, are listed in Table 1.

Tone Generation

The modem can generate voice-band single or dual tones from 0 Hz to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3000 Hz are attenuated. Dual tone generation allows the modem to operate as a programmable DTMF dialer.

Data Encoding

The data encoding conforms to CCITT recommendations V.29, V.27 ter, V.21 Channel 2, and T.3.

Automatic Adaptive Equalizer

An adaptive equalizer in V.29 and V.27 ter modes compensates for transmission line amplitude and group delay distortion.

Compromise Cable Equalizers

Compromise equalization can improve performance when operating over low quality lines. Equalizer characteristics for cable lengths of 0, 1.8, 3.6, or 7.2 km are selectable by two hardware input pins (see CABLE1 and CABLE2 signal description in Table 9). The selected filter operates in both transmit and receive paths.

Transmitted Data Spectrum

The transmitted data spectrum is shaped in the baseband by an excess bandwidth finite impulse response (FIR) filter with the following characteristics:

When operating at 2400 baud, the transmitted spectrum is shaped by a square root of 20% raised cosine filter.

When operating at 1600 baud, the transmitted spectrum is shaped by a square root of 50% raised cosine filter.

When operating at 1200 baud, the transmitted spectrum is shaped by a square root of 90% raised cosine filter.

The transmit spectrum characteristics assume that the cable equalizers are disabled.

The out-of-band transmitter energy levels in the 4 kHz – 50 kHz frequency range are below –55.0 dBm.

Turn-on Sequence

Transmitter turn-on sequence times are shown in Table 2.

Turn-off Sequence

For V.27 ter, the turn-off sequence consists of approximately 10 ms of remaining data and scrambled ones at 1200 baud or approximately 7 ms of data and scrambled ones at 1600 baud followed by a 20 ms period of no transmitted energy.

For V.29, the turn-off sequence consists of approximately 5 ms of remaining data and scrambled ones followed by a 20 ms period of no transmitted energy.

In V.21, the transmitter turns off within 7 ms after $\overline{\text{RTS}}$ goes false.

In Group 2, the transmitter turns off within 200 µs after $\overline{\text{RTS}}$ goes false.

When operating in parallel data mode, the turn-off sequence may be extended by 8 bit times.

When HDLC is selected, the turn-off sequence may be extended by more than 8 bit times.

Table 2. Turn-On Sequence Times

Configuration	$\overline{\text{RTS}}$ On to $\overline{\text{CTS}}$ On	
	Echo Protector Tone Disabled	Echo Protector Tone Enabled
V.29 (All Speeds)	253 ms	441 ms
V.27 ter 4800 bps Long Train	708 ms	915 m
V.27 ter 4800 bps Short Train	50 ms	257 ms
V.27 ter 2400 bps Long Train	943 ms	1150 ms
V.27 ter 2400 bps Short Train	67 ms	274 ms
V.21 channel 2 300 bps	≤14 ms	≤14 m
Group 2	≤400 µs	≤400 µs

Table 1. Configurations, Signaling Rates and Data Rates

Configuration	Modulation[1]	Carrier Frequency (Hz) ±0.01%	Data Rate (bps) ± 0.01%	Baud (Symbols/Sec.)	Bits per Symbol	Constellation Points
V.29 9600	QAM	1700	9600	2400	4	16
V.29 7200	QAM	1700	7200	2400	3	8
V.29 4800	QAM	1700	4800	2400	2	4
V.27 ter 4800	DPSK	1800	4800	1600	3	8
V.27 ter 2400	DPSK	1800	2400	1200	2	4
V.21 channel 2 300	FSK	1650,1850	300	300	1	–
T.3 (Group2)	VSAMPM	2100	–	–	–	–

Notes: 1.Modulation legend: QAM Quadrature Amplitude Modulation
DPSK Differential Phase Shift Keying
FSK Frequency Shift Keying
VSAMPM Vestigial Sideband Amplitude Modulation - Phase Modulation

Transmit Level

The transmitter output level is programmable in the DSP RAM from 0 dBm to –15.0 dBm and is accurate to ± 1.0 dBm. The modem adjusts the output level by digitally scaling the output to the transmitter's digital-to-analog converter.

Scrambler/Descrambler

The modem incorporates a self-synchronizing scrambler/descrambler in accordance with V.29 or V.27 ter recommendations, depending on the selected configuration.

Receive Dynamic Range

The receiver satisfies PSTN performance requirements for received line signal levels from 0 dBm to –43 dBm measured at the Receiver Analog Input (RXA) input. An external input buffer and filter must be supplied between RXA and RXIN.

The default values of the programmable Received Line Signal Detector (RLSD) turn-on and turn-off threshold levels are –43 dBm and –48 dBm, respectively. The RLSD threshold levels can be programmed over the following range:

Turn on: –10 dBm to –47 dBm
Turn off: –10 dBm to –52 dBm

Receiver Timing

The timing recovery circuit can track a ± 0.01% frequency error in the associated transmit timing source.

Carrier Recovery

The carrier recovery circuit can track a ± 7 Hz frequency offset in the received carrier.

Clamping

Received Data (RXD) is clamped to a constant mark whenever RLSD is off.

Tone Detectors

Tone detectors 1 and 2 operate in all non-high speed receive modes. Tone detector 3 operates in all receive modes. The tone detectors can also operate as one 12th order filter (see 12TH bit in Table 10).

The filter coefficients of each filter are host programmable in RAM. The output of the tone detector filter goes to an energy detector. (See *9600 bps MONOFAX Modem Designer's Guide*.)

Voice Mode

The voice mode enables the host to efficiently transmit and receive audio signals and messages. In this mode, the host can directly access modem analog-to-digital (A/D) and digital-to-analog (D/A) converters. Incoming analog voice signals can then be converted to digital format and digital signals can be converted to analog voice output.

General Specifications

The modem power and environmental requirements are shown in Tables 3 and 4, respectively.

Table 3. Power Requirements

Voltage	Current (Typ.) @ 25°C	Current (Max.) @ 0°C
+5 VDC ±5% – 5 VDC ±5%	60 mA 14 mA	64 mA 16 mA
Note: Input voltage ripple ≤ 0.1 volts peak-to-peak. The amplitude of any frequency between 20 kHz and 150 kHz must be less than 500 µV peak.		

Table 4. Environmental Requirements

Parameter	Specification
Temperature	
Operating	0°C to 70°C (32 °F to 158°F)
Storage	–55°C to 125°C (–67°F to 257°F)
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.

HARDWARE INTERFACE SIGNALS

The modem functional hardware interface signals are shown in Figure 3. In this diagram, any point that is active when exhibiting the relatively more negative voltage of a two-voltage system (e.g., 0 VDC for TTL or –12 VDC for EIA-232-D) is called active low and is represented by a small circle at the signal point. Active low signals are overscored (e.g., $\overline{POR}$).

Edge-triggered clocks are indicated by a small triangle (e.g., DCLK).

Open-collector (open-source or open-drain) outputs are denoted by small half circle (e.g., signal $\overline{IRQ}$).

A clock intended to activate logic on its rising edge (low-to-high transition) is called active low, while a clock intended to activate logic on its falling edge (high-to-low transition) is called active high. When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

The modem pin assignments are shown in Figure 4. The pin assignments are listed by pin number in Table 5.

The hardware interconnect signals shown in Figure 3 are listed by functional group in Table 6. The digital and analog signal interface characteristics are defined in Table 7 and Table 8, respectively. The hardware interface signals are defined in Table 9.

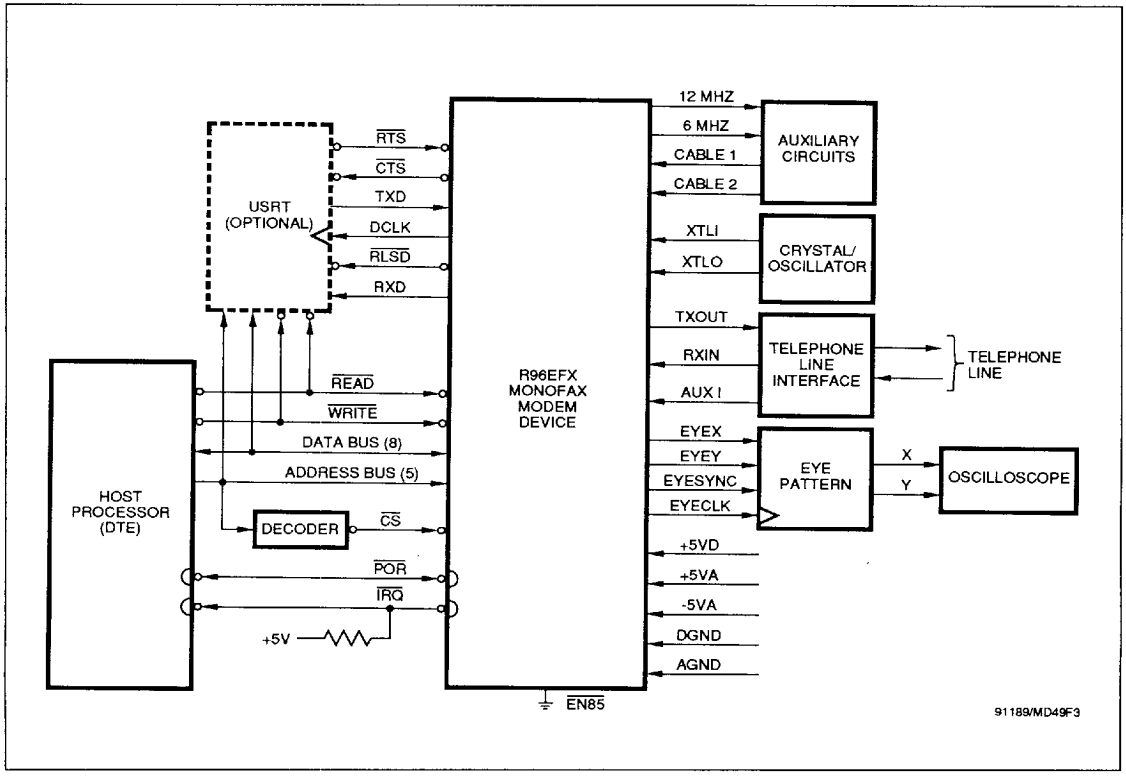
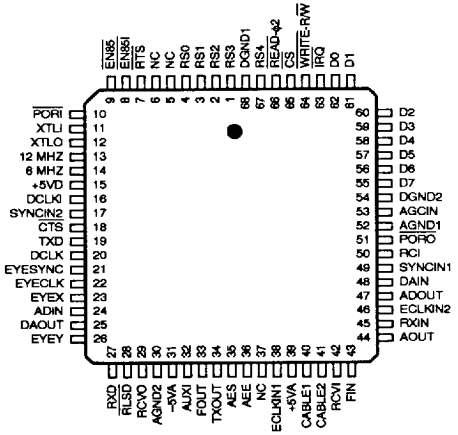
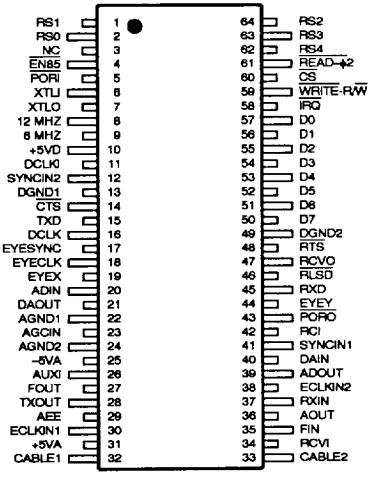


Figure 3. R96EFX Modem Functional Interconnect Signals



68-Pin PLCC



64-Pin QUIP

Figure 4. R96EFX Modem Pin Assignments

Table 5. R96EFX Modem Pin Assignments

68-Pin PLCC Pin Number	64-Pin QUIP Pin Number	Signal Name	I/O Type
3	1	RS1	IA
4	2	RS0	IA
5	–	NC	
6	3	NC	
8	–	EN85I	R
9	4	EN85	R
10	5	PORI	ID
11	6	XTLI	R
12	7	XTLO	R
13	8	12 MHZ	OD
14	9	6 MHZ	OD
15	10	+5VD	PWR
16	11	DCLKI	R
17	12	SYNCIN2	R
68	13	DGND1	GND
18	14	CTS	OA
19	15	TXD	IA
20	16	DCLK	OA
21	17	EYESYNC	OA
22	18	EYECLK	OA
23	19	EYEX	OA
24	20	ADIN	R
25	21	DAOUT	R
52	22	AGND1	GND
53	23	AGCIN	R
30	24	AGND2	GND
31	25	-5VA	PWR
32	26	AUXI	AC
33	27	FOUT	R
34	28	TXOUT	AA
35	-	AES	R
36	29	AEE	R
37	-	NC	
38	30	ECLKIN1	R
39	31	+5VA	PWR
40	32	CABLE1	IB
41	33	CABLE2	IB
42	34	RCVI	R
43	35	FIN	R
44	36	AOUT	R
45	37	RXIN	AB
46	38	ECLKIN2	R
47	39	ADOUT	R
48	40	DAIN	R
49	41	SYNCIN1	R
50	42	RCI	R
51	43	PORO	OE
26	44	EYEY	OA
27	45	RXD	OA
28	46	RLSD	OA
29	47	RCVO	R
7	48	RTS	IA
54	49	DGND2	GND
55	50	D7	IA/OB
56	51	D6	IA/OB
57	52	D5	IA/OB
58	53	D4	IA/OB
59	54	D3	IA/OB
60	55	D2	IA/OB
61	56	D1	IA/OB
62	57	D0	IA/OB
63	58	IRQ	OC
64	59	WRITE-R/W	IA
65	60	CS	IA
66	61	READ-φ2	IA
67	62	RS4	IA
1	63	RS3	IA
2	64	RS2	IA

Notes:
1. NC = No connection, leave pin disconnected (open).
2. I/O Type: Digital signals: see Table 7;
   Analog signals: see Table 8.
3. Required overhead connection; do not connect to host equipment.

Table 6. Modem Hardware Interface Signals

Name	Type[1]	Description
Overhead Signals		
XTLI	R	Connect to Crystal
XTLO	R	Connect to Crystal
PORO	OE	Power-On-Reset Output
PORI	ID	Power-On-Reset Input
+5VD	PWR	Connect to Digital +5V Power
+5VA	PWR	Connect to Analog +5V Power
–5VA	PWR	Connect to Analog –5V Power
DGND1	GND	Connect to Digital Ground
DGND2	GND	Connect to Digital Ground
AGND1	GND	Connect to Analog Ground
AGND2	GND	Connect to Analog Ground
Microprocessor Bus Interface		
D7	IA/OB	Data Bus Line 7
D6	IA/OB	Data Bus Line 6
D5	IA/OB	Data Bus Line 5
D4	IA/OB	Data Bus Line 4
D3	IA/OB	Data Bus Line 3
D2	IA/OB	Data Bus Line 2
D1	IA/OB	Data Bus Line 1
D0	IA/OB	Data Bus Line 0
RS4	IA	Register Select 4
RS3	IA	Register Select 3
RS2	IA	Register Select 2
RS1	IA	Register Select 1
RS0	IA	Register Select 0
$\overline{CS}$	IA	Chip Select
READ-φ2	IA	Read Enable (808X), φ2 Clock (65XX)
WRITE-R/$\overline{W}$	IA	Write Enable (808X), R/$\overline{W}$ (65XX)
$\overline{IRQ}$	OC	Interrupt Request
V.24 Serial Interface		
TXD	IA	Transmit Data
RXD	OA	Received Data
$\overline{RTS}$	IA	Request to Send
$\overline{CTS}$	OA	Clear to Send
$\overline{RLSD}$	OA	Received Line Signal Detected
DCLK	OA	Transmit and Receive Data Clock
Auxiliary Signals		
$\overline{EN85}$	R	Enable 85 Bus
CABLE1	IB	Cable Select 1
CABLE2	IB	Cable Select 2
12 MHZ	OD	12 MHz Output
6 MHZ	OD	6 MHz Output

Table 6. Modem Hardware Interface Signals (Cont'd)

Name	Type[1]	Description
Analog Signals		
TXOUT	AA	Connect to Smoothing Filter Input
RXIN	AB	Connect to Anti-aliasing Filter Output
AUXI	AC	Auxiliary Analog Input
Eye Diagnostic Interface		
EYEX	OA	Serial Eye Pattern X Output
EYEY	OA	Serial Eye Pattern Y Output
EYECLK	OA	Serial Eye Pattern Clock
EYESYNC	OA	Serial Eye Pattern Strobe
Modem Interconnect		
DCLKI	R	Connect to DCLK
ECLKIN1	R	Connect to EYECLK
ECLKIN2	R	Connect to EYECLK
SYNCIN1	R	Connect to EYESYNC
SYNCIN2	R	Connect to EYESYNC
RCVI	R	Connect to RCVO
RCVO	R	Mode Select Output
ADIN	R	Connect to ADOUT
ADOUT	R	ADC Output
DAIN	R	Connect to DAOUT
DAOUT	R	DAC/AGC Output
$\overline{EN85I}$	R	Connect to $\overline{EN85}$[4]
AEE	R	Connect to Analog Ground
AES	R	Connect to Analog Ground[4]
AGCIN	R	AGC Input
AOUT	R	Smoothing Filter Output
FIN	R	Connect to FOUT
FOUT	R	Smoothing Filter Output
RCI	R	RC Junction for POR Time Constant

Notes:

1. Digital signals are described in Table 7. Analog signals are described in Table 8.
2. R = Required overhead connection; no connection to host equipment.
3. Unused inputs tied to +5V or ground require individual 10K Ω series resistors.
4. PLCC only.

Table 7. Digital Interface Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input High Voltage	V_{IH}				Vdc	
Types IA and IB		2.0	–	V_{CC}		
Type ID		0.8(V_{CC})	–	V_{CC}		
Input High Current Type IB	I_{IH}	–	–	40	µA	V_{CC} = 5.25 V, V_{IN} = 5.25 V
Input Low Voltage	V_{IL}	–0.3	–	0.8	Vdc	
Input Low Current Type IB	I_{IL}	–	–	–400	µA	V_{CC} = 5.25 V
Input Leakage Current Types IA and ID	I_{IN}	–	–	±2.5	µA	V_{IN} = 0 to +5 V, V_{CC} = 5.25 V
Output High Voltage	V_{OH}				Vdc	
Types OA and OB		3.5	–	–		I_{LOAD} = – 100 µA
Type OE		2.4	–	–		I_{LOAD} = –40 µA
Output High Current Type OD	I_{OH}	–	–	–0.1	mA	
Output Low Voltage	V_{OL}				Vdc	
Types OA and OC		–	–	0.4		I_{LOAD} = 1.6 mA
Type OB		–	–	0.4		I_{LOAD} = 0.8 mA
Type OE		–		0.4		I_{LOAD} = 0.4 mA
Output Low Current Type OD	I_{OL}	–	–	100	µA	
Output Leakage Current Types OA and OB	I_{LO}	–	–	±10	µA	V_{IN} = 0.4 to V_{CC} –1
Capacitive Load	C_L				pF	
Types IA and ID		–	5	–		
Type IB		–	20	–		
Capacitive Drive	C_D				pF	
Types OA, OB, and OC		–	100	–		
Type OD		–	50	–		
Circuit Type						
Type IA						TTL
Type IB						TTL with pull-up
Type ID						POR
Types OA and OB						TTL with 3-state
Type OC and OE						Open drain
Type OD						Clock
Power Dissipation	P_D	–	370	420	mW	V_{CC} = 5.0 V @ 25°C for P_D typ. V_{CC} = 5.25 V @ 0°C for P_D max.

Note: Loads on 12 MHZ and 6 MHZ outputs must be balanced within 20%.

Table 8. Analog Interface Characteristics

Name	Type	Characteristic
TXOUT	AA	Maximum output: ±3.03 volts Minimum load: 10K Ω Smoothing filter transfer function: 28735.63/(s + 11547.34)
RXIN	AB	Input impedance: > 1M Ω Anti-aliasing filter transfer function: 21551.72/(s + 11547.34)
AUXI	AC	Maximum input frequency: 4800 Hz Input Impedance: > 1M Ω Gain to TXOUT: 0 dBm ±1 dB

Table 9. Hardware Interface Signal Definitions

Label	I/O Type	Signal/Definition
		OVERHEAD SIGNALS
XTLI XTLO	I O	**Crystal In and Crystal Out.** The DSP must be connected to an external crystal circuit consisting of a 24.00014 MHz crystal and two capacitors , or a square wave generator/sine wave oscillator (see Figures 6 and 7).
$\overline{\text{PORI}}$ PORO	ID OE	**Power-On-Reset Input.** **Power-On-Reset Output.** The $\overline{\text{PORI}}$ and $\overline{\text{PORO}}$ pins should be connected together to form a bidirectional $\overline{\text{POR}}$ signal. When power is applied to the modem, the modem pulses ($\overline{\text{POR}}$) within 350 ms. The modem is ready to use 15 ms after the low-to-high transition of $\overline{\text{POR}}$. The POR sequence is reinitiated any time the + 5V supply drops below + 3.5V for more than 15 ms, or an external device drives $\overline{\text{POR}}$ low for at least 3 µs. $\overline{\text{POR}}$ is not pulsed low by the modem when the POR sequence is initiated externally. The POR sequence initializes the modem interface memory (Table 10) to default values.
+5VD	PWR	**+ 5V Digital Supply.** +5VD must be connected to +5V ± 5%.
+5VA	PWR	**+ 5V Analog Supply.** +5VA must be connected to +5V ± 5%.
–5VA	PWR	**–5V Analog Supply.** –5VA must be connected to –5V ± 5%.
DGND1, DGND2	GND	**Digital Ground.** DGND1 and DGND2 must be connected to digital ground.
AGND1, AGND2	GND	**Analog Ground.** AGND1 and AGND2 must be connected to analog ground.
		MICROPROCESSOR BUS INTERFACE Address, data, control, and interrupt hardware interface signals allow modem connection to an 8085 or 6500 bus compatible microprocessor. With the addition of external logic, the interface can be made compatible with a wide variety of other microprocessors, such as the 8080 or 68000. The microprocessor interface allows a microprocessor to change modem configuration, read or write channel and diagnostic data, and supervise modem operation by writing control bits and reading status bits. Note that the modem should not be continuously selected for read operation. Also, read or write operations should be delayed by at least 334 ns from a preceding write cycle.
D0–D7	IA/OB	**Data Lines.** Eight bidirectional data lines (D0–D7) provide parallel transfer of data between the host and the modem. The most significant bit is D7. Data direction is controlled by the Read Enable ($\overline{\text{READ}}$-φ2) and Write Enable (WRITE-$\overline{\text{R/W}}$) signals. During a read cycle, data from the DSP interface memory register is gated onto the data bus by means of three-state drivers in the DSP. These drivers force the data lines high for a one bit, or low for a zero bit. When not being read, the three-state drivers assume their high-impedance (off) state. During a write cycle, data from the data bus is copied into the selected DSP interface memory register, with high and low bus levels representing one and zero bit states, respectively.
RS0–RS4	IA	**Register Select Lines.** The five active high Register Select inputs (RS0–RS4) address interface memory registers within the DSP when $\overline{\text{CS}}$ is low. These lines are typically connected to address lines A0-A4. When selected by $\overline{\text{CS}}$ low, the DSP decodes RS0 through RS4 to address one of 32 8-bit internal interface memory registers (00-1F). The most significant address bit is RS4 while the least significant address bit is RS0. The selected register can be read from, or written into, via the 8-bit parallel data bus (D0–D7).

Table 9. Hardware Interface Signal Definitions (Cont'd)

Label	I/O Type	Signal/Definition
$\overline{CS}$	IA	**Chip Select.** The active low $\overline{CS}$ input selects and enables the modem DSP for parallel data transfer between the DSP and the host over the microprocessor bus. The $\overline{CS}$ input line is typically connected to address line A5 through a decoder.
$\overline{READ}$–$\phi 2$ $\overline{WRITE}$–R/$\overline{W}$	IA IA	**Read Enable–$\phi 2$.** **Write Enable–R/$\overline{W}$.** When $\overline{EN85}$ is low (8085 bus selected), reading or writing is controlled by the host pulsing either $\overline{READ}$ or $\overline{WRITE}$ input low, respectively, during the microprocessor bus access cycle.
$\overline{IRQ}$	OC	**Interrupt Request.** $\overline{IRQ}$ interrupt request output may be connected to the host processor interrupt request input in order to interrupt host program execution for immediate modem service. The $\overline{IRQ}$ output can be enabled in DSP interface memory to indicate immediate change of conditions in the modem. The use of $\overline{IRQ}$ is optional depending upon modem application. The $\overline{IRQ}$ output structure is an open-drain field-effect-transistor (FET). The $\overline{IRQ}$ output can be wire-ORed with other $\overline{IRQ}$ lines in the application system. Any of these sources can drive the host interrupt input low, and the host interrupt servicing process normally continues until all interrupt requests have been serviced (i.e., all $\overline{IRQ}$ lines have returned high). Because of the open-drain structure of $\overline{IRQ}$, an external pull-up resistor to +5V is required at some point on the $\overline{IRQ}$ line. The resistor value should be small enough to pull the $\overline{IRQ}$ line high when all $\overline{IRQ}$ drivers are off (i.e., it must overcome the leakage currents). The resistor value should be large enough to limit the driver sink current to a level acceptable to each driver. If only the modem $\overline{IRQ}$ output is used, a resistor value of 5.6K ohms ±20%, 0.25 W, is sufficient.
		V.24 SERIAL INTERFACE Seven pins provide timing, data, and control signals for implementing a CCITT Recommendation V.24 compatible serial interface. These signals are TTL compatible in order to drive the short wire lengths and circuits normally found within stand-alone modem enclosures or equipment cabinets. For driving longer cables, these signals can be easily converted to EIA-232-D voltage levels.
TXD	IA	**Transmit Data.** The modem obtains serial data to be transmitted from the local DTE on the Transmit Data (TXD) input in serial data mode (selected by PDM bit in interface memory), or from the interface memory Transmit Data Register (DBUFF) in parallel data mode (selected by PDM bit).
RXD	OA	**Received Data.** The modem presents received serial data to the local DTE on the Received Data (RXD) output and to the interface memory Receive Data Register (DBUFF) in both serial and parallel data modes.
$\overline{RTS}$	IA	**Request to Send.** The active low $\overline{RTS}$ input allows the modem to transmit data present at TXD in the serial data mode or in DBUFF in the parallel data mode when $\overline{CTS}$ becomes active. The $\overline{RTS}$ hardware control input is logically ORed with the RTSP bit (Table 10) by the modem to form the resultant control signal.

Table 9. Hardware Interface Signal Definitions (Cont'd)

Label	I/O Type	Signal/Definition
$\overline{CTS}$	OA	**Clear To Send.** $\overline{CTS}$ active indicates to the local DTE that the training sequence has been completed and any data present at the TXD input in the serial data mode or in DBUFF in the parallel data mode will be transmitted. $\overline{CTS}$ response times from $\overline{RTS}$ are shown in Table 2. The $\overline{CTS}$ hardware status output parallels the operation of the CTSP bit (Table 10).
$\overline{RLSD}$	OA	**Received Line Signal Detector.** For V.29 and V.27 ter; $\overline{RLSD}$ goes active at the end of the training sequence. If energy is above the turn-on threshold and training is not detected, the $\overline{RLSD}$ off-to-on response time is 804 baud times. The $\overline{RLSD}$ on-to-off time is 35±5ms for V.29 or 11.6 ± 5 ms for V.27 ter. The $\overline{RLSD}$ on-to-off time ensures that all valid data bits have appeared on RXD. The $\overline{RLSD}$ programmable threshold levels default to –43 dBm for off-to-on and to –48 dBm for on-to-off. A minimum hysteresis of 2 dBm exists between the actual off-to-on and on-to-off transition levels. The threshold level and hysteresis are measured with an unmodulated 2100 Hz tone applied to the Receiver Analog (RXA) input. Note that performance may be degraded when the received signal level is less than –43 dBm.
DCLK	OA	**Data Clock.** The modem outputs a single mode-dependent synchronous data clock (DCLK) for USRT timing. The DCLK frequency is 9600, 7200, 4800, 2400, or 300 Hz (± 0.01%) with a duty cycle of 50 ± 1% except in Group 2. In Group 2, the DCLK frequency is 10368 Hz (± 5 ppm) when using a precision oscillator (see Figures 6 and 7). Transmit Data (TXD) must be stable during the one microsecond period immediately preceding the rising edge of DCLK and following the rising edge of DCLK.
		AUXILIARY SIGNALS
$\overline{EN85}$	I	**Enable 85 Bus.** The $\overline{EN85}$ input selects the modem microprocessor bus compatibility. When $\overline{EN85}$ is low, the modem can interface directly to an 8085 compatible microprocessor bus using $\overline{READ}$ and $\overline{WRITE}$. When $\overline{EN85}$ is high, the modem can interface directly to a 6500 compatible microprocessor bus using $\phi 2$ and R/$\overline{W}$. In the 6500 configuration, the $\overline{READ}$ input becomes $\phi 2$ and the $\overline{WRITE}$ input becomes R/$\overline{W}$. This selection is performed only during initialization, i.e., when power is turned on or when $\overline{POR}$ is activated.
CABLE1, CABLE2	IB IB	**Cable Equalizer Select 1.** **Cable Equalizer Select 2.** The CABLE1 and CABLE2 inputs select equalization for the following cable lengths: **CABLE2 / CABLE1 / Cable Length / Gain (dB) * at 700 Hz / 1500 Hz / 2000 Hz / 3000 Hz** Low / Low / 0.0 km / 0.00 / 0.00 / 0.00 / 0.00 Low / High / 1.8 km / –0.99 / –0.20 / +0.15 / +1.43 High / Low / 3.6 km / –2.39 / –0.65 / +0.87 / +3.06 High / High / 7.2 km / –3.93 / –1.22 / +1.90 / +4.58 * Relative to 1700 Hz for length of 0.4 mm diameter cable. Modems may be connected by direct wiring, such as leased telephone cable or through the PSTN, by means of a data access arrangement. In either case, the modem analog signal is carried by copper wire cabling for at least some of its route. To minimize the impact of this copper wire passband shaping, a compromise equalizer with more attenuation at the lower frequencies than at the higher frequencies can be placed in series with the analog signal. The modem includes three such equalizers designed to compensate for cable distortion. When selected, the equalizers are inserted in the transmit path when transmitting, and in the receive path when receiving.
12 MHZ	OD	**12 MHz Output.** A 12 MHz square wave output derived from XTLI (XTLI divided by 2).
6 MHZ	OD	**6 MHz Output.** A 6 MHz square wave output derived from XTLI (XTLI divided by 4).

Table 9. Hardware Interface Signal Definitions (Cont'd)

Label	I/O Type	Signal/Definition
		ANALOG SIGNALS The Transmitter Analog Output (TXOUT) and Receiver Analog Input (RXIN) allow modem connection to either a leased line or the PSTN through the appropriate buffering and an audio transformer or a data access arrangement. The Auxiliary Input (AUXI) provides access to the transmitter for summing audio signals with the modem's transmitter output. The analog signal characteristics are described in Table 8.
TXOUT	AA	**Transmitter Analog Output.** TXOUT can supply a maximum of ± 3.03 volts into a load resistance of 10K ohms minimum. A 600 ohm line impedance can be matched using an external smoothing filter with a 604 ohm series resistor in its output. The smoothing filter should have a transfer function of 28735.63/(s + 11547.34).
RXIN	AB	**Receiver Analog Input.** The RXIN input impedance is >1M ohms. RXIN requires an external anti-aliasing filter between the modem and the line interface, with a transfer function of 21551.72/(s + 11547.34). The maximum input level into the anti-aliasing filter should not be greater than 0 dBm. The filters required for anti-aliasing on the receiver input and the smoothing filter on the transmitter output have a single pole within the modem's passband. Internal filters compensate for its presence, therefore, the pole location must not be changed. Some variation from the recommended resistor and capacitor values is permitted as long as the pole is not moved, overall gain is preserved, and the device is not required to drive a load of less than 10K ohms.
AUXI	AC	**Auxiliary Analog Input.** AUXI allows access to the transmitter for the purpose of interfacing with user-provided equipment. Because this is a sampled input, any signal above 4800 Hz will cause aliasing errors. The input impedance is > 1M ohm, and the gain to TXOUT is 0 dBm ± 1 dB.
		EYE DIAGNOSTIC INTERFACE Four signals provide the timing necessary to create an oscilloscope quadrature eye pattern. The eye pattern is simply a display of the received baseband constellation. By observing this constellation, common line disturbances can usually be identified.
EYEX, EYEY	OA OA	**Serial Eye Pattern X Output.** **Serial Eye Pattern Y Output.** The EYEX and EYEY outputs provide two serial bit streams containing data for display on the oscilloscope X axis and Y axis, respectively. This serial digital data must first be converted to parallel digital form by two serial-to-parallel converters and then to analog form by two digital-to-analog (D/A) converters. EYEX and EYEY outputs are 9-bit words with their sign bits repeated. The 9-bit data words are shifted out sign bit first. EYEX and EYEY are clocked by the rising edge of EYECLK.
EYECLK	OA	**Serial Eye Pattern Clock.** EYECLK is a 230.4 kHz clock. EYECLK* is a clock derived from EYECLK and EYESYNC for shifting EYEX and EYEY data into the serial-to-parallel converters.
EYESYNC	OA	**Serial Eye Pattern Strobe.** EYESYNC is a 9600 Hz strobe used for loading the eye pattern D/A converters.

SOFTWARE INTERFACE

INTERFACE MEMORY

The DSP communicates with the host processor by means of a dual-port, interface memory. The interface memory in the DSP contains thirty-two 8-bit registers, labeled register 00 through 1F (Figure 5). Each register can be read from, or written into, by both the host and the DSP.

The host can control modem operation by writing control bits to DSP interface memory and writing parameter values to DSP RAM through interface memory. The host can monitor modem operation by reading status bits from DSP interface memory and reading parameter values from DSP RAM through interface memory.

Table 10 defines the interface memory bits. In Table 10, interface memory bits are referred to using the format Z:Q. The register number is designated by Z (00 through 1F), and the bit number by Q (0 through 7, 0 = LSB).

DSP RAM ACCESS

The DSP consists of 16-bit words organized into real (X RAM) and imaginary (Y RAM) parts. The host processor can read or write both the X RAM and the Y RAM.

DSP interface memory is an intermediary during data exchanges between the host and DSP RAM. The address stored in interface memory RAM address registers by the host determines the DSP RAM address for data access.

The 16-bit words are transferred between DSP RAM and DSP interface memory once each baud, or sample time, as selected by the BR1 and BR2 bits. The baud rate is determined by the selected configuration, but the sample rate is fixed at 9600 Hz (except for voice mode and Group 2 configurations).

The DSP RAM access functions, codes, and registers are identified in Table 11.

Register Function	Register Address (Hex)	Bit 7	6	5	4	3	2	1	0	Default Value (Bin)
Interrupt Handling	1F	PIA	—	—	PIE	PIREQ	—	—	SETUP	-XX0-XX0
	1E	IA2	IA1	IE2	—	BA2	IE1	—	BA1	--0X-0X-
Not Available	1D	—	—	—	—	—	—	—	—	XXXXXXXX
	1C	—	—	—	—	—	—	—	—	XXXXXXXX
	1B	—	—	—	—	—	—	—	—	XXXXXXXX
	1A	—	—	—	—	—	—	—	—	XXXXXXXX
	19	—	—	—	—	—	—	—	—	XXXXXXXX
	18	—	—	—	—	—	—	—	—	XXXXXXXX
	17	—	—	—	—	—	—	—	—	XXXXXXXX
	16	—	—	—	—	—	—	—	—	XXXXXXXX
RAM Access 2 Control & Status, HDLC Control, and Data Buffers	15	ACC2	0	0	0	IO2	BR2	WRT2	CR2	00000000
	14	RAM ADDRESS 2 (ADD2)								00000000
	13	X RAM DATA 2 MSB (XDAM2)								--------
	12	X RAM DATA 2 LSB (XDAL2)								--------
	11	Y RAM DATA 2 MSB (YDAM2)								--------
	10	Y RAM DATA 2 LSB (YDAL2)/DATA BUFFER (DBUFF)								--------
High Speed Status and Group 2 Control	0F	FED		—	—	—	—	CTSP	CDET	--XXXX--
	0E	—	—	—	—	—	—	—	—	XXXXXXXX
	0D	RX	PNDET	—	—	G2FGC	—	—	—	--XX0XXX
	0C	—	—	DATA	SCR1	PN	P2	P1	SIDLE	XX------
Programmable Interrupt Control	0B	ITBMSK								00000000
	0A	TRIG		ANDOR	ITADRS					00000000
High Speed Control and HDLC Control & Status	09	OVRUN	EQSV	EQFZ	ZEROC	ABIDL	EOF	CRC	FLAG	-000----
Tone Detect and High Speed Control & Status	08	FR3	FR2	FR1	12TH	PNSUC*	—	—	—	---0-XXX
Mode Control#	07	RTSP	TDIS	PDM	SHTR	EPT	SQEXT	T2	HDLC	00001000
	06	CONF								00010100
RAM Access 1 Control & Status and Data Buffers	05	ACC1	0	0	0	IO1	BR1	WRT1	CR1	10000101
	04	RAM ADDRESS 1 (ADD1)								00010111
	03	X RAM DATA 1 MSB (XDAM1)								--------
	02	X RAM DATA 1 LSB (XDAL1)								--------
	01	Y RAM DATA 1 MSB (YDAM1)								--------
	00	Y RAM DATA 1 LSB (YDAL1)								--------

NOTES: * Not available in R6631-12.
These bits [except RTSP(all) and TDIS (R6631-13 and above)] require the setting of SETUP to become active.
— Indicates reserved for modem use only.

Figure 5. R96EFX DSP Interface Memory Map

Table 10. Modem Interface Memory Bit Definitions

Mnemonic	Memory Location	Default Value	Name/Description
12TH	08:4	0	**Select 12th Order.** When control bit 12TH is set, the tone detectors operate as one 12th order filter (uses FR3). When 12TH is reset, the tone detectors operate as three parallel independent 4th order filters (FR1, FR2, FR3). 12TH is valid in in FSK, Group 2, voice, or tone mode (i.e., CONF = 20, 40, 82, or 80, respectively) with $\overline{RTS}$ off and RTSP reset.
ABIDL	09:3	–	**Abort/Idle.** When the modem is configured as a transmitter and control/status bit ABIDL is set, the modem will finish sending the current DBUFF byte. The modem will then send continuous ones if ZEROC is reset, or continuous zeros if ZEROC is set. When ABIDL is reset, the modem will not send continuous ones or zeros. If ABIDL is reset one DCLK cycle after being set, the modem will transmit eight continuous ones if ZEROC is reset, or eight continuous zeros if ZEROC is set. ABIDL is also set by the modem when the underrun condition occurs (bit OVRUN is set) and the modem will send at least eight continuous ones (if ZEROC is reset) or eight continuous zeros (if ZEROC is set). To stop continuous one or zero transmission, ABIDL must be reset by the host. (HDLC only.) When the modem is configured as a receiver and status bit ABIDL is set, the modem has received a minimum of seven consecutive ones. To recognize further occurrences of this abort condition, ABIDL must be reset by the host. (HDLC only.)
ACC1	05:7	1	**RAM Access 1.** When control bit ACC1 is set, the modem accesses the RAM associated with the address in ADD1 and the CR1 bit. WRT1 determines if a read or write is performed.
ACC2	15:7	0	**RAM Access 2.** When control bit ACC2 is set, the modem accesses the RAM associated with the address in ADD2 and the CR2 bit (provided parallel data mode and HDLC are not selected). WRT2 determines if a read or write is performed.
ADD1	04:0-7	17	**RAM Address 1.** ADD1 contains the RAM address used to access the modem's X and Y Data RAM (CR1 = 0) or X and Y Coefficient RAM (CR1 = 1) via the X RAM Data 1 LSB and MSB words (2:0-7 and 3:0-7, respectively) and the Y RAM Data 1 LSB and MSB words (0:0-7 and 1:0-7, respectively).
ADD2	14:0-7	00	**RAM Address 2.** ADD2 contains the RAM address used to access the modem's X and Y Data RAM (CR2 = 0) or X and Y Coefficient RAM (CR2 = 1) via the X RAM Data 2 LSB and MSB words (12:0-7 and 13:0-7, respectively) and the Y RAM Data 2 LSB and MSB words (10:0-7 and 11:0-7, respectively).
ANDOR	0A:5	–	**AND/OR Bit Mask Function.** When control bit ANDOR is set and the programmable interrupt is enabled, the modem will assert $\overline{IRQ}$ if all the bits in the register specified by ITADRS and masked by ITBMSK are ones. When ANDOR is reset and the programmable interrupt is enabled, the modem will assert $\overline{IRQ}$ if any one of the bits in the register specified by ITADRS and masked by ITBMSK is a one.
BA1	1E:0	–	**Buffer Available 1.** When set, status bit BA1 signifies that the modem has either written diagnostic data to, or read diagnostic data from, the Y RAM DATA 1 LSB (YDAL1) (register 00:0-7). If the modem is in Voice Transmitter mode, the modem sets $\overline{BA1}$ when the contents of register 00:0-7 have been transmitted. Setting BA1 can also cause $\overline{IRQ}$ to be asserted. The host writing to or reading from register 00 resets the BA1 and IA1 bits. (See IE1 and IA1.)
BA2	1E:3	–	**Buffer Available 2.** If the modem is in the parallel data mode or HDLC is selected, the modem sets status bit BA2 when it has read the transmit byte from DBUFF (register 10:0-7) when transmitting (buffer becomes empty), or it has written the received byte to DBUFF (register 10:0-7) when receiving (buffer becomes full). If the modem is not in parallel data mode and HDLC is not selected, the modem sets BA2 when it has either written diagnostic data to, or read diagnostic data from, the Y RAM DATA 2 LSB (YDAL2) (register 10:0-7). Setting BA2 can also cause $\overline{IRQ}$ to be asserted. The host writing to or reading from register 10 resets the BA2 and IA2 bits. (See IE2 and IA2.)

Table 10. Modem Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
BR1	05:2	1	**Baud Rate 1.** When control bit BR1 is set, RAM access for ADD1 occurs at the baud rate; when BR1 is reset, RAM access occurs at the sample rate. This bit must be reset in FSK, Group 2, voice, or tone mode (i.e., CONF = 20, 40, 82, or 80, respectively).
BR2	15:2	0	**Baud Rate 2.** When control bit BR2 is set, RAM access for ADD2 occurs at the baud rate; when BR2 is reset, RAM access occurs at the sample rate. This bit must be reset in FSK, Group 2, voice, or tone mode (i.e., CONF = 20, 40, 82, or 80, respectively).
CDET	0F:0	–	**Carrier Detected.** When status bit CDET is set, the receiver has finished receiving the training sequence, or has turned on due to detecting energy above threshold, and is receiving data. When CDET is reset, the receiver is in the idle state or in the process of training.
CONF	06:0-7	14	**Configuration.** The CONF control bits select the modem configuration as follows: **CONF (Hex) — Configuration** 14 — V.29 9600 bps 12 — V.29 7200 bps 11 — V.29 4800 bps 0A — V.27 ter 4800 bps 09 — V.27 ter 2400 bps 20 — Transmit: V.21 Channel 2 300 bps (FSK); Receive: V.21 Channel 2 300 bps (FSK) and Tone Detector 40 — Transmit: Group 2; Receive: Group 2 and Tone Detector 80 — Transmit: Dual Tone; Receive: Tone Detector 82 — Transmit: 76.8K bps Voice mode (default sample rate = 9600 Hz); Receive: 76.8K bps Voice mode and Tone Detector **Definitions:** 1. **V.29.** When a V.29 configuration is selected, the modem operates as specified in CCITT Recommendation V.29 with concurrent receive single tone detection (FR3). 2. **V.27 ter.** When a V.27 ter configuration is selected, the modem operates as specified in CCITT Recommendation V.27 ter with concurrent receive single tone detection (FR3). 3. **V.21 Channel 2.** When a V.21 Channel 2 configuration is selected, the modem operates as specified in CCITT Recommendation V.21 channel 2. 4. **Group 2.** When the Group 2 configuration is selected, the modem operates as specified in CCITT Recommendation T.3. 5. **Dual Tone.** When the Dual Tone Transmit configuration is selected, the modem transmits single or dual frequency tones in response to $\overline{RTS}$ or RTSP. Tone frequencies and amplitudes are programmable in the DSP RAM. 6. **Tone Detector.** When a Tone Detector configuration is selected and 12TH is set, the three 4th order tone detect filters are combined into a single 12th order tone detect filter (FR3). If 12TH is reset, the three tone detect filters are placed in parallel and are independent (FR1, FR2, and FR3). All tone detect filters are programmable. 7. **Voice Mode.** When the Voice mode configuration is selected, the A/D or the D/A converter is available for voice reception or transmission.
CR1	05:0	1	**Coefficient RAM 1 Select.** When control bit CR1 is set, ADD1 addresses Coefficient RAM. When CR1 is reset, ADD1 addresses Data RAM. This bit must be set according to the desired RAM address (Table 11).
CR2	15:0	0	**Coefficient RAM 2 Select.** When control bit CR2 is set, ADD2 addresses Coefficient RAM. When CR2 is reset, ADD2 addresses Data RAM. This bit must be set according to the desired RAM address (Table 11).

Table 10. Modem Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
CRC	09:1	–	**Cyclic Redundancy Check error.** When status bit CRC is set and status bit EOF is set, the received frame is in error. When CRC is reset and EOF is set, the received frame is correct. CRC only changes immediately before EOF is set. (HDLC only.)
CTSP	0F:1	–	**Clear To Send Parallel.** When set, status bit CTSP indicates to the DTE that the training sequence has been completed and any data present at TXD (PDM = 0) or DBUFF (PDM = 1) will be transmitted. CTSP parallels the operation of the CTS pin.
DATA	0C:5	–	**Data Mode.** When status bit DATA = 1, the high speed transmitter/receiver is in the data mode.
DBUFF	10:0-7	–	**Data Buffer.** In the parallel data mode, the host obtains received data from the modem by reading a data byte from DBUFF; the host sends data to the modem to be transmitted by writing a data byte to DBUFF. The data is received and transmitted bit 0 first.
EOF	09:2	–	**End Of Frame.** When the modem is configured as a transmitter, the EOF bit is a control bit. To convey to the modem that it is time to send the 16-bit FCS and ending flag of a HDLC frame, the host must set the EOF bit after the modem has taken the last byte of data (resides in DBUFF) of the frame (BA2 sets again). EOF will then be reset by the modem after it has recognized the setting of EOF by the host. When the modem is configured as a receiver and status bit EOF is set, the modem has received a frame ending flag and bit CRC is updated. EOF must be reset by the host before receiving the ending flag of a following frame. (HDLC only.)
EPT	07:3	1	**Echo Protector Tone Enable.** When control bit EPT is set, an unmodulated carrier is transmitted for 187.5 ms followed by 20 ms of no transmitted energy prior to the transmission of the training sequence. When EPT is reset, neither the echo protector tone nor the 20 ms of no energy are transmitted prior to the transmission of the training sequence except in V.29 which transmits 20 ms of silence at the beginning of training.
EQFZ	09:5	0	**Equalizer Freeze.** When control bit EQFZ is set, updating of the receiver's adaptive equalizer taps is inhibited.
EQSV	09:6	0	**Equalizer Save.** When control bit EQSV is set, the adaptive equalizer taps are not zeroed when reconfiguring the modem or when entering the training state. Adaptive equalizer taps are also not updated during training. This bit is used in conjunction with the SHTR and EQFZ bits and must be followed by the setting of the SETUP bit.
FED	0F:7,6	–	**Fast Energy Detector.** Status bits FED indicates the level of the received signal according to the following codes. FED — Energy Level 0 — No energy 1 — Invalid 2 — Above Turn-off Threshold 3 — Above Turn-on Threshold
FLAG	09:0	0	**FLAG Mode.** When the modem is configured as a transmitter and status bit FLAG is set, the modem is transmitting a flag sequence. When the modem is configured as a receiver and status bit FLAG is set, the modem has received a flag sequence. (HDLC only.)
FR1	08:5	–	**Frequency No. 1.** Status bit FR1 is set by the modem when energy is being detected above tone detector 1's turn-on threshold (default detection range = 2100 Hz ± 25 Hz). FR1 is operable in FSK, Group 2, voice, or tone mode (i.e., CONF = 20, 40, 82, or 80, respectively) with RTS off and RTSP reset.

Table 10. Modem Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
FR2	08:6	–	**Frequency No. 2.** Status bit FR2 is set by the modem when energy is being detected above tone detector 2's turn-on threshold (default detection range = 1100 Hz ± 30 Hz). FR2 is operable in FSK, Group 2, voice, or tone mode (i.e., CONF = 20, 40, 82, or 80, respectively) with $\overline{RTS}$ off and RTSP reset.
FR3	08:7	–	**Frequency No. 3.** Status bit FR3 is set by the modem when energy is being detected above tone detector 3's turn-on threshold (default detection range = 462 Hz ±14 Hz). FR3 is operable in all receive modes with $\overline{RTS}$ off and RTSP reset.
G2FGC	0D:3	0	**Group 2 Fast Gain Control.** When control bit G2FGC is set, a fast AGC rate (8.6 times standard) is selected (Group 2).
HDLC	07:0	0	**HDLC.** When control bit HDLC is set, the modem performs HDLC framing. To become active, the host must set HDLC and PDM followed by the setting of SETUP. When control bit HDLC is reset, the modem does not perform HDLC framing provided SETUP was set following the resetting of HDLC.
IA1	1E:6	–	**Interrupt Active 1.** When Interrupt Enable 1 is enabled (IE1 is set) and BA1 is set by the modem, the modem asserts $\overline{IRQ}$ and sets status bit IA1 to indicate that BA1 being set caused the interrupt. The host writing to or reading from register 00 resets IA1. (See IE1 and BA1.)
IA2	1E:7	–	**Interrupt Active 2.** When Interrupt Enable 2 is enabled (IE2 is set) and BA2 is set by the modem, the modem asserts $\overline{IRQ}$ and sets status bit IA2 to indicate that BA2 being set caused the interrupt. The host writing to or reading from register 10 resets IA2. (See IE2 and BA2.)
IE1	1E:2	0	**Interrupt Enable 1.** When control bit IE1 is set (interrupt enabled), the modem will assert $\overline{IRQ}$ and set IA1 when BA1 is set. When IE1 is reset (interrupt disabled), BA1 has no effect on $\overline{IRQ}$ and IA1. (See BA1 and IA1.)
IE2	1E:5	0	**Interrupt Enable 2.** When control bit IE2 is set (interrupt enabled), the modem will assert $\overline{IRQ}$ and set IA2 when BA2 is set. When IE2 is reset (interrupt disabled), BA2 has no effect on $\overline{IRQ}$ and IA2. (See BA2 and IA2.)
IO1	05:3	0	**Input/Output RAM 1 Select.** When control bit IO1 is set, ADD1 addresses IO RAM. When IO1 is reset, ADD1 addresses either coefficient or data RAM depending on the state of the CR1 bit. This bit must be set according to the desired RAM address. (See Table 11.)
IO2	15:3	0	**Input/Output RAM 2 Select.** When control bit IO2 is set, ADD2 addresses IO RAM. When IO2 is reset, ADD2 addresses either coefficient or data RAM depending on the state of the CR2 bit. This bit must be set according to the desired RAM address. (See Table 11.)
ITADRS	0A:0-4	–	**Interrupt Address.** These 5 bits specify the register upon which the programmable interrupt and ITBMSK will take affect. The address of the byte on which the modem asserts $\overline{IRQ}$ on a bit or bits in that byte is specified below:

Host Register (Hex)	ITADRS (Hex)	Host Register (Hex)	ITADRS (Hex)
00	00	10	08
01	10	11	18
02	01	12	09
03	11	13	19
04	02	14	0A
05	12	15	1A
06	03	16	0B
07	13	17	1B
08	04	18	0C
09	14	19	1C
0A	05	1A	0D
0B	15	1B	1D
0C	06	1C	0E
0D	16	1D	1E
0E	07	1E	0F
0F	17	1F	1F

Table 10. Modem Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
ITBMSK	0B:0-7	–	**Interrupt Bit Mask.** This byte performs a bit mask on the register specified in ITADRS for the programmable interrupt processing. A one in any position in ITBMSK will cause the modem to assert IRQ on the corresponding bit or bits in the register specified by ITADRS according to the ANDOR bit and the TRIG bits if PIE is set by the host and PIREQ is reset by the host.
OVRUN	09:7	–	**Overrun/Underrun.** When the modem is configured as a transmitter, and status bit OVRUN is set, a transmit underrun condition has occurred. If the host does not load in a new byte of data in DBUFF within eight bit times of loading the previous byte into DBUFF, OVRUN and ABIDL will set. The modem will then automatically send eight continuous ones. The transmission of these ones will continue until the host resets ABIDL. The modem will then finish sending the current group of eight ones and will either start sending another frame (if BA2 is reset) or will transmit continuous flags. The modem will reset OVRUN every time it sets BA2. (HDLC only.) When the modem is configured as a receiver and status bit OVRUN is set, an overrun condition has occurred. To detect the next overrun condition, the host must reset this bit. (HDLC only.)
P1	0C:1	–	**P1 Sequence.** When the modem is configured as a high speed transmitter, status bit P1 = 1 indicates the P1 sequence is being sent. When P1 = 0, the P1 sequence is not being transmitted. When the modem is configured as a receiver, the P1 bit has no meaning.
P2	0C:2	–	**P2 Sequence.** When the modem is configured as a high speed transmitter, status bit P2 = 1 indicates the P2 sequence is being sent. When P2 = 0, the P2 sequence is not being transmitted. When the modem is configured as a high speed receiver, status bit P2 = 1 indicates the search for the P2 to PN transition is occurring. When P2 = 0, the P2 to PN transition search is not occurring.
PDM	07:5	0	**Parallel Data Mode.** When control bit PDM is set and the modem is a transmitter, it accepts data for transmission from DBUFF (10:0-7) rather than the TXD input. When PDM is set and the modem is a receiver, the modem provides the received data to the host using DBUFF (10:0-7).
PIA	1F:7	–	**Programmable Interrupt Active.** When control bit PIE is enabled (PIE is set) and the interrupt condition is true as specified by ITBMSK, ITADRS, TRIG, and ANDOR, the modem asserts IRQ if PIREQ has been previously reset by the host (usually after servicing the previous interrupt). Status bit PIA is set by the modem when the above occurs. PIA is reset when the host resets PIREQ.
PIE	1F:4	0	**Programmable Interrupt Enable.** When control bit PIE is enabled (PIE is set) and the interrupt condition is true as specified by ITBMSK, ITADRS, TRIG, and ANDOR, the modem asserts IRQ if PIREQ has been previously reset by the host (usually after servicing the previous interrupt). Status bit PIA is set by the modem when the above occurs. When PIE is reset (interrupt disabled), ITBMSK, ITADRS, TRIG, ANDOR, and PIREQ have no effect on IRQ and PIA.
PIREQ	1F:3	–	**Programmable Interrupt Request.** When control bit PIE is enabled (PIE is set) and the interrupt condition is true as specified by ITBMSK, ITADRS, TRIG, and ANDOR, the modem asserts IRQ if control bit PIREQ has been previously reset by the host. PIREQ is set by the modem when the programmable interrupt condition is true. The host must reset PIREQ after servicing the interrupt since the modem does not reset PIREQ. If PIREQ is not reset when the interrupt condition occurs again, the modem will not assert IRQ.

Table 10. Modem Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
PN	0C:3	–	**PN Sequence.** When the modem is configured as a high speed transmitter, status bit PN = 1 signals that the PN sequence is being sent. When PN = 0, the PN sequence is not being transmitted. When the modem is configured as a high speed receiver, status bit PN = 1 indicates the PN portion of the training sequence is being received. When PN = 0, the PN portion of training is not being received.
PNDET	0D:6	–	**PN Detected.** When status bit PNDET is set, the receiver has detected the PN portion of the training sequence. When PNDET is reset, PN has not been detected.
PNSUC	08:3	–	**PN Success.** When status bit PNSUC is set, the receiver has successfully trained at the end of the PN portion of the high speed training sequence. When PNSUC is reset, a successful training has not occurred. PNSUC is still valid after the CDET bit is set. (Not available in R6631-12.)
RTSP	07:7	0	**Request To Send Parallel.** The set state of RTSP begins a transmit sequence. The modem will continue to transmit until RTSP is reset, and the turn-off sequence has been completed. RTSP parallels the operation of the hardware $\overline{\text{RTS}}$ control input. These inputs are "ORed" by the modem.
RX	0D:7	–	**Receive State.** When status bit RX is set, the modem is in the receive state and is not transmitting.
SCR1	0C:4	–	**Scrambled Ones.** When the modem is configured as a high speed transmitter, status bit SCR1 = 1 indicates scrambled ones are being sent. When SCR1 = 0, scrambled ones are not being transmitted., When the modem is configured as a high speed receiver, status bit SCR1 = 1 indicates scrambled ones are being received. When SCR1 = 0, scrambled ones are not being received.
SETUP	1F:0	0	**Setup.** Control bit SETUP bit must be set by the host after the host writes a configuration code into the CONF bits (register 6:0-7) or changes a bit in register 7:0-5/6. Setting the SETUP bit informs the modem to implement the configuration change. The modem resets the SETUP bit when the configuration change request is recognized.
SHTR	07:4	0	**Short Train.** When SHTR is set and CONF is either 0A or 09, the modem will perform a V.27 ter short training sequence. A successful V.27 ter long train at the same data rate must precede the short train. The setting of the SHTR bit, along with the setting of the EQSV bit, must be followed by the setting of the SETUP bit.
SIDLE	0C:0	–	**Silence/Idle.** When the modem is configured as a high speed transmitter, status bit SIDLE = 1 indicates the modem is transmitting silence. When the modem is configured as a high speed receiver, status bit SIDLE = 1 indicates the modem is waiting for energy (idling).
SQEXT	07:2	0	**Squelch Extend.** When control bit SQEXT is set, the modem's receiver is inhibited from the reception of any signal for 140 ms after the transmitter turn-off.
T2	07:1	0	**T/2 Equalizer Select.** When control bit T2 is set, the linear section of the receiver's adaptive equalizer is T/2 fractionally spaced. When T2 is reset, the equalizer is T spaced (T = 1 baud time).
TDIS	07:6	0	**Training Disable.** When control bit TDIS is set, the modem as a receiver is prevented from recognizing a training sequence and entering the training state; as a transmitter the modem will not transmit the training sequence when $\overline{\text{RTS}}$ is on or RTSP is set.

Table 10. Modem Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
TRIG	0A:6-7	–	**Interrupt Triggering.** These two bits select how the programmable interrupt is to occur if this interrupt is enabled. The user has the option to be continuously interrupted whenever the interrupt condition is true (DC triggered), to be interrupted only when the interrupt condition transitions from false to true (positive edge triggered), to be interrupted only when the interrupt condition transitions from true to false (negative edge triggered), or to be interrupted when the interrupt condition transitions from false to true or from true to false (edge triggered): TRIG — Description 00 — DC 01 — Positive Edge 10 — Negative Edge 11 — Edge
WRT1	05:1	0	**RAM Write 1.** When control bit WRT1 is set and ACC1 is set, the modem writes the data from the Y RAM Data 1 registers into its internal RAM at the location addressed by ADD1 and CR1. (When the most significant bit of ADD1 is reset, the write is performed to the X RAM location; when a 1, the write is to the Y RAM location.) When WRT1 is reset and ACC1 is set, the modem reads data from its internal RAM from the locations addressed by ADD1 and CR1 and stores it into the X RAM Data 1 registers and Y RAM Data 1 registers, respectively.
WRT2	15:1	0	**RAM Write 2.** When control bit WRT2 is set and ACC2 is set, the modem writes the data from the Y RAM Data 2 registers into its internal RAM at the location addressed by ADD2 and CR2. (When the most significant bit of ADD2 is reset, the write is performed to the X RAM location; when a 1, the write is to the Y RAM location.) When WRT2 is reset and ACC2 is set, the modem reads data from its internal RAM from the locations addressed by ADD2 and CR2 and stores it into the X RAM Data 2 registers and Y RAM Data 2 registers, respectively.
XDAL1	02:0-7	–	**X RAM Data 1 LSB.** XDAL1 is the least significant byte of the 16-bit X RAM 1 data word used in reading X RAM locations.
XDAL2	12:0-7	–	**X RAM Data 2 LSB.** XDAL2 is the least significant byte of the 16-bit X RAM 2 data word used in reading X RAM locations.
XDAM1	03:0-7	–	**X RAM Data 1 MSB.** XDAM1 is the most significant byte of the 16-bit X RAM 1 data word used in reading X RAM locations.
XDAM2	13:0-7	–	**X RAM Data 2 MSB.** XDAM2 is the most significant byte of the 16-bit X RAM 2 data word used in reading X RAM locations.
YDAL1	00:0-7	–	**Y RAM Data 1 LSB.** YDAL1 is the least significant byte of the 16-bit Y RAM 1 data word used in reading or writing Y RAM locations in the modem.
YDAL2	10:0-7	–	**Y RAM Data 2 LSB.** YDAL2 is the least significant byte of the 16-bit Y RAM 2 data word used in reading or writing Y RAM locations in the modem.
YDAM1	01:0-7	–	**Y RAM Data 1 MSB.** YDAM1 is the most significant byte of the 16-bit Y RAM 1 data word used in reading or writing Y RAM locations in the modem.
YDAM2	11:0-7	–	**Y RAM Data 2 MSB.** YDAM2 is the most significant byte of the 16-bit Y RAM 2 data word used in reading or writing Y RAM locations in the modem.
ZEROC	09:4	0	**Zero Clamp.** When control bit ZEROC is set and ABIDL is set, the modem will transmit continuous zeros. When ZEROC is reset and ABIDL is set, the modem will transmit continuous ones. If ABIDL is reset, ZEROC is disabled. (HDLC only.)

Table 11. Modem DSP RAM Access Codes

Function	BRx	CRx	IOx	ADDx	Read Reg. No.
Received Signal Samples	0	0	0	15	2,3
Received Signal Samples (Voice Mode)	0	0	0	A0	0
Received Signal Samples FSK*	0	0	0	31	2,3
Demodulator Output	0	0	0	13	0,1,2,3
Low Pass Filter Output	0	0	0	02	0,1,2,3
Average Energy	0	0	0	14	2,3
AGC Gain Word	0	1	0	15	2,3
AGC Slew Rate	0	0	0	95	0,1
Tone 1 Frequency	0	1	0	21	2,3
Tone 1 Level	0	0	0	22	2,3
Tone 2 Frequency	0	1	0	22	2,3
Tone 2 Level	0	0	0	23	2,3
Output Level	0	0	0	21	2,3
Equalizer Input, Real	1	0	0	1E	0,1
Equalizer Input, Imaginary	1	1	0	1E	0,1
Equalizer Tap Coefficients, 1-40	1	1	0	3A - 61	0,1,2,3
Unrotated Equalizer Output	1	0	0	1C	0,1,2,3
Rotated Equalizer Output, Eye Pattern	1	1	0	17	0,1,2,3
Decision Points, Ideal	1	0	0	17	0,1,2,3
Error Vector	1	1	0	1D	0,1,2,3
Rotation Angle	1	1	0	0C	0,1
Frequency Correction	1	1	0	18	2,3
Eye Quality Monitor, EQM	1	1	0	0D	2,3
RLSD Turn-on Threshold	0	1	0	37	2,3
RLSD Turn-off Threshold	0	1	0	B7	0,1
Receiver Sensitivity, MAXG	0	1	0	24	2,3
Group 2 PLL Frequency Correction	0	0	0	0D	2,3
Group 2 Zero Crossing Threshold (Negative)	0	0	0	19	2,3
Group 2 Zero Crossing Threshold (Positive)	0	0	0	99	0,1
Group 2 AGC Slew Rate	0	1	0	05	2,3
Group 2 Black-White Threshold	0	0	0	24	2,3
Group 2 Phase Limit Value	0	0	0	1A	2,3
Sample Rate, Least Significant Word	0	0	1	28	0,1
Sample Rate, Most Significant Bit	0	0	1	2B	0,1

* R6631-12 only.

MODEM INTERFACE CIRCUIT

CIRCUIT AND COMPONENTS

The modem is supplied as a 68-pin PLCC or 64-pin QUIP device to be designed into OEM circuit boards. The recommended modem interface circuits (Figures 6 and 7) illustrate the connections and components required to connect the modem to the OEM electronics.

If the AUXI input is not used, resistors R10 and R16 can be eliminated and AUXI must be connected to AGND2.

When the cable equalizer controls CABLE1 and CABLE2 are connected to long leads that are subject to picking up noise spikes, a 3K ohm series resistor should be used on each input (CABLE1 and CABLE2) for isolation.

Resistors R7 and R17 can be used to trim the transmit level and receive threshold to the accuracy required by the OEM equipment. For a tolerance of ±1 dBm, the 1% resistor values shown are correct for more than 99.8% of the units.

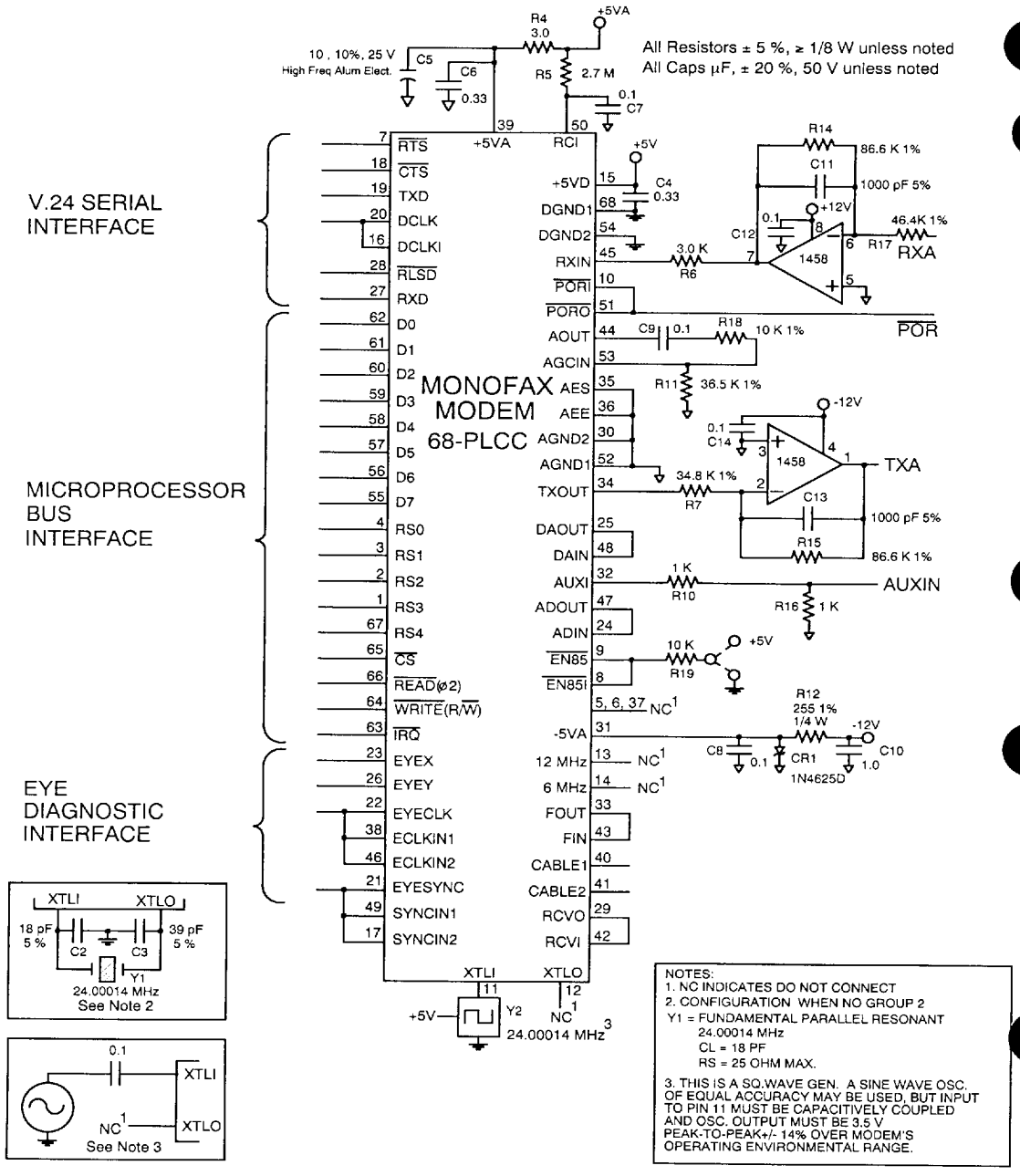


Figure 6. Recommended Modem PLCC Interface Circuit

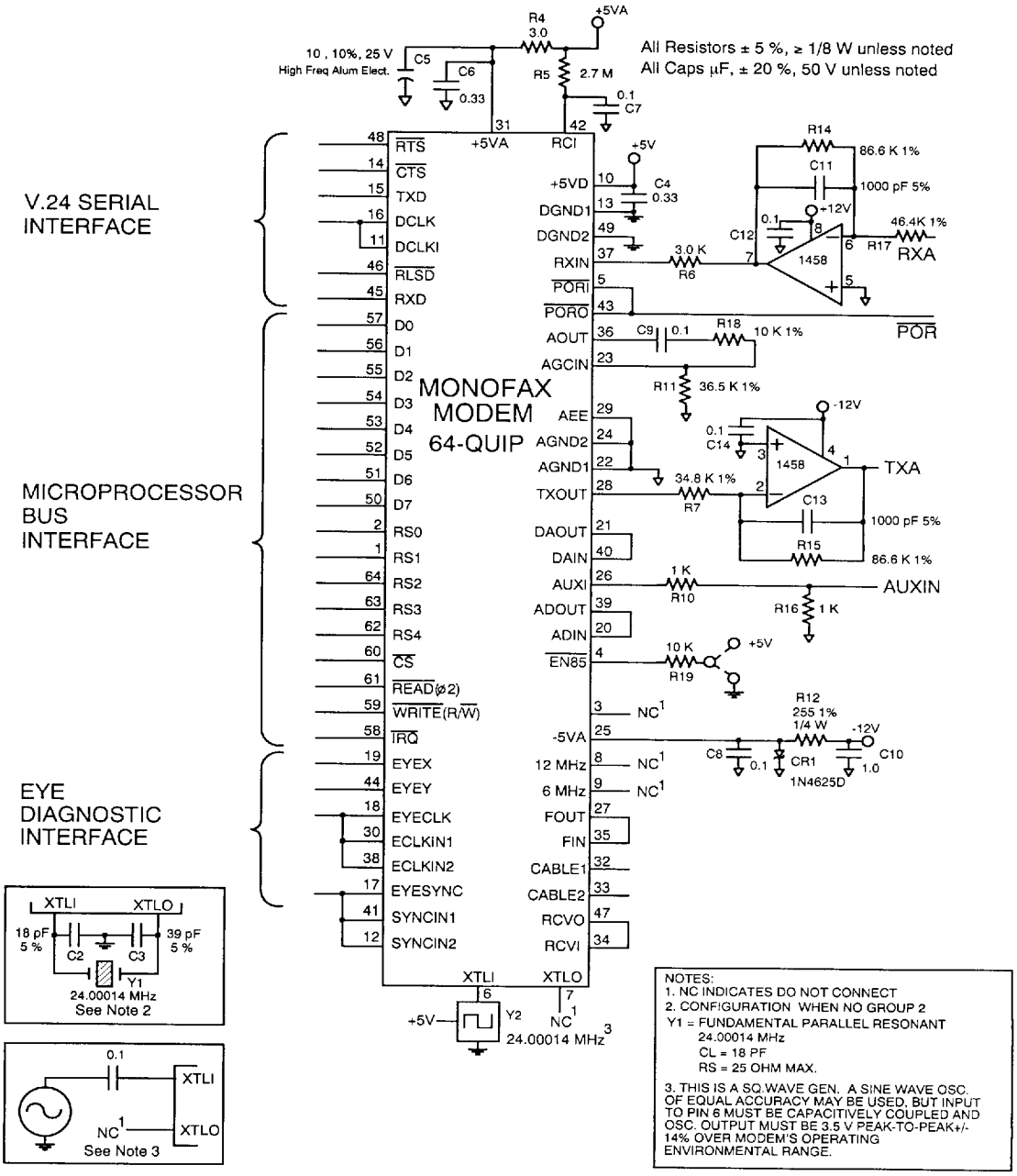


Figure 7. Recommended Modem QUIP Interface Circuit