Features

- **Bipolar Speed**
  - **Read Access Time - 35 ns**
- **Low Power CMOS Operation**
  - **25 mA max. Standby**
  - **45 mA max. Active at 10 MHz**
- **Direct Bipolar PROM Replacement**
- **High Output Drive Capability**
- **Reprogrammable - 100 µs/byte (typical)**
  - **Tested 100% for Programmability**
- **JEDEC Approved Byte-Wide Pinout**
  - **300-mil DIP, 600-mil DIP and LCC packages**
- **CMOS and TTL Compatible Inputs and Outputs**
- **High Reliability Latch-Up Resistant CMOS Technology**
- **Integrated Product Identification Code**
- **Full Military, Industrial and Commercial Temperature Ranges**
- **Fully Compatible with AT27HC641/2**

64K (8K x 8) Reprogrammable CMOS PROM

Description

The AT27HC641R/642R chip family is a high-speed, low-power 65,536 bit reprogrammable read only memory (PROM), which is UV erasable, organized as 8K x 8 bits. All devices require only one 5 V power supply in normal read mode operation. All bytes on the 641R and 642R parts can be accessed in less than 35 ns, making these parts ideal for high-performance systems without penalizing bit density or power consumption.

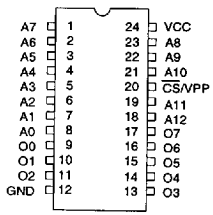
The 640R series of devices come in a choice of JEDEC-approved 24-pin DIP or 28-pad LCC packages, providing a direct power saving CMOS upgrade for systems originally using Bipolar PROMs. The AT27HC641R is available in a standard 600-mil cerdip or one-time programmable plastic (OTP) package, and LCC package, while the AT27HC642R is available in a space-saving 300-mil cerdip or plastic (OTP) package.

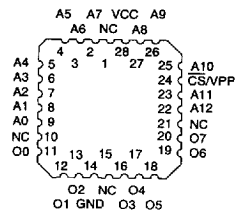
Atmel's 1.2-micron, high-speed CMOS technology provides optimum speed, low-power and high noise immunity. Power consumption on the AT27HC641 and AT27HC642 is typically only 30 mA in Active Mode and less than 10 mA in Standby. The high speed CMOS process is an extension of Atmel's high quality and highly manufacturable floating poly PROM technology. The ability to reprogram the PROM, which is fully tested before shipment, provides inherently better programmability and reliability than one-time fusable PROMs.

(continued)

Pin Configurations

Pin Name	Function
A0-A12	Addresses
$\overline{CS}$/V_{PP}	Chip Select/V_{PP}
O0-O7	Outputs





Description (Continued)

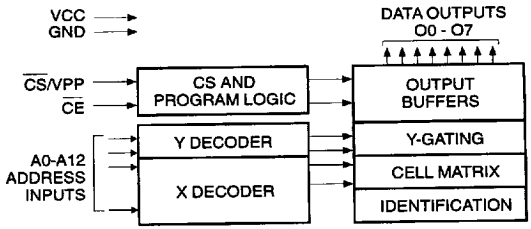
With a storage capacity of 8K bytes, Atmel's 640R series parts allow firmware to be stored reliably and to be accessed at bipolar PROM speeds. All the 640R series parts have exceptional output drive capability - source 4 mA and sink 16 mA per output.

Atmel's 640R series chips also have additional features to ensure high-quality and efficient production use. The Rapid programming algorithm reduces the time required to program the chip and guarantees reliable programming. The Integrated Product Identification Code electronically identifies the device and manufacturing origin. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Erasure Characteristics

The entire memory array of an Atmel 640R series chip is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15W•sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any PROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on A9 with Respect to Ground	-2.0 V to +14.0 V(1)
CS/VPP Supply Voltage with Respect to Ground	-2.0 V to +14.0 V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC}+0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

Operating Modes

MODE \ PIN	CS/VPP	Ai	VCC	Outputs
Read	V_{IL}	Ai	V_{CC}	DOUT
Standby	V_{IH}	X(1)	V_{CC}	High Z
Rapid Program(2)	V_{PP}	Ai	V_{CC}	DIN
PGM Verify	V_{IL}	Ai	V_{CC}	DOUT
Product Identification(4)	V_{IL}	A9=V_H (3) A0=V_{IH} or V_{IL} A1-A12=V_{IL}	V_{CC}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. V_H = 12.0 ± 0.5 V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

D.C. and A.C. Operating Conditions for Read Operation

		AT27HC641R / AT27HC642R				
		-35	-45	-55	-70	-90
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.		-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 5%	5 V ± 10%	5 V ± 10%	5 V ± 10%	5 V ± 10%

4

D.C. and Operating Characteristics for Read Operation

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+1 V			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC}+0.1 V			10	µA
I_{PP1}	$\overline{CS}/V_{PP}$ [1] Read/Standby Current	$\overline{CS}/V_{PP}$ = -0.1 V to V_{CC}+1 V			10	µA
I_{SB}	V_{CC} [1] Standby Current	I_{SB1} (CMOS) $\overline{CS}/V_{PP}$ = V_{CC}-0.3 to V_{CC}+1.0 V	Com.		25	mA
			Ind.,Mil.		30	mA
		I_{SB2} (TTL) $\overline{CS}/V_{PP}$ = 2.0 to V_{CC}+1.0 V	Com.		25	mA
			Ind.,Mil.		30	mA
I_{CC}	V_{CC} Active Current	f = 10 MHz, I_{OUT} = 0 mA, $\overline{CS}/V_{PP}$ = V_{IL}	Com.		45	mA
			Ind.,Mil.		50	mA
I_{OS} [2]	Output Short Circuit Current	V_{OUT} = 0 V			-100	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC}+0.75	V
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			.4	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA		V_{CC}-0.3		V
		I_{OH} = -4.0 mA		2.4		V

Notes: 1. V_{CC} must be applied simultaneously or before $\overline{CS}/V_{PP}$, and removed simultaneously or after $\overline{CS}/V_{PP}$.

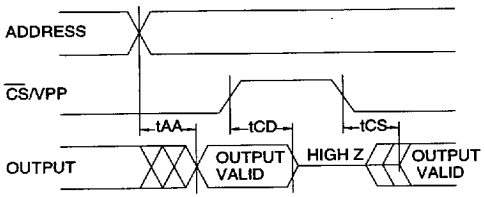
2. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec. This parameter is only sampled and is not 100% tested. See Absolute Maximum Ratings.

A.C. Characteristics for Read Operation

			AT27HC641R / AT27HC642R										
			-35		-45		-55		-70		-90		
Symbol	Parameter		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{AA} [4]	Address to Output Delay	Com.		35		45		55		70		90	ns
		Ind.,Mil				45		55		70		90	ns
t_{CS} [2,4]	$\overline{CS}/V_{PP}$ to Output Delay			25		30		35		45		55	ns
t_{CD} [3,4,5]	$\overline{CS}/V_{PP}$ to Output Float		0	25	0	30	0	35	0	40	0	45	ns

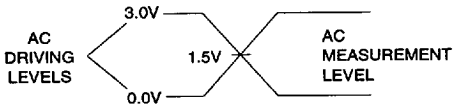
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

A.C. Waveforms for Read Operation [1]



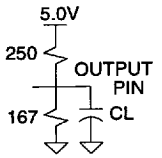
Notes:
1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.
2. Asserting $\overline{CS}/V_{PP}$ may be delayed up to $t_{AA} - t_{CS}$ after the address transition without impact on access time.
3. This parameter is only sampled and is not 100% tested.
4. $C_L = 30$ pF, add 10 ns for $C_L = 100$ pF.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveforms and Measurement Levels



t_R, $t_F < 5$ ns (10% to 90%)

Output Test Load



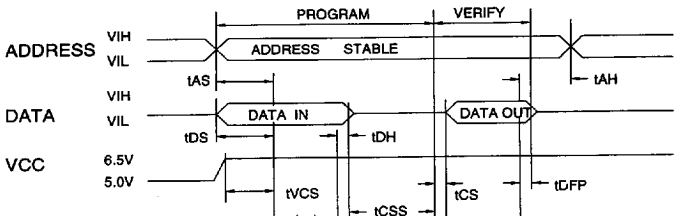
Note: C_L=30pF including jig capacitance.

Pin Capacitance (f = 1 MHz T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. The Input Timing References are 0.0 V for V_{IL} and 3.0 V for V_{IH}.
2. t_{CS} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

D.C. Programming Characteristics

T_A= 25 ± 5°C, V_{CC} = 6.5± 0.25 V, $\overline{CS}/V_{PP}$ = 13.0 ± 0.25 V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC}+1	V
V_{OL}	Output Low Volt.	I_{OL} = 16 mA		.4	V
V_{OH}	Output High Volt.	I_{OH}= -4.0 mA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			50	mA
I_{PP2}	$\overline{CS}/V_{PP}$ Supply Current	$\overline{CS}/V_{PP}=V_{PP}$		30	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

T_A = 25 ± 5°C, V_{CC}= 6.5 ± 0.25 V, $\overline{CS}/V_{PP}$=13.0 ± 0.25 V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Limits Max	Units
t_{AS}	Address Setup Time		2		µs
t_{CSS}	$\overline{CS}/V_{PP}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{CS}/V_{PP}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CS}/V_{PP}$ Program Pulse Width	(Note 3)	95	105	µs
t_{CS}	Data Valid from $\overline{CS}/V_{PP}$			70	ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) ..... 5 ns
Input Pulse Levels ..... 0.0 V to 3.0 V
Input Timing Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V

Notes:

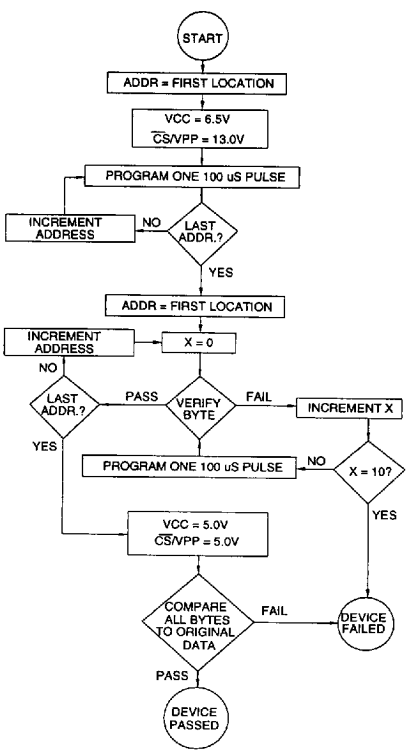
1. V_{CC} must be applied simultaneously or before $\overline{CS}/V_{PP}$ and removed simultaneously or after $\overline{CS}/V_{PP}$.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100 µsec ± 5%.

Atmel's 27HC641R/2R Integrated Product Identification Code

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	1	0	0	0	0	10

Rapid Programming Algorithm

A 100 µs $\overline{CS}/V_{PP}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5 V and $\overline{CS}/V_{PP}$ is raised to 13.0 V. Each address is first programmed with one 100 µs $\overline{CS}/V_{PP}$ pulse without verification. Then a verification / re-programming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. $\overline{CS}/V_{PP}$ is then lowered to 5.0 V and V_{CC} to 5.0 V. All bytes are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
35	45	25	AT27HC641R-35DC AT27HC642R-35DC AT27HC641R-35LC	24DW6 24DW3 28LW	Commercial (0°C to 70°C)
45	45	25	AT27HC641R-45DC AT27HC642R-45DC AT27HC641R-45LC AT27HC641R-45PC AT27HC642R-45PC	24DW6 24DW3 28LW 24P6 24P3	Commercial (0°C to 70°C)
45	50	30	AT27HC641R-45DI AT27HC642R-45DI AT27HC641R-45LI AT27HC641R-45PI AT27HC642R-45PI	24DW6 24DW3 28LW 24P6 24P3	Industrial (-40°C to 85°C)
			AT27HC641R-45DM AT27HC642R-45DM AT27HC641R-45LM	24DW6 24DW3 28LW	Military (-55°C to 125°C)
			AT27HC641R-45DM/883 AT27HC642R-45DM/883 AT27HC641R-45LM/883	24DW6 24DW3 28LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
55	45	25	AT27HC641R-55DC AT27HC642R-55DC AT27HC641R-55LC AT27HC641R-55PC AT27HC642R-55PC	24DW6 24DW3 28LW 24P6 24P3	Commercial (0°C to 70°C)
55	50	30	AT27HC641R-55DI AT27HC642R-55DI AT27HC641R-55LI AT27HC641R-55PI AT27HC642R-55PI	24DW6 24DW3 28LW 24P6 24P3	Industrial (-40°C to 85°C)
			AT27HC641R-55DM AT27HC642R-55DM AT27HC641R-55LM	24DW6 24DW3 28LW	Military (-55°C to 125°C)
			AT27HC641R-55DM/883 AT27HC642R-55DM/883 AT27HC641R-55LM/883	24DW6 24DW3 28LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
70	45	25	AT27HC641R-70DC AT27HC642R-70DC AT27HC641R-70LC AT27HC641R-70PC AT27HC642R-70PC	24DW6 24DW3 28LW 24P6 24P3	Commercial (0°C to 70°C)
70	50	30	AT27HC641R-70DI AT27HC642R-70DI AT27HC641R-70LI AT27HC641R-70PI AT27HC642R-70PI	24DW6 24DW3 28LW 24P6 24P3	Industrial (-40°C to 85°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	50	30	AT27HC641R-70DM AT27HC642R-70DM AT27HC641R-70LM	24DW6 24DW3 28LW	Military (-55°C to 125°C)
			AT27HC641R-70DM/883 AT27HC642R-70DM/883 AT27HC641R-70LM/883	24DW6 24DW3 28LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	45	25	AT27HC641R-90DC AT27HC642R-90DC AT27HC641R-90LC AT27HC641R-90PC AT27HC642R-90PC	24DW6 24DW3 28LW 24P6 24P3	Commercial (0°C to 70°C)
90	50	30	AT27HC641R-90DI AT27HC642R-90DI AT27HC641R-90LI AT27HC641R-90PI AT27HC642R-90PI	24DW6 24DW3 28LW 24P6 24P3	Industrial (-40°C to 85°C)
			AT27HC641R-90DM AT27HC642R-90DM AT27HC641R-90LM	24DW6 24DW3 28LW	Military (-55°C to 125°C)
			AT27HC641R-90DM/883 AT27HC642R-90DM/883 AT27HC641R-90LM/883	24DW6 24DW3 28LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
45	50	30	5962-87515 01 JX 5962-87515 01 KX 5962-87515 01 LX 5962-87515 01 3X	24DW6 24CW 24DW3 28LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
55	50	30	5962-87515 02 JX 5962-87515 02 KX 5962-87515 02 LX 5962-87515 02 3X	24DW6 24CW 24DW3 28LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
70	50	30	5962-87515 03 JX 5962-87515 03 KX 5962-87515 03 LX 5962-87515 03 3X	24DW6 24CW 24DW3 28LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	50	30	5962-87515 04 JX 5962-87515 04 KX 5962-87515 04 LX 5962-87515 04 3X	24DW6 24CW 24DW3 28LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
24CW	24 Lead, Windowed, Ceramic Flat Package (Cerpack)
24DW3	24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
24DW6	24 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
28LW	28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
24P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)