XC9101/02 Series

PWM Controlled, PWM//PFM Switchable Step-Up DC/DC Converters

Sep. 06, 01 Ver. III

◆Input Voltage Range : 2.0V ~20V
◆Output Voltage Range : 2.2V ~ 16V
◆Oscillation Frequency Range : 100kHz ~ 600kHz
◆Output Current : up to 3A
◆Ceramic capacitor compatible
◆MSOP-8A Package

■Applications
●Mobile, Cordless phones
●Palm top computers, PDAst
●Portable games
●Cameras, Digital cameras
●Laptops

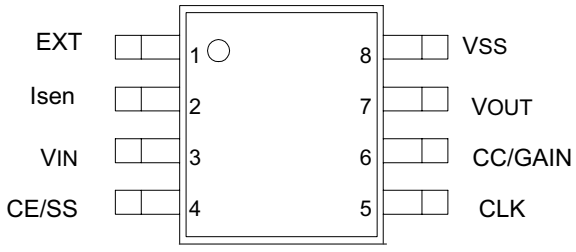
■General Description

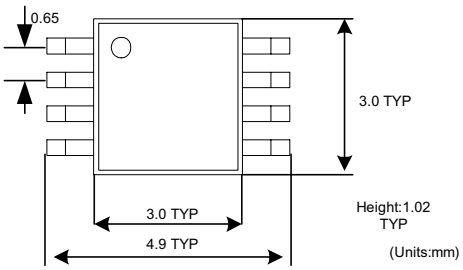
The XC9101/9102 series are step-up multiple current and voltage feedback DC/DC controller ICs. Current sense, clock frequencies and amp feedback gain can all be externally regulated. A stable power supply is possible with output currents of up to 3A and output voltage is selectable in 0.1V steps within a 2.2V - 16.0V (±2.5% accuracy) range (internal). Further, a type which has a 0.9V internal reference voltage and which allows output voltage to be set-up freely via the external components is also available (FB type). Switching frequencies can be regulated externally within a range of 100 ~600 kHz and therefore frequencies suited to your particular application are selectable.
The XC9102 series switches from PWM to current limited PFM control during light loads and the series offers low ripple and high efficiencies from light loads through to large output currents. Further, the drive transistor's current limit can be applied via the current sense function and soft-start times can be regulated by the external resistors and capacitors.
During shutdown (CE pin =L), consumption current can be reduced to as little as 0.5μA or less.

■Features

Stable Operations via Current & Voltage Multiple Feedback
Unlimited Options for Peripheral Selection
PWM/PFM Switching Control (XC9102)
Current Protection Circuit
Low Ripple Output Voltage during Light Loads (XC9102)
Ceramic Capacitor Compatible

■Pin Configuration





■Pin Assignment

PIN NUMBER	PIN NAME	FUNCTION	PIN NUMBER	PIN NAME	FUNCTION
1	EXT	Driver	5	CLK	Clock Input
2	Isen	Current Sense	6	CC / GAIN	Phase Compensation
3	VIN	Power Input	7	VOUT / FB	Voltage Sense
4	CE / SS	CE/Soft Start	8	VSS	Ground

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■Ordering Information

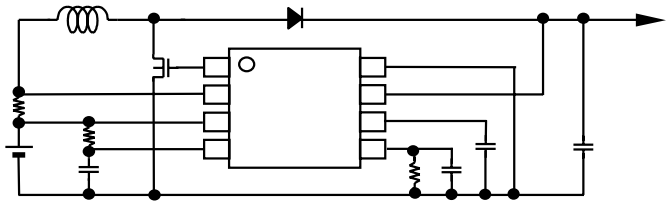
XC9101①②③④⑤⑥

①	C	VOUT	Soft-start externally set-up
	D	FB	Soft-start externally set-up
②③	20 ~ G0	Output Voltage : For the voltage above 10V, see the example	
		10=A, 11=B, 12=C, 13=D, 14=E, 15=F, 16=G	
		e.g. VOUT=2.3V → b=2, c=3 VOUT=13.5V → b=D, c=5	
	09	FB products	
④	A	Adjustable Frequency	
⑤	K	MSOP-8A	
⑥	R	Embossed tape. Standard Feed	
	L	Embossed tape. Reverse Feed	

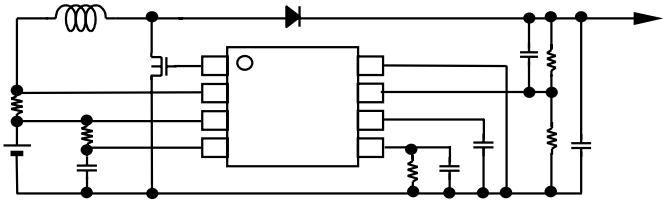
The standard output voltage of XC9101C series are 2.5V, 3.3V, and 5.0V. The voltage other than listed are semi-custom.

■Typical Application

XC9101C/9102C : Output Voltage Internally Set-up



XC9101D/9102D : Output Voltage adjustable externally (FB)



■Absolute Maximum Ratings

Ta=25°C

PARAMETER	SYMBOL	RATINGS	UNITS
EXT pin Voltage	VEXT	-0.3~+22	V
Isen pin Voltage	Visen	-0.3~+22	V
VIN pin Voltage	VIN	-0.3~+22	V
CE/SS pin Voltage	VCE	-0.3~+22	V
CLK pin Voltage	VCLK	-0.3~+22	V
CC/GAIN pin Voltage	VCC	-0.3~+22	V
VOUT/FB pin Voltage	VOUT	-0.3~+22	V
EXT pin Current	IEXT	±100	mA
Continuous Total Power Dissipation	Pd	150	mW
Operating Ambient Temperature	Topr	-40~+85	°C
Storate Temperature	Tstg	-40~+125	°C

■Electrical Characteristics

XC9101C25AKR VOUT=2.5V, FOSC=300kHz, Ta=25°C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUITS
Output Voltage	VOUT	IOUT=300mA	2.438	2.500	2.562	V	❶
Maximum Operating Voltage	VINmax		20			V	
Minimum Operating Voltage	VST1				2.0	V	
Supply Current 1	IDD1	VOUT=Set Output Voltage × 0.95, CE=VIN		130		μA	❷
Supply Current 2	IDD2	VOUT=Set Output Voltage + 0.5, CE=VIN		20		μA	❷
Stand-by Current	ISTB	VIN=20V, CE=VSS		0.3		μA	❷
CLK Oscillation Frequency	FOSC	RT=3.0kΩ, CT=270pF		300		kHz	❸
Frequency Input Stability	$\frac{\Delta FOSC}{\Delta VIN \cdot FOSC}$	VIN=2.0V~16V		5		% / V	❸
Frequency Temperature Fluctuation	$\frac{\Delta FOSC}{\Delta TOPR \cdot FOSC}$	VIN=2.0V		±10		%	❸
Maximum Duty Cycle	MAXDTY	VOUT=VSS (Max.duty of PWM)		83		%	❺
Current Limiter PFM	IPFM	Average SENSE Current (XC9102) Operation switches to PWM when exceeding this value.		400		mA	❺
Current Limiter Maximum Duty Cycle	IPFMDTY	Max.duty of PFM		83		%	❺
Current Limiter SENSE Voltage	CLIM	Rsen : Resistance Voltage		150		mV	❻
CE "High" Voltage	VCEH	Existance of CLK Oscillation		1		V	❺
CE "Low" Voltage	VCEL	Dissapearance of CLK Oscillation		0.9		V	❺
EXT "High" ON Resistance	REXTH	EXT=VIN - 0.5V, VOUT = VSS		16		Ω	❹
EXT "Low" ON Resistance	REXTL	EXT=0.5V, VOUT=Set Voltage x 1.05		16		Ω	❹
Efficiency	EFFI	VIN=2.0V, *1		85		%	❶
Soft-start Time	TSS	CE/SS 240kΩ, 0.0047pF connected *2		5		mS	❾
CC/GAIN Pin Output Impedance	RCCGAIN			500		kΩ	❼

VIN = 2.0V unless specified

*1 : EFFI = {[(Output Voltage) × (Output Current)] ÷ [(Input Voltage) × (Input Current)]} × 100

*2 : Soft-start Time Measuring CE : 0V→ 3.0V

■Electrical Characteristics

XC9101C33AKR VOUT=3.3V, FOSC=300kHz, Ta=25°C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUITS
Output Voltage	VOUT	IOUT=300mA	3.218	3.300	3.383	V	❶
Maximum Operating Voltage	VINmax		20			V	
Minimum Operating Voltage	VST1				2.0	V	
Supply Current 1	IDD1	VOUT=Set Output Voltage × 0.95, CE=VIN		130		μA	❷
Supply Current 2	IDD2	VOUT=Set Output Voltage + 0.5, CE=VIN		20		μA	❷
Stand-by Current	ISTB	VIN=20V, CE=VSS		0.3		μA	❷
CLK Oscillation Frequency	FOSC	RT=3.0kΩ, CT=270pF		300		kHz	❸
Frequency Input Stability	$\frac{\Delta FOSC}{\Delta VIN \cdot FOSC}$	VIN=2.0V~16V		5		% / V	❸
Frequency Temperature Fluctuation	$\frac{\Delta FOSC}{\Delta TOPR \cdot FOSC}$	VIN=2.0V		±10		%	❸
Maximum Duty Cycle	MAXDTY	VOUT=VSS (Max.duty of PWM)		83		%	❺
Current Limiter PFM	IPFM	Average SENSE Current (XC9102) Operation switches to PWM when exceeding this value.		400		mA	❺
Current Limiter Maximum Duty Cycle	IPFMDTY	Max.duty of PFM		83		%	❺
Current Limiter SENSE Voltage	CLIM	Rsen : Resistance Voltage		150		mV	❻
CE "High" Voltage	VCEH	Existance of CLK Oscillation		1		V	❺
CE "Low" Voltage	VCEL	Dissapearance of CLK Oscillation		0.9		V	❺
EXT "High" ON Resistance	REXTH	EXT=VIN - 0.5V, VOUT = VSS		16		Ω	❹
EXT "Low" ON Resistance	REXTL	EXT=0.5V, VOUT=Set Voltage x 1.05		16		Ω	❹
Efficiency	EFFI	VIN=2.0V, *1		85		%	❶
Soft-start Time	TSS	CE/SS 240kΩ, 0.0047pF connected *2		5		mS	❾
CC/GAIN Pin Output Impedance	RCCGAIN			500		kΩ	❼

VIN = 2.0V unless specified

*1 : EFFI = {[(Output Voltage) × (Output Current)] ÷ [(Input Voltage) × (Input Current)]} × 100

*2 : Soft-start Time Measuring CE : 0V→ 3.0V

■Electrical Characteristics

XC9101C50AKR VOUT=5.0V, FOSC=300kHz, Ta=25°C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUITS
Output Voltage	VOUT	IOUT=300mA	4.875	5.000	5.125	V	❶
Maximum Operating Voltage	VINmax		20			V	
Minimum Operating Voltage	VST1				2.0	V	
Supply Current 1	IDD1	VOUT=Set Output Voltage × 0.95, CE=VIN		130		μA	❷
Supply Current 2	IDD2	VOUT=Set Output Voltage + 0.5, CE=VIN		20		μA	❷
Stand-by Current	ISTB	VIN=20V, CE=VSS		0.3		μA	❷
CLK Oscillation Frequency	FOSC	RT=3.0kΩ, CT=270pF		300		kHz	❸
Frequency Input Stability	$\frac{\Delta FOSC}{\Delta VIN \cdot FOSC}$	VIN=2.0V~16V		5		% / V	❸
Frequency Temperature Fluctuation	$\frac{\Delta FOSC}{\Delta TOPR \cdot FOSC}$	VIN=2.0V		±10		%	❸
Maximum Duty Cycle	MAXDTY	VOUT=VSS (Max.duty of PWM)		83		%	❺
Current Limiter PFM	IPFM	Average SENSE Current (XC9102) Operation switches to PWM when exceeding this value.		400		mA	❺
Current Limiter Maximum Duty Cycle	IPFMDTY	Max.duty of PFM		83		%	❺
Current Limiter SENSE Voltage	CLIM	Rsen : Resistance Voltage		150		mV	❻
CE "High" Voltage	VCEH	Existance of CLK Oscillation		1		V	❺
CE "Low" Voltage	VCEL	Dissapearance of CLK Oscillation		0.9		V	❺
EXT "High" ON Resistance	REXTH	EXT=VIN - 0.5V, VOUT = VSS		16		Ω	❹
EXT "Low" ON Resistance	REXTL	EXT=0.5V, VOUT=Set Voltage x 1.05		16		Ω	❹
Efficiency	EFFI	VIN=2.0V, *1		85		%	❶
Soft-start Time	TSS	CE/SS 240kΩ, 0.0047pF connected *2		5		mS	❾
CC/GAIN Pin Output Impedance	RCCGAIN			500		kΩ	❼

VIN = 2.0V unless specified

*1 : EFFI = {[(Output Voltage) × (Output Current)] ÷ [(Input Voltage) × (Input Current)]} × 100

*2 : Soft-start Time Measuring CE : 0V→ 3.0V

■Electrical Characteristics

XC9101D09AKR VOUT=2.7V, FOSC=300kHz, Ta=25°C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUITS
FB Voltage	VOUT	IOUT=300mA	0.878	0.900	0.923	V	❽
Maximum Operating Voltage	VINmax		20			V	
Minimum Operating Voltage	VST1				2.0	V	
Supply Current 1	IDD1	VOUT=Set Output Voltage × 0.95, CE=VIN		130		μA	❷
Supply Current 2	IDD2	VOUT=Set Output Voltage + 0.5, CE=VIN		20		μA	❷
Stand-by Current	ISTB	VIN=20V, CE=VSS		0.3		μA	❷
CLK Oscillation Frequency	FOSC	RT=3.0kΩ, CT=270pF		300		kHz	❸
Frequency Input Stability	$\frac{\Delta FOSC}{\Delta VIN \cdot FOSC}$	VIN=2.0V~20V		5		% / V	❸
Frequency Temperature Fluctuation	$\frac{\Delta FOSC}{\Delta TOPR \cdot FOSC}$	VIN=2.0V		±10		%	❸
Maximum Duty Cycle	MAXDTY	VOUT=VSS (Max.duty of PWM)		83		%	❺
Current Limiter PFM	IPFM	Average SENSE Current (XC9102) Operation switches to PWM when exceeding this value.		400		mA	❺
Current Limiter Maximum Duty Cycle	IPFMDTY	Max.duty of PFM		83		%	❺
Current Limiter SENSE Voltage	CLIM	Rsen : Resistance Voltage		150		mV	❻
CE "High" Voltage	VCEH	Existance of CLK Oscillation		1		V	❺
CE "Low" Voltage	VCEL	Dissapearance of CLK Oscillation		0.9		V	❺
EXT "High" ON Resistance	REXTH	EXT=VIN - 0.5V, VOUT = VSS		16		Ω	❹
EXT "Low" ON Resistance	REXTL	EXT=0.5V, VOUT=Set Voltage x 1.05		16		Ω	❹
Efficiency	EFFI	VIN=2.0V, *1		85		%	❽
Soft-start Time	TSS	CE/SS 240kΩ, 0.0047pF connected *2		5		mS	❿
CC/GAIN Pin Output Impedance	RCCGAIN			500		kΩ	❼

VIN = 2.0V unless specified

*1 : EFFI = {[(Output Voltage) × (Output Current)] ÷ [(Input Voltage) × (Input Current)]} × 100

*2 : Soft-start Time Measuring CE : 0V→ 3.0V

■Test Circuits

Fig. ❶

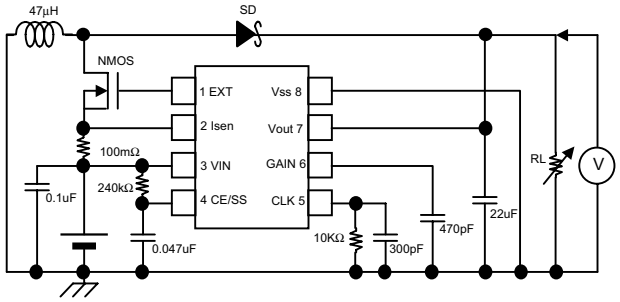


Fig. ❷

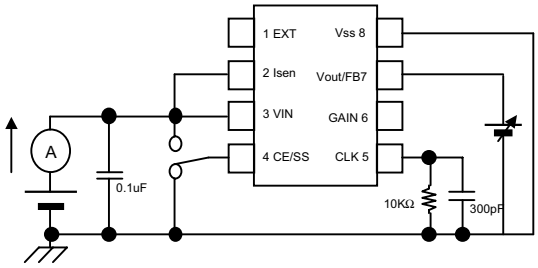


Fig. ❸

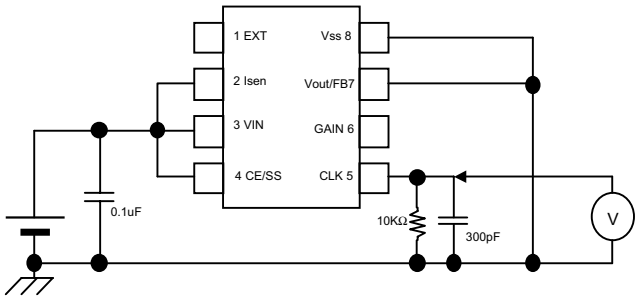


Fig. ❹

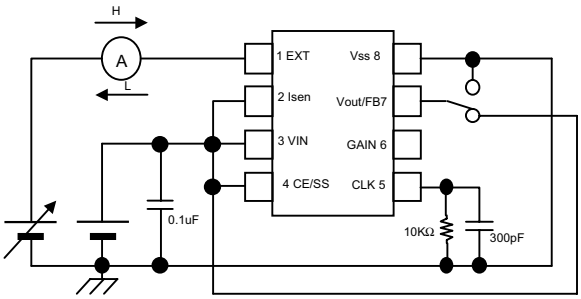


Fig. ❺

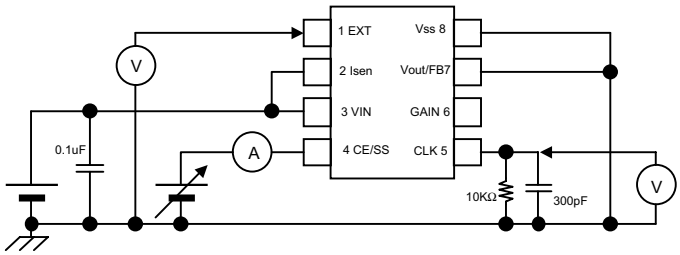


Fig. ❻

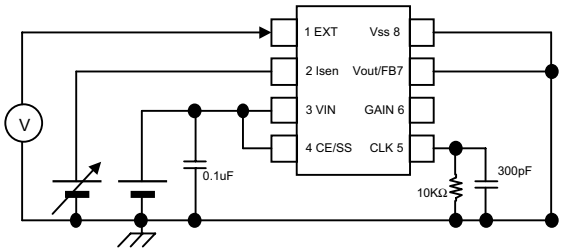


Fig. ❼

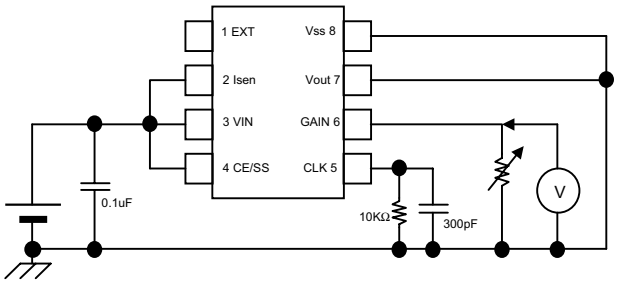


Fig. ❽

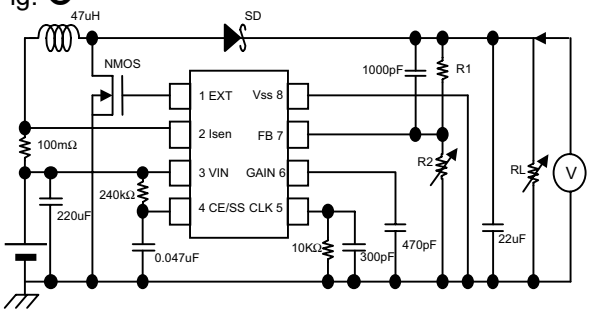


Fig. ❾

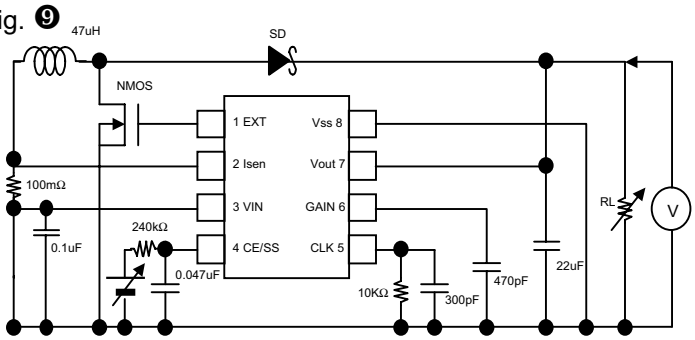
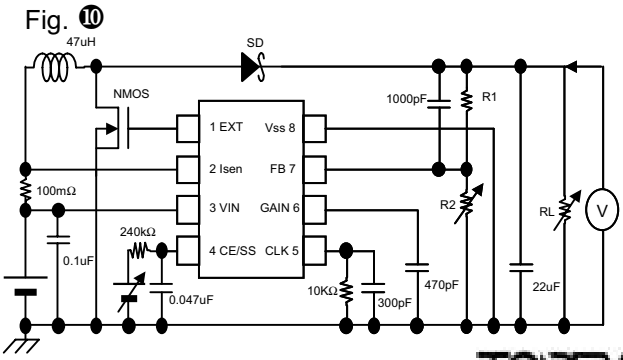


Fig. ❿



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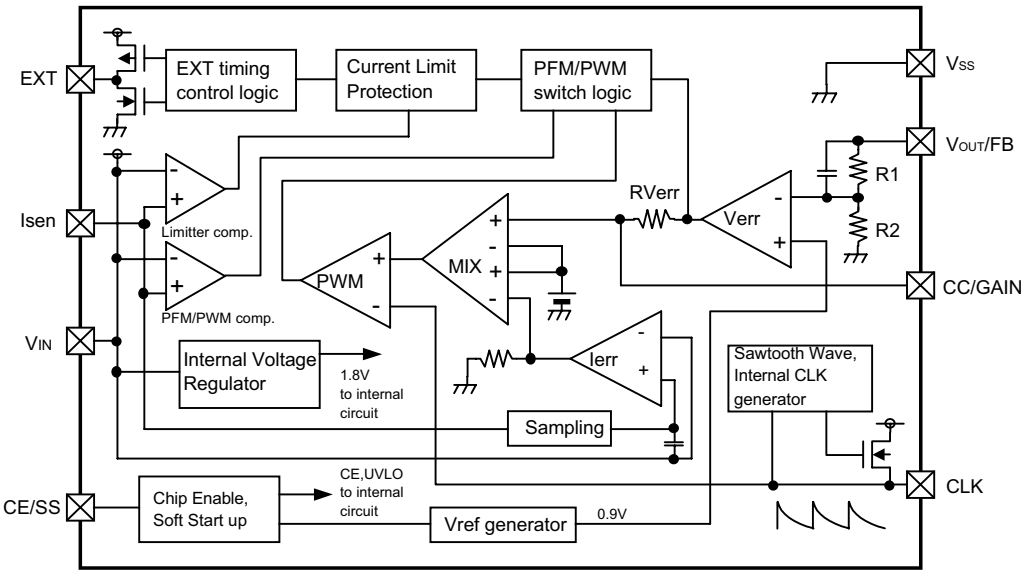
■ Block Diagram



■ Operation Description

Step-up DC/DC converter controllers of the XC9101/9102 series carry out pulse width modulation (PWM) according to the multiple feedback signals of the output voltage and coil current. The XC9102 series achieves high efficiency within a wide load range, shifting to pulse frequency modulation (PFM) under a light load condition.

The internal circuits consist of different blocks that operate at V_{IN} or the stabilized power (1.8 V) of the internal regulator. The output setting voltage of type C controller and the FB pin voltage (Vref = 0.9 V) of type D controller have been adjusted and set by laser-trimming.

<Clock>

With regard to clock pulses, a capacitor and resistor connected to the CLK pin generate sawtooth waveforms whose top and bottom are 0.7 V and 0.15 V, respectively. The frequency can be set within a range of 100 to 600 kHz by external constants (see the section "Functional Settings" for constants). The clock pulses are processed to generate a signal used for synchronizing internal sequence circuits.

<Verr amplifier>

The Verr amplifier is designed to monitor the output voltage. A fraction of the voltage applied to internal resistors (R1, R2) in the case of a type C controller, and the voltage of the FB pin in the case of a type D controller are fed back and compared with the reference voltage. In response to feedback of a voltage lower than the reference voltage, the output voltage of the Verr amplifier increases.

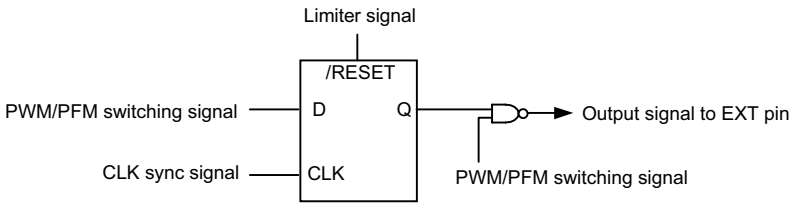
The output of the Verr amplifier goes directly to the PFM/PWM switch logic and is also led to the mixer via a resistor (RVerr). The former signal acts as a voltage sensor in PFM mode. The latter signal works as a pulse width control signal in PWM mode. Connecting an external capacitor and resistor makes it possible to set the gain and frequency characteristics of Verr amplifier signals (see the section "Functional Settings" for constants).

<Ierr amplifier>

The Ierr amplifier monitors the coil current. The potential difference between the V_{IN} and Isen pins are sampled each time of switching operation. Then the potential difference is amplified or held, as necessary, and input to the mixer. The Ierr amplifier outputs a signal ensuring that the greater the potential difference between the V_{IN} and Isen pins, the smaller the switching current. The gain and frequency characteristics of this amplifier are fixed internally.

<Mixer and PWM>
The mixer modulates the signal sent from Verr by the signal from Ierr. The modulated signal enters the PWM comparator for comparison with the sawtooth pulses generated at the CLK pin. If the signal is greater than the sawtooth waveforms, a signal is sent to the output circuit to turn on the external switch.

<Current Limiter>
The current flowing through the coil is monitored by the limiter comparator via the V_{IN} and Isen pins. The limiter comparator outputs a signal when the potential difference between the VIN and Isen pins reaches 150 mV or more. This signal is converted to a logic signal and handled as a DFF reset signal for the internal limiter circuit. When a reset signal is input, a signal is output immediately at the EXT pin to turn off the MOS switch. When the limiter comparator sends a signal to enable data acceptance, a signal to turn on the MOS switch is output at the next clock pulse. If at this time the potential difference between the V_{IN} and Isen pins is great, operation is repeated to turn off the MOS switch again. DFF operates in synchronization with the clock signal of the CLK pin.



<Soft Start>
The soft start function is made available by attaching a capacitor and resistor to the CE/SS pin. The Vref voltage applied to the Verr amplifier is restricted by the start-up voltage of the CE/SS pin. Doing so ensures that the Verr amplifier operates with its two inputs in balance, thereby preventing the ON-TIME signal from becoming stronger than necessary. Consequently, soft start time needs to be set sufficiently longer than the time set to CLK. The start-up time of the CE/SS pin equals the time set for soft start (see the section "Functional Settings" for constants).

<PWM/PFM Switching>
The controllers of the XC9102 series switch between PFM and PWM modes automatically. The PFM/PWM comparator monitors the current each time switching occurs. When the current decreases to a certain value or below, a shift from PWM to PFM mode occurs.

To be specific, current-limiting PFM is carried out in the PFM mode. When V_{OUT} (or the FB voltage in the case of type D) decreases below the set value, the Verr amplifier sends a signal directly to the logic block to turn on the external MOS switch. An ON signal is output from the EXT pin in synchronization with the clock signal of the CLK pin. When the external MOS switch is turned on, a current flows through the coil at the same time. The external MOS switch is turned off by a current-limit signal of the limiter comparator (set to a different level than the limiter voltage in PWM mode), the leading edge of the next clock signal, or an increase in the output voltage. The logic is programmed for the PFM mode so that a signal is generated in synchronization with the leading edge of the clock signal at CLK to turn off the external switch for a fixed period.

The controller stops required operation if the output voltage exceeds the set value after a single cycle of switching operation and waits for another drop in the output voltage. If the set value is not exceeded, pulses are output successively. Since the current flowing through the coil is limited by the limiter comparator, output voltage ripple is held below a certain value.

If the PFM/PWM comparator indicates PWM mode constantly as a result of frequent occurrence of successive pulses, the controller operates in PWM mode continuously. As the PWM mode is active constantly behind the PFM mode, shifting between modes occurs smoothly. Clock pulses at the CLK pin do not stop even in PFM mode.

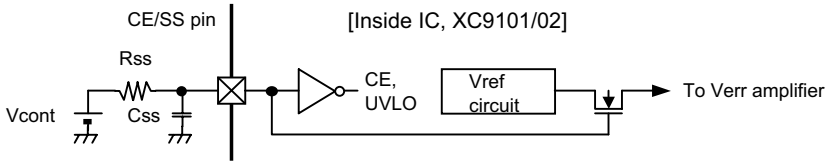
■ Functional Settings

1. Soft Start

CE and soft start (SS) functions are commonly assigned to the CE/SS pin. The soft start function is effective until the voltage at the CE pin reaches approximately 1.55 V rising from 0 V. Soft start time is approximated by the equation below according to values of Vcont, Rss, and Css.

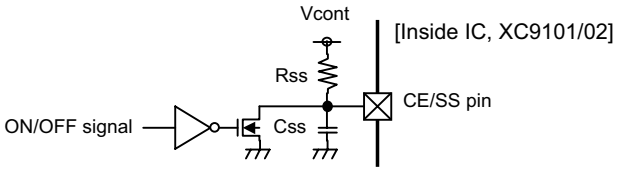
$$T = -Css \times Rss \times \ln((Vcont - 1.55)/Vcont)$$

Example: When Css = 0.1 μF, Rss = 470 kΩ, and Vcont = 5 V, $T = -0.1\ e^{-6} \times 470\ e^{3} \times \ln((5 - 1.55)/5) = 17.44$ ms.

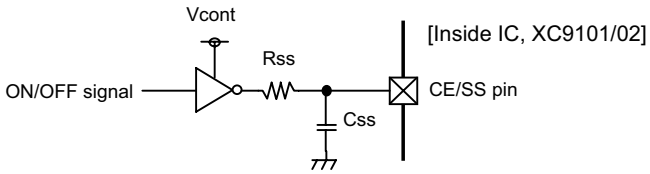


Set the soft start time to a value sufficiently longer than the period of a clock pulse.

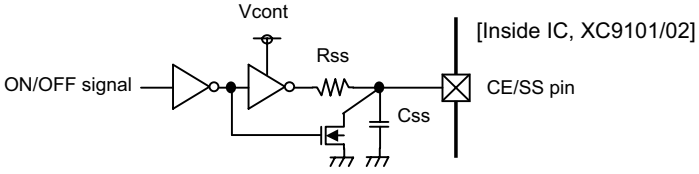
> Circuit example 1: Nch open drain



> Circuit example 2: CMOS logic (low current dissipation)



> Circuit example 3: CMOS logic (low current dissipation), quick off

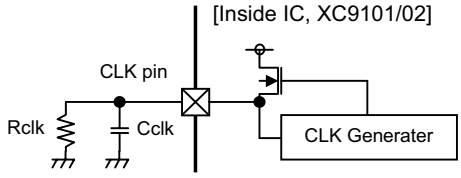


2. Oscillation Frequency

The oscillation frequency of the internal clock generator is approximated by the following equation according to the values of capacitor and resistor attached to the CLK pin.

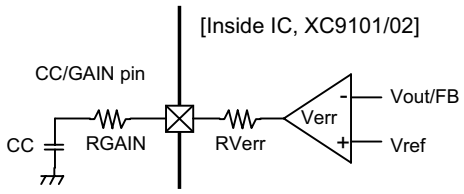
$$f = 1/(-Cclk \times Rclk \times \ln 0.2)$$

Example: When Cclk = 330 pF and Rclk = 5 kΩ, $f = 1/(-330e^{-12} \times 5e^{3} \times \ln(0.2)) = 376.56$ kHz.



3. Gain and Frequency Characteristics of the Verr Amplifier

The gain at output and frequency characteristics of the Verr amplifier are adjusted by the values of capacitor and resistor attached to the CC/GAIN pin. It is generally recommended to attach a CC of 220 to 1,000 pF without an RGAIN. The greater the CC value, the more stable the phase and the slower the transient response.

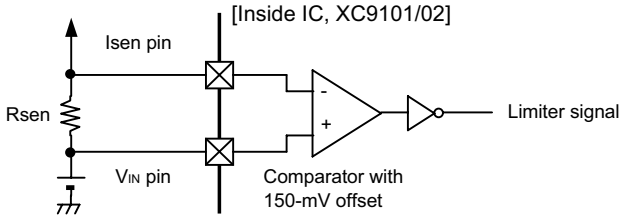


4. Current Limiting

The current limiting value is approximated by the following equation according to resistor Rsen inserted between the V_{IN} and Isen pins. Double function, current FB input and current limiting, is assigned to the Isen pin.

$$Ilimit = 0.15/Rsen$$

Example: When Rsen = 100 mΩ, Ilimit = 0.15/0.1 = 1.5 A



5. FB Voltage and Cfb

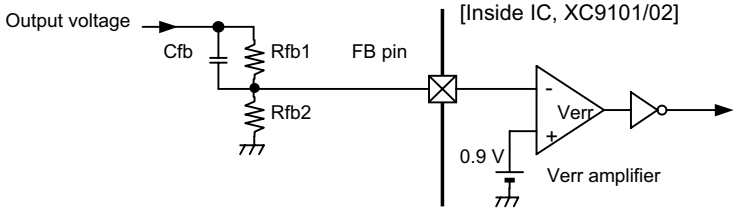
With regard to the XC9101D series, the output voltage is set by attaching externally dividing resistors. The output voltage is determined by the equation shown below according to the values of Rfb1 and Rfb2. In general, the sum of Rfb1 and Rfb2 should be 1 MEG Ω or less.

$$V_{OUT} = 0.9 \times (Rfb1 + Rfb2)/Rfb2$$

The value of Cfb (phase compensation capacitor) is approximated by the following equation according to the values of Rfb1 and fzfb. The value of fzfb should be 10 kHz, as a general rule.

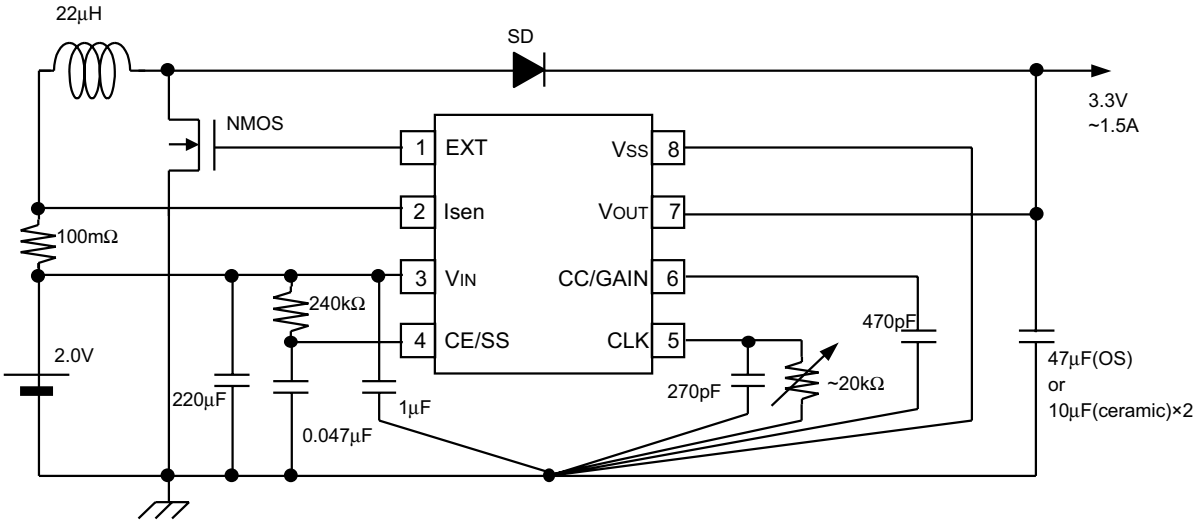
$$Cfb = 1/(2 \times \pi \times Rfb1 \times fzfb)$$

Example: When Rfb1 = 455 kΩ and Rfb2 = 100 kΩ, V_{OUT} = 0.9 x (455 k + 100 k)/100 k = 4.995 V and Cfb = 1/(2 x π x 455 k x 10 k) = 34.98 pF.



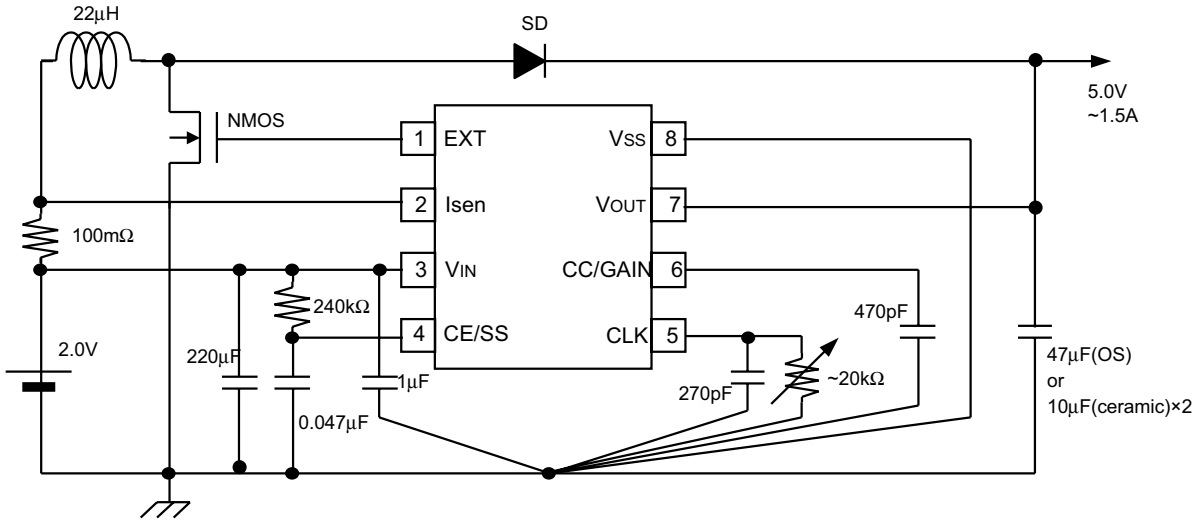
■ Typical Application Circuits

XC9101C33AKR



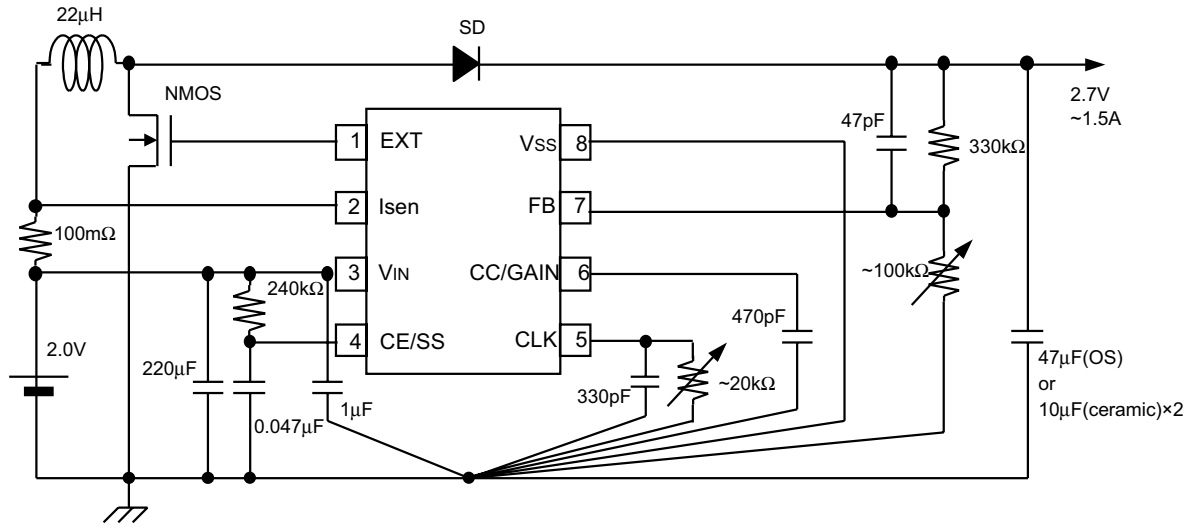
PMOS : XP161A1355PR (TOREX)
Coil : 22µH (CDRH127 SUMIDA)
Resistor : 100mΩ for Isen (NPR1 KOWA), 20kΩ (trimmer) for CLK, 240kΩ for SS
Capacitors : 270pF (ceramic) for CLK, 470pF (ceramic) for CC/GAIN, 0.047µF (any) for SS, 1µF (ceramic) for Bypass
47µF (OS) or 10µF (ceramic) × 2 for CL
SD : U3FWJ44N (TOSHIBA)

XC9101C50AKR



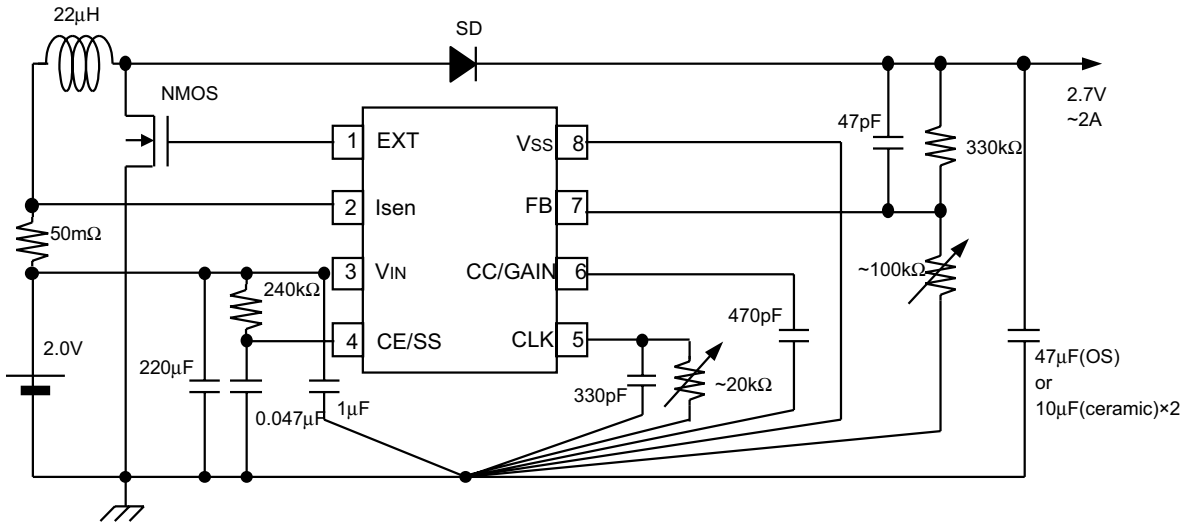
PMOS : XP161A1355PR (TOREX)
Coil : 22µH (CDRH127 SUMIDA)
Resistor : 100mΩ for Isen (NPR1 KOWA), 20kΩ (trimmer) for CLK, 240kΩ for SS
Capacitors : 270pF (ceramic) for CLK, 470pF (ceramic) for CC/GAIN, 0.047µF (any) for SS, 1µF (ceramic) for Bypass
47µF (OS) or 10µF (ceramic) × 2 for CL
SD : U3FWJ44N (TOSHIBA)

XC9101D09AKR



PMOS : XP161A1355PR (TOREX)
Coil : 22µH (CDRH127 SUMIDA)
Resistors : 100mΩ for Isen (NPR1 KOWA), 20kΩ (trimmer) for CLK, 240kΩ for SS, 330kΩ for Output Voltage,
100kΩ (trimmer) for Output Voltage
Capacitors : 330pF (ceramic) for CLK, 470pF (ceramic) for CC/GAIN, 0.047µF (any) for SS, 1µF (ceramic) for Bypass
47pF (ceramic) for FB, 47µF (OS) or 10mF (ceramic) × 2 for CL
SD : U3FWJ44N (TOSHIBA)

XC9101D09AKR



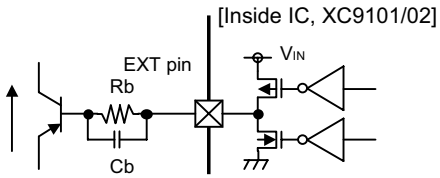
PMOS : XP161A1355PR (TOREX)
Coil : 22µH (CDRH127 SUMIDA)
Resistors : 50mΩ for Isen (NPR1 KOWA), 20kΩ (trimmer) for CLK, 240kΩ for SS, 330kΩ for Output Voltage,
100kΩ (trimmer) for Output Voltage
Capacitors : 330pF (ceramic) for CLK, 470pF (ceramic) for CC/GAIN, 0.047µF (any) for SS, 1µF (ceramic) for Bypass
47pF (ceramic) for FB, 47µF (OS) or 10µF (ceramic) × 2 for CL
SD : U3FWJ44N (TOSHIBA)

■ Notes on Use

1. The XC9101/9102 series are designed for use with a ceramic capacitor as output capacitor. If, however, the potential difference between input and output is too large, a ceramic capacitor may fail to absorb the resulting high switching energy. Then the output may present unusual oscillations. If the input-output potential difference is large, connect an electrolytic capacitor in parallel to compensate for insufficient capacitance.

2. The EXT pin of an IC of the XC9101/9102 series is designed to minimize the through current that occurs in the internal circuitry. However, the gate drive of external PMOS has a low impedance for the sake of speed. Therefore, if the input voltage is high and the bypass capacitor is attached away from the IC, the charge/discharge current to the external PMOS may cause unstable operation due to switching operation of the EXT pin.
   As a solution to this problem, place the bypass capacitor as close to the IC as possible, so that voltage variations at the V_{IN} and VSS pins caused by switching are minimized. If this is not effective, insert a resistor of several to several tens of ohms between the EXT pin and PMOS gate. Remember that the insertion of a resistor slows down the switching speed and may result in reduced efficiency.

3. A PNP transistor can be used in place of PMOS. In this case, insert a resistor (Rb) and capacitor (Cb) between the EXT pin and the base of the PNP transistor in order to limit the base current without slowing the switching speed. Adjust Rb in a range of 500 Ω to 1 kΩ according to the load and hFE of the transistor. Use a ceramic capacitor as Cb, complying with $Cb \leq 1/(2 \times \pi \times Rb \times Fosc \times 0.7)$, as a rule.



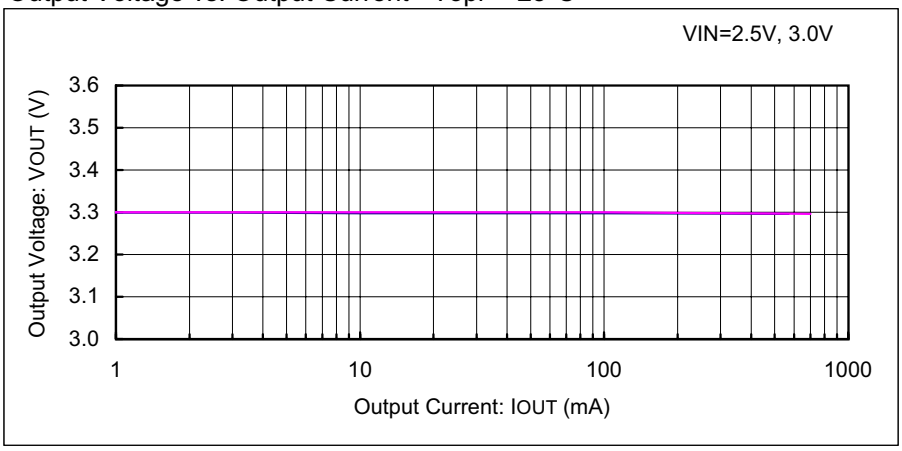
■ N. B.

Ensure that the absolute maximum ratings of external components and the XC9101/9102 series are not exceeded. The characteristics of a DC/DC converter depend largely on external components as well as on the characteristics of the XC9101/9102 series. Refer to the specifications of each component and take sufficient care when selecting components.
Place external components in the proximity of the IC. Use thick and short connecting wires to reduce wiring impedance. In particular, minimize the distance between the bypass capacitor and the IC.

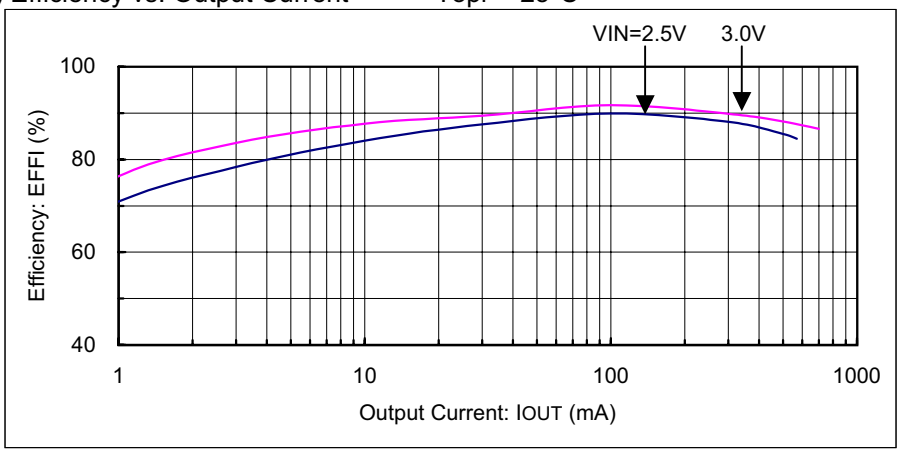
Wire the IC to ground sufficiently. Variations in ground potential caused by ground current at the time of switching may result in unstable operation of the IC. Specifically, provide sufficient ground wiring in the proximity of the Vss pin.

■ XC9101C33A 180kHz

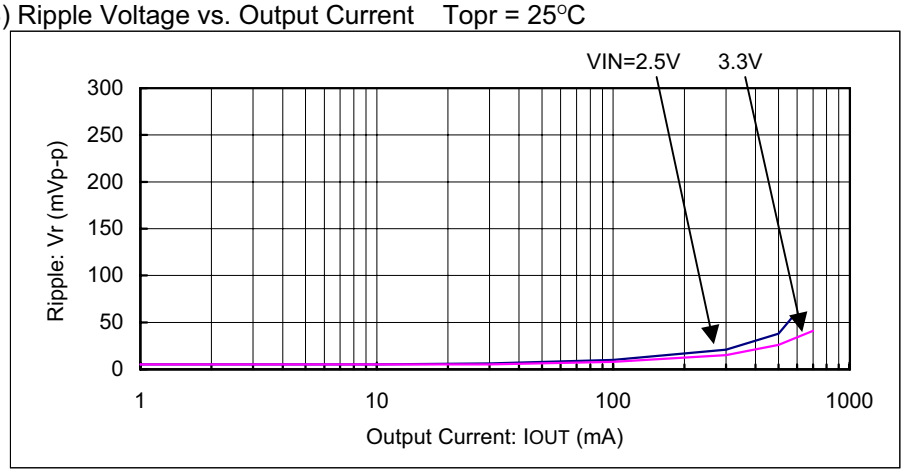
(1) Output Voltage vs. Output Current Topr = 25°C



(2) Efficiency vs. Output Current Topr = 25°C



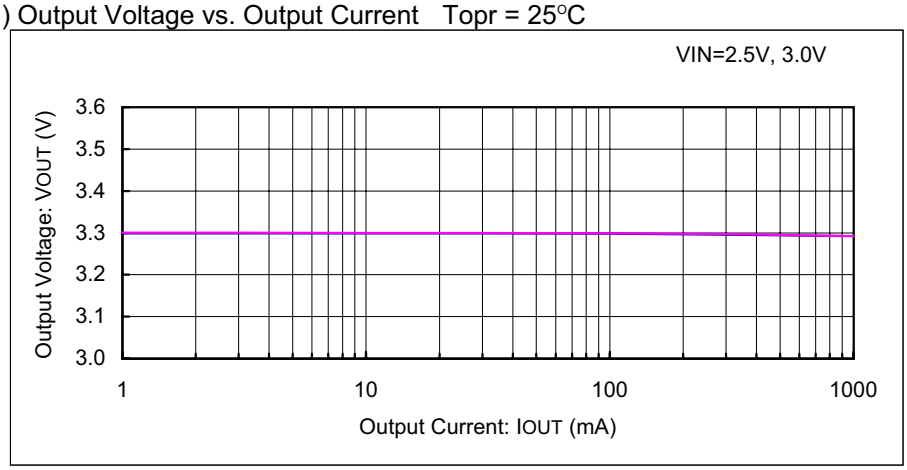
(3) Ripple Voltage vs. Output Current Topr = 25°C



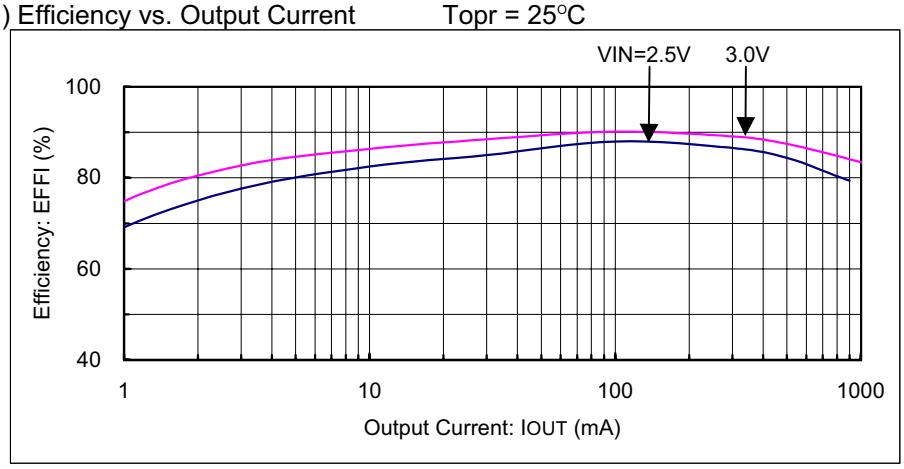
Tr: XP161A1355PR	(TOREX)	Rsen: 0.1Ω	
SD: U3FWJ44N	(TOSHIBA)	CDD: 1μF	(Ceramic Capacitor)
CIN: 220μF	(Aluminium electrolyic Capacitor)	CC/GAIN: 330pF	(Ceramic Capacitor)
CL: 10μF × 4	(Ceramic Capacitor)	CLK: 220pF+20kΩ	(Ceramic Capacitor + Resistor)
L: 22μH	(Sumida: CDRH127)		
CE/SS: 0.047μF+240kΩ	(Ceramic Capacitor + Resistor)		

■ XC9101C33A 330kHz

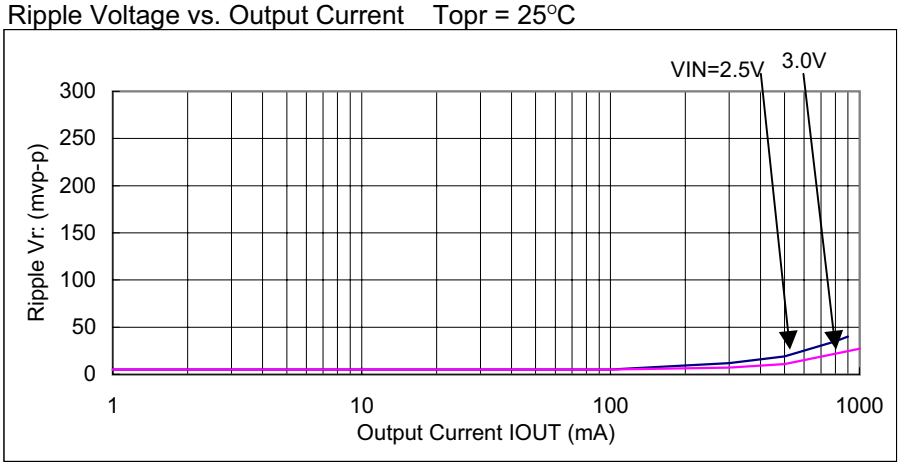
(1) Output Voltage vs. Output Current Topr = 25°C



(2) Efficiency vs. Output Current Topr = 25°C



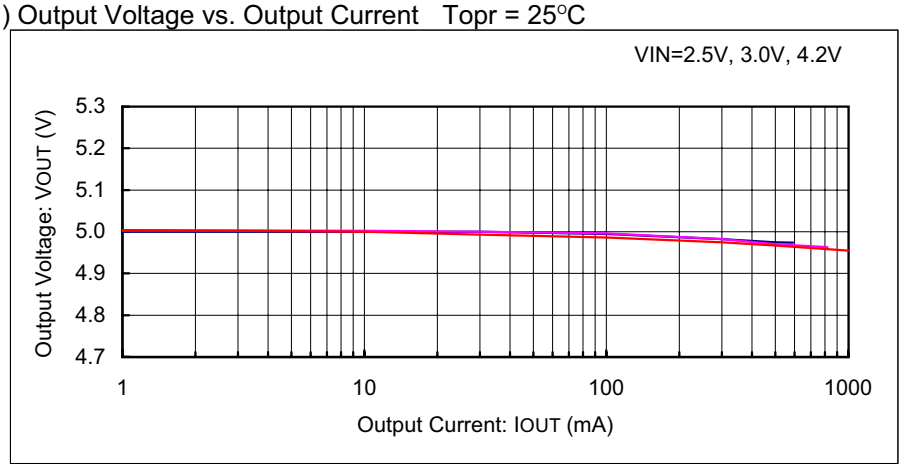
(3) Ripple Voltage vs. Output Current Topr = 25°C



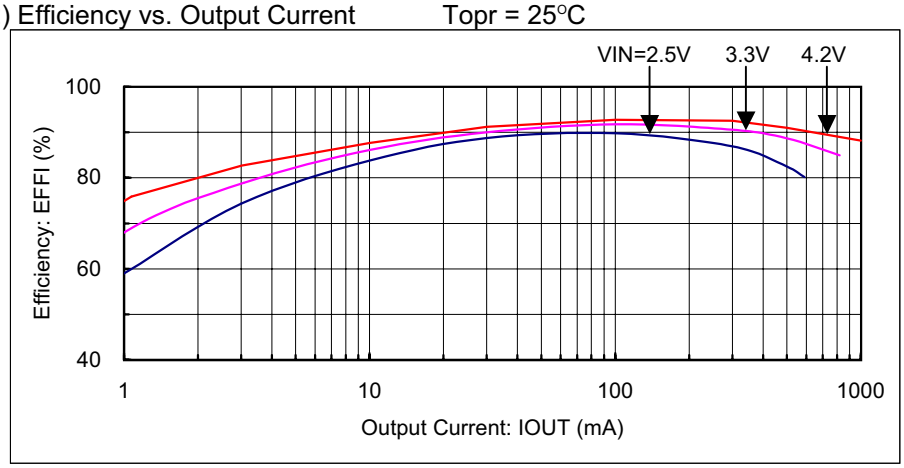
Tr: XP161A1355PR	(TOREX)	Rsen: 0.1Ω	
SD: U3FWJ44N	(TOSHIBA)	CDD: 1μF	(Ceramic Capacitor)
CIN: 220μF	(Aluminium electrolyic Capacitor)	CC/GAIN: 330pF	(Ceramic Capacitor)
CL: 10μF × 4	(Ceramic Capacitor)	CLK: 220pF+10kΩ	(Ceramic Capacitor + Resistor)
L: 10μH	(Sumida: CDRH127)		
CE/SS: 0.047μF+240kΩ	(Ceramic Capacitor + Resistor)		

■ XC9101C50A 180kHz

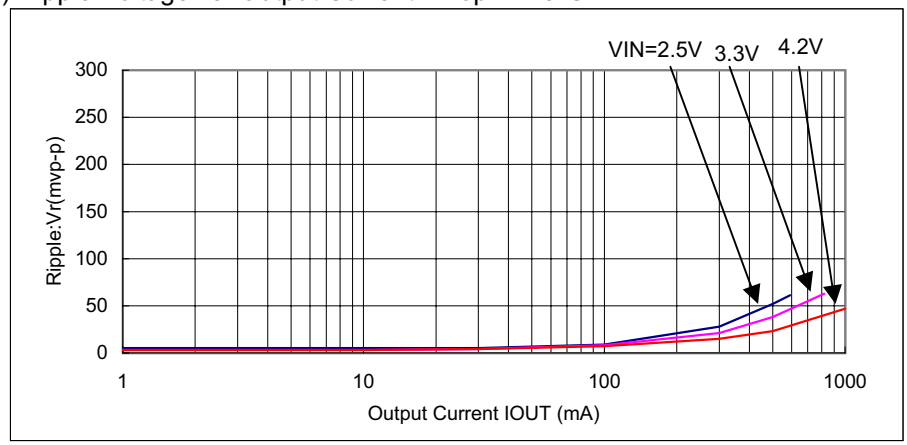
(1) Output Voltage vs. Output Current Topr = 25°C



(2) Efficiency vs. Output Current Topr = 25°C



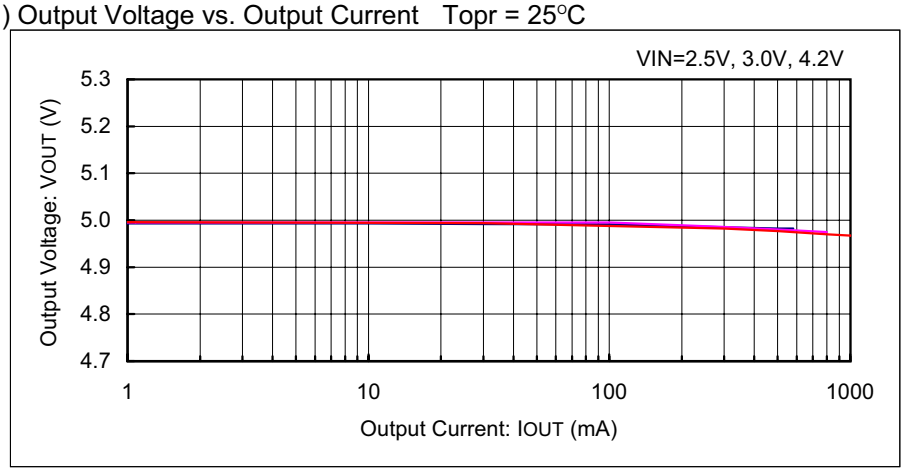
(3) Ripple Voltage vs. Output Current Topr = 25°C



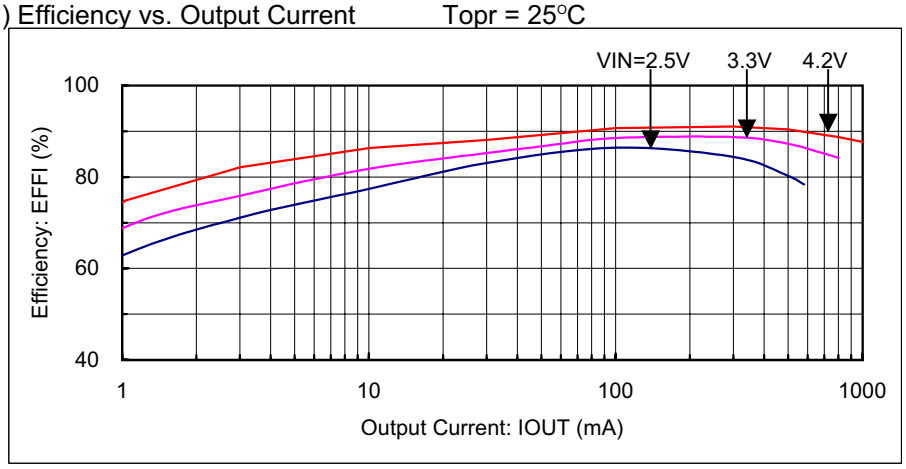
Tr: XP161A1355PR	(TOREX)	Rsen: 0.1Ω	
SD: U3FWJ44N	(TOSHIBA)	CDD: 1μF	(Ceramic Capacitor)
CIN: 220μF	(Aluminium electrolyic Capacitor)	CC/GAIN: 330pF	(Ceramic Capacitor)
CL: 10μF × 4	(Ceramic Capacitor)	CLK: 220pF+20kΩ	(Ceramic Capacitor + Resistor)
L: 22μH	(Sumida: CDRH127)		
CE/SS: 0.047μF+240kΩ	(Ceramic Capacitor + Resistor)		

■ XC9101C50A 330kHz

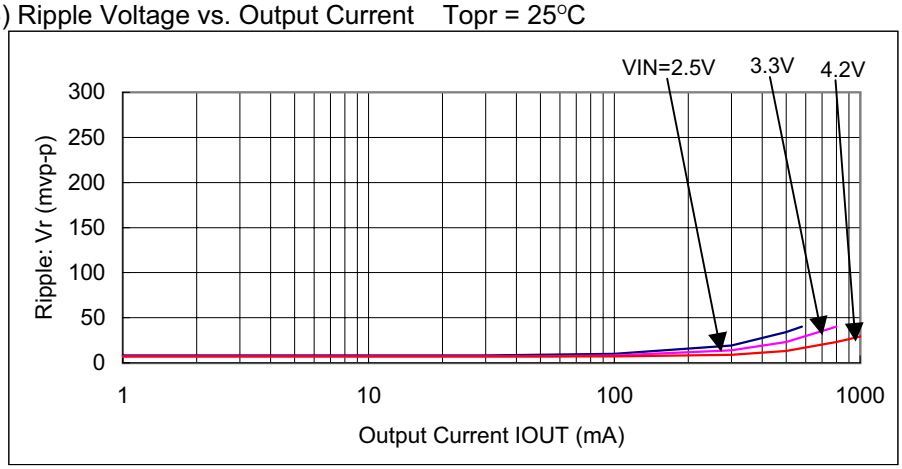
(1) Output Voltage vs. Output Current Topr = 25°C



(2) Efficiency vs. Output Current Topr = 25°C

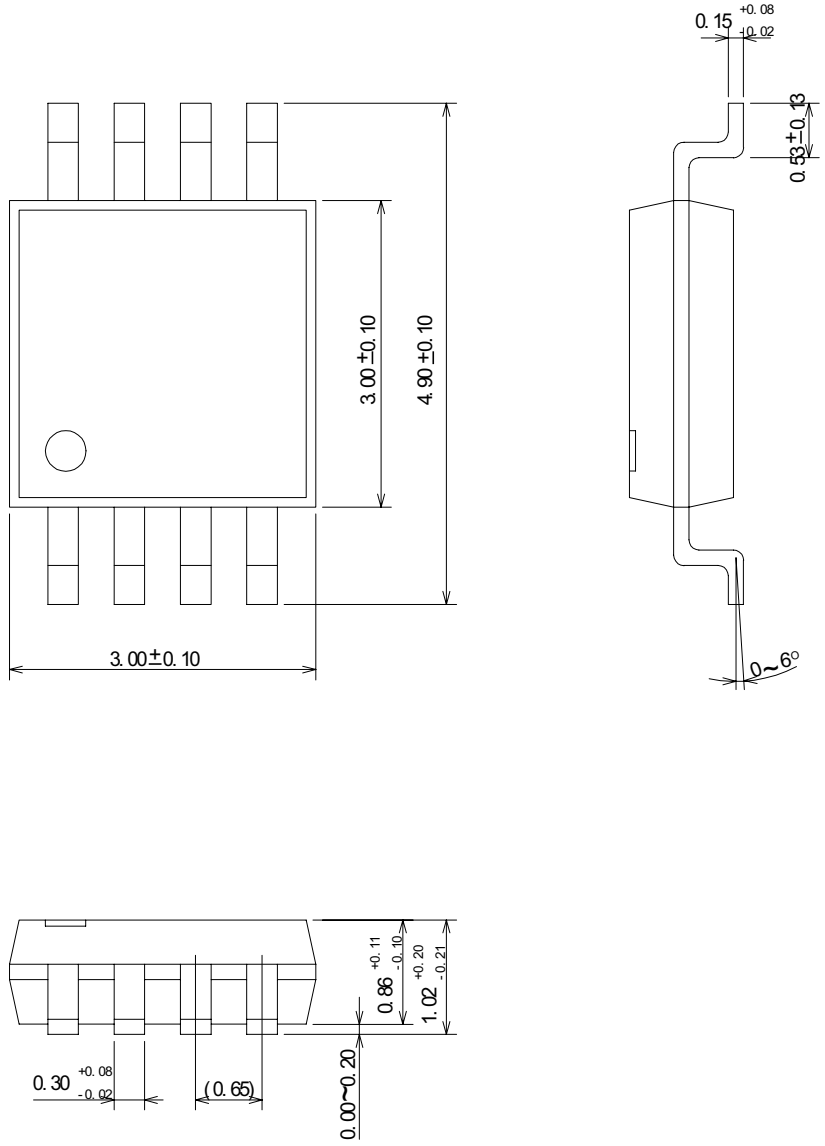


(3) Ripple Voltage vs. Output Current Topr = 25°C



Tr: XP161A1355PR	(TOREX)	Rsen: 0.1Ω	
SD: U3FWJ44N	(TOSHIBA)	CDD: 1μF	(Ceramic Capacitor)
CIN: 220μF	(Aluminium electrolyic Capacitor)	CC/GAIN: 330pF	(Ceramic Capacitor)
CL: 10μF × 4	(Ceramic Capacitor)	CLK: 220pF+10kΩ	(Ceramic Capacitor + Resistor)
L: 10μH	(Sumida: CDRH127)		
CE/SS: 0.047μF+240kΩ	(Ceramic Capacitor + Resistor)		

■ Packaging Information (Dimensions : mm)
MSOP-8A : 1,000pcs. / reel



■ Recommended Pattern Layout (Dimensions : mm)