# RC288DPi/VFC, RC240DPi/VFC, and RC192DPi/VFC V.Fast Class™ (V.FC™) Data/V.17 Fax Modem Data Pump

## INTRODUCTION

The Rockwell RC288DPi/VFC, RC240DPi/VFC, and RC192DPi/VFC are V.Fast Class™ (V.FC™) modem data pump families that support data rates up to 28800 bps, 24000 bps, or 19200 bps, respectively, and fax operation up to 14400 bps. The following models are available to support specific requirements:

| Model | Data | Fax |
|---|---|---|
| RC288DPi/VFC | 28.8 kbps | 14.4 kbps |
| RC288DPi-D/VFC | 28.8 kbps | None |
| RC240DPi/VFC | 24.0 kbps | 14.4 kbps |
| RC240DPi-D/VFC | 24.0 kbps | None |
| RC192DPi/VFC | 19.2 kbps | 14.4 kbps |
| RC192DPi-D/VFC | 19.2 kbps | None |

As a data modem, the modem can operate in 2-wire, full-duplex, synchronous/asynchronous modes at rates up to 28800 bps. Using a V.FC scheme to optimize modem configuration for line conditions, the modem can connect at the highest data rate that the channel can support from 28800 bps to 14400 bps with automatic fallback to V.32 bis. Automode operation in V.32 bis is provided in accordance with EIA/TIA-PN2330.

Internal HDLC support eliminates the need for an external serial input/output (SIO) device in the DTE for products incorporating error correction and T.30 protocols.

The V.FC modems fully support Group 3 facsimile send and receive speeds of 14400, 12000, 9600, 7200, 4800, and 2400 bps.

The modem operates over the public switched telephone network (PSTN) through the appropriate line termination.

The modem is packaged in a single 68-pin plastic leaded chip carrier (PLCC).

Additional information is provided in the RC288DPi/VFC, RC240DPi/VFC and RC192DPi/VFC Modem Designer's Guide (Order No. 898).



## FEATURES

- 2-wire full-duplex
  - —V.Fast Class (V.FC), V.32 bis, V.32, V.22 bis, V.22, V.23, and V.21
  - —Bell 212 and 103
- 2-wire half-duplex
  - —V.17, V.33, V.29, V.27 ter, V.26 bis, V.26 Alternative A, and V.21 channel 2
  - —Bell 208
  - —Short train option in V.17 and V.27 ter
- Serial synchronous and asynchronous data
- Parallel synchronous and asynchronous data
- Parallel synchronous SDLC/HDLC support
- In-band secondary channel
- Automatic mode selection (AMS)
- Automatic rate adaption (ARA)
- Digital near-end and far-end echo cancellation
- Bulk delay for satellite transmission
- Auto-dial and auto-answer
- TTL and CMOS compatible DTE interface
  - —CCITT V.24 (EIA/TIA-232-E) (data/control)
  - —Microprocessor bus (data/configuration/control)
- Dynamic range: –43 dBm to –9 dBm
- Adjustable speaker output to monitor received signal
- DMA support interrupt lines
- Two 16-byte FIFO data buffers for burst data transfer
- NRZI encoding/decoding
- 511 pattern generation/detection
- Diagnostic capability
- V.13 signalling
- V.54 inter-DCE signalling
- V.54 local analog and remote digital loopback
- +5V operation
- Typical power consumption:
  - —Normal mode: 900 mW
  - —Sleep mode: 10 mW
- 68-pin PLCC package

**Data Sheet**
**(Preliminary)**

**Order No. MD96**
**Rev. 1, October 15, 1993**
**(Supersedes earlier issues)**

## TECHNICAL SPECIFICATIONS

### Configurations and Rates

The selectable modem configurations, signaling rates, and data rates are listed in Table 1.

### Automatic Mode Selection (AMS)

When automatic mode selection (AMS) is enabled by the AUTO bit, the modem configures itself to the highest compatible data rate supported by the remote modem. Automode operation in V.32 bis, V.32 V.22 bis, V.22, V.21, V.23, Bell 212A, and Bell 103 modes is in accordance with EIA/TIA-PN2330.

**NOTE:** Bit names refer to data, control, and/or status bits in the modem interface memory (see Table 10).

### Automatic Rate Adaption (ARA)

In V.FC mode, automatic rate adaption (ARA) can be enabled by the EARC bit to select the highest data rate possible based on the measured eye quality monitor (EQM). This selection occurs during handshake/retrain and rate renegotiation.

### Tone Generation

The modem can generate single or dual voice-band tones from 0 Hz to 3600 Hz with a resolution of 0.15 Hz and an accuracy of ±0.01%. Tones over 3000 Hz are attenuated. DTMF tone generation allows the modem to operate as a programmable DTMF dialer.

### Data Encoding

The data encoding implements a V.FC scheme; conforms to CCITT recommendation V.32 bis, V.32, V.17, V.33, V.29, V.27 ter, V.26 bis, V.26 Alternative A, V.22 bis, V.22, V.23, or V.21; or is compatible with Bell 208, 212A, or 103; depending on the configuration.

### Transmitted Data Spectrum

The transmitter spectrum is shaped by raised cosine filter functions as follows:

| Configuration | Raised Cosine Filter Function |
|---|---|
| V.FC, V.32 bis, V.32, V.17, V.33, V.29 | Square root of 12.5% |
| V.27 ter, V.26, Bell 208 | Square root of 50% |
| V.22 bis/V.22, Bell 212A | Square root of 75% |

### RTS – CTS Response Time

The response times of CTS relative to a corresponding transition of RTS are listed in Table 2.

### Transmit Level

The transmitter output level is selectable from 0 dBm to –15 dBm in 1 dB steps and is accurate to ±0.5 dB when used with an external hybrid. The output level can also be fine tuned by changing a gain constant in RAM. The maximum V.FC/V.32 bis/V.32 transmit level for acceptable receive performance should not exceed –9 dBm.

**Note:** In V.FC mode, the transmit level may be automatically changed during the V.FC handshake. This automatic adjustment of the transmit level may be disabled via a parameter in DSP RAM.

### Transmitter Timing

Transmitter timing is selectable between internal (±0.01%), external, or slave.

### Scrambler/Descrambler

A self-synchronizing scrambler/descrambler is used in accordance with the selected configuration.

### Answer Tone

The modem generates a 2100 Hz answer tone for 3.6 seconds at the beginning of the answer handshake when the NV25 bit is a zero (V.FC, V.32 bis, V.32, V.22 bis, V.22, V.23, and V.21). The answer tone has 180° phase reversals every 0.45 second to disable network echo cancellers (V.FC, V.32 bis, V.32).

### Receive Level

The modem satisfies performance requirements for received line signal levels from –9 dBm to –43 dBm measured at the Receiver Analog (RXA) input.

**Note:** A 6 dB pad is required between TIP and RING and the RIN input.

### Receiver Timing

The timing recovery circuit can track a frequency error in the associated transmit timing source of ±0.035% (V.22 bis) or ±0.01% (other configurations).

### Carrier Recovery

The carrier recovery circuit can track a ±7 Hz frequency offset in the received carrier with less than a 0.2 dB degradation in bit error rate (BER).

### Clamping

Received Data (RXD) is clamped to a constant mark whenever the Received Line Signal Detector ($\overline{\text{RLSD}}$) is off. $\overline{\text{RLSD}}$ can be clamped off (RLSDE bit).

### Echo Canceller

A data echo canceller with near-end and far-end echo cancellation is included for 2-wire full-duplex V.FC/V.32 bis/V.32 operation. The combined echo span of near and far cancellers can be up to 40 ms. The proportion allotted to each end is automatically determined by the modem. The delay between near-end and far-end echoes can be up to 1.2 seconds. The canceller can compensate for ± 7 Hz frequency offset in the far-end echo.

### Voice Pass-Through Mode

**Transmit Voice.** 16-bit transmit voice samples can be sent to the modem DAC from the host.

**Receive Voice.** 16-bit received voice samples from the modem ADC can be read by the host.

**Table 1. Configurations, Signaling Rates and Data Rates**

| Configuration | Modulation[1] | Carrier Frequency (Hz) ±0.01% | Data Rate (bps) ±0.01% | Symbol Rate (Symbols/Sec.) | Bits per Symbol | | Constellation Points |
|---|---|---|---|---|---|---|---|
| | | | | | Data | TCM | |
| V.FC 28800 TCM[3] | TCM | Note 2 | 28800 | Note 2 | Note 2 | Note 2 | Note 2 |
| V.FC 26400 TCM[3] | TCM | Note 2 | 26400 | Note 2 | Note 2 | Note 2 | Note 2 |
| V.FC 24000 TCM[3,4] | TCM | Note 2 | 24000 | Note 2 | Note 2 | Note 2 | Note 2 |
| V.FC 21600 TCM[3,4] | TCM | Note 2 | 21600 | Note 2 | Note 2 | Note 2 | Note 2 |
| V.FC 19200 TCM | TCM | Note 2 | 19200 | Note 2 | Note 2 | Note 2 | Note 2 |
| V.FC 16800 TCM | TCM | Note 2 | 16800 | Note 2 | Note 2 | Note 2 | Note 2 |
| V.FC 14400 TCM | TCM | Note 2 | 14400 | Note 2 | Note 2 | Note 2 | Note 2 |
| V.32 bis 14400 TCM | TCM | 1800 | 14400 | 2400 | 6 | 1 | 128 |
| V.32 bis 12000 TCM | TCM | 1800 | 12000 | 2400 | 5 | 1 | 64 |
| V.32 bis 9600 TCM | TCM | 1800 | 9600 | 2400 | 4 | 1 | 32 |
| V.32 bis 7200 TCM | TCM | 1800 | 7200 | 2400 | 3 | 1 | 16 |
| V.32 bis 4800 | QAM | 1800 | 4800 | 2400 | 2 | 0 | 4 |
| V.32 9600 TCM | TCM | 1800 | 9600 | 2400 | 4 | 1 | 32 |
| V.32 9600 | QAM | 1800 | 9600 | 2400 | 4 | 0 | 16 |
| V.32 4800 | QAM | 1800 | 4800 | 2400 | 2 | 0 | 4 |
| V.26 bis 2400 | DPSK | 1800 | 2400 | 1200 | 2 | 0 | 4 |
| V.26 bis 1200 | DPSK | 1800 | 1200 | 1200 | 1 | 0 | 4 |
| V.26 A 2400 | DPSK | 1800 | 2400 | 1200 | 2 | 0 | 4 |
| V.22 bis 2400 | QAM | 1200/2400 | 2400 | 600 | 4 | 0 | 16 |
| V.22 bis 1200 | DPSK | 1200/2400 | 1200 | 600 | 2 | 0 | 4 |
| V.22 1200 | DPSK | 1200/2400 | 1200 | 600 | 2 | 0 | 4 |
| V.22 600 | DPSK | 1200/2400 | 600 | 600 | 1 | 0 | 4 |
| V.23 1200/75 | FSK | 1700/420 | 1200/75 | 1200 | 1 | 0 | – |
| V.21 | FSK | 1080/1750 | 0–300 | 300 | 1 | 0 | – |
| Bell 208 4800 | DPSK | 1800 | 4800 | 1600 | 3 | 0 | 8 |
| Bell 212A | DPSK | 1200/2400 | 1200 | 600 | 2 | 0 | 4 |
| Bell 103 | FSK | 1170/2125 | 0–300 | 300 | 1 | 0 | – |
| V.23 1200/75 | FSK | 1700/420 | 1200/75 | 1200 | 1 | 0 | – |
| V.21 | FSK | 1080/1750 | 0–300 | 300 | 1 | 0 | – |
| V.17 14400 TCM/V.33[5] | TCM | 1700 or 1800 | 14400 | 2400 | 6 | 1 | 128 |
| V.17 12000 TCM/V.33[5] | TCM | 1700 or 1800 | 12000 | 2400 | 5 | 1 | 64 |
| V.17 9600 TCM[5] | TCM | 1700 or 1800 | 9600 | 2400 | 4 | 1 | 32 |
| V.17 7200 TCM[5] | TCM | 1700 or 1800 | 7200 | 2400 | 3 | 1 | 16 |
| V.29 9600[5] | QAM | 1700 | 9600 | 2400 | 4 | 0 | 16 |
| V.29 7200[5] | QAM | 1700 | 7200 | 2400 | 3 | 0 | 8 |
| V.29 4800[5] | QAM | 1700 | 4800 | 2400 | 2 | 0 | 4 |
| V.27 4800[5] | DPSK | 1800 | 4800 | 1600 | 3 | 0 | 8 |
| V.27 2400[5] | DPSK | 1800 | 2400 | 1200 | 2 | 0 | 4 |
| V.21 Channel 2[5] | FSK | 1750 | 300 | 300 | 1 | 0 | – |
| Tone Transmit | – | – | – | – | – | – | – |

**Notes:**

1. Modulation legend: TCM: Trellis-Coded Modulation; QAM: Quadrature Amplitude Modulation; FSK: Frequency Shift Keying; DPSK: Differential Phase Shift Keying

2. Adaptive; established during handshake:

| Symbol Rate (Baud) | Default Carrier Rate (Hz) |
|---|---|
| 2400 | 1800 |
| 2800 | 1866.67 |
| 3000 | 1875 |
| 3200 | 1920 |
| 3429 | 1959.18 |

3. RC288DPi/VFC and RC288DPi-D/VFC.
4. RC240DPi/VFC and RC240DPi-D/VFC.
5. Models with fax support only.

### Data Formats

***Serial Synchronous Data***

Data rate: 28800[1], 26400[1], 24000[1,2], 21600[1,2], 19200, 16800, 14400, 12000, 9600, 7200, 4800, 2400, 1200, 600, or 300 bps ±0.01%.

Selectable clock: Internal, external, or slave.

***Serial Asynchronous Data***

Data rate: 28800[1], 26400[1], 24000[1,2], 21600[1,2], 19200, 16800, 14400, 12000, 9600, 7200, 4800, 2400, 1200 or 600 bps +1% (or +2.3%), –2.5%;

0-300 bps (V.21 and Bell 103);

1200/75 bps (V.23).

Bits per character: 7, 8, 9, 10, or 11.

***Parallel Synchronous Data***

Normal sync: 8-bit data for transmit and receive

Data rate: 28800[1], 26400[1], 24000[1,2], 21600[1,2], 19200, 16800, 14400, 12000, 9600, 7200, 4800, 2400, 1200, 600, or 300 bps ±0.01%.

SDLC/HDLC support:

Transmitter: Flag generation, 0 bit stuffing, CCITT CRC-16 or CRC-32 generation.

Receiver: Flag detection, 0 bit deletion, CCITT CRC-16 or CRC-32 checking.

***Parallel Asynchronous Data***

Data rate: 28800[1], 26400[1], 24000[1,2], 21600[1,2], 19200, 16800, 14400, 12000, 9600, 7200, 4800, 2400, 1200 or 600 bps +1% (or 2.3%), –2.5%;

1200, 300, or 75 bps (FSK).

Data bits per character: 5, 6, 7, or 8.

Parity generation/checking: Odd, even, or 9th data bit.

***Notes:***

1. RC288DPi/VFC and RC288DP-D/VFC.
2. RC240DPi/VFC and RC240DP-D/VFC.

### Async/Sync and Sync/Async Conversion

An asynchronous-to-synchronous converter is provided in the transmitter and a synchronous-to-asynchronous converter is provided in the receiver. The converters operate in both serial and parallel modes. The asynchronous character format is 1 start bit, 5 to 8 data bits, an optional parity bit, and 1 or 2 stop bits. Valid character size, including all bits, is 7, 8, 9, 10, or 11 bits per character. Two ranges of signaling rates are provided:

- Basic range: +1% to –2.5%
- Extended overspeed range: +2.3% to –2.5%

When the transmitter's converter is operating at the basic signaling rate, no more than one stop bit will be deleted per 8 consecutive characters. When operating at the extended rate, no more than one stop bit will be deleted per 4 consecutive characters. Break handling is performed as described in V.14.

Asynchronous characters are accepted on the TXD serial input and are issued on the RXD serial output.

### V.54 Inter-DCE Signalling

The modem supports V.54 inter-DCE signalling procedures in synchronous and asynchronous configurations. Transmission and detection of the preparatory, acknowledgment, and termination phases as defined in V.54 are provided. Three control bits in the transmitter allow the host to send the appropriate bit patterns (V54T, V54A, and V54P bits). Three control bits in the receiver are used to enable one of three bit pattern detectors (V54TE, V54AE, and V54PE bits). A status bit indicates when the selected pattern detector has found the corresponding bit pattern (V54DT bit).

### V.13 Remote RTS Signalling

The modem supports V.13 remote RTS signalling. Transmission and detection of signalling bit patterns in response to a change of state in the RTS bit or the RTS input signal are provided. The RRTSE bit enables V.13 signalling. The RTSDE bit enables detection of V.13 patterns. The RTSDT status bit indicates the state of the remote RTS signal. This feature may be used to clamp/unclamp the local RLSD and RXD signals in response to a change in the remote RTS signal in order to simulate controlled carrier operation in a constant carrier environment. The modem automatically clamps and unclamps RLSD.

**Table 2. RTS-CTS Response Time**

| Configuration | RTS-CTS Response[1] | | Turn-Off Sequence[3] |
|---|---|---|---|
| | Constant Carrier | Controlled Carrier | |
| V.FC, V.32 bis, V.32 | ≤ 2 ms | N/A | N/A |
| V.33/V.17 Long | N/A | 1393 ms[2] | 15 ms[4] |
| V.33/V.17 Short | N/A | 142 ms[2] | 15 ms[4] |
| V.29 | N/A | 253 ms[2] | 12 ms |
| V.27 4800 Long | N/A | 708 ms[2] | 7 ms[4] |
| V.27 4800 Short | N/A | 50 ms[2] | 7 ms[4] |
| V.27 2400 Long | N/A | 943 ms[2] | 10 ms[4] |
| V.27 2400 Short | N/A | 67 ms[2] | 10 ms[4] |
| V.26 | N/A | 60 ms | 10 ms |
| V.22 bis, V.22, Bell 212A | ≤ 2 ms | 270 ms | N/A |
| V.21 | 500 ms | 500 ms | N/A |
| V.23, Bell 103 | 210 ms | 210 ms | N/A |

**Notes:**

1. Times listed are CTS turn-on. The CTS OFF-to-ON response time is host programmable in DSP RAM.
2. Add echo protector tone duration plus 20 ms when echo protector tone is used during turn-on.
3. Turn-off sequence consists of transmission of remaining data and scrambled ones for controlled carrier operation. CTS turn-off is less than 2 ms for all configurations.
4. Plus 20 ms of no transmitted energy.
5. N/A = not applicable.

### Auto-Dialing and Auto-Answering Control

The host can perform auto-dialing and auto-answering. These functions include DTMF or pulse dialing, ringing detection, and a comprehensive supervisory tone detection scheme. The major parameters are host programmable.

### Supervisory Tone Detection

Three parallel tone detectors (A, B, and C) are provided for supervisory tone detection. The signal path to these detectors is separate from the main received signal path. Therefore, the tone detect signal does not pass through the highpass section of the analog receive bandpass filter, enabling the tone detection to be largely independent of the receiver status.

The tone detection bandwidth depends on the configuration:

| Receiver Configuration | Detection Bandwidth |
|---|---|
| V.FC, V.32 bis, V.32, V.17, V.29, V.27 ter, V.26, V.23, Bell 208 | 0–3400 Hz |
| V.22 bis, V.22, Bell 212A, Bell 103 Originate | 0–2800 Hz |
| V.22 bis, V.22, Bell 212A, Bell 103 Answer | 0–1700 Hz |
| V.21 Originate | 0–2200 Hz |
| V.21 Answer | 0–1300 Hz |

Each tone detector consists of two cascaded second order IIR biquad filters. The coefficients are host programmable. Each fourth order filter is followed by a level detector which has host programmable turn-on and turn-off thresholds allowing hysteresis. Tone detector C is preceded by a prefilter and squarer. This circuit is useful for detecting a tone with frequency equal to the difference between two tones that may be simultaneously present on the line. The squarer may be disabled by the SQDIS bit causing tone detector C to be an eighth order filter. The tone detectors are disabled in data mode.

The tone detection sample rate is 9600 Hz in V.FC mode and 7200 Hz in non-V.FC modes. The default call progress filter coeficients are based on a 7200 Hz sampling rate and apply to non-V.FC modes only.

### Supervisory Tone Detectors, Default Characteristics

The default bandwidths and thresholds of the tone detectors are as follows:

| Tone Detector | Bandwidth | Turn-On Threshold | Turn-Off Threshold |
|---|---|---|---|
| A | 245 – 650 Hz | –25 dBm | –31 dBm |
| B | 360 – 440 Hz | –25 dBm | –31 dBm |
| C Prefilter | 0 – 500 Hz | N/A | N/A |
| C | 50 – 110 Hz | * | * |

*Tone Detector C will detect a difference tone within its bandwidth when the two tones present are in the range –1 dBm to –26 dBm.

### 511 Pattern Generation/Detection

In a synchronous mode, a 511 pattern can be generated and detected (control bit S511). Use of this bit pattern during self-test eliminates the need for external test equipment.

### In-Band Secondary Channel

A full-duplex in-band secondary channel is provided in V.FC (19200 bps and above) and V.32 bis/V.32 (7200 bps and above) modes. Control bit SECEN enables and disables the secondary channel operation. The secondary channel operates in parallel data mode with independent transmit and receive interrupts and data buffers. The main channel may operate in parallel or serial mode. The secondary channel data rate is 200 bps in V.FC modes and 150 bps in V.32 bis/V.32 modes. The rate is host programmable when configured for V.32 bis/V.32 modes.

The secondary channel may also be used to perform rate changes in V.FC modes (control bit SRCEN).

### Transmit and Receive FIFO Data Buffers

Two 16-byte first-in first-out (FIFO) data buffers allow the DTE/host to rapidly output up to 16 bytes of transmit data and input up to 16 bytes of accumulated received data. The receiver FIFO is always enabled. The transmitter FIFO is enabled by the FIFOEN control bit. TXHF and RXHF bits indicate the corresponding FIFO buffer half full (4 or more bytes loaded) status. TXFNF and RXFNE bits indicate the TX FIFO buffer not full and RX FIFO buffer not empty status, respectively. An interrupt mask register allows an interrupt request to be generated whenever the TXFNF, RXFNE, RXHF, or TXHF status bit changes state.

### DMA Support Interrupt Request Lines

DMA support is available in synchronous, asynchronous, and HDLC parallel data modes. Control bit DMAE enables and disables DMA support. When DMA support is enabled, the modem $\overline{RI}$ and $\overline{DSR}$ lines are assigned to Transmitter Request (TXRQ) and Receiver Request (RXRQ) hardware output interrupt request lines, respectively. The TXRQ and RXRQ signals follow the assertion of the TDBE and RDBF interrupt bits thus allowing the DTE/host to respond immediately to the interrupt request without masking out status bits to determine the interrupt source.

### NRZI Encoding/Decoding

NRZI data encoding/decoding may be selected in synchronous and HDLC modes instead of the default NRZ (control bit NRZIEN). In NRZ encoding, a 1 is represented by a high level and a 0 is represented by a low level. In NRZI encoding, a 1 is represented by no change in level and a 0 is represented by a change in level.

### CCITT CRC-32 Support

CCITT CRC-32 generation/checking may be selected instead of the default CCITT CRC-16 in HDLC mode using DSP RAM access.

### Caller ID Demodulation

Caller ID information can be demodulated in V.23 1200 receive configuration and presented to the host/DTE in serial (TXD) and parallel (RBUFFER) form.

### Telephone Line Interface

**Line Transformer Interface:** V.FC/V.32 bis/V.32 places high requirements upon the DAA. V.FC uses the same bandwidth for transmission of data in both directions. Any non-linear distortion generated by the DAA in the transmit direction (known as near-end echo) cannot be canceled by the modem's echo canceller and interferes with data reception. The designer must, therefore, ensure that the total harmonic distortion due to near-end echo at the RXA input to the modem is at least 45 dB below the minimum level of received signal at the same point.

**Relay Control:** Direct control of the off-hook and talk/data relays is provided. Internal relay drivers allow direct connection to the off-hook and talk/data relays. The talk/data relay output can optionally be used for pulse dial.

### Speaker Interface

A SPKR output is provided with on/off and volume control logic incorporated in the modem, requiring only an external amplifier to drive a loudspeaker.

## HARDWARE INTERFACE SIGNALS

A functional interconnect diagram showing the typical modem connection in a system is illustrated in Figure 1.

In Figure 1, any point that is active low is represented by a small circle at the signal point.

Edge triggered inputs are denoted by a small triangle (e.g., TDCLK). Active low signals are overscored (e.g., RESET).

A clock intended to activate logic on its rising edge (low-to-high transition) is called active low (e.g., RDCLK), while a clock intended to activate logic on its falling edge (high-to-low transition) is called active high (e.g., TDCLK). When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

The pin assignments for the modem packaged in a single 68-pin PLCC are listed in Table 3 and are shown in Figure 2.

The modem hardware interface signals are described in Table 4.

The digital interface characteristics are defined in Table 5.

The analog interface characteristics are defined in Table 6.

The power requirements are defined in Table 7.

The absolute maximum ratings are defined in Table 8.

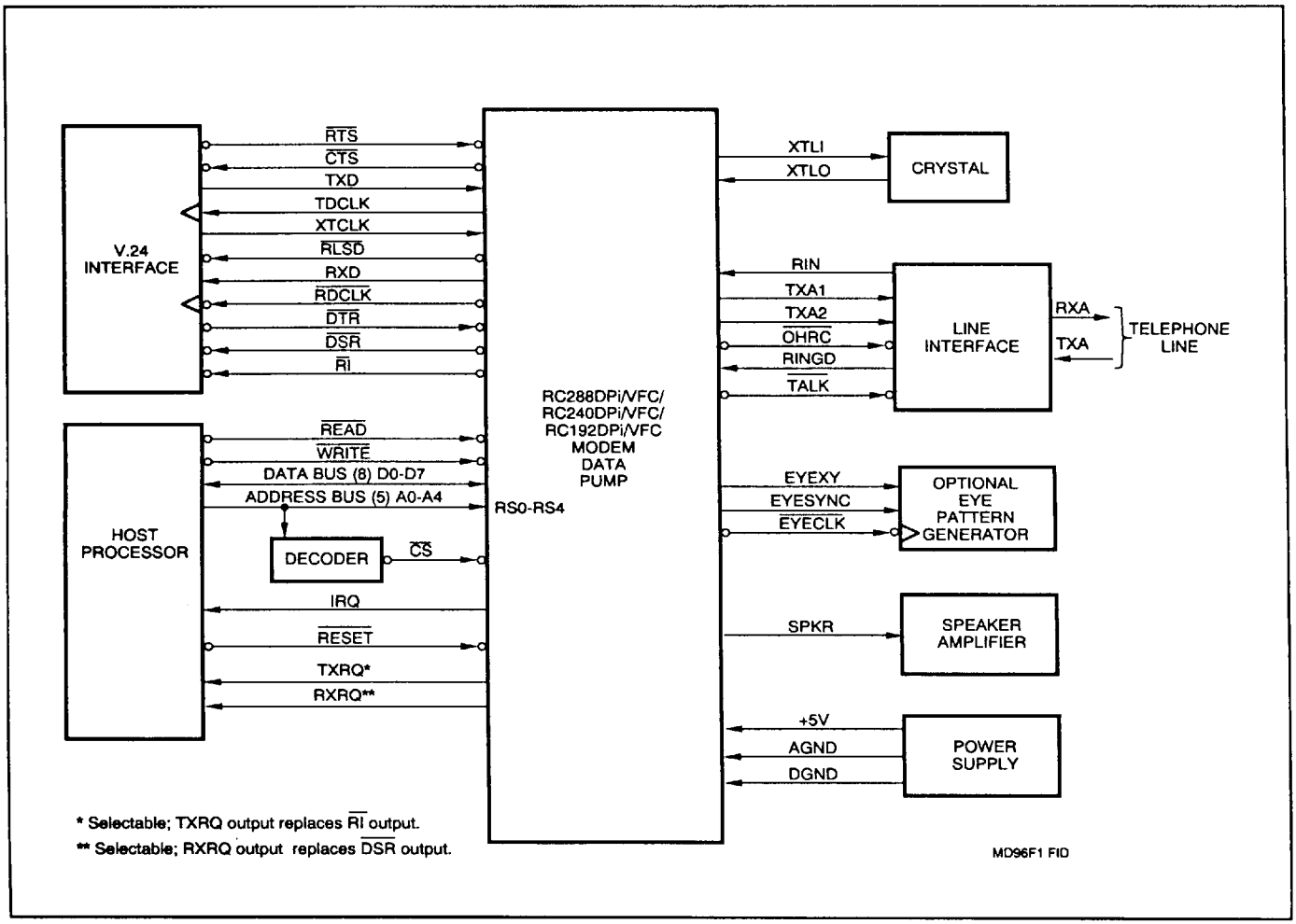


**Figure 1. Modem Functional Interconnect Diagram**

**Table 3. Modem Pin Assignments - 68-Pin PLCC**

| Pin | Signal Label | Type | Interface |
|---|---|---|---|
| 1 | VREG | MI | To GND through 0.1 μF[3] |
| 2 | DSP_RESET | MI | Output to RES |
| 3 | IA_CLKIN | MI | Output to CLKIN |
| 4 | DSP_IRQ | MI | Input from IRQ |
| 5 | RI/TXRQ | OA | DTE Serial/DMA Interface |
| 6 | RINGD | IA | Line Interface |
| 7 | RTS | IA | DTE Serial Interface |
| 8 | IRQ | OA | Host Parallel Interface |
| 9 | D1 | IA/OA | Host Parallel Interface |
| 10 | DGND1 | GND | |
| 11 | +5VD1 | PWR | |
| 12 | XTLI | I | Crystal/Clock Circuit |
| 13 | XTLO | O | Crystal/Clock Circuit |
| 14 | D0 | IA/OA | Host Parallel Interface |
| 15 | D2 | IA/OA | Host Parallel Interface |
| 16 | D3 | IA/OA | Host Parallel Interface |
| 17 | D5 | IA/OA | Host Parallel Interface |
| 18 | D7 | IA/OA | Host Parallel Interface |
| 19 | DGND2 | GND | |
| 20 | RS0 | IA | Host Parallel Interface |
| 21 | +5VA | PWR | |
| 22 | AGND1 | GND | |
| 23 | RIN | I(DA) | Line Interface |
| 24 | VC | MI | To GND through capacitors |
| 25 | VREF | MI | To VC through capacitors |
| 26 | TXA2 | O(DD) | Line Interface |
| 27 | TXA1 | O(DD) | Line Interface |
| 28 | TALK | OA | Line Interface |
| 29 | SPKR | O(DF) | Speaker Circuit |
| 30 | AGND2 | GND | |
| 31 | OHRC | OD | Line Interface |
| 32 | POR | MI | Connect to RESET |
| 33 | CLKIN | MI | Output from IA_CLKOUT |
| 34 | DTR | IA | DTE Serial Interface |
| 35 | RXD | OA | DTE Serial Interface |
| 36 | +5VD2 | PWR | |
| 37 | CTS | OA | DTE Serial Interface |
| 38 | IRQ | MI | Output to DSP_IRQ |
| 39 | RES | MI | Input from DSP_RESET |
| 40 | DGND3 | GND | |
| 41 | +5VD3 | PWR | |
| 42 | RXOUT | | NC |
| 43 | DGND4 | GND | |
| 44 | RMODE | MI | Connect to TMODE |
| 45 | TMODE | MI | Connect to RMODE |
| 46 | EYESYNC | OA | Eye Pattern Test Circuit |
| 47 | EYECLK | OA | Eye Pattern Test Circuit |
| 48 | EYEXY | OA | Eye Pattern Test Circuit |
| 49 | TXDAT | | NC |
| 50 | TDCLK | OA | DTE Serial Interface |
| 51 | RLSD | OA | DTE Serial Interface |
| 52 | RDCLK | OA | DTE Serial Interface |
| 53 | GP0 | MI | Connect to EYESYNC |
| 54 | XTCLK | IA | DTE Serial Interface |
| 55 | DGND5 | GND | |
| 56 | +5VD4 | PWR | |
| 57 | TXD | IA | DTE Serial Interface |
| 58 | DSR/RXRQ | OA | DTE Serial/DMA Interface |
| 59 | RESET | OA | Host Parallel Interface |

**Table 3. Modem Pin Assignments - 68-Pin PLCC (Cont'd)**

| Pin | Signal Label | Type | Interface |
|---|---|---|---|
| 60 | READ | IA | Host Parallel Interface |
| 61 | WRITE | IA | Host Parallel Interface |
| 62 | CS | IA | Host Parallel Interface |
| 63 | RS4 | IA | Host Parallel Interface |
| 64 | RS3 | IA | Host Parallel Interface |
| 65 | RS2 | IA | Host Parallel Interface |
| 66 | RS1 | IA | Host Parallel Interface |
| 67 | D6 | IA/OA | Host Parallel Interface |
| 68 | D4 | IA/OA | Host Parallel Interface |

**Notes:**

1. I/O types:
   MI = Modem interconnect.
   IA, IB = Digital input.
   OA, OB, OD = Digital output.
   I(DA)] = Analog input.
   O(DD), O(DF) = Analog output.
2. NC = No external connection allowed.
3. VREG pin can be NC; capacitor connection required for compatibility with future products.

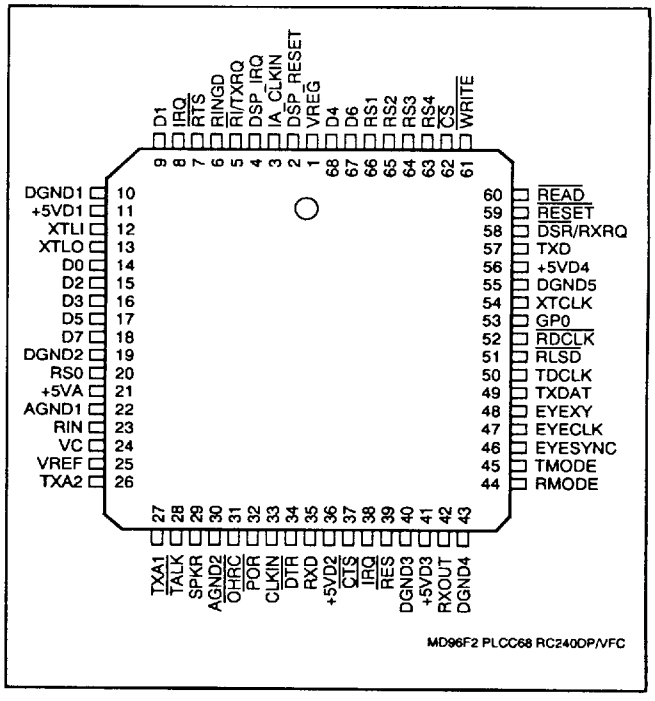


**Figure 2. Modem Pin Assignments- 68-Pin PLCC**

**Table 4. Hardware Interface Signal Definitions**

| Label | I/O Type | Signal/Definition |
|---|---|---|
| | | **OVERHEAD SIGNALS** |
| XTLI, XTLO | I, O | **Crystal In and Crystal Out.** The modem must be connected to an external crystal circuit consisting of a 40.32 MHz crystal, three capacitors, and an inductor. |
| $\overline{\text{RESET}}$ | IA | **Reset.** $\overline{\text{RESET}}$ low holds the modem in the reset state. $\overline{\text{RESET}}$ must be held low for at least 3 µs. $\overline{\text{RESET}}$ going high releases the modem from the reset state and initiates normal operation using power turn-on (default) values. The modem is ready to use 400 ms after the low-to-high transition of $\overline{\text{RESET}}$. |
| +5VD | PWR | **+ 5V Digital Supply.** +5V ± 5%. |
| +5VA | PWR | **+ 5V Analog Supply.** +5V ± 5%. |
| DGND, AGND | GND | **Digital Ground and Analog Ground.** Connect to ground. |
| | | **MICROPROCESSOR BUS**<br>Address, data, control, and interrupt hardware interface signals allow modem connection to an 8086-compatible microprocessor bus. With the addition of external logic, the interface can be made compatible with a wide variety of other microprocessors such as the 6502, 8086 or 68000. The microprocessor interface allows a microprocessor to change modem configuration, read or write channel and diagnostic data, and supervise modem operation by writing control bits and reading status bits. |
| D0–D7 | IA/OB | **Data Lines.** Eight bidirectional data lines (D0–D7) provide parallel transfer of data between the host and the modem. The most significant bit is D7. Data direction is controlled by the Read Enable and Write Enable signals. |
| RS0–RS4 | IA | **Register Select Lines.** The five active high register select lines (RS0–RS4) address interface memory registers within the modem interface memory. These lines are typically connected to the five least significant lines (A0–A4) of the address bus.<br>The modem decodes RS0 through RS4 to address one of 32 internal interface memory registers (00–1F). The most significant address bit is RS4 while the least significant address bit is RS0. The selected register can be read from or written into via the 8-bit parallel data bus (D0–D7). The most significant data bit is D7 while the least significant data bit is D0. |
| $\overline{\text{CS}}$ | IA | **Chip Select.** $\overline{\text{CS}}$ selects the modem for microprocessor bus operation. $\overline{\text{CS}}$ is typically generated by decoding host address bus lines. |
| $\overline{\text{READ}}$ | IA | **Read Enable.** During a read cycle ($\overline{\text{READ}}$ asserted), data from the selected interface memory register is gated onto the data bus by means of three-state drivers in the modem. These drivers force the data lines high for a one bit, or low for a zero bit. When not being read, the three-state drivers assume their high-impedance (off) state. |
| $\overline{\text{WRITE}}$ | IA | **Write Enable.** During a write cycle ($\overline{\text{WRITE}}$ asserted), data from the data bus is copied into the selected modem interface memory register, with high and low bus levels representing one and zero bit states, respectively. |
| IRQ | OA | **Interrupt Request.** The modem IRQ output may be connected to the host processor interrupt request input in order to interrupt host program execution for immediate modem service. The IRQ output can be enabled in the modem interface memory to indicate immediate change of conditions. The use of IRQ is optional depending upon modem application. The IRQ output is driven by a TTL-compatible CMOS driver. |
| TXRQ | OA | **Transmitter Request.** When control bit DMAE in interface memory is set 1, pin 5 (68-pin PLCC) operates as the TXRQ output function rather than the $\overline{\text{RI}}$ function. TXRQ is a high active signal that follows the state of the TDBE bit. DMA operation is available in asynchronous, synchronous and HDLC modes. Bit FIFOEN must be set in asynchronous modes in order to obtain the TXRQ interrupt. (TPDM = 1) |
| RXRQ | OA | **Receiver Request.** When control bit DMAE in interface memory is set 1, pin 58 (68-pin PLCC) operates as the the RXRQ output function rather than the $\overline{\text{DSR}}$ function. RXRQ is a high active signal that follows the state of the RDBF bit. DMA operation is available in asynchronous, synchronous and HDLC modes. Bit FIFOEN must be set in asynchronous modes in order to obtain the RXRQ interrupt. (TPDM = 1) |

**Table 4. Hardware Interface Signal Definitions (Cont'd)**

| Label | I/O Type | Signal/Definition |
|---|---|---|
| | | **V.24 SERIAL INTERFACE**<br>Timing, data, control, and status signals provide a V.24-compatible serial interface. These signals are TTL compatible in order to drive the short wire lengths and circuits normally found within a printed circuit board, stand-alone modem enclosures, or equipment cabinets. For driving longer cables, these signals can be easily converted to EIA/TIA-232-E voltage levels. |
| TXD | IA | **Transmitted Data.** The modem obtains serial data to be transmitted from the local DTE on the Transmitted Data (TXD) input. |
| RXD | OA | **Received Data.** The modem presents received serial data to the local DTE on the Received Data (RXD) output. |
| $\overline{RTS}$ | IA | **Request to Send.** Activating ($\overline{RTS}$) causes the modem to transmit data on TXD when $\overline{CTS}$ becomes active. The $\overline{RTS}$ pin is logically ORed with the RTS bit. |
| $\overline{CTS}$ | OA | **Clear To Send. $\overline{CTS}$** active indicates to the local DTE that the modem will transmit any data present on TXD. CTS response times from an active condition of RTS are shown in Table 1-2. |
| $\overline{RLSD}$ | OA | **Received Line Signal Detector.** $\overline{RLSD}$ active indicates to the local DTE that energy above the receive level threshold is present on the receiver input, and that the energy is not a training sequence.<br>One of four $\overline{RLSD}$ receive level threshold options can be selected (RTH bits). A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold level and hysteresis action are measured with a modulated signal applied to the Receiver Analog (RXA) input. Note that performance may be degraded when the received signal level is less than -43 dBm. The $\overline{RLSD}$ on and off thresholds are host programmable in DSP RAM. |
| $\overline{DTR}$ | IA | **Data Terminal Ready.** In V.32 bis, V.32, V.22 bis, V.22, or Bell 212A configuration, activating $\overline{DTR}$ initiates the handshake sequence, provided that the DATA bit is a 1. If in answer mode, the transmitter will immediately send answer tone.<br>In V.21, V.23, or Bell 103 configuration, activating $\overline{DTR}$ causes the modem to enter the data state provided that the DATA bit is a 1. If in answer mode, the transmitter will immediately send answer tone. In these modes, if controlled carrier is enabled, carrier is controlled by RTS.<br>During the data mode, deactivating $\overline{DTR}$ causes the transmitter and receiver to turn off and return to the idle state.<br>The $\overline{DTR}$ input and the DTR control bit are logically ORed. |
| $\overline{DSR}$ | OA | **Data Set Ready.** $\overline{DSR}$ ON indicates that the modem is in the data transfer state. $\overline{DSR}$ OFF indicates that the DTE is to disregard all signals appearing on the interchange circuits except Ring Indicator ($\overline{RI}$). $\overline{DSR}$ is OFF when the modem is in a test mode (i.e., local analog or remote digital loopback). The DSR status bit reflects the state of the $\overline{DSR}$ output.<br>When control bit DMAE in interface memory is set 1, pin 58 (68-pin PLCC) operates as the the RXRQ output function rather than the $\overline{DSR}$ function (see RXRQ under Microprocessor Bus). |
| $\overline{RI}$ | OA | **Ring Indicator.** $\overline{RI}$ output follows the ringing signal present on the line with a low level (0V) during the ON time, and a high level (+5V) during the OFF time coincident with the ringing signal. The RI status bit reflects the state of the $\overline{RI}$ output.<br>When control bit DMAE in interface memory is set 1, pin 5 (68-pin PLCC) operates as the TXRQ output function rather than the $\overline{RI}$ function (see TXRQ under Microprocessor Bus). |
| TDCLK | OA | **Transmit Data Clock.** The modem outputs a synchronous Transmit Data Clock (TDCLK) for USRT timing. The TDCLK frequency is the data rate (±0.01%) with a duty cycle of 50 ±1%. The TDCLK source can be internal, external (input on XTCLK) or slave (to $\overline{RDCLK}$) as selected by TXCLK bits in interface memory. |
| XTCLK | IA | **External Transmit Clock.** In synchronous communication, an external transmit data clock can be connected to the modem XTCLK input. The clock supplied at XTCLK must exhibit the same characteristics as TDCLK. The XTCLK input is then reflected at the TDCLK output. |
| $\overline{RDCLK}$ | OA | **Receive Data Clock.** The modem outputs a synchronous Receive Data Clock ($\overline{RDCLK}$) for USRT timing. The $\overline{RDCLK}$ frequency is the data rate (±0.01%) with a duty cycle of 50 ±1%. The $\overline{RDCLK}$ low-to-high transitions coincide with the center of the received data bits. |

Table 4. Hardware Interface Signal Definitions (Cont'd)

| Label | I/O Type | Signal/Definition |
|---|---|---|
| | | **LINE INTERFACE** |
| TXA1, TXA2 | O(DF) | **Transmit Analog 1 and 2.** The TXA1 and TXA2 outputs are differential outputs 180 degrees out of phase with each other. Each output can drive a 300 Ω load. |
| RIN | I(DA) | **Receive Analog.** RIN is a single-ended receive data input from the telephone line interface or an optional external hybrid circuit. |
| RINGD | IA | **Ring Detect.** The RINGD input is monitored for pulses in the range of 15 Hz to 68 Hz. The frequency detection range may be changed by ConfigurACE. The circuit driving RINGD should be a 4N35 optoisolator or equivalent. The circuit driving RINGD should not respond to momentary bursts of ringing less than 125 ms in duration, or less than 40 VRMS (15 Hz to 68 Hz) across TIP and RING. The idle state (no ringing) output of the ring detect circuit should be low. |
| $\overline{\text{OHRC}}$ | OD | **Off-Hook Relay Control.** The $\overline{\text{OHRC}}$ output can directly drive a +5V reed relay coil with a minimum resistance of 360 ohms (13.9 mA max. @ 5.0V) and having a must-operate voltage of no greater than 4.0 Vdc. A clamp diode, such as a 1N4148, should be installed across the relay coil. An external transistor can be used to drive heavier loads (e.g., electro-mechanical relays). $\overline{\text{OHRC}}$ is controlled by the host setting the RA bit.<br>In a typical application, $\overline{\text{OHRC}}$ is connected to the normally open Off-Hook relay. In this case, $\overline{\text{OHRC}}$ active closes the relay to connect the modem to the telephone line. |
| $\overline{\text{TALK}}$ | OD | **Talk/Data Relay Control.** The $\overline{\text{TALK}}$ output can directly drive a +5V reed relay coil with a minimum resistance of 360 ohms (13.9 mA max. @ 5.0V) and having a must-operate voltage of no greater than 4.0 Vdc. A clamp diode, such as a 1N4148, should be installed across the relay coil. An external transistor can be used to drive heavier loads (e.g., electro-mechanical relays). $\overline{\text{TALK}}$ is controlled by the host setting the RB bit.<br>In a typical application, $\overline{\text{TALK}}$ is connected to the normally closed Talk/Data relay. In this case, $\overline{\text{TALK}}$ active opens the relay to disconnect the handset from the telephone line. |
| | | **SPEAKER INTERFACE** |
| SPKR | O(DF) | **Speaker Analog Output.** The SPKR output reflects the received analog input signal. The SPKR on/off and three levels of attenuation are controlled by bits in DSP RAM. When the speaker is turned off, the SPKR output is clamped to the voltage at the VC pin. The SPKR output can drive an impedance as low as 300 ohms. In a typical application, the SPKR output is an input to an external LM386 audio power amplifier. |
| | | **DIAGNOSTIC SIGNALS**<br>Three signals provide the timing and data necessary to create an oscilloscope quadrature eye pattern. The eye pattern is simply a display of the received baseband constellation. By observing this constellation, common line disturbances can usually be identified. |
| EYEXY | OA | **Serial Eye Pattern X/Y Output.** EYEXY is a serial output containing two 15-bit diagnostic words (EYEX and EYEY) for display on the oscilloscope X axis (EYEX) and Y axis (EYEY). EYEX is the first word clocked out; EYEY follows. Each word has 8-bits of significance. Each 15-bit data word is shifted out most significant bit first with the seven most significant bits set to zero. EYEXY is clocked by the rising edge of $\overline{\text{EYECLK}}$. This serial digital data must be converted to parallel digital form by a serial-to-parallel converter and then to analog form by two digital-to-analog (D/A) converters. |
| $\overline{\text{EYECLK}}$ | OA | **Serial Eye Pattern Clock.** $\overline{\text{EYECLK}}$ is a 288 kHz output clock for use by the serial-to-parallel converters. The low-to-high transitions of $\overline{\text{RDCLK}}$ coincide with the low-to-high transitions of $\overline{\text{EYECLK}}$. $\overline{\text{EYECLK}}$, therefore, can be used as a receiver multiplexer clock. |
| EYESYNC | OA | **Serial Eye Pattern Strobe.** EYESYNC is a strobe for loading the D/A converters. |

**Table 5. Digital Interface Characteristics**

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| Input High Voltage | $V_{IH}$ | | | | Vdc | |
| Types IA and IB | | 2.0 | – | $V_{CC}$ | | |
| Type ID | | 0.8($V_{CC}$) | – | $V_{CC}$ | | |
| Input High Current | $I_{IH}$ | – | – | 40 | µA | $V_{CC}$ = 5.25V, $V_{IN}$ = 5.25V |
| Input Low Voltage | $V_{IL}$ | 0.3 | – | 0.8 | Vdc | |
| Input Low Current | $I_{IL}$ | – | – | 400 | µA | $V_{CC}$ = 5.25V |
| Input Leakage Current | $I_{IN}$ | – | – | ±2.5 | µA | $V_{IN}$ = 0 to +5V, $V_{CC}$ = 5.25V |
| Output High Voltage | $V_{OH}$ | | | | Vdc | |
| Type OA | | 3.5 | – | – | | $I_{LOAD}$ = – 100 µA |
| Type OD | | – | – | $V_{CC}$ | | $I_{LOAD}$ = 0 mA |
| Output Low Voltage | $V_{OL}$ | | | | Vdc | |
| Type OA | | – | – | 0.4 | | $I_{LOAD}$ = 1.6 mA |
| Type OB | | – | – | 0.4 | | $I_{LOAD}$ = 0.8 mA |
| Type OD | | – | | 0.75 | | $I_{LOAD}$ = 15 mA |
| Three–State Input Current (Off) | $I_{TSI}$ | – | – | ±10 | µA | $V_{IN}$ = 0.4 to $V_{CC}$ –1 |

**Table 6. Analog Interface Characteristics**

| Name | Type | Characteristic | Value |
|---|---|---|---|
| RIN | I (DA) | Input Impedance | > 70K Ω |
| | | Voltage Range | 2.5 ±1.6 V |
| TXA1, TXA2 | O (DD) | Minimum Load | 300 Ω |
| | | Maximum Capacitive Load | 0.01 µF |
| | | Output Impedance | 10 Ω |
| | | Output Voltage | 2.5 ± 1.6 V |
| | | D.C. Offset | < 200 mV |
| SPKR | O (DF) | Minimum Load | 300 Ω |
| | | Maximum Capacitive Load | 0.01 µF |
| | | Output Impedance | 10 Ω |
| | | Output Voltage | 2.5 ± 1.6 V |
| | | D.C. Offset | < 20 mV |

**Table 7. Power Requirements**

| Mode | Current ($I_D$) | | | Power ($P_D$) | | |
|---|---|---|---|---|---|---|
| | Typical Current @$T_A$ = 25°C | Maximum Current @$T_A$ = 0°C | Maximum Current @$T_A$ = -40°C | Typical Power @$T_A$ = 25°C | Maximum Power @$T_A$ = 0°C | Maximum Power @$T_A$ = -40°C |
| Normal mode | 180 mA | 215 mA | 270 mA | 900 mW | 1135 mW | 1420 mW |
| Sleep mode | 2.0 mA | 2.4 mA | 3.1 mA | 10.0 mW | 12.6 mW | 16.3 mW |

**Notes:**
1. Maximum power @ -40°C specified only for extended temperature range parts.
2. Test conditions: VCC = 5.0 VDC for typical values; VCC = 5.25 VDC for maximum values.
3. Input voltage ripple ≤ 0.1 V peak-peak.

**Table 8. Absolute Maximum Ratings**

| Parameter | Symbol | Limits | Units |
|---|---|---|---|
| Supply Voltage | $V_{DD}$ | -0.5 to +7.0 | V |
| Input Voltage | $V_{IN}$ | -0.5 to +5VD +0.5 | V |
| Analog Inputs | $V_{IN}$ | -0.3 to +5VA + 0.3 | V |
| Voltage Applied to Outputs in High Impedance (Off) State | $V_{HZ}$ | -0.5 to +5VD + 0.5 | V |
| DC Input Clamp Current | $I_{IK}$ | ±20 | mA |
| DC Output Clamp Current | $I_{OK}$ | ±20 | mA |
| Static Discharge Voltage (25°C) | $V_{ESD}$ | ±3000 | V |
| Latch-up Current (25°C) | $I_{TRIG}$ | ±200 | mA |
| Operating Temperature Range | $T_A$ | | |
| Commercial | | -0 to +70 | °C |
| Industrial (E Model Number Suffix) | | -40 to +85 | °C |
| Storage Temperature Range | $T_{STG}$ | -55 to +125 | °C |

## SOFTWARE INTERFACE

Modem functions are implemented in firmware executing in the modem DSP.

### INTERFACE MEMORY

The DSP communicates with the host processor by means of a dual-port, interface memory. The interface memory contains thirty-two 8-bit registers, labeled register 00 through 1F (Figure 3). Each register can be read from, or written into, by both the host and the DSP. The host communicates with the DSP interface memory via the microprocessor bus.

The host can control modem operation by writing control bits to DSP interface memory and writing parameter values to DSP RAM through the interface memory. The host can monitor modem operation by reading status bits from DSP interface memory and reading parameter values from DSP RAM through interface memory.

Table 9 defines the individual bits in the interface memory. Bits in the interface memory are referred to using the format Z:Q. The register number is specified by Z (00 through 1F) and the bit number by Q (0 through 7; 0 = LSB).

| Register | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 1F | NSIA | NCIA | — | NSIE | NEWS | NCIE | — | NEWC |
| 1E | TDBIA | RDBIA | TDBIE | — | TDBE | RDBIE | — | RDBF |
| 1D | MEACC | — | MEMW | MEMCR | MEMORY ACCESS ADDR HIGH B-8 (MEADDH) | | | |
| 1C | MEMORY ACCESS ADDR LOW 7-0 (MEADDL) | | | | | | | |
| 1B | — | — | — | — | — | — | — | — |
| 1A | SFRES | RIEN | RION | DMAE | — | SCOBF | SCIBE | SECEN |
| 19 | MEMORY ACCESS DATA MSB F-8 (MEDAM) | | | | | | | |
| 18 | MEMORY ACCESS DATA LSB 7-0 (MEDAL) | | | | | | | |
| 17 | SECONDARY TRANSMIT BUFFER (SECTXB) | | | | | | | |
| 16 | SECONDARY RECEIVE BUFFER (SECRXB) | | | | | | | |
| 15 | SLEEP | — | RDWK | HWRWK | AUTO | RREN | EXL3 | EARC |
| 14 | ABCODE | | | | | | | |
| 13 | TLVL | | | | RTH | | TXCLK | |
| 12 | CONFIGURATION (CONF) | | | | | | | |
| 11 | BRKS | PARSL | | TXV | RXV | V23HDX | TEOF | TXP |
| 10 | TRANSMIT BUFFER (TBUFFER)/VOICE TRANSMIT BUFFER (VBUFT) | | | | | | | |
| 0F | RLSD | FED | CTS | DSR | RI | TM | RTSDT | V54DT |
| 0E | RTDET | BRKD | RREDT | V32BDT | SPEED | | | |
| 0D | P2DET | PNDET | S1DET | SCR1 | U1DET/ ECTRN | SADET/ DETID | TXFNF | HKAB |
| 0C | AADET/ PROBED | ACDET/ MODEOK | CADET/ NEGDET | CCDET/ DET800 | SDET | SNDET | RXFNE | RSEQ |
| 0B | TONEA | TONEB | TONEC | ATV25 | ATBEL | — | V32DIS | EQMAT |
| 0A | PNSUC | FLAGDT | PE | FE | OE | CRCS | FLAGS | SYNCD |
| 09 | NV25 | CC | DTMF | ORG | LL | DATA | RRTSE | DTR |
| 08 | ASYN | TPDM | V21S | V54T | V54A | V54P | RTRN | RTS |
| 07 | RDLE | RDL | L2ACT | DDIS | L3ACT | L4ACT | RA | MHLD |
| 06 | RTDIS | EXOS | CF17 | HDLC | PEN | STB | WDSZ | |
| 05 | ECFZ | ECSQ | FECSQ | TXSQ | CEQ | TTDIS | STOFF | LECEN |
| 04 | RB | EQT2 | V32BS | FIFOEN | EQFZ | NRZIEN | TOD | STRN |
| 03 | EPT | SEPT | SRCEN | RLSDE | ARC | SDIS | GTE | GTS |
| 02 | TDE | SQDIS | S511 | — | RTSDE | V54TE | V54AE | V54PE |
| 01 | VOLUME | | — | — | — | TXHF | RXHF | RXP |
| 00 | RECEIVE BUFFER (RBUFFER)/VOICE RECEIVE BUFFER (VBUFR) | | | | | | | |

**Note:** — in the "Bit" columns indicates the bit is reserved for modem use only.

**Figure 3. Modem Interface Memory Map**

**Table 9. Interface Memory Bit Definitions**

| Mnemonic | Memory Location | Default Value | Name/Description |
|---|---|---|---|
| AADET | 0C:7 | – | **AA Detector.** AADET indicates the AA sequence detection status. (V.FC, V.32 bis, V.32) |
| ABCODE | 14:0–7 | 00 | **Abort Code.** ABCODE contains a code indicating the point in the handshake where the handshake failure occurred as indicated by status bit HKAB. (V.FC, V.32 bis, V.32) |
| ACDET | 0C:6 | – | **AC Detector.** ACDET indicates the AC sequence detection status. (V.FC, V.32 bis, V.32) |
| ARC | 03:3 | 1 | **Automatic Rate Change Enable.** Control bit ARC is used to inform the modem to automatically condition itself to transmit data at the highest common rate negotiated during the handshake. (V.FC, V.32 bis, V.32)<br>The modem will try to connect in V.FC then drop down to V.32 bis and V.32 (ARC = 1) or will try to connect in V.FC only (ARC = 0). (V.FC)<br>The host may specify the undefined bits in the rate sequence in DSP RAM. (V.32 bis, V.32)<br>Control bit ARC is used to allow setting of the RTRN bit to cause the modem to send a rate change sequence rather than the normal retrain sequence. (V.22 bis) (See RTRN.) |
| ASYN | 08:7 | 0 | **Asynchronous/Synchronous.** Control bit ASYN selects either asynchronous or synchronous mode. (V.FC, V.32 bis, V.32, V.22 bis, V.22, Bell 212A) |
| ATBEL | 0B:3 | – | **Bell Answer Tone Detector.** ATBEL indicates the modem receiver 2225 Hz answer tone detection status. ATBEL is active only when the DATA bit is a 0 and the modem is in originate mode. (Bell 212A, Bell 103) |
| ATV25 | 0B:4 | – | **V25 Answer Tone Detector.** ATV25 indicates the modem receiver 2100 Hz answer tone detection status. ATV25 is only active when the DATA bit is a 0 and the modem is in originate mode. (V.FC, V.32 bis, V.32, V.22 bis, V.22, V.23, V.21) |
| AUTO | 15:3 | 0 | **Automatic Mode Change Enable.** Control bit AUTO is used to enable the modem to automatically determine the communication standard supported by the remote modem and configure itself accordingly. The possible operating modes are: V.FC, V.32 bis, V.32, V.22 bis, V.22, Bell 212A, Bell 103, V.23 and V.21. |
| BRKD | 0E:6 | – | **Break Detected.** Status bit BRKD is used to indicate when the modem is receiving continuous space. |
| BRKS | 11:7 | 0 | **Break Sequence.** Control bit BRKS is used to enable sending of continuous space or sending of parallel data from the TBUFFER in parallel asynchronous mode (see TPDM). |
| CADET | 0C:5 | – | **CA Detector.** CADET indicates the CA sequence detection status. (V.FC, V.32 bis, V.32) |
| CC | 09:6 | 0 | **Controlled Carrier.** Control bit CC selects RTS controlled carrier or constant carrier operation. (V.22 bis, V.22, V.23, V.21, Bell 212A) |
| CCDET | 0C:4 | – | **CC Detector.** CCDET indicates the CC sequence detection status. (V.FC, V.32 bis, V.32) |
| CEQ | 05:3 | 1 | **Compromise Equalizer Enable.** Control bit CEQ enables or disables insertion of the digital compromise equalizer into the transmit path. |
| CF17 | 06:5 | 0 | **Carrier Frequency 1700 Hz.** Control bit CF17 selects 1700 Hz or 1800 Hz carrier frequency. The non-standard 1700 Hz option is provided for use with a secondary channel which is added at the high end of the band. (V.17) |

**Table 9. Interface Memory Bit Definitions (Cont'd)**

| Mnemonic | Memory Location | Default Value | Name/Description |
|---|---|---|---|
| CONF | 12:0–7 | 76 | **Modem Configuration.** The CONF control bits select the modem configuration from the following codes: |

| Mode | Data Rate | CONF (Hex) | |
|---|---|---|---|
| V.FC Clear Down | — | 40 | See Note 1. |
| V.FC TCM | 28800 | 4C | |
| V.FC TCM | 26400 | 4B | |
| V.FC TCM | 24000 | 4A | |
| V.FC TCM | 21600 | 49 | |
| V.FC TCM | 19200 | 48 | |
| V.FC TCM | 16800 | 47 | |
| V.FC TCM | 14400 | 46 | |
| V.32 bis TCM | 14400 | 76 | |
| V.32 bis TCM | 12000 | 72 | |
| V.32 TCM | 9600 | 74 | |
| V.32 | 9600 | 75 | |
| V.32 bis TCM | 7200 | 78 | |
| V.32 | 4800 | 71 | |
| V.32 bis/V.32 Clear Down | — | 70 | See Note 1. |
| V.17 TCM | 14400 | B1 | |
| V.17 TCM | 12000 | B2 | |
| V.17 TCM | 9600 | B4 | |
| V.17 TCM | 7200 | B8 | |
| V.29 | 9600 | 14 | |
| V.29 | 7200 | 12 | |
| V.29 | 4800 | 11 | |
| V.27 ter | 4800 | 02 | |
| V.27 ter | 2400 | 01 | |
| V.26 bis | 2400 | 08 | |
| V.26 bis | 1200 | 04 | |
| V.26 A | 2400 | 0C | |
| V.22 bis | 2400 | 84 | |
| V.22 bis | 1200 | 82 | See Note 2. |
| V.22 | 1200 | 52 | |
| V.22 | 600 | 51 | |
| V.21 | 0-300 | A0 | |
| V.21 Channel 2 | 300 | A8 | |
| Bell 208 | 4800 | 23 | |
| Bell 212A | 1200 | 62 | |
| Bell 103 | 0-300 | 60 | |
| V.23 | 1200 TX/75 RX | A4 | |
| V.23 | 75 TX/1200 RX | A1 | |
| Transmit Single Tone | — | 80 | See Notes 3 and 4. |
| Transmit Dual Tone | — | 83 | See Notes 3 and 4. |
| Dialing | — | 81 | See Note 4. |

**NOTES:**

1. The modem can transmit a V.FC/V.32 bis/V.32 GSTN Clear Down sequence during a retrain or a rate renegotiation.

   In V.32 bis/V.32, the remote modem will automatically detect the Clear Down sequence and both modems will drop carrier at the end of the retrain or rate renegotiation.

   In V.FC, the modem will indicate the Clear Down detection by writing a 96h in ABCODE. The host must terminate the connection by resetting DTR and setting NEWC.
2. Configuration 82 allows for possible fall forward to 2400 bps.
3. The modem transmits one or two tones depending upon the selected mode. The tone frequencies and levels are host programmable in DSP RAM.
4. Voice pass-through mode can run concurrently; see TXV and RXV bits.

**Table 9. Interface Memory Bit Definitions (Cont'd)**

| Mnemonic | Memory Location | Default Value | Name/Description |
|---|---|---|---|
| CRCS | 0A:2 | 0 | **CRC Sending.** Status bit CRCS is used to indicate that the transmitter is sending or not sending the CRC (2 bytes) in HDLC synchronous parallel mode. |
| CTS | 0F:5 | – | **Clear To Send.** Status bit CTS is used to indicate that the training sequence has been completed and any data present at TXD (serial mode) or in TBUFFER (parallel mode) will be transmitted. CTS response times from an RTS ON or OFF transition after the modem has completed a handshake are shown in Table 2. The CTS OFF-to-ON response time is programmable in DSP RAM. |
| DATA | 09:2 | 1 | **Data.** Control bit DATA is used to prevent the transmitter from entering and proceeding with the handshake (start-up) sequence and to ignore all V.24 interface signals. |
| DDIS | 07:4 | 0 | **Descrambler Disable.** Control bit DDIS is used to disable or enable the receiver's descrambler. |
| DET800 | 0C:4 | 0 | **800 Hz Tone Detected.** Status bit DET800 is used to indicate that the 800 Hz tone sent by the V.FC originating modem confirming the start of the V.FC handshake has been detected. (V.FC). |
| DETID | 0D:2 | 0 | **Answer Tone Identification Sequence Detected.** Status bit DETID is used to indicate that the answer tone identification sequence sent by the answering modem confirming the start of the V.FC handshake has been detected. (V.FC). |
| DMAE | 1A:4 | 0 | **DMA Signals Enabled.** Control bit DMAE is used to enable DMA by assigning the $\overline{RI}$ and $\overline{DSR}$ output signals to TXRQ (Transmitter Request ) and RXRQ (Receiver Request), respectively. TXRQ is an active high signal that follows the assertion state of the TDBE bit and RXRQ is an active high signal that follows the assertion state of the RDBF bit. DMA is available in asynchronous, synchronous, and HDLC modes (TPDM = 1). |
| DSR | 0F:4 | – | **Data Set Ready.** Status bit DSR is used to indicate the modem is in the data transfer state. The DTE is to disregard all signals appearing on the interchange circuits except $\overline{RI}$ when DTR is OFF. DSR will switch to the OFF state when the modem is in a test mode. |
| DTMF | 09:5 | 1 | **DTMF Select.** Control bit DTMF selects either DTMF or pulse dialing mode. |
| DTR | 09:0 | 0 | **Data Terminal Ready.** In modes V.FC, V.32 bis, V.32, V.22 bis, V.22, and Bell 212A, control bit DTR is used to initiate a handshake sequence in originate mode when the DATA bit is set, or to immediately send answer tone in answer mode.<br><br>In modes V.21, V.23, and Bell 103, control bit DTR must be set for the modem to enter data state when DATA bit is set. If in answer mode, the transmitter will send answer tone. If controlled carrier is selected, the carrier is controlled by the $\overline{RTS}$ pin or RTS bit.<br><br>During the data mode, setting $\overline{DTR}$ will cause the transmitter to turn off. The DTR bit parallels the operation of the hardware $\overline{DTR}$ control input. These inputs are ORed by the modem. |
| EARC | 15:0 | 1 | **Extended Automatic Rate Change.** Control bit EARC is used to enable automatic rate adaption in V.FC modes or automatic rate change in V.32 bis/V.32 modes during the handshake. (V.FC, V.32 bis, V.32). |
| ECFZ | 05:7 | 0 | **Echo Canceller Freeze.** Control bit ECFZ inhibits or enables updating of the echo canceller taps. (V.FC, V.32 bis, V.32) |
| ECSQ | 05:6 | 0 | **Echo Canceller Squelch.** Control bit ECSQ is used to force the echo canceller output to zero. (V.FC, V.32 bis, V.32) |
| ECTRN | 0D:3 | 0 | **Training Detected.** Status bit ECTRN is used to indicate that the V.FC training sequence has been detected. (V.FC). |
| EPT | 03:7 | 0 | **Echo Protector Tone Enable.** Control bit EPT is used to enable transmission of the echo protector tone prior to the transmission of the training sequence. (V.17, V.29, V.27 ter) |
| EQFZ | 04:3 | 0 | **Equalizer Freeze.** Control bit EQFZ inhibits or enables updating of the receiver's adaptive equalizer taps. (V.FC, V.32 bis, V.32, V.22 bis, V.22, Bell 212A) |
| EQMAT | 0B:0 | 0 | **EQM Above Threshold.** Status bit EQMAT is used to indicate that the measured EQM is above the threshold value programmed in DSP RAM. |
| EQT2 | 04:6 | 1 | **Equalizer T/2 Spacing Select.** Control bit EQT2 selects the receiver's adaptive equalizer spacing to be either T/2 fractionally spaced or T spaced (T = 1 baud time). (V.FC, V.32 bis, V.32, V.22 bis, V.22, Bell 212A) |

**Table 9. Interface Memory Bit Definitions (Cont'd)**

| Mnemonic | Memory Location | Default Value | Name/Description |
|---|---|---|---|
| EXL3 | 15:1 | 0 | **External Loop 3 Selector.** Control bit EXL3 selects either external or internal path during local analog test (loop 3). (See L3ACT.) |
| EXOS | 06:6 | 0 | **Extended Overspeed.** Control bit EXOS selects Extended or Normal Overspeed mode. (V.FC, V.32 bis, V.32, V.22 bis, V.22, Bell 212A) |
| FE | 0A:4 | 0 | **Framing Error.** Status bit FE is used to indicate that more than 1 in 8 (or 1 in 4 for extended overspeed) characters were received without a Stop bit in asynchronous mode, or an ABORT sequence was detected in HDLC synchronous parallel mode. |
| FECSQ | 05:5 | 0 | **Far Echo Canceller Squelch.** Control bit FECSQ is used to force the output of the far-end echo canceller to zero. (V.FC, V.32 bis, V.32) |
| FED | 0F:6 | – | **Fast Energy Detector.** Status bit FED is used to indicate energy in the passband above the selected receiver threshold has been detected (see RTH). |
| FIFOEN | 04:4 | 0 | **FIFO Enable.** Control bit FIFOEN is used to allow the host to write up to 16 bytes of data through TBUFFER, or voice samples through VBUFT, using the TDBE bit as a software interrupt or the TXRQ signal (DMAE = 1) as a DMA request. (TPDM = 1) |
| FLAGDT | 0A:6 | – | **V.21 Channel 2 Flag Detected.** Status bit FLAGDT is used to indicate that the V.21 Channel 2 Flag (7Eh) has been detected. (V.17, V.29, V.27 ter) |
| FLAGS | 0A:1 | 0 | **Flag Sequence.** Status bit FLAGS is used to indicate that the transmitter is sending the Flag sequence in HDLC mode, sending a constant mark in asynchronous parallel mode, or sending data. |
| GTE | 03:1 | 0 | **Guard Tone Enable.** Control bit GTE enables or disables transmission of guard tone by the answering modem as selected by the GTS bit. (V.22 bis, V.22) |
| GTS | 03:0 | 0 | **Guard Tone Select.** Control bit GTS selects the 550 Hz or 1800 Hz guard tone. (V.22 bis, V.22) |
| HDLC | 06:4 | 0 | **HDLC Select.** Control bit HDLC is used to enable HDLC operation in synchronous parallel data mode. |
| HKAB | 0D:0 | – | **Handshake Abort.** Status bit HKAB is used to indicate the handshake has failed. Upon failure detection, the transmitter remains in an abort state for 1 second after which HKAB is reset and the transmitter returns to the idle mode. (V.FC, V.32 bis, V.32) |
| HWRWK | 15:4 | 1 | **Host Write Wake up.** Control bit HWRWK is used to enable waking up of the modem from the sleep mode when the host writes to any register except 1D:0-7 (see SLEEP bit.) |
| L2ACT | 07:5 | 0 | **Loop 2 Activate.** Control bit L2ACT is used to cause the receiver's digital output to be connected to the transmitter's digital input (locally activated remote digital loopback) in accordance with V.54. (Not valid in FSK modes.) |
| L3ACT | 07:3 | 0 | **Loop 3 Activate.** Control bit L3ACT is used to cause the transmitter's analog output to be coupled internally to the receiver's analog input through an attenuator (local analog loopback) per V.54. The signal path for loop 3 can also be established externally to the modem (see EXL3). |
| L4ACT | 07:2 | 0 | **Loop 4 Activate.** Control bit L4ACT is used to cause the receiver's analog input to be connected internally to the transmitter's output (remote analog loopback) per V.54. (V.17, V.29, V.27 ter). (LL device only.) |
| LECEN | 05:0 | 0 | **Listener Echo Canceller Enable.** Control bit LECEN is used to enable the listener echo canceller in the receiver and to reduce the number of taps in the transmitter compromise equalizer from 25 to 5. Use of this bit improves performance over lines exhibiting listener echo. NEWC must be set after changing LECEN. (V.32 bis, V.32) |
| LL | 09:3 | 0 | **Leased Line.** Control bit LL selects leased or switched line operation. (V.22 bis, V.22) |
| MEACC | 1D:7 | 0 | **Memory Access Enable.** Control bit MEACC is used to enable modem accessing of the RAM associated with the address in MEADDH and MEADDL. The MEMW bit controls read or write. |
| MEADDL | 1C:0–7 | 00 | **Memory Access Address Low (7-0).** MEADDL contains the lower 8 bits (bits 7-0) of the address used to access modem RAM via the memory access data LSB (18) and MSB (19) registers. |
| MEADDH | 1D:0–3 | 0 | **Memory Access Address High (B-0).** MEADDH contains the upper 8 bits (bits B-8) of the address used to access modem RAM via the memory access data LSB (18) and MSB (19) registers. |

**Table 9. Interface Memory Bit Definitions (Cont'd)**

| Mnemonic | Memory Location | Default Value | Name/Description |
|---|---|---|---|
| MEDAL | 18:0–7 | 00 | **Memory Data LSB.** MEDAL is the least significant byte (bits 7-0) of the 16-bit data word used in reading or writing data locations in modem RAM. |
| MEDAM | 19:0–7 | 00 | **Memory Data MSB.** MEDAM is the most significant byte (bits F-8) of the 16-bit data word used in reading or writing data locations in modem RAM. |
| MEMCR | 1D:4 | 0 | **Memory Continuous Read.** Control bit MEMCR is used to enable continuous DSP RAM read. |
| MEMW | 1D:5 | 0 | **Memory Write.** When MEMW is set and MEACC is set, the modem copies data from interface memory data registers MEDAL (18) and MEDAH (19) to the memory location addressed by MEADDL and MEADDH. When control bit MEMW is reset and MEACC is set, the DSP copies data from the location addressed by MEADDL and MEADDH to MEDAL (18) and MEDAH (19). |
| MHLD | 07:0 | 0 | **Mark Hold.** Control bit MHLD is used to enable the transmitter to either clamp the digital input data to a mark or to take the input from TXD or TBUFFER (see TPDM). |
| MODEOK | 0C:6 | 0 | **Mode OK.** Status bit MODEOK is used to indicate that the modem has configured itself based on the results of the V.FC negotiation and is ready to continue with training and rate negotiation. (V.FC). |
| NCIA | 1F:6 | – | **NEWC Interrupt Active.** Status bit NCIA is used to indicate that NEWC caused IRQ to be asserted when enabled by the NCIE bit. (See NEWC and NCIE.) |
| NCIE | 1F:2 | 0 | **NEWC Interrupt Enable.** Control bit NCIE enables or disables assertion of IRQ and setting of NCIA when NCIA is set by the modem. (See NEWC and NCIA.) |
| NEGDET | 0C:5 | 0 | **Negotiation Frames Detected.** Status bit NEGDET is used to indicate that negotiation frames sent during the V.FC handshake have been detected. (V.FC). |
| NEWC | 1F:0 | 0 | **New Configuration.** Control bit NEWC must be set after the host changes the configuration mode code in the CONF bits or changes any of the following control bits: CEQ, CF17, EQT2, GTE, GTS, L3ACT, LECEN, LL, ORG, RTH, RXV, SFRES, SLEEP, TLVL, TXV, V21S, V23HDX, or V32BS. This informs the modem to implement the new configuration. The DSP resets the NEWC bit when the configuration change is implemented. |
| NEWS | 1F:3 | – | **New Status.** Status bit NEWS is used to indicate one or more status bits located in registers 0A–0F, 1A, or 1B have changed state, or a DSP RAM read or write has been completed. The host may mask the effect of individual status bits upon NEWS by writing mask values to DSP RAM. |
| NRZIEN | 04:2 | 0 | **NRZI Enable.** Control bit NRZIEN is used to enable NRZI transmitter encoding and receiver decoding in synchronous and HDLC modes. When NRZIEN = 0, NRZ is used. |
| NSIA | 1F:7 | – | **NEWS Interrupt Active.** Status bit NSIA is used to indicate NEWS bit caused IRQ to be asserted when enabled by the NSIE bit. (See NEWS and NSIE.) |
| NSIE | 1F:4 | 0 | **NEWS Interrupt Enable.** Control bit NSIE enables or disables assertion of IRQ when NEWS is set by the modem. (See NEWS and NSIA.) |
| NV25 | 09:7 | 0 | **No V.25 Answer Tone.** Control bit NV25 is used to disable transmission of the 2100 Hz CCITT answer tone when a handshake sequence is initiated. (V.FC, V.32 bis, V.32, V.22 bis, V.22, V.23, V.21) |
| OE | 0A:3 | 0 | **Overrun Error.** Status bit OE is used to indicate that the RBUFFER was loaded from the RXA input before the host read the old data from RBUFFER in asynchronous mode or HDLC synchronous parallel mode. |
| ORG | 09:4 | 0 | **Originate.** Control bit ORG selects either originate or answer mode. |
| P2DET | 0D:7 | 0 | **P2 Sequence Detected.** Status bit P2DET is used to indicate the receiver is detecting the P2 portion of the training sequence. (V.17, V.29, V.27 ter) |
| PARSL | 11:5, 6 | 00 | **Parity Select.** Control bits PARSL select the method (stuff, space, even, or odd parity) by which parity is generated and checked during the asynchronous parallel data mode (ASYN = 1). |
| PE | 0A:5 | 0 | **Parity Error.** Status bit PE is used to indicate that a character with bad parity was received in the asynchronous mode or bad CRC was detected in the HDLC synchronous parallel mode. |

**Table 9. Interface Memory Bit Definitions (Cont'd)**

| Mnemonic | Memory Location | Default Value | Name/Description |
|---|---|---|---|
| PEN | 06:3 | 0 | **Parity Enable.** Control bit PEN enables or disables parity in asynchronous mode. (V.FC, V.32 bis, V.32, V.22, V.22 bis, Bell 212A) |
| PNDET | 0D:6 | – | **PN Sequence Detected.** Status bit PNDET is used to indicate the receiver is detecting the PN portion of the training sequence. (V.17, V.29, V.27 ter) |
| PNSUC | 0A:7 | 0 | **PN Success.** Status bit PNSUC is used to indicate that the receiver has successfully trained at the end of the PN portion of the high speed training sequence. (V.17, V.29, V.27 ter) |
| PROBED | 0C:7 | 0 | **Probing Complete.** Status bit PROBED is used to indicate that V.FC probing is complete and the modem is analyzing the results. (V.FC). |
| RA | 07:1 | 0 | **Relay A Activate.** Control bit RA activates or turns off the $\overline{\text{OHRC}}$ output. |
| RB | 04:7 | 0 | **Relay B Activate.** Control bit RB activates or turns off the $\overline{\text{TALK}}$ output. |
| RBUFFER | 00:0–7 | – | **Receive Data Buffer.** The host obtains channel data from the modem receiver in the parallel data mode by reading a data byte from the RBUFFER. |
| RDBF | 1E:0 | – | **Receive Data Buffer Full.** Status bit RDBF is used to signify that the receiver wrote valid data into RBUFFER. This condition can also cause IRQ to be asserted. (See RDBIE and RDBIA.) |
| RDBIA | 1E:6 | – | **Receive Data Buffer Interrupt Active.** When the receive data buffer interrupt is enabled (by RDBIE) and RBUFFER is written to by the modem (RDBF is set), the modem asserts IRQ and sets RDBIA to indicate that RDBF being set caused the interrupt. (See RDBF and RDBIE.) |
| RDBIE | 1E:2 | 0 | **Receive Data Buffer Interrupt Enable.** Control bit RDBIE is used to enable the modem to assert IRQ and set the RDBIA bit when RDBF is set by the modem. (See RDBF and RDBIA.) |
| RDL | 07:6 | 0 | **Remote Digital Loopback.** Control bit RDL is used to cause the modem to initiate a V.22 bis request for the remote modem to go into digital loopback. (V.22 bis, Bell 212A/1200) |
| RDLE | 07:7 | 1 | **Remote Digital Loopback Response Enable.** Control bit RDLE is used to enable the modem to respond to another modem's remote digital loopback request, thus going into loopback. (V.22 bis) |
| RDWK | 15:5 | 1 | **Ring Detect Wake up.** Control bit RDWK is used to enable the modem to wake up from sleep mode when incoming ring signal is detected on the RINGD pin. (See SLEEP bit.) |
| RI | 0F:3 | – | **Ring Indicator.** Status bit RI is used to indicate a ringing signal is being detected. Ringing is detected if pulses are present on the RINGD input in the 15 Hz–68 Hz frequency range. The decision bounds are host programmable in DSP RAM. |
| RIEN | 1A:6 | 0 | **RION Enable.** When control bit is a 1, the RI output will reflect the RION bit. When a 0, the RI output follows the ringing signal on the RINGD input. |
| RION | 1A:5 | 0 | **Ring Indicator On.** Control bit RION determines the state of the $\overline{\text{RI}}$ output (1 = low; 0 = high) when bit RIEN is set and the DATA bit is reset. |
| RLSD | 0F:7 | – | **Received Line Signal Detector.** Status bit RLSD is used to indicate that the receiver has completed receiving the training sequence or has detected energy above threshold, and is receiving data. |
| RLSDE | 03:4 | 1 | **RLSD Enable.** Control bit RLSDE is used to enable the $\overline{\text{RLSD}}$ pin to either reflect the RLSD bit state or to be clamped OFF regardless of the state of the RLSD bit. |
| RREDT | 0E:5 | – | **Rate Renegotiation Detected.** Status bit RREDT indicates rate renegotiation sequence detection status. (V.FC, V.32 bis, V.32) |
| RREN | 15:2 | 0 | **Rate Renegotiation.** Control bit RREN is used to initiate a rate negotiation sequence when the modem is in data mode. (V.FC, V.32 bis) |
| RRTSE | 09:1 | 0 | **Remote RTS Signalling Enable.** Control bit RRTSE is used to enable remote RTS signalling by sending either a pattern (idle pattern) produced by scrambling a binary 1 with the polynomial $1+x^{-3}+x^{-7}$ (RTS OFF) or a pattern of 8 bits (turn-on pattern) produced by scrambling a binary 0 with the polynomial $1+x^{-3}+x^{-7}$ (RTS ON) followed by the user data. |
| RSEQ | 0C:0 | 0 | **Rate Sequence Received.** Status bit RSEQ is used to indicate the 16-bit rate sequence included in the start-up procedure has been received and the 16-bit rate sequence word is available in DSP RAM. (V.FC, V.32 bis, V.32) |

**Table 9. Interface Memory Bit Definitions (Cont'd)**

| Mnemonic | Memory Location | Default Value | Name/Description |
|---|---|---|---|
| RTDET | 0E:7 | – | **Retrain Detector.** RTDET indicates the training sequence detection status. This bit parallels the operation of the ACDET, AADET, or S1DET bit. (V.FC, V.32 bis, V.32, or V.22 bis). |
| RTDIS | 06:7 | 0 | **Receiver Training Disable.** Control bit RTDIS is used to prevent the receiver from recognizing a training sequence and entering the training state. (V.17, V.29, V.27 ter) |
| RTH | 13:2,3 | 0 | **Receiver Threshold.** The RTH control bits select the receiver energy detector threshold:<br>RTH / RLSD ON / RLSD OFF<br>0 / – 43 dBm / – 48 dBm<br>1 / – 33 dBm / – 38 dBm<br>2 / – 26 dBm / – 31 dBm<br>3 / – 16 dBm / – 21 dBm |
| RTRN | 08:1 | 0 | **Retrain.** Control bit RTRN is used to initiate a retrain sequence. (V.FC, V.32 bis, V.32 or V.22 bis) |
| RTS | 08:0 | 0 | **Request to Send.** Control bit RTS is used to enable the modem to transmit any data on TXD when CTS becomes active. The RTS bit parallels the operation of the $\overline{RTS}$ hardware control input. These inputs are ORed by the modem. (See CTS and DTR bits.)<br>In V.22 bis, V.22, V.23, V.21, and Bell 103 constant carrier, and in V.FC, V.32 bis, and V.32 modes, RTS controls data transmission and DTR controls the carrier.<br>In V.22 bis and V.22 controlled carrier mode, RTS independently controls the carrier when DTR is ON.<br>In V.21, V.23 and Bell 103 controlled carrier modes, RTS independently controls the carrier when DTR is ON. When RTS is turned ON, CTS is turned ON per Table 2. |
| RTSDE | 02:3 | 0 | **Remote RTS Pattern Detector Enable.** Control bit RTSDE enables or disables the remote RTS pattern detector in the receiver. (See RTSDT). |
| RTSDT | 0F:1 | – | **Remote RTS Pattern Detected.** Status bit RTSDT indicates the remote RTS signal is either ON or OFF. This status bit is valid only when RTSDE is set. |
| RXFNE | 0C:1 | - | **Receiver FIFO Not Empty.** Status bit RXFNE is used to indicate that the receiver FIFO contains one or more bytes of data. (TPDM = 1, FIFOEN = 1) |
| RXHF | 01:1 | 0 | **Receiver FIFO Half Full.** Status bit RXHF is used to indicate when there are 8 or more bytes in the receiver FIFO buffer. |
| RXP | 01:0 | 0 | **Received Parity Bit.** The RXP is used to indicate the received parity when parity is enabled and word size is set for 8 bits per character. |
| RXV | 11:3 | 0 | **Receive Voice.** Control bit RXV is used to enable the modem to provide voice samples in the Voice Receive Buffer (VBUFR). (Configuration codes 80, 81, and 83) |
| S1DET | 0D:5 | – | **S1 Detector.** S1DET indicates the V.22 bis S1 sequence detection status. (V.22 bis) |
| S511 | 02:5 | 0 | **Send 511.** Control bit S511 is used to instruct the modem to generate and transmit a 511 pattern in the current configuration. (Synchronous modes only.) |
| SADET | 0D:2 | – | **Scrambled Alternating Sequence Detector.** Status bit SADET is used to indicate that scrambled alternating data is being received during an automatic rate change sequence. (V.22 bis) |
| SCIBE | 1A:1 | – | **Secondary Channel Input Buffer Empty.** Status bit SCIBE is used to indicate that the secondary channel transmit buffer (SECTXB) is empty. (See SECEN.) (V.FC/V.32 bis/V.32) |
| SCOBF | 1A:2 | – | **Secondary Channel Output Buffer Full.** Status bit SCOBF is used to indicate that the secondary channel receive buffer (SECRXB) is full. (See SECEN.) (V.FC/V.32 bis, V.32) |
| SCR1 | 0D:4 | – | **Scrambled Ones Detector.** SCR1 indicates the V.22 bis scrambled 1s detection status during handshake. (V.22 bis, V.22, Bell 212) |
| SDET | 0C:3 | – | **S Detector.** SDET indicates the S sequence detection status. (V.FC, V.32 bis, V.32) |
| SDIS | 03:2 | 0 | **Scrambler Disable.** Control bit SDIS disables or enables the transmitter scrambler circuit. |

**Table 9. Interface Memory Bit Definitions (Cont'd)**

| Mnemonic | Memory Location | Default Value | Name/Description |
|---|---|---|---|
| SECEN | 1A:0 | 0 | **Secondary Channel Enable.** Control bit SECEN enables or disables the secondary channel. (V.FC at 19200 bps or above or V.32 bis/V.32 at 7200 bps or above.) |
| SECRXB | 16:0-7 | – | **Secondary Receive Buffer.** The host obtains secondary channel data from the modem receiver by reading a data byte from the SECRXB when bit SCOBF is set. (V.FC/V.32 bis, V.32) |
| SECTXB | 17:0-7 | – | **Secondary Transmit Buffer.** The host conveys secondary channel output data to the transmitter by writing a data byte to the SECTXB when bit SCIBE is set. (V.FC/V.32 bis, V.32)<br>In the transmit voice mode with the FIFO not enabled, SECTXB contains the low byte and VBUFT contains the high byte of the transmit voice sample. (See TXV and FIFOEN.) (Voice transmit mode). |
| SEPT | 03:6 | 0 | **Short Echo Protector Tone.** Control bit SEPT selects 30 ms or 185 ms echo protector tone. (V.17, V.29, V.27 ter) |
| SFRES | 1A:7 | 0 | **Soft Reset.** Control bit SFRES is used to enable power-on reset processing. Bit NEWC will automatically be reset to a 0 by the modem upon completion of the reset processing. |
| SLEEP | 15:7 | 0 | **Sleep Mode.** Control bit SLEEP is used to command the modem into sleep mode. If both RDWK and HWRWK are reset, only a power-on reset will bring the modem out of sleep mode. |
| SNDET | 0C:2 | – | **S Negative Detector.** SNDET indicates the $\overline{S}$ sequence detection status. (V.FC, V.32 bis, V.32) |
| SPEED | 0E:0–3 | – | **Speed Indication.** The SPEED bits contain a code indicating the receiver's data rate at the completion of a handshake. |
| SQDIS | 02:6 | 0 | **Squarer Disable (Tone Detector C).** Control bit SQDIS is used to disable the squarer in front of tone detector C thus cascading prefilter and filter C to create an 8th-order filter. |
| SRCEN | 03:5 | 0 | **Secondary Rate Change Enable.** Control bit SRCEN is used to initiate a rate change request over the secondary channel. |
| STB | 06:2 | 0 | **Stop Bit Number.** Control bit STB selects one or two stop bits in asynchronous mode. (V.FC, V.32 bis, V.32, V.22, V.22 bis, Bell 212A) |
| STOFF | 05:1 | 0 | **Soft Turn Off.** Control bit STOFF is used to enable the transmitter to send one of the following mark frequency turn-off tones at the end of a transmission.<br>Configuration / Frequency (Hz) / Duration (ms)<br>V.23/1200 / 900 / 7<br>V.21 Originate / 880 / 30<br>V.21 Answer / 1550 / 30<br>Bell 103 Originate / 1370 / 30<br>Bell 103 Answer / 2325 / 30 |
| STRN | 04:0 | 0 | **Short Train Select.** Control bit STRN selects long or short training mode. (V.17, V.27 ter) |
| SYNCD | 0A:0 | 0 | **Sync Pattern Detected.** Status bit SYNCD is used to indicate that HDLC flags (7E pattern) are being detected in HDLC synchronous parallel mode. |
| TBUFFER | 10:0–7 | 00 | **Transmit Data Buffer.** The host conveys output data to the transmitter in the parallel mode by writing a data byte to the TBUFFER. Parallel data mode is available in both synchronous and asynchronous modes. The data is transmitted bit 0 first. |
| TDE | 02:7 | 1 | **Tone Detectors Enable.** Control bit TDE enables or disables tone detectors A, B, and C. |
| TDBE | 1E:3 | – | **Transmit Data Buffer Empty.** Status bit TDBE is used to signify that the transmitter has read TBUFFER and the host can write new data into TBUFFER. This condition can also cause IRQ to be asserted. The host writing to TBUFFER resets the TDBE and TDBIA bits. |
| TDBIA | 1E:7 | – | **Transmit Data Buffer Interrupt Active.** When the transmit data buffer interrupt is enabled (TDBIE is set) and register 10 is empty (TDBE is set), the modem asserts IRQ and sets status bit TDBIA to indicate that TDBE being set caused the interrupt. The host writing to register 10 resets the TDBIA bit and clears the interrupt request due to TDBE. (See TDBIE and TDBE.) |
| TDBIE | 1E:5 | 0 | **Transmit Data Buffer Interrupt Enable.** When control bit TDBIE is set (interrupt enabled), the modem will assert IRQ and set the TDBIA bit when TDBE is set by the modem. When TDBIE is reset (interrupt disabled), TDBE has no effect on IRQ or TDBIA. (See TDBE and TDBIA.) |
| TEOF | 11:1 | 0 | **HDLC Transmit End of Frame.** Control bit TEOF is used to inform the modem of the last data byte in the frame. (HDLC = 1, TPDM = 1, FIFOEN = 1) |

**Table 9. Interface Memory Bit Definitions (Cont'd)**

| Mnemonic | Memory Location | Default Value | Name/Description |
|---|---|---|---|
| TLVL | 13:4–7 | 9 | **Transmit Level.** The TLVL code selects the transmitter analog output level at the TXA pin. The output can vary from 0 ±0.5 dBm (TLVL = 0) to -15 ±0.5 dBm (TLVL = F) in steps of 1 dB. The host can fine tune the transmit level within a 1 dB step by changing a value in DSP RAM. |
| TM | 0F:2 | – | **Test Mode.** Status bit TM is used to indicate that the modem has completed the handshake and is in RDL test mode. (V.22 bis, V.22, Bell 212A) |
| TOD | 04:1 | 0 | **Train On Data.** Control bit TOD is used to enable the train-on-data algorithm to converge the equalizer if the signal quality degrades to a BER of $10^{-3}$ for 0.5 seconds. (V.32 bis, V.32, V.29, V.27, V.17) |
| TONEA | 0B:7 | – | **Tone A Detected.** Status bit TONEA is used to indicate that energy is present on the line within the tone detector A passband and above its threshold. The tone A, B, and C bandpass filter coefficients are host programmable in DSP RAM. |
| TONEB | 0B:6 | – | **Tone B Detected.** Status bit TONEB is used to indicate that energy is present on the line within the tone detector B passband and above its threshold. |
| TONEC | 0B:5 | – | **Tone C Detected.** Status bit TONEC is used to indicate that energy is present on the line within the tone detector C passband and above its threshold. |
| TPDM | 08:6 | 0 | **Transmitter Parallel Data Mode.** Control bit TPDM is used to select transmitter parallel data mode in which the modem accepts data for transmission from the TBUFFER (register 10) rather than the TXD input. (See TDBE.) |
| TTDIS | 05:2 | 0 | **Transmitter Training Disable.** Control bit TTDIS is used to inhibit the modem transmitter from generating the training sequence at the start of transmission. (V.17, V.29, V.27 ter) |
| TXCLK | 13:0,1 | 0 | **Transmit Clock Select.** The TXCLK control bits designate the origin of the transmitter data clock to be internal, external (XTCLK), or slave (RDCLK). |
| TXFNF | 0D:1 | - | **Transmitter FIFO Not Full.** Status bit TXFNF is used to indicate that the transmitter FIFO is not full and that the host may continue to write data to the TX FIFO. (TPDM = 1, FIFOEN = 1) |
| TXHF | 01:2 | 0 | **Transmitter FIFO Half Full.** Status bit TXHF is used to indicate when there are 8 or more bytes in the transmitter FIFO buffer. |
| TXP | 11:0 | 0 | **Transmit Parity Bit (or 9th Data Bit).** The TXP contains the stuffed parity bit (or 9th data bit) for transmission when parity is enabled, stuff parity is selected, and word size is set for 8 bits per character (see PEN, PARSL, and WDSZ bits). |
| TXSQ | 05:4 | 0 | **Transmitter Squelch.** Control bit TXSQ enables or disables squelching of the transmitter output. |
| TXV | 11:4 | 0 | **Transmit Voice.** Control bit TXV is used to enable the modem to accept voice samples from VBUFT when the FIFO is enabled or from VBUFT (high byte) and SECTXB (low byte) when the FIFO is not enabled. (See FIFOEN.) (Configuration codes 80, 81, and 83) |
| U1DET | 0D:3 | – | **Unscrambled 1s Detector.** U1DET indicates the V.22 bis unscrambled 1s sequence detection status. (V.22 bis) |
| V21S | 08:5 | 0 | **V21 Synchronous.** Control bit V21S selects synchronous or asynchronous mode in V.21. |
| V23HDX | 11:2 | 0 | **V.23 Half Duplex.** Control bit V23HDX selects half-duplex or full-duplex operation in V.23. |
| V32BDT | 0E:4 | – | **V.32 bis Rate Sequence Detected.** V32BDT indicates the V.32 bis rate sequence detection status. (V.32 bis, V.32) |
| V32BS | 04:5 | 1 | **V.32 bis Select.** Control bit V32BS selects V.32 bis or V.32 operation. (V.FC, V.32 bis ) |
| V32DIS | 0B:1 | – | **V.32 Disconnect Detect.** Status bit V32DIS is used to indicate that a line disconnection has occurred and the modem has synchronized on its own transmit signal. (V.FC, V.32 bis, V.32) |
| V54A | 08:3 | 0 | **V.54 Acknowledgment Signalling.** Control bit V54A is used to enable sending of a pattern of 1948 bits produced by scrambling a binary 1 with the polynomial $1+x^{-4}+x^{-7}$ per V.54 at the modem data signalling rate. (Not valid in FSK modes.) |
| V54AE | 02:1 | 0 | **V.54 Acknowledgment Phase Detector Enable.** Control bit V54AE enables or disables the V.54 acknowledgment phase detector in the receiver. (See V54DT). (Not valid in FSK modes.) |

**Table 9. Interface Memory Bit Definitions (Cont'd)**

| Mnemonic | Memory Location | Default Value | Name/Description |
|---|---|---|---|
| V54DT | 0F:0 | 0 | **V.54 Pattern Detected.** Status bit V54DT is used to indicate that one of the three V.54 patterns is being detected. (Not valid in FSK modes.) |
| V54P | 08:2 | 0 | **V.54 Preparatory Signalling.** Control bit V54P is used to enable the sending of a pattern of 2048 bits produced by scrambling a binary 0 with the polynomial $1+x^{-4}+x^{-7}$ per V.54 at the modem data signalling rate. (Not valid in FSK modes.) |
| V54PE | 02:0 | 0 | **V.54 Preparatory Phase Detector Enable.** Control bit V54PE enables or disables the V.54 preparatory phase detector in the receiver. (Not valid in FSK modes.) |
| V54T | 08:4 | 0 | **V.54 Termination Signalling.** Control bit V54T is used to enable the sending of a pattern of 8192 bits produced by scrambling a binary 1 with the polynomial $1+x^{-4}+x^{-7}$ followed by 64 binary 1s per V.54 at the modem signalling rate. (Not valid in FSK modes.) |
| V54TE | 02:2 | 0 | **V.54 Termination Phase Detector Enable.** Control bit V54TE enables or disables the V.54 termination phase detector in the receiver. (See V54DT). (Not valid in FSK modes.) |
| VBUFR | 00:0-7 | – | **Voice Receive Buffer.** In voice receive mode, VBUFR contains one of two consecutive bytes of the 16-bit output voice sample. The first byte read is the low byte: the second byte read is the high byte. (See RXV.) (Receive voice only.) |
| VBUFT | 10:0-7 | – | **Voice Transmit Buffer.** When the FIFO is enabled in the voice transmit mode, VBUFT contains one of two consecutive bytes of the 16-bit input voice sample. The first byte written is the low byte; the second byte written is the high byte.<br>When the FIFO is not enabled in the voice transmit mode, VBUFT contains the high byte of the 16-bit input voice sample while SECTXB contains the low byte of the 16-bit input voice sample. (See TXV and FIFOEN.) (Transmit voice only.) |
| VOLUME | 01:6,7 | 0 | **Volume Control.** Two-bit encoded speaker volume field selects volume off or one of three volume on levels. |
| WDSZ | 06:0,1 | 0 | **Data Word Size.** The WDSZ bits select a word size of 5, 6, 7, or 8 data bits per character in asynchronous mode. (V.FC, V.32 bis, V.32, V.22, V.22 bis, Bell 212A) |

## MODEM INTERFACE CIRCUIT

Recommended modem interface connections to the modem packaged in a 68-pin PLCC are shown in Figure 4.

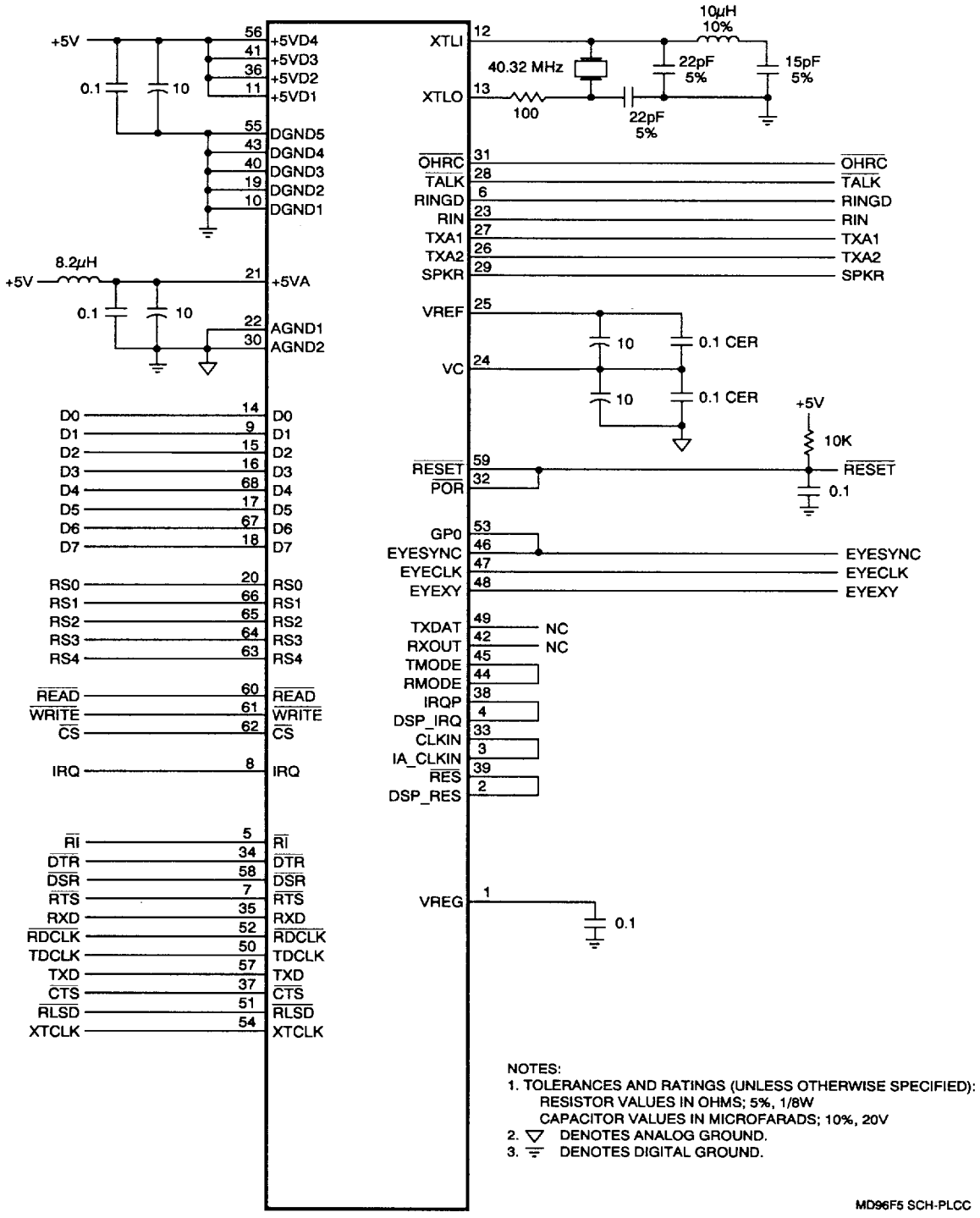


**Figure 4. Typical Interface to Modem in PLCC**