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RC10-XX

Sense Resistors for Fairchild Semiconductor DC-DC Controllers

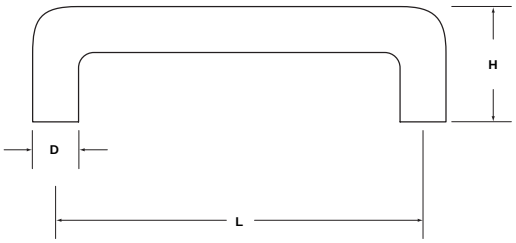
Features

- Resistor typical tolerance ± 5%
- Resistance wire TCR +20ppm/C
- Wire alloy MnCu (0.624mΩ/mm)

Sense Resistor Selection

CPU Type	CPU I_{MAX}	Fairchild Semiconductor Controller	Fairchild Semiconductor Sense Resistor Part Number
Socket 7: P54C, P55C, K6, M2	10A	RC5036	RC10-58
		RC5041 RC5050 RC5051	RC10-73
	13A	RC5036	RC10-44
		RC5041 RC5050 RC5051	RC10-58
Pentium Pro Pentium II Klamath Pentium II Deschutes	13A	RC5050 RC5051	RC10-58
	15A	RC5050 RC5051	RC10-52
	18A	RC5050 RC5051	RC10-44

Resistor Dimensions



Type	R (mΩ)	D (mm)	L (mm)	H (mm)
RC10-58	5.8	1.0	9.3	5.0
RC10-73	7.3	1.0	11.7	5.0
RC10-52	5.2	1.0	8.3	5.0
RC10-44	4.4	1.0	7.1	5.0

Preliminary Information

Preliminary Information

System Requirements

The design of the sense resistor is driven by the following system requirements:

- Load current, (I_{LOAD}). This is the full load DC current the converter is designed to support.
- The controller short circuit current detect threshold voltage (V_{TH}), which for Fairchild Semiconductor family of Controllers is specified at 120+/-20mV for the RC5040, RC5041, RC5042, RC5050, and RC5051, or 90 ±10mV for the RC5036.
- The inductor current ripple (I_R). A reasonable design guideline is to assume the current ripple is limited to 1.5A.

Design Equations

The design of the sense resistor must consider carefully the output requirements during normal operation and during a fault condition. If the sense resistor is too high, it may develop enough voltage drop accross it to trip the short circuit detect circuitry so that the DC-DC converter may not be able to deliver the maximum required load current. If the sense resistor is too low, the controller may not be disabled when a certain safe amount of load current is exceeded, thus the power dissipation within the MOSFET(s) may rise to destructive levels.

The design equations used to calculate the sense resistor are as follows:

$$I_{SC(MIN)} = (I_{LOAD} + I_R + 1)$$

$$R_{SENSE(MAX)} = \frac{V_{TH(MIN)}}{I_{SC(MIN)}}$$

and, assuming a 10% tolerance, the nominal design value of the sense resistor is given by:

$$R_{SENSE} = \frac{R_{SENSE(MAX)}}{(1 + 0.10)}$$

Wire Sense Resistors

There are several types of sense resitors available to the system designer in a wide range of cost and specifications.

The resistors with higher precision (i.e. 1% SMT) demand the highest cost (i.e. $0.47); however a 10% to 15% tolerance is adequate for most DC-DC converters designs and wire resistors offer a very cost effective alternative.

MnCu or CuNi alloy wire resistors have been used extensively in the manufacture of sense resistors used in the Fairchild Semiconductor's family of DC-DC converters.

These resistive wires are available in all the most common gages and Table 1 and Table 2 describe the specifications of MnCu and CuNi alloys for various wire diameters.

Wire with diameter of ~1 mm is best suited to make sense resistors for DC-DC converters used in motherboard applications. Refer to Figure 1 for the typical shape of a wire sense resistor and Figure 2 through Figure 5 for the dimensions of the resistor as function of the load current requirements of the converter.

Table 1. MnCu Wire Resistor Specifications

Diameter (mm)	Ω/m	mΩ/mm	Imax (Amp)
1.40	0.31831	0.318	154
1.30	0.36916	0.369	133
1.10	0.51561	0.516	95
1.00	0.62389	0.624	79
0.90	0.77023	0.770	64
0.80	0.97482	0.975	50

Note:
1. $J = 10^4$ A/cm^2

Table 2. CiNi Wire Resistor Specifications

AWG	Diameter (mm)	Ω/ft	mΩ/m	Imax (Amp)
15	1.45	0.09049	0.30	165
16	1.29	0.11300	0.37	131
17	1.15	0.14520	0.48	104
18	1.02	0.18370	0.60	82
19	0.912	0.22690	0.74	65
20	0.812	0.28710	0.94	52

Note:
1. $J = 10^4$ A/cm^2

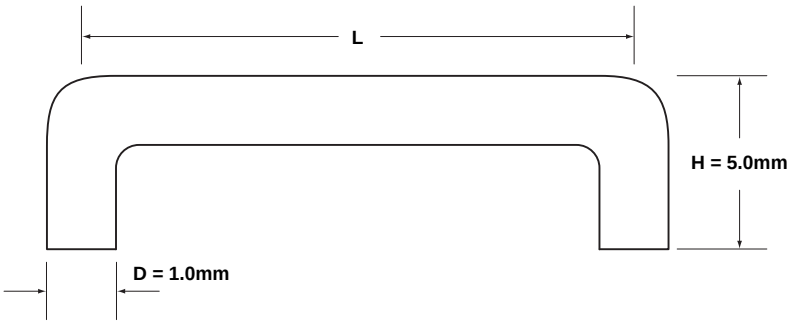


Figure 1. Wire Resistor

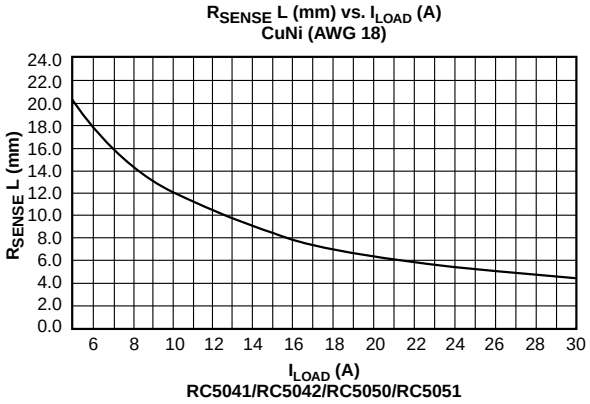


Figure 2. Rsense vs. Imax (CuNi)

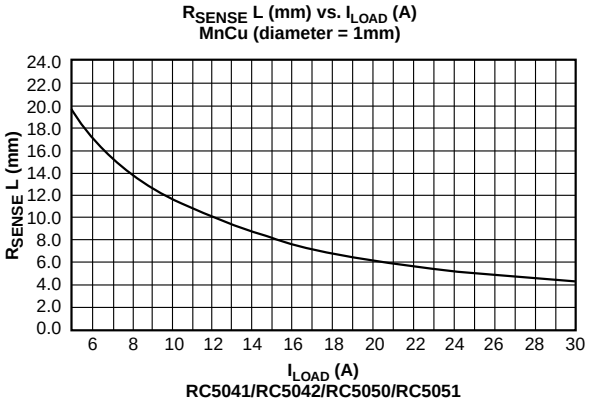


Figure 3. Rsense vs. Imax (MnCu)

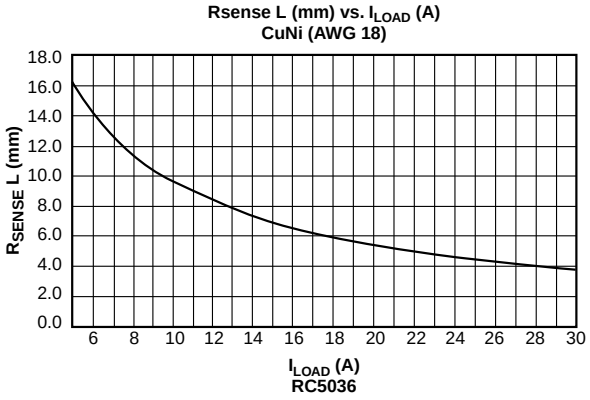


Figure 4. Rsense vs. Imax (CuNi)

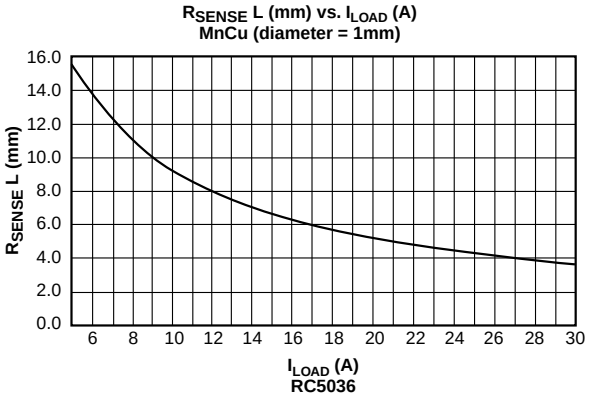


Figure 5. Rsense vs. Imax (MnCu)

Preliminary Information

Preliminary Information

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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RC1117

1A Adjustable/Fixed Low Dropout Linear Regulator

Features

- Low dropout voltage
- Load regulation: 0.05% typical
- Trimmed current limit
- On-chip thermal limiting
- Standard SOT-223 and TO-263 packages
- Three-terminal adjustable or fixed 2.5V, 2.85V, 3.3V, 5V

Applications

- Active SCSI terminators
- High efficiency linear regulators
- Post regulators for switching supplies
- Battery chargers
- 5V to 3.3V linear regulators
- Motherboard clock supplies

Description

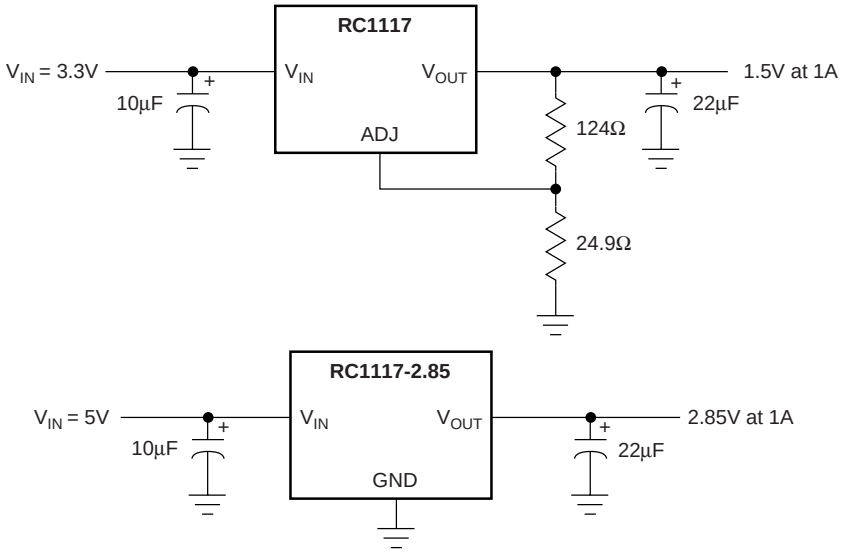
The RC1117 and RC1117-2.5, -2.85, -3.3 and -5 are low dropout three-terminal regulators with 1A output current capability. These devices have been optimized for low voltage where transient response and minimum input voltage are critical. The 2.85V version is designed specifically to be used in Active Terminators for SCSI bus.

Current limit is trimmed to ensure specified output current and controlled short-circuit current. On-chip thermal limiting provides protection against any combination of overload and ambient temperatures that would create excessive junction temperatures.

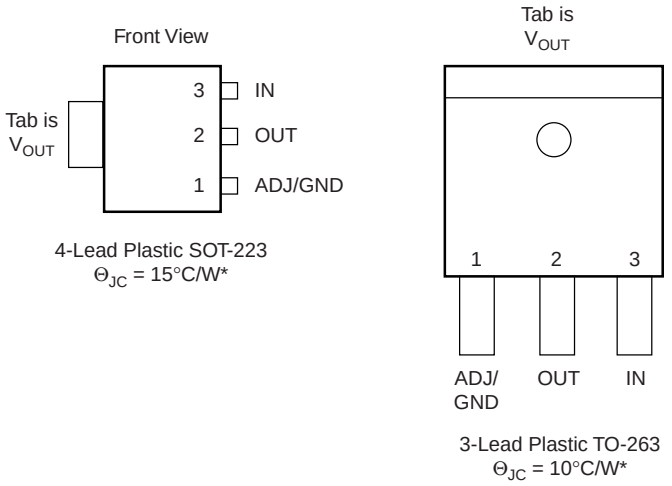
Unlike PNP type regulators where up to 10% of the output current is wasted as quiescent current, the quiescent current of the RC1117 flows into the load, increasing efficiency.

The RC1117 series regulators are available in the industry-standard SOT-223 and TO-263 power packages.

Typical Applications



Pin Assignments



*With package soldered to 0.5 square inch copper area over backside ground plane or internal power plane., Θ_{JA} can vary from 30°C/W to more than 50°C/W. Other mounting techniques may provide better thermal resistance than 30°C/W.

Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
V_{IN}		7.5	V
Operating Junction Temperature Range	0	125	°C
Storage Temperature Range	-65	150	°C
Lead Temperature (Soldering, 10 sec.)		300	°C

Electrical Characteristics

Operating Conditions: $V_{IN} \leq 7V$, $T_J = 25°C$ unless otherwise specified.

The • denotes specifications which apply over the specified operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
Reference Voltage[3]	$1.5V \leq (V_{IN} - V_{OUT}) \leq 5.75V$, $10mA \leq I_{OUT} \leq 1A$	•	1.225 (-2%)	1.250	1.275 (+2%)	V
Output Voltage	$10mA \leq I_{OUT} \leq 1A$					
	RC1117-2.5, $4V \leq V_{IN} \leq 7V$	•	2.450	2.5	2.550	V
	RC1117-2.85, $4.35V \leq V_{IN} \leq 7V$	•	2.793	2.85	2.907	V
	RC1117-3.3, $4.8V \leq V_{IN} \leq 7V$	•	3.234	3.3	3.366	V
	RC1117-5, $6.5V \leq V_{IN} \leq 7V$	•	4.900	5.0	5.100	V
Line Regulation[1,2]	$(V_{OUT} + 1.5V) \leq V_{IN} \leq 7V$, $I_{OUT} = 10mA$	•		0.005	0.2	%
Load Regulation[1,2]	$(V_{IN} - V_{OUT}) = 2V$, $10mA \leq I_{OUT} \leq 1A$	•		0.05	0.5	%
Dropout Voltage	$\Delta V_{REF} = 1\%$, $I_{OUT} = 1A$	•		1.100	1.200	V
Current Limit	$(V_{IN} - V_{OUT}) = 2V$	•	1.1	1.5		A
Adjust Pin Current[3]		•		35	120	µA
Adjust Pin Current Change[3]	$1.5V \leq (V_{IN} - V_{OUT}) \leq 5.75$, $10mA \leq I_{OUT} \leq 1A$	•		0.2	5	µA
Minimum Load Current	$1.5V \leq (V_{IN} - V_{OUT}) \leq 5.75$	•	10			mA
Quiescent Current	$V_{IN} = V_{OUT} + 1.25V$	•		4	13	mA
Ripple Rejection	f = 120Hz, C_{OUT} = 22µF Tantalum, $(V_{IN} - V_{OUT}) = 3V$, $I_{OUT} = 1A$		60	72		dB
Thermal Regulation	$T_A = 25°C$, 30ms pulse			0.004	0.02	%/W
Temperature Stability		•		0.5		%
Long-Term Stability	$T_A = 125°C$, 1000hrs.			0.03	1.0	%
RMS Output Noise (% of V_{OUT})	$T_A = 25°C$, $10Hz \leq f \leq 10kHz$			0.003		%
Thermal Resistance, Juncation to Case	SOT-223			15		°C/W
	TO-263			10		°C/W
Thermal Shutdown	Junction Temperature			155		°C
Thermal Shutdown Hysteresis				10		°C

Notes:

1. See thermal regulation specifications for changes in output voltage due to heating effects. Load and line regulation are measured at a constant junction temperature by low duty cycle pulse testing.
2. Line and load regulation are guaranteed up to the maximum power dissipation (18W). Power dissipation is determined by input/output differential and the output current. Guaranteed maximum output power will not be available over the full input/output voltage range.
3. RC1117 only.

Typical Performance Characteristics

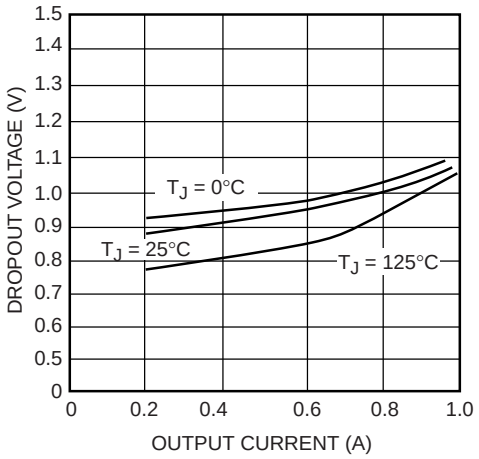


Figure 1. Dropout Voltage vs. Output Current

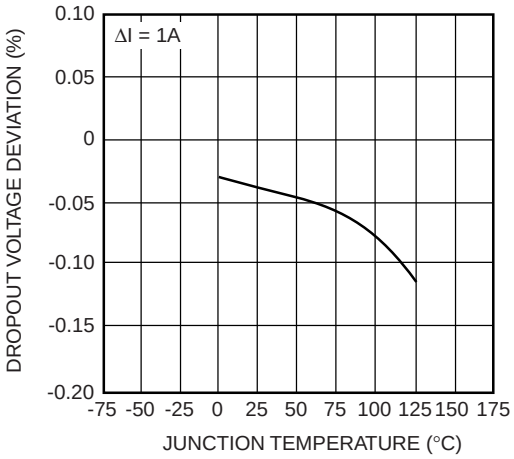


Figure 2. Load Regulation vs. Temperature

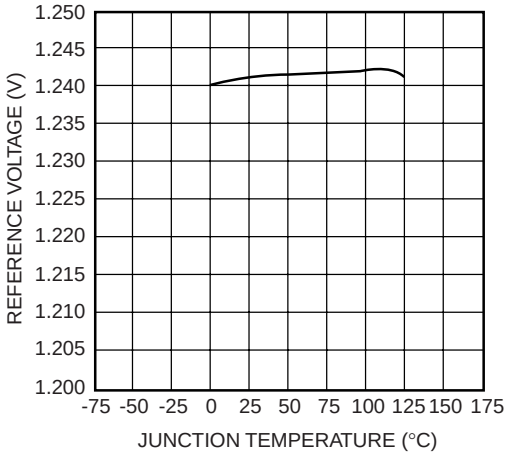


Figure 3. Reference Voltage vs. Temperature

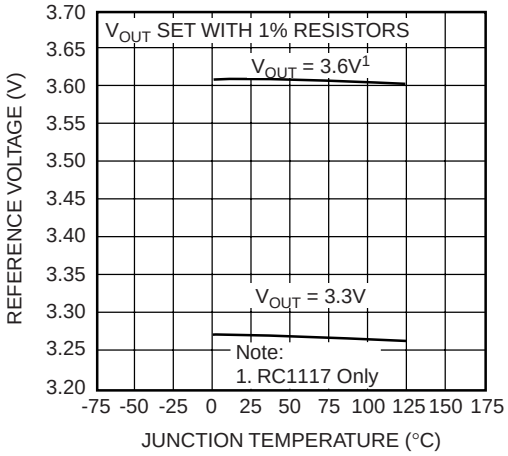


Figure 4. Output Voltage vs. Temperature

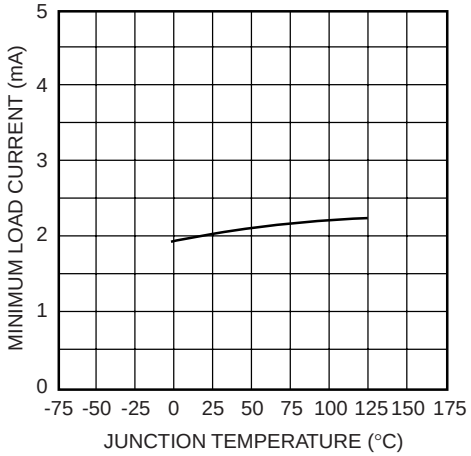


Figure 5. Minimum Load Current vs. Temperature

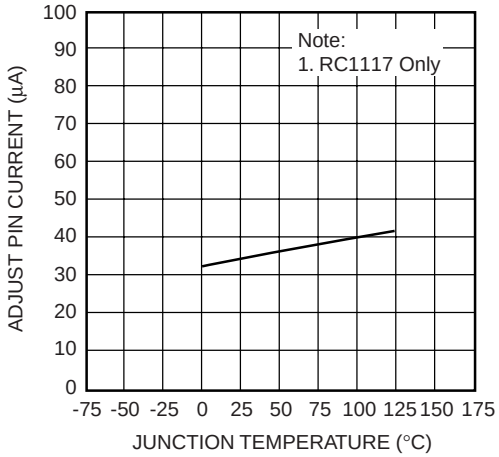


Figure 6. Adjust Pin Current vs. Temperature

Typical Performance Characteristics (continued)

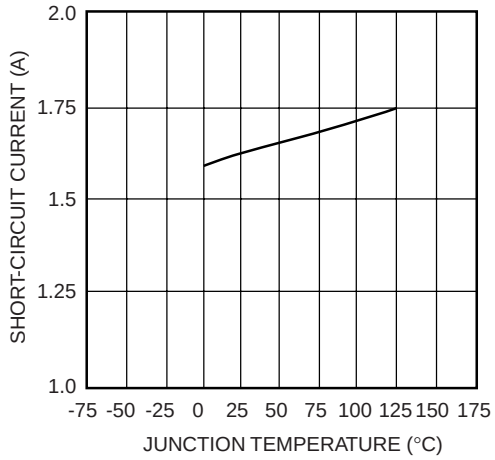


Figure 7. Short-Circuit Current vs. Temperature

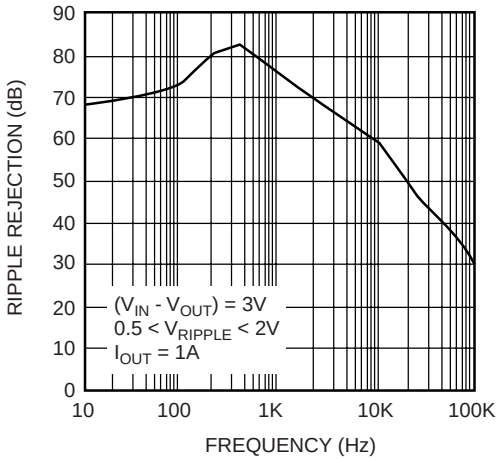


Figure 8. Ripple Rejection vs. Frequency

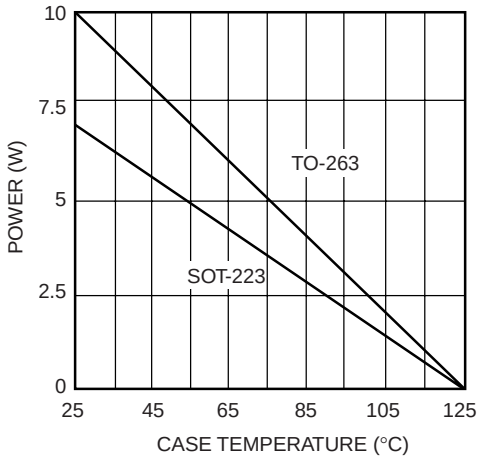


Figure 9. Maximum Power Dissipation

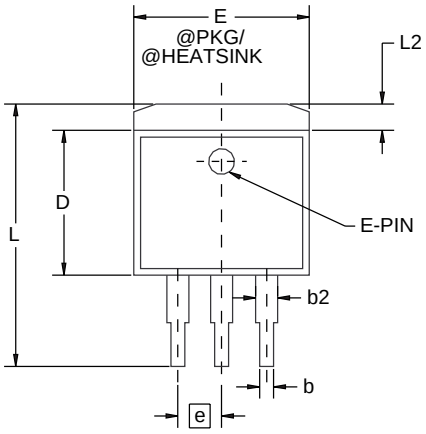
Mechanical Dimensions

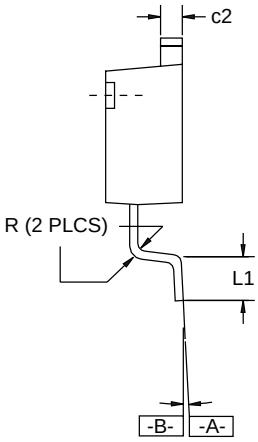
3-Lead TO-263 Package

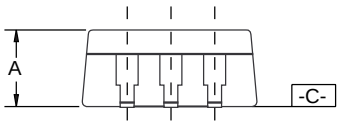
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.160	.190	4.06	4.83	
b	.020	.039	0.51	0.99	
b2	.049	.051	1.25	1.30	
c2	.045	.055	1.14	1.40	
D	.340	.380	8.64	9.65	
E	.380	.405	9.65	10.29	
e	.100 BSC		2.54 BSC		
L	.575	.625	14.61	10.88	
L1	.090	.100	2.29	2.79	
L2	—	.055	—	1.40	
R	.017	.019	0.43	0.48	
α	0°	8°	0°	8°	

Notes:

1. Dimensions are exclusive of mold flash and metal burrs.
2. Stand off-height is measured from lead tip with ref. to Datum -B-.
3. Foot length is measured with ref. to Datum -A- with lead surface (at inner R).
4. Dimension exclusive of dambar protrusion or intrusion.
5. Formed leads to be planar with respect to one another at seating place -C-.



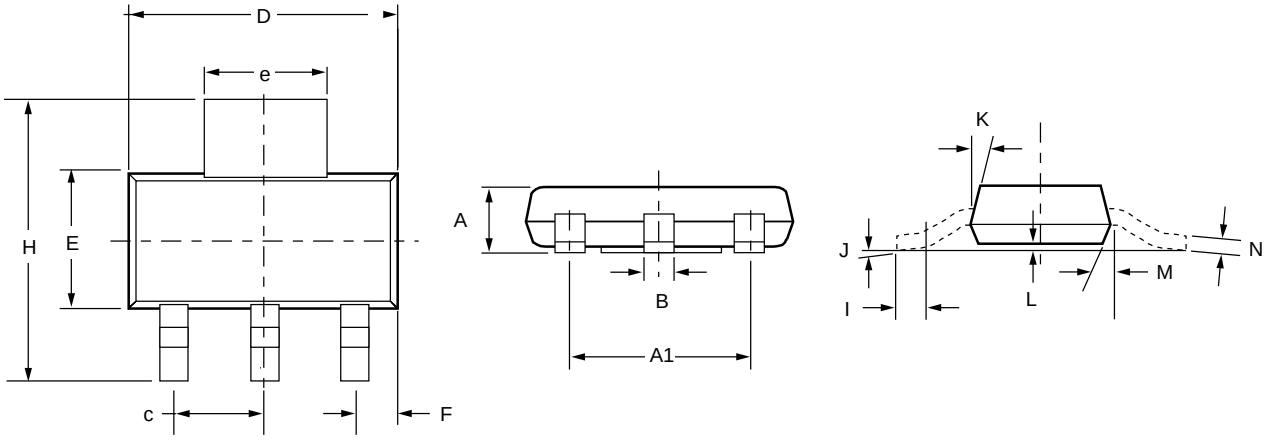




Mechanical Dimensions

4-Lead SOT-223 Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.071	—	1.80	
A1	—	.181	—	4.80	
B	.025	.033	.640	.840	
c	—	.090	—	2.29	
D	.248	.264	6.30	6.71	
E	.130	.148	3.30	3.71	
e	.115	.124	2.95	3.15	
F	.033	.041	.840	1.04	
H	.264	.287	6.71	7.29	
I	.012	—	.310	—	
J	—	10°	—	10°	
K	10°	16°	10°	16°	
L	.0008	.0040	.0203	.1018	
M	10°	16°	10°	16°	
N	.010	.014	.250	.360	



Ordering Information

Product Number	Package
RC1117M	TO-263
RC1117S	SOT-223
RC1117M-2.5	TO-263
RC1117S-2.5	SOT-223
RC1117M-2.85	TO-263
RC1117S-2.85	SOT-223
RC1117M-3.3	TO-263
RC1117S-3.3	SOT-223
RC1117M-5	TO-263
RC1117S-5	SOT-223

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SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

RC1584

7A Adjustable/Fixed Low Dropout Linear Regulator

Features

- Fast transient response
- Low dropout voltage at up to 7A
- Load regulation: 0.05% typical
- Trimmed current limit
- On-chip thermal limiting
- Standard TO-220, TO-263 and TO-263 center cut packages

Applications

- Pentium® Class GTL+ bus supply
- Low voltage logic supply
- Post regulator for switching supply

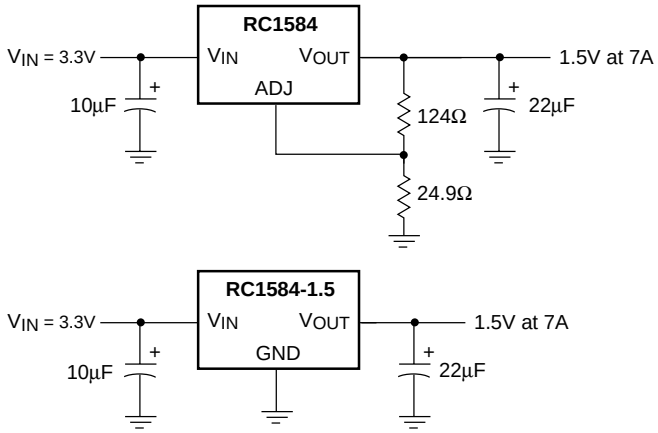
Description

The RC1584 and RC1584-1.5 are low dropout three-terminal regulators with 7A output current capability. These devices have been optimized for low voltage applications including V_{TT} bus termination, where transient response and minimum input voltage are critical. The RC1584 is ideal for low voltage microprocessor applications requiring a regulated output from 1.5V to 3.6V with an input supply of 5V or less. The RC1584-1.5 offers fixed 1.5V with 7A current capability for GTL+ bus V_{TT} termination.

Current limit is trimmed to ensure specified output current and controlled short-circuit current. On-chip thermal limiting provides protection against any combination of overload and ambient temperature that would create excessive junction temperatures.

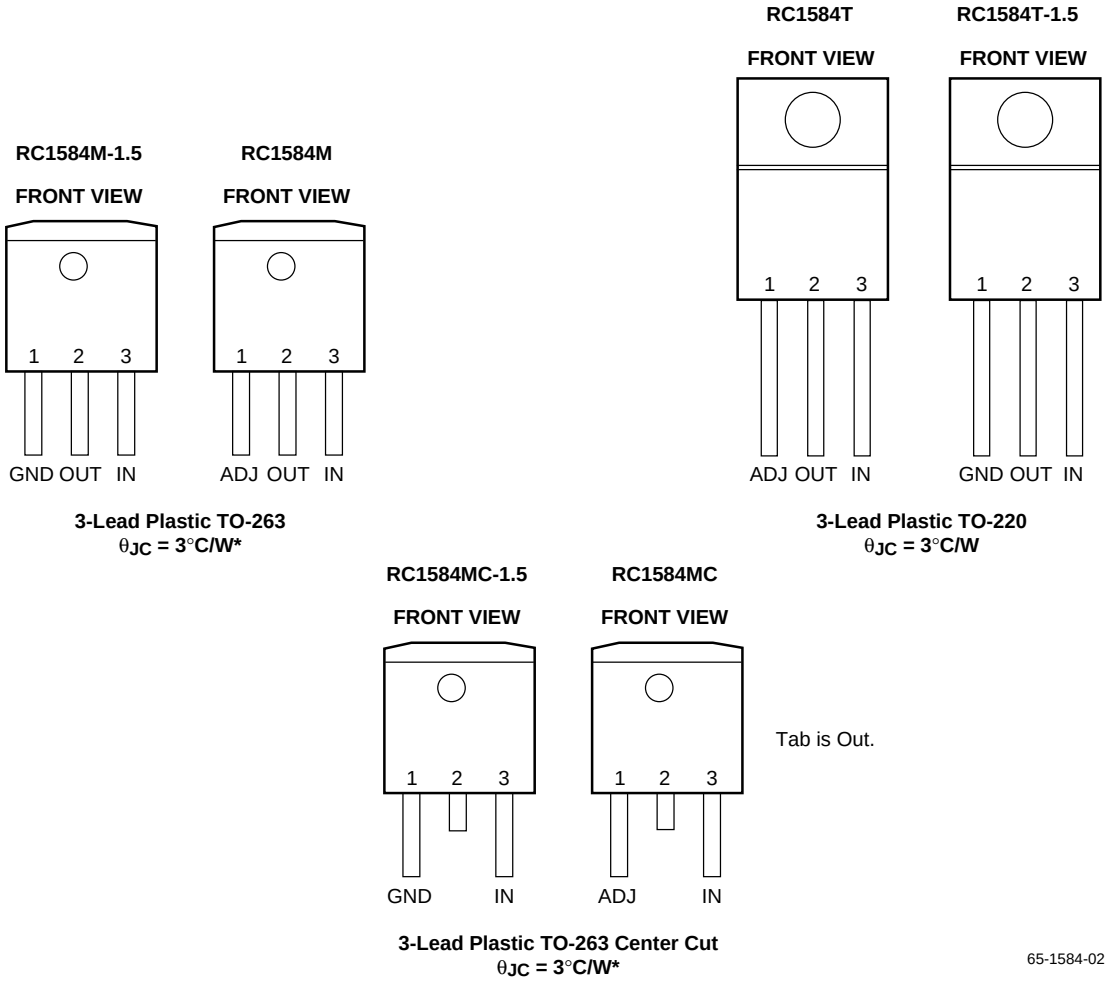
The RC1584 and RC1584-1.5 are available in the industry-standard TO-220, TO-263 and TO-263 center cut power packages.

Typical Applications



Pentium is a registered trademark of Intel Corporation.

Pin Assignments



* θ_{JA} can vary from 20°C/W to >40°C/W with various mounting techniques.

Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
V_{IN}		7	V
Operating Junction Temperature Range	0	125	°C
Storage Temperature Range	-65	150	°C
Lead Temperature (Soldering, 10 sec.)		300	°C

Electrical Characteristics

Tj = 25°C unless otherwise specified.

The • denotes specifications which apply over the specified operating temperature range.

Parameter	Conditions		Min.	Typ.	Max	Units
Reference Voltage[3]	$1.5V \le (V_{IN} - V_{OUT}) \le 5.75V$, $10mA \le I_{OUT} \le 7A$	•	1.225 (-2%)	1.250	1.275 (+2%)	V
Output Voltage[4]	$3.3V \le V_{IN} \le 7V$ $10mA \le I_{OUT} \le 7A$	•	1.47	1.5	1.53	V
Line Regulation[1, 2]	$(V_{OUT} + 1.5V) \le V_{IN} \le 7V$, $I_{OUT} = 10mA$	•		0.005	0.2	%
Load Regulation[1, 2]	$(V_{IN} - V_{OUT}) = 3V$ $10mA \le I_{OUT} \le 7A$	•		0.05	0.5	%
Dropout Voltage	$\Delta V_{REF} = 1\%$, $I_{OUT} = 7A$	•		1.150	1.300	V
Current Limit	$(V_{IN} - V_{OUT}) = 2V$	•	7.1	8		A
Adjust Pin Current[3]		•		35	120	µA
Adjust Pin Current Change[3]	$1.5V \le (V_{IN} - V_{OUT}) \le 5.75V$, $10mA \le I_{OUT} \le 7A$	•		0.2	5	µA
Minimum Load Current	$1.5V \le (V_{IN} - V_{OUT}) \le 5.75V$	•	10			mA
Quiescent Current	$V_{IN} = 5V$	•		4	13	mA
Ripple Rejection	f = 120Hz, C_{OUT} = 22µF Tantalum, $(V_{IN} - V_{OUT}) = 3V$, $I_{OUT} = 7A$		60	72		dB
Thermal Regulation	$T_A = 25°C$, 30ms pulse			0.004	0.02	%/W
Temperature Stability		•		0.5		%
Long-Term Stability	$T_A = 125°C$, 1000 hrs.			0.03	1.0	%
RMS Output Noise (% of V_{OUT})	$T_A = 25°C$, $10Hz \le f \le 10kHz$			0.003		%
Thermal Resistance, Junction to Case	TO-220			3		°C/W
	TO-263			3		°C/W
Thermal Shutdown				150		°C

Notes:

1. See thermal regulation specifications for changes in output voltage due to heating effects. Load and line regulation are measured at a constant junction temperature by low duty cycle pulse testing.
2. Line and load regulation are guaranteed up to the maximum power dissipation (18W). Power dissipation is determined by input/output differential and the output currrent. Guaranteed maximum output power will not be available over the full input/ output voltage range.
3. RC1584 only.
4. RC1584-1.5 only.

Typical Performance Characteristics

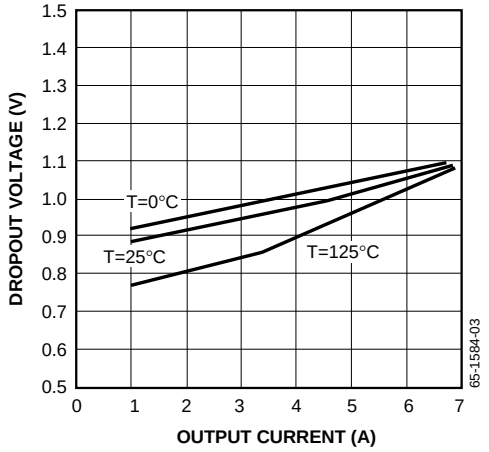


Figure 1. Dropout Voltage vs. Output Current

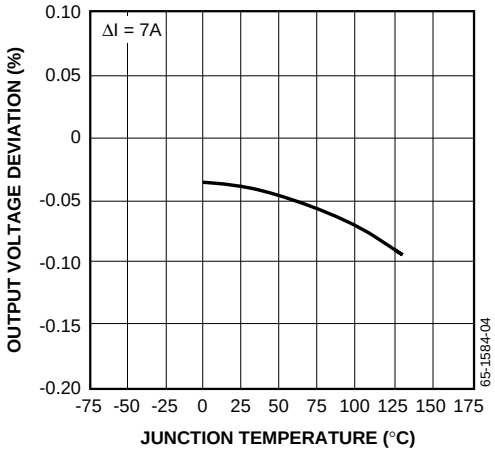


Figure 2. Load Regulation vs. Temperature

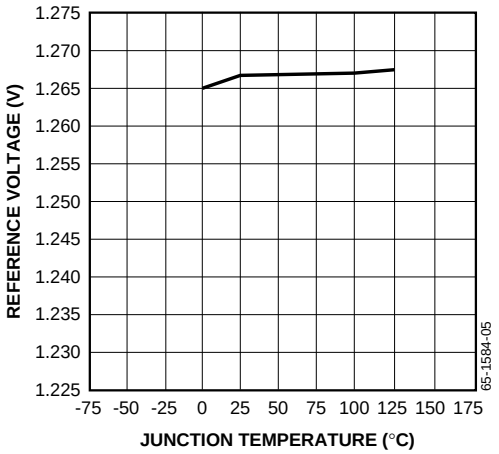


Figure 3. Reference Voltage vs. Temperature

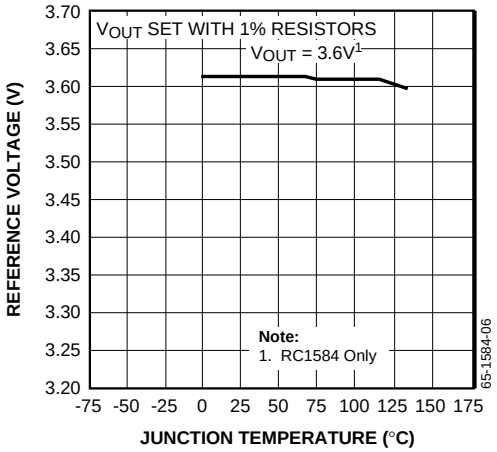


Figure 4. Output Voltage vs. Temperature

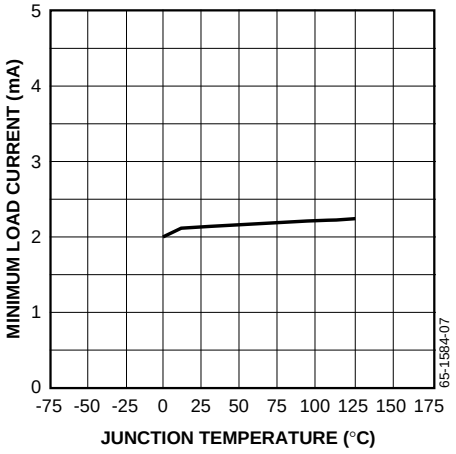


Figure 5. Minimum Load Current vs. Temperature

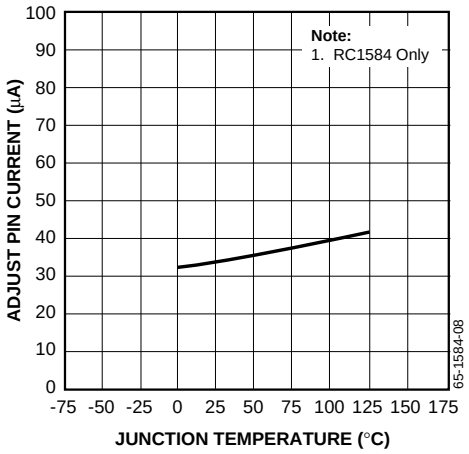


Figure 6. Adjust Pin Current vs. Temperature

Typical Performance Characteristics (continued)

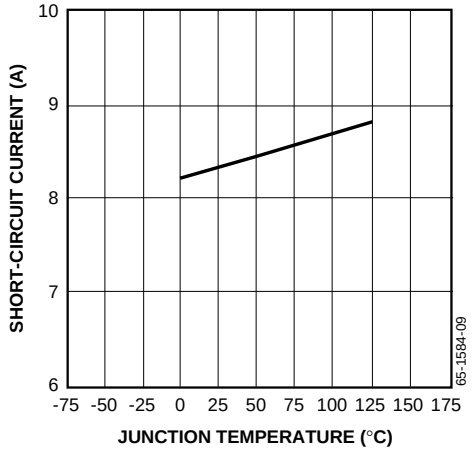


Figure 7. Short-Circuit Current vs. Temperature

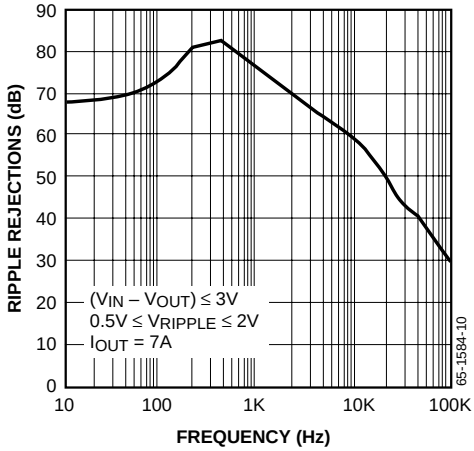


Figure 8. Ripple Rejection vs. Frequency

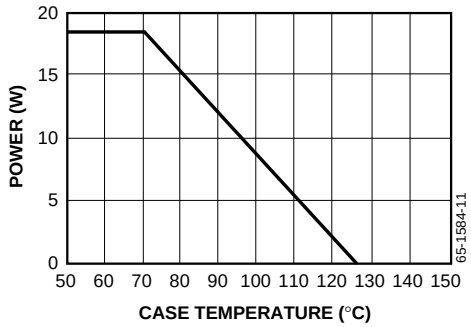


Figure 9. Maximum Power Dissipation

Applications Information

General

The RC1584 and RC1584-1.5 are three-terminal regulators optimized for GTL+ V_{TT} termination applications. These devices are short-circuit protected, and offer thermal shutdown to turn off the regulator when the junction temperature exceeds about 150°C. The RC1584 series provides low dropout voltage and fast transient response. Frequency compensation uses capacitors with low ESR while still maintaining stability. This is critical in addressing the needs of low voltage high speed microprocessor buses like GTL+.

Stability

The RC1584 series require an output capacitor as a part of the frequency compensation. It is recommended to use a 22µF solid tantalum or a 100µF aluminum electrolytic on the output to ensure stability. The frequency compensation of these devices optimizes the frequency response with low ESR capacitors. In general, it is suggested to use capacitors with an ESR of <1Ω. It is also recommended to use bypass capacitors such as a 22µF tantalum or a 100µF aluminum on the adjust pin of the RC1584 for low ripple and fast transient response. When these bypassing capacitors are not used at the adjust pin, larger values of output capacitors provide equally good results.

Protection Diodes

In normal operation, the RC1584 series does not require any protection diodes. For the RC1584, internal resistors limit internal current paths on the adjust pin. Therefore, even with bypass capacitors on the adjust pin, no protection diode is needed to ensure device safety under shortcircuit conditions.

A protection diode between the input and output pins is usually not needed. An internal diode between the input and output pins on the RC1584 series can handle microsecond surge currents of 50A to 100A. Even with large value output capacitors it is difficult to obtain those values of surge currents in normal operation. Only with large values of output capacitance, such as 1000µF to 5000µF, and with the input pin instantaneously shorted to ground can damage occur. A crowbar circuit at the input can generate those levels of current; a diode from output to input is then recommended, as shown in Figure 10. Usually, normal power supply cycling or system “hot plugging and unplugging” will not generate current large enough to do any damage.

The adjust pin can be driven on a transient basis ±7V with respect to the output, without any device degradation. As with any IC regulator, exceeding the maximum input-to-output voltage differential causes the internal transistors to break down and none of the protection circuitry is then functional.

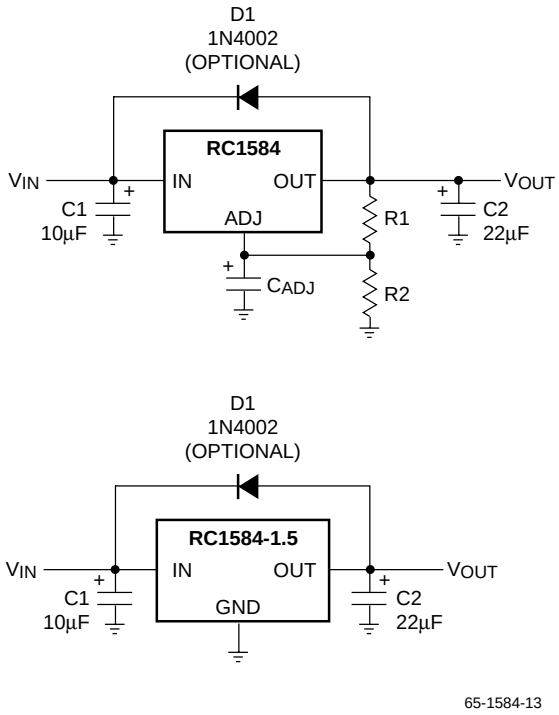


Figure 10. Optional Protection

Ripple Rejection

In applications that require improved ripple rejection, a bypass capacitor from the adjust pin of the RC1584 to ground reduces the output ripple by the ratio of V_{OUT}/1.25V. The impedance of the adjust pin capacitor at the ripple frequency should be less than the value of R1 (typically in the range of 100Ω to 120Ω) in the feedback divider network in Figure 10. Therefore, the value of the required adjust pin capacitor is a function of the input ripple frequency. For example, if R1 equals 100Ω and the ripple frequency equals 120Hz, the adjust pin capacitor should be 22µF. At 10kHz, only 0.22µF is needed.

Output Voltage

The RC1584 regulator develops a 1.25V reference voltage between the output pin and the adjust pin (see Figure 11). Placing a resistor R1 between these two terminals causes a constant current to flow through R1 and down through R2 to set the overall output voltage. Normally, this current is the specified minimum load current of 10mA.

The current out of the adjust pin adds to the current from R1 and is typically 35µA. Its output voltage contribution is small and only needs consideration when very precise output voltage setting is required.

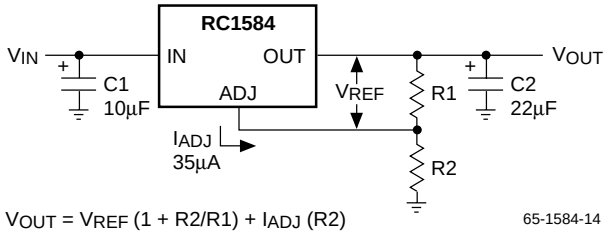


Figure 11. Basic Regulator Circuit

Load Regulation

It is not possible to provide true remote load sensing because the RC1584 series are three-terminal devices. Load regulation is limited by the resistance of the wire connecting the regulators to the load. Load regulation per the data sheet specification is measured at the bottom of the package.

For fixed voltage devices, negative side sensing is a true Kelvin connection with the ground pin of the device returned to the negative side of the load. This is illustrated in Figure 12.

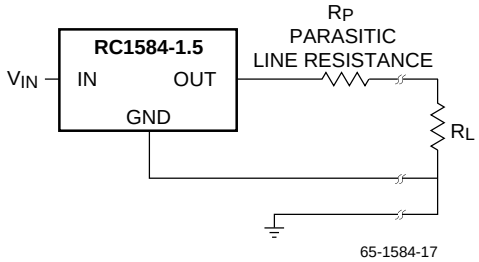


Figure 12. Connection for Best Load Regulation

For adjustable voltage devices, negative side sensing is a true Kelvin connection with the bottom of the output divider returned to the negative side of the load. The best load regulation is obtained when the top of resistor divider R1 connects directly to the regulator output and not to the load. Figure 13 illustrates this point.

If R1 connects to the load, then the effective resistance between the regulator and the load would be:

$R_P \times (1 + R2/R1)$, R_P = Parasitic Line Resistance

The connection shown in Figure 13 does not multiply R_P by the divider ratio. As an example, R_P is about four milliohms per foot with 16-gauge wire. This translates to 4mV per foot at 1A load current. At higher load currents, this drop represents a significant percentage of the overall regulation. It is important to keep the positive lead between the regulator and the load as short as possible and to use large wire or PC board traces.

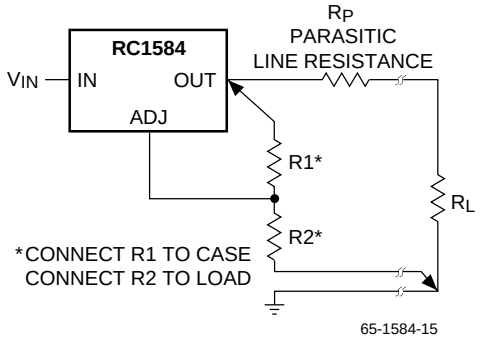


Figure 13. Connection for Best Load Regulation

Thermal Considerations

The RC1584 series protect themselves under overload conditions with internal power and thermal limiting circuitry. However, for normal continuous load conditions, do not exceed maximum junction temperature ratings. It is important to consider all sources of thermal resistance from junction-to-ambient. These sources include the junction-to-case resistance, the case-to-heat sink interface resistance, and the heat sink resistance. Thermal resistance specifications have been developed to more accurately reflect device temperature and ensure safe operating temperatures.

For example, look at using an RC1584T to generate 7A @ 1.5V ± 2% from a 1.8V source (1.71V to 1.89V).

Assumptions:

- V_{IN} = 1.89V worst case
- V_{OUT} = 1.46V worst case
- I_{OUT} = 7A continuous
- T_A = 70°C
- $\theta_{Case\text{-}to\text{-}Ambient}$ = 3°C/W (assuming both a heatsink and a thermally conductive material)

The power dissipation in this application is:

$P_D = (V_{IN} - V_{OUT}) * (I_{OUT}) = (1.89 - 1.46) * (3) = 3.01W$

From the specification table:

$T_J = T_A + (P_D) * (\theta_{Case\text{-}to\text{-}Ambient} + \theta_{JC})$
$= 70 + (3.01) * (3 + 3) = 88°C$

The junction temperature is below the maximum rating.

Junction-to-case thermal resistance is specified from the IC junction to the bottom of the case directly below the die. This is the lowest resistance path for heat flow. Proper mounting ensures the best thermal flow from this area of the package to the heat sink. Use of a thermally conductive material at the case-to-heat sink interface is recommended. Use a thermally conductive spacer if the case of the device must be electrically isolated and include its contribution to the total thermal resistance. The cases of the RC1584 series are directly connected to the output of the device.

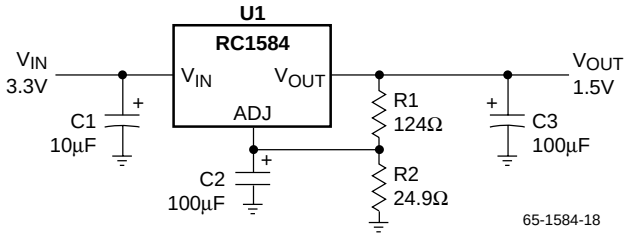


Figure 14. Application Circuit (RC1584)

Table 1. Bill of Materials for Application Circuit for the RC1584

Item	Quantity	Manufacturer	Part Number	Description
C1	1	Xicon	L10V10	10µF, 10V Aluminum
C2, C3	2	Xicon	L10V100	100µF, 10V Aluminum
R1	1	Generic		124Ω, 1%
R2	1	Generic		24.9Ω, 1%
U1	1	Fairchild	RC1584T	7A Regulator

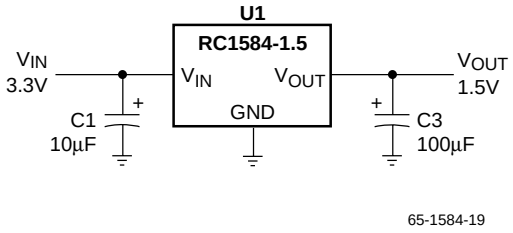


Figure 15. Application Circuit (RC1584-1.5)

Table 2. Bill of Materials for Application Circuit for the RC1584-1.5

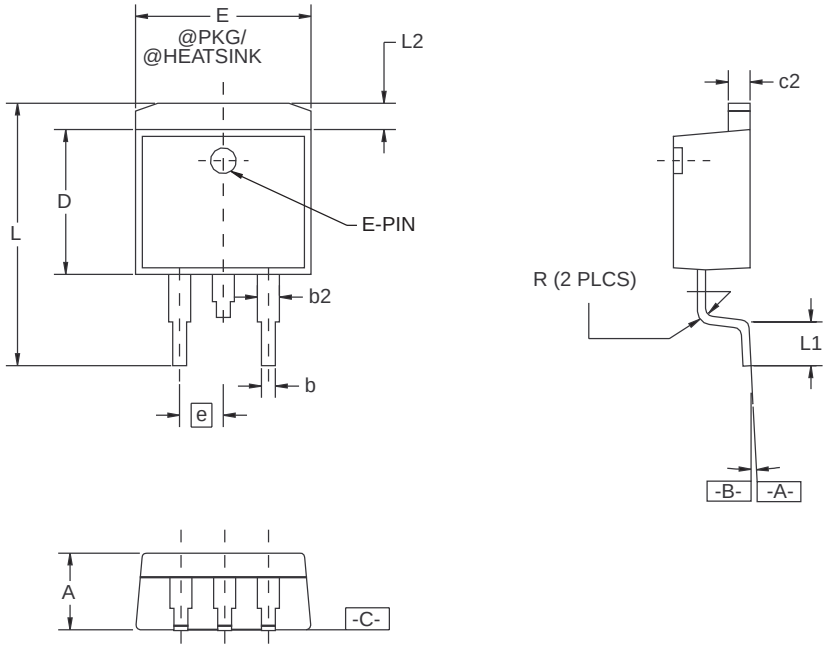
Item	Quantity	Manufacturer	Part Number	Description
C1	1	Xicon	L10V10	10µF, 10V Aluminum
C3	1	Xicon	L10V100	100µF, 10V Aluminum
U1	1	Fairchild	RC1584T-1.5	7A Regulator

Mechanical Dimensions

3-Lead TO-263 Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.160	.190	4.06	4.83	
b	.020	.039	0.51	0.99	
b2	.049	.051	1.25	1.30	
c2	.045	.055	1.14	1.40	
D	.340	.380	8.64	9.65	
E	.380	.405	9.65	10.29	
e	.100 BSC		2.54 BSC		
L	.575	.625	14.61	15.88	
L1	.090	.110	2.29	2.79	
L2	—	.055	—	1.40	
R	.017	.019	0.43	0.78	
α	0°	8°	0°	8°	

Notes:
1. Dimensions are exclusive of mold flash and metal burrs.
2. Standoff-height is measured from lead tip with ref. to Datum -B-.
3. Foot length is measured with ref. to Datum -A- with lead surface (at inner R).
4. Dimensiuon exclusive of dambar protrusion or intrusion.
5. Formed leads to be planar with respect to one another at seating place -C-.

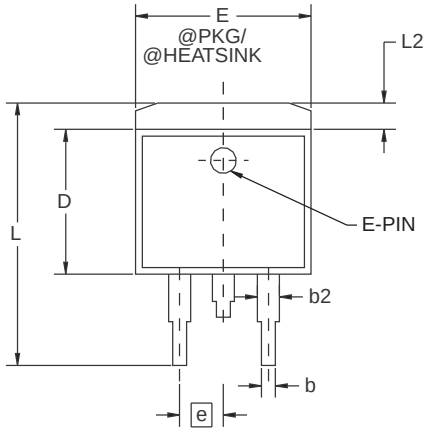


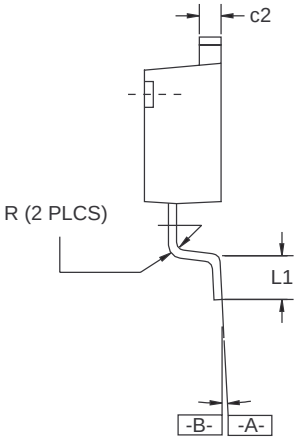
Mechanical Dimensions (continued)

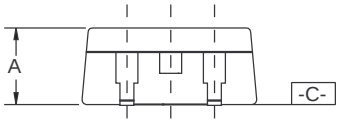
3-Lead TO-263 Center Cut Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.160	.190	4.06	4.83	
b	.020	.039	0.51	0.99	
b2	.049	.051	1.25	1.30	
c2	.045	.055	1.14	1.40	
D	.340	.380	8.64	9.65	
E	.380	.405	9.65	10.29	
e	.100 BSC		2.54 BSC		
L	.575	.625	14.61	15.88	
L1	.090	.110	2.29	2.79	
L2	—	.055	—	1.40	
R	.017	.019	0.43	0.78	
α	0°	8°	0°	8°	

Notes:
1. Dimensions are exclusive of mold flash and metal burrs.
2. Standoff-height is measured from lead tip with ref. to Datum -B-.
3. Foot length is measured with ref. to Datum -A- with lead surface (at inner R).
4. Dimensiuon exclusive of dambar protrusion or intrusion.
5. Formed leads to be planar with respect to one another at seating place -C-.





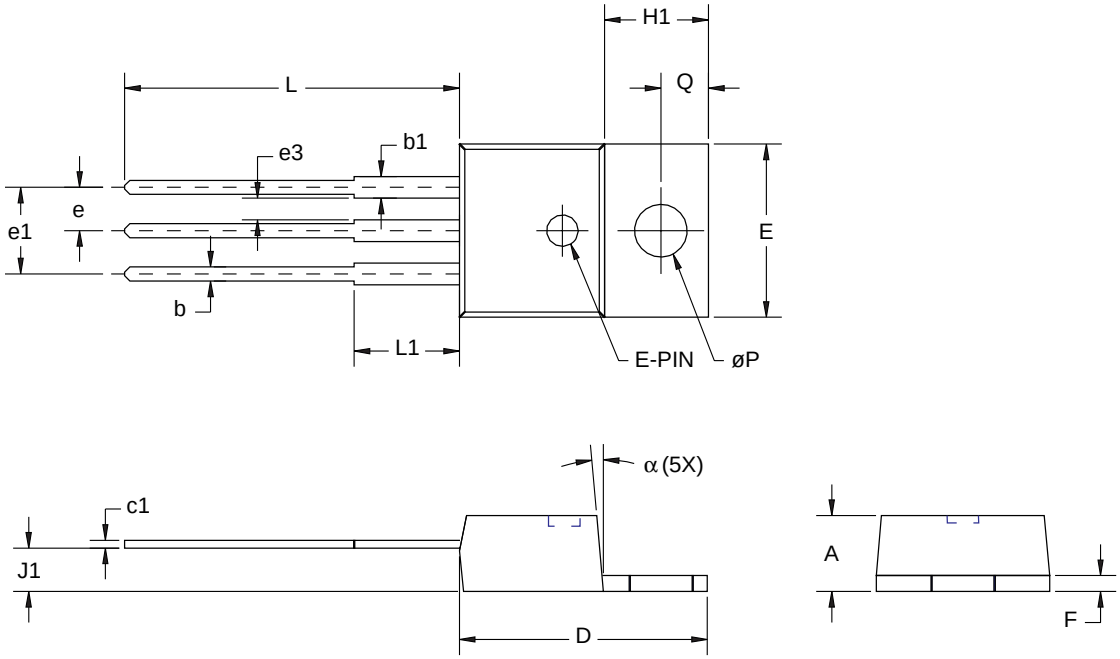


Mechanical Dimensions (continued)

3-Lead TO-220 Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.140	.190	3.56	4.83	
b	.015	.040	.38	1.02	
b1	.045	.070	1.14	1.78	
c1	.014	.022	.36	.56	
øP	.139	.161	3.53	4.09	
D	.560	.650	14.22	16.51	
E	.380	.420	9.65	10.67	
e	.090	.110	2.29	2.79	
e1	.190	.210	4.83	5.33	
e3	.045	—	1.14	—	
F	.020	.055	.51	1.40	
H1	.230	.270	5.94	6.87	
J1	.080	.115	2.04	2.92	
L	.500	.580	12.70	14.73	
L1	.250 BSC		6.35 BSC		
Q	.100	.135	2.54	3.43	
α	3°	7°	3°	7°	

Notes:
1. Dimension c1 apply for lead finish.



Ordering Information

Product Number	Package
RC1584M	TO-263
RC1584MC	TO-263 center cut
RC1584T	TO-220
RC1584M-1.5	TO-263
RC1584MC-1.5	TO-263 center cut
RC1584T-1.5	TO-220

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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

RC1585

5A Adjustable/Fixed Low Dropout Linear Regulator

Features

- Fast transient response
- Low dropout voltage at up to 5A
- Load regulation: 0.05% typical
- Trimmed current limit
- On-chip thermal limiting
- Standard TO-220, TO-263 and TO-263 center cut packages

Applications

- Pentium® class GTL+ bus supply
- Low voltage logic supply
- Post regulator for switching supply

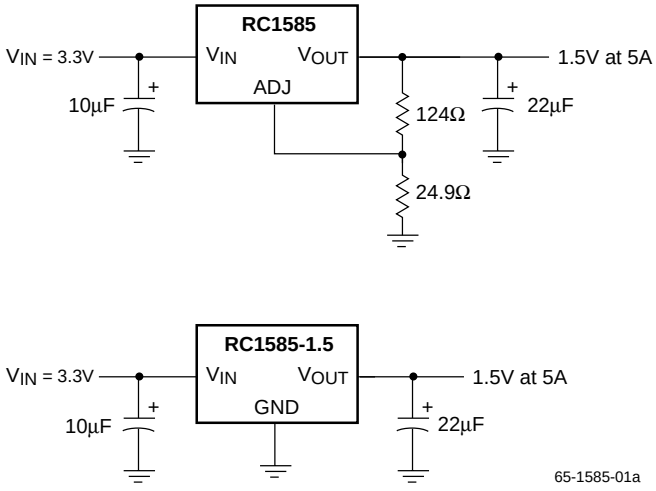
Description

The RC1585 and RC1585-1.5 are low dropout three-terminal regulators with 5A output current capability. These devices have been optimized for low voltage applications including V_{TT} bus termination, where transient response and minimum input voltage are critical. The RC1585 is ideal for low voltage microprocessor applications requiring a regulated output from 1.5V to 3.6V with an input supply of 5V or less. The RC1585-1.5 offers fixed 1.5V with 5A current capabilities for GTL+ bus V_{TT} termination.

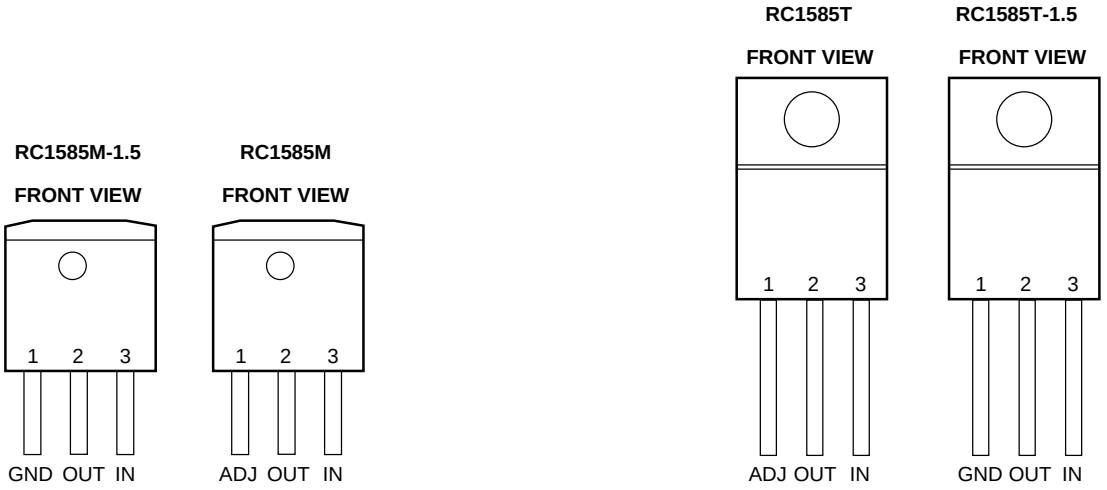
Current limit is trimmed to ensure specified output current and controlled short-circuit current. On-chip thermal limiting provides protection against any combination of overload and ambient temperature that would create excessive junction temperatures.

The RC1585 series regulators are available in the industry-standard TO-220, TO-263 and TO-263 center cut power packages.

Typical Applications

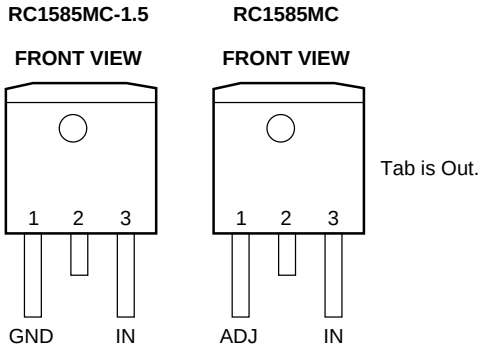


Pin Assignments



3-Lead Plastic TO-263
θ_{JC} = 3°C/W*

3-Lead Plastic TO-220
θ_{JC} = 3°C/W



3-Lead Plastic TO-263 Center Cut
θ_{JA} = 3°C/W*

* θ_{JA} can vary from 20°C/W to >40°C/W with various mounting techniques.

65-1585-02

Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
V_{IN}		7	V
Operating Junction Temperature Range	0	125	°C
Storage Temperature Range	-65	150	°C
Lead Temperature (Soldering, 10 sec.)		300	°C

Electrical Characteristics

Tj = 25°C unless otherwise specified.

The ● denotes specifications which apply over the specified operating temperature range.

Parameter	Conditions		Min.	Typ.	Max	Units
Reference Voltage[3]	1.5V ≤ (V_{IN} – V_{OUT}) ≤ 5.75V, 10mA ≤ I_{OUT} ≤ 5A	•	1.225 (-2%)	1.250	1.275 (+2%)	V
Output Voltage[4]	3V ≤ V_{IN} ≤ 7V 10mA ≤ I_{OUT} ≤ 5A	•	1.47	1.5	1.53	V
Line Regulation[1, 2]	(V_{OUT} + 1.5V) ≤ V_{IN} ≤ 7V, I_{OUT} = 10mA	•		0.005	0.2	%
Load Regulation[1, 2, 3]	(V_{IN} – V_{OUT}) = 3V, 10mA ≤ I_{OUT} ≤ 5A	•		0.05	0.5	%
Dropout Voltage	ΔV_{REF} = 1%, I_{OUT} = 5A	•		1.150	1.300	V
Current Limit	(V_{IN} – V_{OUT}) = 2V	•	5.1	5.5		A
Adjust Pin Current[3]		•		35	120	µA
Adjust Pin Current Change[3]	1.5V ≤ (V_{IN} – V_{OUT}) ≤ 5.75V, 10mA ≤ I_{OUT} ≤ 5A	•		0.2	5	µA
Minimum Load Current	1.5V ≤ (V_{IN} – V_{OUT}) ≤ 5.75V	•	10			mA
Quiescent Current	V_{IN} = 5V	•		4	13	mA
Ripple Rejection	f = 120Hz, C_{OUT} = 22µF Tantalum, (V_{IN} – V_{OUT}) = 3V, I_{OUT} = 5A		60	72		dB
Thermal Regulation	T_A = 25°C, 30ms pulse			0.004	0.02	%/W
Temperature Stability		•		0.5		%
Long-Term Stability	T_A = 125°C, 1000 hrs.			0.03	1.0	%
RMS Output Noise (% of V_{OUT})	T_A = 25°C, 10Hz ≤ f ≤ 10kHz			0.003		%
Thermal Resistance, Junction to Case	TO-220			3		°C/W
	TO-263			3		°C/W
Thermal Shutdown				150		°C

Notes:

1. See thermal regulation specifications for changes in output voltage due to heating effects. Load and line regulation are measured at a constant junction temperature by low duty cycle pulse testing.
2. Line and load regulation are guaranteed up to the maximum power dissipation (18W). Power dissipation is determined by input/output differential and the output currrent. Guaranteed maximum output power will not be available over the full input/ output voltage range.
3. RC1585 only.
4. RC1585-1.5 only.

Typical Performance Characteristics

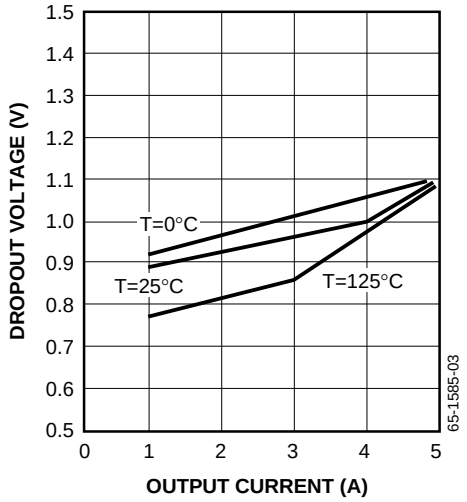


Figure 1. Dropout Voltage vs. Output Current

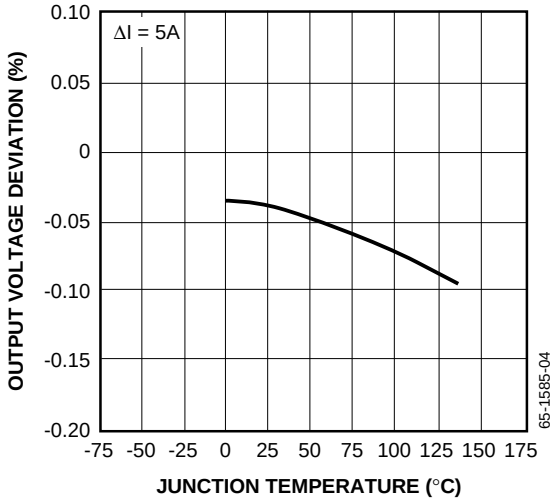


Figure 2. Load Regulation vs. Temperature

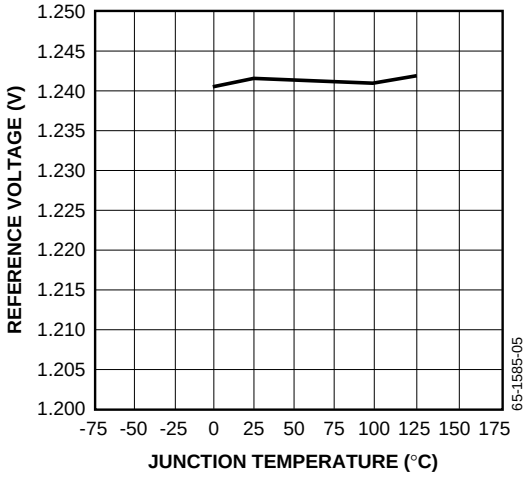


Figure 3. Reference Voltage vs. Temperature

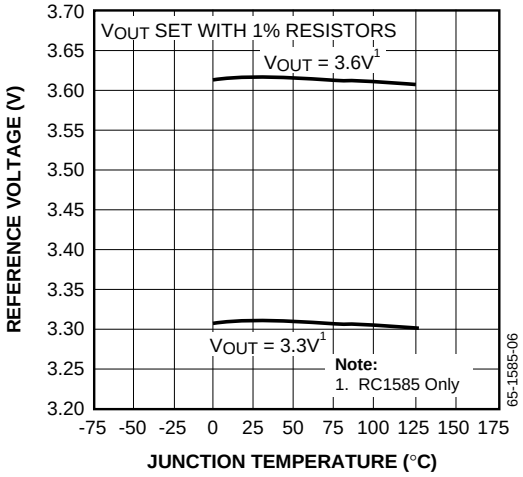


Figure 4. Output Voltage vs. Temperature

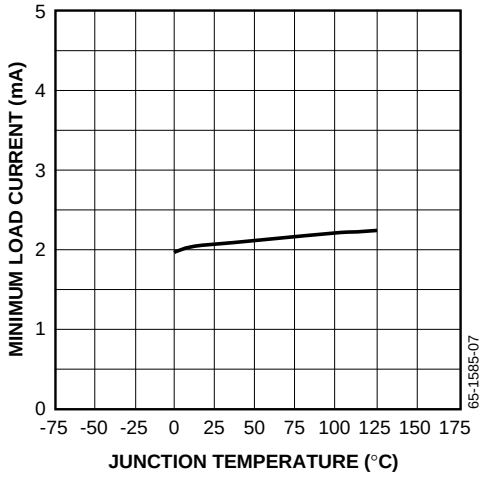


Figure 5. Minimum Load Current vs. Temperature

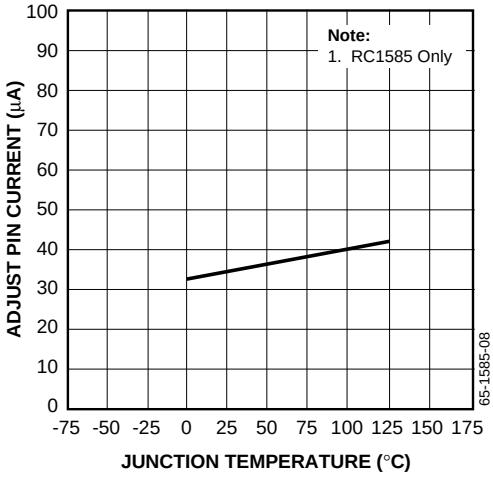


Figure 6. Adjust Pin Current vs. Temperature

Typical Performance Characteristics (continued)

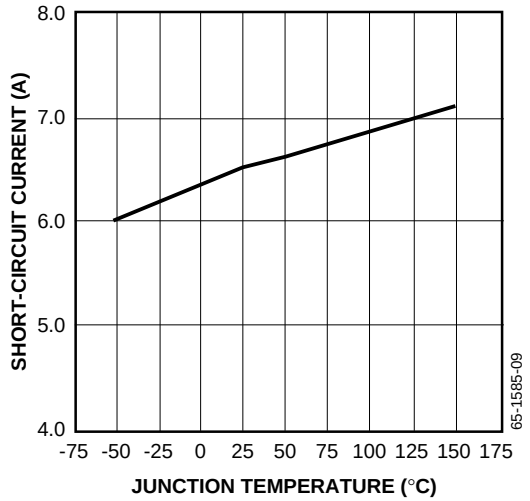


Figure 7. Short-Circuit Current vs. Temperature

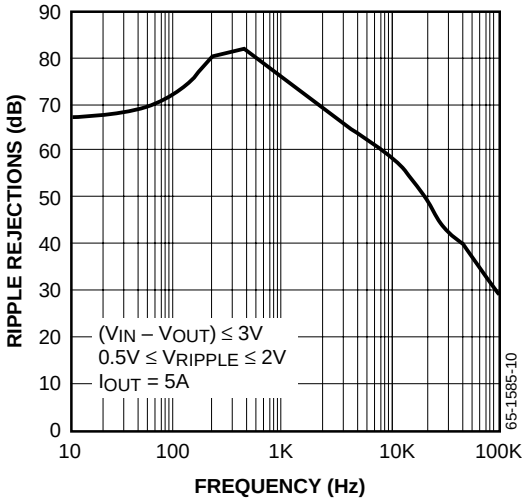


Figure 8. Ripple Rejection vs. Frequency

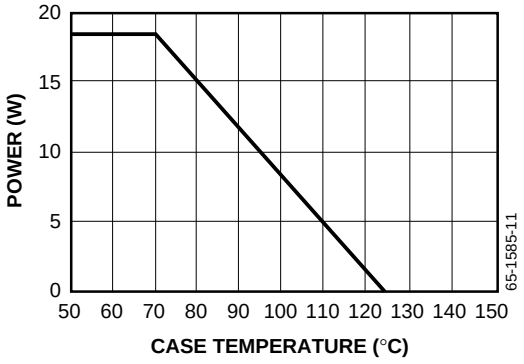


Figure 9. Maximum Power Dissipation

Applications Information

General

The RC1585 and RC1585-1.5 are three-terminal regulators optimized for GTL+ V_{TT} termination and logic applications. These devices are short-circuit protected and offer thermal shutdown to turn off the regulator when the junction temperature exceeds about 150°C. The RC1585 series provides low dropout voltage and fast transient response. Frequency compensation uses capacitors with low ESR while still maintaining stability. This is critical in addressing the needs of low voltage high speed microprocessor buses like GTL+.

Stability

The RC1585 series requires an output capacitor as a part of the frequency compensation. It is recommended to use a 22µF solid tantalum or a 100 µF aluminum electrolytic on the output to ensure stability. The frequency compensation of these devices optimizes the frequency response with low ESR capacitors. In general, it is suggested to use capacitors with an ESR of <1Ω. It is also recommended to use bypass capacitors such as a 22µF tantalum or a 100µF aluminum on the adjust pin of the RC1585 for low ripple and fast transient response. When these bypassing capacitors are not used at the adjust pin, larger values of output capacitors provide equally good results.

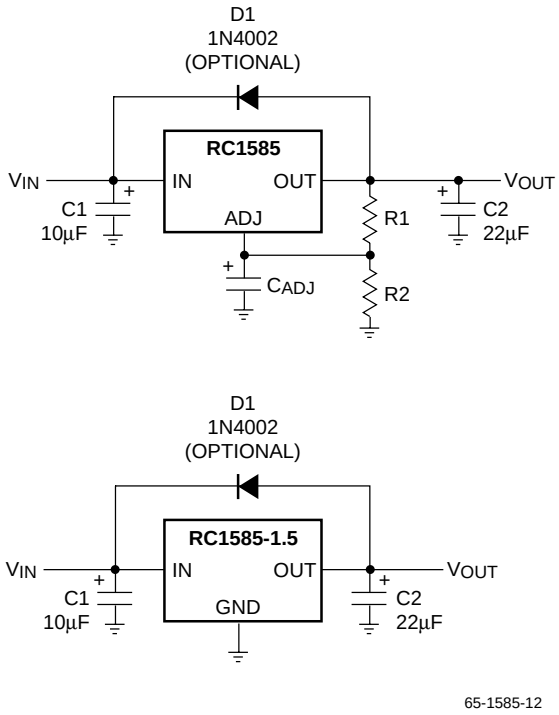


Figure 10. Optional Protection

Protection Diodes

In normal operation, the RC1585 series does not require any protection diodes. For the RC1585, internal resistors limit internal current paths on the adjust pin. Therefore, even with bypass capacitors on the adjust pin, no protection diode is needed to ensure device safety under short-circuit conditions.

A protection diode between the input and output pins is usually not needed. An internal diode between the input and the output pins on the RC1585 series can handle microsecond surge currents of 50A to 100A. Even with large value output capacitors it is difficult to obtain those values of surge currents in normal operation. Only with large values of output capacitance, such as 1000µF to 5000µF, and with the input pin instantaneously shorted to ground can damage occur. A crowbar circuit at the input can generate those levels of current; a diode from output to input is then recommended, as shown in Figure 10. Usually, normal power supply cycling or system “hot plugging and unplugging” will not generate current large enough to do any damage.

The adjust pin can be driven on a transient basis ±7V with respect to the output, without any device degradation. As with any IC regulator, exceeding the maximum input-to-output voltage differential causes the internal transistors to break down and none of the protection circuitry is then functional.

Ripple Rejection

In applications that require improved ripple rejection, a bypass capacitor from the adjust pin of the RC1585 to ground reduces the output ripple by the ratio of V_{OUT}/1.25V. The impedance of the adjust pin capacitor at the ripple frequency should be less than the value of R1 (typically in the range of 100Ω to 120Ω) in the feedback divider network in Figure 10. Therefore, the value of the required adjust pin capacitor is a function of the input ripple frequency. For example, if R1 equals 100Ω and the ripple frequency equals 120Hz, the adjust pin capacitor should be 22µF. At 10kHz, only 0.22µF is needed.

Output Voltage

The RC1585 regulator develops a 1.25V reference voltage between the output pin and the adjust pin (see Figure 11). Placing a resistor R1 between these two terminals causes a constant current to flow through R1 and down through R2 to set the overall output voltage. Normally, this current is the specified minimum load current of 10mA.

The current out of the adjust pin adds to the current from R1 and is typically 35µA. Its output voltage contribution is small and only needs consideration when a very precise output voltage setting is required.

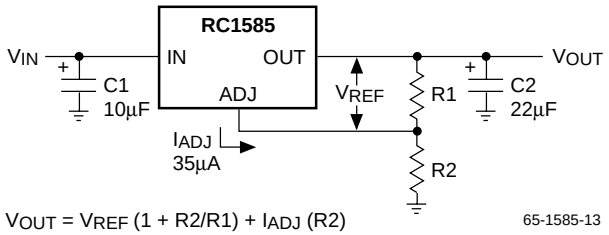


Figure 11. Basic Regulator Circuit

Load Regulation

It is not possible to provide true remote load sensing because the RC1585 series are three-terminal devices. Load regulation is limited by the resistance of the wire connecting the regulators to the load. Load regulation per the data sheet specification is measured at the bottom of the package.

For fixed voltage devices, negative side sensing is a true Kelvin connection with the ground pin of the device returned to the negative side of the load. This is illustrated in Figure 12.

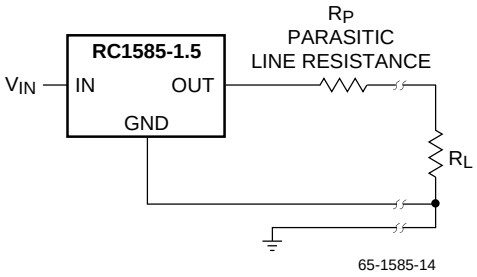


Figure 12. Connection for Best Load Regulation

For adjustable voltage devices, negative side sensing is a true Kelvin connection with the bottom of the output divider returned to the negative side of the load. The best load regulation is obtained when the top of the resistor divider R1 connects directly to the regulator output and not to the load. Figure 13 illustrates this point.

If R1 connects to the load, then the effective resistance between the regulator and the load would be:

R_P x (1 + R2/R1), R_P = Parasitic Line Resistance

The connection shown in Figure 13 does not multiply R_P by the divider ratio. As an example, R_P is about four milliohms per foot with 16-gauge wire. This translates to 4mV per foot at 1A load current. At higher load currents, this drop represents a significant percentage of the overall regulation. It is important to keep the positive lead between the regulator and the load as short as possible and to use large wire or PC board traces.

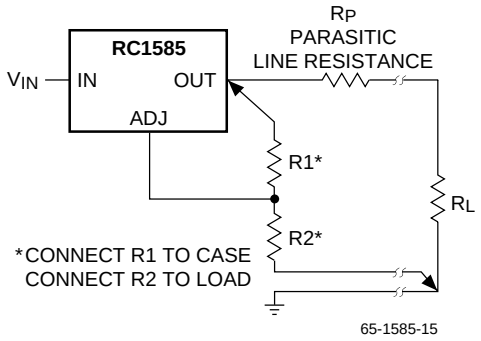


Figure 13. Connection for Best Load Regulation

Thermal Considerations

The RC1585 series protect themselves under overload conditions with internal power and thermal limiting circuitry. However, for normal continuous load conditions, do not exceed maximum junction temperature ratings. It is important to consider all sources of thermal resistance from junction-to-ambient. These sources include the junction-to-case resistance, the case-to-heat sink interface resistance, and the heat sink resistance. Thermal resistance specifications have been developed to more accurately reflect device temperature and ensure safe operating temperatures.

For example, look at using an RC1585T to generate 5A @ 1.5V ± 2% from a 3.3V source (3.2V to 3.6V).

Assumptions:

- V_{IN} = 3.6V worst case
- V_{OUT} = 1.46V worst case
- I_{OUT} = 5A continuous
- T_A = 60°C
- $\theta_{Case\text{-}to\text{-}Ambient}$ = 3°C/W (assuming both a heatsink and a thermally conductive material)

The power dissipation in this application is:

$P_D = (V_{IN} - V_{OUT}) * (I_{OUT}) = (3.6 - 1.46) * (5) = 10.7W$

From the specification table:

$T_J = T_A + (P_D) * (\theta_{Case\text{-}to\text{-}Ambient} + \theta_{JC})$
$= 60 + (10.7) * (3 + 3) = 120°C$

The junction temperature is below the maximum rating.

Junction-to-case thermal resistance is specified from the IC junction to the bottom of the case directly below the die. This is the lowest resistance path for heat flow. Proper mounting ensures the best thermal flow from this area of the package to the heat sink. Use of a thermally conductive material at the case-to-heat sink interface is recommended. Use a thermally conductive spacer if the case of the device must be electrically isolated and include its contribution to the total thermal resistance. The cases of the RC1585 series are directly connected to the output of the device.

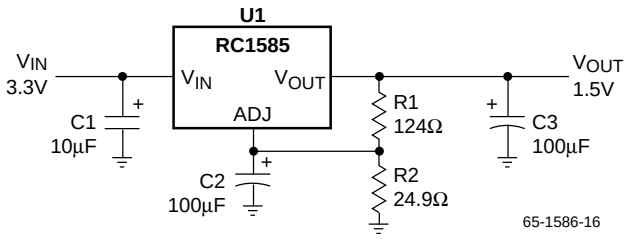


Figure 14. Application Circuit (RC1585)

Table 1. Bill of Materials for Application Circuit for the RC1585

Item	Quantity	Manufacturer	Part Number	Description
C1	1	Xicon	L10V10	10µF, 10V Aluminum
C2, C3	2	Xicon	L10V100	100µF, 10V Aluminum
R1	1	Generic		124Ω, 1%
R2	1	Generic		24.9Ω, 1%
U1	1	Fairchild	RC1585T	5A Regulator

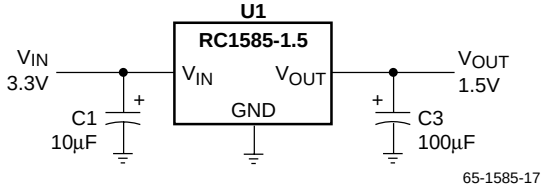


Figure 15. Application Circuit (RC1585-1.5)

Table 2. Bill of Materials for Application Circuit for the RC1585-1.5

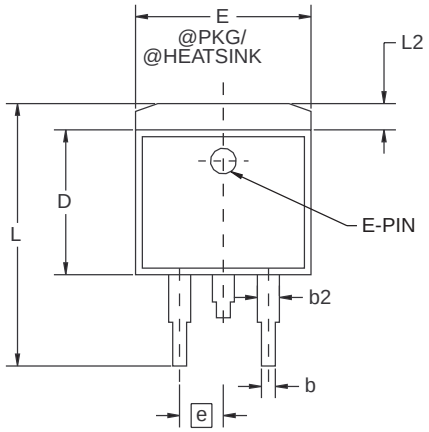
Item	Quantity	Manufacturer	Part Number	Description
C1	1	Xicon	L10V10	10µF, 10V Aluminum
C3	1	Xicon	L10V100	100µF, 10V Aluminum
U1	1	Fairchild	RC1585T-1.5	5A Regulator

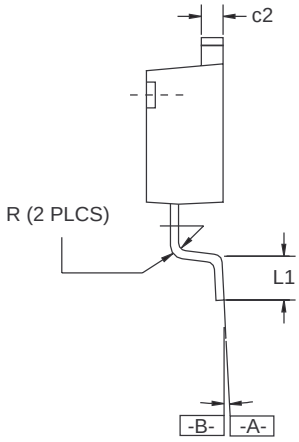
Mechanical Dimensions

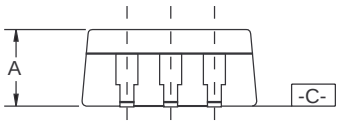
3-Lead TO-263 Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.160	.190	4.06	4.83	
b	.020	.039	0.51	0.99	
b2	.049	.051	1.25	1.30	
c2	.045	.055	1.14	1.40	
D	.340	.380	8.64	9.65	
E	.380	.405	9.65	10.29	
e	.100 BSC		2.54 BSC		
L	.575	.625	14.61	15.88	
L1	.090	.110	2.29	2.79	
L2	—	.055	—	1.40	
R	.017	.019	0.43	0.78	
α	0°	8°	0°	8°	

Notes:
1. Dimensions are exclusive of mold flash and metal burrs.
2. Standoff-height is measured from lead tip with ref. to Datum -B-.
3. Foot length is measured with ref. to Datum -A- with lead surface (at inner R).
4. Dimensiuon exclusive of dambar protrusion or intrusion.
5. Formed leads to be planar with respect to one another at seating place -C-.





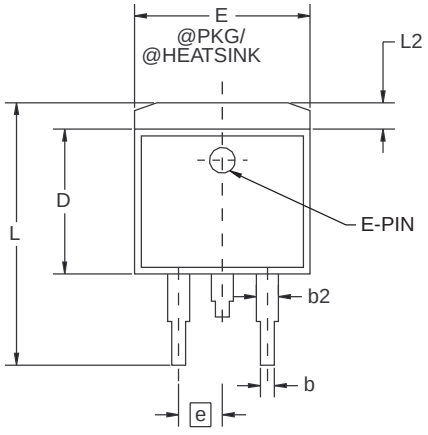


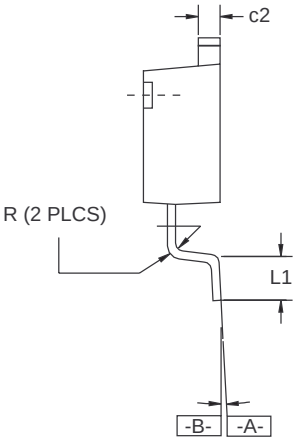
Mechanical Dimensions (continued)

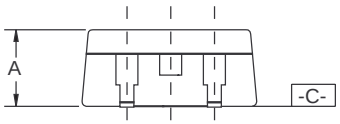
3-Lead TO-263 Center Cut Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.160	.190	4.06	4.83	
b	.020	.039	0.51	0.99	
b2	.049	.051	1.25	1.30	
c2	.045	.055	1.14	1.40	
D	.340	.380	8.64	9.65	
E	.380	.405	9.65	10.29	
e	.100 BSC		2.54 BSC		
L	.575	.625	14.61	15.88	
L1	.090	.110	2.29	2.79	
L2	—	.055	—	1.40	
R	.017	.019	0.43	0.78	
α	0°	8°	0°	8°	

Notes:
1. Dimensions are exclusive of mold flash and metal burrs.
2. Standoff-height is measured from lead tip with ref. to Datum -B-.
3. Foot length is measured with ref. to Datum -A- with lead surface (at inner R).
4. Dimensiuon exclusive of dambar protrusion or intrusion.
5. Formed leads to be planar with respect to one another at seating place -C-.





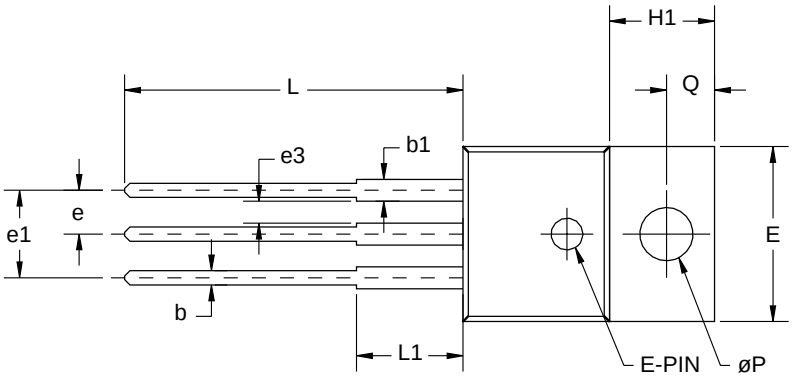


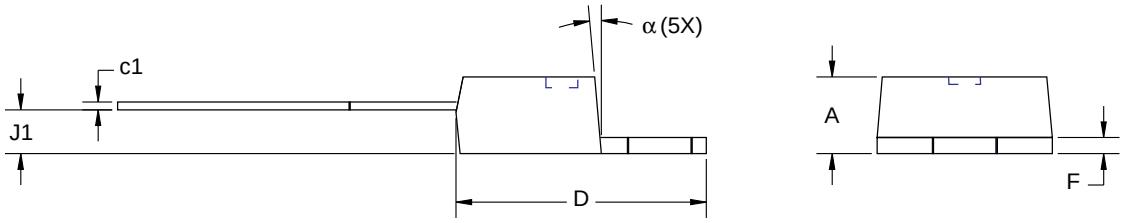
Mechanical Dimensions (continued)

3-Lead TO-220 Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.140	.190	3.56	4.83	
b	.015	.040	.38	1.02	
b1	.045	.070	1.14	1.78	
c1	.014	.022	.36	.56	
øP	.139	.161	3.53	4.09	
D	.560	.650	14.22	16.51	
E	.380	.420	9.65	10.67	
e	.090	.110	2.29	2.79	
e1	.190	.210	4.83	5.33	
e3	.045	—	1.14	—	
F	.020	.055	.51	1.40	
H1	.230	.270	5.94	6.87	
J1	.060	.115	2.04	2.92	
L	.500	.580	12.70	14.73	
L1	.250 BSC		6.35 BSC		
Q	.100	.135	2.54	3.43	
α	3°	7°	3°	7°	

Notes:
1. Dimension c1 apply for lead finish.





Ordering Information

Product Number	Package
RC1585M	TO-263
RC1585MC	TO-263 Center Cut
RC1585T	TO-220
RC1585M-1.5	TO-263
RC1585MC-1.5	TO-263 Center Cut
RC1585T-1.5	TO-220

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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

RC1587

3A Adjustable/Fixed Low Dropout Linear Regulator

Features

- Fast transient response
- Low dropout voltage at up to 3A
- Load regulation: 0.05% typical
- Trimmed current limit
- On-chip thermal limiting
- Standard TO-220, TO-263 and TO-263 center cut packages

Applications

- Pentium® Class GTL+ bus supply
- Low voltage logic supply
- Post regulator for switching supply

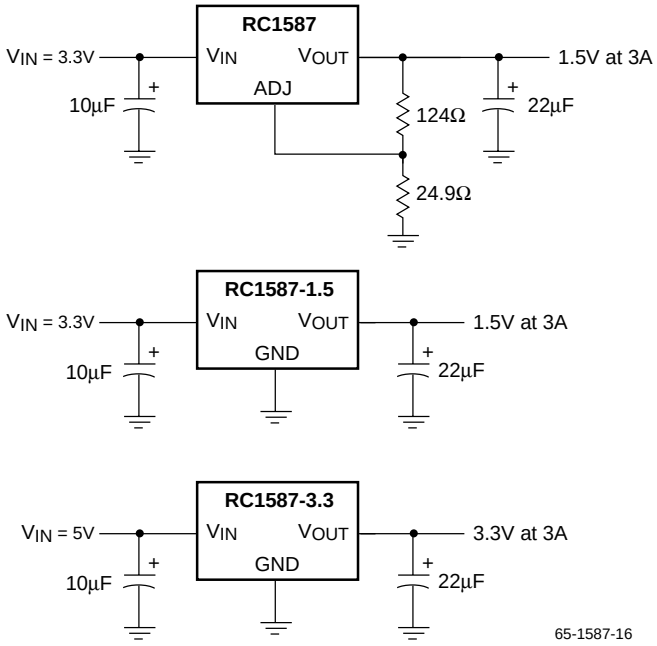
Description

The RC1587, RC1587-1.5, and RC1587-3.3 are low dropout three-terminal regulators with 3A output current capability. These devices have been optimized for low voltage applications including V_{TT} bus termination, where transient response and minimum input voltage are critical. The RC1587 is ideal for low voltage microprocessor applications requiring a regulated output from 1.5V to 3.6V with an input supply of 5V or less. The RC1587-1.5 offers fixed 1.5V with 3A current capability for GTL+ bus V_{TT} termination. The RC1587-3.3 offers fixed 3.3V current capability for logic IC operation.

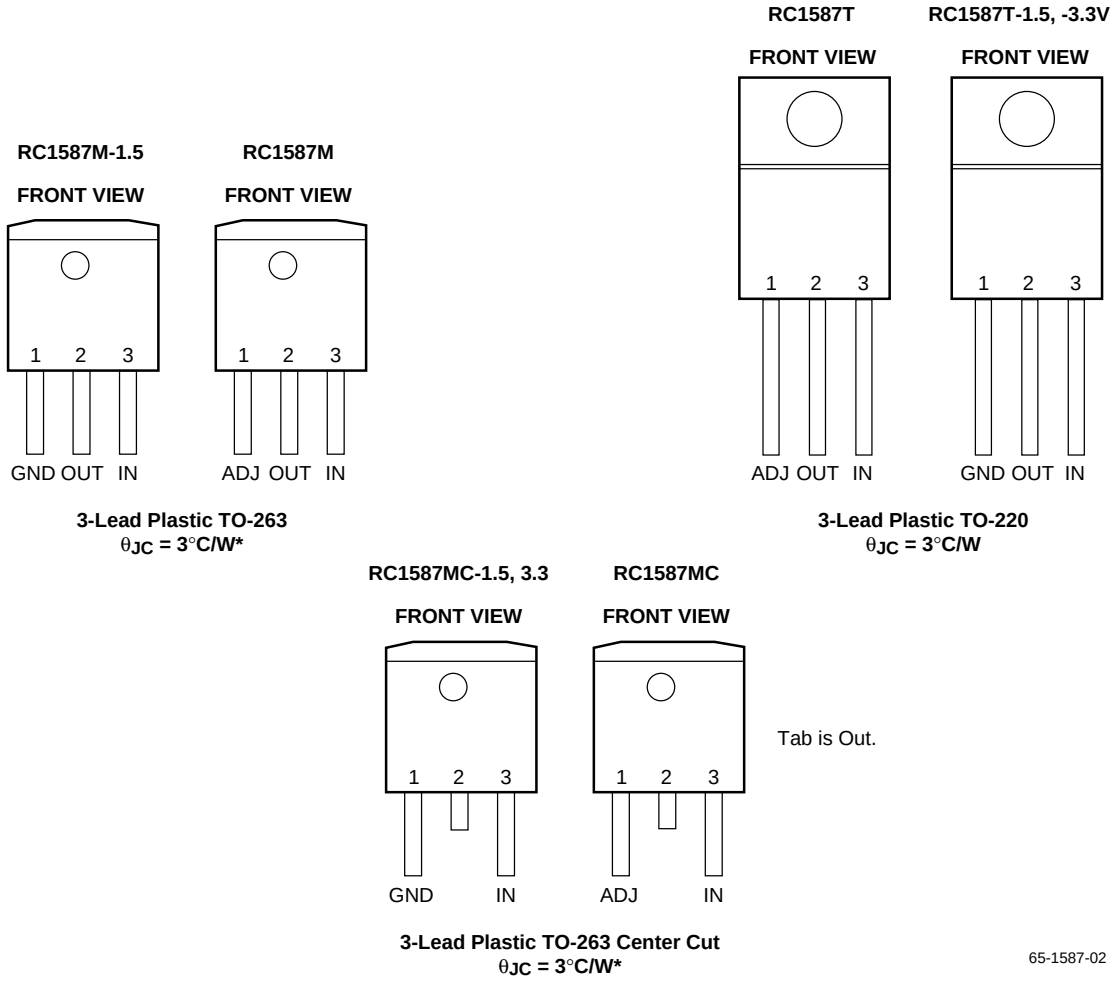
Current limit is trimmed to ensure specified output current and controlled short-circuit current. On-chip thermal limiting provides protection against any combination of overload and ambient temperature that would create excessive junction temperatures.

The RC1587, RC1587-1.5, and RC1587-3.3 are available in the industry-standard TO-220, TO-263 and TO-263 center cut power packages.

Typical Applications



Pin Assignments



* θ_{JA} can vary from 20°C/W to >40°C/W with various mounting techniques.

Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
V_{IN}		7	V
Operating Junction Temperature Range	0	125	°C
Storage Temperature Range	-65	150	°C
Lead Temperature (Soldering, 10 sec.)		300	°C

Electrical Characteristics

Tj = 25°C unless otherwise specified.

The • denotes specifications which apply over the specified operating temperature range.

Parameter	Conditions		Min.	Typ.	Max	Units
Reference Voltage[3]	$1.5V \le (V_{IN} - V_{OUT}) \le 5.75V$, $10mA \le I_{OUT} \le 3A$	•	1.225 (-2%)	1.250	1.275 (+2%)	V
Output Voltage[4]	$3.3V \le V_{IN} \le 7V$ $10mA \le I_{OUT} \le 3A$	•	1.47	1.5	1.53	V
Output Voltage[5]	$5.1V \le V_{IN} \le 7V$ $10mA \le I_{OUT} \le 3A$	•	3.234	3.3	3.366	V
Line Regulation[1, 2]	$(V_{OUT} + 1.5V) \le V_{IN} \le 7V$, $I_{OUT} = 10mA$	•		0.005	0.2	%
Load Regulation[1, 2]	$(V_{IN} - V_{OUT}) = 3V$ $10mA \le I_{OUT} \le 3A$	•		0.05	0.5	%
Dropout Voltage	$\Delta V_{REF} = 1\%$, $I_{OUT} = 3A$	•		1.150	1.300	V
Current Limit	$(V_{IN} - V_{OUT}) = 2V$	•	3.1	4		A
Adjust Pin Current[3]		•		35	120	µA
Adjust Pin Current Change[3]	$1.5V \le (V_{IN} - V_{OUT}) \le 5.75V$, $10mA \le I_{OUT} \le 3A$	•		0.2	5	µA
Minimum Load Current	$1.5V \le (V_{IN} - V_{OUT}) \le 5.75V$	•	10			mA
Quiescent Current	$V_{IN} = 5V$	•		4	13	mA
Ripple Rejection	f = 120Hz, C_{OUT} = 22µF Tantalum, $(V_{IN} - V_{OUT}) = 3V$, $I_{OUT} = 3A$		60	72		dB
Thermal Regulation	$T_A = 25°C$, 30ms pulse			0.004	0.02	%/W
Temperature Stability		•		0.5		%
Long-Term Stability	$T_A = 125°C$, 1000 hrs.			0.03	1.0	%
RMS Output Noise (% of V_{OUT})	$T_A = 25°C$, $10Hz \le f \le 10kHz$			0.003		%
Thermal Resistance, Junction to Case	TO-220			3		°C/W
	TO-263			3		°C/W
Thermal Shutdown				150		°C

Notes:

1. See thermal regulation specifications for changes in output voltage due to heating effects. Load and line regulation are measured at a constant junction temperature by low duty cycle pulse testing.
2. Line and load regulation are guaranteed up to the maximum power dissipation (18W). Power dissipation is determined by input/output differential and the output currrent. Guaranteed maximum output power will not be available over the full input/output voltage range.
3. RC1587 only.
4. RC1587-1.5 only.
5. RC1587-3.3 only.

Typical Performance Characteristics

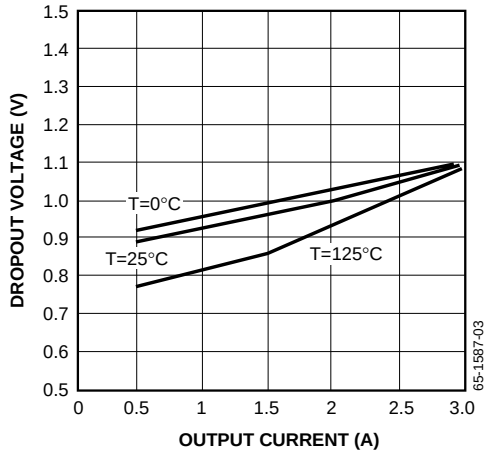


Figure 1. Dropout Voltage vs. Output Current

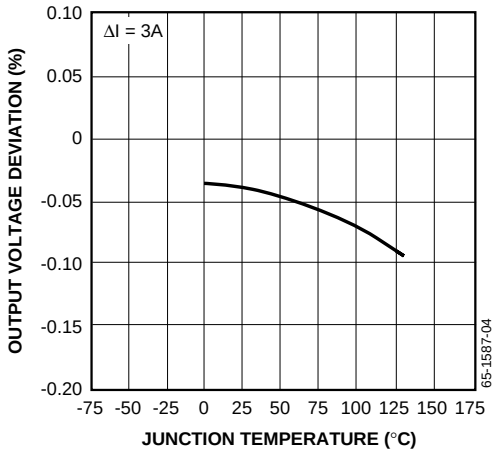


Figure 2. Load Regulation vs. Temperature

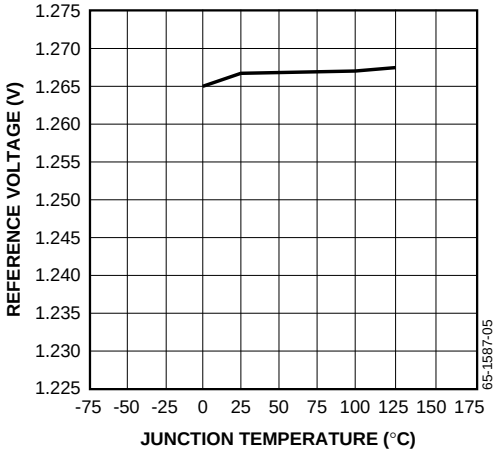


Figure 3. Reference Voltage vs. Temperature

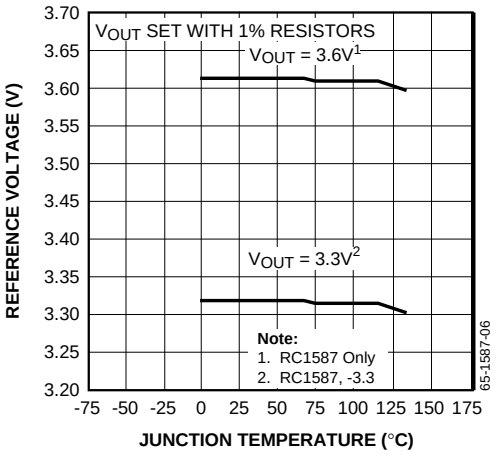


Figure 4. Output Voltage vs. Temperature

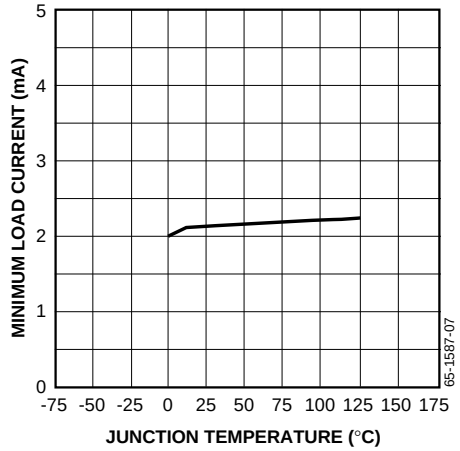


Figure 5. Minimum Load Current vs. Temperature

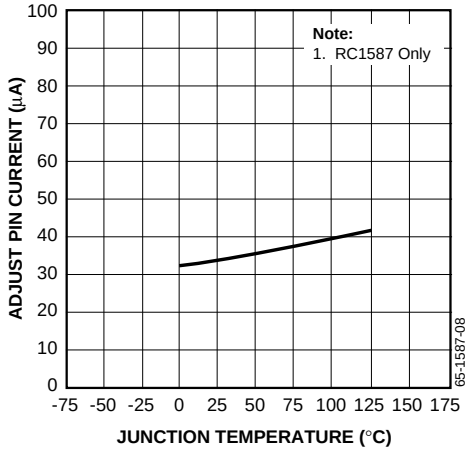


Figure 6. Adjust Pin Current vs. Temperature

Typical Performance Characteristics (continued)

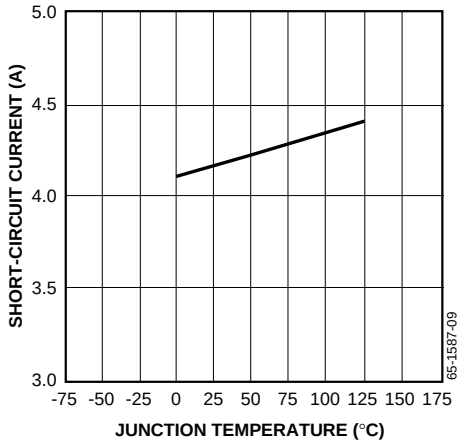


Figure 7. Short-Circuit Current vs. Temperature

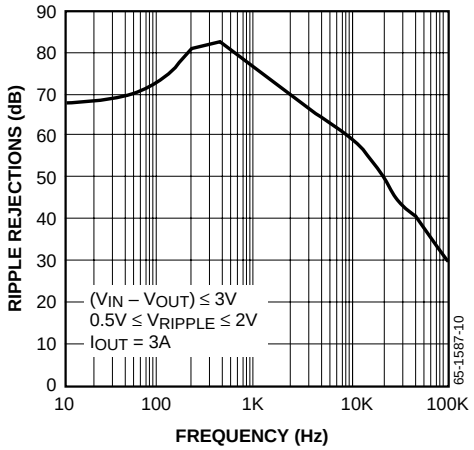


Figure 8. Ripple Rejection vs. Frequency

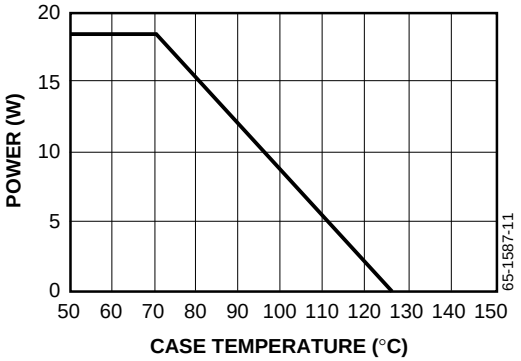


Figure 9. Maximum Power Dissipation

Applications Information

General

The RC1587, RC1587-1.5, and RC1587-3.3 are three-terminal regulators optimized for GTL+ V_{TT} termination applications. These devices are short-circuit protected, and offer thermal shutdown to turn off the regulator when the junction temperature exceeds about 150°C. The RC1587 series provides low dropout voltage and fast transient response. Frequency compensation uses capacitors with low ESR while still maintaining stability. This is critical in addressing the needs of low voltage high speed microprocessor buses like GTL+.

Stability

The RC1587 series require an output capacitor as a part of the frequency compensation. It is recommended to use a 22µF solid tantalum or a 100µF aluminum electrolytic on the output to ensure stability. The frequency compensation of these devices optimizes the frequency response with low ESR capacitors. In general, it is suggested to use capacitors with an ESR of <1Ω. It is also recommended to use bypass capacitors such as a 22µF tantalum or a 100µF aluminum on the adjust pin of the RC1587 for low ripple and fast transient response. When these bypassing capacitors are not used at the adjust pin, larger values of output capacitors provide equally good results.

Protection Diodes

In normal operation, the RC1587 series does not require any protection diodes. For the RC1587, internal resistors limit internal current paths on the adjust pin. Therefore, even with bypass capacitors on the adjust pin, no protection diode is needed to ensure device safety under shortcircuit conditions.

A protection diode between the input and output pins is usually not needed. An internal diode between the input and output pins on the RC1587 series can handle microsecond surge currents of 50A to 100A. Even with large value output capacitors it is difficult to obtain those values of surge currents in normal operation. Only with large values of output capacitance, such as 1000µF to 5000µF, and with the input pin instantaneously shorted to ground can damage occur. A crowbar circuit at the input can generate those levels of current; a diode from output to input is then recommended, as shown in Figure 10. Usually, normal power supply cycling or system “hot plugging and unplugging” will not generate current large enough to do any damage.

The adjust pin can be driven on a transient basis ±7V with respect to the output, without any device degradation. As with any IC regulator, exceeding the maximum input-to-output voltage differential causes the internal transistors to break down and none of the protection circuitry is then functional.

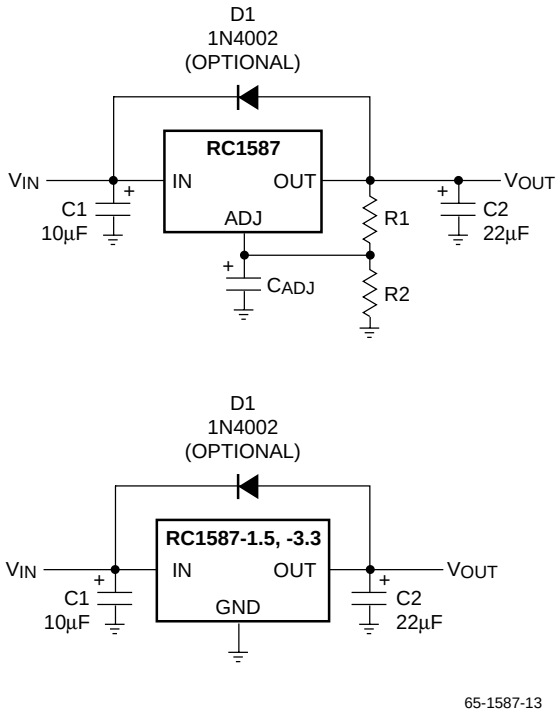


Figure 10. Optional Protection

Ripple Rejection

In applications that require improved ripple rejection, a bypass capacitor from the adjust pin of the RC1587 to ground reduces the output ripple by the ratio of V_{OUT}/1.25V. The impedance of the adjust pin capacitor at the ripple frequency should be less than the value of R1 (typically in the range of 100Ω to 120Ω) in the feedback divider network in Figure 10. Therefore, the value of the required adjust pin capacitor is a function of the input ripple frequency. For example, if R1 equals 100Ω and the ripple frequency equals 120Hz, the adjust pin capacitor should be 22µF. At 10kHz, only 0.22µF is needed.

Output Voltage

The RC1587 regulator develops a 1.25V reference voltage between the output pin and the adjust pin (see Figure 11). Placing a resistor R1 between these two terminals causes a constant current to flow through R1 and down through R2 to set the overall output voltage. Normally, this current is the specified minimum load current of 10mA.

The current out of the adjust pin adds to the current from R1 and is typically 35µA. Its output voltage contribution is small and only needs consideration when very precise output voltage setting is required.

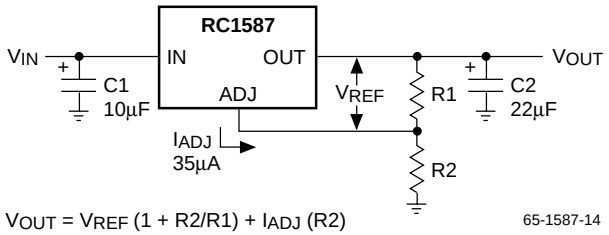


Figure 11. Basic Regulator Circuit

Load Regulation

It is not possible to provide true remote load sensing because the RC1587 series are three-terminal devices. Load regulation is limited by the resistance of the wire connecting the regulators to the load. Load regulation per the data sheet specification is measured at the bottom of the package.

For fixed voltage devices, negative side sensing is a true Kelvin connection with the ground pin of the device returned to the negative side of the load. This is illustrated in Figure 12.

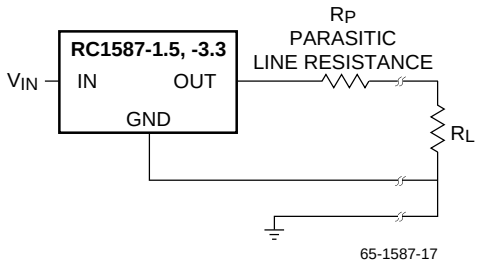


Figure 12. Connection for Best Load Regulation

For adjustable voltage devices, negative side sensing is a true Kelvin connection with the bottom of the output divider returned to the negative side of the load. The best load regulation is obtained when the top of resistor divider R1 connects directly to the regulator output and not to the load. Figure 13 illustrates this point.

If R1 connects to the load, then the effective resistance between the regulator and the load would be:

$R_P \times (1 + R2/R1)$, R_P = Parasitic Line Resistance

The connection shown in Figure 13 does not multiply R_P by the divider ratio. As an example, R_P is about four milliohms per foot with 16-gauge wire. This translates to 4mV per foot at 1A load current. At higher load currents, this drop represents a significant percentage of the overall regulation. It is important to keep the positive lead between the regulator and the load as short as possible and to use large wire or PC board traces.

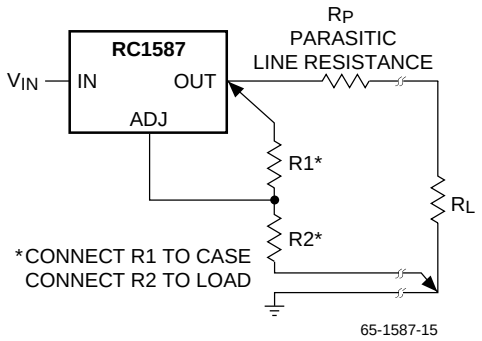


Figure 13. Connection for Best Load Regulation

Thermal Considerations

The RC1587 series protect themselves under overload conditions with internal power and thermal limiting circuitry. However, for normal continuous load conditions, do not exceed maximum junction temperature ratings. It is important to consider all sources of thermal resistance from junction-to-ambient. These sources include the junction-to-case resistance, the case-to-heat sink interface resistance, and the heat sink resistance. Thermal resistance specifications have been developed to more accurately reflect device temperature and ensure safe operating temperatures.

For example, look at using an RC1587T to generate 3A @ 1.5V ± 2% from a 3.3V source (3.2V to 3.6V).

Assumptions:

- V_{IN} = 3.6V worst case
- V_{OUT} = 1.46V worst case
- I_{OUT} = 3A continuous
- T_A = 70°C
- $\theta_{Case\text{-}to\text{-}Ambient}$ = 3°C/W (assuming both a heatsink and a thermally conductive material)

The power dissipation in this application is:

$P_D = (V_{IN} - V_{OUT}) * (I_{OUT}) = (3.6 - 1.46) * (3) = 6.42W$

From the specification table:

$T_J = T_A + (P_D) * (\theta_{Case\text{-}to\text{-}Ambient} + \theta_{JC})$
$= 70 + (6.42) * (3 + 3) = 109°C$

The junction temperature is below the maximum rating.

Junction-to-case thermal resistance is specified from the IC junction to the bottom of the case directly below the die. This is the lowest resistance path for heat flow. Proper mounting ensures the best thermal flow from this area of the package to the heat sink. Use of a thermally conductive material at the case-to-heat sink interface is recommended. Use a thermally conductive spacer if the case of the device must be electrically isolated and include its contribution to the total thermal resistance. The cases of the RC1587 series are directly connected to the output of the device.

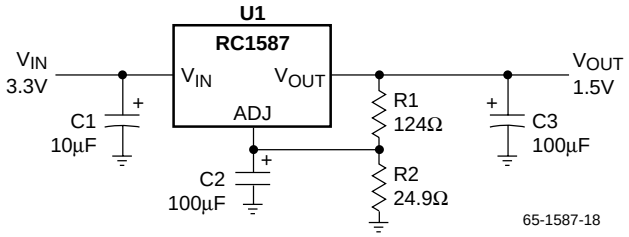


Figure 14. Application Circuit (RC1587)

Table 1. Bill of Materials for Application Circuit for the RC1587

Item	Quantity	Manufacturer	Part Number	Description
C1	1	Xicon	L10V10	10µF, 10V Aluminum
C2, C3	2	Xicon	L10V100	100µF, 10V Aluminum
R1	1	Generic		124Ω, 1%
R2	1	Generic		24.9Ω, 1%
U1	1	Fairchild	RC1587T	3A Regulator

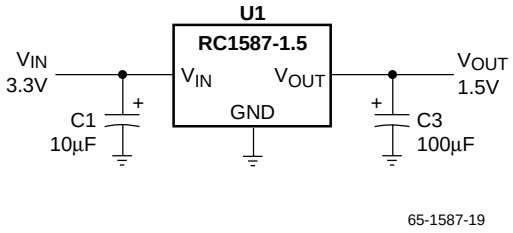


Figure 15. Application Circuit (RC1587-1.5)

Table 2. Bill of Materials for Application Circuit for the RC1587-1.5

Item	Quantity	Manufacturer	Part Number	Description
C1	1	Xicon	L10V10	10µF, 10V Aluminum
C3	1	Xicon	L10V100	100µF, 10V Aluminum
U1	1	Fairchild	RC1587T-1.5	3A Regulator

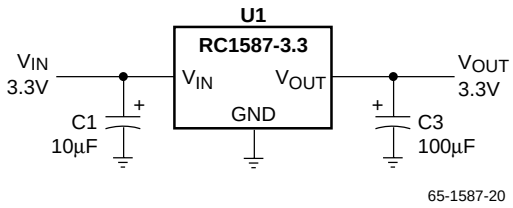


Figure 16. Application Circuit (RC1587-3.3)

Table 3. Bill of Materials for Application Circuit for the RC1587-1.5

Item	Quantity	Manufacturer	Part Number	Description
C1	1	Xicon	L10V10	10µF, 10V Aluminum
C3	1	Xicon	L10V100	100µF, 10V Aluminum
U1	1	Fairchild	RC1587T-3.3	3A Regulator

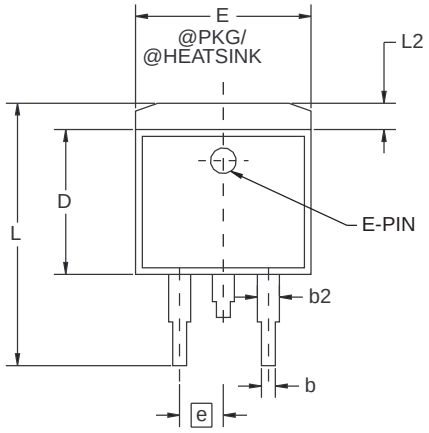
Notes

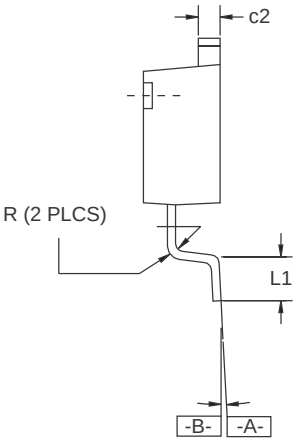
Mechanical Dimensions

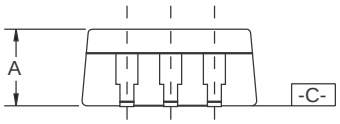
3-Lead TO-263 Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.160	.190	4.06	4.83	
b	.020	.039	0.51	0.99	
b2	.049	.051	1.25	1.30	
c2	.045	.055	1.14	1.40	
D	.340	.380	8.64	9.65	
E	.380	.405	9.65	10.29	
e	.100 BSC		2.54 BSC		
L	.575	.625	14.61	15.88	
L1	.090	.110	2.29	2.79	
L2	—	.055	—	1.40	
R	.017	.019	0.43	0.78	
α	0°	8°	0°	8°	

Notes:
1. Dimensions are exclusive of mold flash and metal burrs.
2. Standoff-height is measured from lead tip with ref. to Datum -B-.
3. Foot length is measured with ref. to Datum -A- with lead surface (at inner R).
4. Dimensiuon exclusive of dambar protrusion or intrusion.
5. Formed leads to be planar with respect to one another at seating place -C-.





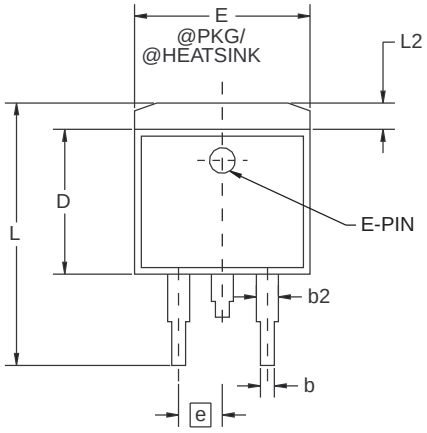


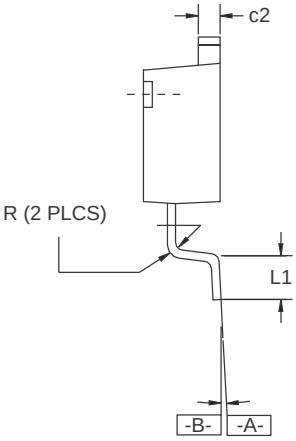
Mechanical Dimensions (continued)

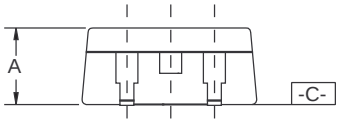
3-Lead TO-263 Center Cut Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.160	.190	4.06	4.83	
b	.020	.039	0.51	0.99	
b2	.049	.051	1.25	1.30	
c2	.045	.055	1.14	1.40	
D	.340	.380	8.64	9.65	
E	.380	.405	9.65	10.29	
e	.100 BSC		2.54 BSC		
L	.575	.625	14.61	15.88	
L1	.090	.110	2.29	2.79	
L2	—	.055	—	1.40	
R	.017	.019	0.43	0.78	
α	0°	8°	0°	8°	

Notes:
1. Dimensions are exclusive of mold flash and metal burrs.
2. Standoff-height is measured from lead tip with ref. to Datum -B-.
3. Foot length is measured with ref. to Datum -A- with lead surface (at inner R).
4. Dimensiuon exclusive of dambar protrusion or intrusion.
5. Formed leads to be planar with respect to one another at seating place -C-.





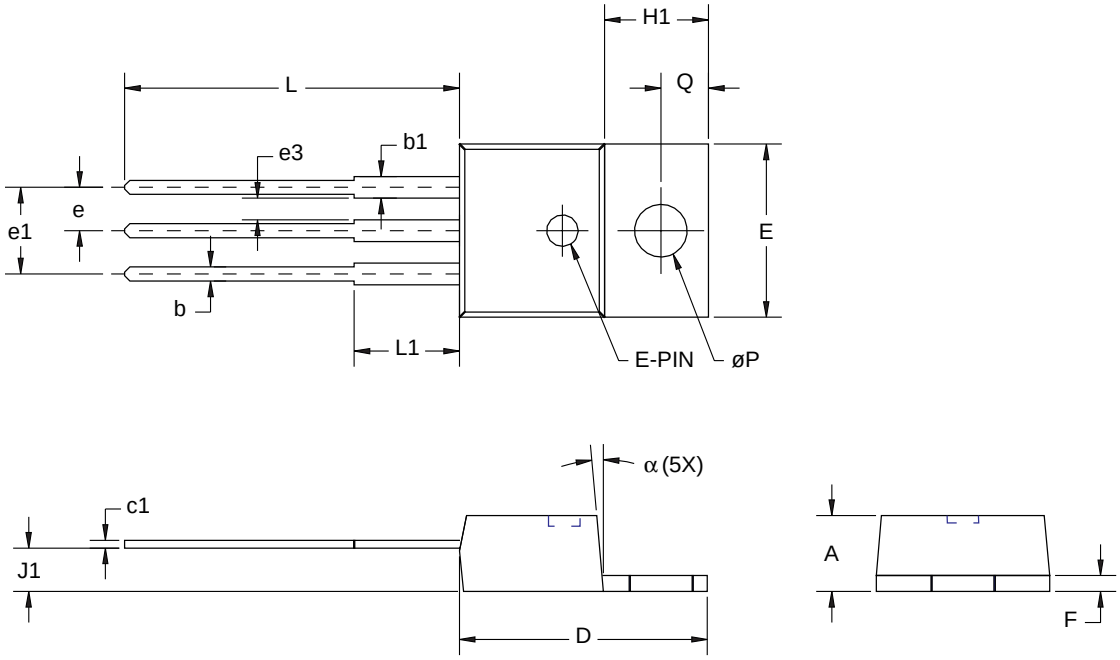


Mechanical Dimensions (continued)

3-Lead TO-220 Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.140	.190	3.56	4.83	
b	.015	.040	.38	1.02	
b1	.045	.070	1.14	1.78	
c1	.014	.022	.36	.56	
øP	.139	.161	3.53	4.09	
D	.560	.650	14.22	16.51	
E	.380	.420	9.65	10.67	
e	.090	.110	2.29	2.79	
e1	.190	.210	4.83	5.33	
e3	.045	—	1.14	—	
F	.020	.055	.51	1.40	
H1	.230	.270	5.94	6.87	
J1	.080	.115	2.04	2.92	
L	.500	.580	12.70	14.73	
L1	.250 BSC		6.35 BSC		
Q	.100	.135	2.54	3.43	
α	3°	7°	3°	7°	

Notes:
1. Dimension c1 apply for lead finish.



Ordering Information

Product Number	Package
RC1587M	TO-263
RC1587MC	TO-263 center cut
RC1587T	TO-220
RC1587M-1.5	TO-263
RC1587MC-1.5	TO-263 center cut
RC1587T-1.5	TO-220
RC1587M-3.3	TO-263
RC1587MC-3.3	TO-263 center cut
RC1587T-3.3	TO-220

RC1616

0.5A Adjustable/Fixed Low Dropout Linear Regulator

Features

- Low dropout voltage
- Load regulation: 0.05% typical
- Current limit
- On-chip thermal limiting
- Standard SOT-223 and TO-263 packages
- Three-terminal adjustable or fixed 2.5V, 3.3V or 5V

Applications

- USB Controlled Power Supply
- High efficiency linear regulators for Mixed Voltage Logic, ASIC, FPGA based systems
- Post regulators for switching supplies
- Battery chargers
- 5V to 3.3V, or 2.5V, 1.8V, 1.5V linear regulators
- Motherboard clock supplies
- SDRAM Module supplies

Description

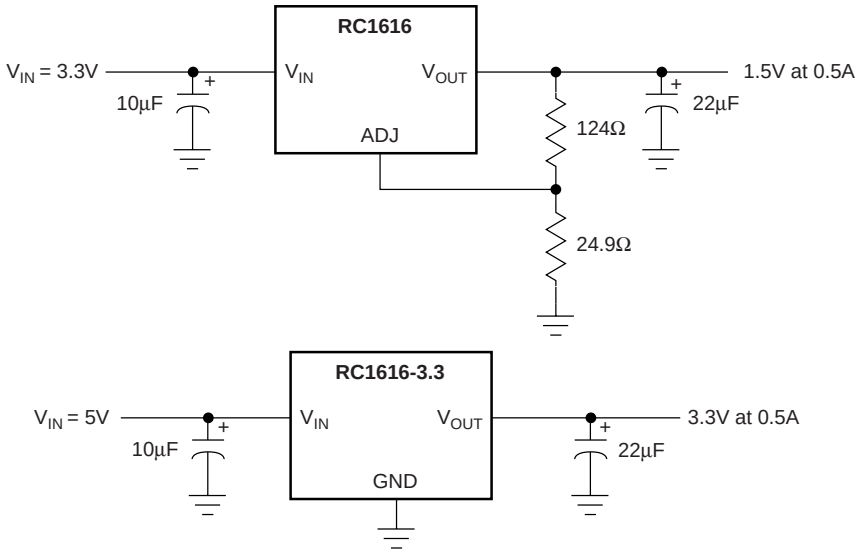
The RC1616 and RC1616-2.5, -3.3 and -5 are low dropout three-terminal regulators with 0.5A output current capability. These devices have been optimized for low voltage where transient response and minimum input voltage are critical. The 5V version is designed also to be used in USB Hub and Motherboard applications.

On-chip thermal limiting provides protection against any combination of overload and ambient temperature that would create excessive junction temperatures.

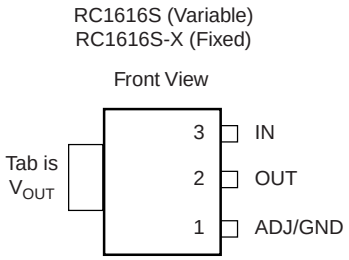
Unlike PNP type regulators where up to 10% of the output current is wasted as quiescent current, the bias current of the RC1616 flows into the load, increasing efficiency.

The RC1616 series regulators are available in the industry-standard SOT-223 and TO-263 power packages.

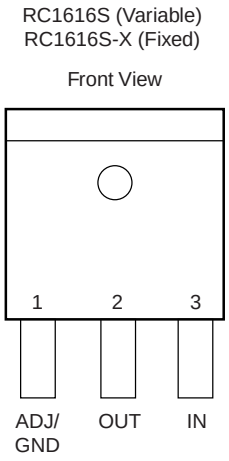
Typical Applications



Pin Assignments



4-Lead Plastic SOT-223
Θ_{JC} = 15°C/W*



3-Lead Plastic TO-263
Θ_{JC} = 10°C/W*

*With package soldered to 0.5 square inch copper area over backside ground plane or internal power plane, Θ_{JA} can vary from 30°C/W to >50°C/W. Other mounting techniques may provide better power dissipation than 30°C/W.

Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
V_{IN}		7.5	V
Operating Junction Temperature Range	0	125	°C
Storage Temperature Range	-65	150	°C
Lead Temperature (Soldering, 10 sec.)		300	°C

Electrical Characteristics

Operating Conditions: $V_{IN} \leq 7V$, $T_J = 25°C$ unless otherwise specified.

The • denotes specifications which apply over the specified operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
Reference Voltage[3]	$1.5V \leq (V_{IN} - V_{OUT}) \leq 5.75V$, $10mA \leq I_{OUT} \leq 0.5A$	•	1.225 (-2%)	1.250	1.275 (+2%)	V
Output Voltage	$10mA \leq I_{OUT} \leq 0.5A$					
	RC1616-2.5, $4.0V \leq V_{IN} \leq 7V$	•	2.450	2.500	2.550	V
	RC1616-3.3, $4.5V \leq V_{IN} \leq 7V$	•	3.234	3.300	3.366	V
	RC1616-5, $6.2V \leq V_{IN} \leq 7V$	•	4.900	5.000	5.100	V
Line Regulation[1,2]	$(V_{OUT} + 1.5V) \leq V_{IN} \leq 7V$, $I_{OUT} = 10mA$	•		0.005	0.2	%
Load Regulation[1,2,3]	$(V_{IN} - V_{OUT}) = 2V$, $10mA \leq I_{OUT} \leq 0.5A$	•		0.05	0.5	%
Dropout Voltage	$\Delta V_{REF} = 1\%$, $I_{OUT} = 0.5A$	•		1.000	1.200	V
Adjust Pin Current[3]		•		35	120	µA
Adjust Pin Current Change[3]	$1.5V \leq (V_{IN} - V_{OUT}) \leq 5.75$, $10mA \leq I_{OUT} \leq 0.5A$	•		0.2	5	µA
Minimum Load Current	$1.5V \leq (V_{IN} - V_{OUT}) \leq 5.75$	•	10			mA
Quiescent Current	$V_{IN} = V_{OUT} + 1.25V$	•		4	13	mA
Ripple Rejection	f = 120Hz, $C_{OUT} = 22\mu F$ Tantalum, $(V_{IN} - V_{OUT}) = 3V$, $I_{OUT} = 0.5A$		60	72		dB
Thermal Regulation	$T_A = 25°C$, 30ms pulse			0.004	0.02	%/W
Temperature Stability		•		0.5		%
Long-Term Stability	$T_A = 125°C$, 1000hrs.			0.03	1.0	%
RMS Output Noise (% of V_{OUT})	$T_A = 25°C$, $10Hz \leq f \leq 10kHz$			0.003		%
Thermal Resistance, Juncation to Case	SOT-223			15		°C/W
	TO-263			10		°C/W
Thermal Shutdown				150		°C

Notes:

1. See thermal regulation specifications for changes in output voltage due to heating effects. Load and line regulation are measured at a constant junction temperature by low duty cycle pulse testing.
2. Line and load regulation are guaranteed up to the maximum power dissipation. Power dissipation is determined by input/output differential and the output current. Guaranteed maximum output power will not be available over the full input/output voltage range.
3. RC1616 only.

Typical Performance Characteristics

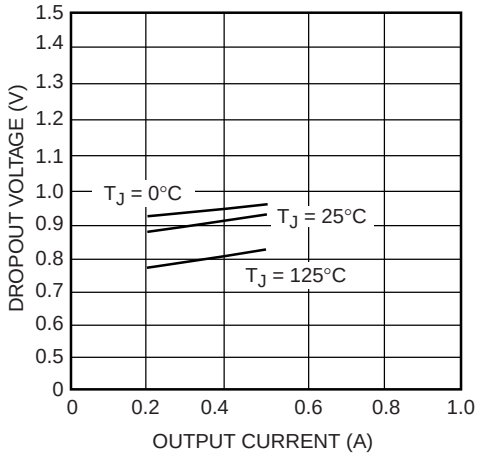


Figure 1. Dropout Voltage vs. Output Current

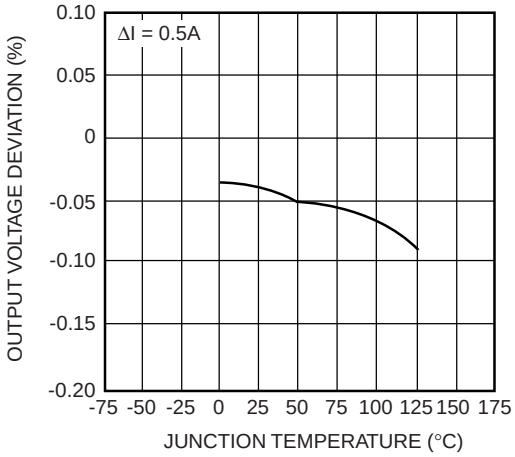


Figure 2. Load Regulation vs. Temperature

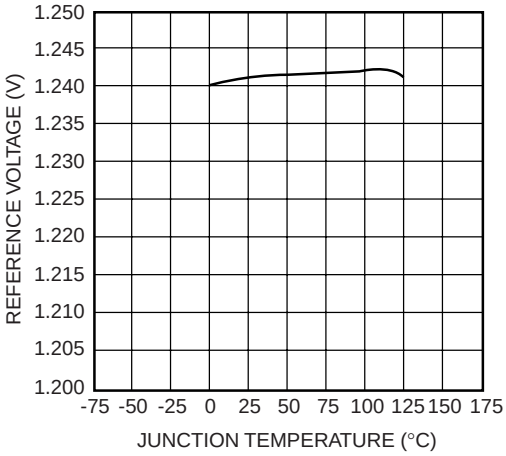


Figure 3. Reference Voltage vs. Temperature

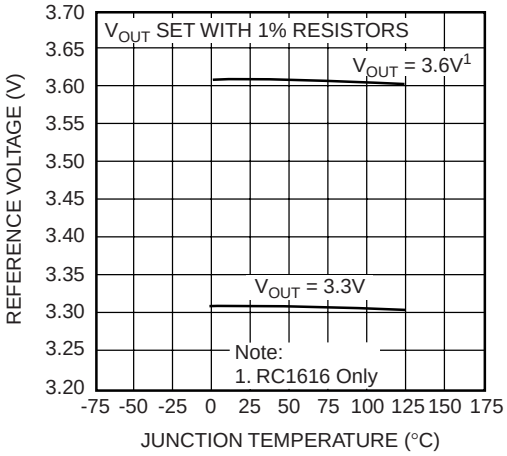


Figure 4. Output Voltage vs. Temperature

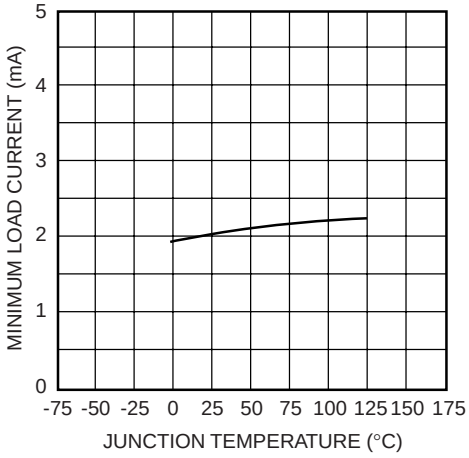


Figure 5. Minimum Load Current vs. Temperature

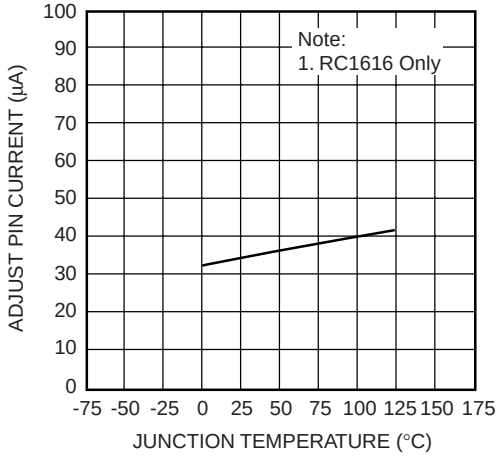


Figure 6. Adjust Pin Current vs. Temperature

Typical Performance Characteristics (continued)

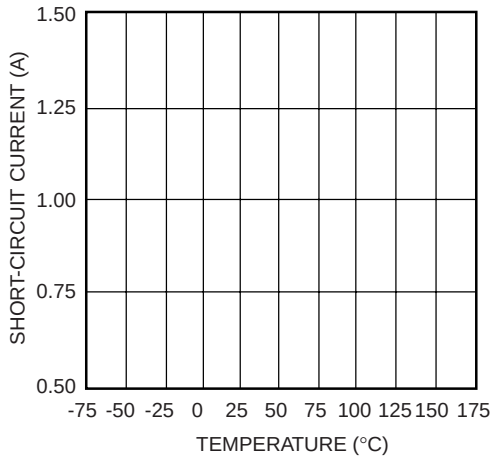


Figure 7. Short-Circuit Current vs. Temperature

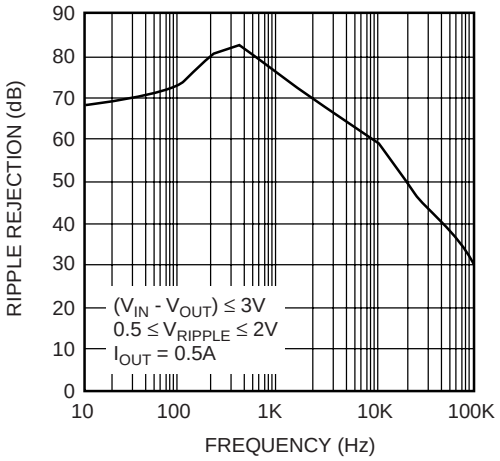


Figure 8. Ripple Rejection vs. Frequency

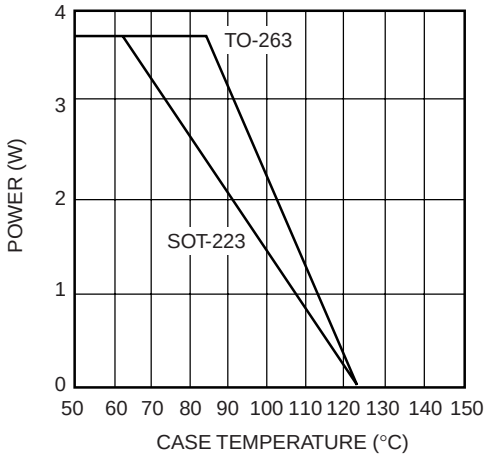


Figure 9. Maximum Power Dissipation

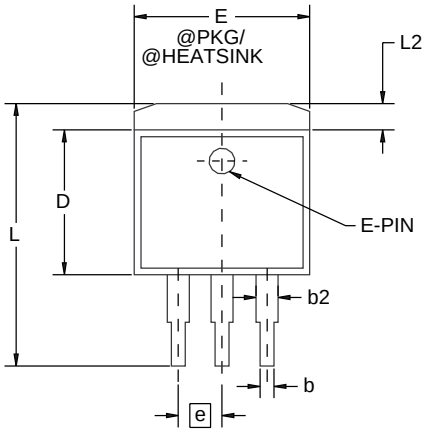
Mechanical Dimensions

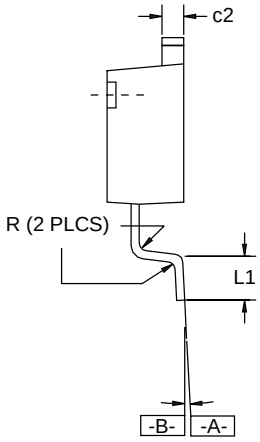
3-Lead TO-263 Package

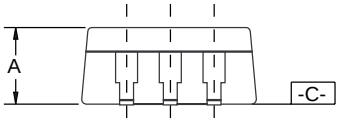
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.160	.190	4.06	4.83	
b	.020	.039	0.51	0.99	
b2	.049	.051	1.25	1.30	
c2	.045	.055	1.14	1.40	
D	.340	.380	8.64	9.65	
E	.380	.405	9.65	10.29	
e	.100 BSC		2.54 BSC		
L	.575	.625	14.61	10.88	
L1	.090	.100	2.29	2.79	
L2	—	.055	—	1.40	
R	.017	.019	0.43	0.48	
α	0°	8°	0°	8°	

Notes:

1. Dimensions are exclusive of mold flash and metal burrs.
2. Standoff-height is measured from lead tip with ref. to Datum -B-.
3. Foot length is measured with ref. to Datum -A- with lead surface (at inner R).
4. Dimension exclusive of dambar protrusion or intrusion.
5. Formed leads to be planar with respect to one another at seating place -C-.



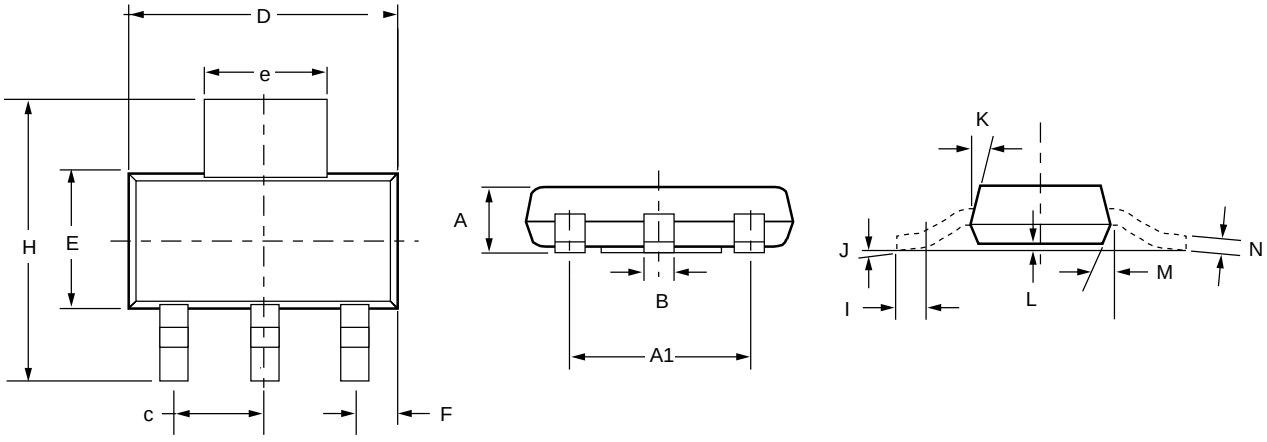




Mechanical Dimensions

4-Lead SOT-223 Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.071	—	1.80	
A1	—	.181	—	4.80	
B	.025	.033	.640	.840	
c	—	.090	—	2.29	
D	.248	.264	6.30	6.71	
E	.130	.148	3.30	3.71	
e	.115	.124	2.95	3.15	
F	.033	.041	.840	1.04	
H	.264	.287	6.71	7.29	
I	.012	—	.310	—	
J	—	10°	—	10°	
K	10°	16°	10°	16°	
L	.0008	.0040	.0203	.1018	
M	10°	16°	10°	16°	
N	.010	.014	.250	.360	



Ordering Information

Product Number	Package
RC1616M	TO-263
RC1616S	SOT-223
RC1616M-2.5	TO-263
RC1616S-2.5	SOT-223
RC1616M-3.3	TO-263
RC1616S-3.3	SOT-223
RC1616M-5	TO-263
RC1616S-5	SOT-223

RC2207

Voltage Controlled Oscillator

Features

- Excellent temperature stability — 20 ppm/°C
- Linear frequency sweep
- Adjustable duty cycle — 0.1% to 99.9%
- Two or four level FSK capability
- Wide sweep range — 1000:1 min.
- Logic compatible input and output levels
- Wide supply voltage range — ±4V to ±13V
- Low supply sensitivity ±0.15%/V
- Wide frequency range — 0.01 Hz to 1 MHz
- Simultaneous triangle and squarewave outputs

Applications

- FSK generation
- Voltage and current-to-frequency conversion
- Stable phase-locked loop
- Waveform generation triangle, sawtooth, pulse, squarewave
- FM and sweep generation

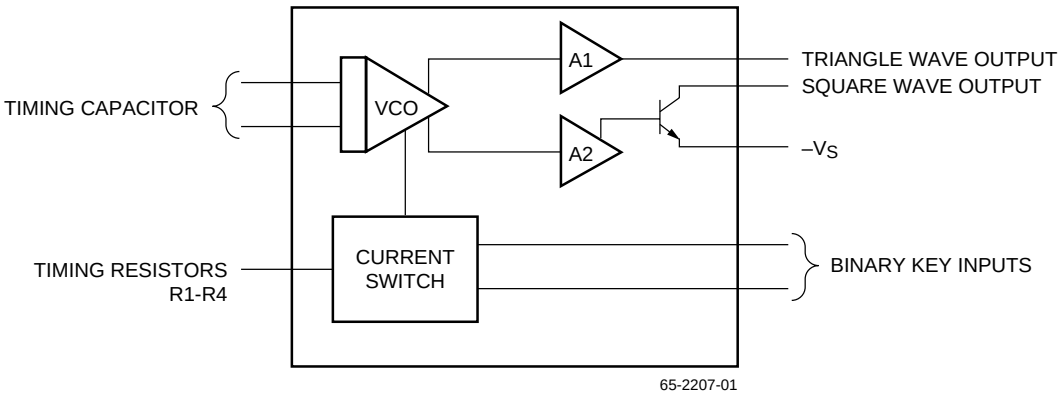
Description

The RC2207 is a monolithic voltage-controlled oscillator (VCO) integrated circuit featuring excellent frequency stability and a wide tuning range. The circuit provides simultaneous triangle and squarewave outputs over a frequency range of 0.01 Hz to 1 MHz. It is ideally suited for FM, FSK and sweep or tone generation as well as for phase-locked loop applications.

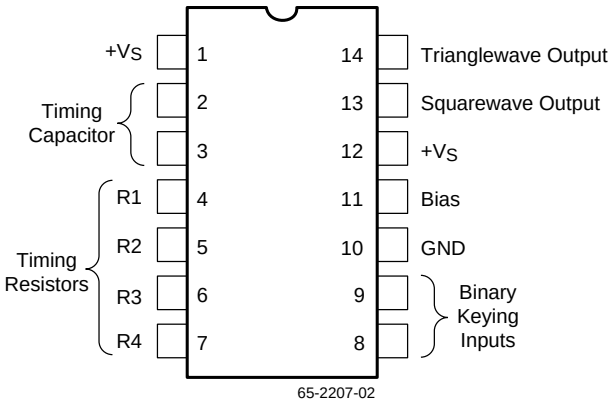
As shown in the Block Diagram, the circuit is comprised of four functional blocks: a variable-frequency oscillator which generates the basic periodic waveforms; four current switches actuated by binary keying inputs; and buffer amplifiers for both the triangle and squarewave outputs. The internal switches transfer the oscillator current to any of four external timing resistors to produce four discrete frequencies which are selected according to the binary logic levels at the keying terminals (pins 8 and 9).

The RC2207 has a typical drift specification of 20 ppm/°C. The oscillator frequency can be linearly swept over a 1000:1 range with an external control voltage; and the duty cycle of both the triangle and the squarewave outputs can be varied from 0.1% to 99.9% to generate stable pulse and sawtooth waveforms.

Block Diagram



Pin Assignments



Pin Descriptions

Pin Name	Pin Number	Pin Function Description
Bias for Single Supply	11	For single supply operations, pin 11 should be externally biased to a potential between $+V_S/3$ and $+V_S/2$ (see Figure 8). The bias current at pin 11 is nominally 5% of the total oscillation timing current I_T.
Binary Keying Inputs	8, 9	The internal impedance at these pins is approximately 5 kΩ. Keying levels are <1.4V for zero and > 3V for one logic levels referenced to the DC voltage at pin 10.
Ground	10	For split supply operation, this pin serves as circuit ground. For single supply operation, pin 10 should be AC grounded through a 1 μF bypass capacitor. During split supply operation, a ground current of 2 I_T flows out of this terminal, where I_T is the total timing current.
Squarewave Output	13	The squarewave output at pin 13 is an open-collector stage capable of sinking up to 20 mA of load current. R_L serves as a pull-up load resistor for this output. Recommended values for R_L range from 1 kΩ to 10 kΩ
Supply Voltage ($+V_S$, $-V_S$)	1, 12	The RC2207 is designed to operate over a power supply range of +4V to ±13V for split supplies, or 8V to 26V for single supplies. At high supply voltages, the frequency sweep range is reduced. Performance is optimum for ±6V, or 12V single supply operation.
Timing Capacitor	2, 3	The oscillator frequency is inversely proportional to the timing capacitor, C. The minimum capacitance value is limited by stray capacitances and the maximum value by physical size and leakage current considerations. Recommended values range from 100 pF to 100 μF. The capacitor should be non-polarized.
Timing Resistors (R1–R4)	4–7	The timing resistors determine the total timing current, I_T, available to charge the timing capacitor. Values for timing resistors can range from 1.5 kΩ to 2 MΩ; however, for optimum temperature and power supply stability, recommended values are 4 kΩ to 200 kΩ. To avoid parasitic pick up, timing resistor leads should be kept as short as possible. For noise environments, unused or deactivated timing terminals should be bypassed to ground through 0.1 μF capacitors. Otherwise, they may be left open.
Trianglewave Output	14	The output at pin 14 is a trianglewave with a peak swing of approximately one-half of the total supply voltage. Pin 14 has a very low output impedance of 10Ω and is internally protected against short circuits. Notice that the triangle waveform linearity is sensitive to parasite coupling between the square and the trianglewave outputs (pins 13 and 14). In board layout or circuit wiring, care should be taken to minimize stray wiring capacitance between those pins.

Absolute Maximum Ratings

Parameter	Min.	Max.	Units
Supply Voltage		+26	V
Storage Temperature Range	-65	+150	V
Operating Temperature Range	-55	+125	°C
Lead Soldering Temperature (60 seconds)		+300	°C

Thermal Characteristics

	Ceramic DIP	SOIC	Plastic DIP
Maximum Juncton Temperature	+175°C	+125°C	+125°C
Maximum P_D T_A < 50°C	1042 mW	300 mW	468 mW
Thermal Resistance, θ_{JC}	60°C/W	60°C/W	60°C/W
Thermal Resistance, θ_{JA}	120°C/W	200°C/W	160°C/W
For T_A > 50°C Derate at	8.33 mW/°C	5.0 mW/°C	6.25 mW/°C

Electrical Characteristics

(Test Circuit of Figure 1, V_S = ±6V, T_A = +25°C, C = 5000 pF, R1= R2 = R3 = R4 = 20 kΩ, R_L = 4.7Ω binary inputs grounded, S1 and S2 closed unless otherwise specified)

Parameters			Test Conditions		Min.	Typ.	Max.	Units
General Characteristics								
Supply Voltage	Single Supply		See Typical Performance Characteristics		+8.0	+12	+26	V
	Split Supplies				±4	±6	±13	V
Supply Current	Single Supply		Measured at pin 1, S1 open (See Fig. 8)			5.0	7.0	mA
	Split Supplies	Positive	Measured at pin 1, S1 open (See Fig. 7)	RC2207		5.0	7.0	mA
				RM2207			8.0	
		Negative	Measured at pin 12, S1, S2 open	RC2207			7.0	mA
				RM2207		4.0	6.0	
Binary Keying Inputs								
Switching Threshold			Measured at pins 8 and 9. Refer to pin 10.		1.4	2.2	2.8	V
Input Resistance						5.0		kΩ
Oscillator Section—Frequency Characteristics								
Upper Frequency Limit			C = 500 pF, R3 = 2 kΩ		0.5	1.0		MHz
Lower Practical Frequency			C = 50 μF, R3 = 2 kΩ			0.01		Hz
Frequency Accuracy						±1.0	±3.0	% of f_0
Frequency Matching						0.5		% of f_0
Frequency Stability	vs. Temperature (Note 1)		0°C < T_A < +70°C			20	50	ppm/°C
	vs. Supply Voltage					0.15		%/V
Sweep Range			R3 = 1.5 kΩ for f_H R3 = 2 MΩ for f_L		1000:1	3000:1		f_H/f_L
Sweep Linearity			C = 5000 pF					
	10:1 Sweep[1]		f_H = 10 kHz, f_L = 1 kHz			1.0	2.0	%
	1000:1 Sweep		f_H = 100 kHz, f_L = 100 Hz			5.0		%
FM Distortion			±10% FM Deviation			0.1		%
Recommended Range of Timing Resistors			See Characteristic Curves		1.5		2000	kΩ
Impedance at Timing Pins			Measured at pins 4, 5, 6, or 7			75		Ω
DC Level at Timing Terminals						10		mV
Output Characteristics								
Triangle output	Amplitude		Measured at pin 14		4	6		V_{P-P}
	Impedance					10		Ω
	DC Level		Referenced to pin 10			+100		mV
	Linearity		from 10% to 90% of swing			0.1		%
Squarewave Output	Amplitude		Measured at pin 13, S2 Closed		11	12		V_{P-P}
	Saturation Voltage		Referenced to pin 12			0.2	0.4	V
	Rise Time		C_L ≤ 10 pF			200		ns
	Fall Time		C_L ≤ 10 pF			20		ns

Note:

1. Guaranteed by design.

Typical Performance Characteristics

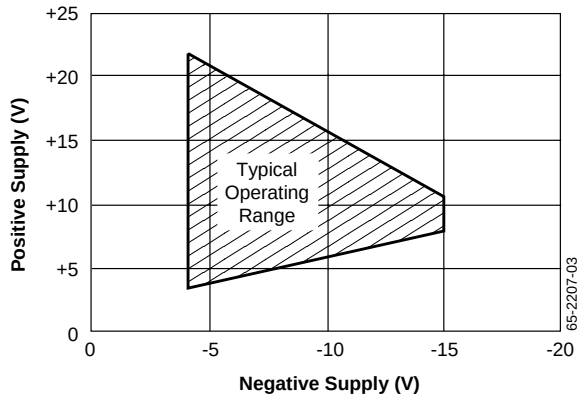


Figure 1. Typical Operating Range for Split Supply Voltage

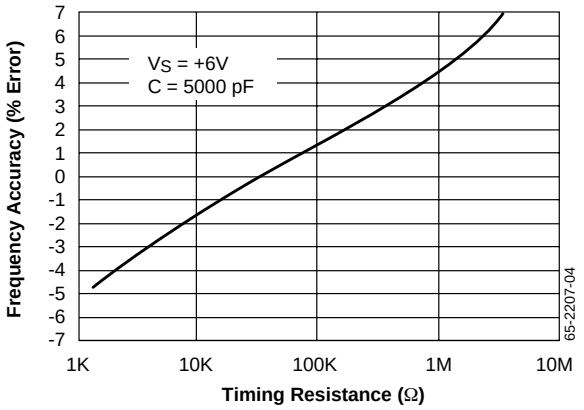
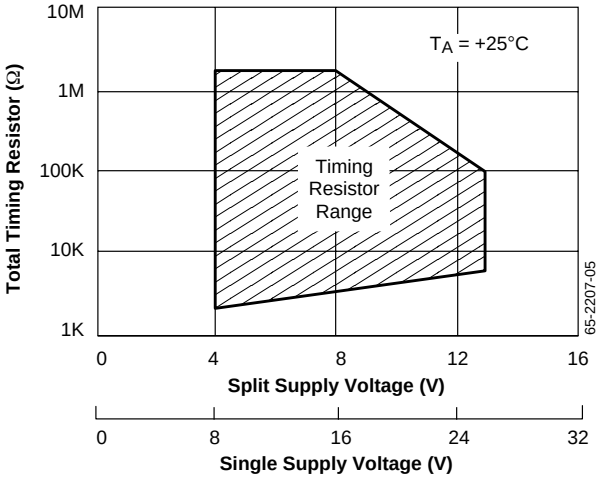


Figure 2. Frequency Accuracy vs. Timing Resistance



[1]R_T = Parallel Combination of Activated Timing Resistors

Figure 3. Recommended Timing Resistor Value vs. Power Supply Voltage

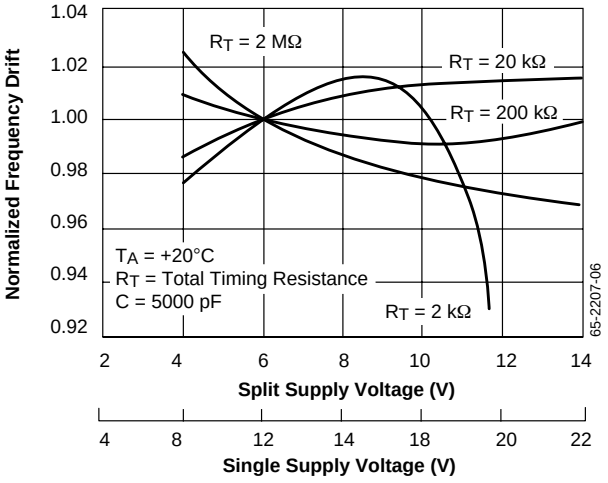


Figure 4. Normalized Frequency Drift vs. Supply Voltage

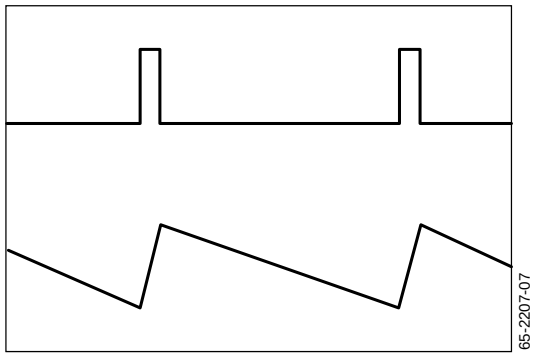


Figure 5. Pulse and Sawtooth Outputs

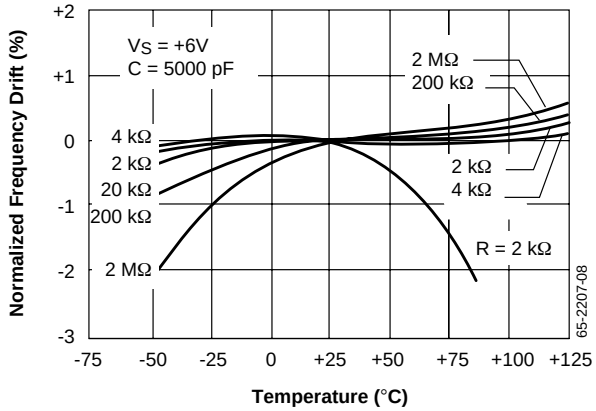


Figure 6. Normalized Frequency Drift vs. Temperature

Applications Information

Precautions

The following precautions should be observed when operating the RC2207 family of integrated circuits:

- Pulling excessive current from the timing terminals will adversely affect the temperature stability of the circuit. To minimize this disturbance, it is recommended that the total current drawn from pins 4, 5, 6 and 7 be limited to <6 mA. In addition, permanent damage to the device may occur if the total timing current exceeds 10 mA.
- Terminals 2, 3, 4, 5, 6 and 7 have very low internal impedance and should, therefore, be protected from accidental shorting to ground or the supply voltages.
- The keying logic pulse amplitude should not exceed the supply voltage.

Split Supply Operation

Figure 7 is the recommended circuit connection for split supply operation. The frequency of operation is determined by the timing capacitor (C) and the activated timing resistors (R1 through R4). The timing resistors are activated by the logic signals at the binary keying inputs (pins 8 and 9), as shown in Table 1. If a single timing resistor activated, the frequency is 1/RC.

Otherwise, the frequency is either 1/(R1| |R2)C or 1/(R1| |R4)C.

Table 1. Logic Table for Binary Keying Controls

Logic Level		Selected Timing Pins	Frequency	Definitions
8	9			
0	6	f1	$f_1 = 1/R3C$	$\Delta f1 = 1/R4C$
0	1	6 & 7	$f_1 + \Delta f_1$	$f_2 = 1/R2C$, $\Delta f_2 = 1/R1C$
1	0	5	f2	Logic levels: 0 = Ground
14	&5	f2 + fΔ2	Logic levels:	1 = ≥3V

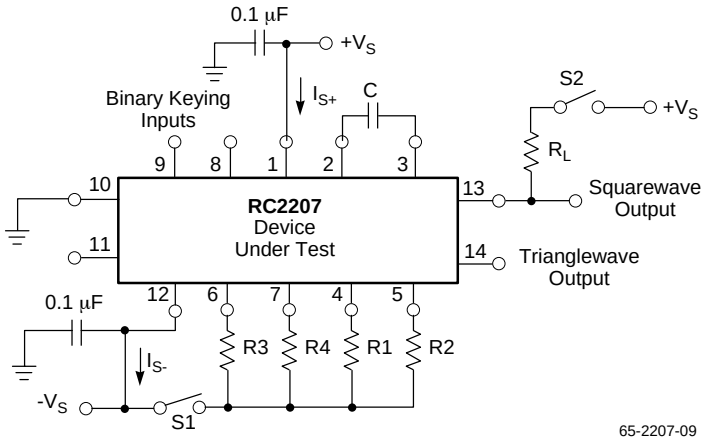
Note:
1. For single supply operation, logic levels are referenced to voltage at pin 10.

The squarewave output is obtained at pin 13 and has a peak-to-peak voltage swing equal to the supply voltages. This output is an open-collector type and requires an external pull-up load resistor (nominally 5 kΩ) to the positive supply. The triangle waveform obtained at pin 14 is centered about ground and has a peak amplitude of $+V_S/2$.

The circuit operates with supply voltages ranging from ±4V to it ±13V. Minimum drift occurs with ±6V supplies.

Single Supply Operation

The circuit should be interconnected as shown in Figure 8 for single supply operation. Pin 12 should be grounded, and pin 11 biased from $+V_S$ through a resistive divider to a value of bias voltage between $+V_S/3$ and $+V_S/2$. Pin 10 is bypassed to ground through a 0.1μF capacitor.



Note: This circuit is for Bench Tests only. DC testing is normally performed with automated test equipment using an equivalent circuit.

Figure 7. Test Circuit for Split Supply Operation

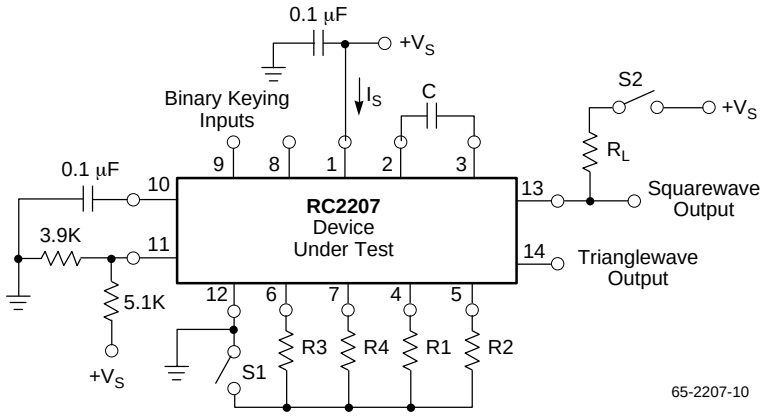


Figure 8. Test Circuit for Single Supply Operation

For single supply operation, the DC voltage at pin 10 and the timing terminals (pins 4 through 7) are equal and approximately 0.6V above V_B, the bias voltage at pin 11 . The logic levels at the binary keying terminals are referenced to the voltage at pin 10.

On-Off Keying

The RC2207 can be keyed on and off by simply activating an open circuited timing pin. Under certain conditions, the circuit may exhibit very low frequency (<1 Hz) residual oscillation in the off state due to internal bias current. If this effect is undesirable, it can be eliminated by connecting a 10 MΩ resistor from pin 3 to + V_S.

Frequency Control (Sweep and FM)

The frequency of operation is controlled by varying the total timing current, I_T, drawn from the activated timing pin 4, 5, 6 or 7. The timing current can be modulated by applying a control voltage, V_C, to the activated timing pin through a series resistor R_C as shown in Figure 9.

For split supply operation, a negative control voltage, V_C, applied to the circuit of Figure 9 causes the total timing current, I_T, and the frequency, to increase.

As an example, in the circuit of Figure 9, the binary keying inputs are grounded. Therefore, only timing pin 6 is activated.

The frequency of operation determined by:

$$f = \frac{1}{R3C_B}\left[1 - \frac{V_C R3}{(R_C)(-V_C)}\right] Hz$$

Pulse and Sawtooth Operation

The duty cycle of the output waveforms can be controlled by frequency shift keying at the end of every half cycle of oscillator output. This is accomplished by connecting one or both of the binary keying inputs (pin 8 or 9) to the squarewave output at pin 13. The output waveforms can then be converted to positive or negative pulses and sawtooth waveform.

Figure 10 is the recommended circuit connection for duty cycle control. Pin 8 is shorted to pin 13 so that the circuit switches between the 0 0 and the 1 0 logic states given in Table 1. Timing pin 5 is activated when the output is high, and pin 6 is activated when the squarewave output goes to a low state.

The duty cycle of the output waveforms given as:

$$\text{Duty Cycle} = \frac{R2}{R2 + R3}$$

and can be varied from 0.1% to 99.9% by proper choice of timing resistors. The frequency of oscillation, f, is given as:

$$f = \frac{2}{C}\left[\frac{1}{R2 + R3}\right]$$

The frequency can be modulated or swept without changing the duty cycle by connecting R2 and R3 to a common control voltage V_C instead of to -V_S. The sawtooth and the pulse output waveforms are shown in the Typical Performance Characteristics Graphs.

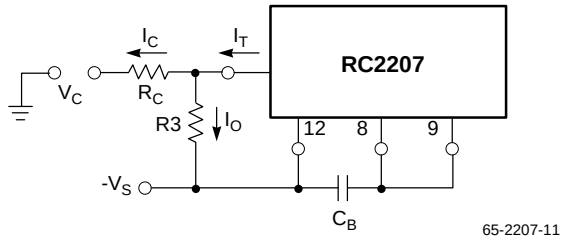


Figure 9. Frequency Sweep Operation

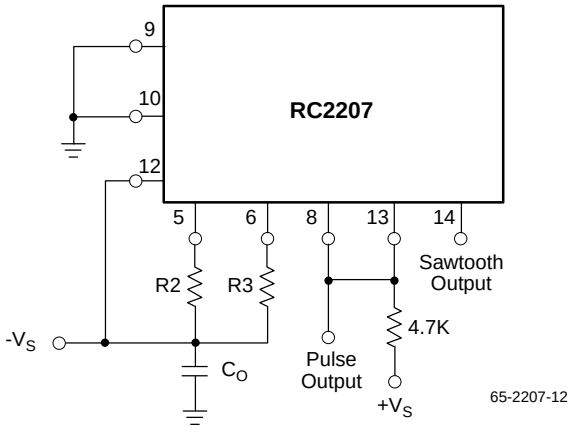


Figure 10. Pulse and Sawtooth Generation

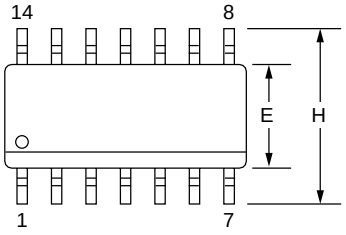
Mechanical Dimensions

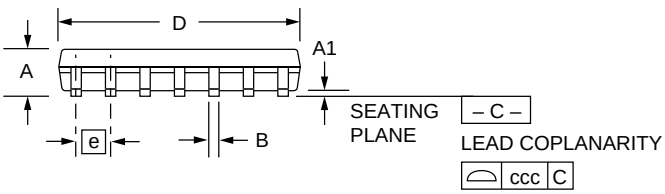
14-Lead SOIC

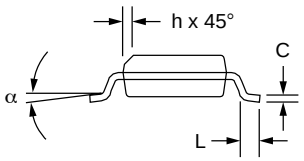
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.19	0.25	5
D	.336	.345	8.54	8.76	2
E	.150	.158	3.81	4.01	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	14		14		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







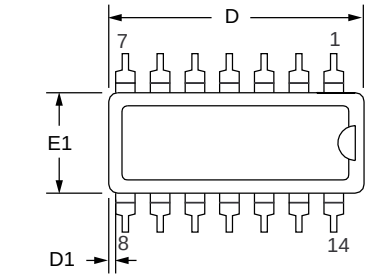
Mechanical Dimensions (continued)

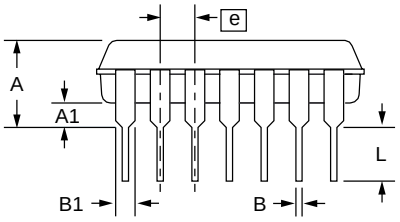
14-Lead Plastic DIP

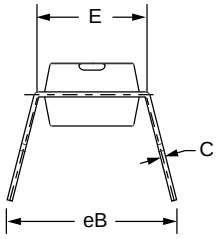
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	.725	.795	18.42	20.19	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.200	2.92	5.08	
N	14		14		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are shown for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.







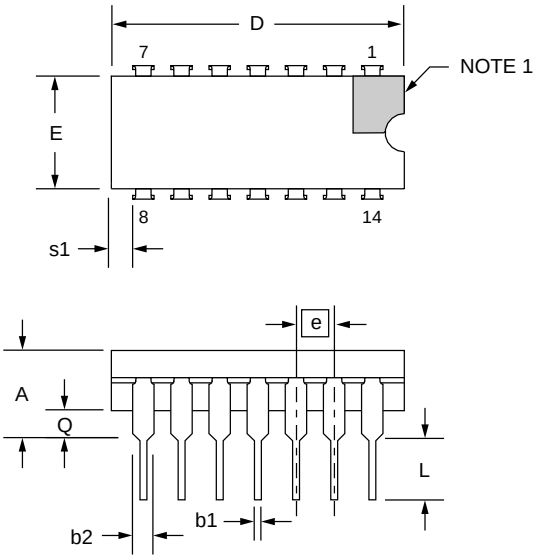
Mechanical Dimensions (continued)

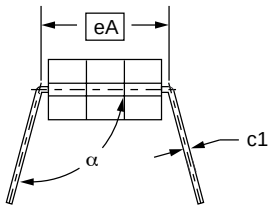
14-Lead Ceramic DIP

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2
c1	.008	.015	.20	.38	8
D	—	.785	—	19.94	4
E	.220	.310	5.59	7.87	4
e	.100 BSC		2.54 BSC		5, 9
eA	.300 BSC		7.62 BSC		7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 7, 8 and 14 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 14.
6. Applies to all four corners (leads number 1, 7, 8, and 14).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Twelve spaces.





Ordering Information

Part Number	Package	Operating Temperature Range
RC2207M	14 Lead SOIC	0°C to +70°C
RC2207N	14 Lead Plastic DIP	0°C to +70°C
RV2207M	14 Lead SOIC	-25°C to +85°C
RV2207N	14 Lead Plastic DIP	-25°C to +85°C
RM2207D	14 Lead Ceramic DIP	-55°C to +125°C
RM2207D/883B	14 Lead Ceramic DIP	-55°C to +125°C

Note:

1. /883B suffix denotes MIL-STD-883, Level B processing

5/20/98 0.0m 001
Stock#DS30002207

Embedded Secure Document

The file *http://www.fairchildsemi.com/ds/RC/RC2211.pdf* is a secure document that has been embedded in this document. Double click the pushpin to view RC2211.pdf.

RC2211A

FSK Demodulator/Tone Decoder

Features

- Wide frequency range – 0.01 Hz to 300 kHz
- Wide supply voltage range – 4.5V to 20V
- DTL/TTL/ECL logic compatibility
- FSK demodulation with carrier-detector
- Wide dynamic range – 2 mV to 3 V_{RMS}
- Adjustable tracking range – ±1% to ±80%
- Excellent temperature stability – 20 ppm/°C typical

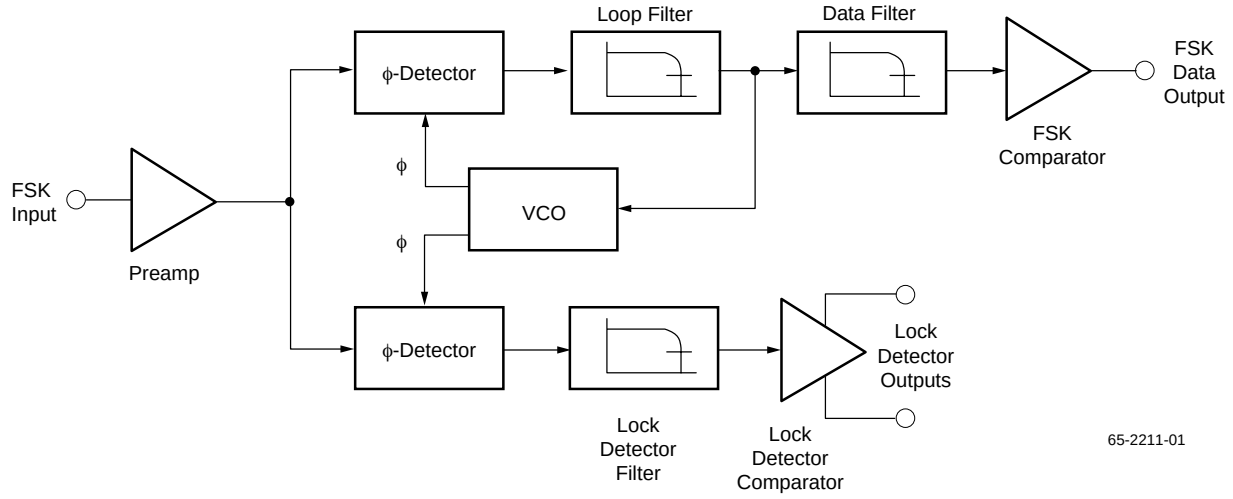
Applications

- FSK demodulation
- Data synchronization
- Tone decoding
- FM detection
- Carrier detection

Description

The RC2211A is a monolithic phase-locked loop (PLL) system especially designed for data communications. It is particularly well-suited for FSK modem applications, and operates over a wide frequency range of 0.01 Hz to 300 kHz. It can accommodate analog signals between 2 mV and 3V, and can interface with conventional DTL, TTL and ECL logic families. The circuit consists of a basic PLL for tracking an input signal frequency within the passband, a quadrature phase detector which provides carrier detection, and an FSK voltage comparator which provides FSK demodulation. External components are used to independently set carrier frequency, bandwidth and output delay.

Block Diagram



Functional Description

Signal Input (Pin 2)

The input signal is AC coupled to this terminal. The internal impedance at pin 2 is 20 kΩ. Recommended input signal level is in the range of 10 mV_{RMS} to 3 V_{RMS}.

Quadrature Phase Detector Output, Q (Pin 3)

This is the high impedance output of the quadrature phase detector, and is internally connected to the input of lock detector voltage comparator. In tone detection applications, pin 3 is connected to ground through a parallel combination of R_D and C_D (see Figure 1) to eliminate chatter at the lock detector outputs. If this tone detector section is not used, pin 3 can be left open circuited.

Lock Detector Output, Q (Pin 5)

The output at pin 5 is at a "high" state when the PLL is out of lock and goes to a "low" or conducting state when the PLL is locked. It is an open collector output and requires a pull-up resistor, R_L, to $+V_S$ for proper operation. In the "low" state it can sink up to 5 mA of load current.

Lock Detector Complement, $\overline{Q}$ (Pin 6)

The output at pin 6 is the logic complement of the lock detector output at pin 5. This output is also an open collector type stage which can sink 5 mA of load current in the low or "on" state.

FSK Data Output (Pin 7)

This output is an open collector stage which requires a pull-up resistor, R_L, to $+V_S$ for proper operation. It can sink 5 mA of load current. When decoding FSK signals the FSK data output will switch to a "high" or off state for low input frequency, and will switch to a "low" or on state for high input frequency. If no input signal is present, the logic state at pin 7 is indeterminate.

FSK Comparator Input (Pin 8)

This is the high impedance input to the FSK voltage comparator. Normally, an FSK post detection or data filter is connected between this terminal and the PLL phase detector output (pin 11). This data filter is formed by R_F and C_F of Figure 1. The threshold voltage of the comparator is set by the internal reference voltage, V_R, available at pin 10.

Reference Bypass (Pin 9)

This pin can have an optional 0.1 μF capacitor connected to the ground.

Reference Voltage, V_R (Pin 10)

This pin is internally biased at the reference voltage level, V_R; $V_R = +V_S/2 - 650$ mV. The DC voltage level at this pin forms an internal reference for the voltage levels at pin 3, 8, 11 and 12. Pin 10 must be bypassed to ground with a 0.1 μF capacitor.

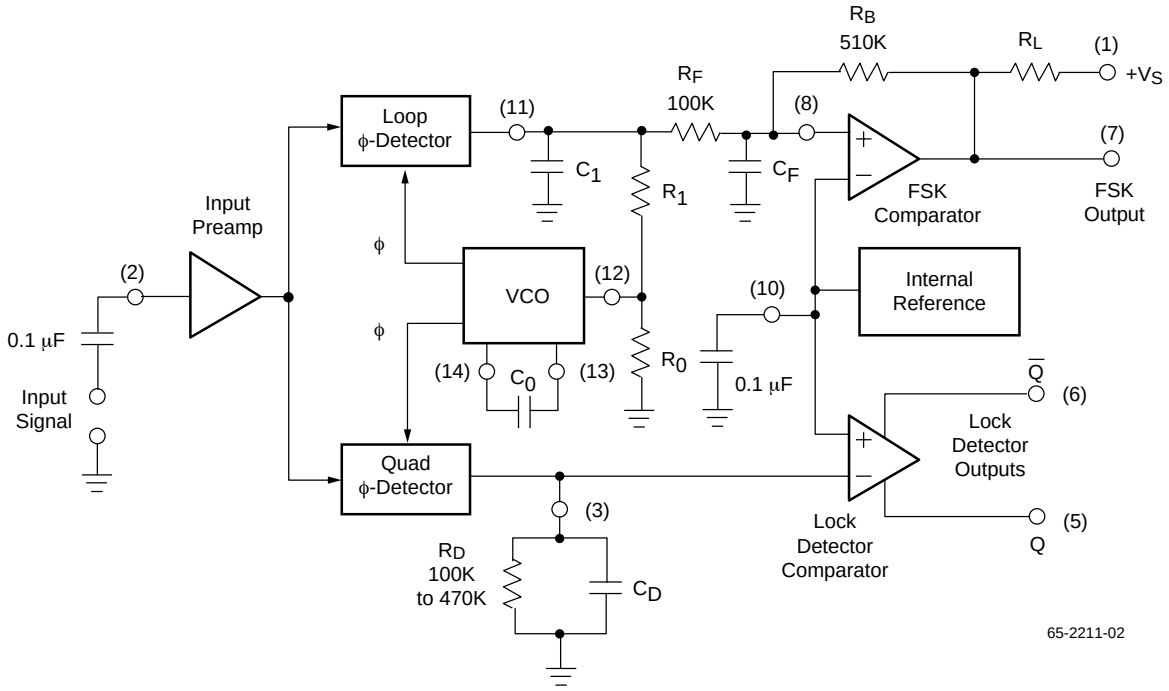


Figure 1. Generalized Circuit Connection for FSK and Tone Detection

Loop Phase Detector Output (Pin 11)

This terminal provides a high impedance output for the loop phase detector. The PLL loop filter is formed by R1 and C1 connected to pin 11 (see Figure 1). With no input signal, or with no phase error within the PLL, the DC level at pin 11 is very nearly equal to V_R. The peak voltage swing available at the phase detector output is equal to $\pm V_R$.

VCO Control Input (Pin 12)

VCO free running frequency is determined by external timing resistor, R0, connected from this terminal to ground. The VCO free running frequency, F_0 is given by:

$$F_0(\text{Hz}) = \frac{1}{R_0 C_0}$$

where C_0 is the timing capacitor across pins 13 and 14. For optimum temperature stability R_0 must be in the range of 10 kΩ to 100 kΩ (see Typical Performance Characteristics).

This terminal is a low impedance point, and is internally biased at a DC level equal to V_R. The maximum timing current drawn from pin 12 must be limited to ≤3 mA for proper operation of the circuit.

VCO Timing Capacitor (Pins 13 and 14)

VCO frequency is inversely proportional to the external timing capacitor, C_0, connected across these terminals. C_0 must be non-polarized, and in the range of 200 pF to 10 μF.

VCO Frequency Adjustment

VCO can be fine tuned by connecting a potentiometer, Rx, in series with R_0 at pin 12 (see Figure 2).

VCO Free-Running Frequency, F_0

The RC2211A does not have a separate VCO output terminal. Instead, the VCO outputs are internally connected to the phase detector sections of the circuit. However, for set-up or adjustment purposes, the VCO freerunning frequency can be measured at pin 3 (with C_D disconnected) with no input and with pin 2 shorted to pin 10.

Design Equations

See Figure 1 for Definitions of Components.

1. VCO Center Frequency, F_0:

$$F_0(\text{Hz}) = \frac{1}{R_0 C_0}$$

2. Internal Reference Voltage, V_R (measured at pin 10)

$$V_R = \left(\frac{+V_S}{2}\right) - 650\ \text{mV}$$

3. Loop Lowpass Filter Time Constant, τ

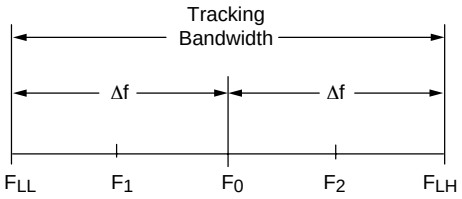
$$\tau = R_1 C_1$$

4. Loop Dampening, ζ:

$$\zeta = \left(\sqrt{\frac{C_0}{C_1}}\right)\left(\frac{1}{4}\right)$$

5. Loop Tracking Bandwidth, $\pm\Delta F/F_0$:

$\Delta f/F_O = R0/R1$



65-2211-03

6. FSK Data Filter Time Constant, τ_F:

$$\tau_F = R_F C_F$$

7. Loop Phase Detector Conversion Gain, Kϕ (Kϕ is the differential DC voltage across pins 10 and 11, per unit of phase error at phase-detector input):

$$k\phi(\text{in volts per radian}) = \frac{(-2)(V_R)}{\pi}$$

8. VCO Conversion Gain, K_0 is the amount of change in VCO frequency per unit of DC voltage change at pin 11:

$$K0(\text{in Hertz per volt}) = \frac{-1}{C_0 R_1 V_R}$$

9. Total Loop Gain, K_T:

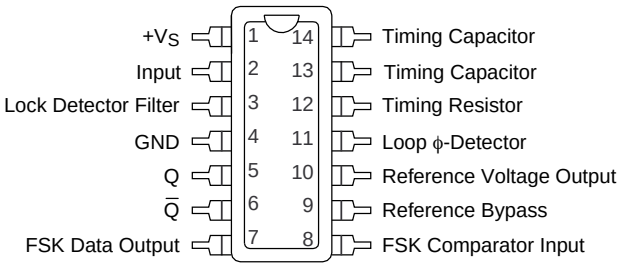
K_T (in radians per second per volt)= $2\pi K\phi K0$

$$= \frac{4}{C_0 R_1}$$

10. Peak Phase Detector Current, I_A:

$$I_A(\text{mA}) = \frac{V_R}{25}$$

Pin Assignments



65-2211-04

Absolute Maximum Ratings

Parameter	Conditions	Min.	Max.	Unit
Supply Voltage			+20	V
Input Signal Level			3	V_{RMS}
Storage Temperature Range		-65	+150	°C
Operating Temperature Range	RV2211A	-25	+85	°C
	RC2211A	0	+70	°C
Junction Temperature			+125	°C
Lead Soldering Temperature (60 sec.)			+300	°C
Max. P_D T_A<50°C			468	mW

Thermal Characteristics

Parameter	14 Lead Plastic DIP	14 Lead SOIC
Therm. Res. θ_{JA}	92°C/W	150°C/W

Electrical Characteristics

(Test Conditions $+V_S$ = +12V, T_A +25°C, R_0 = 30 kΩ, C_0 = 0.033 μF. See Figure 1 for component designations.)

Parameters	Test Conditlons	RV2211A			RC2211A			Units
		Min.	Typ.	Max.	Min.	Typ .	Max.	
General								
Supply Voltage[2]		4.5		20	4.5		20	V
Supply Current	$R_0 \geq 10$ kΩ		5.0	11.0		5.0	11	mA
Oscillator								
Frequency Accuracy	Deviation from $f_0 = 1/R_0C_0$		±1.0	±3.0		±1.0	±5	%
Frequency Stability[1]								
Temperature Coefficient	$R_1 = \infty$		±20			±20		ppm/°C
Power Supply Rejection	$+V_S$ = 12 ±1V $+V_S$ = 5 ±0.5V		0.05 0.2	0.5	 0.2	0.05	0.5	%/V %/V
Upper Frequency Limit	R_0 = 8.2 kΩ, C_0 = 400 pF	100	300			300		kHz
Lowest Practical Operating Frequency[1]	R_0 = 2 MΩ, C_0 = 50 μF		0.01			0.01		Hz
Timing Resistor, R_0								
Operating Range		5.0		2000	5.0		2000	kΩ
Recommended Range		15		100	15		100	kΩ
Loop Phase Detector								
Peak Output Current	Measured at pin 11	±150	±200	±300	±100	±200	±300	μA
Output Offset Current			±1.0			±2.0		μA
Output Impedance			1.0			1.0		MΩ
Maximum Swing	Ref. to pin 10	±4.0	±5.0		±4.0	±5.0		V
Quadrature Phase Detector								
Peak Output Current[3]	Measured at pin 3	100	150			150		μA
Output Impedance			1.0			1.0		MΩ
Maximum Swing			11			11		V_{P-P}
Input Preamp								
Input Impedance	Measured at pin 2		18			18		kΩ
Input Signal Voltage Required to Cause Limiting[3]	V_S = +6V f = 1.7 kHz	2.0	1.0		2.0	1.0		mV_{RMS}
Voltage Comparator								
Input Impedance	Measured at pins 3 & 8		2.0			2.0		MΩ
Input Bias Current			100			100		nA
Voltage Gain[1]	R_L = 5.1 kΩ	55	70		55	70		dB
Output Voltage Low	I_C = 3mA		300			300		mV
Output Leakage Current	V_0 = 12V		0.01			0.01		μA
Internal Reference								
Voltage Level	Measured at pin 10	4.9	5.3	5.7	4.75	5.3	5.85	V
Output Impedance			100			100		Ω

Notes:

1. Guaranteed by design.
2. Individual applications may need special circuitry to function at <12V.
3. Sample tested.

Typical Performance Characteristics

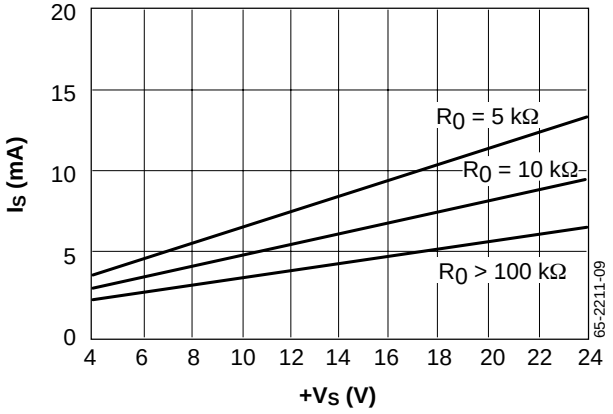


Figure 6. Supply Current vs. Supply Voltage (Logic Outputs Open Circuited)

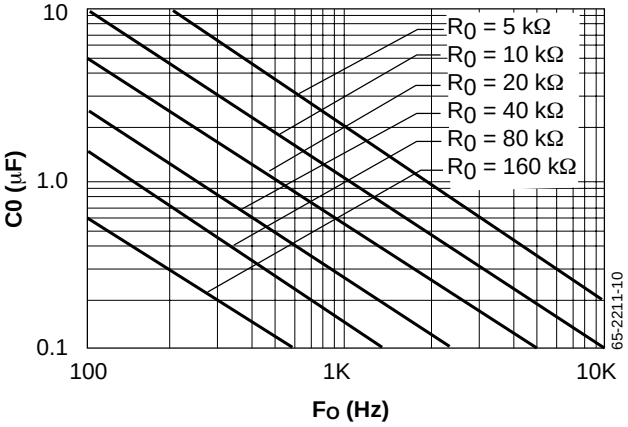


Figure 7. Timing Resistor with Timing Capacitor vs. VCO Frequency

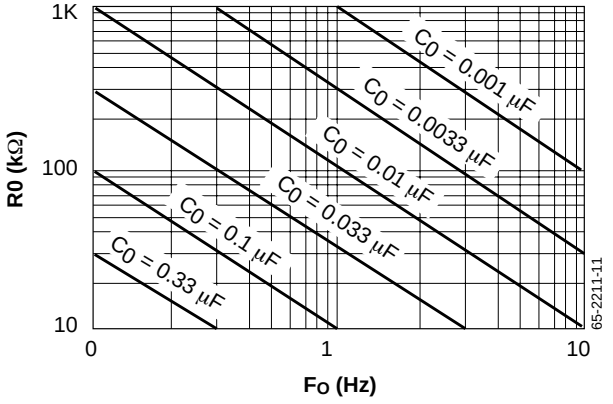


Figure 8. Timing Capacitor with Timing Resistor vs. VCO Frequency

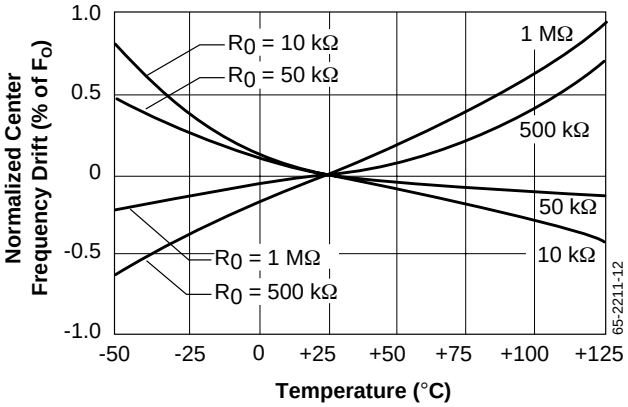
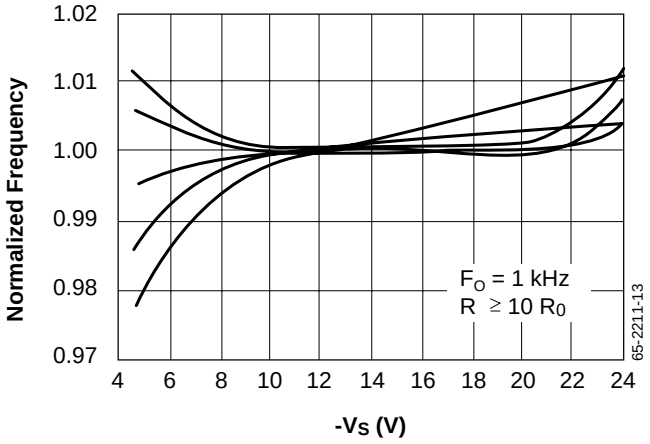


Figure 9. Center Frequency Drift vs. Temperature



Curve	R_0
1	5K
2	10K
3	30K
4	100K
5	300K

Figure 10. VCO Frequency vs. Supply Voltage

Applications Discussion

FSK Decoding

Figure 2 shows the basic circuit connection for FSK decoding. With reference to Figures 1 and 2, the functions of external components are defined as follows: R_0 and C_0 set the PLL center frequency, R_1 sets the system bandwidth, and C_1 sets the loop filter time constant and the loop damping factor. C_F and R_F form a one pole post-detection filter for the FSK data output. The resistor R_B (510 kΩ) from pin 7 to pin 8 introduces positive feedback across FSK comparator to facilitate rapid transition between output logic states.

Recommended component values for some of the most commonly used FSK bauds are given in Table 1.

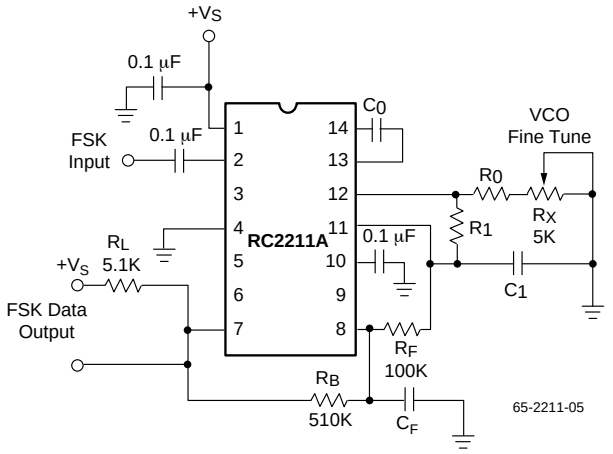


Figure 2. Circuit Connection for FSK Decoding

Table 1. Recommended Component Values for Commonly Used FSK Bands
(see Circuit of Figure 2)

FSK Band	Component Values
300 Baud	C_0 = 0.039 µF, C_F = 0.005 µF
F_1 = 1070 Hz	C_1 = 0.01 µF, R_0 = 18 kΩ
F_2 = 1270 Hz	R_1 = 100 kΩ
300 Baud	C_0 = 0.022 µF, C_F = 0.005 µF
F_1 = 2025 Hz	C_1 = 0.0047 µF, R_0 = 18 kΩ
F_2 = 2225 Hz	R_1 = 200 kΩ
1200 Baud	C_0 = 0.027 µF, C_F = 0.0022 µF
F_1 = 1200 Hz	C_1 = 0.01 µF, R_0 = 18 kΩ
F_2 = 2200 Hz	R_1 = 30 kΩ

Design Instructions

The circuit of Figure 2 can be tailored for any FSK decoding application by the choice of five key circuit components: R_0, R_1, C_0, C_1 and C_F. For a given set of FSK mark and space frequencies, F_1 and F_2, these parameters can be calculated as follows:

1. Calculate PLL center frequency, F_0

   $$F_0 = \frac{F_1 + F_2}{2}$$

2. Choose a value of timing resistor R_0 to be in the range of 10 kΩ to 100 kΩ. This choice is arbitrary. The recommended value is R_0 = 20 kΩ. The final value of R_0 ios normally finetuned with the series potentiometer, R_X.

3. Calculate value of C_0 from Design Equation No. 1 or from Typical Performance Characteristics:

   $C_0 = 1/R_0F_0$

4. Calculate R_1 to give a Δf equal to the markspace deviation:

   $R_1 = R_0 [F_0/(F_1 - F_2)]$

5. Calculate C_1 to set loop damping. (See Design Equation No. 4)

   Normally, $\zeta \approx 1/2$ is recommended
   Then: $C_1 = C_0/4$ for $\zeta = 1/2$

6. Calculate Data Filter Capacitance, C_F:
   For R_F = 100 kΩ, R_B = 510 kΩ, the recommended value of C_F is:

   $$C_F(\text{in } \mu F) = \frac{3}{\text{Baud Rate}}$$

Note: All calculated component values except R_0 can be rounded off to the nearest standard value, and R_0 can be varied to fine-tune center frequency through a series potentiometer, R_X (see Figure 2).

Design Example

75 Baud FSK demodulator with mark space frequencies of 1110/1170 Hz:

Step 1: Calculate F_0:
F_0=(1110+1170)(1/2)= 1140Hz

Step 2: Choose R_0 = 20 kΩ (18 kΩ fixed resistor in series with 5 kΩ potentiometer)

Step 3: Calculate C_0 from VCO Frequency vs. Timing Capacitor: C_9 = 0.044µF

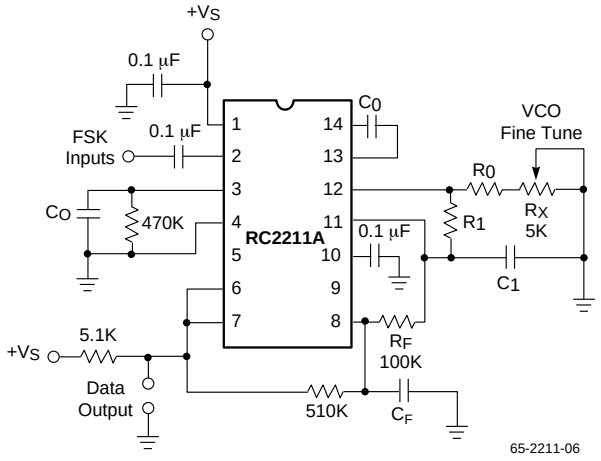
Step 4: Calculate R_1: $R_1 = R_0$ (1140/60) = 380 kΩ

Step 5: Calculate C_1: $C_1 = C_0/4$ = 0.011 µF

Note: All values except R_0 can be rounded off to nearest standard value.

FSK Decoding with Carrier Detector

The lock detector section of the RC2211A can be used as a carrier detector option for FSK decoding. The recommended circuit connection for this application is shown in Figure 3. The open-collector lock detector output, pin 6, is shorted to the data output (pin 7). Thus, the data output will be disabled at "low" state, until there is a carrier within the detection band of the PLL, and the pin 6 output goes "high" to enable the data output.



Note: Data output is "low" when no carrier is present.

Figure 3. External Connections for FSK Demodulation with Carrier Detector Capability

The minimum value of the lock detector filter capacitance C_D is inversely proportional to the capture range, $\pm\Delta f_C$. This is the range of incoming frequencies over which the loop can acquire lock and is always less than the tracking range. It is further limited by C_1. For most applications, $\Delta F_C < \Delta F/2$. For R_D = 470 kΩ, the approximate minimum value of C_D can be determined by:

$$C_D(\mu F) \geq 16/\text{capture range in Hz}$$

With values of C_D that are too small, chatter can be observed on the lock detector output as an incoming signal frequency approaches the capture bandwidth. Excessively large values of C_D will slow the response time of the lock detector output.

Tone Detection

Figure 4 shows the generalized circuit connection for tone detection. The logic outputs, Q and $\overline{Q}$ at pins 5 and 6 are normally at "high" and "low" logic states, respectively. When a tone is present within the detection band of the PLL, the logic state at these outputs becomes reversed to the duration of the input tone. Each logic output can sink 5 mA of load current.

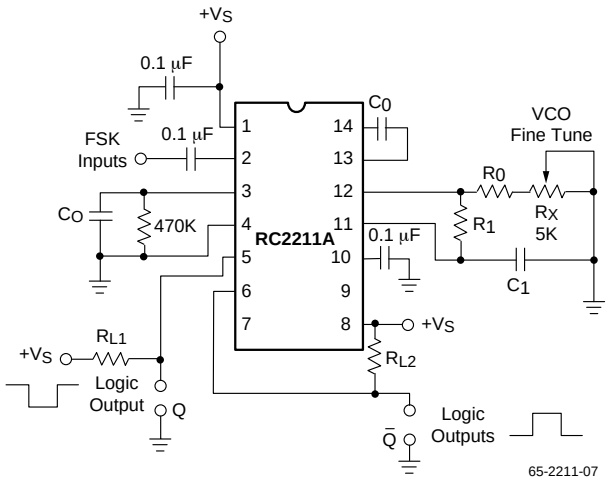


Figure 4. Circuit Connection for Tone Detection

Both logic outputs at pins 5 and 6 are open-collector type stages, and require external pull-up resistors R_{L1} and R_{L2} as shown in Figure 4.

With reference to Figures 1 and 4, the function of the external circuit components can be explained as follows: R_0 and C_0 set VCO center frequency, R_1 sets the detection bandwidth, C_1 sets the lowpass-loop filter time constant and the loop dampening factor, and R_{L1} and R_{L2} are the respective pull-up resistors for the Q and $\overline{Q}$ logic outputs.

Design Instructions

The circuit of Figure 4 can be optimized for any tone-detection application by the choice of five key circuit components: R_0, R_1, C_0, C_1 and C_D. For a given input tone frequency, F_S, these parameters are calculated as follows:

1. Choose R_0 to be in the range of 15 kΩ to 100 kΩ. This choice is arbitrary.
2. Calculate C_0 to set center frequency, f_0 equal to F_S: $C_0 = 1/R_0F_S$.
3. Calculate R_1 to set bandwidth $\pm\Delta F$ (see Design Equation No. 5): $R_1 = R_0(F_0/\Delta F)$. Note: The total detection bandwidth covers the frequency range of $F_0 \pm \Delta F$.
4. Calculate value of C_1 for a given loop damping factor:

   $C_1 = C_0/16\zeta^2$

   Normally $\zeta = 1/2$ is optimum for most tone detector applications, giving $C_1 = 0.25\ C0$.

   Increasing C_1 improves the out-of-band signal rejection, but increases the PLL capture time.
5. Calculate value of filter capacitor C_D. To avoid chatter at the logic output, with R_D = 470Ω, C_D must be:

   $C_D(\mu F) \geq (16/\text{capture range in Hz})$

   Increasing C_D slows the logic output response time.

Design Examples

Tone detector with a detection band of 1 kHz ±20 Hz:

Step 1: Choose R_0 = 20 kΩ (18 kΩ in series with 5 kΩ potentiometer) .

Step 2: Choose C_0 for F_0 = 1 kHz: C_0 = 0.05 μF.

Step 3: Calculate R_1: $R_1 = (R_0)\ (1000/20)$ = 1 MΩ.

Step 4: Calculate C_1: for ζ = 1/2, C_1 = 0.25 μF, C_0 = 0.013 μF.

Step 5: Calculate C_D: C_D = 16/38 = 0.42 μF.

Step 6: Fine tune the center frequency with the 5 kΩ potentiometer. R_X.

Linear FM Detection

The RC2211A can be used as a linear FM detector for a wide range of analog communications and telemetry applications. The recommended circuit connection for the application is shown in Figure 5. The demodulated output is taken from the loop phase detector output (pin 11), through a post detection filter made up of R_F and C_F, and an external buffer amplifier. This buffer amplifier is necessary because of the high impedance output at pin 11. Normally, a non-inverting unity gain op amp can be used as a buffer amplifier, as shown in Figure 5.

The FM detector gain, i.e., the output voltage change per unit of FM deviation, can be given as:

$$V_{OUT} = R_1\ V_R/100\ R_0 \quad \text{Volts/\% deviation}$$

where V_R is the internal reference voltage. For the choice of external components R_1, R_0, C_0, C_1 and C_F, see the section on Design Instructions.

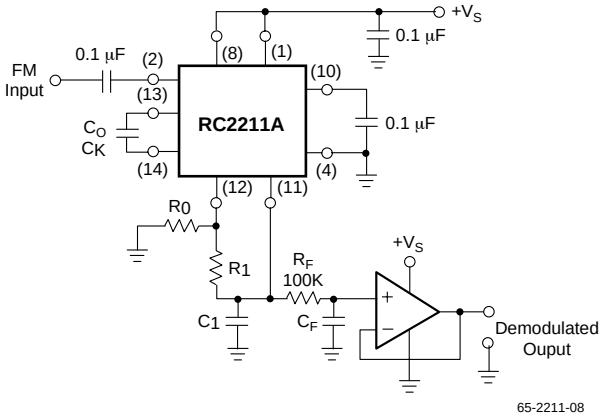


Figure 5. Linear FM Detector Using RC2211A and an External Op Amp

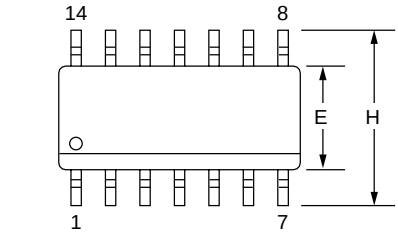
Mechanical Dimensions

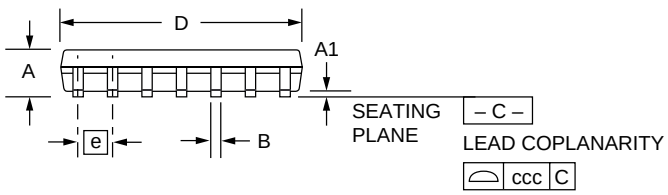
14-Pin SOIC Package

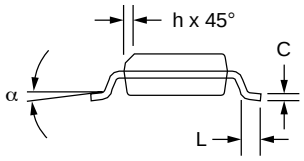
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.19	0.25	5
D	.336	.345	8.54	8.76	2
E	.150	.158	3.81	4.01	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	14		14		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







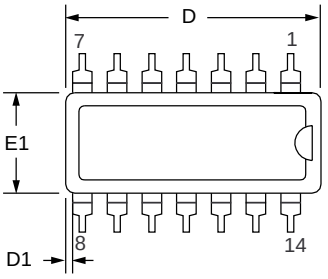
Mechanical Dimensions (continued)

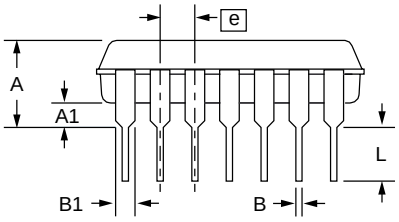
14-Lead Plastic DIP Package

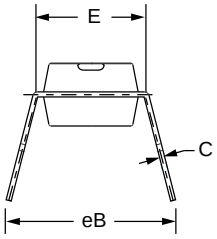
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	.725	.795	18.42	20.19	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.200	2.92	5.08	
N	14		14		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are shown for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.







Ordering Information

Part Number	Package	Operating Temperature Range
RC2211AN	14-Lead Plastic DIP	0°C to +70°C
RC2211AM	14-Lead Plastic SOIC	0°C to +70°C
RV2211AN	14-Lead Plastic DIP	-25°C to +85°C
RV2211AM	14-Lead Plastic SOIC	-25°C to +85°C

RC2798

Integrated QAM IF Downconverter

Features

- RF input frequency range 30 to 250MHz
- On chip VCO with LO frequency range 30 to 250MHz
- IF amplifier with AGC setting
- High dynamic range -9dBm IIP3
- On chip Video Amplifier
- Built in ESD protection
- Supply voltage range 5 to 10 V
- Space saving 20-Lead TSSOP package

Applications

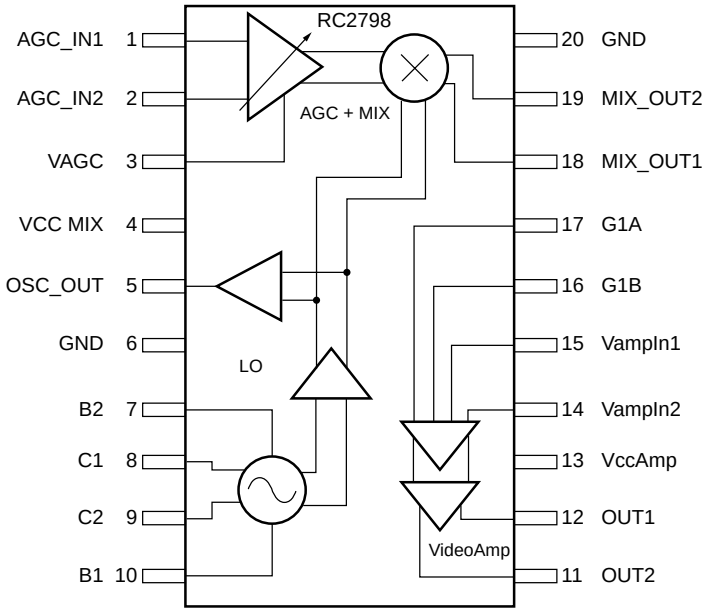
- Digital Set-top receivers
- Cable modems
- Internet surfboards
- Network Interface Modules
- Multimedia PCs

Description

The RC2798 is an integrated solution for the down-conversion of QAM IF signals in the front-end design of cable modem and set-top receivers. It is intended for use in 64QAM and 256QAM IF downconversion applications. The RC2798 integrates IF amplifier with AGC , mixer, VCO, and a video amplifier on a single chip. It accepts the QAM IF signals via SAW filter and downconverts it to 5MHz baseband signal.

The baseband signal can be digitized using Fairchild Semiconductor's 8 bit A/D (TMC1175 series) or 10bit A/D (TMC1185 series) and decoded further with a QAM demodulator. The IF, Oscillator and Mixer section work at 5V. The video amplifier works at 5V to 10V. The RC2798 is available in a 20 Lead TSSOP package.

Block Diagram



Absolute Maximum Ratings (T_A = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
Video Amplifier 5V Operation						
Vcc_Mix	Supply voltage 1 (for AGC amplifier, oscillator, and mixer)	AGC amplifier, oscillator, and mixer block			6	V
VccVamp	Supply voltage 2 (for video amplifier)	Video amplifier block			6	V
P_D	Power dissipation	T_A = 85°C[1]			430	mW
T_A	Operation temperature range		-40		+85	°C
Tstg	Storage temperature range		-55		+150	°C
Video Amplifier 9V Operation						
Vcc_Mix	Supply voltage 1 (for AGC amplifier, oscillator, and mixer)	AGC amplifier, oscillator, and mixer block			6	V
VccVamp	Supply voltage 2 (for video amplifier)	Video amplifier block			11	V
P_D	Power dissipation	T_A = 75°C[1]			500	mW
T_A	Operation temperature range		-40		+75	°C
Tstg	Storage temperature range		-55		+150	°C

Notes:

1. Mounted on 50 X 50 X 1.6mm double epoxy glasss board.

Recommended Operating Range

Parameter		Min.	Typ.	Max.	Unit
Vcc_Mix	Supply voltage 1 (for AGC amplifier, oscillator, and mixer)	4.5	5.0	5.5	V
VccVamp	Supply voltage 2 (for video amplifier)	4.5	5.0	10.0	V
Ta1	Operation temperature range 1[1]	-40	+25	+85	°C
Ta2	Operation temperature range 2[2]	-40	+25	+75	°C

Notes:

1. @ Vcc_Mix = VccVamp = 4.5 to 5.5V
2. @ Vcc_Mix = 4.5 to 5.5V, VccVamp = 4.5 to 10.0V

Electrical Characteristics (T_A = 25°C)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
AGC Amplifier, Oscillator, and Mixer Blocks (Vcc = 5V)						
Icc1	Supply current 1	no input signal	17.0	23.0	31.0	mA
f_{RF}	RF input frequency range		30		250	MHz
f_{OSC}	OSC frequency range		30		250	MHz
f_{IF}	IF output frequency range		DC		150	MHz
CG_{MAX}	Maximum conversion gain	V_{AGC} = 4.0V		25		dB
CG_{MIN}	Minimum conversion gain	V_{AGC} = 1.0V		-7		dB
GCR	AGC dynamic range	V_{AGC} = 1.0 to 4.0V	24	32	40	dB
NF	Noise figure	SSB, V_{AGC} = 4.0V At maximum gain		9		dB
V_{AGC} H	AGC voltage high level	At maximum gain	4.0			V
V_{AGC} L	AGC voltage low level	At minimum gain			1.0	V
Video Amplifier Block (Vcc = 5V)						
Icc2	Supply current 2	No input signal	7.0	12.5	17.0	mA
V_{OUT}	Output voltage	RL = 1KΩ, differential		3.0		Vp-p
G1	Differential gain 1	G1A-G1B pins: short, V_{OUT} = 3Vp-p	150	200	250	V/V
G2	Differential gain 2	G1A-G1B pins: open, V_{OUT} = 3Vp-p	22.0	26.0	30.0	V/V
Video Amplifier Block (Vcc = 9V)						
Icc2	Supply current 2	no input signal	18.0	24.0	32.0	mA
V_{OUT}	Output voltage	RL = 1KΩ, differential		3.0		Vp-p
G1	Differential gain 1	G1A-G1B pins: short, RL = 2KΩ	300	385	470	V/V
G2	Differential gain 2	G1A-G1B pins: open, RL = 2KΩ	25.0	28.5	32.0	V/V
Video Amplifier Block (Vcc = 5V or 9V)						
BW_{G1}	Bandwidth 1	G1		50		MHz
BW_{G2}	Bandwidth 2	G2		50		MHz
Rin1	Input resistance 1	G1		3.5		KΩ
Rin2	Input resistance 2	G2		7.5		KΩ
Cin	Input capacitance			1.6		pF

Standard Characteristics (V_{CC} = 5V, T_A = 25°C)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
AGC Amplifier Block (Vcc = 5V)						
AGC IIP3	AGC input intercept point	At minimum gain (AGC amplifier + mixer)		-9		dBm
Video Amplifier Block (Vcc = 5V or 9V)						
CMRR	Common mode rejection ratio			80		dB
PSRR	Power supply rejection ratio			70		dB
τ_r	Rise time			2.6		nS
τ_{PD}	Propagation delay time			4.4		nS

Typical Characteristics

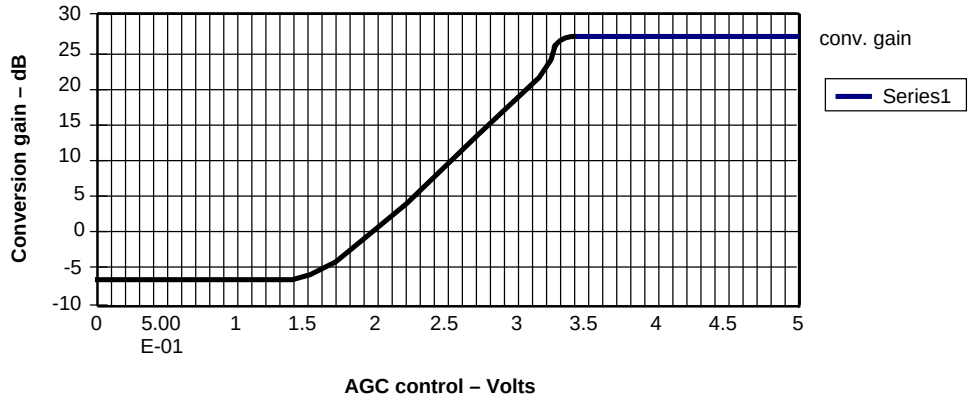


Figure 1. AGC Control Characteristics

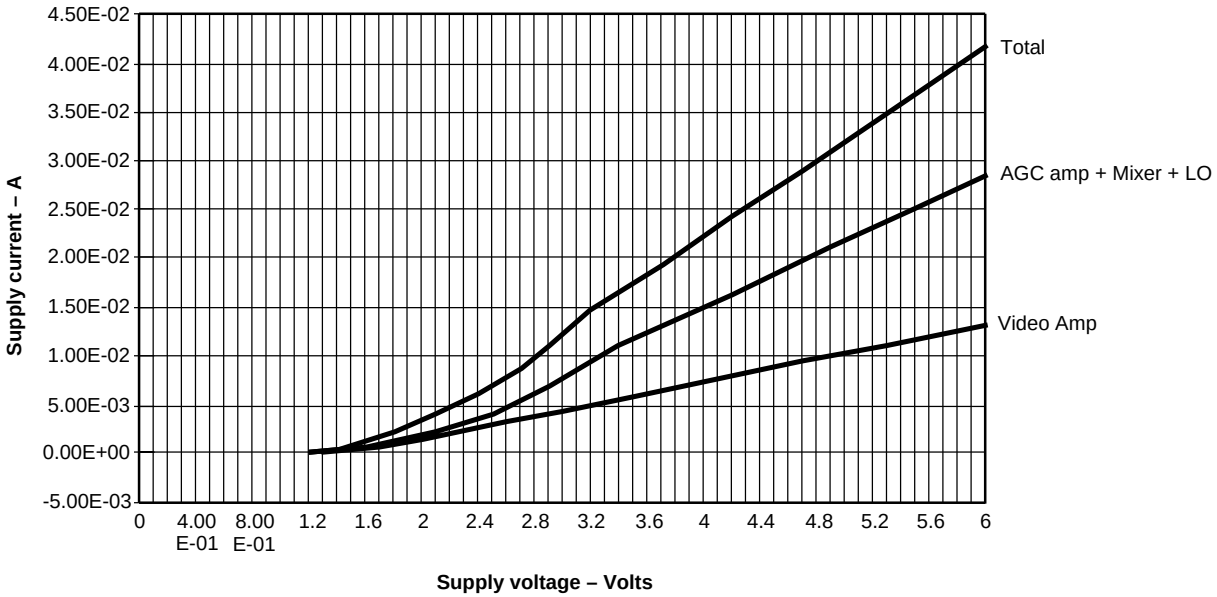


Figure 2. Supply Current vs. Supply Voltage

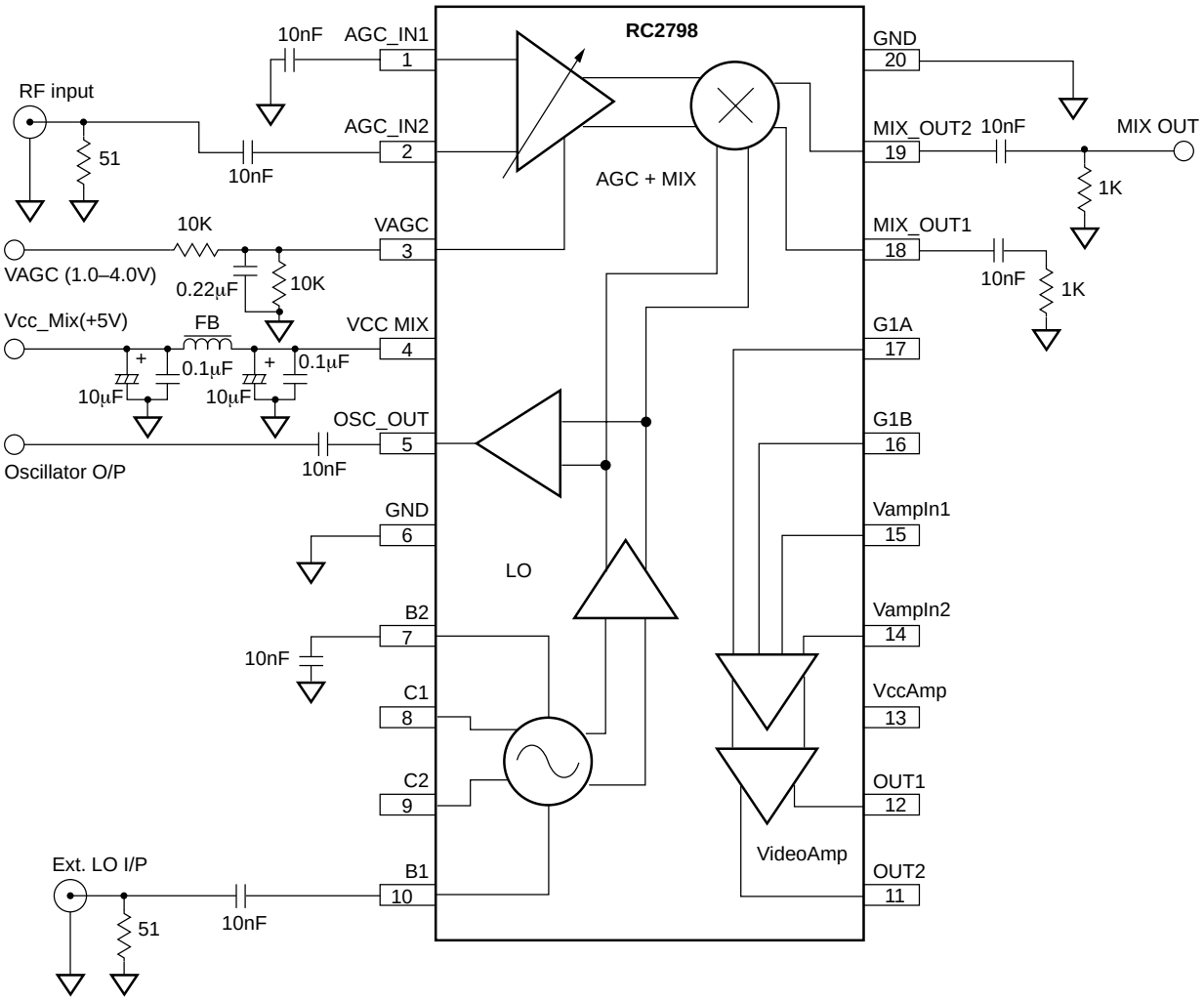


Figure 3. Measurement Circuit 1—AGC + MIX Block

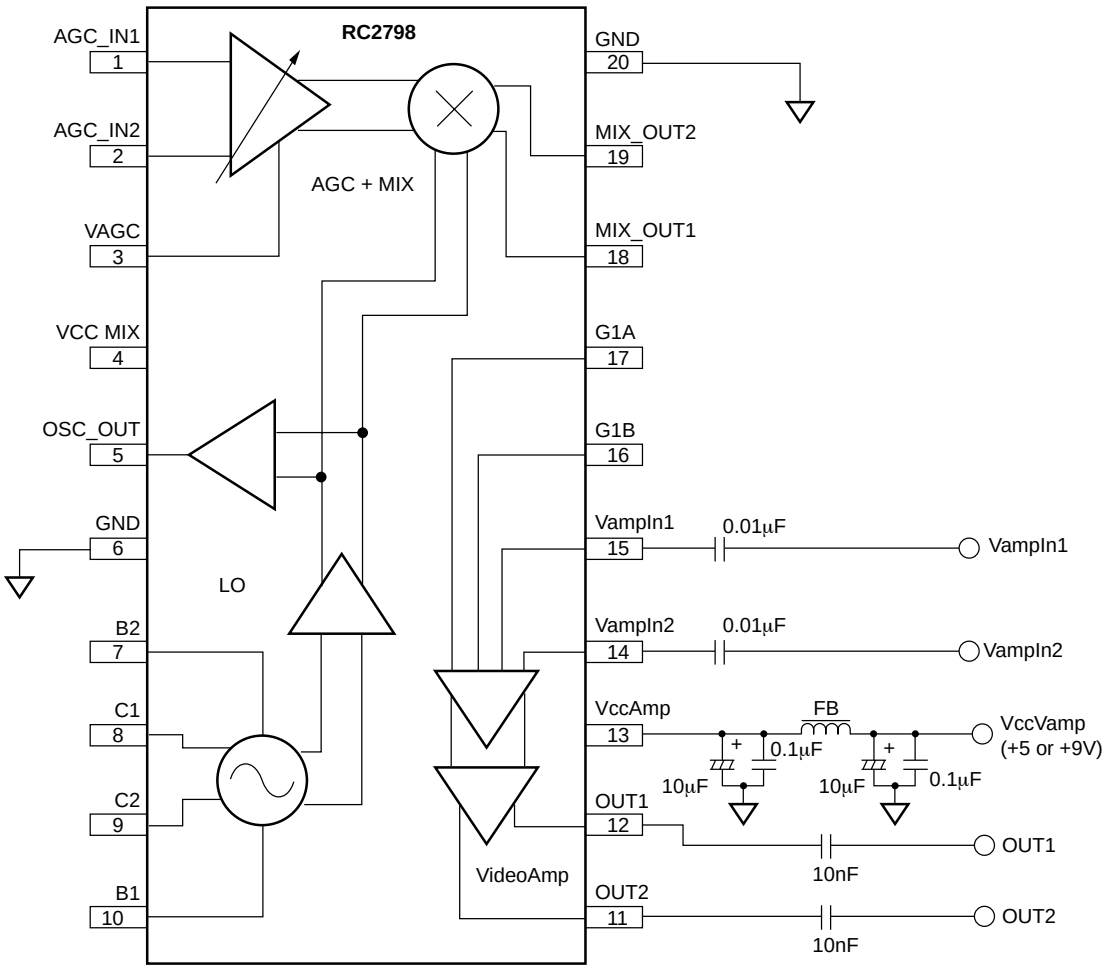
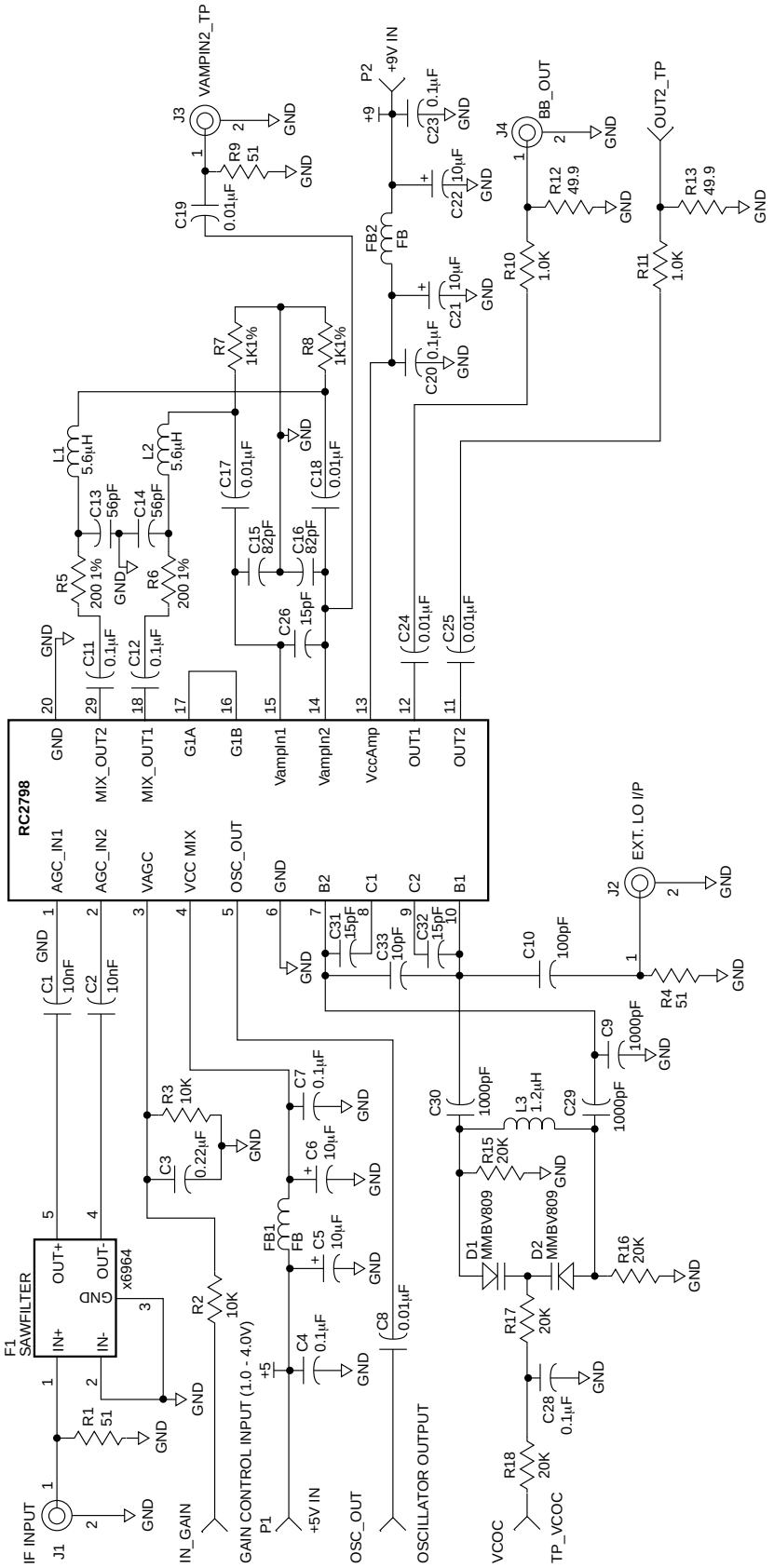


Figure 4. Measurement Circuit 2—Video Amplifier Block

Applications Discussion



Notes:
1. For self oscillation, do not load C9, and C10.
2. Fro external injection (VCO), do not load C28, C29, C30, C31, C32, C33, L3, D1, D2, R15, R16, R17, and R18.
3. For down convesion with video amplifier, do not load C19.
4. For using video amplifier only, do not load C17, C18, C16, C26, and change C15 to 0.1µF.

Figure 5. Application Circuit

Crystal Oscillator Implementation

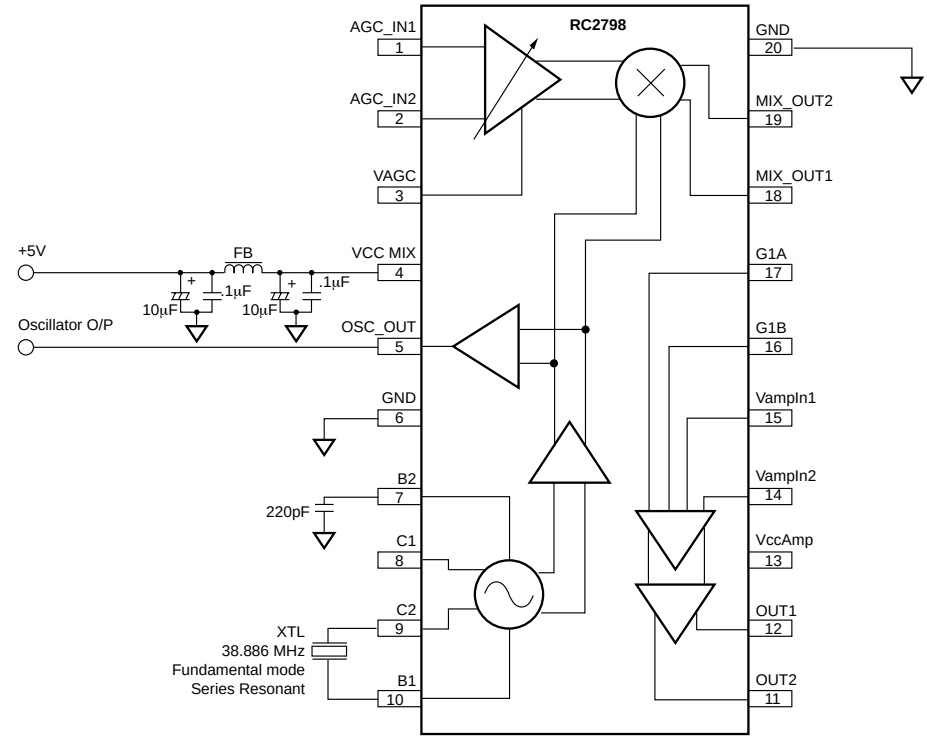


Figure 6. Fundamental Mode—Series Resonant XTL

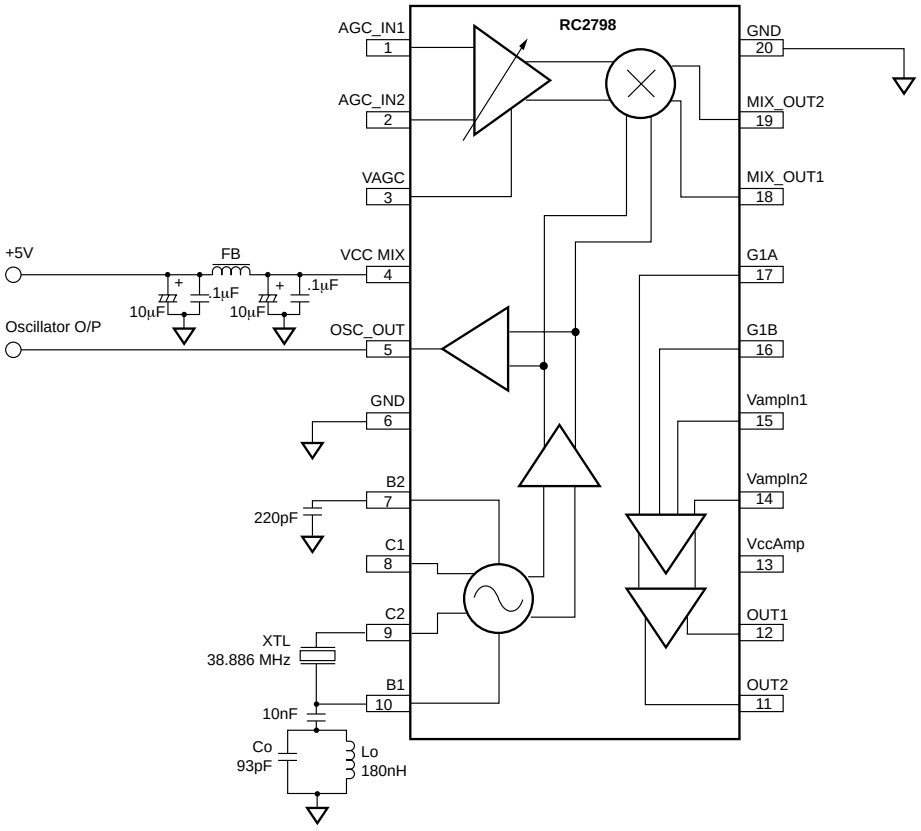


Figure 7. Overtone Mode—Series Resonant XTL

Overtone Mode—Series Resonant XTL

If it is desired to operate a XTL at non-fundamental or overtone frequency, an AC coupled parallel resonant network should be connected to feedback input pin, B1. The typical impedance looking into B1 with B2 AC grounded is approximately Rin =1KΩ @ 38MHz. It is recommended to design the value of Qo at approximately 15 to 25. The Lo and Co values can be calculated from the following equations:

$$Qo = \omega_o \, Co \, Rin$$

$$\omega_o = 2\pi \; fo = (1/LoCo)^{1/2}$$

The XTL is a series resonant type and it is operated at third overtone frequency.

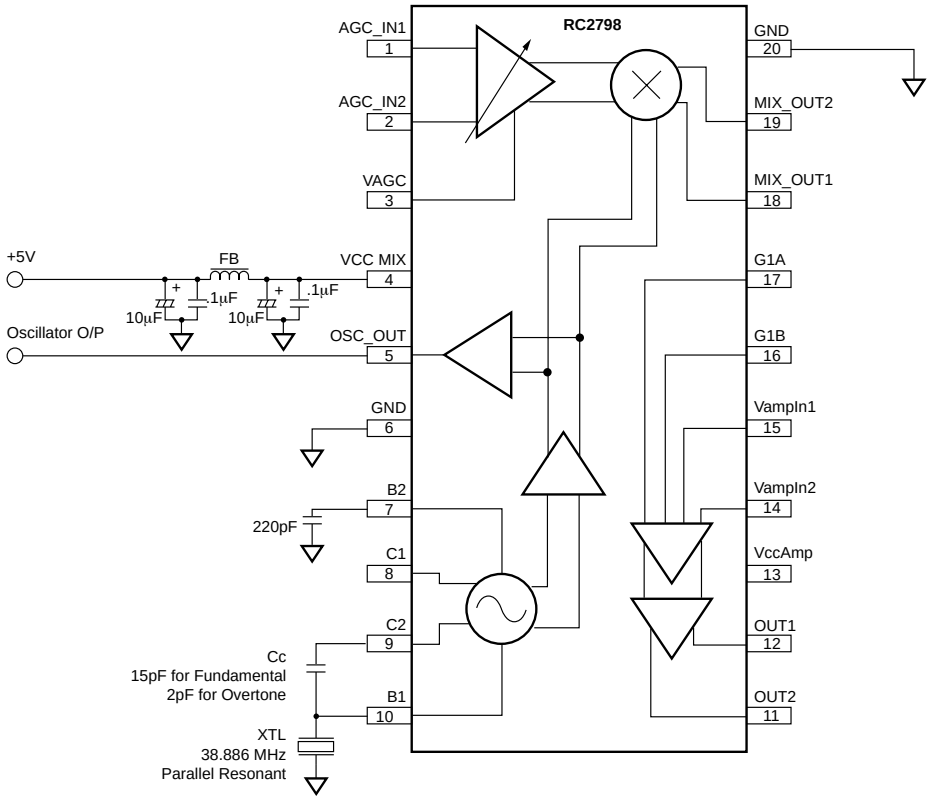


Figure 8. Fundamental or Overtone Mode—Parallel Resonant XTL

Fundamental or Overtone Mode– Parallel Resonant XTL

Figure 8 shows the implemenation of parallel resonant XTL at fundamental or overtone frequency. The XTL is a parallel resonant type and can be operated at either fundamental or third overtone frequency depending upon the feedback capacitor, Cc. When used with Cal Crystal Lab's XTL, P/N#CCL-6-38.8860G153, for Cc = 15pF it operates at fundamental mode and for Cc = 2pF, it operates at third overtone mode (38.886MHz).

For symmetrical reasons, the following design is recommended for better duty cycle (50 to 50%) output from VCO (see Figure 9).

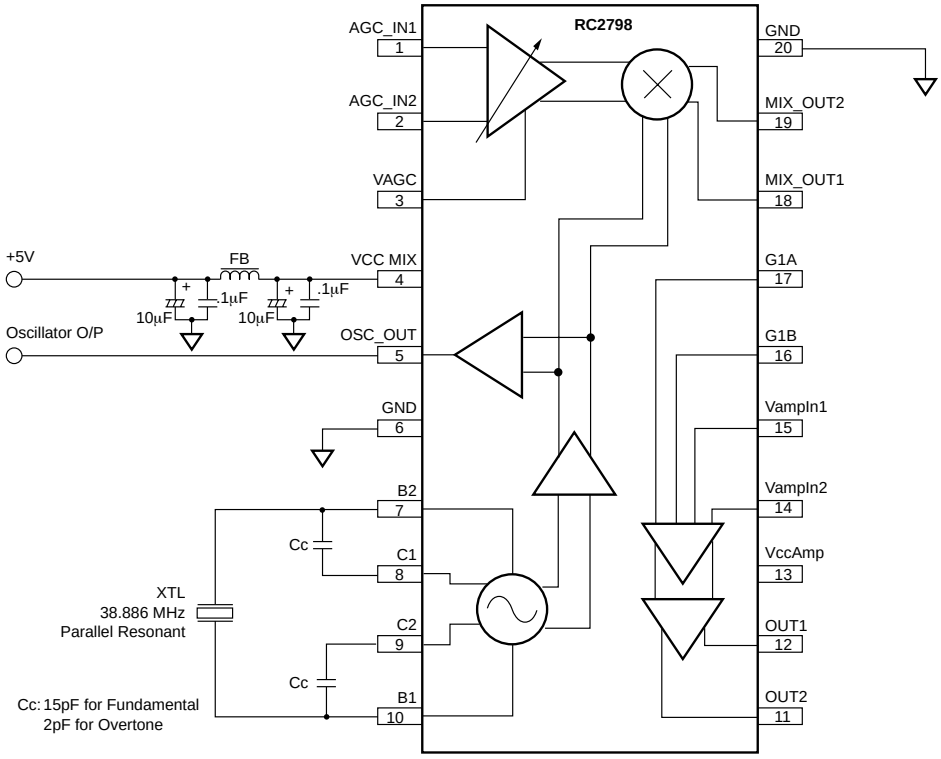


Figure 9. Fundamental or Overtone Mode with Improved Duty Cycle—Parallel Resonant XTL

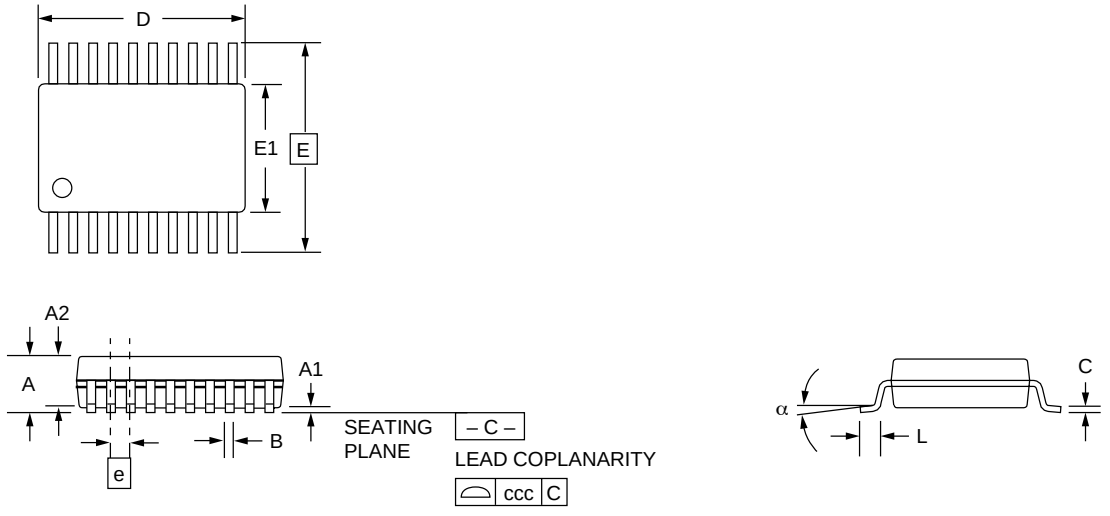
Package Dimensions

20-pin TSSOP package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.047	—	1.20	
A1	.002	.006	0.05	0.15	
A2	.031	.041	0.80	1.05	
B	.007	.012	0.19	0.30	5
C	.004	.008	0.09	0.20	5
D	.250	.257	6.40	6.60	2, 4
E	.240	.264	6.10	6.70	
E1	.168	.176	4.30	4.50	
e	.026 BSC		0.65 BSC		
L	.018	.029	0.45	0.75	3
N	20		20		6
α	0°	10°	0°	10°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "B" & "C" dimensions include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.



Ordering Information

Product Number	Package
RC2798G	20 pin TSSOP

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

5/20/98 0.0m 001
Stock#DS30002798

RC2951

Adjustable Micropower Voltage Regulator

Features

- High accuracy output voltage
- Guaranteed 100 mA output current
- Extremely low quiescent current
- Extremely tight load and line regulation
- Requires only a 1.0µF output capacitor for stability
- Internal Current and Thermal Limiting
- Error flag warns of output dropout
- Logic-controlled electronic shutdown
- Output programmable from 1.24 to 29V
- Fixed 3.3V version available
- 8 lead SOIC package

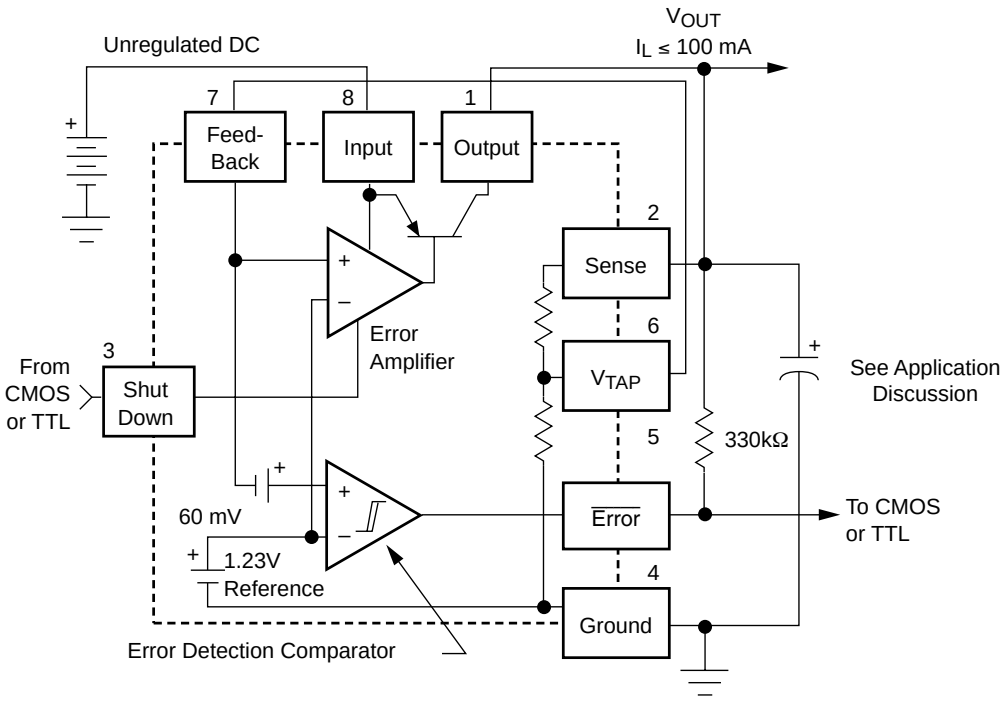
Description

The RC2951 is a voltage regulator specifically designed to maintain proper regulation with a very low dropout voltage (Typ. 40mV at light loads and 380 mV at 100mA). It has a low quiescent bias current of 75µA and is capable of supplying output currents in excess of 100mA. It has internal current and thermal limiting protection. The output can be programmed from 1.24V to 29V with two external resistors. A fixed output voltage (3.3V) is also available.

The error flag output can be used as power-on reset for warning of a low output voltage. The Shutdown input feature allows a logic level signal to turn on and off the regulator output. The RC2951 is ideally suited for battery powered computer, consumer, and industrial equipment where an extension of useful battery life is desirable. The RC2951 is available in an 8-pin SOIC package.

Preliminary Information

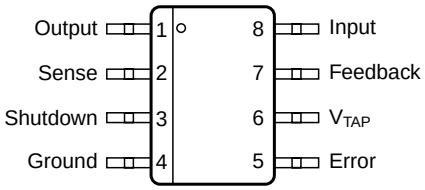
Block Diagram



Rev. 0.9.3

Pin Assignments

8 Lead SOIC Package



Top View

Absolute Maximum Ratings

Power Dissipation	Internally Limited
Lead Temp. (Soldering, 5 seconds)	260°C
Storage Temperature Range	–65° to +150°C
Operating Junction Temperature Range[1]	–55° to +150°C
Input Supply/Voltage	–0.3 to +30V
Feedback Input Voltage[2,3]	–1.5 to +30V
Shutdown Input Voltage[2]	–0.3 to +30V
Error Comparator Output Voltage[2]	–0.3 to +30V

Notes:

1. Junction to ambient thermal resistance for the S.O. (M) package is 160°C/W.
2. May exceed input supply voltage.
3. When used in dual-supply systems where the output terminal sees loads returned to a negative supply, the output voltage should be diode-clamped to ground.

Electrical Characteristics

The • denotes that the limits apply at temperature extremes.

Parameter	Conditions[1]		Typ.	Tested Limit[2]	Units
Output Voltage (RC2951M)	T_J = 25°C		5.0	5.025 4.975	V max V min
	-25°C ≤ T_J ≤ 85°C		5.0		V max V min
	Full Operating Temperature Range	• •	5.0	5.06 4.94	V max V min
Output Voltage (RC2951M)	100µA ≤ I_L ≤ 100mA T_J ≤ T_{JMAX}	• •	5.0	5.075 4.925	V max V min
Output Voltage (RC2951M-3.3)	T_J = 25°C		3.3	3.317 3.284	V max V min
	-25°C ≤ T_J ≤ 85°C		3.3		V max V min
	Full Operating Temperature Range	• •	3.3	3.340 3.260	V max V min
Output Voltage (RC2951M-3.3)	100µA ≤ I_L ≤ 100mA T_J ≤ T_{JMAX}	• •	3.3	3.346 3.254	V max V min
Output Voltage Temperature Coefficient[7]		•	20	120	ppm/°C

Preliminary Information

Electrical Characteristics (continued)

The • denotes that the limits apply at temperature extremes.

Parameter	Conditions[1]		Typ.	Tested Limit[2]	Units
Line Regulation[9, 10]	$(V_O NOM + 1)V \le V_{in} \le 20V$	•	0.03	0.1 0.5	% max % max
Load Regulation[9]	$100\ \mu A \le I_L \le 100$ mA	•	0.08	0.2 0.4	% max % max
Dropout Voltage[3]	$I_L = 100\ \mu A$	•	50	80 150	mV max mV max
	$I_L = 100$ mA	•	380	500 700	mV max mV max
Ground Current	$I_L = 100\ \mu A$	•	75	120 140	µA max µA max
	$I_L = 100$ mA	•	8	14 15	mA max mA max
Dropout Ground Current	$V_{in} = (V_O NOM - 0.5)V$ $I_L = 100\ \mu A$	•	110	250 300	µA max µA max
Current Limit	$V_{out} = 0$	•	160	200 220	mA max mA max
Thermal Regulation[8]			0.05	0.2	%/W max
Output Noise, 10 Hz to 100 KHz	$C_L = 1\ \mu F$ (5V Only)		430		µV rms
	$C_L = 200\ \mu F$		160		µV rms
	$C_L = 3.3\ \mu F$ (Bypass = 0.01 µF Pins 7 to 1 (RC2951)		100		µV rms
Reference Voltage		• •	1.235	1.25 1.26 1.22 1.2	V max V max V min V min
Reference Voltage[5]		• •		1.27 1.19	V max V min
Feedback Pin Bias Current		•	20	40 60	nA max nA max
Reference Voltage Temperature Coefficient[7]			20		ppm/°C
Feedback Pin Bias Current Temperature Coefficient			0.1		nA/°C
Error Comparator					
Output Leakage Current	$V_{OH} = 30V$	•	0.01	1 2	µA max µA max
Output Low Voltage	$V_{in} = (V_O NOM - 0.5)V$ $I_{OL} = 400\ \mu A$	•	150	250 400	mV max mV max
Upper Threshold Voltage[4]		•	60	40 25	mV min mV min
Lower Threshold Voltage[4]		•	75	95 140	mV max mV max
Hysteresis[4]			15		mV

Preliminary Information

Electrical Characteristics (continued)

The • denotes that the limits apply at temperature extremes.

Parameter	Conditions[1]		Typ.	Tested Limit[2]	Units
Shutdown Input					
Input Logic Voltage			1.3		V
	Low (Regulator ON)	•		0.6	V max
	High (Regulator OFF)	•		2.0	V min
Shutdown Pin Input Current	$V_{shutdown}$ = 2.4V		30	50	μA max
		•		100	μA max
	$V_{shutdown}$ = 30V		450	600	μA max
		•		750	μA max
Regulator Output Current in Shutdown[6]			3	10	μA max
		•		20	μA max

Notes:

1. Unless otherwise specified all limits guaranteed for T_J - 25°C, V_{in} = (V_ONOM + 1)V, I_L = 100μA and C_L = 1 μF for 5V versions, and 2.2 μF for 3V and 3.3V versions. Additional conditions for the 8-pin versions are Feedback tied to V_{TAP}, Output tied to Output Sense and $V_{shutdown}$ < 0.8V.
2. Guaranteed and 100% production tested.
3. Dropout Voltage is defined as the input to output differential at which the output voltage drops 100 mV below its nominal value measured at 1V differential. At very low values of programmed output voltage, the minimum input supply voltage of 2V (2.3V over temperature) must be taken into account.
4. Comparator thresholds are expressed in terms of a voltage differential at the Feedback terminal below the nominal reference voltage measured at V_{in} = (V_ONOM + 1)V. To express these thresholds in terms of output voltage change, multiply by the error amplifier gain = V_{out}/V_{ref} = (R1 + R2)/R2. For example, at a programmed output voltage of 5V, the Error output is guaranteed to go low when the output drops by 95 mV x 5V/1.235V = 384 mV. Thresholds remain constant as a percent of V_{out} as V_{out} is varied, with the dropout warning occurring at typically 5% below nominal, 7.5% guaranteed.
5. $V_{ref} < V_{out} \le (V_{in} - 1V)$, $2.3V \le V_{in} \le 30V$, $100\mu A \le I_L \le 100$ mA, $T_J \le T_{JMAX}$.
6. $V_{shutdown} \ge 2V$, $V_{in} \le 30V$, V_{out} = 0, Feedback pin tied to V_{TAP}.
7. Output or reference voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.
8. Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 50 mA load pulse at V_{IN} = 30V (1.25W pulse) for T = 10 ms.
9. Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.
10. Line regulation for the RC2951 is tested at 150°C for I_L = 1 mA. For I_L = 100 μA and T_J = 125°C, line regulation is guaranteed by design to 0.2%. See Typical Performance Characteristics for line regulation versus temperature and load current.

Applications Discussion

The RC2951 regulator is designed with internal current limiting and thermal shutdown. It is not internally compensated and requires a 1.0μF (or greater) capacitor between the output terminal and ground for stability. At lower output voltages, more capacitance is required (2.2μF or more is recommended for 3V and 3.3V versions) for stability. Most types of aluminum, tantalum or multilayer ceramic capacitors will perform adequately. Solid tantalums or appropriate multilayer ceramic capacitors are suggested for operation below 25°C. At lower values of output current, less capacitance is needed to maintain stability at output. The capacitor at the output can be reduced to 0.33μF for currents less that 10mA, or 0.1μF for currents below 1.0mA.

Using the adjustable versions at voltages below 5V runs the error amplifier at lower gains so that more output capacitance is needed. For the worst-case situation of a 100 mA load at 1.23V output (Output shorted to Feedback) a 3.3 μF (or greater) capacitor should be used.

When setting the output voltage of the RC2951 versions with external resistors, a minimum load of 1 μA is recommended. A 1 μF tantalum or aluminum electrolytic capacitor should be placed from the RC2951 input to ground if there is more than 10 inches of wire between the input and the AC filter capacitor or if a battery is used as the input.

Stray capacitance to the RC2951 Feedback terminal can cause instability. This may especially be a problem when using high value external resistors to set the output voltage. Adding a 100 pF capacitor between Output and Feedback and increasing the output capacitor to at least 3.3 μF will fix this problem.

Error Detection Comparator Output

The comparator switches to a logic low whenever the RC2951 output falls out of regulation by more than approximately 5%. This value is the comparator's built-in offset of about 60 mV divided by the 1.235 internal reference voltage. This trip level remains "5% below normal" regardless of the value of the output voltage. For example, the error flag trip level is typically 4.75V for a 5V output or 11.4V for a 12V output. The out of regulation condition may be due either to low input voltage, current limiting, or thermal limiting.

Figure 1 is a timing diagram showing the $\overline{\text{ERROR}}$ signal and the regulated output voltage as the RC2951 input is ramped up and down. For 5V versions, the $\overline{\text{ERROR}}$ signal becomes valid (low) at about 1.3V input. It goes high at about 5V input (the input voltage at which V_{OUT} = 4.75.) Since the RC2951's dropout voltage is load-dependent (see curve in typical performance characteristics), the input voltage trip point (about 5V) will vary with the load current. The output voltage trip point (approx. 4.75V) does not vary with load.

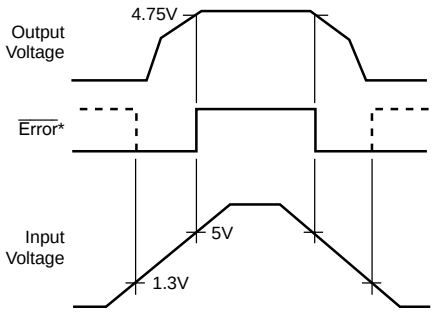


Figure 1. $\overline{\text{ERROR}}$ Output Timing

The error comparator has an open-collector output which requires an external pullup resistor. This resistor may be returned to the output or some other supply voltage depending on system requirements. In determining a value for this resistor, note that while the output is rated to sink 400 μA, this sink current adds to battery drain in a low battery condition. Suggested values range from 100k to 1MΩ. The resistor is not required if this output is unused.

Programming the Output Voltage (RC2951)

The RC2951 may be pin-strapped for the nominal fixed output voltage using its internal voltage divider by tying the output and sense pins together, and also tying the feedback and V_{TAP} pins together. Alternatively, it may be programmed for any output voltage between its 1.235V reference and its 30V maximum rating. As seen in Figure 2 an external pair of resistors is required.

Preliminary Information

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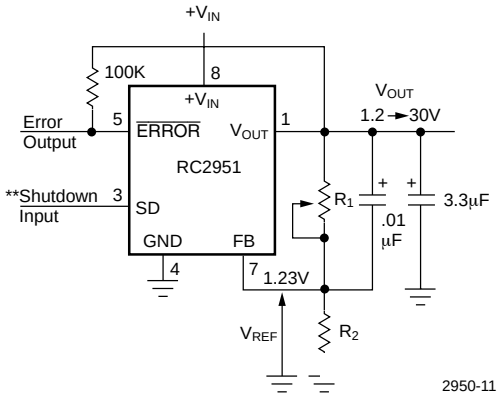


$$V_{OUT} = V_{REF}\left(1 + \frac{R_1}{R_2}\right)$$

** Drive with TTL-high to shut down. Ground or leave open if shutdown feature is not to be used.

Figure 2. Adjustable Regulator

The complete equation for the output voltage is

$$V_{OUT} = V_{REF} \bullet \left(1 + \frac{R_1}{R_2}\right) + I_{FB}R_1$$

$$\frac{V_{REF}}{R_2} = \frac{V_{OUT}}{R_1 + R_2}$$

$$V_{OUT} = V_{REF}\left(\frac{R_1 + R_2}{R_2}\right)$$

$$V_{OUT} = V_{REF}\left(1 + \frac{R_1}{R_2}\right)$$

Adding the error term,

$$V_{OUT} = V_{REF}\left(1 + \frac{R_1}{R_2}\right) + I_{FB}R_2$$

where V_{REF} is the nominal 1.235 reference voltage and I_{FB} is the feedback pin bias current, nominally -20 nA. The minimum recommended load current of 1 μA forces an upper limit of 1.2 MΩ on the value of R_2, if the regulator must work with no load (a condition often found in CMOS in standby). I_{FB} will produce a 2% typical error in V_{OUT} which may be eliminated at room temperature by trimming R_1. For better accuracy, choosing R_2 = 100k reduces this error to 0.17% while increasing the resistor program current to 12 μA. Since the RC2951 typically draws 60 μA at no load with Pin 2 open-circuited, this is a small price to pay.

Reducing Output Noise

In reference applications it may be advantageous to reduce the AC noise present at the output. One method is to reduce the regulator bandwidth by increasing the size of the output capacitor.

Noise can be reduced fourfold by a bypass capacitor across R_1, since it reduces the high frequency gain from 4 to unity. Pick

$$C_{BYPASS} \cong \frac{1}{2\pi R_1 \bullet 200\text{Hz}}$$

or about 0.01 μF. When doing this, the output capacitor must be increased to 3.3 μF to maintain stability. These changes reduce the output noise from 430 μV to 100 μV rms for a 100 kHz bandwidth at 5V output. With the bypass capacitor added, noise no longer scales with output voltage so that improvements are more dramatic at higher output voltages.

Typical Applications

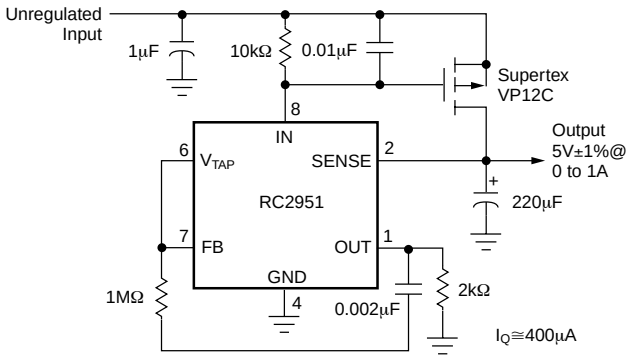


Figure 3. 1A Regulator with 1.2V Dropout

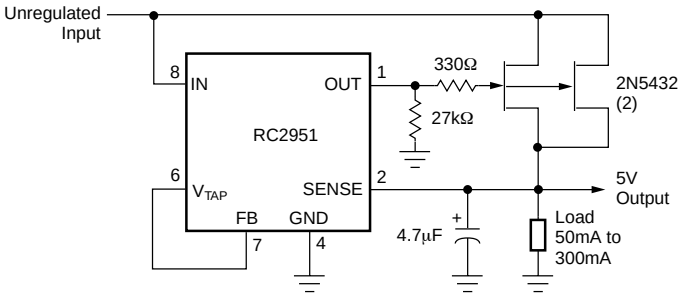
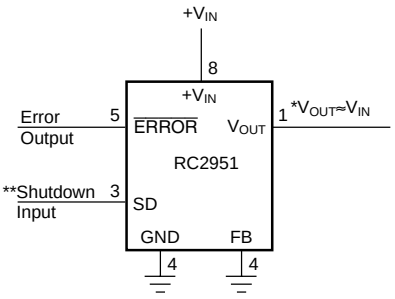


Figure 4. 300 mA Regulator with 0.75 Dropout



*Minimum input-output voltage ranges from 40 mV to 400 mV, depending on load current. Current limit is typically 160 mA.

Figure 5. Wide Input Voltage Range Current Limiter

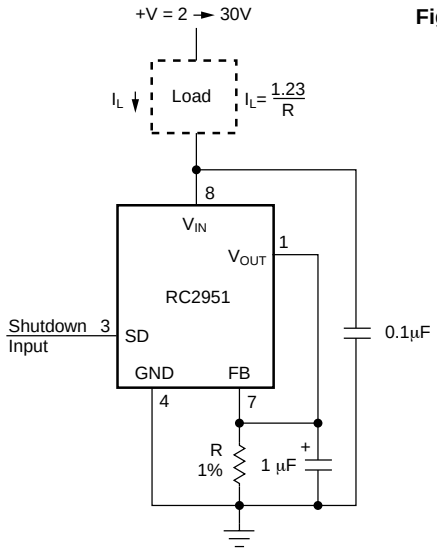


Figure 6. Low Drift Current Source

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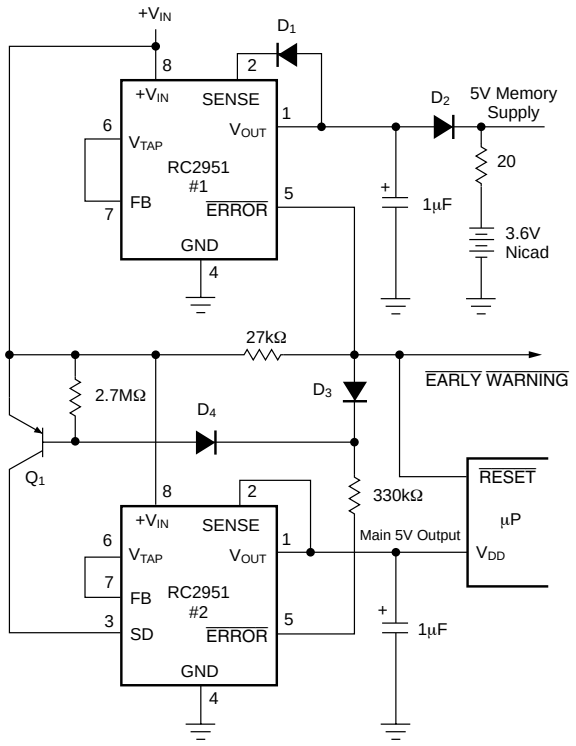
Typical Applications (continued)



- Early warning flag on low input voltage
- Main output latches of f at lower input voltages
- Battery backup on auxillary output

Operation Reg. #1's V_{OUT} is programmed one diode drop above 5V. Its error flag becomes active when $V_{in} \leq 5.7V$. WhenV_{in} drops below 5.3V, the error flag of Reg. #2 becomes active and via Q1 latches the main output off. When V_{in} again exceeds 5.7V Reg. #1 is back in regulation and the early warning signal rises unlatching Reg. #2 via D3.

Figure 7. Regulator with Early Warning and Auxillary Output

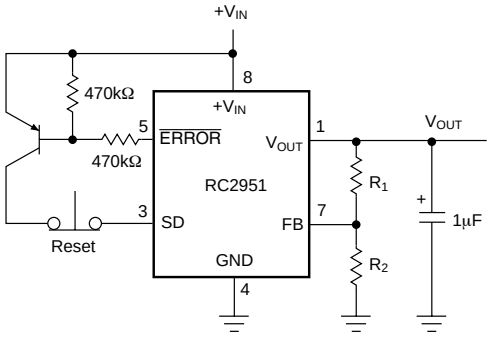
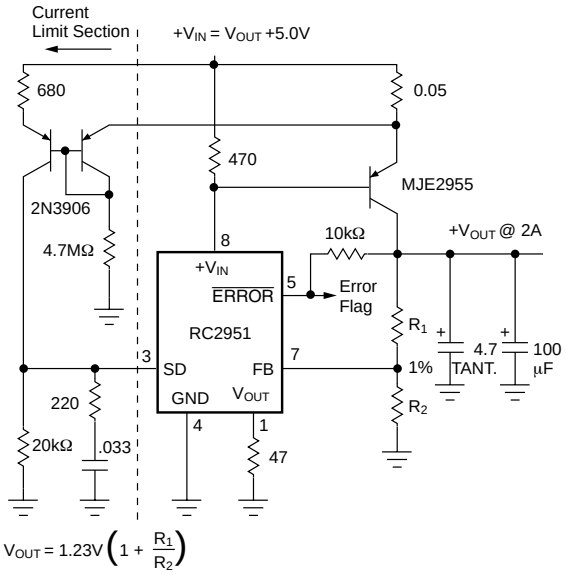


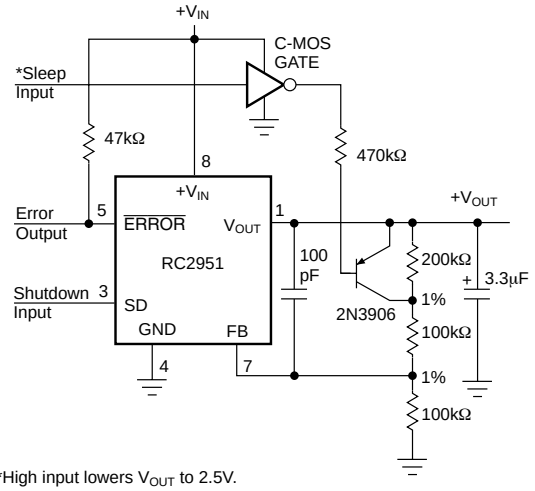
Figure 8. Latch Off When Error Flag Occurs



$$V_{OUT} = 1.23V\left(1 + \frac{R_1}{R_2}\right)$$

For 5V_{OUT},use internal resistors. Wire pin 6 to 7, & wire pin 2 +V_{OUT} Buss.

Figure 9. 2 Ampere Low Dropout Regulator



*High input lowers V_{OUT} to 2.5V.

Figure 10. 5V Regulator with 2.5V Sleep Function

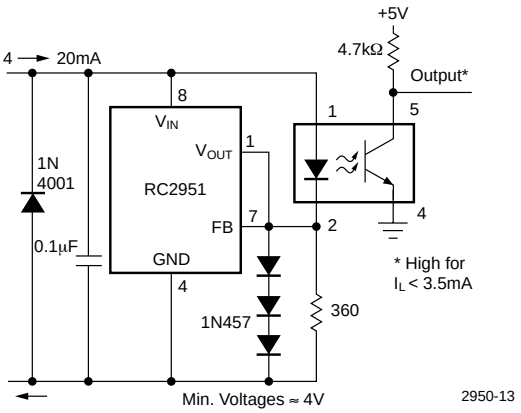
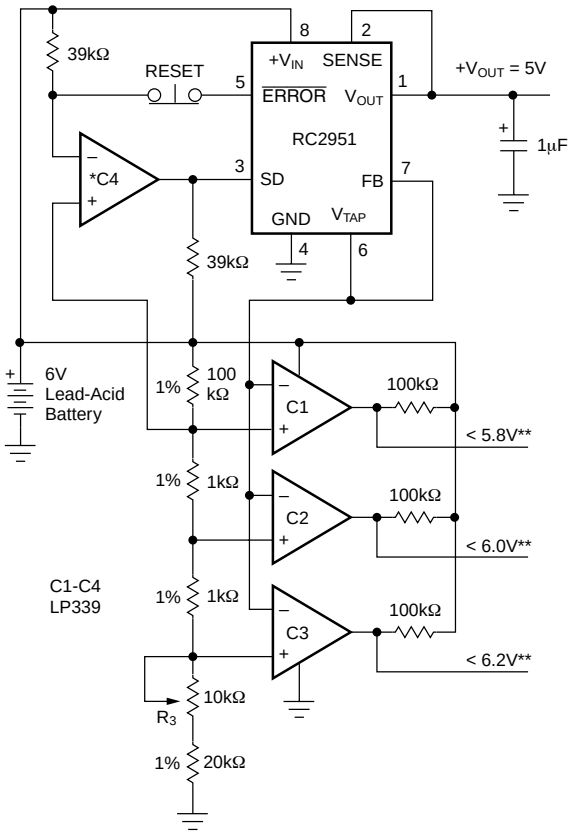


Figure 11. Open Circuit Detector for 4mA to 20mA Current Loop

Typical Applications (continued)

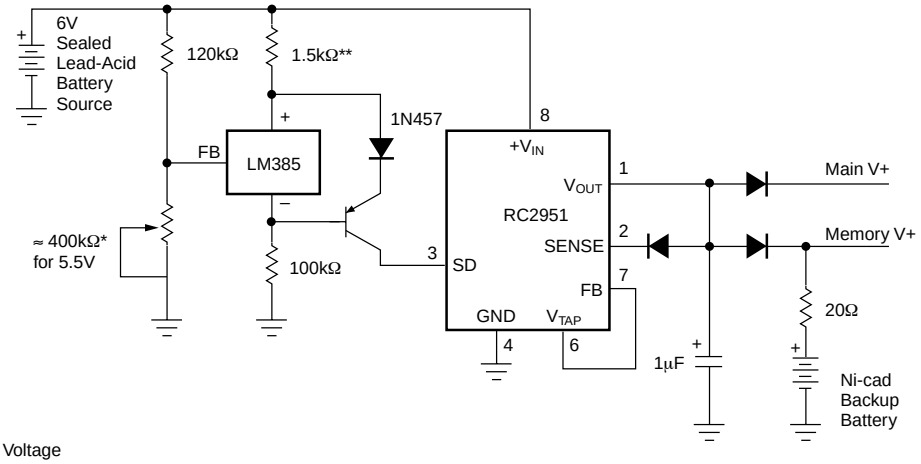


*Optional Latch off when drop out occurs. Adjust R3 for C2 Switching when V_{in} is 6.0V.

**Outputs go low whenV_{in} drops below designated thresholds.

Figure 12. Regulator with State-of-Charge Indicator

For values shown, Regulator shuts down when V_{in} < 5.5V and turns on again at 6.0V. Current drain in disconnected mode is ≈ 150 µA.



*Sets disconnect Voltage

**Sets disconnect Hysteresis

Figure 13. Low Battery Disconnect

Preliminary Information

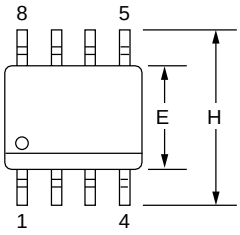
Notes:

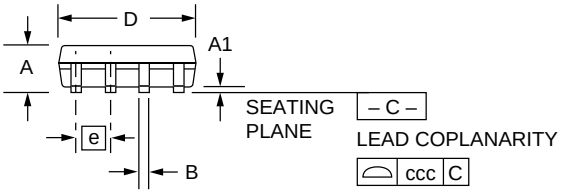
Mechanical Dimensions – 8 Lead SOIC

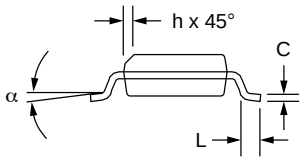
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.20	0.25	5
D	.189	.197	4.80	5.00	2
E	.150	.158	3.81	4.01	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	8		8		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Preliminary Information

Ordering Information

Product Number	Package
RC2951M	8 pin SOIC
RC2951M-3.3	8 pin SOIC

Preliminary Information

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

5/20/98 0.0m 001
Stock#DS30002951

RC3403A

Ground Sensing Quad Operational Amplifier

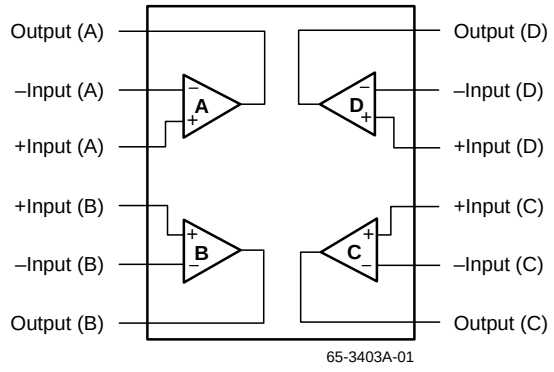
Features

- Class AB output stage – no crossover distortion
- Output voltage swings to ground in single supply operation
- High slew rate – 1.2 V/μS
- Single or split supply operation
- Wide supply operation – +2.5V to +36V or ±1.25V to ±18V
- Pin compatible with LM324 and MC3403
- Low power consumption – 0.8 mA/amplifier
- Common mode range includes ground

Description

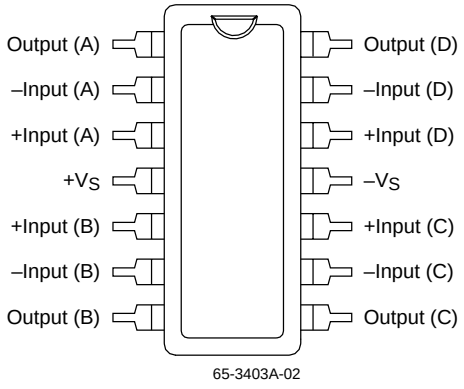
The RC3403A is a high performance ground sensing quad operational amplifier featuring improved dc specifications equal to or better than the standard 741 type general purpose op amp. The ground sensing differential input stage of this op amp provides increased slew rate compared to 741 types.

Block Diagram



65-3403A-01

Pin Assignments



65-3403A-02

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Min	Typ	Max	Units
Supply Voltage			+36 or ±18	V
Input Voltage	-0.3		36	V
Differential Voltage			36	V
$P_D T_A$ < 50°C			468	mW
Operating Temperature	0		70	°C
Storage Temperature	-65		150	°C
Junction Temperature			125	°C
Lead Soldering Temperature (60 seconds)			300	°C
For T_A > 50°C Derate at 6.25mW/°C				

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter		Min	Typ	Max	Units
θ_{JA}	Thermal resistance		160		°C/W

Low Voltage Electrical Characteristics

$+V_S$ = +5V, $-V_S$ = GND, and T_A = +25°C

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage			2.0	10	mV
Input Bias Current			-150	-500	nA
Input Offset Current			30	50	nA
Supply Current	$R_L = \infty$ All Amplifiers		2.5	5.0	mA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$	20	200		V/mV
Output Voltage Swing[1]	$R_L \geq 10k\Omega$	3.5			V_{p-p}
Channel Separation	1kHz ≤ F ≤ 200kHz (Input referred)		120		dB
Power Supply Rejection Ratio		76			dB

Note:

1. Output will swing to ground.

Electrical Characteristics

$+V_S$ = ±15V, 0°C ≤ T_A ≤ +70°C

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage				10	mV
Input Bias Current				-800	nA
Input Offset Current				200	nA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$	15			V/mV
Output Voltage Swing	$R_L \geq 2k\Omega$	±10			V

Electrical Characteristics $+V_S = \pm15V, T_A = +25°C$

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage			2.0	6.0[1]	mV
Input Bias Current			-150	-500	nA
Input Offset Current			30	50	nA
Input Voltage Range		0		$+V_S - 2$	V
Supply Current	$R_L = \infty$ On All Op Amps		3.0	5.0[1]	mA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$	25[1]	100		V/mV
Output Voltage Swing[1]	$R_L \geq 10k\Omega$	±13	±14		V
Common Mode Rejection Ratio	DC	70	90		dB
Channel Separation	±1 kHz to 20kHz		120		dB
Output Source Current	$+V_{IN} = 1V, -V_{IN} = 0V$	20	40		mA
Output Sink Current		10	20		mA
Unity Gain Bandwidth			1.0		MHz
Slew Rate	$A_V = 1, -10 \leq V_{IN} < +10$		1.2[1]		V/μS
Distortion (Crossover)	$F = 20kHz, V_{OUT} = 10V_{p-p}$		1.0		%
Power Bandwidth	$V_{OUT} = 10V_{p-p}$		40		kHz
Power Supply Rejection Ratio		80	94		dB

Note:

1. Significantly improved performance.

Electrical Characteristics Comparison – RC3403A, MC3403, LM324

MAX Ratings	RC3403A			MC3403			LM324			Unit
Supply Voltage	+36 or ±18			+36 or ±18			+32 or ±16			V
Differential Input Voltage	36			36			32			V
Input Voltage	36			36			32			V
Electrical Characteristics	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Test Conditions		±15			±15			+5.0		V
Input Offset Voltage		2.0	6.0		2.0	8.0		2.0	7.0	mV
Input Offset Current		±30	±50		±30	±50		±5.0	±50	nA
Input Bias Current		150	500		200	500		45	500	nA
Input Voltage Range	0		$+V_S - 2$	0		$+V_S - 2$	0		$+V_S - 1.5$	V
Supply Current		3.0	5.0		2.8	7.0		0.8	2.0	mA
Large Signal Voltage Gain	25	100		20	200			100		V/mV
Output Voltage Swing	±13	±14		±10	±13		0		$+V_S - 1.5$	V
Common Mode Rejection Ratio	70	90		70	90			85		dB
Power Supply Rejection Ratio	80	94		76	90			85		dB
Unity Gain Bandwidth		1.0			1.0			1.0		MHz
Slew Rate		1.2			0.6			0.4		V/μS
Output Sink Current	10	20						20		mA
Output Source Current	20	40					20	40		mA
Channel Separation		120			120			120		dB
Distortion (Crossover)		1.0			1.0					%

Typical Performance Characteristics

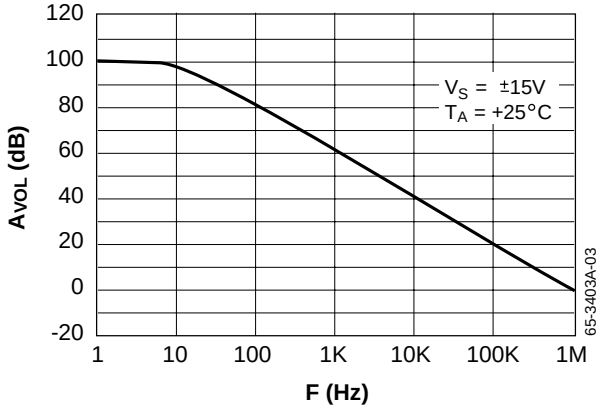


Figure 1. Open Loop Gain vs. Frequency

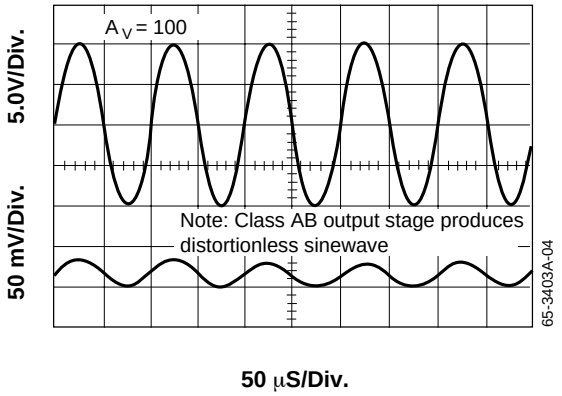


Figure 2. Sinewave Response

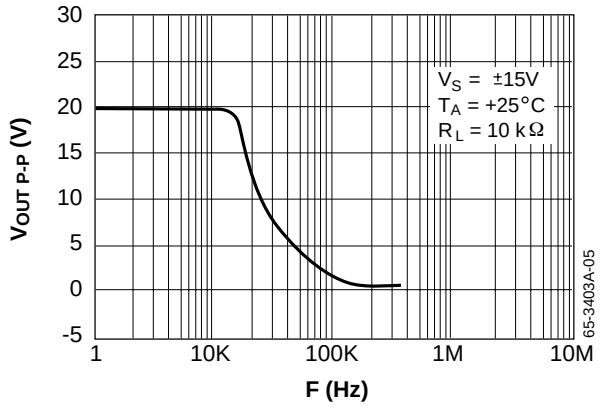


Figure 3. Output Voltage vs. Frequency

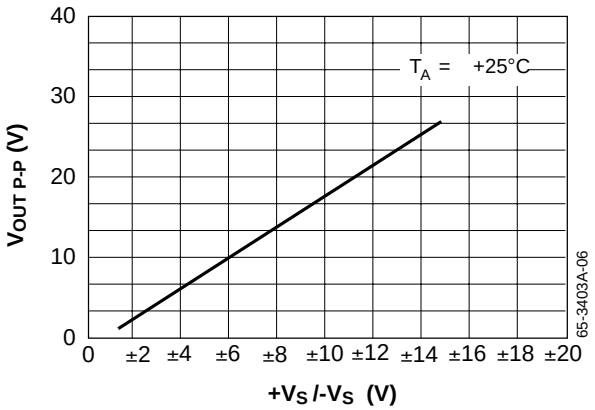


Figure 4. Output Swing vs Supply Voltage

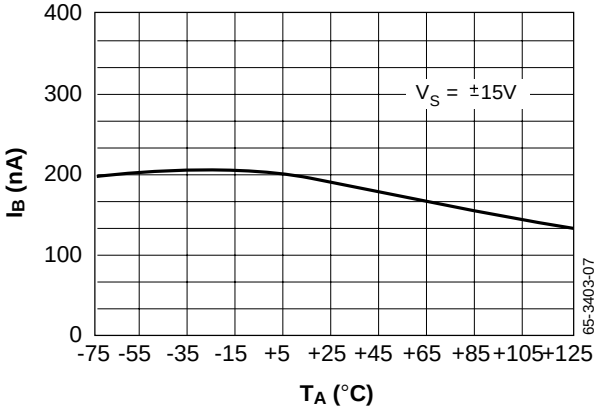


Figure 5. Input Bias Current vs. Temperature

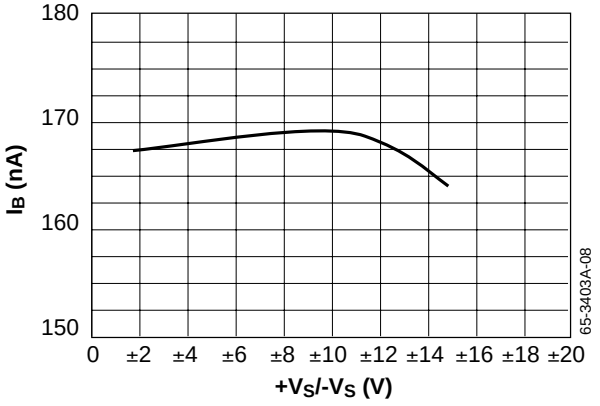


Figure 6. Input Bias Current vs. Supply Voltage

Typical Applications

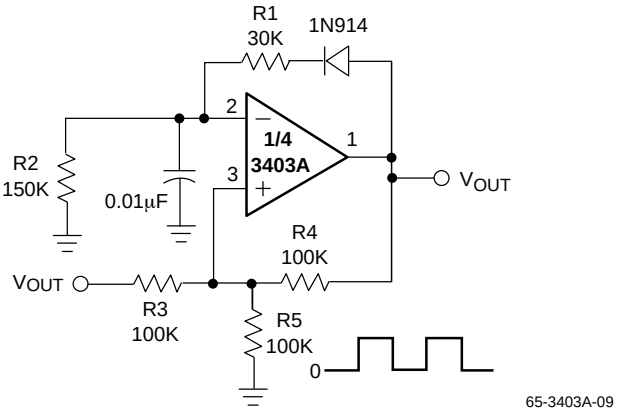


Figure 7. Pulse Generator

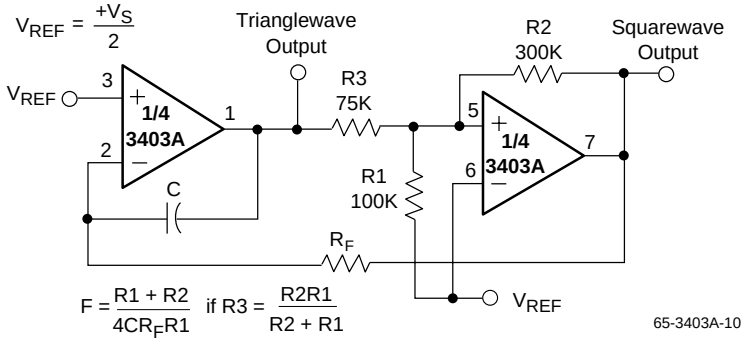


Figure 8. Function Generator

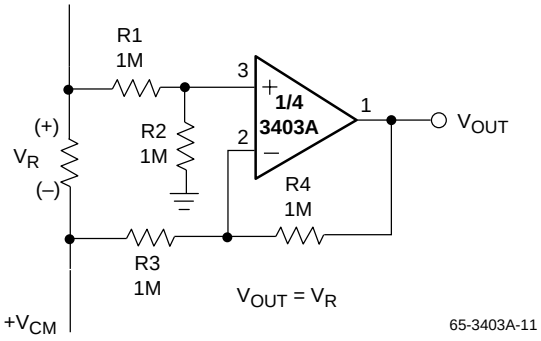


Figure 9. Ground Referencing a Differential Input Signal

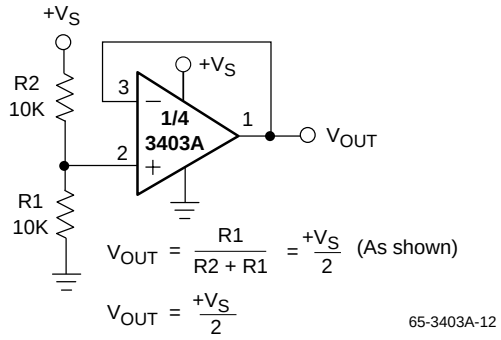


Figure 10. Voltage Reference

Typical Applications (continued)

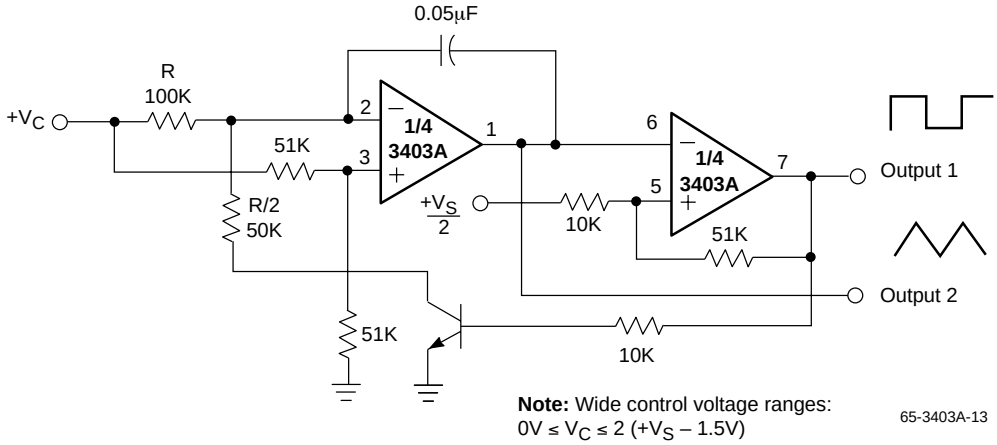


Figure 11. Voltage Controlled Oscillator

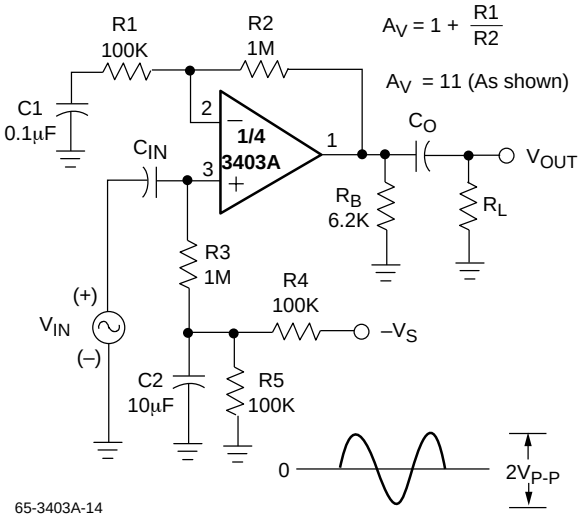


Figure 12. AC Coupled Non-Inverting Amplifier

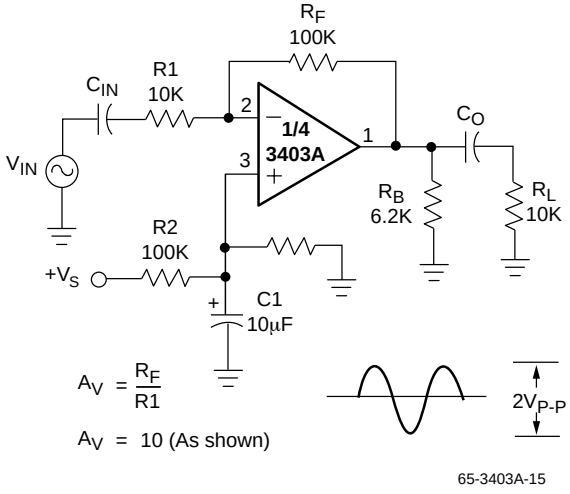
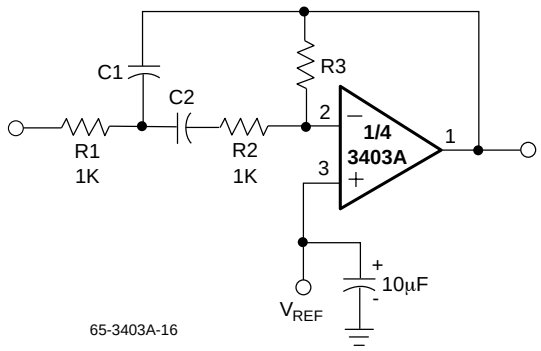


Figure 13. AC Coupled Inverting Amplifier



F_O Δ Center Frequency
BW Δ Bandwidth
R in kΩ
C in μF

$Q = \frac{F_O}{BW} < 10$

$C1 = C2 = \frac{Q}{3}$

$R1 = R2 = 1$
$R3 = 9Q^2 - 1$ } Use scaling factors in these expressions.

If source impedance is high or varies, filter may be preceeded with voltage follower buffer to stabilize filter parameters.

Design Example:

Given: Q = 5, F_O = 1 kHz
Let R1 = R2 = 10 k Ω
Then R3 = 9 $(5)^2$ - 10
R3 = 215 k Ω

$C = \frac{5}{3} = 1.6$ nF

Figure 14. Multiple Feedback Bandpass FIlter

Typical Applications (continued)

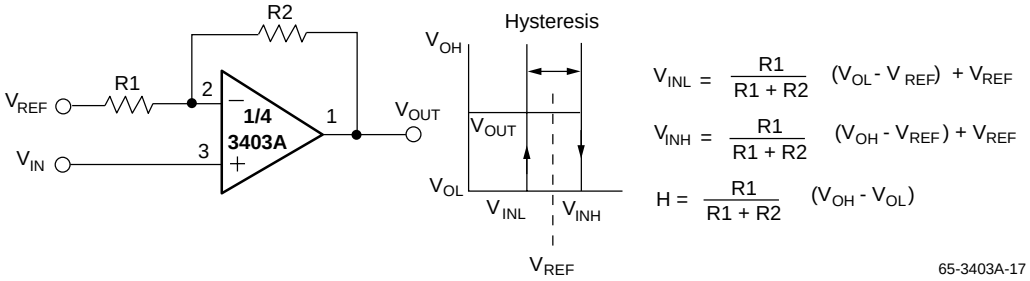


Figure 15. Comparator with Hysteresis

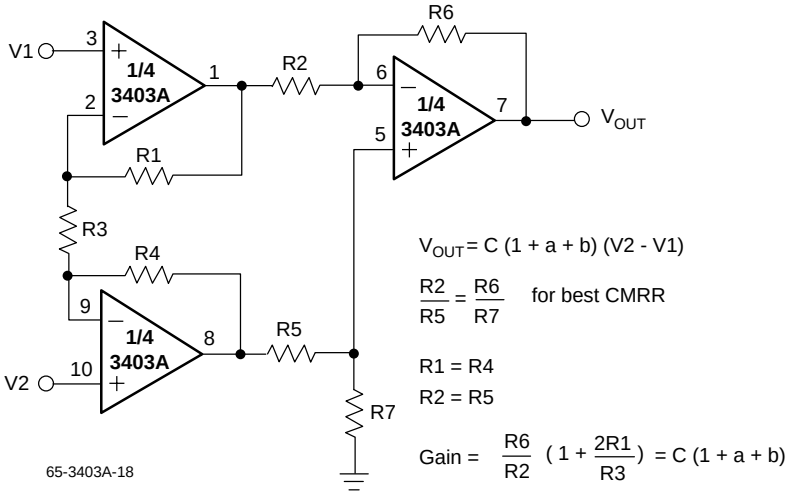


Figure 16. High Impedance Differential Amplifier

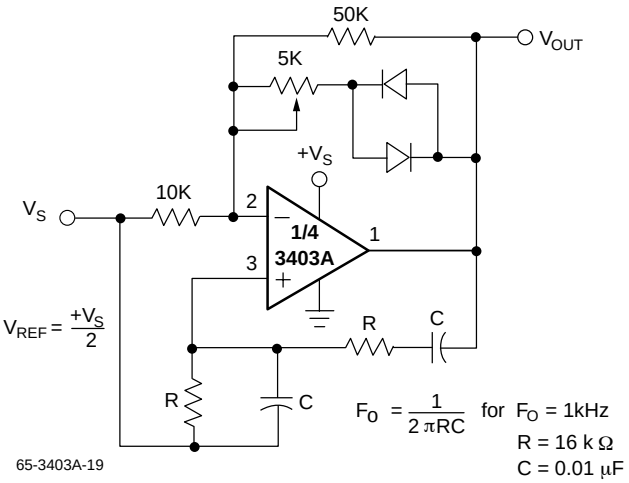
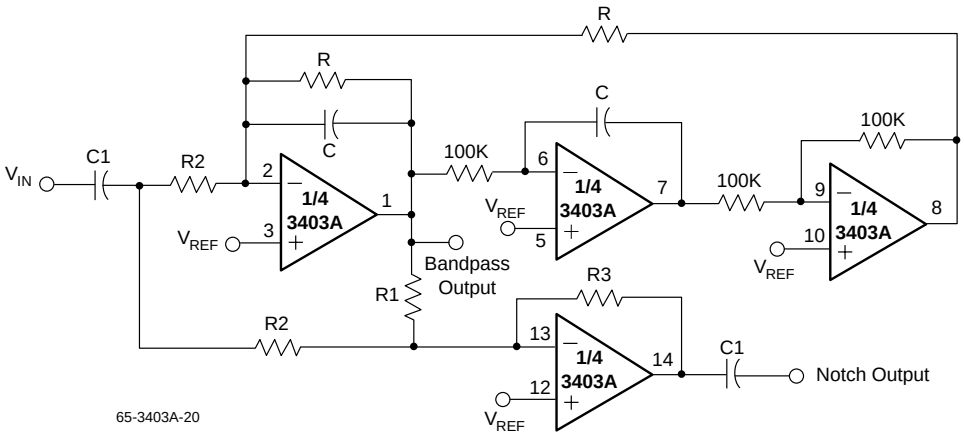


Figure 17. Wein Bridge Oscillator

Typical Applications (continued)



$$Q = \frac{F_O}{BW}$$

Where:

T_{BP} = Center Frequency Gain

T_N = Bandpass Notch Gain

$$F_O = \frac{1}{2\pi RC}$$

$R1 = QR$

$$R2 = \frac{R1}{T_{BP}}$$

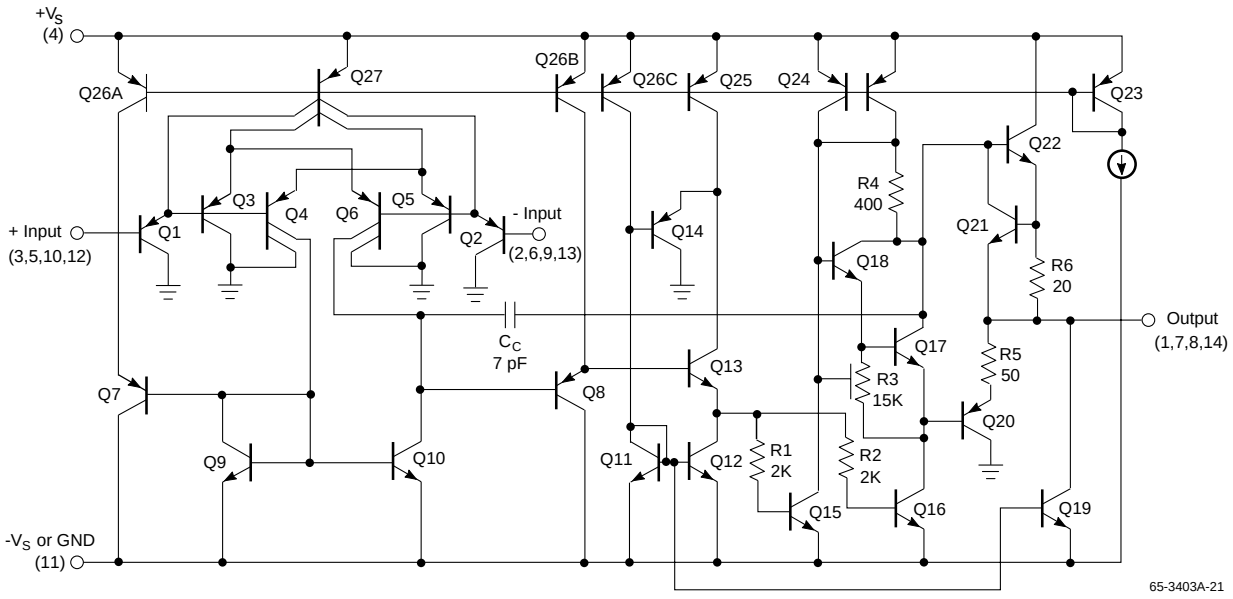
$R3 = T_N R2$

$C1 = 10C$

Example:
F_O = 1000 Hz
BW = 100 Hz
T_{BP} = 1
T_N = 1
R = 160 kΩ
R1 = 1.6 MΩ
R2 = 1.6 MΩ
R3 = 1.6 MΩ
C = 0.001μF

Figure 18. Bi-Quad Filter

Simplified Schematic Diagram (1/4 Shown)

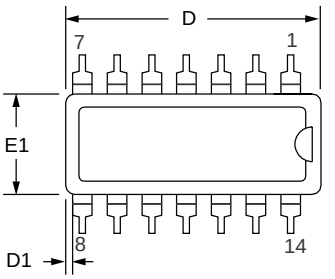


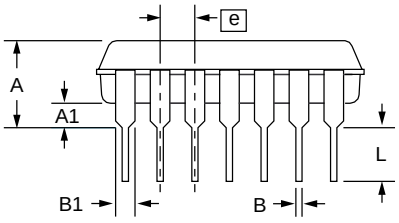
Mechanical Dimensions – 14-Lead Plastic DIP Package

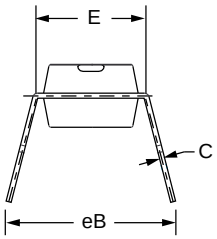
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	.725	.795	18.42	20.19	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.200	2.92	5.08	
N	14		14		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are shown for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.







Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
RC3403AN	0° to 70°C	Commercial	14 Pin Plastic DIP	RC3403AN

RC40-XX

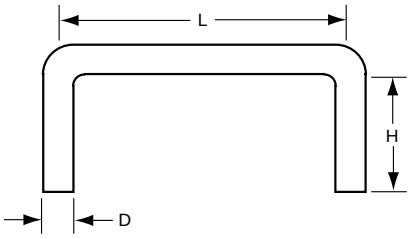
Sense Resistors for Fairchild Semiconductor DC-DC Controllers

Features

- Resistor typical tolerance ± 5%
- Resistance wire TCR +20ppm/C
- Wire alloy MnCu (mangnin)

Resistor Dimensions

Type	R (mΩ)	D (mm)	L (mm)	H (mm)
RC40-58	5.8	1.00	9.3	5.0
RC40-44	4.4	1.00	7.1	5.0



Applications

Controller Type	I_{Lmax} (A)	R_{sense} Type
RC5036	10	RC40-58
RC5036	14	RC40-36
RC5041/RC5042	13	RC40-58
RC5041/RC5042	18	RC40-36
RC5050/RC5051	13	RC40-58
RC5050/RC5051	18	RC40-36

System Requirements

The design of the sense resistor is driven by the following system requirements:

1. Load current, (I_{LOAD}). This is the full load DC current the converter is designed to support.

2. The controller short circuit current detect threshold voltage (V_{TH}), which for Fairchild Semiconductor family of Controllers is specified at 120+/-20mV for RC5040/41/42/50/51 or 90 ±10mV for RC5036.

3. The inductor current ripple (I_R). A reasonable design guideline is to assume the current ripple is limited to 1.5A.

Design Equations

The design of the sense resistor must consider carefully the output requirements during normal operation and during a fault condition. If the sense resistor is too high, it may develop enough voltage drop accross it to trip the short circuit detect circuitry so that the DC-DC converter may not be able to deliver the maximum required load current. If the sense resistor is too low, the controller may not be disabled when a certain safe amount of load current is exceeded, thus the power dissipation within the MOSFET(s) may rise to destructive levels.

The design equations used to calculate the sense resistor are as follows:

$$I_{SC(MIN)} = (I_{LOAD} + I_R + 1)$$

$$R_{SENSE(MAX)} = \frac{V_{TH(MIN)}}{I_{SC(MIN)}}$$

and, assuming a 10% tolerance, the nominal design value of the sense resistor is given by:

$$R_{SENSE} = \frac{R_{SENSE(MAX)}}{(1 + 0.10)}$$

Wire Sense Resistors

There are several types of sense resitors available to the system designer in a wide range of cost and specifications.

The resistors with higher precision (i.e. 1% SMT) demand the highest cost (i.e. $0.47); however a 10% to 15% tolerance is adequate for most DC-DC converters designs and wire resistors offer a very cost effective alternative.

Mangnin or Copel wire resistors, made respectively of MnCu and CuNi alloys, have been used extensively in the manufacture of sense resistors used in the Fairchild Semiconductor's family of DC-DC converters.

These resistive wires are available in all the most common gages and Table 1 and 2 describe the specifications of Mangnin and Copel for various diameter wire size.

Wire with diameter of ~1 mm is best suited to make sense resistors for DC-DC converters used in motherboard applications. Refer to Figure 1 for the typical shape of a wire sense resistor and Graph 1 through 4 for the dimensions of the resistor as function of the load current requirements of the converter.

Advanced Information

Table 1. Mangnin Wire Resistor Specifications

Diameter (mm)	Ω/m	mΩ/mm	Imax (Amp)
1.40	0.31831	0.318	154
1.30	0.36916	0.369	133
1.10	0.51561	0.516	95
1.00	**0.62389**	**0.624**	**79**
0.90	0.77023	0.770	64
0.80	0.97482	0.975	50

Note:
1. $J = 10^4$ A/cm^2

Table 2. Copel Wire Resistor Specifications

AWG	Diameter (mm)	Ω/ft	mΩ/m	Imax (Amp)
15	1.45	0.09049	0.30	165
16	1.29	0.11300	0.37	131
17	1.15	0.14520	0.48	104
18	**1.02**	**0.18370**	**0.60**	**82**
19	0.912	0.22690	0.74	65
20	0.812	0.28710	0.94	52

Note:
1. $J = 10^4$ A/cm^2

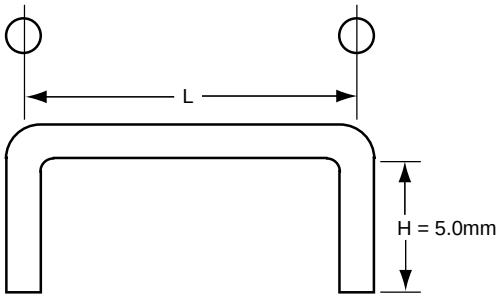
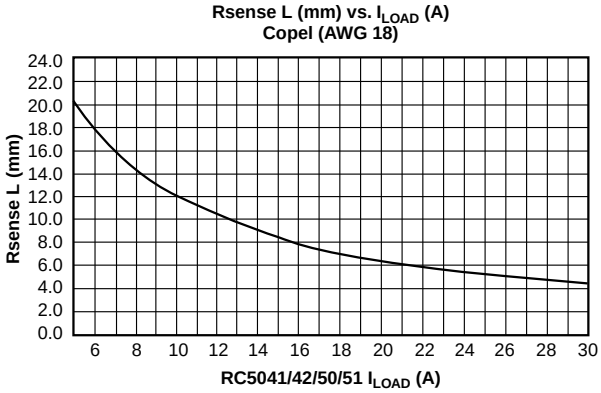
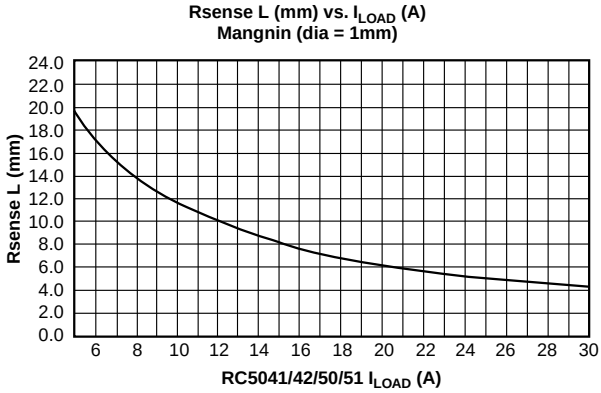


Figure 1. Manganin or Copel Wire Resistor

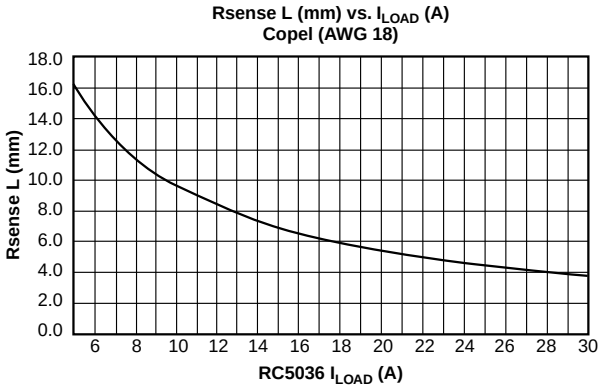
Advanced Information



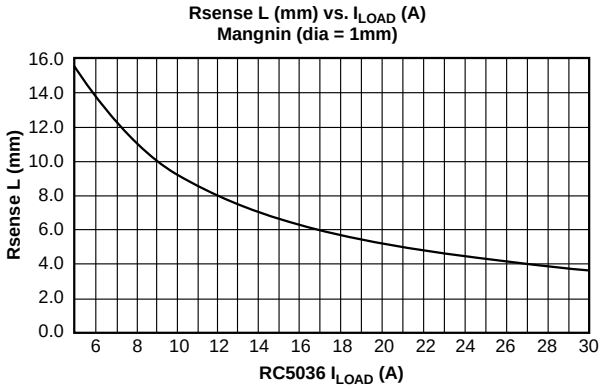
Graph 1. Rsense vs. Imax (Copel)



Graph 2. Rsense vs. Imax (Magnin)



Graph 3. Rsense vs. Imax (Copel)



Graph 4. Rsense vs. Imax (Magnin)

Advanced Information

Advanced Information

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Fax:81-3-5620-6179

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RC4136

General Performance Quad 741 Operational Amplifier

Features

- Unity gain bandwidth – 3 MHz
- Short circuit protection
- No frequency compensation required
- No latch-up
- Large common mode and differential voltage ranges
- Low power consumption
- Parameter tracking over temperature range
- Gain and phase match between amplifiers

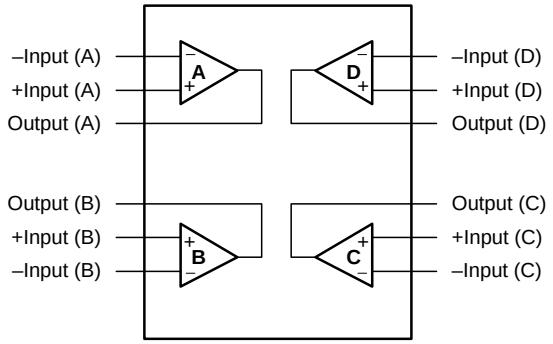
Description

The RC4136 is made up of four 741 type independent high gain operational amplifiers internally compensated and constructed on a single silicon chip using the planar epitaxial process.

This amplifier meets or exceeds all specifications for 741 type amplifiers. Excellent channel separation allows the use of the RC4136 quad amplifier in all 741 operational amplifier applications providing the highest possible packaging density.

The specially designed low noise input transistors allow the RC4136 to be used in low noise signal processing applications such as audio preamplifiers and signal conditioners.

Block Diagram



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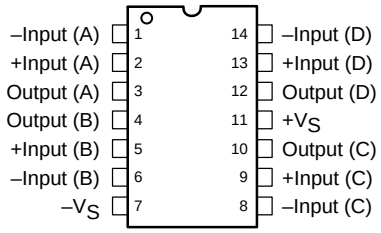
Pin Assignments



65-4136-02

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min	Typ	Max	Units
Supply Voltage	RC4136			±18	V
	RM4136			±22	V
Input Voltage[2]				±30	V
Differential Input Voltage				30	V
Output Short Circuit Duration[3]		Indefinite			
$P_D T_A$ < 50°C	SOIC			300	mW
	PDIP			468	mW
	CerDIP			1042	mW
Operating Temperature	RC4136	0		70	°C
	RM4136	-55		125	°C
Storage Temperature		-65		150	°C
Junction Temperature	SOIC, PDIP			125	°C
	CerDIP			175	°C
Lead Soldering Temperature (60 seconds)	DIP			300	°C
	SOIC			260	°C

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground, typically 45 mA.

Operating Conditions

Parameter			Min	Typ	Max	Units
θ_{JC}	Thermal resistance			60		°C/W
θ_{JA}	Thermal resistance	SOIC		200		°C/W
		PDIP		160		°C/W
		CerDIP		120		°C/W
For T_A > 50°C Derate at		SOIC		5.0		mW/°C

Electrical Characteristics

(V_S = ±15V and T_A = +25˚C, unless otherwise noted)

Parameters	Test Conditions	RM4136			RC4136			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \le 10k\Omega$		0.5	5.0		0.5	6.0	mV
Input Offset Current			5.0	200		5.0	200	nA
Input Bias Current			40	500		40	500	nA
Input Resistance		0.3	5.0		0.3	5.0		MΩ
Large Signal Voltage Gain	$R_L \ge 2k\Omega$, V_{OUT} = ±10V	50	300		20	300		V/mV
Output Voltage Swing	$R_L \ge 10k\Omega$	±12	±14		±12	±14		V
	$R_L \ge 2k\Omega$	±10	±13		±10	±13		
Input Voltage Range		±12	±14		±12	±14		V
Common Mode Rejection Ratio	$R_S \le 10k\Omega$	70	100		70	100		dB
Power Supply Rejection Ratio	$R_S \le 10k\Omega$	76	100		76	100		dB
Power Consumption	$R_L = \infty$, All Outputs		210	340		210	340	mW
Transient Response								
Rise Time	V_{IN} = 20mV, R_L = 2kΩ		0.13			0.13		μS
Overshoot	$C_L \le 100pF$		5.0			5.0		%
Unity Gain Bandwidth			3.0			3.0		MHz
Slew Rate	$R_L \ge 2k\Omega$		1.5			1.0		V/μS
Channel Separation	F = 1.0kHz, R_S =1kΩ		90			90		dB

Electrical Characteristics

(RM = -55°C ≤ T_A ≤ = 125°, RC = 0°C ≤ T_A ≤ = 70°, V_S = ± 15V)

Parameters	Test Conditions	RM4136			RC4136			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \le 10k\Omega$			6.0			7.5	mV
Input Offset Current				500			300	nA
Input Bias Current				1500			800	nA
Large Signal Voltage Gain	$R_L \ge 2k\Omega$, V_{OUT} = ±10V	25			15			V/mV
Output Voltage Swing	$R_L \ge 2k\Omega$	±10			±10			V
Power Consumption			240	400		240	400	mW

Electrical Characteristics Comparison

(V_S = ±15V and T_A +25°C unless otherwise noted)

Parameter	RC4136 (Typ.)	RC741 (Typ.)	LM324 (Typ.)	Units
Input Offset Voltage	0.5	2.0	2.0	mV
Input Offset Current	5.0	10	5.0	nA
Input Bias Current	40	80	55	nA
Input Resistance	5.0	2.0		MΩ
Large Signal Voltage Gain (R_L = 2kΩ)	300	200	100	V/mV
Output Voltage Swing (R_L= 2kΩ)	±13V	±13V	|+V_S – 1.2V| to –V_S	V
Input Voltage Range	±14V	±13V	|+V_S – 1.5V| to –V_S	V
Common Mode Rejection Ratio	100	90	85	dB
Power Supply Rejection Ratio	100	90	100	dB
Transient Response				
Rise Time	0.13	0.3		μS
Overshoot	5.0	5.0		%
Unity Gain Bandwidth	3.0	0.8	0.8	MHz
Slew Rate	1.0	0.5	0.5	V/μS
Input Noise Voltage Density (F= 1kHz)	10	22.5		nV/√Hz
Short Circuit Current	±45	±25		mA

Typical Performance Characteristics

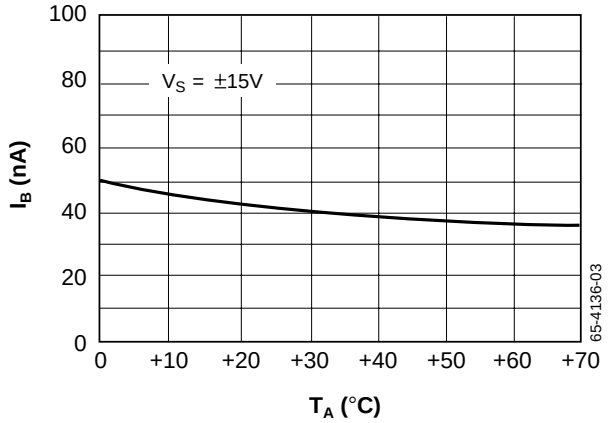


Figure 1. Input Bias Current vs. Temperature

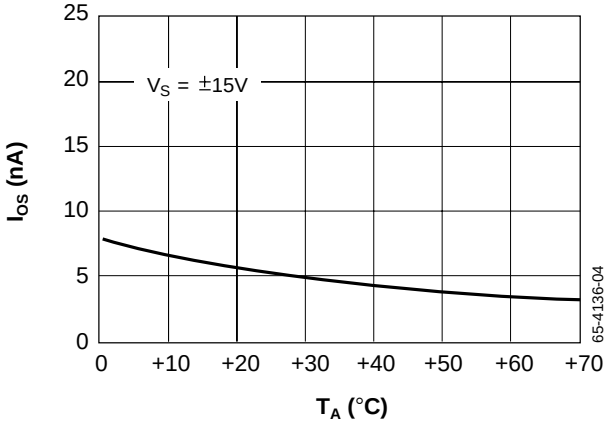


Figure 2. Input Offset Current vs. Temperature

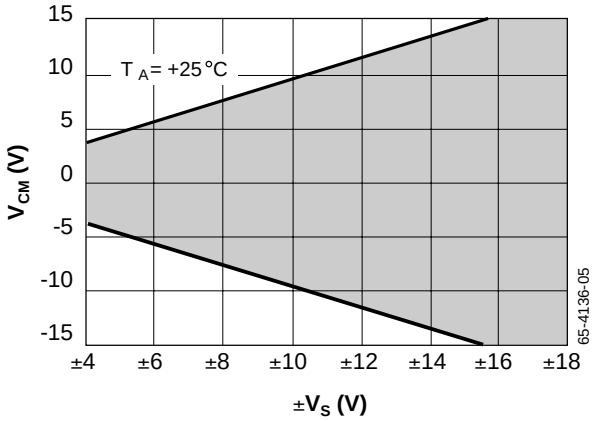


Figure 3. Input Common Mode Voltage Range vs. Supply Voltage

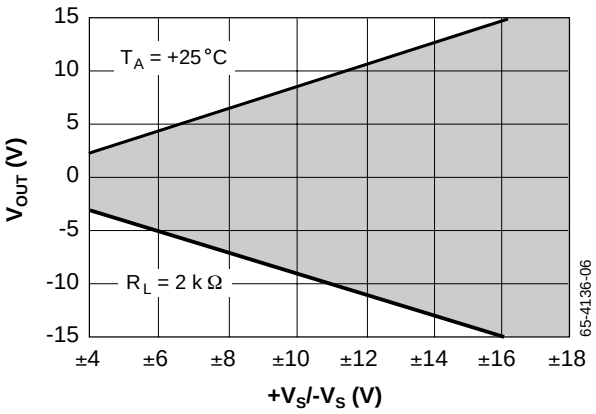


Figure 4. Output Voltage vs. Supply Voltage

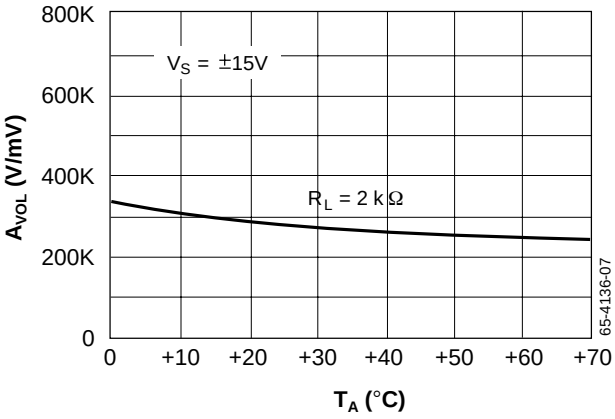


Figure 5. Open Loop Gain vs. Temperature

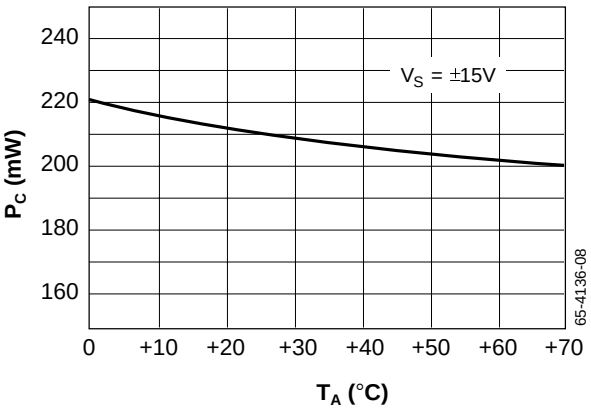


Figure 6. Power Consumption vs. Temperature

Typical Performance Characteristics (continued)

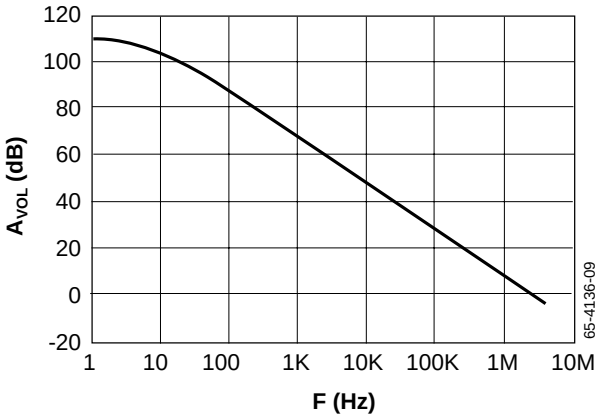


Figure 7. Open Loop Gain vs. Frequency

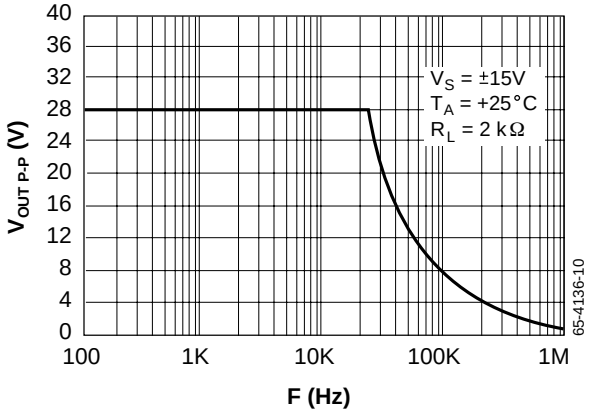


Figure 8. Output Voltage Swing vs. Frequency

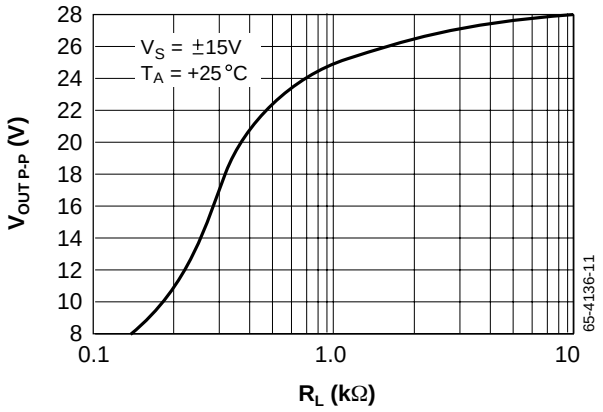


Figure 9. Output Voltage Swing vs. Load Resistance

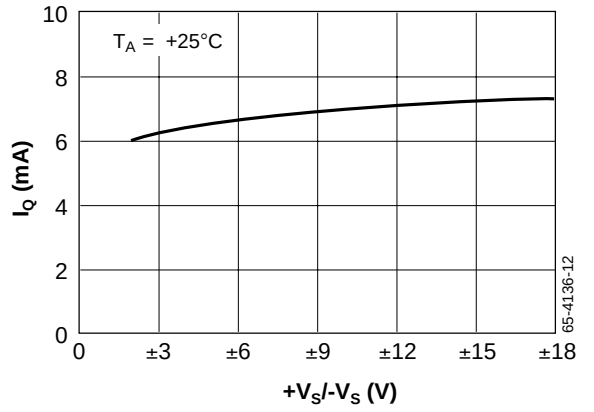


Figure 10. Quiescent Current vs. Supply Voltage

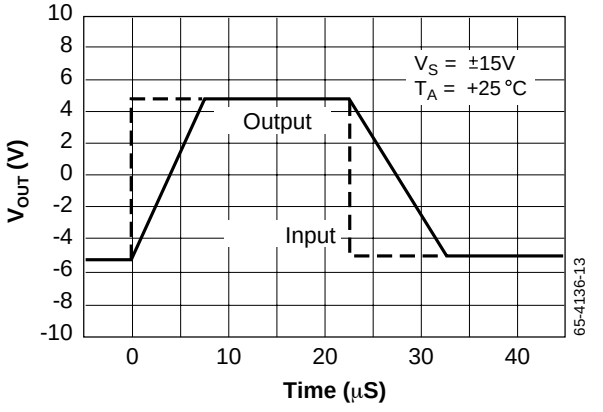


Figure 11. Follower Large Signal Pulse Response

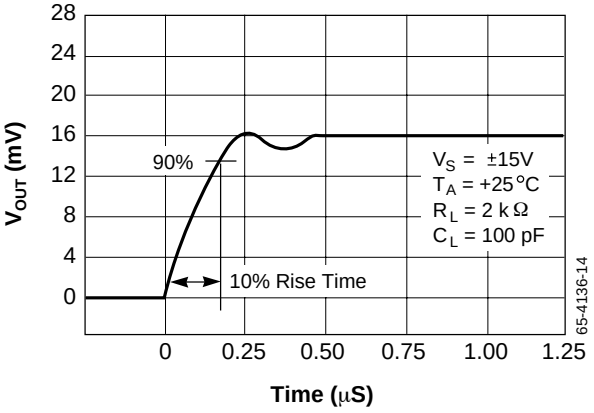


Figure 12. Transient Response Output Voltage vs. Time

Typical Performance Characteristics (continued)

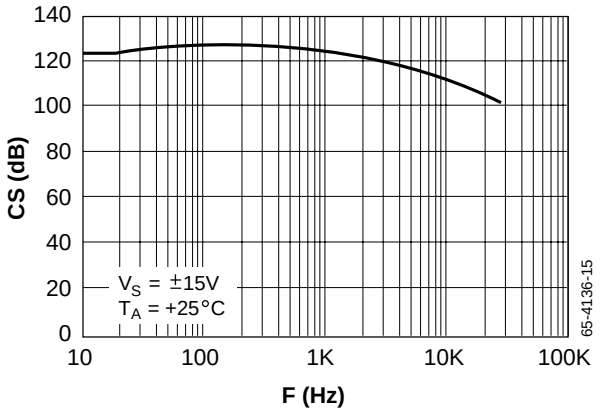


Figure 13. Channel Separation vs. Frequency

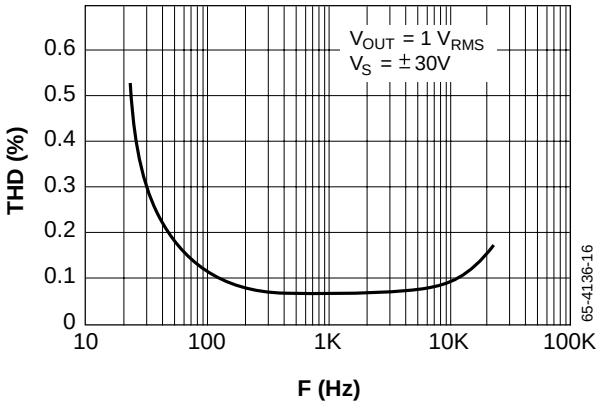


Figure 14. Total Harmonic Distortion vs. Frequency

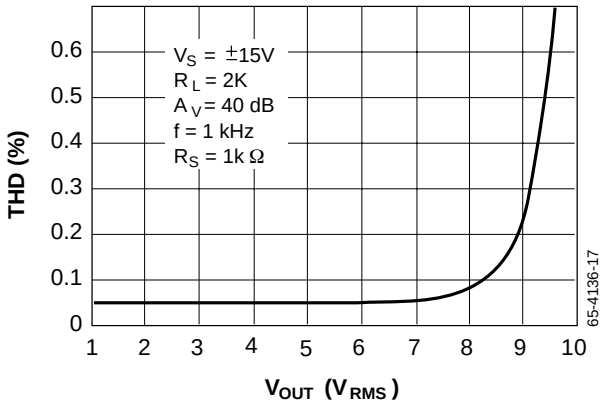


Figure 15. Total Harmonic Distortion vs. Output Voltage

RC4136 Versus LM324

Although the LM324 is an excellent device for single-supply applications where ground sensing is important, it is a poor substitute for four 741s in split supply circuits. The simplified input circuit of the RC4136 exhibits much lower noise than that of the LM324 and exhibits no crossover distortion as compared with the LM324 (see Figure 16). The LM324 shows significant crossover distortion and pulse delay in attempting to handle a large signal input pulse.

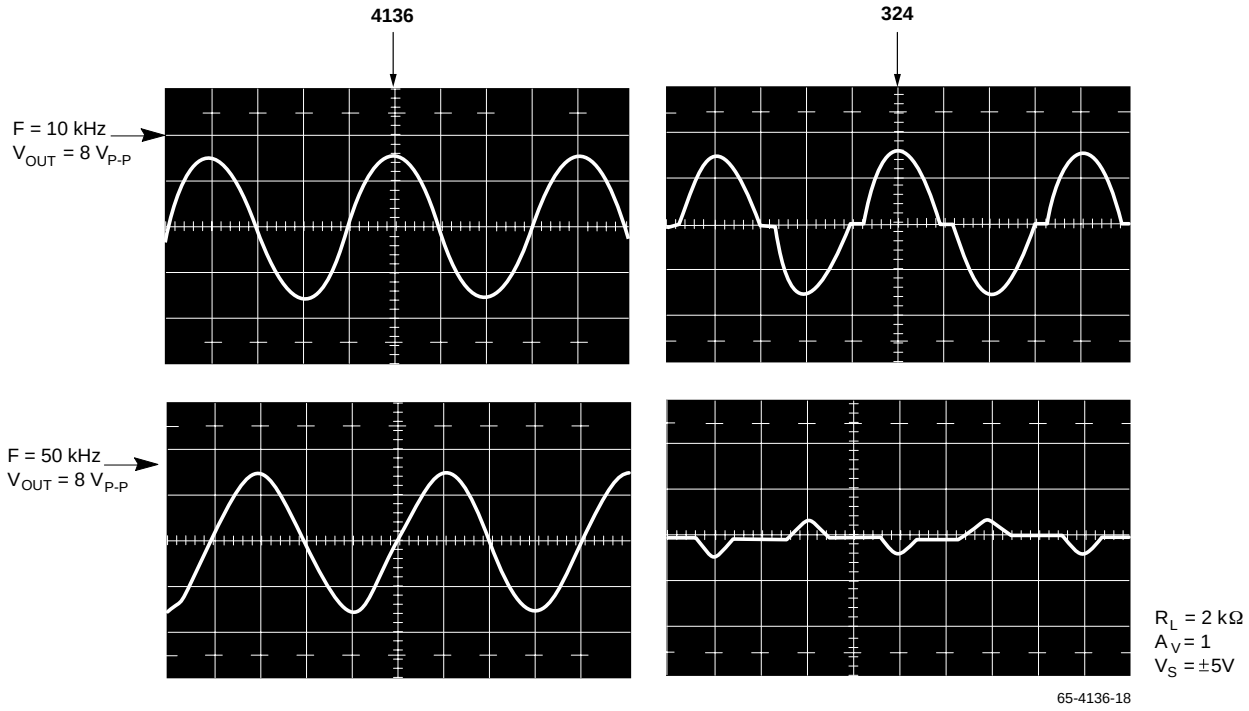


Figure 16. Comparative Crossover Distortion

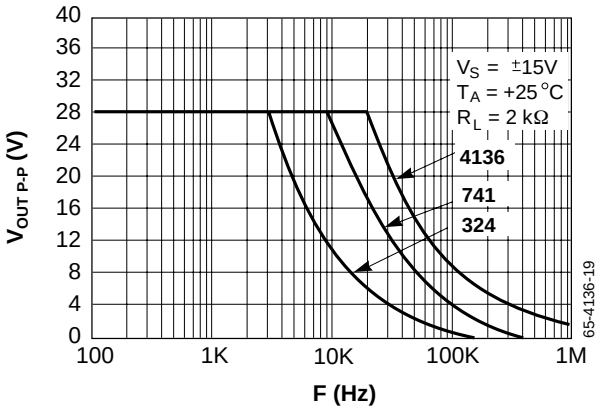


Figure 17. Output Voltage Swing vs. Frequency

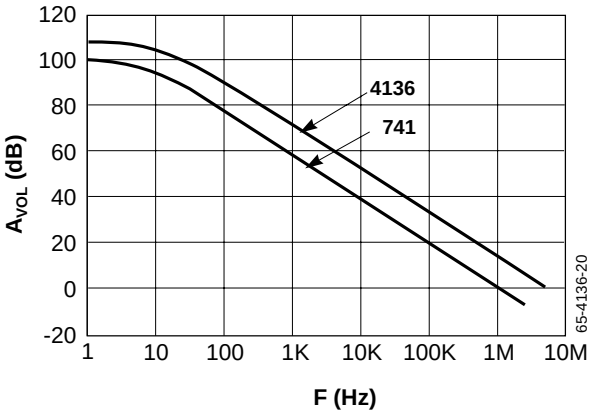


Figure 18. Open Loop Gain vs. Frequency

RC4136 Versus LM324 (continued)

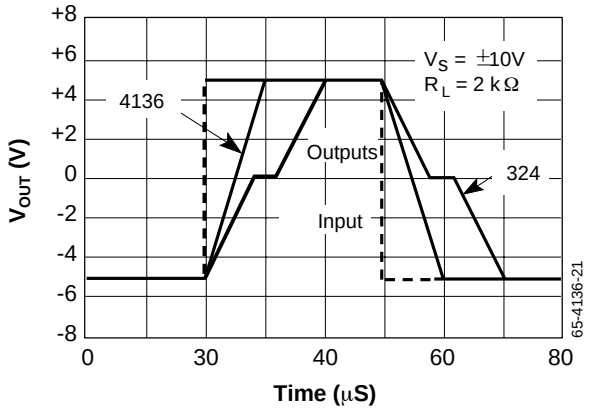


Figure 19. Follower Large Signal Pulse Response Output Voltage vs. Time

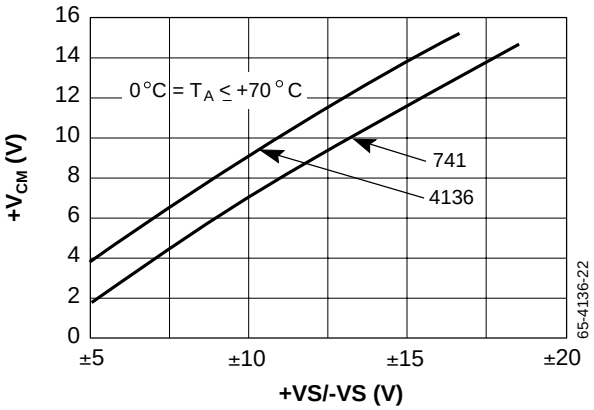


Figure 20. Input Common Mode Voltage Range vs. Supply Voltage

Typical Applications

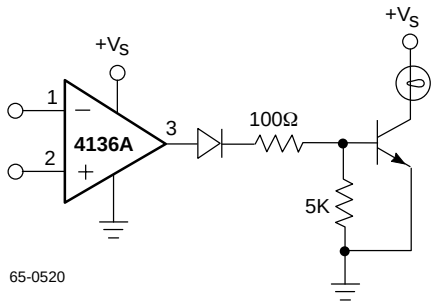


Figure 21. Lamp Driver

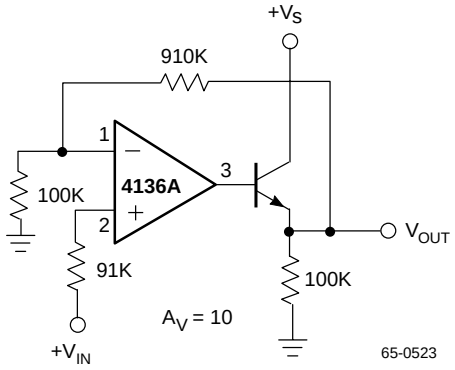


Figure 22. Power Amplifier

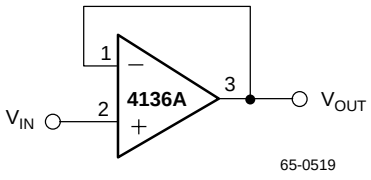


Figure 23. Voltage Follower

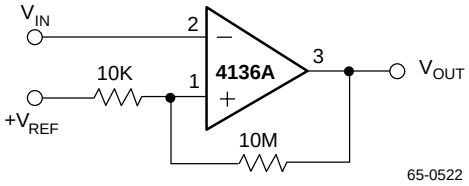


Figure 24. Comparator with Hysteresis

Typical Applications (continued)

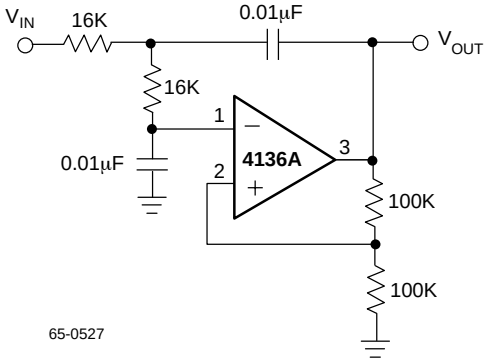


Figure 25. DC Coupled 1kHz Lowpass Active Filter

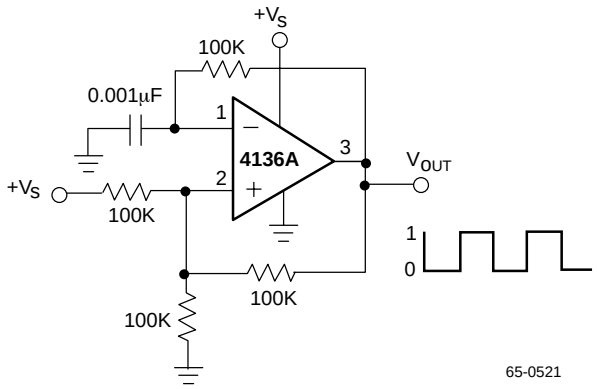


Figure 26. Squarewave Oscillator

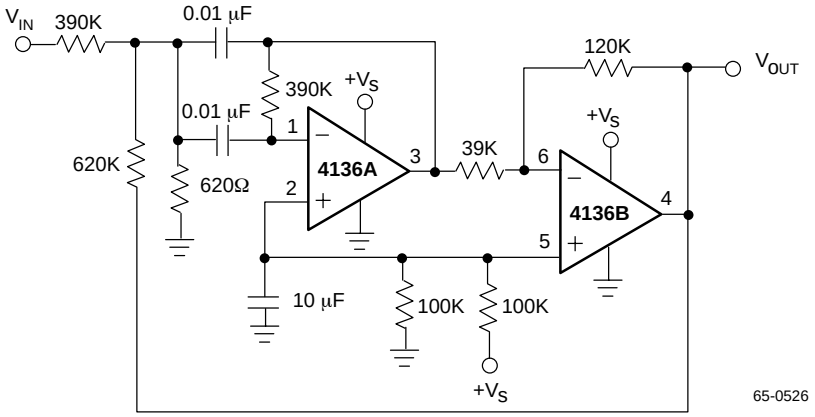


Figure 27. 1kHz Bandpass Active Filter

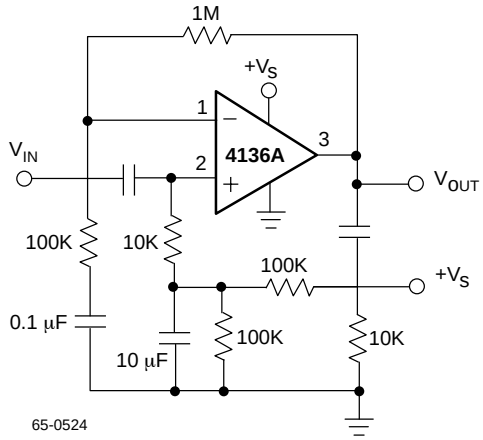


Figure 28. AC Coupled Non-Inverting Amplifier

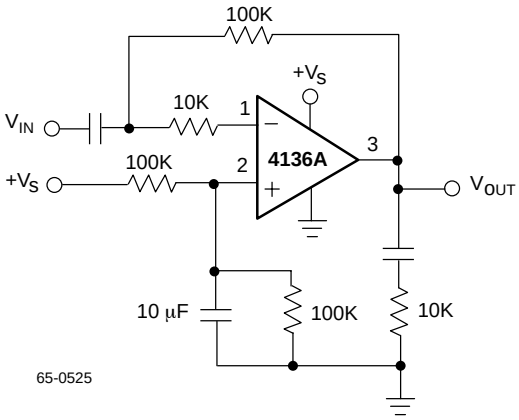
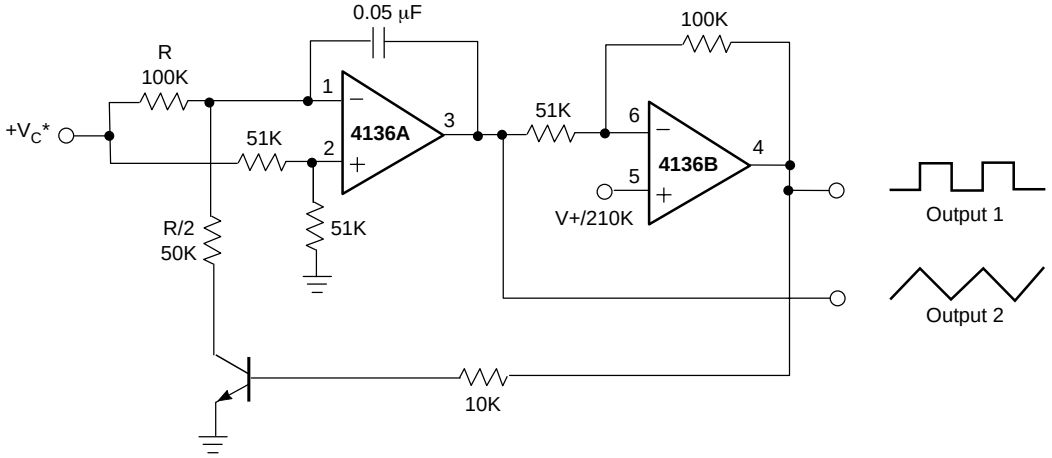


Figure 29. AC Coupled Inverting Amplifier

Typical Applications (continued)



* Wide control voltage range: $0V < V_C < 2(+V_S - 1.5V)$

Figure 30. Voltage Control Oscillator (VCO)

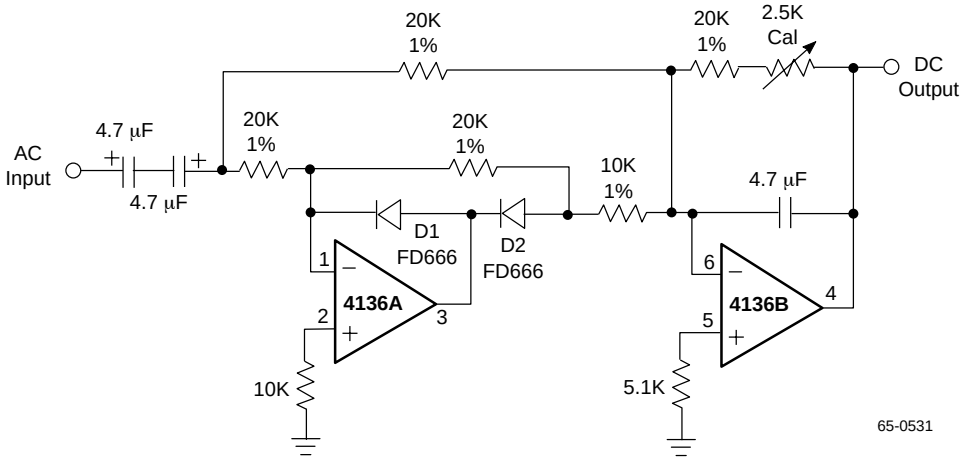


Figure 31. Full-Wave Rectifier and Averaging Filter

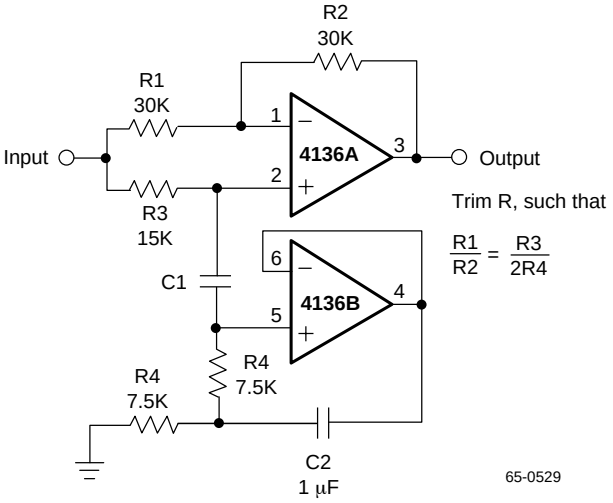


Figure 32. Notch Filter Using the RC4136 as a Gyrator

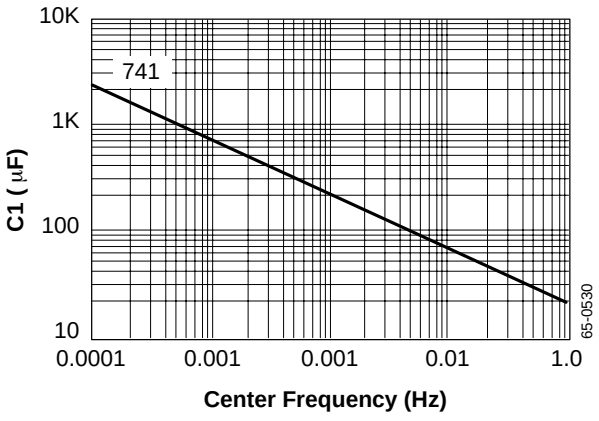


Figure 33. Notch Frequency vs. C1

Typical Applications (continued)

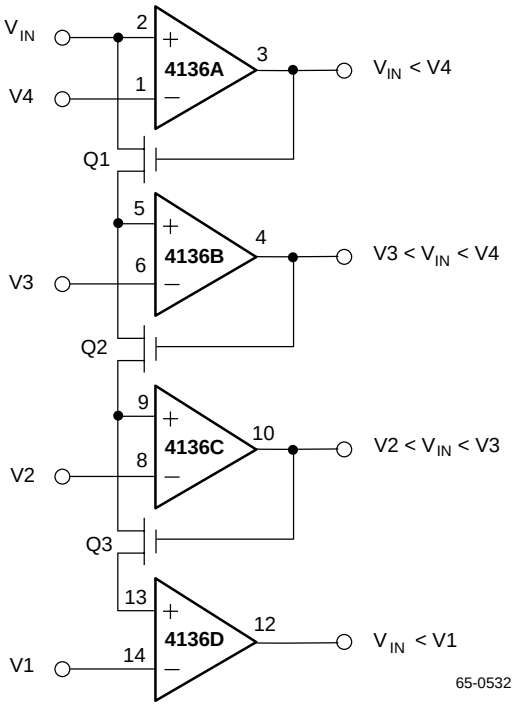


Figure 34. Multiple Aperture Window Discriminator

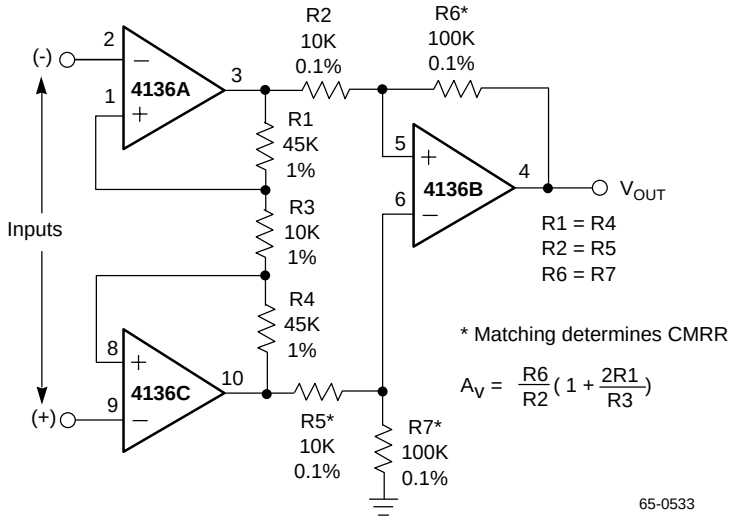


Figure 35. Differential Input Instrumentation Amplifier with High Common Mode Rejection

Typical Applications (continued)

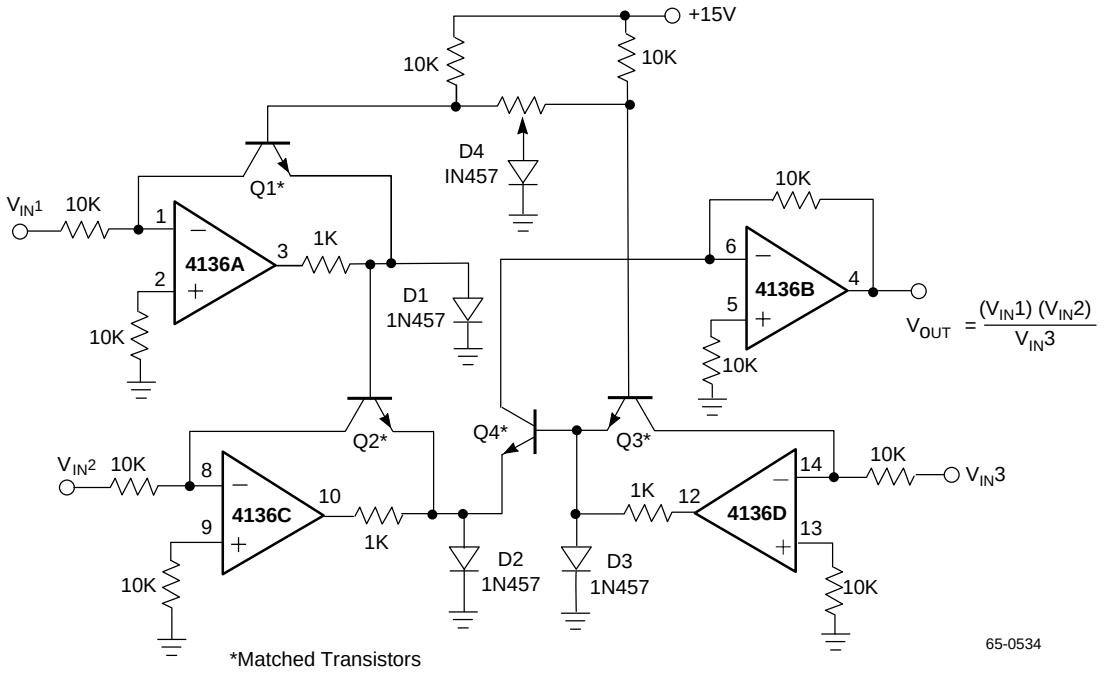


Figure 36. Analog Multiplier/Divider

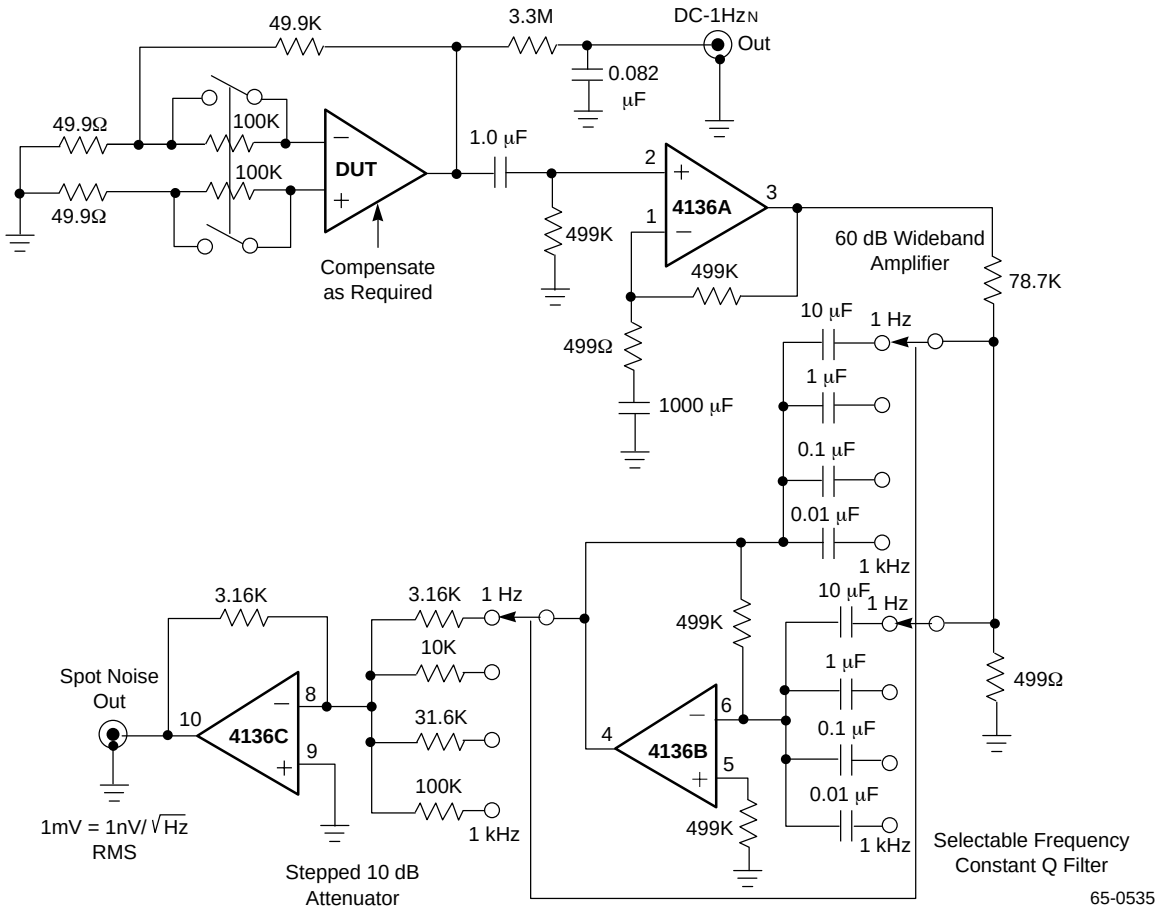
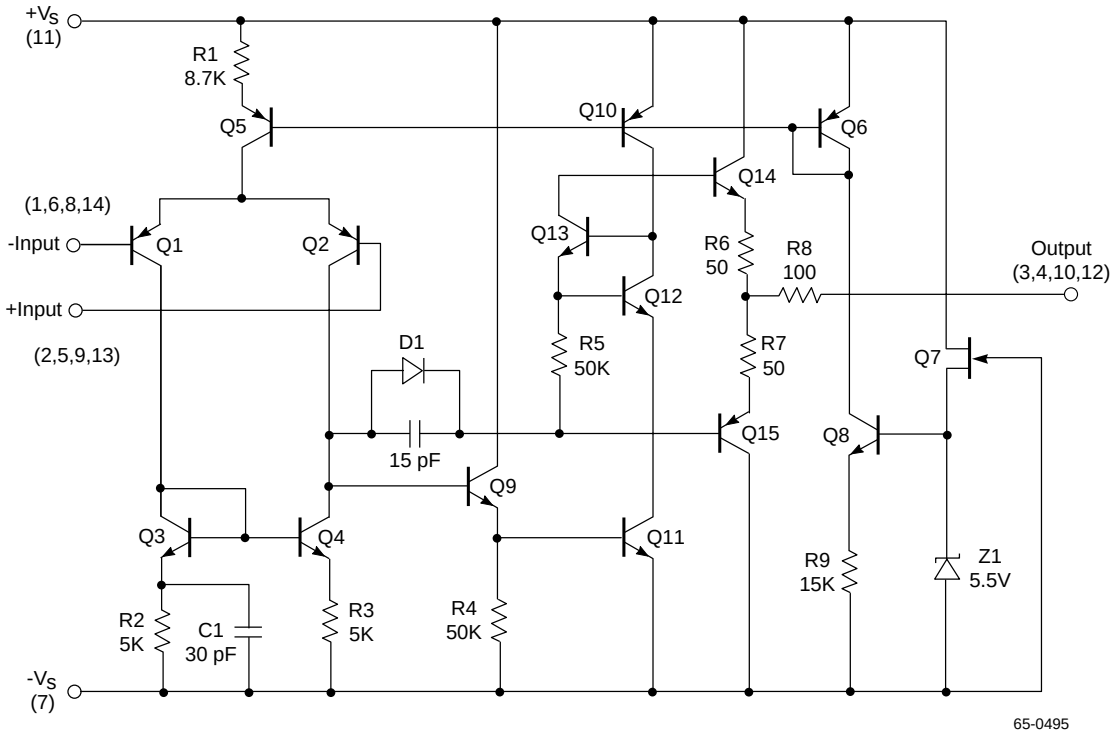


Figure 37. Spot Noise Measurement Test Circuit

Simplified Schematic Diagram



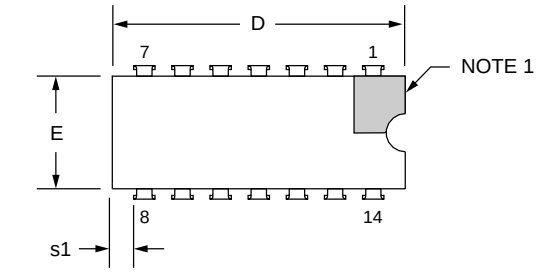
Mechanical Dimensions

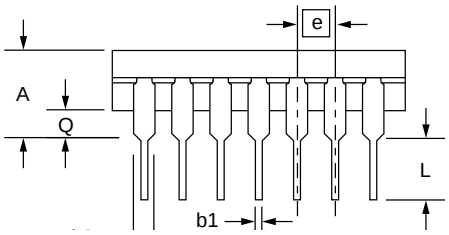
14-Lead Ceramic DIP Package

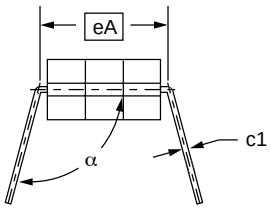
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2
c1	.008	.015	.20	.38	8
D	—	.785	—	19.94	4
E	.220	.310	5.59	7.87	4
e	.100 BSC		2.54 BSC		5, 9
eA	.300 BSC		7.62 BSC		7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 7, 8 and 14 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 14.
6. Applies to all four corners (leads number 1, 7, 8, and 14).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Twelve spaces.







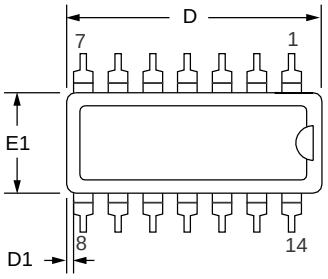
Mechanical Dimensions (continued)

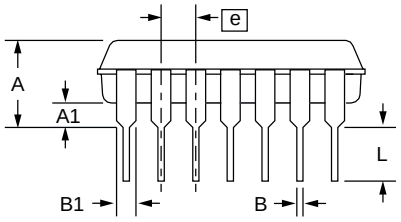
14-Lead Plastic DIP Package

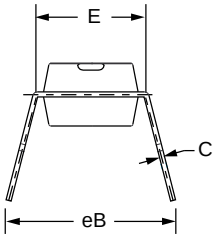
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	.725	.795	18.42	20.19	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.200	2.92	5.08	
N	14		14		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are shown for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.







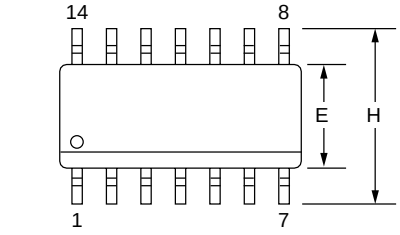
Mechanical Dimensions (continued)

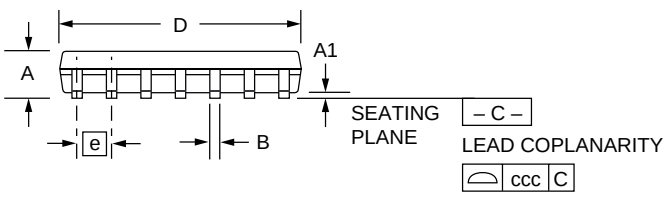
14-Lead SOIC Package

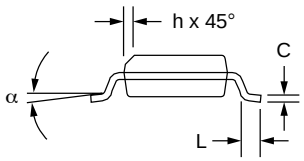
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.19	0.25	5
D	.336	.345	8.54	8.76	2
E	.150	.158	3.81	4.01	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	14		14		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
RC4136N	0° to 70°C	Commercial	14 Pin Plastic DIP	RC4136N
RC4136M	0° to 70°C	Commercial	14 Pin Narrow SOIC	RC4136M
RM4136D	-55°C to +125°C		14 Pin Ceramic DIP	
RM4136D/883[1]	-55°C to +125°C	Military	14 Pin Ceramic DIP	

Note:

1. /883 denotes MIL-STD-883, Par. 1.2.1 compliant device.

RC4152

Voltage-to-Frequency Converters

Features

- Single supply operation
- Pulse output DTL/TTL/CMOS compatible
- Programmable scale factor (K)
- High noise rejection
- Inherent monotonicity
- Easily transmittable output
- Simple full scale trim
- Single-ended input, referenced to ground
- V-F or F-V conversion
- Voltage or current input
- Wide dynamic range

Applications

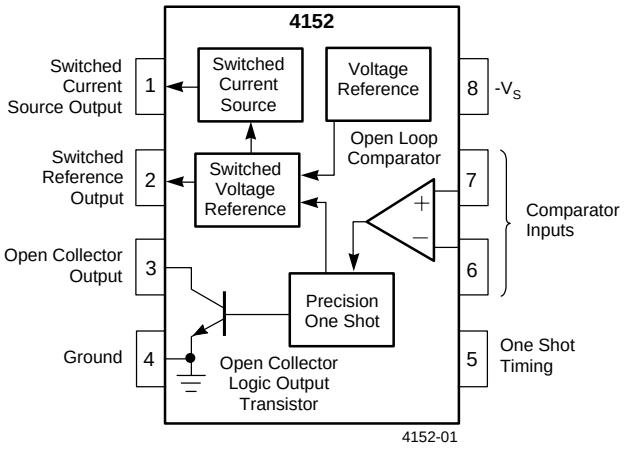
- Precision voltage-to-frequency converters
- Pulse-width modulators
- Programmable pulse generators
- Frequency-to-voltage converters
- Integrating analog-to-digital converters
- Long-term analog integrators
- Signal conversion:
  - Current-to-Frequency
  - Temperature-to-Frequency
  - Pressure-to-Frequency
  - Capacitance-to-Frequency
  - Frequency-to-Current
- Signal isolation:
  - VFC—opto-isolaton—FVC
  - ADC with opto-isolation
- Signal encoding:
  - FSK modulation/demodulation
  - Pulse-width modulation
- Frequency scaling
- DC motor speed control

Description

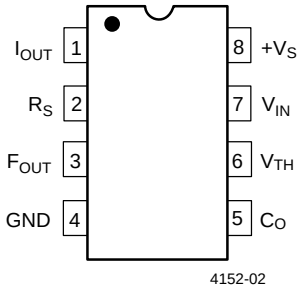
The RC4152 is a monolithic circuit containing all of the active components needed to build a complete voltage-to-frequency converter. Circuits that convert a DC voltage to a pulse train can be built by adding a few resistors and capacitors to the internal comparator, one-shot, voltage reference, and switched current source. Frequency-to-voltage converters (FVCs) and many other signal conditioning circuits are also easily created using these converters.

The RC4151 was the first monolithic VFC available and offers guaranteed temperature and accuracy specifications. The converter is available in a standard 8-pin plastic DIP.

Functional Block Diagram



Pin Assignments



Pin Descriptions

Pin	Function
1	Switched Current Source Output (I_{OUT})
2	Switched Voltage Reference (R_S)
3	Logic Output (Open Collector) (F_{OUT})
4	Ground (GND)
5	One-Shot R, C Timing (C_O)
6	Threshold (V_{TH})
7	Input Voltage (V_{IN})
8	$+V_S$

Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Units
Supply Voltage			+22	V
Internal Power Dissipation			500	mW
Input Voltage	-0.2		$+V_S$	V
Output Sink Current (Frequency Output)			20	mA
Output Short Circuit to Ground			Continuous	
Storage Temperature Range	-65		+150	°C
Operating Temperature Range				
RC4152	0		+70	°C
RV4152N	-25		+85	°C

Note:

1. “Absolute maximum ratings” are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. If the device is subjected to the limits in the absolute maximum ratings for extended periods, its reliability may be impaired. The tables of Electrical Characteristics provides conditions for actual device operation.

Thermal Characteristics

	8-Lead Plastic DIP	Small Outline SO-8
Max. Junction Temp.	+125°C	+125°C
Max. P_D T_A<50°C	468 mW	300mW
Therm. Res θ_{JC}	—	—
Therm. Res θ_{JC}	160°C/W	240°C/W
For T_A>50°C Derate at	6.25 mW/°C	4.17mW/°C

Electrical Characteristics

(V_S = +15V, and T_A = +25°C unless otherwise noted)

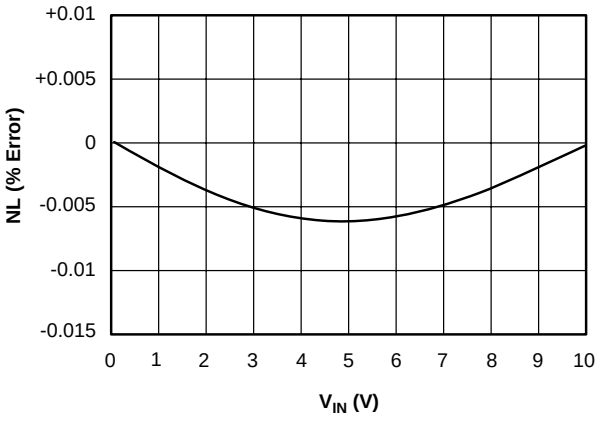
Parameters	Test Conditions	Min.	Typ.	Max.	Units
Power Supply Requirements (Pin 8)					
Supply Current	V_S = +15V		2.5	6.0	mA
Supply Voltage		+7.0	+15	+18	V
Input Comparator (Pins 6 and 7)					
V_{OS}			±2.0	±10	mV
Input Bias Current			-50	-300	nA
Input Offset Current			±30	±100	nA
Input Voltage Range		0	VS-2	VS-3	V
One Shot (Pin 5)					
Threshold Voltage		0.65	0.67	0.69	V_S
Input Bias Current			-50	-500	nA
Saturation Voltage	I = 2.2 mA		0.1	0.5	V
Drift of Timing vs. Temperature[2]	T = 75 μs over the specified temperature range		±30	±50	ppm/°C
Timing Drift vs. Supply Voltage			±100		ppm/V
Switched Current Source (pin 1)[1]					
Output Current	R_S = 16.7K		+138		μA
Drift vs. Temperature[2]	over specified temperature range		±50	±100	ppm/°C
Drift vs. Supply Voltage			0.10		%/V
Leakage Current	Off State		1.0	50	nA
Compliance	Pin 1 = 0V to +10V	1.0	2.5		μA
Reference Voltage (Pin 2)					
V_{REF}		2.0	2.25	2.5	V
Drift vs. Temperature[2]	over specified temperature range		±50	±100	ppm/°C
Logic output (Pin 3) Saturation Voltage	I_{SINK} = 3 mA		0.1	0.5	V
	I_{SINK} = 10 mA		0.8		V
Leakage Current	Off State		0.1	1.0	μA
Nonlinearity Error (Voltage Sourced Circuit of Figure 3)	1.0 Hz to 10 kHz		0.007	0.05	%
Temperature Drift Voltage[2] (Voltage Sourced Circuit of Figure 3)	F_{OUT} = 10 kHz, over specified temperature range		±75	±150	ppm/°C

Notes:

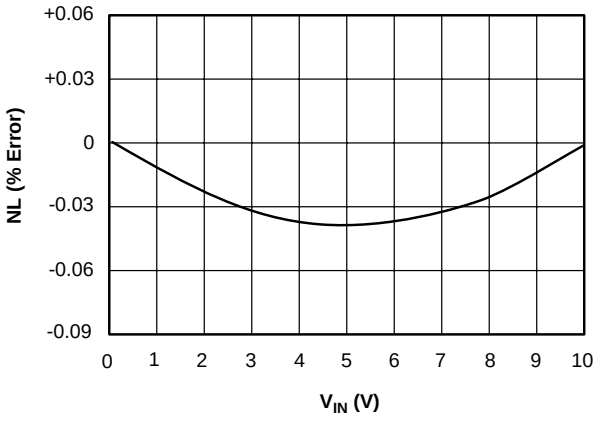
1. Temperature coefficient of output current source (pin 1 output) exclusive of reference voltage drift.
2. Guaranteed but not tested.

Typical Performance Characteristics

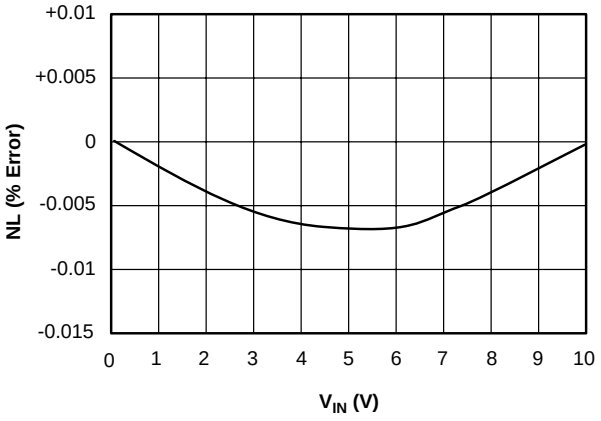
10 KHz Current-Sourced VFC Nonlinearity vs. Input Voltage



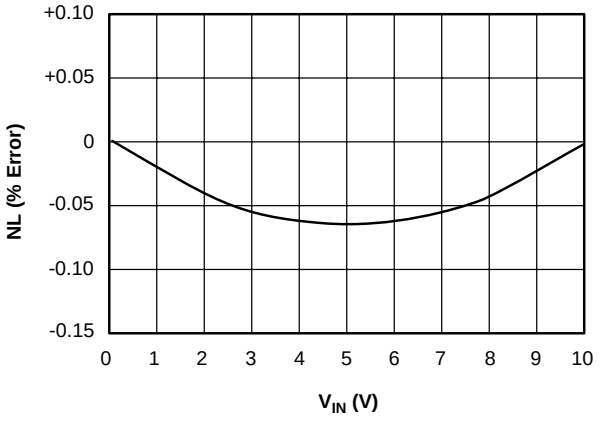
100 KHz Current-Sourced VFC Nonlinearity vs. Input Voltage



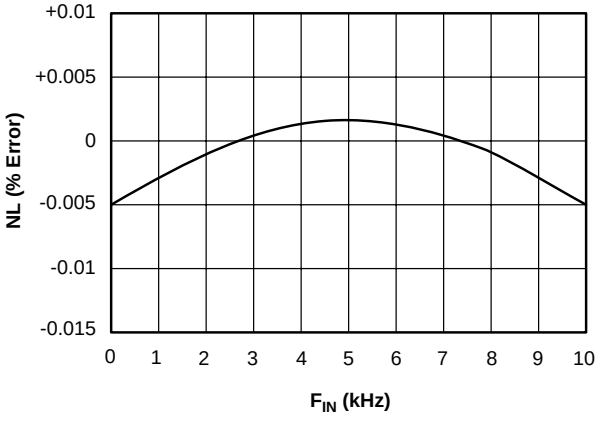
10 KHz Voltage-Sourced VFC Nonlinearity vs. Input Voltage



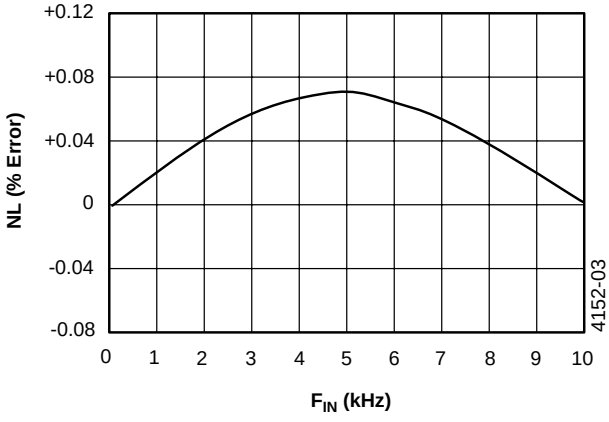
100 KHz Voltage-Sourced VFC Nonlinearity vs. Input Voltage



10 KHz Precision VFC Nonlinearity vs. Input Frequency



100 KHz Precision VFC Nonlinearity vs. Input Frequency



4152-03

Principles of Operation

The RC4152 contains the following components: an open loop comparator, a precision one-shot timer, a switched voltage reference, a switched current source, and an open collector logic output transistor. These functional blocks are internally interconnected. Thus, by adding some external resistors and capacitors, a designer can create a complete voltage-to-frequency converter.

The comparator's output controls the one-shot (monostable timer). The one-shot in turn controls the switched voltage reference, the switched current source and the open collector output transistor. The functional block diagram shows the components and their interconnection.

To detail, if the voltage at pin 7 is greater than the voltage at pin 6, the comparator switches and triggers the one-shot. When the one-shot is triggered, two things happen. First, the one-shot begins its timing period. Second, the one-shot's output turns on the switched voltage reference, the switched current source and the open collector output transistor.

The one-shot creates its timing period much like the popular 555 timer does, by charging a capacitor from a resistor tied to +VS. The one-shot senses the voltage on the capacitor (pin 5) and ends the timing period when the voltage reaches 2/3 of the supply voltage. At the end of the timing period, the capacitor is discharged by a transistor similar to the open collector output transistor.

Meanwhile, during the timing period of the one-shot, the switched current source, the switched voltage reference, and the open collector output transistor all will be switched on. The switched current source (pin 1) will deliver a current proportional to both the reference and an external resistor, RS. The switched reference (pin 2) will supply an output voltage equal to the internal reference voltage (2.25V). The open collector output transistor we be turned on, forcing the logic output (pin 3) to a low state. At the end of the timing period all of these outputs will turn off. The switched voltage reference has produced an off-on-off voltage pulse, the switched current source has emitted a quanta of charge, and the open collector output has transmitted a logic pulse.

To summarize, the purpose of the circuit is to produce a current pulse, well-defined in amplitude and duration, and to simultaneously produce an output pulse which is compatible with most logic families. The circuit's outputs show a pulse waveform in response to a voltage difference between the comparators inputs.

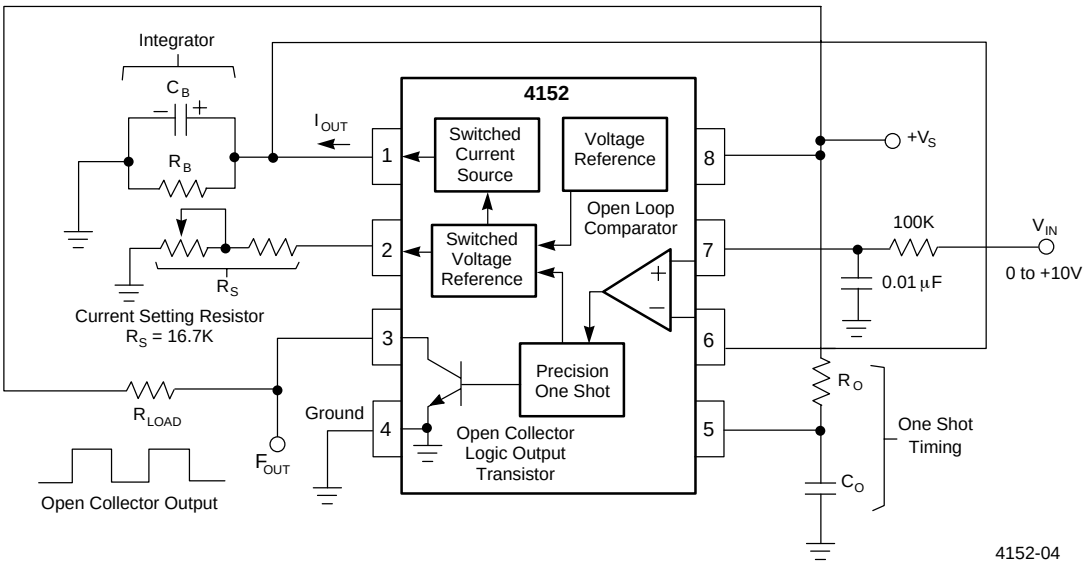


Figure 1. Single Supply VFC

Applications

Single Supply VFC

The stand-alone voltage-to-frequency converter is one of the simplest applications for the RC4152. This application uses only passive external components to create the least expensive VFC circuit (see Figure 1).

The positive input voltage V_{IN} is applied to the input comparator through a low pass filter. The one-shot will fire repetitively and the switched current source will pump out current pulses of amplitude V_{REF}/R_S and duration 1.1 R_OC_O into the integrator. Because the integrator is tied back to the inverting comparator input, a feedback loop is created. The pulse repetition rate will increase until the average voltage on the integrator is equal to the DC input voltage at pin 7. The average voltage at pin 6 is proportional to the output frequency because the amount of charge in each current pulse is precisely controlled.

Because the one-shot firing frequency is the same as the open collector output frequency, the output frequency is directly proportional to V_{IN}.

The external passive components set the scale factor. For best linearity, R_S should be limited to a range of 12 kΩ to 20 kΩ

The reference voltage is nominally 2.25V for the RC4152. Recommended values for different operating frequencies are shown in the table below.

Operating Range	R_O	C_O	R_B	C_B
DC to 1.0 kHz	6.8 kΩ	0.1 μF	100 kΩ	10 μF
DC to 10 kHz	6.8 kΩ	0.01 μF	100 kΩ	10 μF
DC to 100 kHz	6.8 kΩ	0.001 μF	100 kΩ	10 μF

The single supply VFC is recommended for uses where dynamic range of the input is limited, and the input does not reach 0V. With 10 kHz values, nonlinearity will be less than 1.0% for a 10 mV to 10V input range, and response time will be about 135 ms.

Precision Current Sourced VFC

This circuit operates similarly to the single supply VFC, except that the passive R-C integrator has been replaced by an active op amp integrator. This increases the dynamic range down to 0V, improves the response time, and eliminates the nonlinearity error introduced by the limited compliance of the switched current source output.

The integrator algebraically sums the positive current pulses from the switched current source with the current V_{IN}/R_B. To operate correctly, the input voltage must be negative, so that when the circuit is balanced, the two currents cancel.

$$T = \frac{1}{F_{OUT}}$$

$$\frac{|V_{IN}|}{R_B} = I_{OUT}\left[\frac{T_P}{T}\right] \text{ where } TP = 1.1\ R_OC_O$$

$$I_{OUT} = \frac{V_{REF}}{R_S}$$

By rearranging and substituting,

$$F_{OUT} = \frac{|V_{IN}|}{V_{REF}}\frac{R_S}{R_B}\frac{1}{1.1R_OC_O}$$

Recommended component values for different operating frequencies are shown in the table below.

Range Input V_{IN}	Output F_O	Scale Factor	R_O	C_O	C_I	R_B
0 to -10V	0 to 1.0 kHz	0.1 KHz/V	6.8 kΩ	0.1 μF	0.05 μF	100 kΩ
0 to -10V	0 to 10 kHz	1.0 KHz/V	6.8 kΩ	0.01 μF	0.005 μF	100 kΩ
0 to -10V	0 to 100 kHz	10 KHz/V	6.8 kΩ	0.001 μF	500 pF	100 kΩ

The graphs shown under Typical Performance Characteristics show nonlinearity versus input voltage for the precision current sourced VFC. The best linearity is achieved by using an op amp having greater than 1.0 V/μs slew rate, but any op amp can be used.

Precision Voltage Sourced VFC

This circuit is identical to the current sourced VFC, except that the current pulses into the integrator are derived directly from the switched voltage reference. This improves temperature drift at the expense of high frequency linearity.

The switched current source (pin 1) output has been tied to ground, and RS has been put in series between the switched voltage reference (pin 2) and the summing node of the op amp. This eliminates temperature drift associated with the switched current source. The graphs under the Typical Performance Characteristics show that the nonlinearity error is worse at high frequency, when compared with the current sourced circuit.

Single Supply FVC

A frequency-to-voltage converter performs the exact opposite of the VFCs function; it converts an input pulse train into an average output voltage. Incoming pulses trigger the input comparator and fire the one-shot. The one-shot then dumps a charge into the output integrator. The voltage on the integrator becomes a varying DC voltage proportional to the frequency of the input signal. Figure 4 shows a complete single supply FVC.

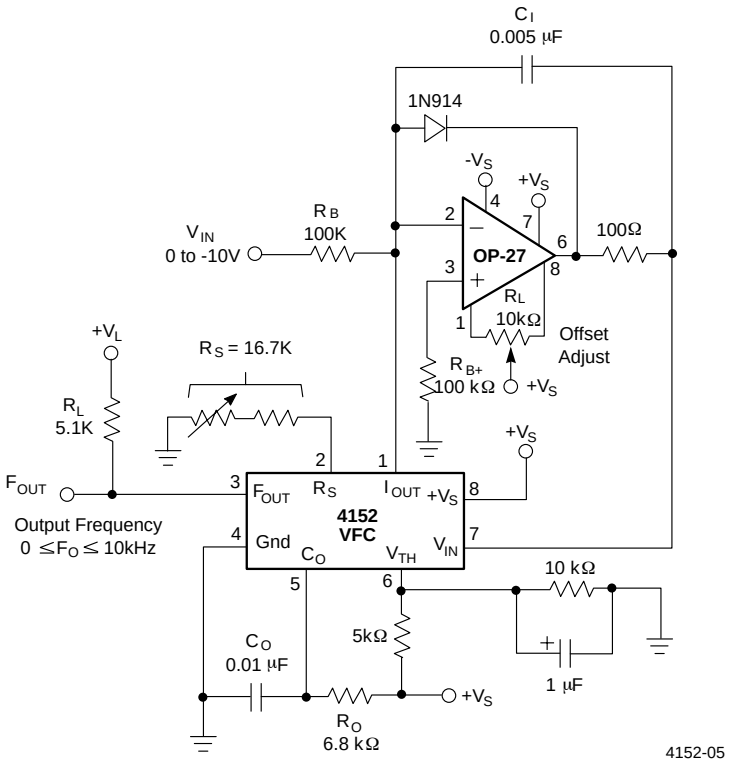


Figure 2. Precision Current Sourced VFC

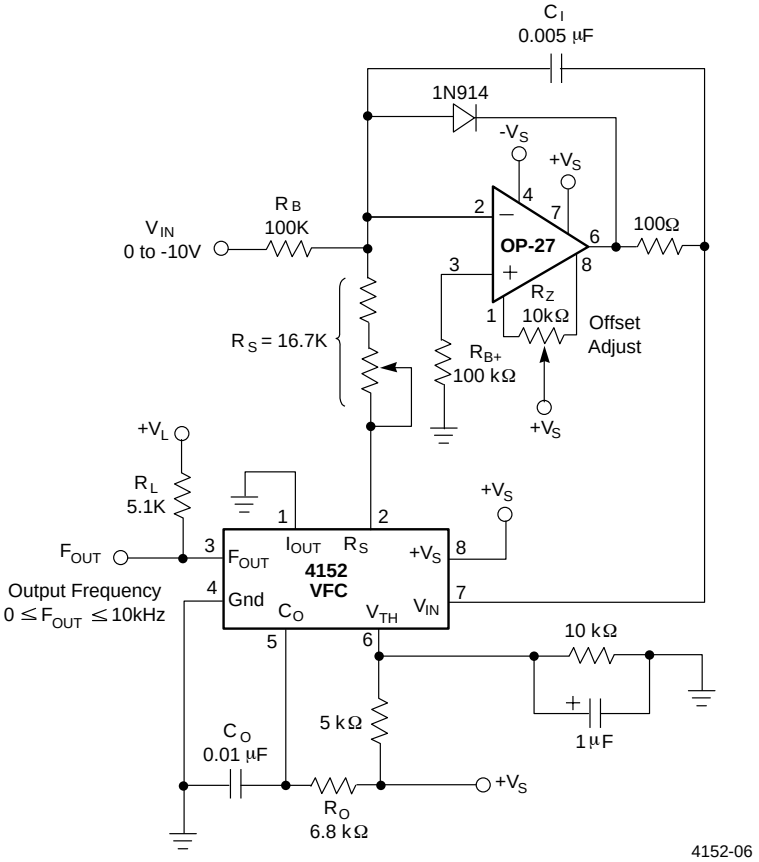


Figure 3. Precision Voltage Sourced VFC

The input waveform must have fast slewing edges, and the differentiated input signal must be less than the timing period of the one-shot, 1.1 $R_O C_O$. A differentiator and divider are used to shape and bias the trigger input; a negative going pulse at pin 6 will cause the comparator to fire the one-shot. The input pulse amplitude must be large enough to trip the comparator, but not so large as to exceed the ICs input voltage ratings.

The output voltage is directly proportional to the input frequency:

$$V_{OUT} = \left[\frac{1.1 R_O C_O R_B V_{REF}}{R_S}\right] F_{IN}(Hz)$$

Output ripple can be minimized by increasing CB, but this will limit the response time. Recommended values for various operating ranges are shown in the following table.

Input Operating Rage	C_{IN}	R_O	C_O	R_B	C_B	Ripple
0 to 1.0 kHz	0.02 µF	6.8 kΩ	0.1 µF	100 kΩ	100 µF	1.0 mV
0 to 10 kHz	0.002 µF	6.8 kΩ	0.01 µF	100 kΩ	10 µF	1.0 mV
0 to 100 kHz	200 pF	6.8 kΩ	0.001 µF	100 kΩ	1.0 µF	1.0 mV

Precision FVC

Linearity, offset and response time can be improved by adding one or more op amps to form an active lowpass filter at the output. A circuit using a single pole active integrator is shown in Figure 5.

The positive output current pulses are averaged by the inverting integrator, causing the output voltage to be negative. Response time can be further improved by adding a double pole filter to replace the single pole filter. Refer to the graphs under Typical Performance Characteristics that show nonlinearity error versus input frequency for the precision FVC circuit.

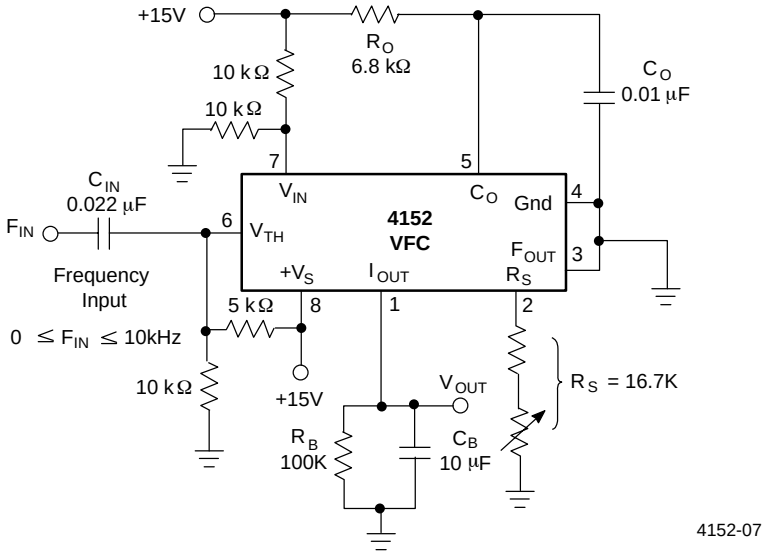
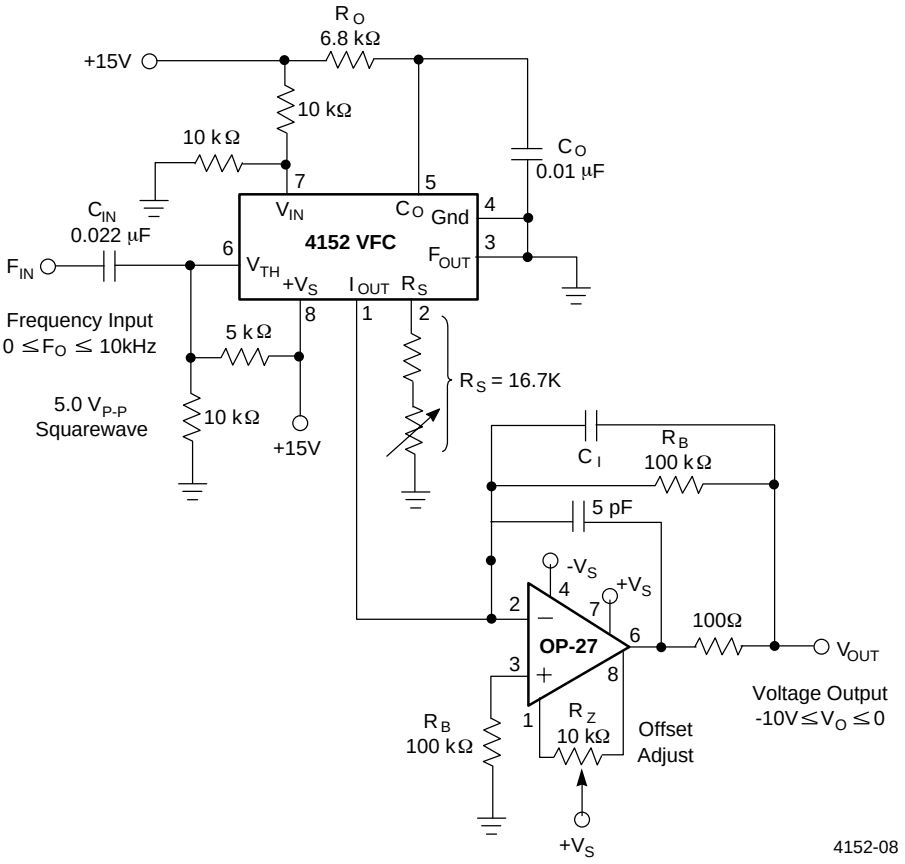
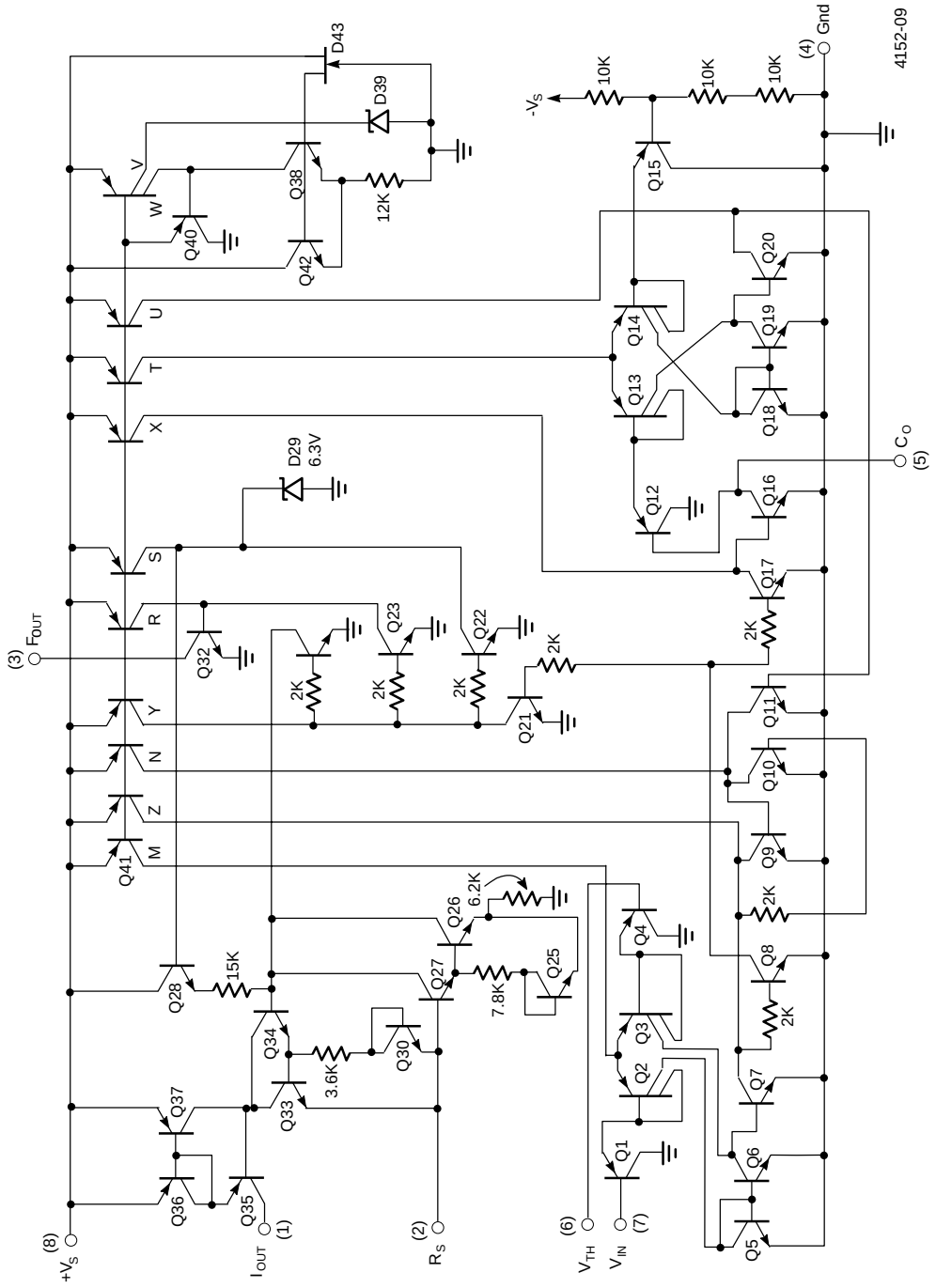


Figure 4. Single Supply FVC


R O
6.8 kΩ
+15V
10 kΩ
10 kΩ
C O
0.01 µF
7
5
C IN
0.022 µF
V IN
C O
Gnd
4
4152 VFC
F OUT
3
F IN
6
V TH
+V S
I OUT
R S
Frequency Input
0 ≤ F O ≤ 10kHz
8
1
2
5 kΩ
R S = 16.7K
5.0 V P-P
Squarewave
10 kΩ
+15V
C I
R B
100 kΩ
5 pF
-V S
+V S
4
7
2
OP-27
6
100Ω
V OUT
3
8
Voltage Output
-10V ≤ V O ≤ 0
R B
100 kΩ
1
R Z
10 kΩ
Offset
Adjust
+V S
4152-08

Schematic Diagram



Notes:

Ordering Information

Part Number	Package	Operating Temperature Range
RC4152N	N	0°C to +70°C
RC4152M	M	0°C to 70°C
RV4152N	N	-25°C to +85°C

Notes:
N = 8-lead plastic DIP
M = 8-lead plastic SOIC

6/25/98 0.0m 003
Stock#DS30004152

RC4153

Voltage-to-Frequency Converter

Features

- 0.1 Hz to 250 kHz dynamic range
- 0.01% F.S. maximum nonlinearity error—0.1Hz to 10 kHz
- 50 ppm/°C maximum gain temperature coefficient (external reference)
- Few external components required

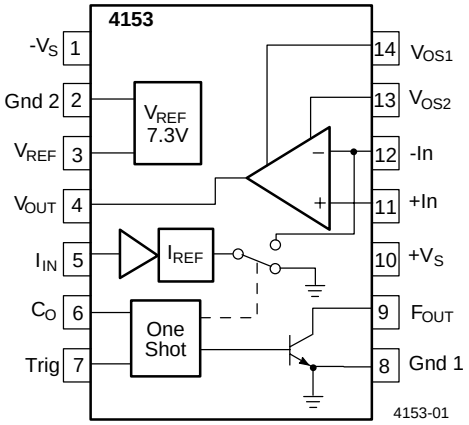
Applications

- Precision voltage-to-frequency converters
- Serial transmission of analog information
- Pulse width modulators
- Frequency-to-voltage converters
- A/D converters and long term integrators
- Signal isolation
- FSK modulation/demodulation
- Frequency scaling
- Motor speed controls
- Phase lock loop stabilization

Description

The 4153 sets a new standard for ease of application and high frequency performance in monolithic voltage-to-frequency converters. This voltage-to-frequency converter requires only four passive external components for precision operation, making it ideal for many low cost applications such as A/D conversion, frequency-to-voltage conversion, and serial data transmission. The improved linearity at high frequency makes it comparable to many dual slop A/D converters both in conversion time and accuracy, while retaining the benefits of voltage-to-frequency conversion, i.e., serial output, cost and size. The speed accuracy and temperature performance of the 4153 is achieved by incorporating high speed ECL logic, a high gain, wide bandwidth op amp, and a buried Zener reference on a single monolithic chip.

Pin Assignments



Pin Descriptions

Pin	Function
1	$-V_S$
2	REF Gnd
3	V_{REF} Output
4	V_{OUT} (Op Amp)
5	I_{IN} (REF Input)
6	C_O (Pulse Width)
7	Trigger Input
8	Circuit Gnd
9	Frequency Output (Open Collector)
10	$+V_S$
11	(+) Op Amp Input
12	(-) Op Amp Input
13	V_{OS} Trim
14	V_{OS} Trim

Absolute Maximum Ratings(1)

Parameter	Min.	Typ.	Max.	Units
Supply Voltage			±18	V
Internal Power Dissipation			500	mW
Input Voltage	$-V_S$		$+V_S$	
Output Sink Current (Frequency Output)			20	mA
Storage Temperature Range	-65		+150	°C
Operating Temperature Range				
RV4153	-25		+80	
RC4153	0°		+70	°C

Note:

1. “Absolute maximum ratings” are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. If the device is subjected to the limits in the absolute maximum ratings for extended periods, its reliability may be impaired. The tables of Electrical Characteristics provide conditions for actual device operation.

Thermal Characteristics

	14-Lead Ceramic DIP	14-Lead Plastic DIP
Max. Junction Temp	+175°C	+125°C
Max. P_D T_A<50°C	1042 mW	468 mW
Therm Res θ_{JC}	60°C/W	—
Therm Res θ_{JA}	120°C/W	160°C/W
For T_A >50°C Derate at	8.33 mW/°C	6.25 mW/°C

Electrical Characteristics

(V_S = ±15V and T_A = +25°C unless otherwise noted)

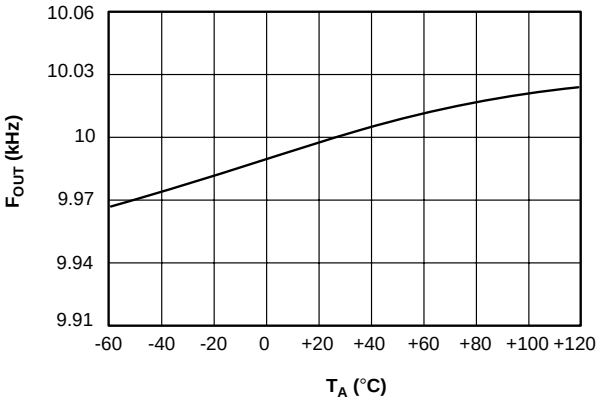
Parameters	Min.	Typ.	Max.	Units
Power Supply Requirements				
Supply Voltage	±12	±15	±18	V
Supply Current ($+V_S$, I_{OUT} = 0)		+4.2	+7.5	mA
($-V_S$, I_{OUT} = 0)		-7	-10	
Full Scale Frequency	250	500		kHz
Transfer Characteristics				
Nonlinearity Error Voltage-to-Frequency[1]				
0.1 Hz ≤ F_{OUT} ≤ 10 kHz		0.002	0.01	%FS
1.0 Hz ≤ F_{OUT} ≤ 100 kHz		0.025	0.05	%FS
5.0 Hz ≤ F_{OUT} ≤ 250 kHz		0.06	0.1	%FS
Nonlinearity Error Frequency-to-Voltage[1]				
0.1 Hz ≤ F_{IN} ≤ 10 kHz		0.002	0.01	%FS
1.0 Hz ≤ F_{IN} ≤ 100 kHz		0.05	0.1	%FS
5.0 Hz ≤ F_{IN} ≤ 250 kHz		0.07	0.12	%FS
Scale Factor Tolerance, F = 10 = kHz $K = \frac{1}{2V_{REF}R_{IN}C_O}$		±0.5		%
Change of Scale Factor with Supply		0.008		%/V
Reference Voltage (V_{REF})		7.3		V
Temperature Stability (0°C to 70°C)[1, 2, 3]				
Scale Factor 10 KHz Nominal		±75	±150	ppm/°C
Reference Voltage		±50	±100	ppm/°C
Scale Factor (External Ref) 10 KHz FS		±25	±50	ppm/°C
Scale Factor (External Ref) 100 KHz FS		±50	±100	ppm/°C
Scale Factor (External Ref) 250 KHz FS		±100	±150	ppm/°C
Op Amp				
Open Loop Output Resistance		230		Ω
Short Circuit Current		25		mA
Gain Bandwidth Product[1]	2.5	3.0		MHz
Slew Rate	0.5	2.0		V/μs
Output Voltage Swing (R_L ≥ 2K)	0 to +10	-0.5 to +14.3		V
Input Bias Current		70	400	nA
Input Offset Voltage (Adjustable to 0)		0.5	5.0	mV
Input Offset Current		30	60	nA
Input Resistance (Differential Mode)		1.0		MΩ
Common Mode Rejection Ratio	75	100		dB
Power Supply Rejection Ratio	70	106		dB
Large Signal Voltage Gain	25	350		V/mV

Parameters	Min.	Typ.	Max.	Units
Switched Current Source				
Reference Current (External Reference)		1.0		mA
Digital Input (Frequency-to-Voltage, Pin 7)				
Logic “0”			0.5	V
Logic “1”	2.0			V
Trigger Current		-50		μA
Logic Output (Open Collector)				
Saturation Voltage (Pin 9)				
I_{SINK} = 4 mA		0.15	0.4	V
I_{SINK} = 10 mA		0.4	1.0	V
I_{LEAK} (Off State)		150		nA

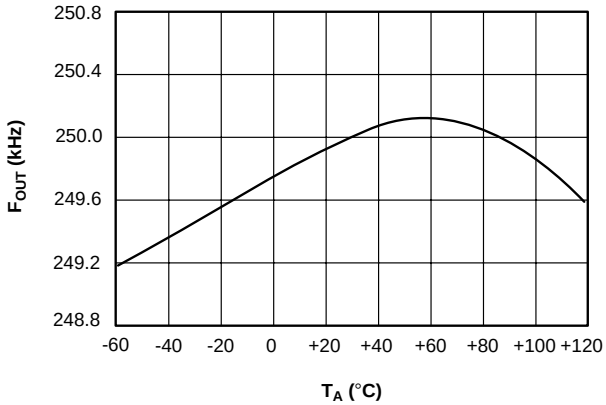
Notes:
1. Guaranteed but not tested.
2. V_{REF} Range: $6.6V \le V_{REF} \le 8.0V$.
3. Over the specified operating temperature range.

Typical Performance Characteristics

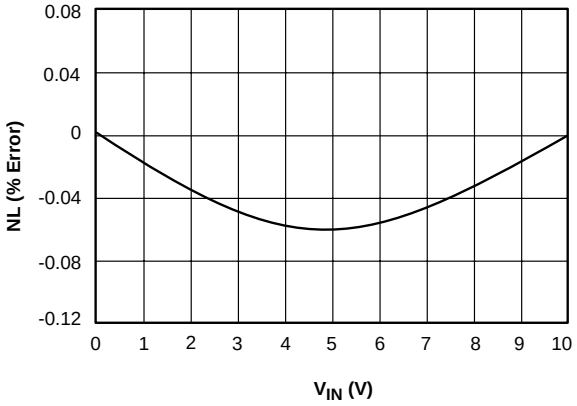
10 kHz Full Scale Drift
Output Frequency vs. Temperature



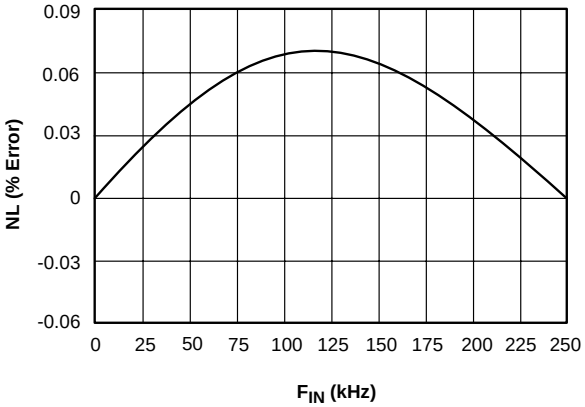
250 kHz Full Scale Drift
Output Frequency vs. Temperature



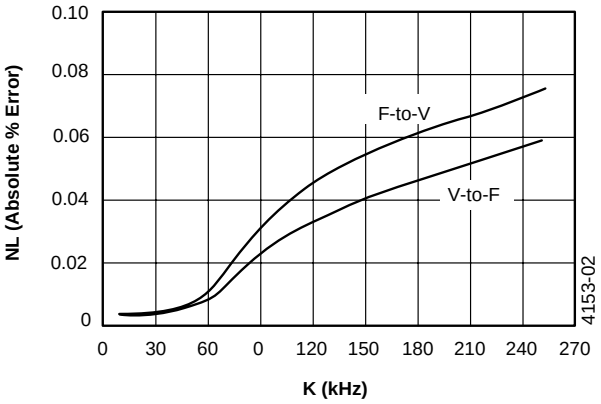
250 kHz Frequency-to-Voltage
Nonlinearity vs. Input Voltage



250 kHz Voltage-to-Frequency
Nonlinearity vs. Input Voltage

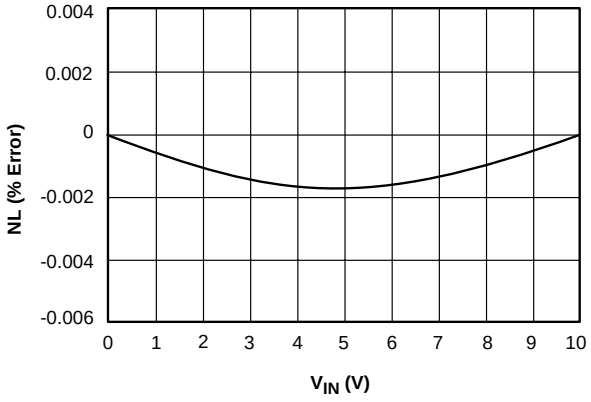


250 kHz Full Scale Peak
Nonlinearity vs. Scale Factor

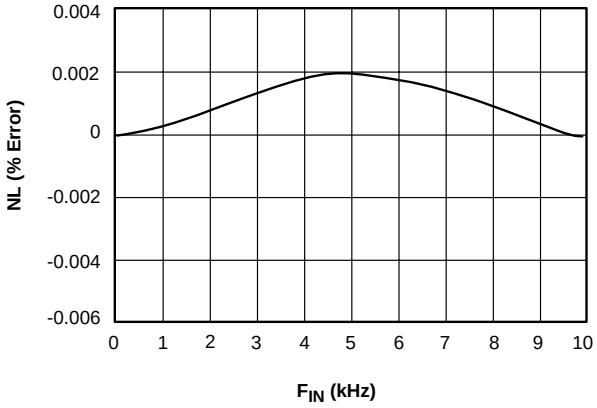


Typical Performance Characteristics

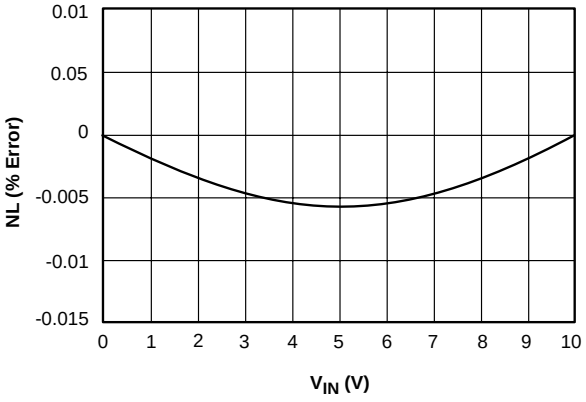
10 KHz Voltage-to-Frequency Nonlinearity vs. Input Voltage



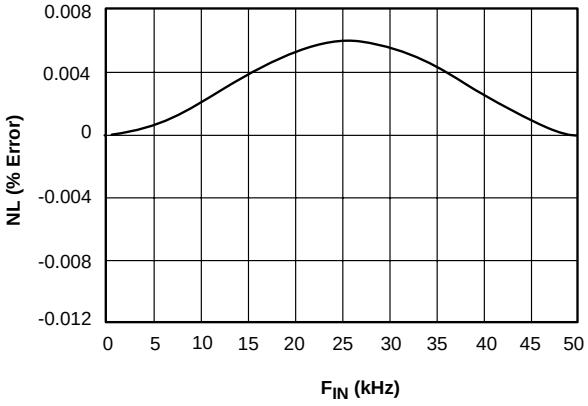
10 KHz Frequency-to-Voltage Nonlinearity vs. Input Frequency



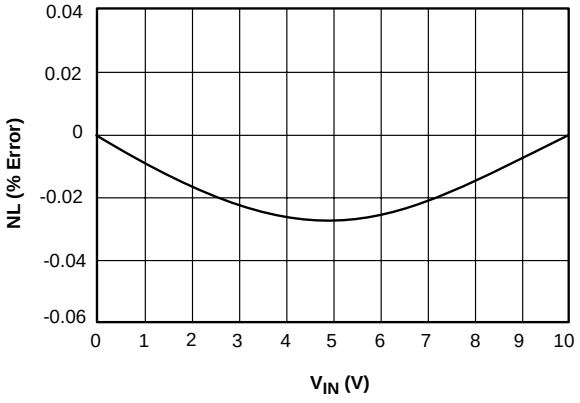
50 KHz Voltage-to-Frequency Nonlinearity vs. Input Voltage



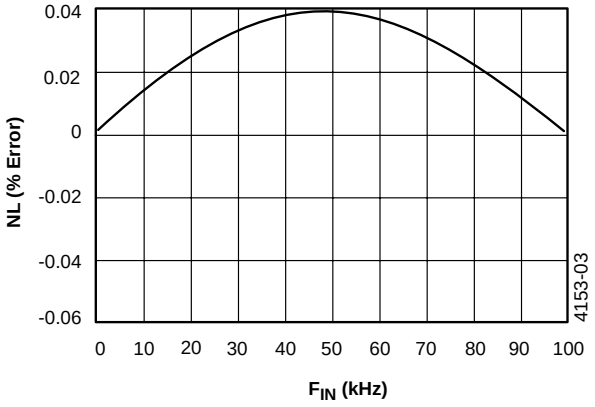
50 KHz Frequency-to-Voltage Nonlinearity vs. Input Frequency



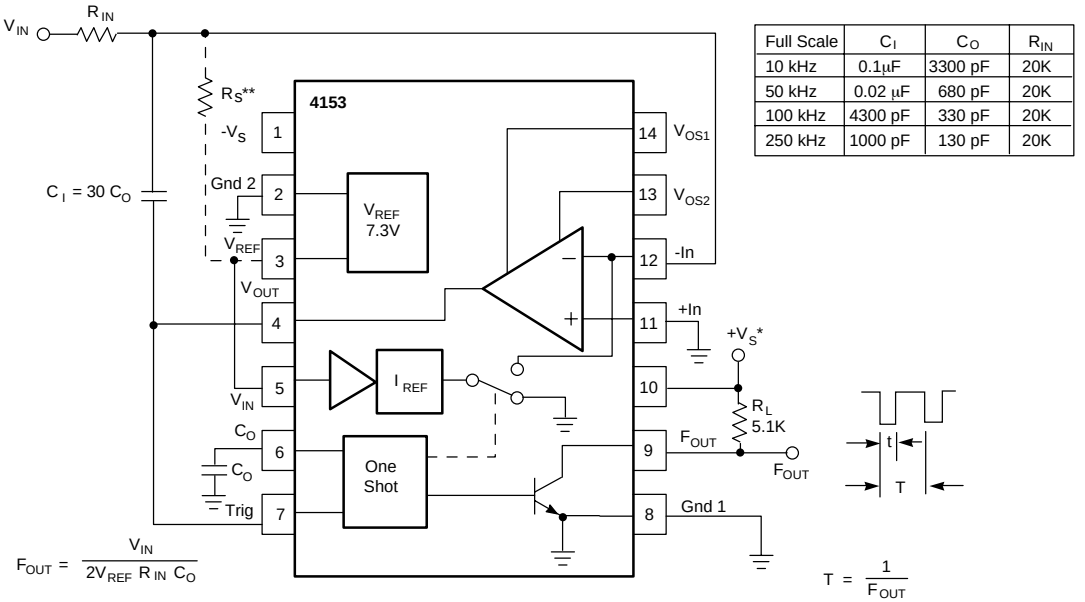
100 KHz Voltage-to-Frequency Nonlinearity vs. Input Voltage



100 KHz Frequency-to-Voltage Nonlinearity vs. Input Frequency

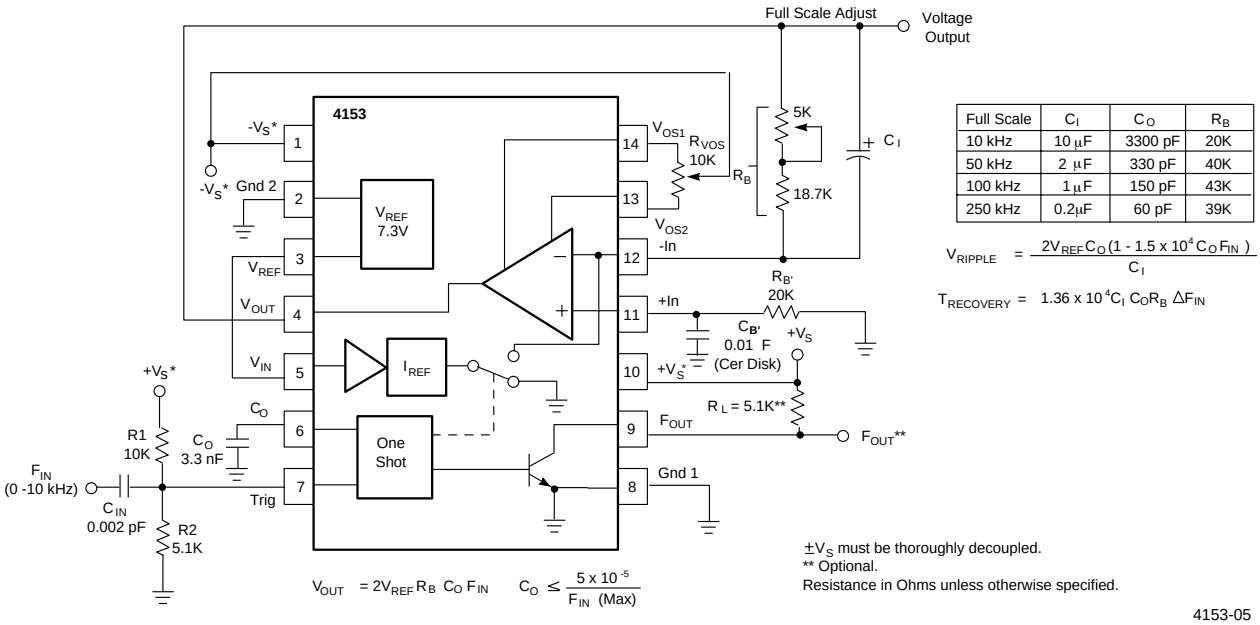


Typical Application Circuits



Full Scale	C_I	C_O	R_{IN}
10 kHz	0.1µF	3300 pF	20K
50 kHz	0.02 µF	680 pF	20K
100 kHz	4300 pF	330 pF	20K
250 kHz	1000 pF	130 pF	20K

Figure 1. Voltage-to-Frequency Converter Minimum Circuit



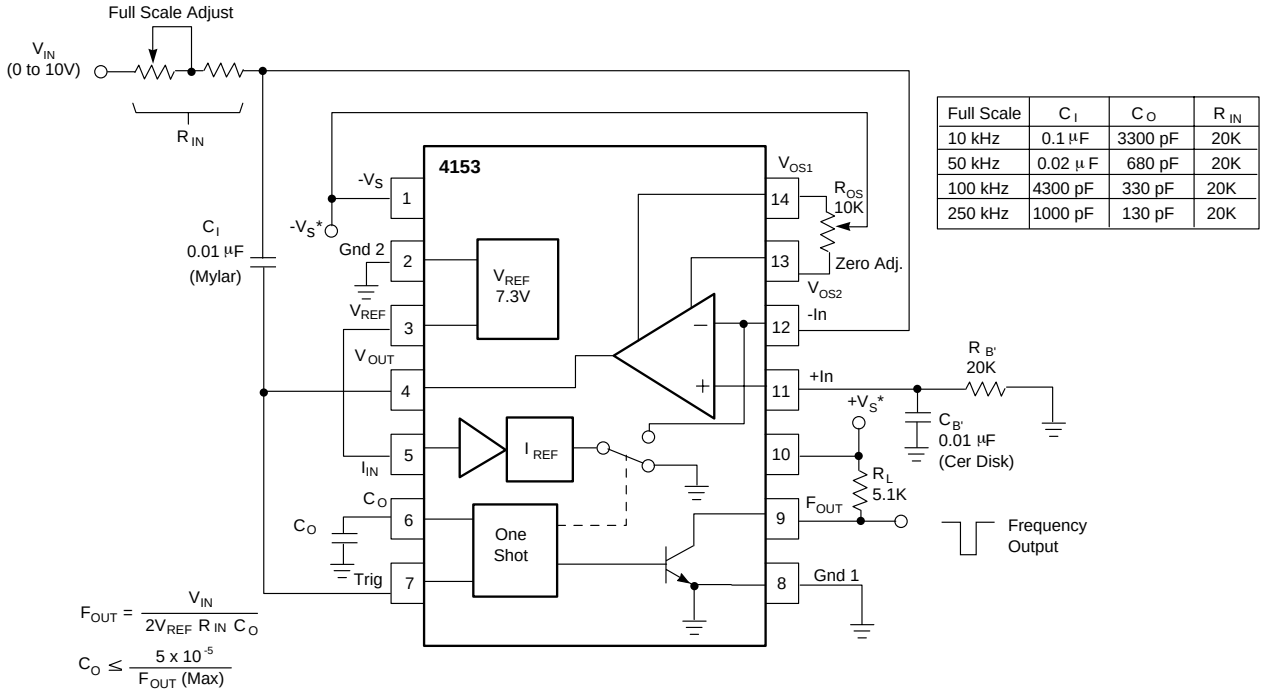
Full Scale	C_I	C_O	R_B
10 kHz	10 µF	3300 pF	20K
50 kHz	2 µF	330 pF	40K
100 kHz	1 µF	150 pF	43K
250 kHz	0.2µF	60 pF	39K

$V_{RIPPLE} = \frac{2V_{REF}C_O(1 - 1.5 \times 10^4 C_O F_{IN})}{C_I}$

$T_{RECOVERY} = 1.36 \times 10^4 C_I\ C_O R_B\ \Delta F_{IN}$

Figure 2. Frequency-to-Voltage Converter

Typical Application Circuit (Continued)



Full Scale	C_I	C_O	R_{IN}
10 kHz	0.1 µF	3300 pF	20K
50 kHz	0.02 µF	680 pF	20K
100 kHz	4300 pF	330 pF	20K
250 kHz	1000 pF	130 pF	20K

* $\pm V_S$ must be thoroughly decoupled.
Resistance in Ohms unless otherwise specified.

4153-06

Figure 3. Voltage-to-Frequency Converter with Offset and Gain Adjusts

Principles of Operation

The 4153 consists of several functional blocks which provide either voltage-to-frequency or frequency-to-voltage conversion, depending on how they are connected. The operation is best understood by examining the block diagram as it is powered in a voltage-to-frequency mode (Figure 4).

When power is first applied, all capacitors are discharged. The input current, V_{IN}/R_{IN}, causes C_I to charge, and point C will try to ramp down. The trigger threshold of the one-shot is approximately +1.3V, and if the integrator output is less than +1.3V, the one-shot will fire and pulse the open collector output E and the switched current source A (see Figures 4 and 5). Because the point C is less than +1.3V, the one-shot fires, and the switched current source delivers a negative current pulse to the integrator. This causes C_{IN} to charge in the opposite direction, and point C will ramp up until the end of the one-shot pulse. At that time, the positive current V_{IN}/R_{IN} will again make point C ramp down until the trigger threshold is reached.

When power is applied, the one-shot will continuously fire until the integrator output exceeds the trigger threshold. Once this is reached, the one-shot will fire as needed to keep the integrator output above the trigger threshold. If V_{IN} is increased, the slope of the downward ramp increases, and the one-shot will fire more often in order to keep the integrator output high. Since the one-shot firing frequency is the same as the open collector output frequency, any increase in V_{IN} will cause an increase in F_{OUT}. This relationship is very linear because the amount of charge in each I_{OUT} pulse is carefully defined, both in magnitude and duration. The duration of the pulse is set by the timing capacitor C_O (point D). This feedback system is called a charge-balanced loop.

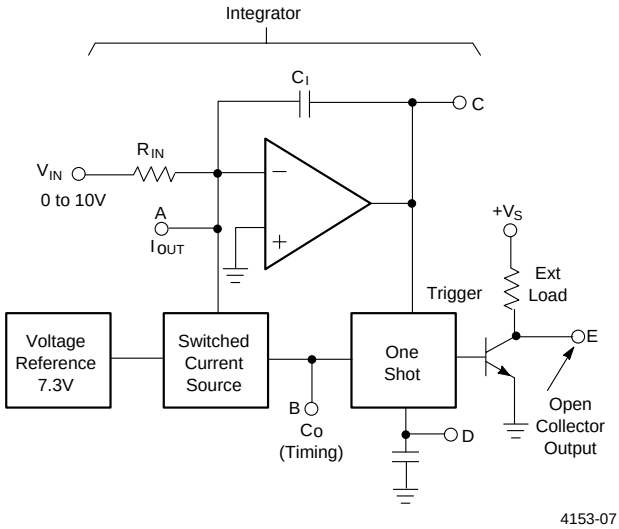


Figure 4. Voltage-to-Frequency Block Diagram

The scale factor K (the number of pulses per second or a specified V_{IN}), is adjusted by changing either R_{IN} and therefore I_{IN}, or by changing the amount of charge in each I_{OUT} pulse. Since the magnitude of I_{OUT} is fixed at 1 milliamp, the way to change the amount of charge is by adjusting the one-shot duration set by C_O (I_{OUT} may be adjusted by changing V_{REF}). The accuracy of the relationship between V_{IN} and F_{OUT} is affected by three major sources of error: temperature drift, nonlinearity and offset.

The total temperature drift is the sum of the individual drift of the components that make up the system. The greatest source of drift in a typical application is in the timing capacitor, C_O. Low temperature coefficient capacitors, such as silver mica and polystyrene, should be measured for drift using a capacitance meter. Experimentation has shown that the lowest tempco's are achieved by wiring a parallel capacitor composed of 70% silver mica and 30% polystyrene.

The reference on the chip can be replaced by an external reference with much tighter drift specifications, such as an LM199. The 199's 6.9V output is close to the 4153's 7.3V output, and has less than 10 ppm/°C drift.

Nonlinearity is primarily caused by changes in the precise amount of charge in each I_{OUT} pulse. As frequency increases, internal stray capacitances and switching problems change the width and amplitude of the I_{OUT} pulses, causing a nonlinear relationship between V_{IN} and F_{OUT}.

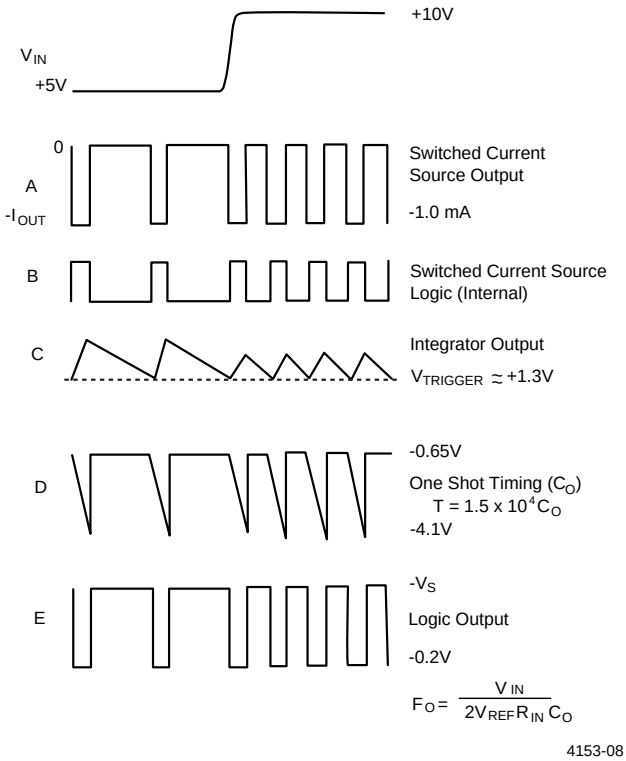


Figure 5. Voltage-to-Frequency Timing Waveforms

For this reason, the scale factor you choose should be below 1 KHz/V or as low as the acquisition time of your system will allow.

Nonlinearity is also affected by the rate of C_I to C_O. Less error can be achieved by increasing the value of C_I, but this affects response time and temperature drift. Optimum value for C_I and C_O are shown In the tables in Figures 1, 2, and 3. These values represent the best compromise of nonlinearity and temperature drift. Polypropylene, mylar or polystyrene capacitors should be used for C_I.

The accuracy at low input voltages is limited by the offset and V_{OS} drift of the op amp. To improve this condition, an offset adjust is provided.

Once your system is running, it may be calibrated as follows: apply a measured full scale input voltage and adjust R_{IN} until the scale factor is correct. For precise applications, trimming by soldering metal film resistors in parallel is recommended instead of trimpots, which have bad tempco's and are easily taken out of adjustment by mechanical shock. After the scale factor is calibrated, apply a known small input voltage (approximately 10 mV) and adjust the op amp offset until the output frequency equals the input multiplied by the scale factor.

The output E consists of a series of negative going pulses with a pulse width equal to the one-shot time. The open collector pull-up resistor may be connected to a different supply (such as 5V for TTL) as long a it does not exceed the value of $+V_S$ applied to pin 10. The load current should be kept below 10 mA in order to minimize strain on the device. Pins 2 and 8 must be grounded in all applications, even if the open collector transistor is not used.

Figure 6 shows the complete circuit for a precision frequency-to-voltage converter. The circuit converts an input frequency to a proportional voltage by integrating the switched current source output. As the input frequency increases, the number of I_{OUT} pulses delivered to the integrator increases, thus increasing the average output voltage. Depending on the time constant of the integrator, there will be some ripple on the output. The output may be further filtered, but this will reduce the response time. A second order filter will decrease ripple and improve response time.

The input waveform must meet three conditions for proper frequency-to-voltage operation. First, it must have sufficient amplitude and offset to swing above and below the 1.3V trigger threshold (See Figure 6 for an example of AC coupling and offset bias.) Second, it must be a fast slewing waveform having a quick rise time. A comparator may be used to square it up. Finally, the input pulse width must not exceed the one-shot time, in order to avoid retriggering the one-shot (AC couple the Input).

Capacitive coupling between the trigger input and the timing capacitor pin may occur if the input waveform is a square-wave or the input has a short period. This can cause gross nonlinearity due to changes in the one-shot timing waveform (See Figure 7). This problem can be avoided by keeping the value of C_O small, and thereby keeping the timing period less than the input waveform period.

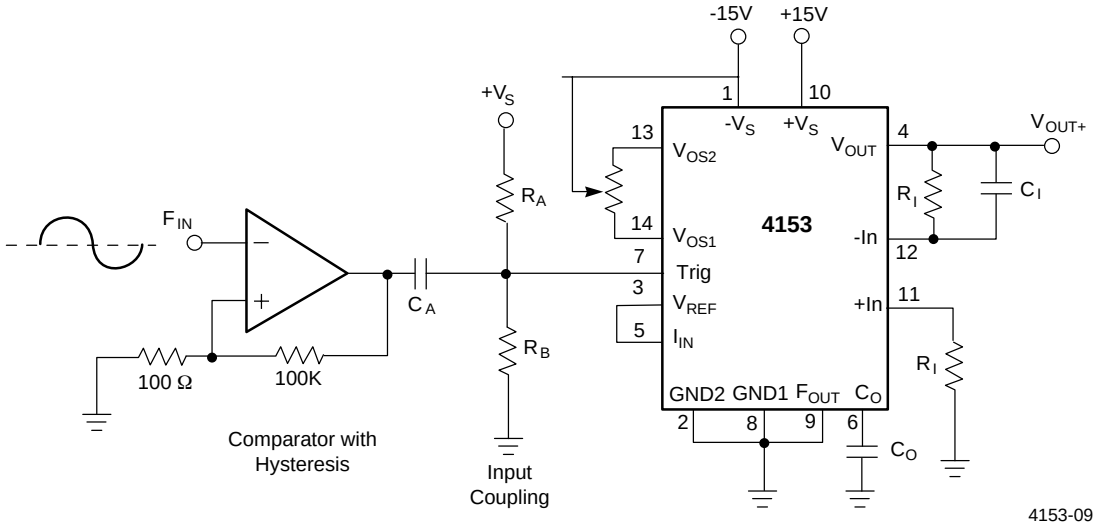


Figure 6. Frequency-to-Voltage Precision Converter

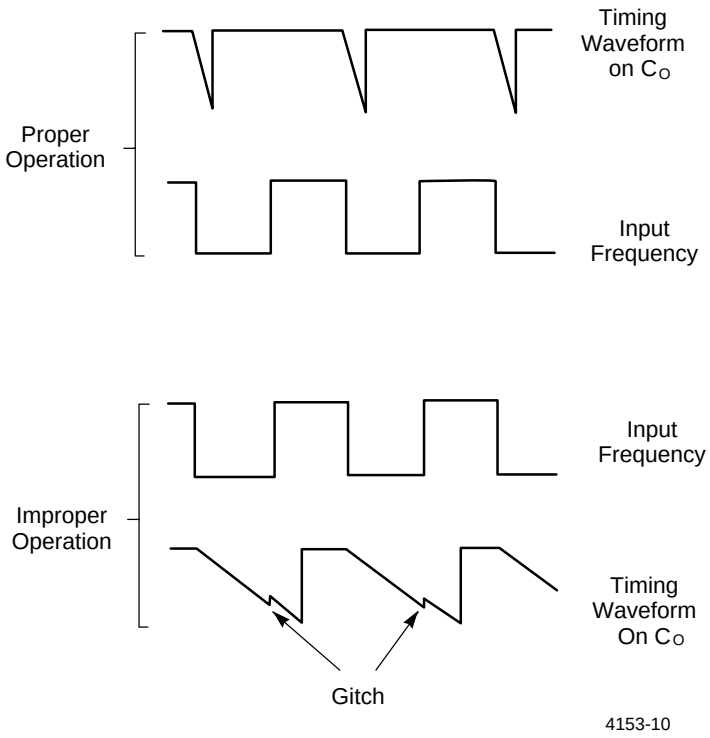


Figure 7. Frequency-to-Voltage Timing Waveforms

Detailed Circuit Operation

The circuit consists of a buried zener reference (breakdown occurs below the surface of the die, reducing noise and contamination), a high speed one-shot, a high speed switched precision voltage-to-current converter and an open-collector output transistor.

Figure 8 shows a block diagram of the high speed one-shot and Figure 9 shows the monolithic implementation. A trigger pulse sets the R-S latch, which lets C_O charge from I_T. When the voltage on C_O exceeds V_{TH}. the comparator resets the latch and discharges C_O. Looking at the detailed schematic, a positive trigger voltage turns on Q5, turns off Q4, and turns on Q3. Q3 provides more drive to Q5 keeping it on and latching the base of Q11 low. This turns on the switched current source and turns off Q1, allowing C_O to charge in a negative direction. When the voltage on C_O exceeds V_{TH}, Q13's collector pulls Q3's base down, resetting the latch, turning off the switched current source and discharging C_O through Q1. Note that all of the transistors in the signal path are NPNs, and that the voltage swings are minimized ECL fashion to reduce delays. Minimum delay means minimum drift of the resultant VFC scale factor at high frequency.

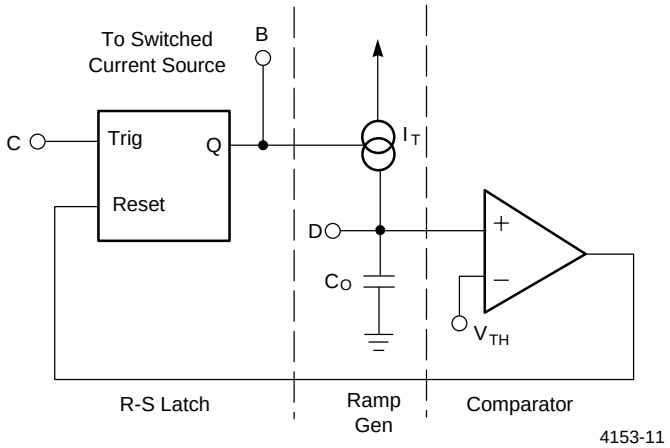


Figure 8. One-Shot Block Diagram

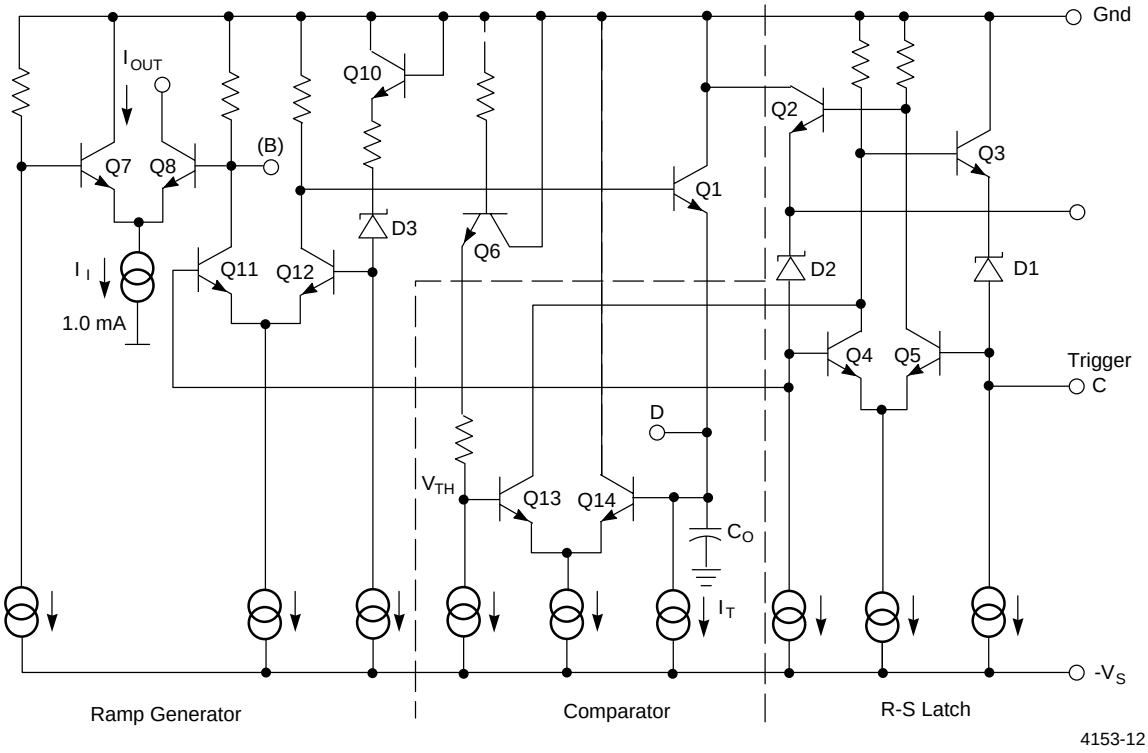


Figure 9. One-Shot (Detail)

The switched current source is shown as a block diagram in Figure 10 and detailed in Figure 11. The summing node (+ input of the op amp) is held at 0V by the amplifier feedback, causing V_{REF} to be applied across R60. This current (V_{REF}/R60), minus the small amplifier bias current, flows through Q35. Q35 develops a V_{BE} dependent on that current. This V_{BE} is developed across Q36. Since Q35 and Q36 are equal in area, the currents are equal. The mirrored current is switched by the one-shot output.

The detail schematic shows the amplifier and load (Q21 through Q34), the mirror transistors (Q35, Q36) and the differential switching transistors (Q7, Q8). The amplifier uses a complementary paraphase input composed of Q21 through Q26 with a current mirror formed by Q27 through Q30, which converts from differential to single-ended output. Level-shift diodes Q32 and Q34 and emitter follower Q31 bootstrap the emitters of the mirror devices Q29 and Q30 to increase gain and lower input offsets, which would otherwise be caused by unbalanced collector voltages on Q23 and Q26.

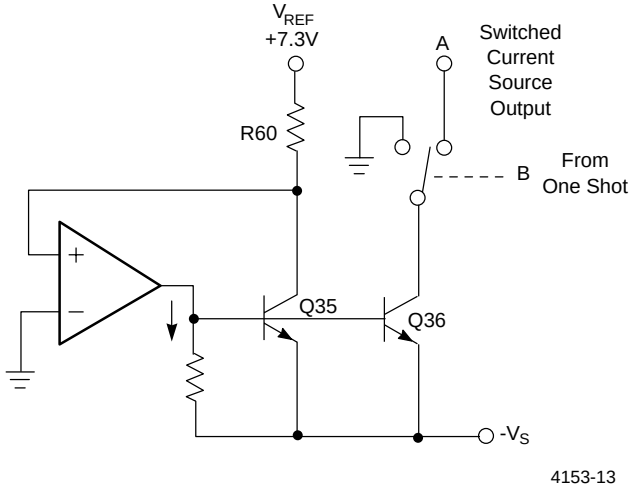


Figure 10. Switched Current Source Block Diagram

Matching emitter currents in Q35 and Q36 are assured by degeneration resistors R3 and R4. The differential switch allows the current source to remain active continuously, shunting to ground in the off state. This helps stabilize the output, and again, NPNs reduce switching time, timing errors, and most important, drift of timing errors over temperature.

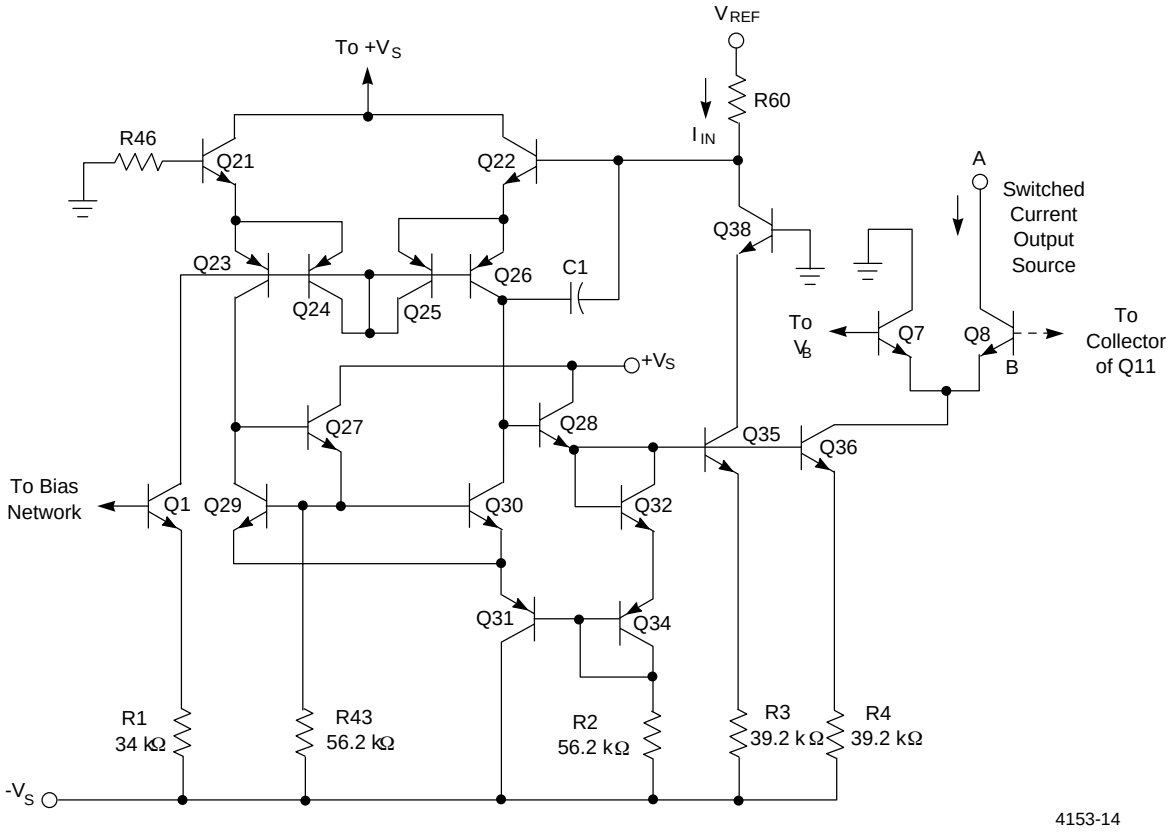
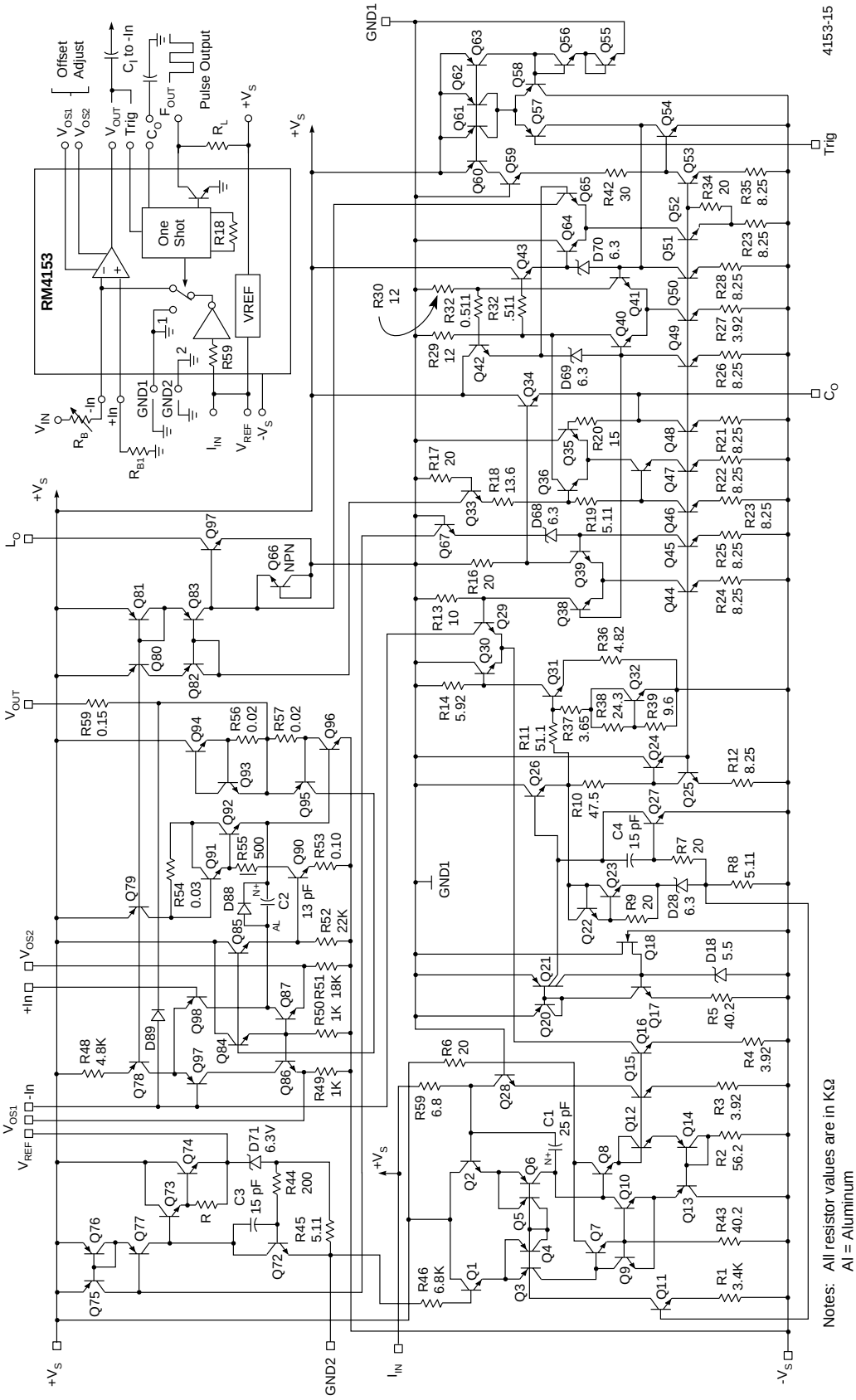


Figure 11. Switched Current Source (Detail)

Schematic Diagram



Notes:

Ordering Information

Part Number	Package	Operating Temperature Range
RC4153N	N	0°C to +70°C
RV4153N	N	-25°C to 80°C

Notes:
N = 14-lead plastic DIP

6/25/98 0.0m 002
Stock#DS30004153

RC4156/RC4157

High Performance Quad Operational Amplifiers

Features

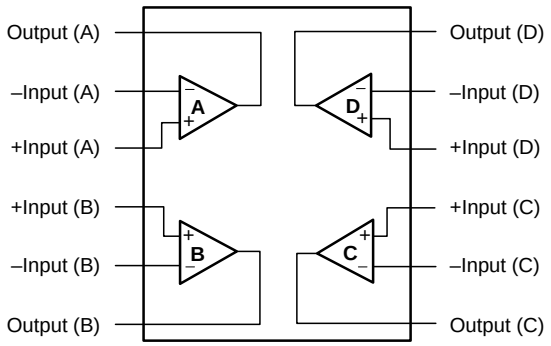
- Unity gain bandwidth for RC4156 – 3.5 MHz
- Unity gain bandwidth for RC4157 – 19 MHz
- High slew rate for RC4156 – 1.6 V/μS
- High slew rate for RC4157 – 8.0V/μS
- Low noise voltage – 1.4 μVRMS
- Indefinite short circuit protection
- No crossover distortion

Description

The RC4156 and RC4157 are monolithic integrated circuits, consisting of four independent high performance operational amplifiers constructed with an advanced epitaxial process.

These amplifiers feature improved AC performance which far exceeds that of the 741 type amplifiers. Also featured are excellent input characteristics and low noise, making this device the optimum choice for audio, active filter and instrumentation applications. The RC4157 is a decompensated version of the RC4156 and is AC stable in gain configurations of -5 or greater.

Block Diagram



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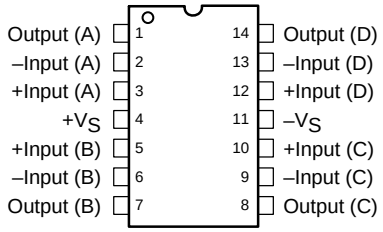
Pin Assignments



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Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min	Typ	Max	Units
Supply Voltage				±20	V
Input Voltage[2]				±15	V
Differential Input Voltage				30	V
Output Short Circuit Duration[3]		Indefinite			
$P_D T_A$ < 50°C	SOIC			300	mW
	PDIP			468	mW
	CerDIP			1042	mW
Operating Temperature	RC4156/RC4157	0		70	°C
	RM4156/RM4157	-55		+125	°C
Storage Temperature		-65		150	°C
Junction Temperature	SOIC, PDIP			125	°C
	CerDIP			175	°C
Lead Soldering Temperature (60 seconds)	DIP			300	°C
	SOIC			260	°C
For T_A > 50°C Derate at	SOIC		5.0		mW/°C
	PDIP		6.25		mW/°C
	CerDIP		8.38		mW/°C

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit to ground on one amplifier only.

Operating Conditions

Parameter			Min	Typ	Max	Units
θ_{JC}	Thermal resistance			60		°C/W
θ_{JA}	Thermal resistance	SOIC		200		°C/W
		PDIP		160		°C/W
		CerDIP		120		°C/W

Electrical Characteristics

(V_S = ±15V, RM = -55°C ≤ T_A ≤ +125°C, RC = 0°C ≤ T_A ≤ +70°C)

Parameters	Test Conditions	RM4156/4157			RC4156/4157			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	R_S ≤ 10 kΩ			5.0			6.5	mV
Input Offset Current				75			100	nA
Input Bias Current				320			400	nA
Large Signal Voltage Gain	R_L ≥ 2 kΩ,V_{OUT} ±10V	25			15			V/mV
Output Voltage Swing	R_L ≥ 2 kΩ	±10			±10			V
Supply Current			10			10		mA
Average Input Offset Voltage Drift			5.0			5.0		μV/°C

Electrical Characteristics

(V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	RM4156/4157			RC4156/4157			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 10\ k\Omega$		0.5	3.0		1.0	5.0	mV
Input Offset Current			15	30		30	50	nA
Input Bias Current			60	200		60	300	nA
Input Resistance			0.5			0.5		MΩ
Large Signal Voltage Gain	$R_L \geq 2\ k\Omega$, V_{OUT} ±10V	50	100		25	100		V/mV
Output Voltage Swing	$R_L \geq 10\ k\Omega$	±12	±14		±12	±14		V
	$R_L \geq 2\ k\Omega$	±10	±13		±10	±13		V
Input Voltage Range		±12	±14		±12	±14		V
Output Resistance			230			230		Ω
Short Circuit Current			25			25		mA
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	80			80			dB
Power Supply Rejection Ratio	$R_S \leq 10\ k\Omega$	80			80			dB
Supply Current (All Amplifiers)	$R_L = \infty$		4.5	5.0		5.0	7.0	mA
Transient Response (4156)								
Rise Time			60			60		nS
Overshoot			25			25		%
Slew Rate		1.3	1.6		1.3	1.6		V/μS
Unity Gain Bandwidth (4156)		2.8	3.5		2.8	3.5		MHz
Phase Margin (4156)	R_L = 2 kΩ, C_L = 50 pF		50			50		%
Transient Response (4157)	A_V = -5							
Rise Time			50			50		nS
Overshoot			25			25		%
Slew Rate		6.5	8.0		6.5	8.0		V/μS
Unity Gain Bandwidth (4157)	A_V = -5	15	19		15	19		MHz
Phase Margin (4157)	A_V = -5, R_L = 2 kΩ, C_L = 50 pF		50			50		%
Power Bandwidth	$V_{OUT} = 20V_{p-p}$	20	25		20	25		kHz
Input Noise Voltage [1]	F = 20 Hz to 20 kHz		1.4	5.0		1.4	5.0	μV_{RMS}
Input Noise Current	F = 20 Hz to 20 kHz		15			15		pA_{RMS}
Channel Separation			108			108		dB

Note:

1. Sample tested only.

Typical Performance Characteristics

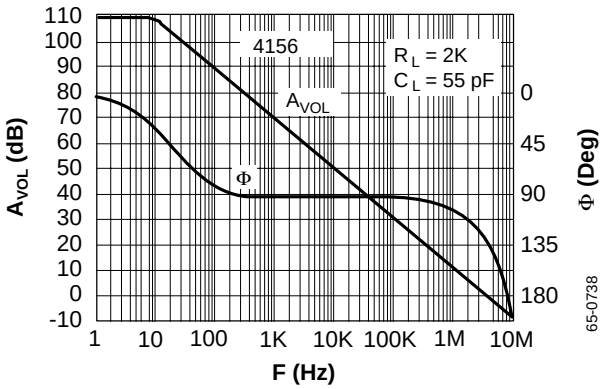


Figure 1. Open Loop Gain, Phase vs. Frequency

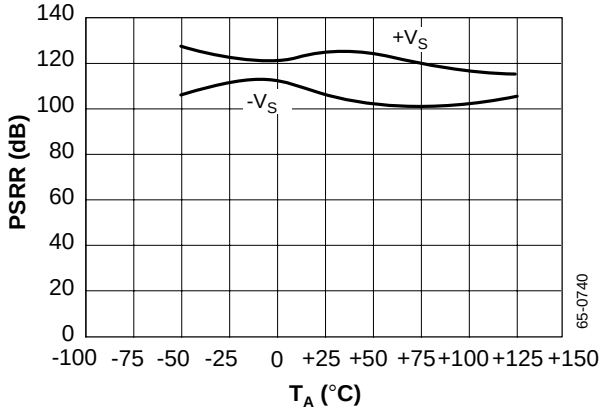
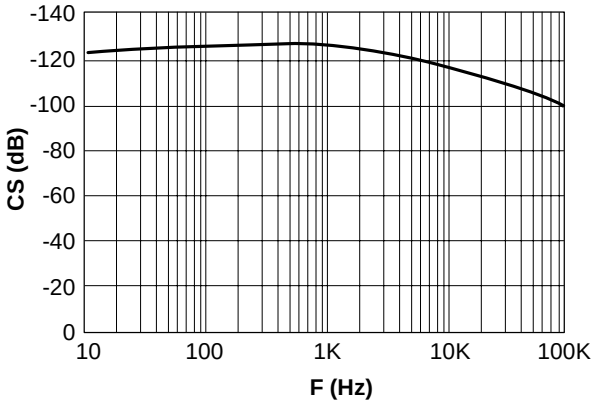


Figure 2. PSRR vs. Temperature



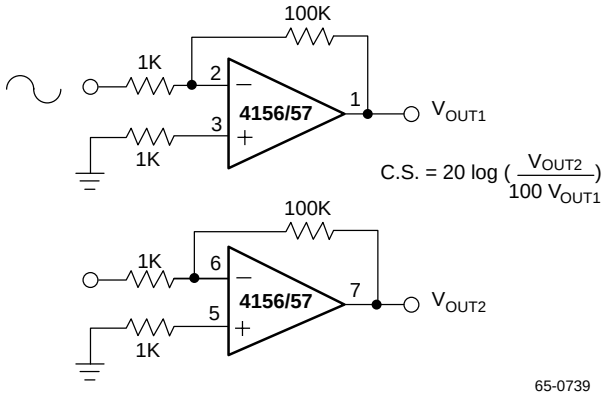


Figure 3. Channel Separation vs. Frequency

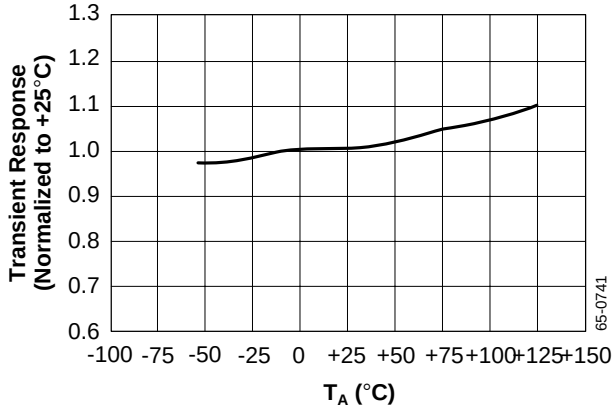


Figure 4. Transient Response vs. Temperature

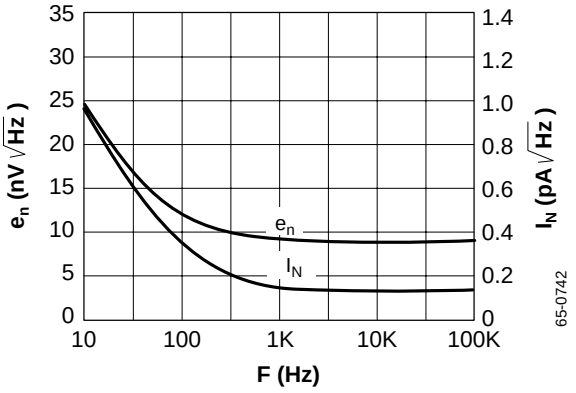


Figure 5. Input Noise Voltage, Current Density vs. Frequency

Typical Performance Characteristics (continued)

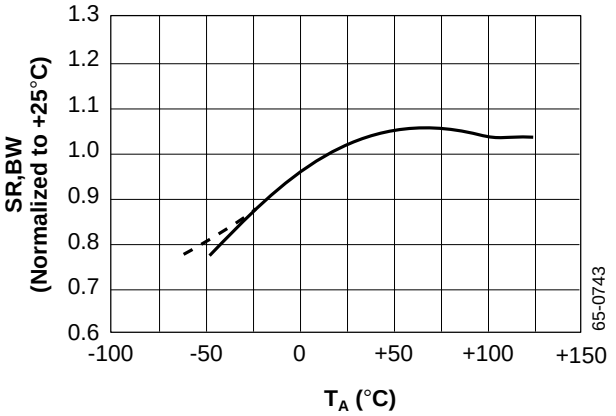


Figure 6. Slew Rate, Bandwidth vs. Temperature

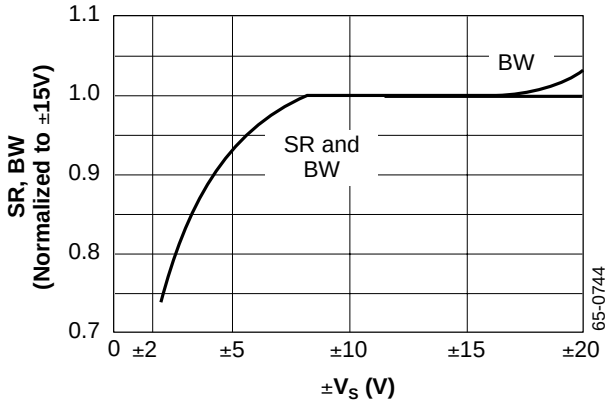


Figure 7. Slew Rate, Bandwidth vs. Supply Voltage

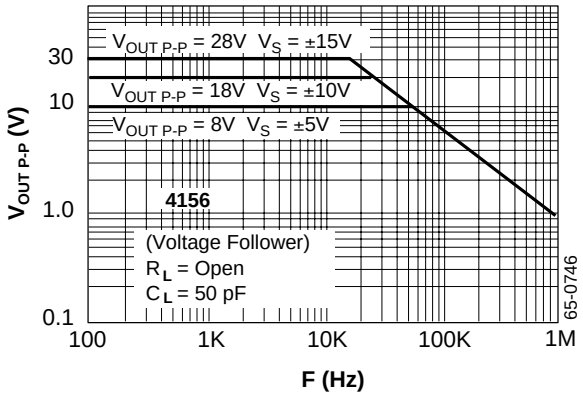


Figure 8. Output Voltage Swing vs. Frequency

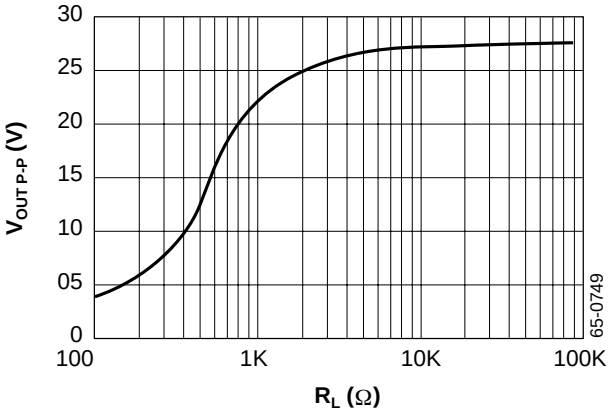


Figure 9. Output Voltage Swing vs. Load Resistance

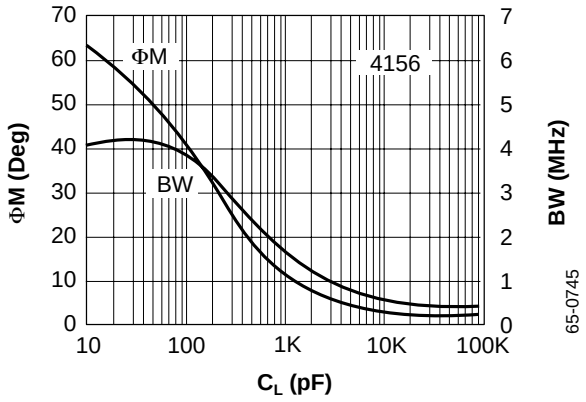


Figure 10. Small Signal Phase Margin, Unity Gain Bandwidth vs. Load Capacitance

Typical Performance Characteristics (continued)

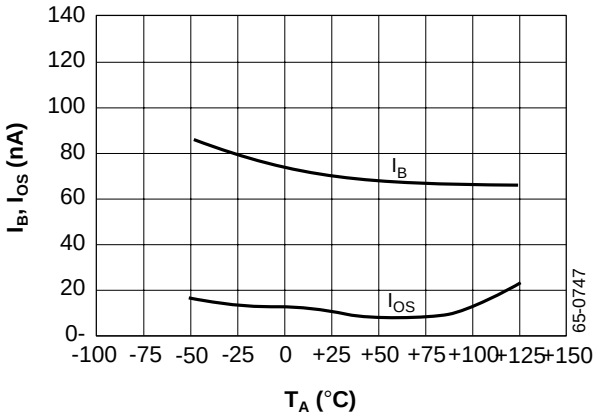


Figure 11. Input Bias, Offset Current vs. Temperature

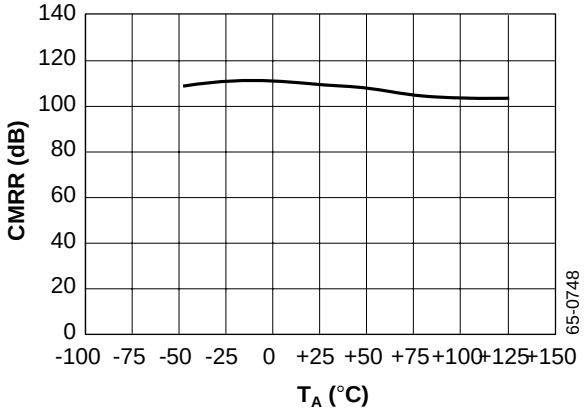


Figure 12. CMRR vs. Temperature

Applications

The RC4156 and RC4157 quad operational amplifiers can be used in almost any 741 application and will provide superior performance. The higher unity gain bandwidth and slew rate make it ideal for applications requiring good frequency response, such as active filter circuits, oscillators and audio amplifiers.

The following applications have been selected to illustrate the advantages of using the Fairchild Semiconductor RC4156 and RC4157 quad operational amplifiers.

Triangle and Square Wave Generator

The circuit of Figure 13 uses a positive feedback loop closed around a combined comparator and integrator. When power is applied the output of the comparator will switch to one of two states, to the maximum positive or maximum negative voltage. This applies a peak input signal to the integrator, and the integrator output will ramp either down or up, opposite of the input signal. When the integrator output (which is connected to the comparator input) reaches a threshold set by R1 and R2, the comparator will switch to the opposite polarity. This cycle will repeat endlessly, the integrator charging positive then negative, and the comparator switching in a square wave fashion.

The amplitude of V_2 is adjusted by varying R1. For best operation, it is recommended that R1 and V_R be set to obtain a triangle wave at V_2 with ±12V amplitude. This will then allow A3 and A4 to be used for independent adjustment of output-offset and amplitude over a wide range.

The triangle wave frequency is set by C0, R0, and the maximum output voltages of the comparator. A more symmetrical waveform can be generated by adding a back-to-back Zener diode pair as shown in Figure 14.

An asymmetric triangle wave is needed in some applications. Adding diodes as shown by the dashed lines is a way to vary the positive and negative slopes independently.

The frequency range can be very wide and the circuit will function well up to about 10 kHz. The square wave transition time at V_1 is less than 21 μS when using the RC4156.

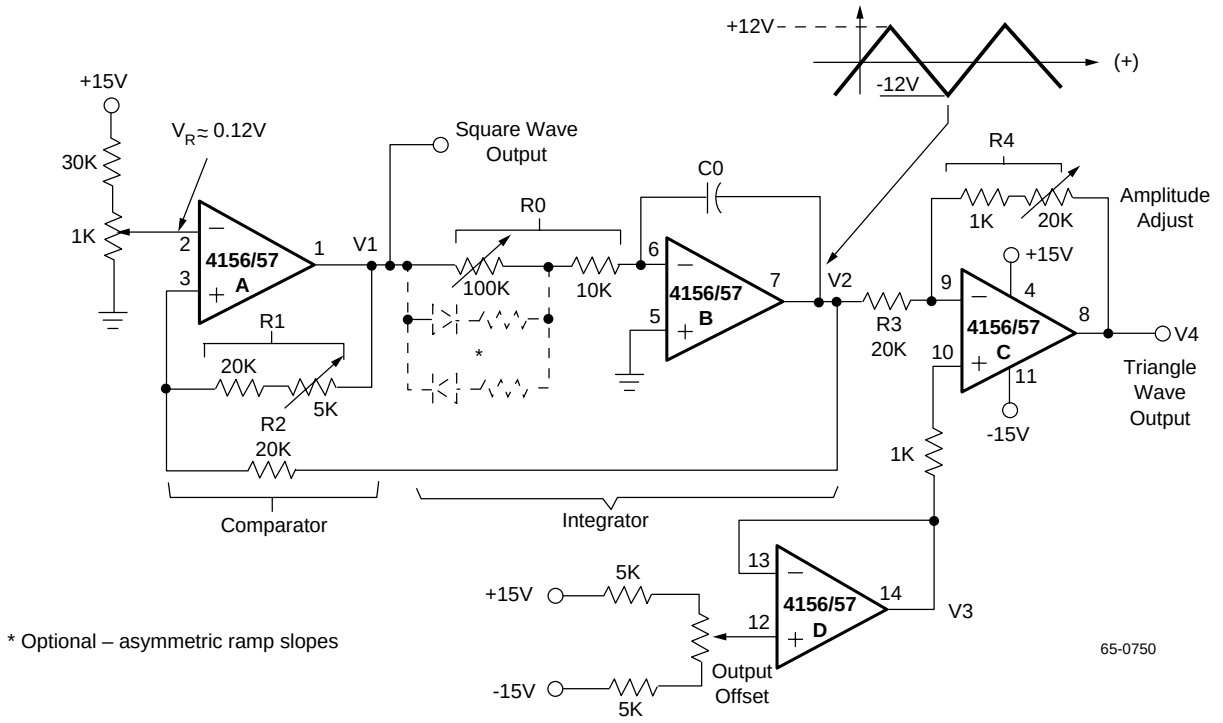


Figure 13. Triangle and Square Wave Generator

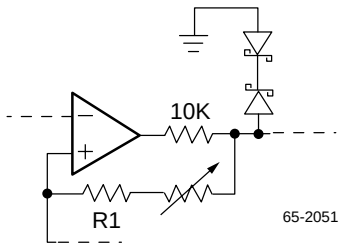


Figure 14. Triangle Generator—Symmetrical Output Option

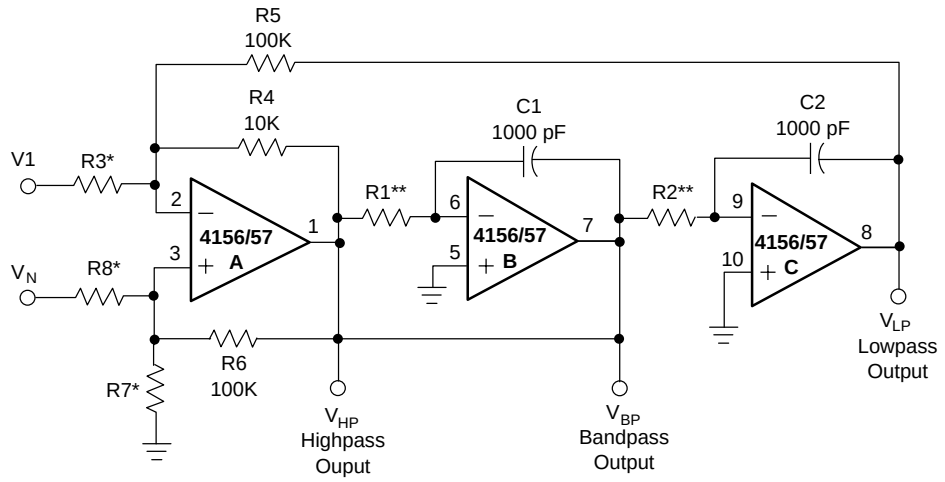
Active Filters

The introduction of low-cost quad op amps has had a strong impact on active filter design. The complex multiple-feedback, single op amp filter circuits have been rendered obsolete for most applications. State-variable active-filter circuits using three to four op amps per section offer many advantages over the single op amp circuits. They are relatively insensitive to the passive-component tolerances and variations. The Q, gain, and natural frequency can be independently adjusted. Hybrid construction is very practical because resistor and capacitor values are relatively low and the filter parameters are determined by resistance ratios rather than by single resistors. A generalized circuit diagram of the 2-pole state-variable active filter is shown in Figure 15. The particular input connections and component-values can be calculated for specific applications. An important feature of the state-variable filter is that it can be inverting or non-inverting and can simultaneously provide three outputs: lowpass, bandpass, and highpass. A notch filter can be realized by adding one summing op amp.

The RC4156 was designed and characterized for use in active filter circuits. Frequency response is fully specified with minimum values for unity-gain bandwidth, slew-rate, and full-power response. Maximum noise is specified.

Output swing is excellent with no distortion or clipping. The RC4156 provides full, undistorted response up to 20 kHz and is ideal for use in high-performance audio and telecommunication equipment.

In the state-variable filter circuit, one amplifier performs a summing function and the other two act as integrators. The choice of passive component values is arbitrary, but must be consistent with the amplifier operating range and input signal



* Input connections are chosen for inverting or non-inverting response. Values of R3,R7,R8 determine gain and Q.
** Values of R1 and R2 determine natural frequency.

65-0751

Figure 15. 2-Pole State-Variable Active Filter

characteristics. The values shown for C1, C2, R4, R5 and R6 are arbitrary. Pre-selecting their values will simplify the filter tuning procedures, but other values can be used if necessary.

The generalized transfer function for the state-variable active filter is:

$$T(s) = \frac{a_2 s^2 + a_1 s + a_0}{s^2 + b_1 s + b_0}$$

Filter response is conventionally described in terms of a natural frequency ω_0 in radians/sec, and Q, the quality of the complex pole pair. The filter parameters ω_0 and Q relate to the coefficients in T(s) as:

$$\omega_0 = \sqrt{b_0} \text{ and } Q = \frac{\omega_0}{b_0}$$

The input configuration determines the polarity (inverting or non-inverting), and the output selection determines the type of filter response (lowpass, bandpass, or highpass).

Notch and all-pass configurations can be implemented by adding another summing amplifier.

Bandpass filters are of particular importance in audio and telecommunication equipment. A design approach to bandpass filters will be shown as an example of the state-variable configuration.

Design Example Bandpass Filter

For the bandpass active filter (Figure 16) the input signal is applied through R3 to the inverting input of the summing amplifier and the output is taken from the first integrator (V_{BP}). The summing amplifier will maintain equal voltage at the inverting and non-inverting inputs (see Equation 1).

$$\frac{\frac{R3R5}{R3+R5}}{R4+\frac{R3R5}{R3+R5}} V_{HP}(s) + \frac{\frac{R3R4}{R3+R4}}{R5+\frac{R3R4}{R3+R4}} V_{LP}(s) + \frac{\frac{R4R5}{R4+R5}}{R3+\frac{R4R5}{R4+R5}} V_{IN}(s) + \frac{R7}{R6+R7} V_{BP}(s)$$

Equation 1.

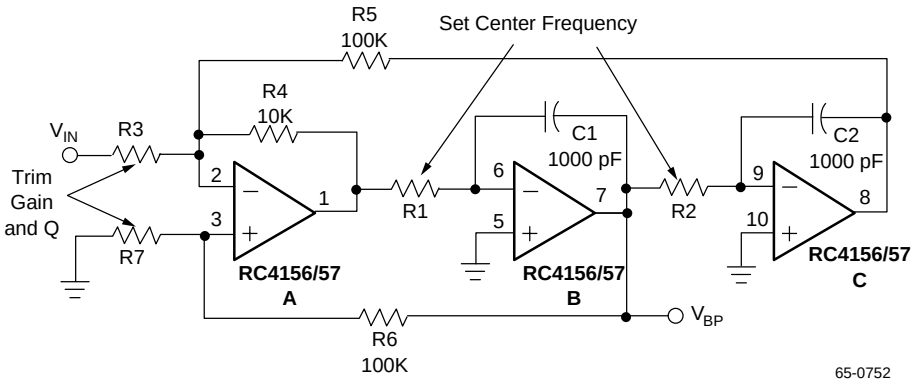


Figure 16. Bandpass Active Filter

These equations can be combined to obtain the transfer function:

$$V_{BP}(s) = -\frac{1}{R1C1S}V_{HP}(s) \quad \text{and} \quad V_{LP}(s) = -\frac{1}{R2C2S}V_{BP}(s)$$

$$\frac{V_{BP}(s)}{V_{IN}(s)} = \frac{\frac{R4}{R3}\cdot\frac{1}{R1C1}S}{S^2 + \frac{R7}{R6+R7}\left(1+\frac{R4}{R5}+\frac{R4}{R3}\right)\left(\frac{1}{R1C1}\right)S + \left(\frac{R4}{R5}\right)\left(\frac{1}{R1C1R2C2}\right)}$$

Defining 1/R1C1 as ω1, 1/R2C2 as ω2, and substituting in the assigned values for R4, R5, and R6, then the transfer function simplifies to:

$$\frac{V_{BP}(s)}{V_{IN}(s)} = \frac{\frac{10^4}{R3}\cdot\omega_1 s}{S^2 + \left[\frac{1.1+\frac{10^4}{R3}}{1+\frac{10^5}{R7}}\right]\omega_1 s + \frac{1}{\omega_1\omega_2}}$$

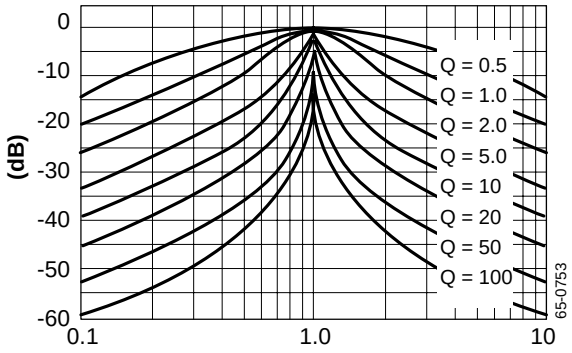
This is now in a convenient form to look at the center-frequency ω_0 and filter Q.

$$\omega_0 = \sqrt{0.1\omega_1\omega_2}$$

$$\omega_0 = 10^{-9}\sqrt{0.1R1R2} \quad \text{and}$$

$$Q = \left[\frac{1+\frac{10^5}{R7}}{1.1+\frac{10^4}{R3}}\right]\omega_0$$

The frequency responses for various values of Q are shown in Figure 17.



$$\frac{\omega}{\omega_0}$$

$$\frac{V_{BP}}{V_{IN}} = \frac{\frac{\omega}{\omega_0}\,\frac{1}{Q}}{\sqrt{\left[1-\left(\frac{\omega}{\omega_0}\right)^2\right]^2 + \left(\frac{1}{Q}\,\frac{\omega}{\omega_0}\right)^2}}$$

Figure 17. Bandpass Transfer Characteristics Normalized for Unity Gain and Frequency

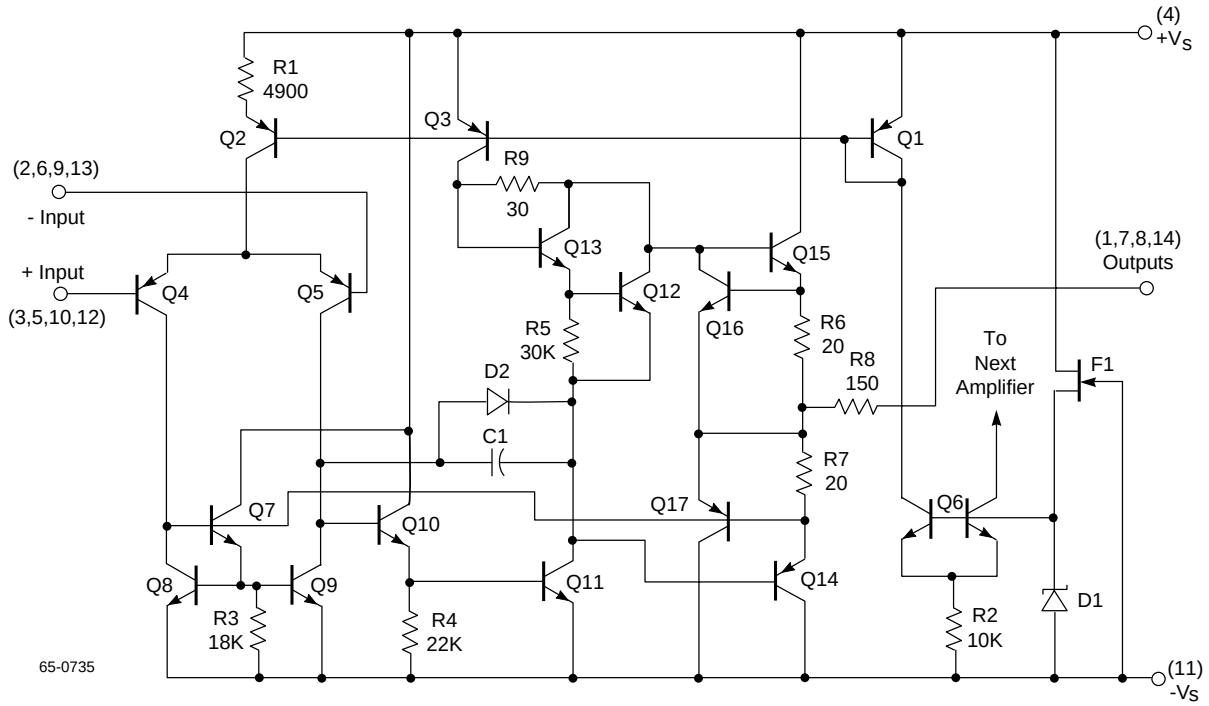
These equations suggest a tuning sequence where ω is first trimmed via R1 or R2, then Q is trimmed by varying R7 and/or R3. An important advantage of the state-variable bandpass filter is that Q can be varied without affecting center frequency ω_0.

This analysis has assumed ideal op amps operating within their linear range, which is a valid design approach for a reasonable range of ω_0 and Q. At extremes of ω_0 and at high values of Q, the op amp parameters become significant. A rigorous analysis is very complex, but some factors are particularly important in designing active filters.

1. The passive component values should be chosen such that all op amps are operating within their linear region for the anticipated range of input signals. Slew rate, output current rating, and common-mode input range must be considered. For the integrators, the current through the feedback capacitor (I = C dV/dt) should be included in the output current computations.
2. From the equation for Q, it should seem that infinite Q could be obtained by making R7 zero. But as R7 is made small, the Q becomes limited by the op amp gain at the frequency of interest. The effective closed-loop gain is being increased directly as R7 is made smaller, and the ratio of open-loop gain to closed-loop gain is becoming less. The gain and phase error of the filter at high Q is very dependent on the op amp open-loop gain at w_0.
3. The attenuation at extremes of frequency is limited by the op amp gain and unity-gain bandwidth. For integrators, the finite open-loop op amp gain limits the accuracy at the low-end. The open-loop roll-off of gain limits the filter attenuation at high frequency.

The RC4156 quad operational amplifier has much better frequency response than a conventional 741 circuit and is ideal for active filter use. Natural frequencies of up to 10 kHz are readily achieved and up to 20 kHz is practical for some configurations. Q can range up to 50 with very good accuracy and up to 500 with reasonable response. The extra gain of the RC4156 at high frequencies gives the quad op amp an extra margin of performance in active-filter circuits.

Schematic Diagram (1/4 shown)



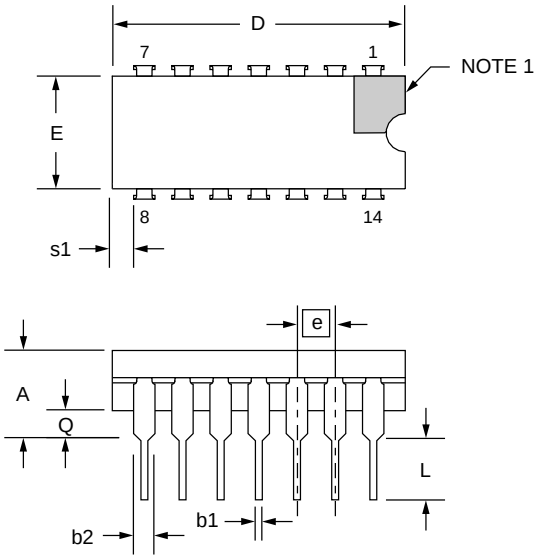
Mechanical Dimensions

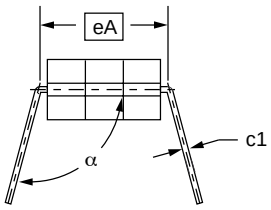
14-Lead Ceramic DIP Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2
c1	.008	.015	.20	.38	8
D	—	.785	—	19.94	4
E	.220	.310	5.59	7.87	4
e	.100 BSC		2.54 BSC		5, 9
eA	.300 BSC		7.62 BSC		7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 7, 8 and 14 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 14.
6. Applies to all four corners (leads number 1, 7, 8, and 14).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Twelve spaces.





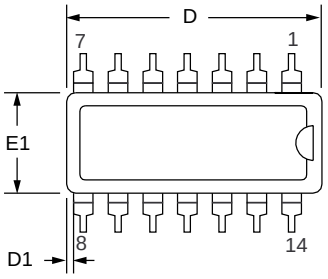
Mechanical Dimensions (continued)

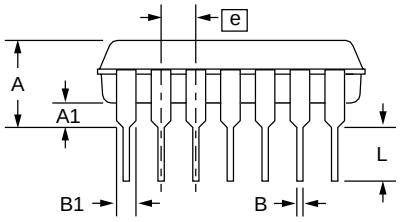
14-Lead Plastic DIP Package

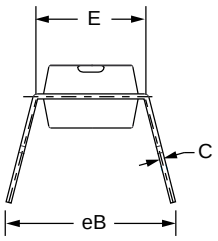
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	.725	.795	18.42	20.19	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.200	2.92	5.08	
N	14		14		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are shown for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.







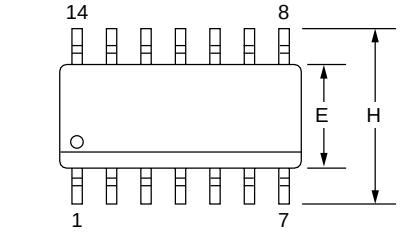
Mechanical Dimensions (continued)

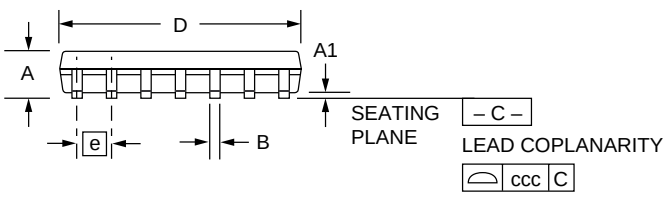
14-Lead SOIC Package

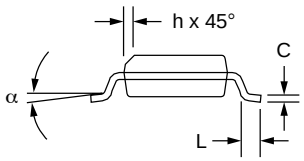
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.19	0.25	5
D	.336	.345	8.54	8.76	2
E	.150	.158	3.81	4.01	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	14		14		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
RC4156N	0° to 70°C	Commercial	14 Pin Plastic DIP	RC4156N
RC4157N	0° to 70°C	Commercial	14 Pin Plastic DIP	RC4157N
RC4156M	0° to 70°C	Commercial	14 Pin Wide SOIC	RC4156M
RC4157M	0° to 70°C	Commercial	14 Pin Wide SOIC	RC4157M
RM4156D	-55°C to +125°C	Commercial	14 Pin Ceramic DIP	RM4156DM
RM4156D/883B	-55°C to +125°C	Military	14 Pin Ceramic DIP	RM4156DMB

RC4190

Micropower Switching Regulator

Features

- High efficiency – 85% typical
- Low quiescent current – 215 μA
- Adjustable output – 1.3V to 30V
- High switch current – 200 mA
- Bandgap reference – 1.31V
- Accurate oscillator frequency – ±10%
- Remote shutdown capability
- Low battery detection circuitry
- Low component count
- 8-lead packages including small outline (SO-8)

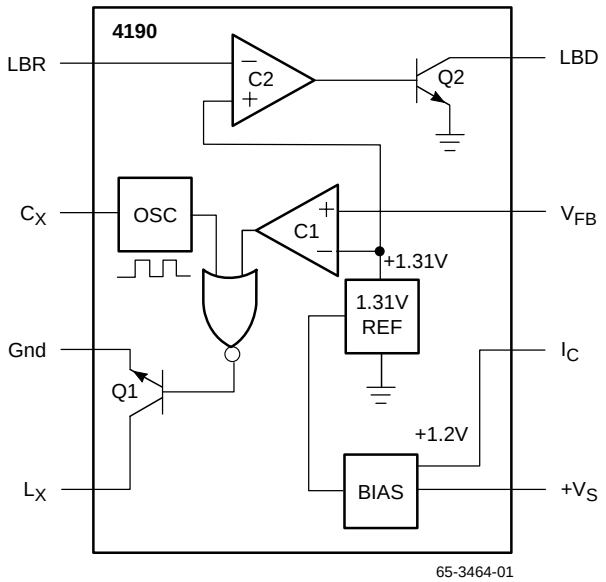
Description

The RC4190 monolithic IC is a low power switch mode regulator intended for miniature power supply applications. This DC-to-DC converter IC provides all of the active components needed to create supplies for micropower circuits (load power up to 400 mW, or up to 10W with an external power transistor). Contained internally are an oscillator, switch, reference, comparator, and logic, plus a discharged battery detection circuit.

Application areas include on-card circuits where a non-standard voltage supply is needed, or in battery operated instruments where an RC4190 can be used to extend battery lifetime.

These regulators can achieve up to 85% efficiency in most applications while operating over a wide supply voltage range, 2.2V to 30V, at a very low quiescent current drain of 215 μA.

Block Diagram



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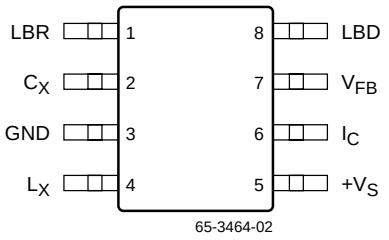
The standard application circuit requires just seven external components for step-up operation: an inductor, a steering diode, three resistors, a low value timing capacitor, and an electrolytic filter capacitor. The combination of simple application circuit, low supply current, and small package make the RC4190 adaptable to a wide range of miniature power supply applications.

The RC4190 is most suited for single ended step-up ($V_{OUT} > V_{IN}$) circuits because the NPN internal switch transistor is referenced to ground. It is complemented by another Fairchild Semiconductor micropower switching regulator, the RC4391, which is dedicated to step-down ($V_{OUT} < V_{IN}$) and inverting $V_{OUT} = -V_{IN}$) applications. Between the two devices the ability to create all three basic switching regulator configurations is assured. Refer to the RC4391 data sheet for step-down and inverting applications.

With some optional external components the application circuit can be designed to signal a display when the battery has decayed below a predetermined level, or designed to signal a display at one level and then shut itself off after the battery decays to a second level. See the applications section for these and other unique circuits.

The RC4190 micropower switching regulator series consists of three devices, each with slightly different specifications. The RM4190 has a 1.5% maximum output voltage tolerance, 0.2% maximum line regulation, and operation to 30V. The RC4190 has a 5.0% maximum output voltage tolerance, 0.5% maximum line regulation, and operation to 24V. Other specifications are identical. Each type is available in plastic and ceramic DIPs, or SO-8 packages.

Pin Assignments



Pin Definitions

Pin Name	Pin Number	Pin Function Description
LBR	1	Low Battery (Set) Resistor
C_X	2	Timing Capacitor
Gnd	3	Ground
L_X	4	External Inductor
$+V_S$	5	Positive Supply Voltage
I_C	6	Reference Set Current
V_{FB}	7	Feedback Voltage
LBD	8	Low Battery Detector Output

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min	Typ	Max	Units
Supply Voltage (Without External Transistor)	RM4190			30	V
	RC4190			24	V
$P_D T_A$ < 50°C	SOIC			300	mW
	PDIP			468	mW
	CerDIP			833	mW
Operating Temperature	RM4190	-55		125	°C
	RC4190	0		70	°C
Storage Temperature		-65		150	°C
Junction Temperature	SOIC, PDIP		125		°C
	CerDIP		175		°C
Switch Current	Peak			375	mA
For T_A > 50°C Derate at	SOIC		4.17		mW/°C
	PDIP		6.25		mW/°C
	CerDIP		8.33		mW/°C

Note:

1. Functional operation under any of these conditions is NOT implied.

Operating Conditions

Parameter			Min	Typ	Max	Units
θ_{JC}	Thermal resistance	CerDIP		45		°C/W
θ_{JA}	Thermal resistance	SOIC		200		°C/W
		PDIP		160		°C/W
		CerDIP		120		°C/W

Electrical Characteristics

($+V_S$ = +6.0V, I_C = 5.0 μA over the full operating temperature range unless otherwise noted.)

Symbol	Parameters	Conditions	RM4190			RC4190			Units
			Min	Typ	Max	Min	Typ	Max	
$+V_S$	Supply Voltage		2.6		30	2.6		24	V
V_{REF}	Reference Voltage (Internal)		1.25	1.31	1.37	1.20	1.31	1.42	V
I_{SY}	Supply Current	Measure at Pin 5 $I_4 = 0$		235	350		235	350	μA
	Line Regulation	$0.5\ V_{OUT} < V_S < V_{OUT}$		0.2	0.5		0.5	1.0	% V_O
L_I	Load Regulation	$V_S = 0.5\ V_{OUT}$ P_L = 150 mW		0.5	1.0		0.5	1.0	% V_O
I_C	Reference Set Current		1.0	5.0	50	1.0	5.0	50	μA
I_{CO}	Switch Leakage Current	V_4 = 24V (RC4190) 30V (RM4190)			30			30	μA
I_{SO}	Supply Current (Disabled)	$V_C \leq$ 200 mV			30			30	μA
I_{LBD}	Low Battery Output Current	V_8 = 0.4V, V_1 = 1.1V	500	1200		500	1200		μA
	Oscillator Frequency Temperature Drift			±200			±200		ppm/°C

Electrical Characteristics

(+V_S = +6.0V, I_C = 5.0 μA, and T_A = +25°C unless otherwise noted.)

Symbol	Parameters	Conditions	RM4190			RC4190			Units
			Min	Typ	Max	Min	Typ	Max	
$+V_S$	Supply Voltage		2.2		30	2.2		24	V
V_{REF}	Reference Voltage (Internal)		1.29	1.31	1.33	1.24	1.31	1.38	V
I_{SW}	Switch Current	V_4 = 400 mV	100	200		100	200		mA
I_{SY}	Supply Current	Measure at Pin 5 I_4 = 0		215	300		215	300	μA
ef	Efficiency			85			85		%
	Line Regulation	0.5 V_{OUT} < V_S < V_{OUT}		0.04	0.2		0.04	0.5	% V_O
L_I	Load Regulation	V_S = +0.5 V_{OUT} P_L = 150 mW		0.2	0.5		0.2	0.5	% V_O
F_O	Operating Frequency Range		0.1	25	75	0.1	25	75	kHz
I_C	Reference Set Current		1.0	5.0	50	1.0	5.0	50	μA
I_{CO}	Switch Leakage Current	V_4 = 24V (RC4190) 30V (RM4190, RC4190A)		0.01	5.0		0.01	5.0	μA
I_{SO}	Supply Current (Disabled)	V_C ≤ 200 mV		0.1	5.0		0.1	5.0	μA
I_1	Low Battery Bias Current	V_1 = 1.2V		0.7			0.7		μA
I_{CX}	Capacitor Charging Current			8.6			8.6		μA
	Oscillator Frequency Tolerance			±10			±10		%
$+V_{THX}$	Capacitor Threshold Voltage +			1.4			1.4		V
$-V_{THX}$	Capacitor Threshold Voltage –			0.5			0.5		V
I_{FB}	Feedback Input Current	V_7 = 1.3V		0.1			0.1		μA
I_{LBD}	Low Battery Output Current	V_8 = 0.4V, V_1 = 1.1V	500	1500		500	1500		μA

Typical Performance Characteristics

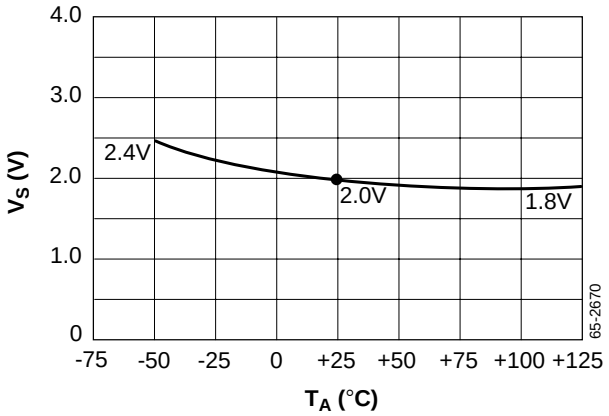


Figure 1. Minimum Supply Voltage vs. Temperature

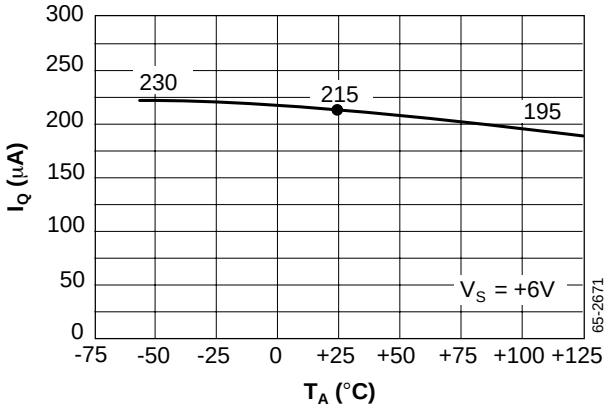


Figure 2. Quiescent Current vs. Temperature

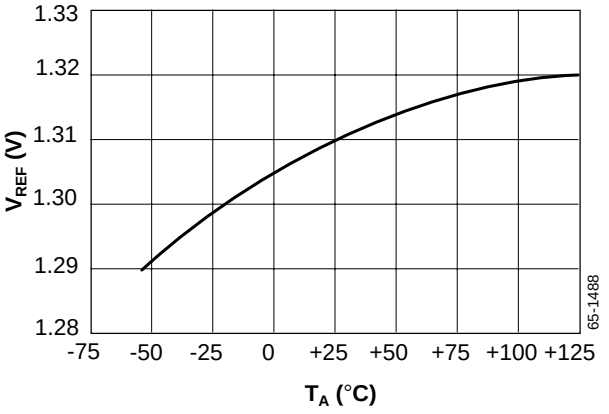


Figure 3. Reference Voltage vs. Temperature

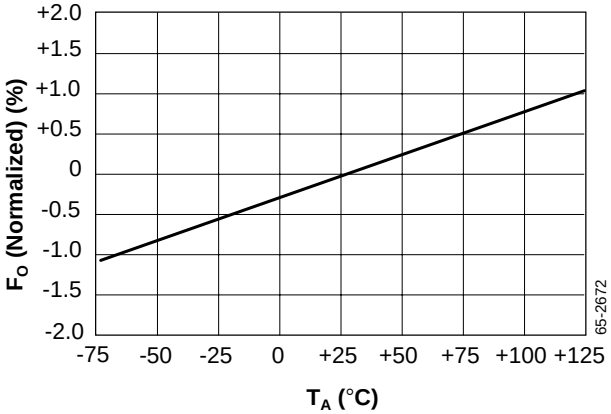


Figure 4. Oscillator Frequency vs. Temperature

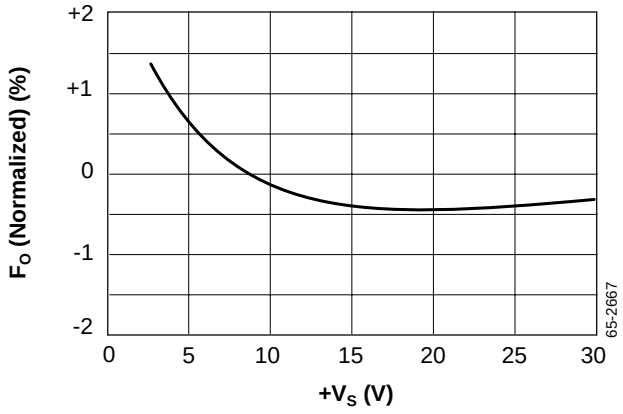


Figure 5. Minimum Supply Voltage vs. Temperature

Principles of Operation

Simple Step-Up Converter

The most common application, the step-up regulator, is derived from a simple step-up ($V_{OUT} > V_{BAT}$) DC-to-EC Converter (Figure 6).

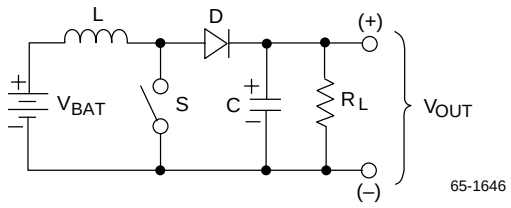


Figure 6. Simple Set-Up

When switch S is closed, the battery voltage is applied across the inductor L. Charging current flows through the inductor, building up a magnetic field, increasing as the switch is held closed. While the switch is closed, the diode D is reverse biased (open circuit) and current is supplied to the load by the capacitor C. Until the switch is opened, the inductor current will increase linearly to a maximum value determined by the battery voltage, inductor value, and the amount of time the switch is held closed ($I_{MAX} = V_{BAT}/L \times T_{ON}$). When the switch is opened, the magnetic field collapses, and the energy stored in the magnetic field is converted into a discharge current which flows through the inductor in the same direction as the charging current. Because there is no path for current to flow through the switch, the current must flow through the switch, the current must flow through the diode to supply the load and charge the output capacitor.

If the switch is opened and closed repeatedly, at a rate much greater than the time constant of the output RC, then a constant dc voltage will be produced at the output.

An output voltage higher than the input voltage is possible because of the high voltage produced by a rapid change of current in the inductor. When the switch is opened, the inductor voltage will instantly rise high enough to forward bias the diode, to $V_{OUT} + V_D$.

In the complete RC4190 regulator, a feedback control system adjusts the on time of the switch, controlling the level of inductor current, so that the average inductor discharge current equals the load current, thus regulating the output voltage.

Complete Step-Up Regulator

A complete schematic of the minimum step-up application is shown in Figure 7. The ideal switch in the DC-to-DC Converter diagram is replaced by an open collector NPN transistor Q1. C_F functions as the output filter capacitor, and D1 and L_X replace D and L.

When power is first applied, the current in R1 supplies bias current to pin 6 (I_C). This current is stabilized by a unity gain current source amplifier and then used as bias current for the 1.31V bandgap reference. A very stable bias current generated by the bandgap is mirrored and used to bias the remainder of the chip. At the same time the RC4190 is starting up, current will flow through the inductor and the diode to charge the output capacitor to $V_{BAT} - V_D$.

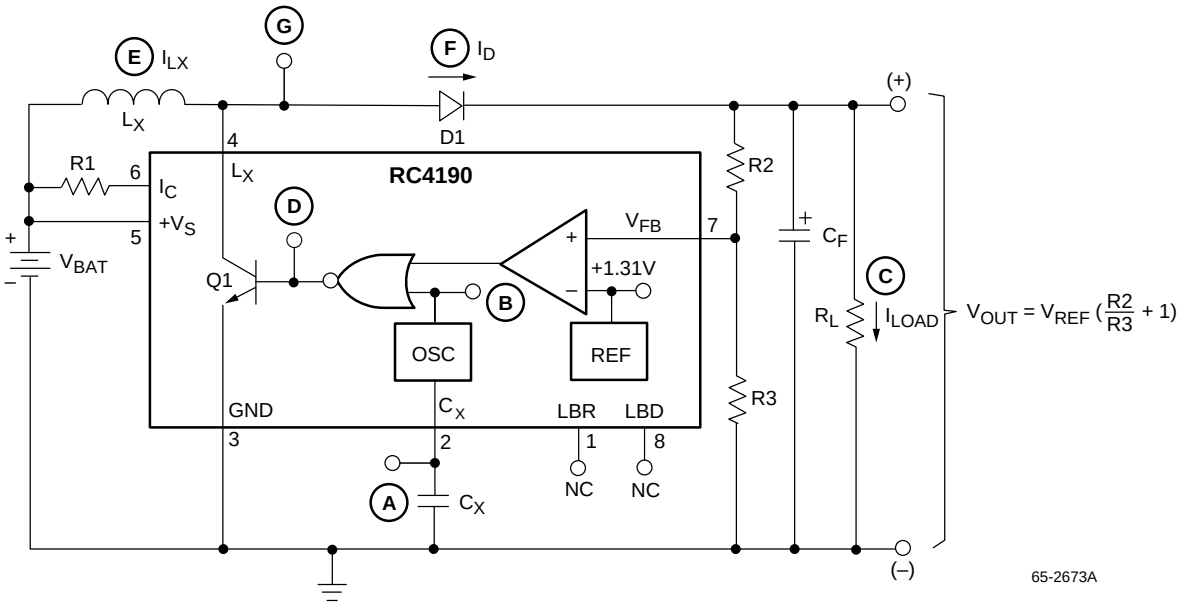


Figure 7. Complete Step-Up Regulator

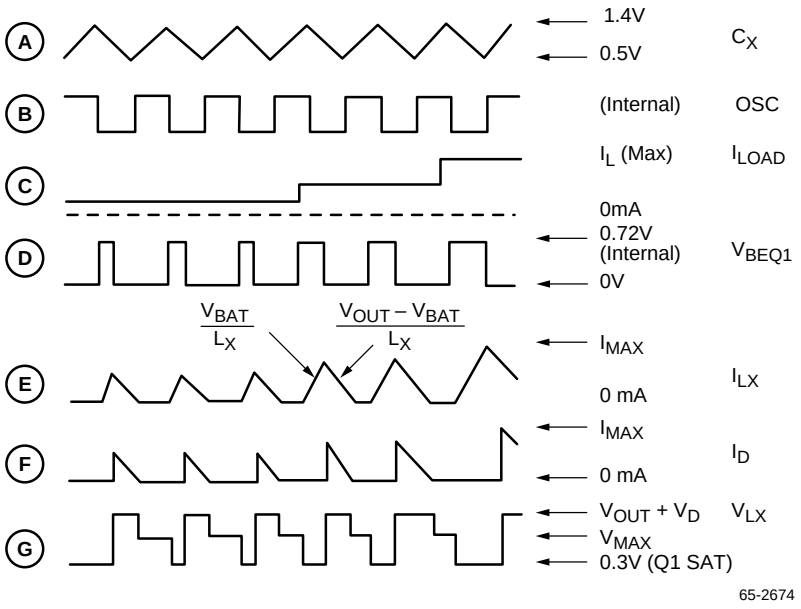


Figure 8. Step-Up Regulator Waveforms

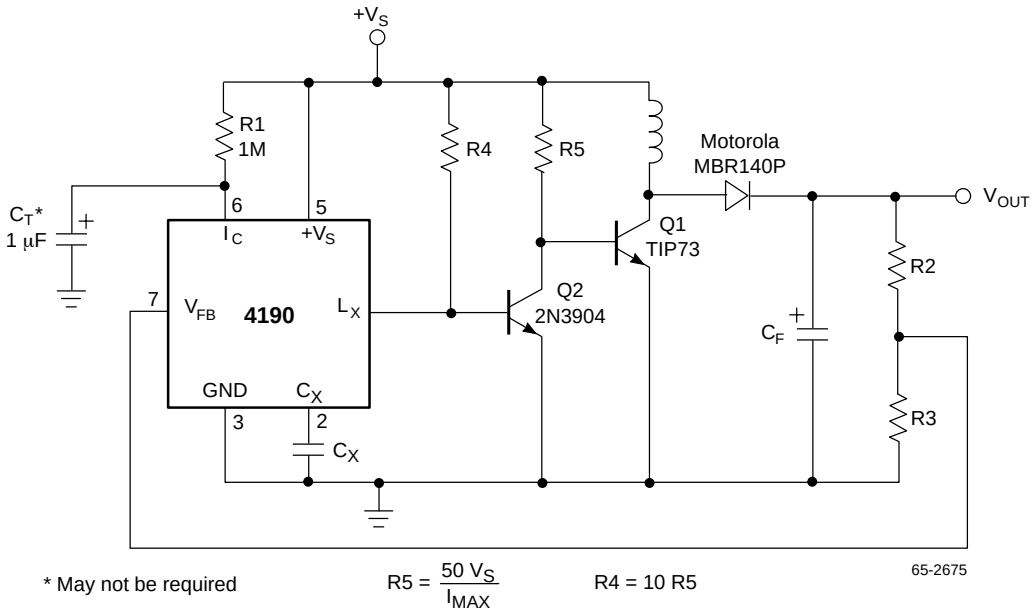


Figure 9. High Power Step-Up Regulator
(With the addition of a power transistor (TIP73) and a few components, the 4190 can accomodate load power up to 10W.)

At this point, the feedback (pin 7) senses that the output voltage is too low, by comparing a division of the output voltage (set by the ratio of R2 to R3) to the +1.31V reference. If the output voltage is too low then the comparator output changes to a logical zero. The NOR gate then effectively ANDs the oscillator square wave with the comparator signal; if the comparator output is zero AND the oscillator output is low, then the NOR gate output is high and the switch transistor will be forced on. When the oscillator goes high again, the NOR gate output goes low and the switch transistor will turn off. This turning on and off of the switch transistor performs the same function that opening and closing the switch in the simple DC-to-DC Converter does; i.e., it stores energy in the inductor during the on time and releases it into the capacitor during the off time.

The comparator will continue to allow the oscillator to turn the switch on and off until enough charge has been delivered to the capacitor to raise the feedback voltage above 1.31V.

Thereafter, this feedback system will vary the duration of the on time in response to changes in load current or battery

voltage (see Figure 8). If the load current increases (waveform C), then the transistor will remain on (waveform D) for a longer portion of the oscillator cycle (waveform B), thus allowing the inductor current (waveform E) to build up to a higher peak value. The duty cycle of the switch transistor varies in response to changes in load and time.

The inductor value and oscillator frequency must be carefully tailored to the battery voltage, output current, and ripple requirements of the application (refer to the Design Equations Section). If the inductor value is too high or the oscillator frequency is too high, then the inductor current will never reach a value high enough to meet the load current drain and the output voltage will collapse. If the inductor value is too low or the oscillator frequency too low, then the inductor current will build up too high, causing excessive output voltage ripple, or over stressing of the switch transistor, or possibly saturating the inductor.

Simple Step-Down Converter

Figure 10 shows a step-down DC-to-DC Converter ($V_{OUT} \leq V_{BAT}$) with no feedback control.

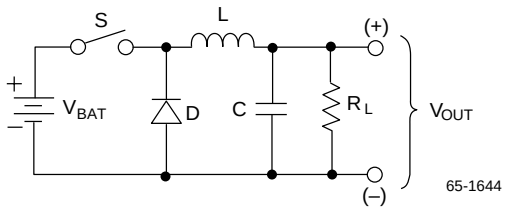


Figure 10. Simple Step-Down Converter

When S is closed, the battery voltage minus the output voltage is applied across the inductor. All of the inductor current will flow into the load until the inductor current exceeds the load current. The excess current will then charge the capacitor and the output voltage will rise. When S is opened, the voltage applied across the inductor will discharge into the load. As in the step-up case, the average inductor current equals the load current. The maximum inductor current I_{MAX} will equal $(V_{BAT} - V_{OUT})/L$ times the maximum on time of the switch transistor (T_{ON}). Current flows to the load during both half cycles of the oscillator.

Complete Step-Down Regulator

Most step-down applications are better served by the RC4391 step-down and inverting switching regulator (refer to the RC4391 data sheet). However, there is a range of load power for which the RC4190 has an advantage over the RC4391 in step-down applications. From approximately 500 mW to 2W of load power, the RC4190 step-down circuit of Figure 6 offers a lower component count and simpler circuit than the comparable RC4391 circuit, particularly when stepping down a voltage greater than 30V.

Since the switch transistor in the RC4190 is in parallel with the load, a method must be used to convert it to a series connection for step-down applications. The circuit of Figure 11 accomplishes this. The 2N2907 replaces S of Figure 10, and R6 and R7 are added to provide the base drive to the 2N2907 in the correct polarity to operate the circuit properly.

Greater Than 30V Step-Down Regulator

Adding a zener diode in series with the base of the 2N2907 allows the battery voltage to increase by the value of the zener, with only a slight decrease in efficiency. As an example, if a 24V zener is used, the maximum battery voltage can go to 48V[2] when using a RC4190. Refer to Figure 12.

Notes:

1. The addition of the zener diode will not alter the maximum change of supply. With a 24V zener, the circuit will stop operating when the battery voltage drops below 24V + 2.2V = 26.2V.
2. Maximum battery voltage is 54V when using RM4190 (30V + 24V).

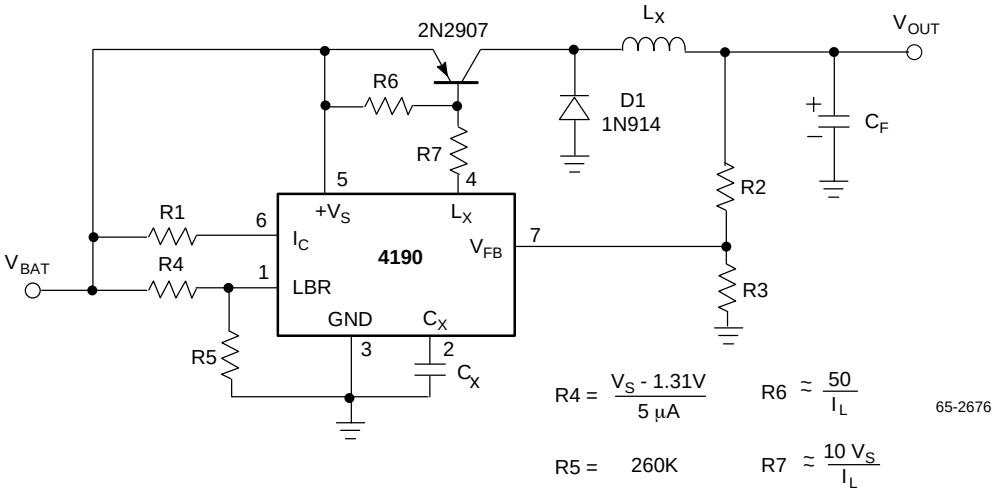


Figure 11. Complete Step-Down Regulator

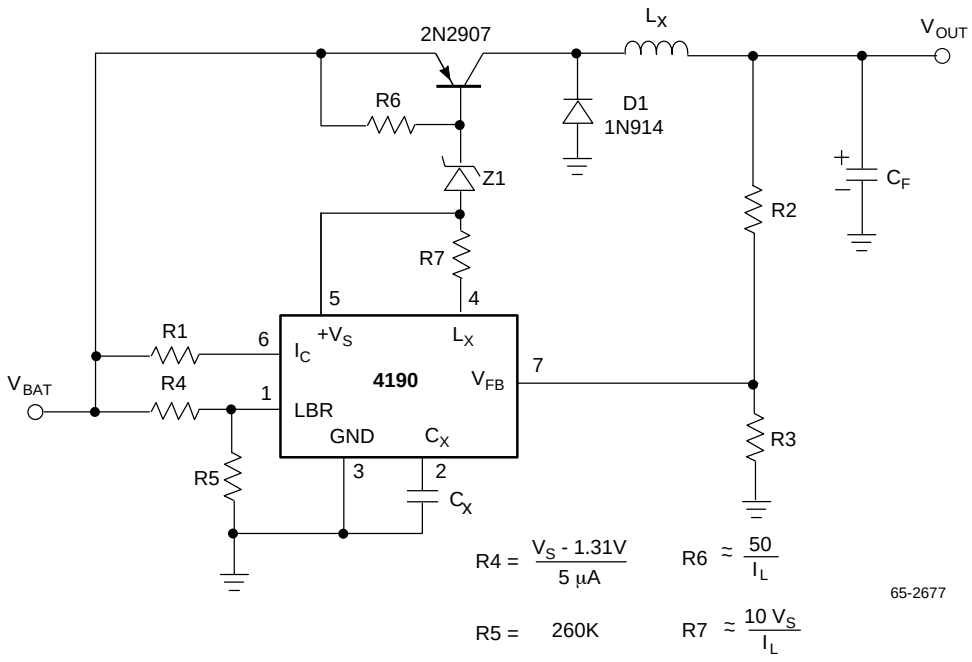


Figure 12. Step-Down Regulator Greater Than 30V

Design Equations

The inductor value and timing capacitor (C_X) value must be carefully tailored to the input voltage, input voltage range, output voltage, and load current requirements of the application. The key to the problem is to select the correct inductor value for a given oscillator frequency, such that the inductor current rises to a high enough peak value (I_{MAX}) to meet the average load current drain. The selection of this inductor value must take into account the variation of oscillator frequency from unit to unit and the drift of frequency over temperature. Use ±20% as a maximum change from the nominal oscillator frequency.

The worst-case conditions for calculating ability to supply load current are found at the minimum supply voltage; use $+V_S$ (min) to calculate the inductor value. Worst-case conditions for ripple are at $+V_S$ (max).

The value of the timing capacitor is set according to the following equation:

$$f_O(Hz) = \frac{2.4 \times 10^6}{C_X(pF)}$$

The squarewave output of the oscillator is internal and cannot be directly measured, but is equal in frequency to the triangle waveform measurable at pin 4. The switch transistor is normally on when the triangle waveform is ramping up and off when ramping down. Capacitor selection depends on the application; higher operating frequencies will reduce the output voltage ripple and will allow the use of an inductor with a physically smaller inductor core, but excessively high frequencies will reduce load driving capability and efficiency.

Find a value for the start-up resistor R1:

$$R1 = \frac{V_S - 1.2V}{5\mu A}$$

Find a value for the feedback resistors R2 and R3:

$$R2 = \frac{V_{OUT} - 1.31V}{I_A}$$

$$R3 = \frac{1.31V}{I_A}$$

Where I_A is the feedback divider current (recommended value is between 50 μA and 100 μA).

Step-Up Design Procedure

1. Select an operating frequency and timing capacitor as shown above (10 kHz to 40kHz is typical).

2. Find the maximum on time (add 5 μS for the turn-off base recombination delay of Q1):

   $$T_{ON} = \frac{1}{2F_O} + 5\mu s$$

3. Calculate the peak inductor current I_{MAX} (if this value is greater than 375 mA, then an external power transistor must be used in place of Q1):

   $$I_{MAX} = \left(\frac{V_{OUT} + V_D - V_S}{(F_O)T_{ON}[V_S - V_{SW}]}\right) 2I_L$$

   where: V_S = supply voltage
   V_D = diode forward voltage
   I_L = dc load current
   V_{SW} = saturation voltage of Q1 (typ 0.5V)

4. Find an inductance value for L_X:

$$L_X(\text{Henries}) = \left(\frac{V_S - V_{SW}}{I_{MAX}}\right) T_{ON}$$

5. The inductor chosen must exhibit approximately this value at a current level equal to I_{MAX}.

6. Calculate a value for the output filter capacitor:

$$C_F(\mu F) = \frac{T_{ON}\left(\frac{V_S I_{MAX}}{V_{OUT}} + I_L\right)}{V_R}$$

where V_R = ripple voltage (peak)

Step-Down Design Procedure

1. Select an operating frequency.

2. Determine the maximum on time (T_{ON}) as in the step-up design procedure.

3. Calculate I_{MAX}:

$$I_{MAX} = \frac{2I_L}{(F_O)(T_{ON})\left(\frac{V_S - V_{OUT}}{V_{OUT} - V_D}\right) + 1}$$

4. Calculate L_X:

$$L_X = \left(\frac{V_S - V_{OUT}}{I_{MAX}}\right)(T_{ON})$$

5. Calculate a value for the output filter capacitor:

$$C_F(\mu F) = \frac{T_{ON}\left(\frac{(V_S - V_{OUT})I_{MAX}}{V_{OUT}} + I_L\right)}{V_R}$$

Alternate Design Procedure

The design equations above will not work for the certain input/output voltage ratios, and for these circuits another method of defining component values must be used. If the slope of the current discharge waveform is much less than the slope of the current charging waveform, then the inductor current will become continuous (never discharging completely), and the equations will become extremely complex. So, if the voltage applied across the inductor during the charge time is greater than during the discharge time, used the design procedure below. For example, a step-down circuit with 20V input and 5V output will have approximately 15V across the inductor when charging, and approximately 5V when discharging. So in this example, the inductor current will be continuous and the alternate procedure will be necessary.

1. Select an operating frequency (a value between 10 kHz and 40 kHz is typical).

2. Build the circuit and apply the worst case conditions to it, i.e., the lowest battery voltage and the highest load current at the desired output voltage.

3. Adjust the inductor value down until the desired output voltage is achieved, then go a little lower (approximately 20%) to cover manufacturing tolerances.

4. Check the output voltage with an oscilloscope for ripply, at high supply voltages, at voltages as high as are expected. Also check for efficiency by monitoring supply and output voltages and currents [eff = (V_{OUT})(I_{OUT})/(+V_S)(I_{SY}) x 100%$].

5. If the efficiency is poor, go back to (1) and start over. If the ripple is excessive, then increase the output filter capacitor value or start over.

Compensation

When large values (>50 kΩ) are used for the voltage setting resistors, R2 and R3 of Figure 7, stray capacitance at the V_{FB} input can add a lag to the feedback response, destabilizing the regulator, increasing low frequency ripple, and lowering efficiency. This can often be avoided by minimizing the stray capacitance at the V_{FB} node. It can also be remedied by adding a lead compensation capacitor of 100 pF to 10 nF in parallel with R2 in Figure 7.

Inductors

Efficiency and load regulation will improve if a quality high Q inductor is used. A ferrite pot core is recommended; the wind-yourself type with an air gap adjustable by washers or spacers is very useful for breadboarding prototypes. Care must be taken to choose a permeable enough core to handle the magnetic flux produced at I_{MAX}; if the core saturates, then efficiency and output current capability are severely degraded and excessive current will flow though the switch transistor. A pot core inductor design section is provided later in this datasheet.

An isolated AC current probe for an oscilloscope (example: Tektronix P6042) is an excellent tool for saturation problems; with it the inductor current can be monitored for nonlinearity at the peaks (a sign of saturation).

Low Battery Detector

An open collector signal transistor Q2 with comparator C2 provides the designer with a method of signaling a display or computer whenever the battery voltage falls below a programmed level (see Figure 8). This level is determined by the +1.3V reference level and by the selection of two external resistors according to the equation:

$$V_{TH} = V_{REF}\left(\frac{R4}{R5} + 1\right)$$

Where V_{TH} = Threshold Voltage for Detection

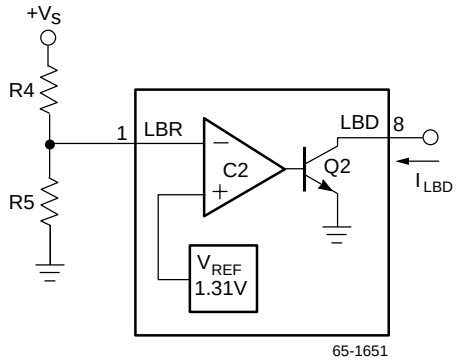


Figure 13. Low Battery Detector

When the battery voltage drops below this threshold Q2 will turn on and sink over 1500 μA typically. The low battery detector circuitry may also be used for other, less conventional applications (see Figures 19 and 20).

Automatic Shutdown

The bias control current for the reference is externally set by a resistor from the I_C pin to the battery. This current can vary from 1.0 μA to 50 μA without affecting the operation of the I_C. Interrupting this current will disable the entire circuit, causing the output voltage to go to 0V for step-down applications, and reducing the supply current to less than 1.0 μA.

Automatic shutdown of the RC4190 can be achieved using the circuit of Figure 14.

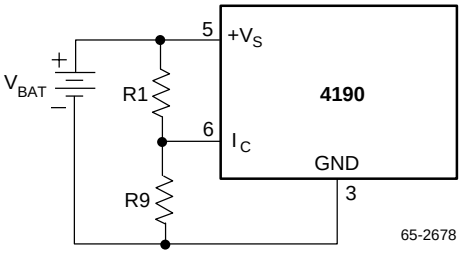


Figure 14. Automatic Shutdown

A resistor is placed from the I_C pin to ground, creating a voltage divider. When the voltage at the I_C pin is less than 1.2V, the RC4190 will begin to turn off. This scheme should only be used in limited temperature range applications since the "turn off" voltage at the I_C pin has a temperature coefficient of -4.0 mV/°C. At 25°C, typically 250 nA is the minimum current required by the I_C pin to sustain operation. A 5.0 μA voltage divider works well taking into account the sustaining current of 250 nA and a threshold voltage of 0.4V at turn off. As an example, if 3.0V is to be the turn off voltage, then R9 = 1.1/4.75 μA and R1 = (3.0 – 1.1) 5.0 μA or about 240 kΩ and 390 kΩ respectively. The tempco at the top of the divider will be -4.0 mV (R1 + R9)/R9 or -10.5 mV/°C, an acceptable number for many applications.

Another method of automatic shutdown without temperature limitations is the use of a zener diode in series with the I_C pin and set resistor. When the battery voltage falls below V_Z + 1.2V the circuit will start to shut down. With this connection and the low battery detector, the application can be designed to signal a display when the battery voltage has dropped to the first programmed level, then shut itself off as the battery reaches the zener threshold.

The set current can also be turned off by forcing the I_C pin to 0.2V or less using an external transistor or mechanical switch. An example of this is shown in Figure 15.

In this circuit an external control voltage is used to determine the operating state of the RC4190. If the control voltage V_C is a logic 1 at the input of the 4025 (CMOS Triple NOR Gate), the voltage at the I_C pin will be less than 0.5V forcing the 4190 off (<0.1 μA I_{CC}). Both the 2N3904 and 2N2907 will be off insuring long shelf for the battery since less than 1.0 μA is drawn by the circuit.

When V_C goes to a logic 0, 2.0 μA is forced into the I_C pin through the 2.2 MΩ resistor and the NOR gate, and at the same time the 2N3904 and 2N2907 turn on, connecting the battery to the load.

As long as V_C remains low the circuit will regulate the output to 5.0V. This type of circuit is used to back up the main supply voltage when line interruptions occur, a particularly useful feature when using volatile memory systems.

9.0V Battery Life Extender

Figure 16 shows a common application: a circuit to extend the lifetime of a 9.0V battery. The regulator remains in its quiescent state (drawing only 215 μA) until the battery voltage decays below 7.5V, at which time it will start to switch and regulate the output at 7.0V until the battery falls below 2.2V.

If this circuit operates at its typical efficiency of 80%, with an output current of 10 mA, at 5.0V battery voltage, then the average input current will be $I_{IN} = (V_{OUT} \times I_L) \div (V_{BAT} \times ef)$ or (7.0V x 10 mA) ÷ (5.0V x 0.8 mA) = 17.5 mA.

Bootstrapped Operation (Step-Up)

In step-up applications, power to the RC4190 can be derived from the output voltage by connecting the $+V_S$ pin and the top of R1 to the output voltage (Figure 17).

One requirement for this circuit is that the battery voltage must be greater than 3.0V when it is energized or else there will not be enough voltage at pin 5 to start up the I_C. The big advantage of this circuit is the ability to operate down to a discharged battery voltage of 1.0V.

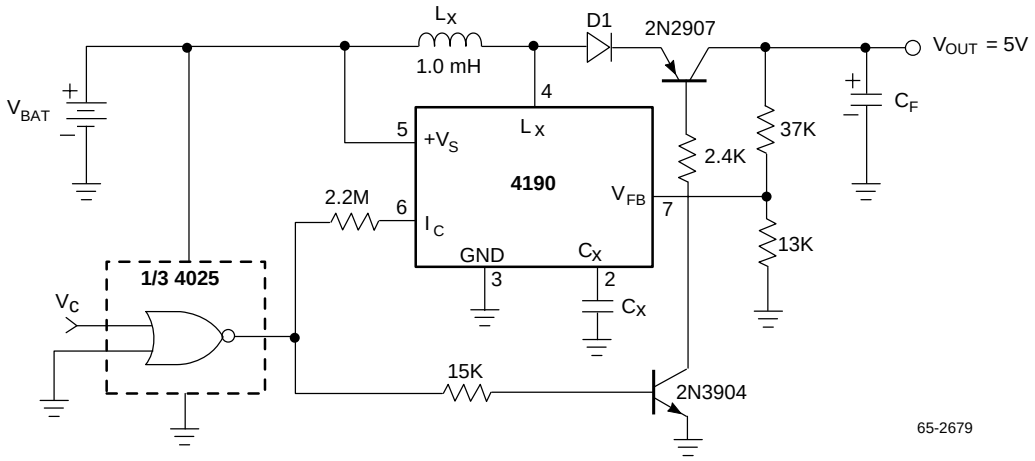


Figure 15. Battery Back-Up Circuit

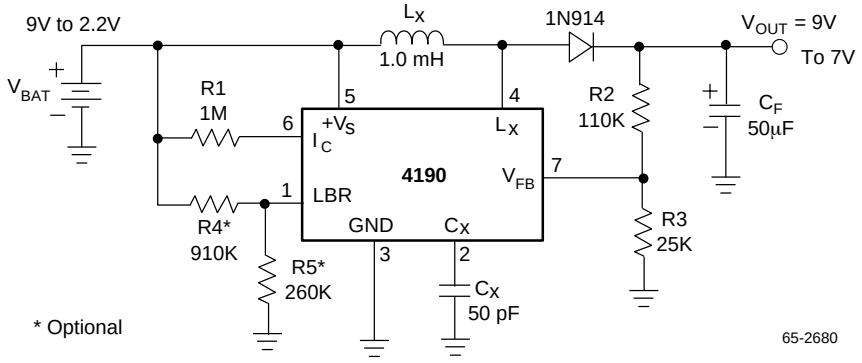


Figure 16. 9.0V Battery Life Extender

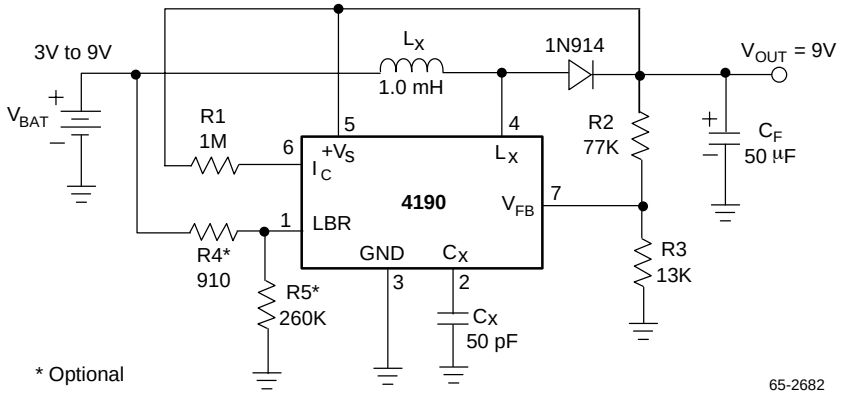


Figure 17. Bootstrapped Operation (Step-Up)

Buck-Boost Circuit (Step-Up/Down)

A disadvantage of the standard step-up and step-down circuits is the limitation of the input voltage range; for a step-up circuit, the battery voltage must always be less than the programmed output voltage, and for a step-down circuit, the battery voltage must always be greater than the output voltage. The following circuit eliminates this disadvantage, allowing a battery voltage above the programmed output voltage to decay to well below the output voltage (see Figure 18).

The circuit operation is similar to the step-up circuit operation, except that both terminal of the inductor are connected to switch transistors. This switching method allows the inductor to be disconnected from the battery during the time the inductor is being discharged. A new discharge path is provided by D1, allowing the inductor to be referenced to ground and independent of the battery voltage. The efficiency of this circuit will be reduced to 55-60% by losses in the extra switch transistor and diode. Efficiency can be improved by choosing transistors with low saturation voltages and by using power Schottky diodes such as Motorola's MBR030.

Step-Up Voltage Dependent Oscillator

The RC4190's ability to supply load current at low battery voltages depends on the inductor value and the oscillator frequency. Low values of inductance or a low oscillator frequency will cause a higher peak inductor current and therefore increase the load current capability. A large inductor current is not necessarily best, however, because the large amount of energy delivered with each cycle will cause a large voltage ripple at the output, especially at high input voltages. This trade-off between load current capability and output ripple can be improved with the circuit connection shown in Figure 19. This circuit uses the low battery detector to sense for a low battery voltage condition and will decrease the oscillator frequency after a pre-programmed threshold is reached.

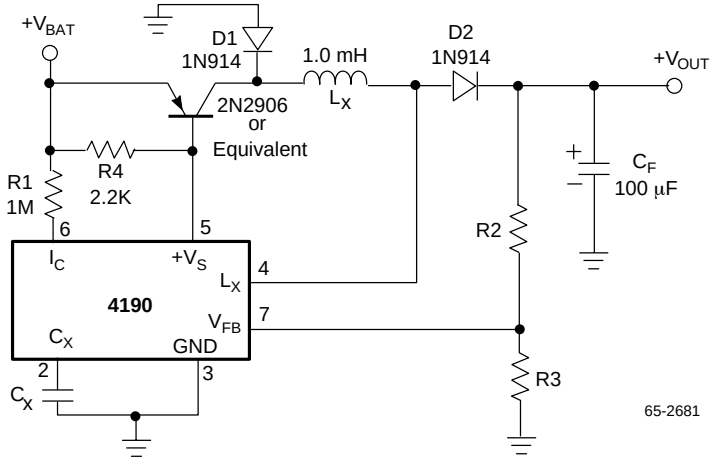


Figure 18. Buck Boost Circuit (Step-Up/Down)

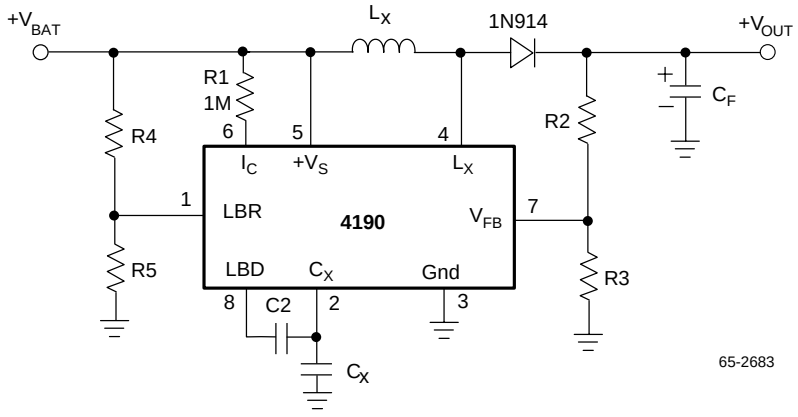


Figure 19. Step-Up Voltage Dependent Oscillator

The threshold is programmed exactly as the noram low battery detector connection:

$$V_{TH} = V_{REF}\left(\frac{R4}{R5} + 1\right)$$

When the battery voltage reaches this threshold, the comparator will turn on the open collector transistor at pin 8, effectively putting C2 in parallel with C_X. This added capacitance will reduce the oscillator frequency according to the following equation:

$$F_O = \frac{2.4 \times 10^{-6}}{C_X + C2}$$

Where C is in pF and F_O is in Hz.

Component values for a typical application might be R2 = 330 kΩ, R5 = 150 kΩ, C_X = 100 pF, and C2 = 100 pF. These values would set the threshold voltage at 4.1V and change the operating frequency from 48 kHz to 24 kHz. Note that this technique may be used for step-up, step-down, or inverting applications.

Step-Down Regulator With Protection

One disadvantage of the simple application circuits is their lack of short circuit protection, especially for the step-up circuit, which has a very low resistance path for current flow from the input to the output. A current limiting circuit which senses the output voltage and shuts down the 4190 if the output voltage drops too low can be built using the low battery detector circuitry. The low battery detector is connected to sense the output voltage and will shut off the oscillator by forcing pin 2 low if the output voltage drops. Figure 20 shows a schematic of a step-down regulator with this connection.

R2 and R3 set the output voltage, as in the circuit of Figure 2. Choose resistor values so R5 = R3 and R4 = R2, and make R8 25 to 35 times higher than R3. When the output is shorted, the open collector transistor at pin 8 will force pin 2 low and shut off the oscillator and therefore shut off the external switch transistor. The regulator will then remain in a low current off condition until power is removed and reapplied. C2 provides momentary current to ensure proper start-up. This scheme will not work with the simple step-up regulator, but will work with the boost-buck converter, providing short circuit protection in both step-up and step-down modes.

RC4190/RC4391 ± Power Supply

A positive and negative dual tracking power supply using a step-up RC4190 and an inverting RC4391 is shown in Figure 21. The inductor and capacitor values were chosen to achieve the highest practical output currents from a +12V battery, as it decays, while keeping the output voltage ripple under 100 mV_{p-p} at ±15V output.

The circuit may be adapted to other voltages and currents, but note that the RC4190 is step-up, so V_{OUT} must be greater than V_{BAT}.

The output voltages may both be trimmed by adjusting a single resistor value (R3 or R4), because the reference for the negative output is derived from $+V_{OUT}$. This connection also allows the output voltages to track each other with changes in temperature and line voltage.

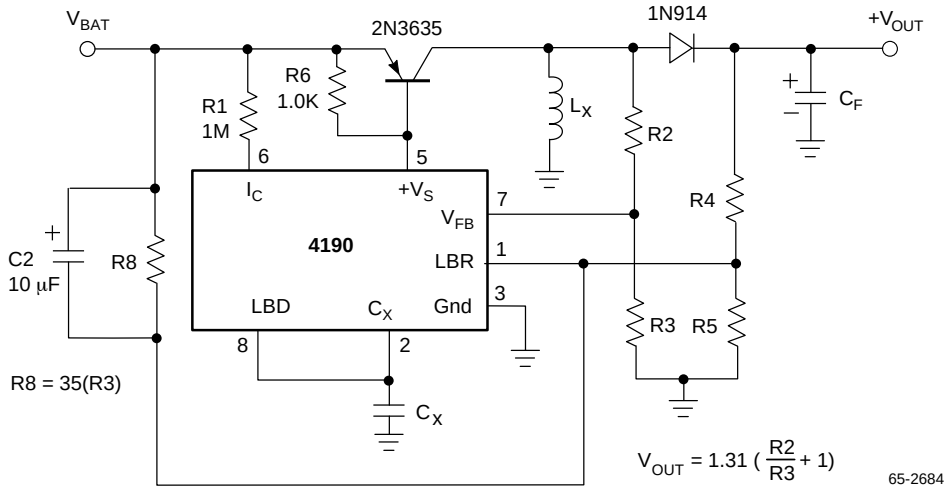


Figure 21. Step-Down Regulator with Protection

The timing capacitors are set up exactly as in the voltage dependent oscillator application of Figure 19. The values of R2, R5, C6, and C4 that are given were chosen to optimize for the +12V battery conditions, setting the threshold for oscillator frequency change at V_{BAT} = +8.5V.

As given, this power supply is capable of delivering +45 mA and -15 mA with regulation, until the battery decays below 5.0V.

For information on adjusting the RC4391 to meet a specific application refer to the Fairchild Semiconductor RC4391 data sheet.

Negative Step-Up Regulator

In the circuit of Figure 22, a bootstrap arrangement of supply and ground pins helps generate an output voltage more negative than the input voltage. On power-up, the output filter capacitor (C_F) will charge through D2 and L_X. When the voltage goes below -2.4V, the RC4190 begins switching and charging C_F. The output will regulate at a value equal to the reference voltage (1.31V) plus the zener voltage of D1. R_Z sets the value of zener current, stabilized at 1.31V/R2.

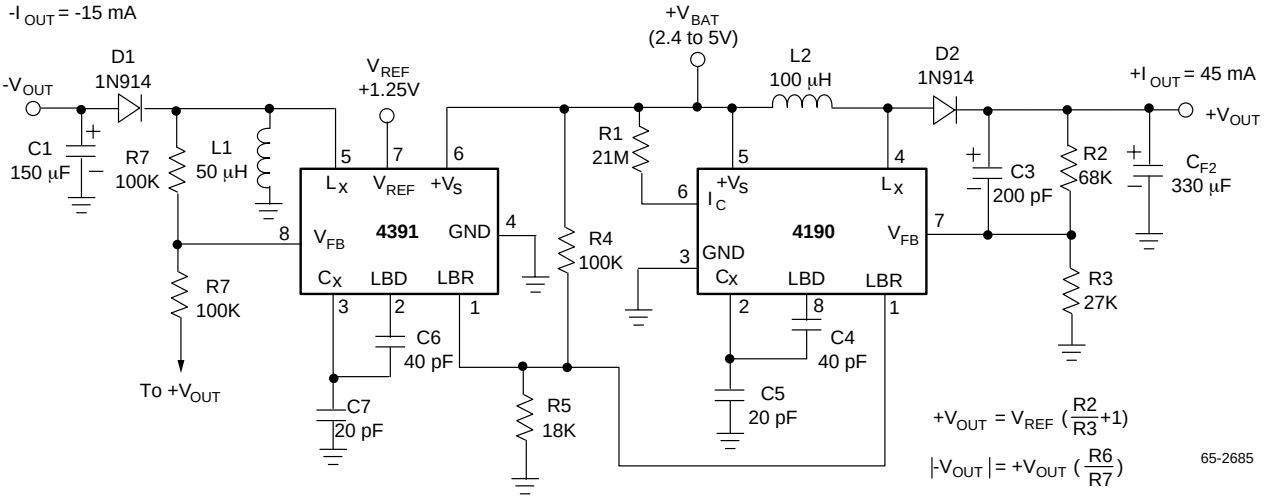


Figure 21. RC4190/RC4391 Power Supply (±15V)

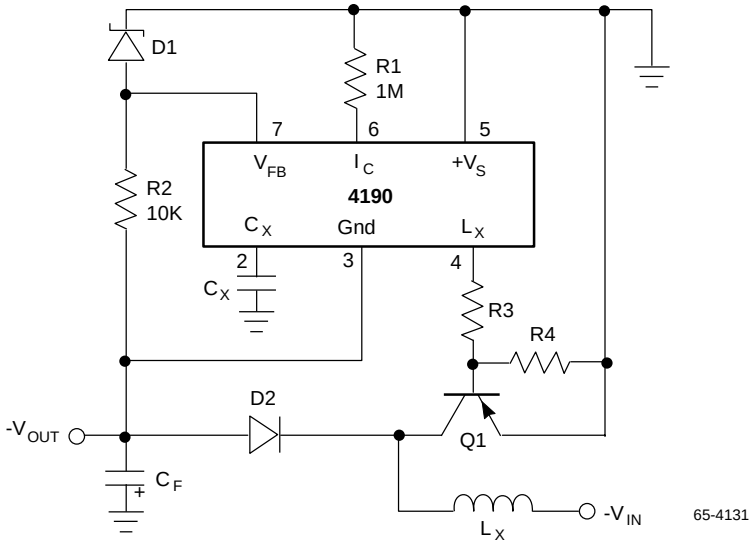
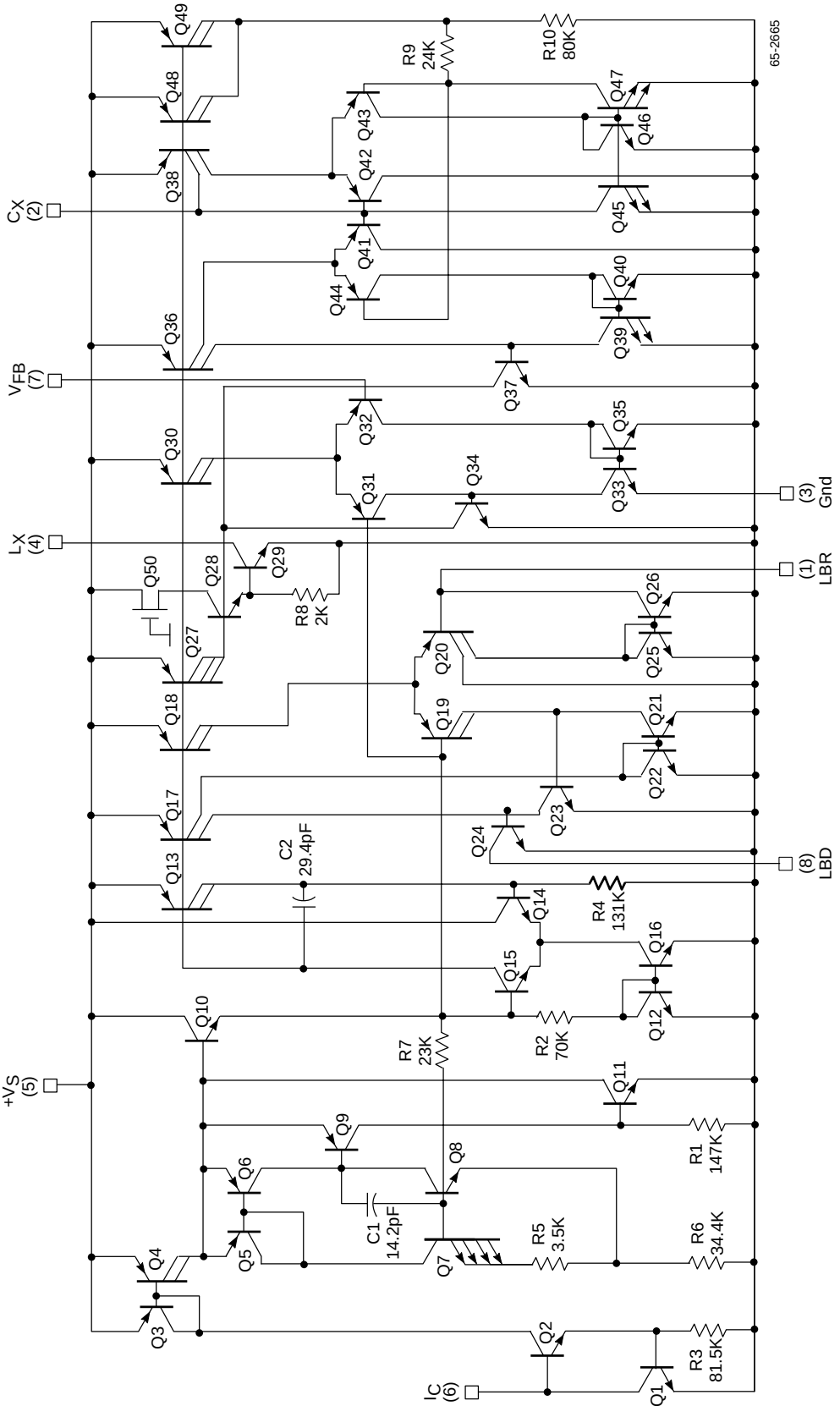
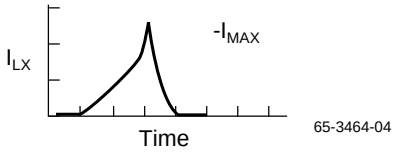
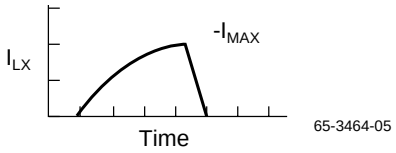
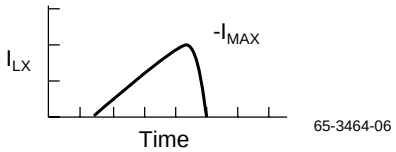


Figure 22. Negative Step-Up Regulator

Simplified Schematic Diagram



Troubleshooting Chart

Symptom	Possible Problem
Draws excessive supply current on start-up	Battery not "stiff" — inadequate supply bypass capacitor.
	Inductance value too low.
	Operating frequency (F_O) too low.
Output voltage is low.	Inductance value too high for F_O or core saturating.
Inductor "sings" with audible hum.	Not potted well or bolted loosely.
L_X in appears noisy — scope will not synchronize.	Normal operating condition.
Inductor current shows nonlinear waveform. 	Inductor is saturating: 1. Core too small. 2. Core too hot. 3. Operating frequency too low.
Inductor current shows nonlinear waveform. 	Waveform has resistive component: 1. Wire size too small. 2. Power transistor lacks base drive. 3. Components not rated high enough. 4. Battery has high series resistance.
Inductor current is linear until high current is reached. 	External transistor lacks base drive or beta is too low.
Poor efficiency.	Core saturating.
	Diode or transistor: 1. Not fast enough. 2. Not rated for current level (high V_{CE} SAT).
	High series resistance.
	Operating frequency too high.
Motorboating (erratic current pulses).	Loop stability problem — needs feedback capacitor from V_{OUT} to V_{FB} (pin 7), 100 to 1000 pF.

Background Information

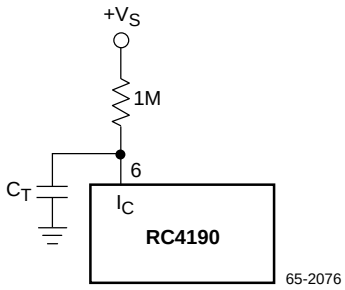
During the past several years there have been various switching regulator ICs introduced by many manufacturers, all of which attended to the same market, namely controllers for use in power supplies delivering greater than 10W of DC power. Fairchild Semiconductor felt there was another area which could use a switching regulator to even more advance the area of battery powered equipment. Battery powered systems have problems peculiar unto themselves: changes in supply voltage, space considerations, battery life and usually cost. The RC4190 was designed with each of these in mind.

The RC4190 was partitioned to work in an eight pin package, making it smaller than other controllers which go into 14 and 16 pin packages.

Battery powered applications require the load as seen by the battery to be as small as possible to extend battery life. To this end, the quiescent current of the RC4190 is 15 to 100 times less than controllers designed for nonbattery applications. At the same time, the switch transistor can sink 200 mA at 0.4V, comparable to or better than higher powered controllers. As an example, the 4190 configured in the step-up mode can supply 5.0V at 40 mA output with an input of 3.0V.

Cost is usually a primary consideration in battery powered systems. The RC4190, guaranteed to work down to 2.2V, can save the designer and end user money as well because battery costs decrease as the number of cells needed goes down.

Soft Start



The delay introduced by the RC time constant at start-up allows the output filter capacitor to charge up, reducing the instantaneous supply current. A typical value for C is in the 0.1μF range.

Bootstrapped Low Voltage Start-Up

Figure 24 shows the bootstrapped application can be "kicked on" using an extra capacitor and triple pole double throw switch (3PDT). This connection allows the circuit to start up using a single Ni-Cad cell of 1.2V to 1.6V. When power is first applied the 1.2V battery does not provide enough voltage to meet the minimum 2.2V supply voltage requirement. The 22μF capacitor, when switched, temporarily doubles the battery voltage to bias up the RC4190.

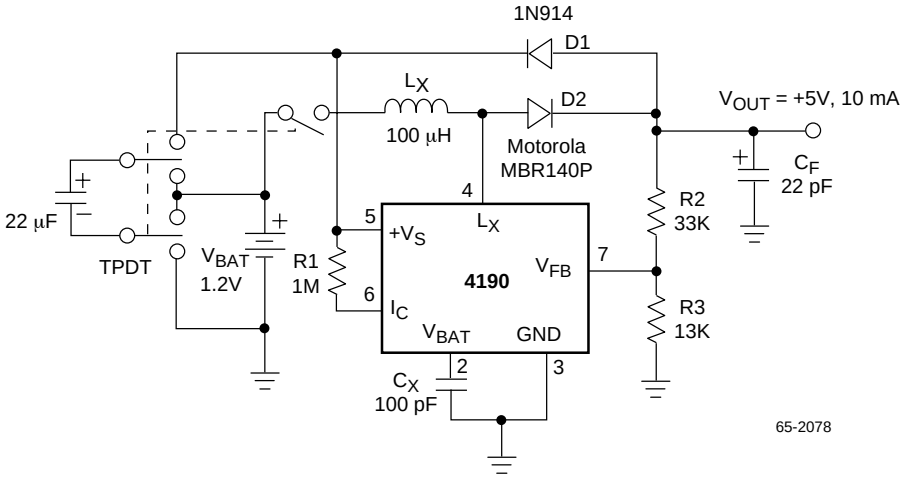


Figure 24. Bootstrapped Low Voltage Start-Up

When the switch is the down position, the capacitor charges up to the battery voltage. The, when the switch is changed to the up position, the capacitor is put in series connection with the battery, and the doubled voltage is applied directly to the positive power supply lead of the RC4190. This voltage is enough to bias the junctions internal to the RC4190 and gets it started. Then, when the stepped up output voltage reaches a high enough value, diode D1 is forward biased and the output voltage takes over supplying power to the RC4190. The circuit is shown with component values for +5V output, but the circuit can be set up for other voltages.

Electricity Versus Magnetism

Electrically the inductor must meet just one requirement, but that requirement can be hard to satisfy. The inductor must exhibit the correct value of inductance (L, in Henrys) as the inductor current rises to its highest operating value (I_{MAX}). This requirement can be met most simply by choosing a very large core and winding it until it reaches the correct inductance value, but that brute force technique wastes size, weight and money. A more efficient design technique must be used.

Question: What happens if too small a core is used?

First, one must understand how the inductor's magnetic field works. The magnetic circuit in the inductor is very similar to a simple resistive electrical circuit (see Figure 20). There is a magnetizing force (H, in oersteds), a flow of magnetism, or flux density (B, in Gauss), and resistance to the flux, called permeability (U, in Gauss per oersted). H is equivalent to voltage in the electrical model, flux density is like current flow, and permeability is like resistance (except for two important differences discussed on the following page).

First Difference: Permeability, instead of being analogous to resistance, is actually more like conductance (1/R). As permeability increases, flux increases.

Second Difference: Resistance is a linear function. As voltage increases, current increases proportionally, and the resistance value stays the same. In a magnetic circuit the value of permeability varies as the applied magnetic force varies. This nonlinear characteristic is usually shown in graph form in ferrite core manufacturer's data sheets. See Figure 26.

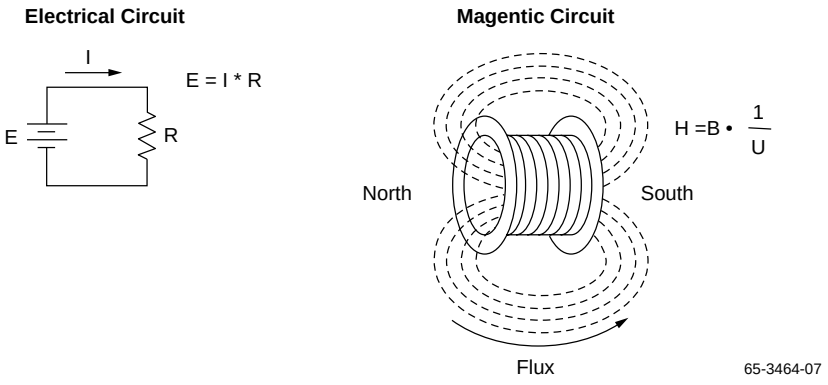


Figure 25. Electricity Versus Magnetism

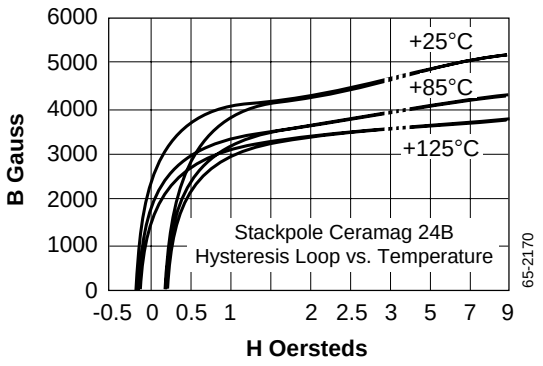


Figure 26. Typical Manufacturer's Curve Showing Saturation Effect

As the applied magnetizing force increases, at some point the permeability will start decreasing, and therefore the amount of magnetic flux will not increase any further, even as the magnetizing force increases. The physical reality is that, at the point where the permeability decreases, the magnetic field has realigned all of the magnetic domains in the core material. Once all of the domains have been aligned the core will then carry no more flux than just air; it becomes as if there were no core at all. This phenomenon is called saturation. Because the inductance value, L, is dependent on the amount of flux, core saturation will cause the value of L to decrease dramatically, in turn causing excessive and possibly destructive inductor current.

Pot Cores for RC4190

Pot core inductors are best suited for the RC4190 micropower switching regulator for several reasons:

1. **They are available in a wide range of sizes. RC**4190 applications are usually low power with relatively low peak currents (less than 500mA). A small inexpensive pot core can be chosen to meet the circuit requirements.

2. **Pot cores are easily mounted.** They can be bolted directly to the PC card adjacent to the regulator IC.

3. **Pot cores can be easily air-gapped**. The length of the gap is simply adjusted using different washer thicknesses. Cores are also available with predetermined air gaps.

4. **Electromagnetic interference (EMI) is kept to a minimum.** The completely enclosed design of pot core reduces stray electromagnetic radiation—an important consideration of the regulator circuit is built on a PC card with other circuitry.

Core Size

Question: Is core size selected according to load power?

Not quite. Core size is dependent on the amount of energy stored, not on load power. Raising the operating frequency allows smaller cores and windings. Reduction of the size of the magnetics is the main reason switching regulator design tends toward higher operating frequency. Designs with the RC4190 should use 75kHz as a maximum running frequency, because the turn off delay of the power transistor and stray capacitive coupling begin to interfere. Most applications are in the 10 to 50kHz range, for efficiency and EMI reasons.

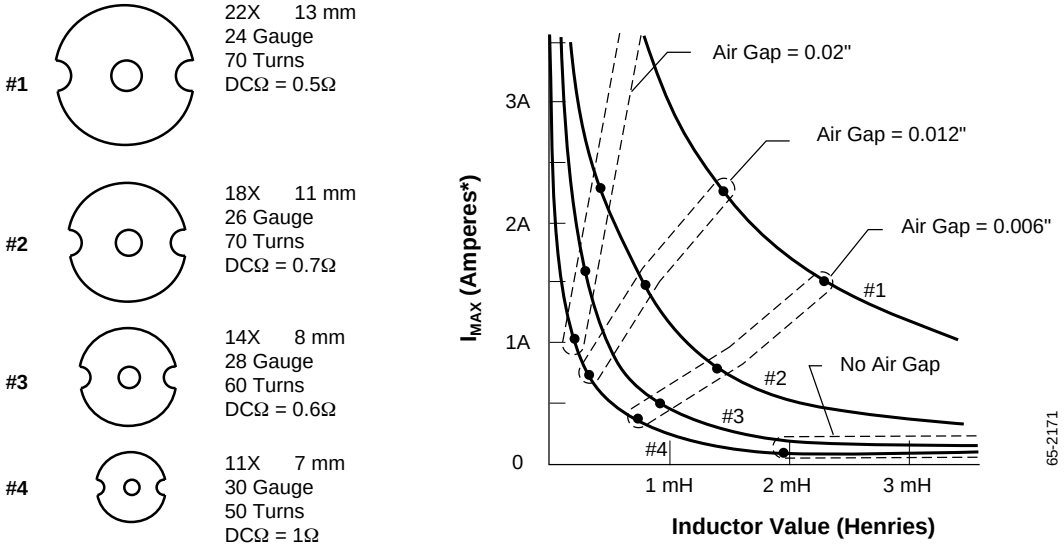
The peak inductor current (I_{MAX}) must reach a high enough value to meet the load current drain. If the operating frequency is increased, and simultaneously the inductor value is decreased, then the core can be made smaller. For a given core size and winding, an increase in air gap spacing (an air gap is a break in the material in the magnetic path, like a section broken off a doughnut) will cause the inductance to decrease and I_{MAX} (the usable peak current before saturation) to increase.

The curves shown in Figure 26 are typical of the ferrite manufacturer's power HF material, such as Siemens N27 or Stackpole 24B, which are usually offered in standard millimeter sizes including the sizes shown.

Use of the Design Aid Graph (Figure 27)

1. From the application requirement, determine the inductor value (L) and the required peak current (I_{MAX}).

2. Observe the curves of the design aid graph and determine the smallest core that meets both the L and I requirements.



*Includes safety margin (25%) to ensure nonsaturation

Figure 27. Inductor Design Aid

3. Note the approximate air gap at I_{MAX} for the selected core, and order the core with the gap. (If the gapping is done by the user, remember that a washer spacer results in an air gap of twice the washer thickness, because two gaps will be created, one at the center post and one at the rim, like taking two bites from a doughnut.)

4. If the required inductance is equal to the indicated value on the graph, then wind the core with the number of turns shown in table of sizes. The turns given are the maximum number for that gauge of wire that can be easily wound in the cores winding area.

5. If the required inductance is less than the value indicated on the graph, a simple calculation must be done to find the adjusted number of turns. Find A_L (inductance index) for a specific air gap.

   $$\frac{L(indicated)}{Turns^2} = A_L$$

   in Henrys/turn^2

   Then divide the required inductance value by A_L to give the actual turns squared, and take the square root to find the actual turns needed.

   $$ActualTurns = \frac{L(required)}{A_L}$$

   If the actual number of turns is significantly less than the number from the table then the wire size can be increased to use up the left-over winding area and reduce resistive losses.

6. Wind and gap the core as per calculations, and measure the value with an inductance meter. Some adjustment of the number of turns may be necessary.

   The saturation characteristics may be checked with the inductor wired into the switching regulator application circuit. To do so, build and power up the circuit. Then (recommend Tektronix P6042 or equivalent) around the inductor lead and monitor the current in the inductor. Draw the maximum load current from the application circuit so that the regulator is running at close to full duty cycle.

   Compare the waveform you see to those pictured in Figure 28.

   Check for saturation at the highest expected ambient temperature.

7. After the operation in circuit has been checked, reassemble and pot the core using a potting compound recommended by the manufacturer.

   If the core material differs greatly in magnetic characteristics from the standard power material shown in Figure 22, then the following general equation can be used to help in winding and gapping. This equation can be used for any core geometry, such as an E-E core.

   $$L_X = \frac{(1.26)(N^2)(Ae)(10^8)}{g = (le)/(ue)}$$

   Where: N = number of turns
   Ae = core area from data sheet (in cm2)
   le = magnetic path length from data sheet (in cm)
   ue = permeability of core from manufacturer's graph
   g = center post air gap (in cm)

Manufacturers

Below is a list of several pot core manufacturers:

Ferroxcube Company
5083 Kings Highway
Saugerties, NY 12477

Indiana General Electronics
Keasley, NJ 08832

Siemens Company
186 Wood Avenue South
Iselin, NJ 08830

Stackpole Company
201 Stackpole Street
St. Mary, PA 15857

TDK Electronics
13-1-Chome
Nihonbaski, Chuo-ku, Tokyo

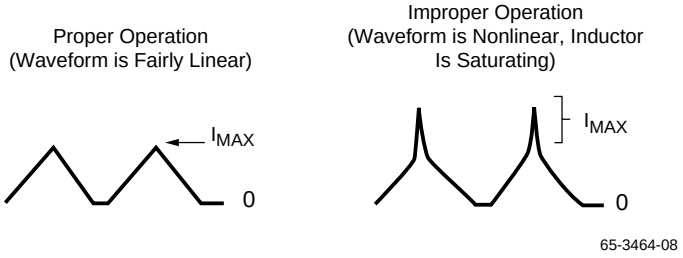


Figure 28. Inductor Current Waveforms

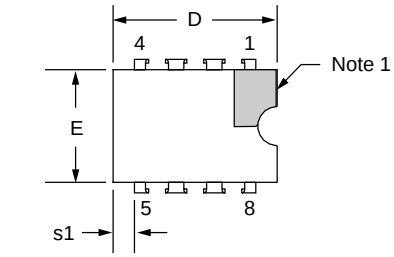
Mechanical DImensions

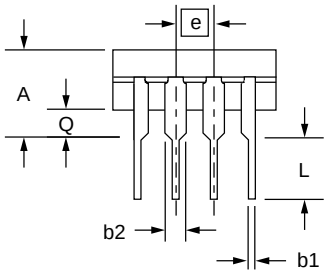
8-Lead Ceramic DIP Package

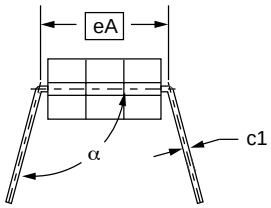
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2, 8
c1	.008	.015	.20	.38	8
D	—	.405	—	10.29	4
E	.220	.310	5.59	7.87	4
e	.100 BSC		2.54 BSC		5, 9
eA	.300 BSC		7.62 BSC		7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 4, 5 and 8 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 8.
6. Applies to all four corners (leads number 1, 4, 5, and 8).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Six spaces.







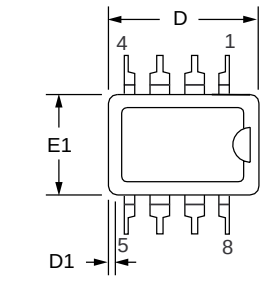
Mechanical DImensions (continued)

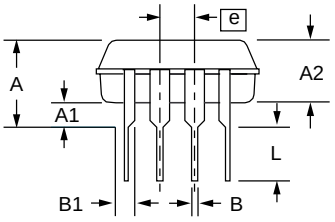
8-Lead Plastic DIP Package

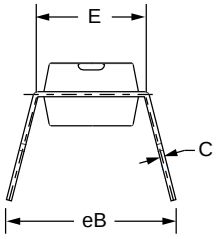
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	.348	.430	8.84	10.92	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.160	2.92	4.06	
N	8°		8°		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.







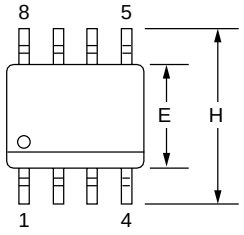
Mechanical DImensions (continued)

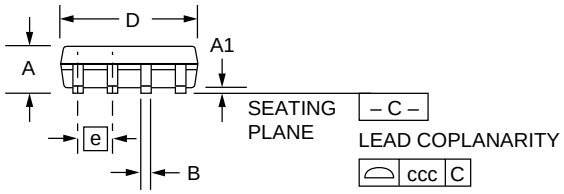
8-Lead SOIC Package

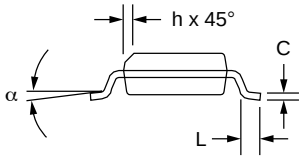
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.20	0.25	5
D	.189	.197	4.80	5.00	2
E	.150	.158	3.81	4.01	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	8		8		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Ordering Information

Product Number	Temperature Range	Screening	Package
RC4190M	0° to 70°C	Commercial	8 Pin Narrow SOIC
RC4190N	0° to 70°C	Commercial	8 Pin Plastic DIP
RM4190D	-55°C to +125°C		8 Pin Ceramic DIP
RM4190D/883B	-55°C to +125°C	Military	8 Pin Ceramic DIP
RV4190N	-25°C to +85°C	Industrial	8 Pin Plastic DIP

Note:

1. /883B suffix denotes MIL-STD-883, Level B processing.

5/20/98 0.0m 001
Stock#DS30004190

RC4191/RC4192/RC4193

Micropower Switching Regulator

Features

- High efficiency – 85% typical
- Low quiescent current – 215 μA
- Adjustable output – 1.3V to 30V
- High switch current – 200 mA
- Bandgap reference – 1.31V
- Accurate oscillator frequency – ±10%
- Remote shutdown capability
- Low battery detection circuitry
- Low component count
- 8-lead packages

Description

The RC4191/4192/4193 series of monolithic ICs are low power switch mode regulators intended for miniature power supply applications. These DC-to-DC converter ICs provide all of the active components needed to create supplies for micropower circuits. Contained internally are an oscillator, switch, reference, comparator, and logic, plus a discharged battery detection circuit.

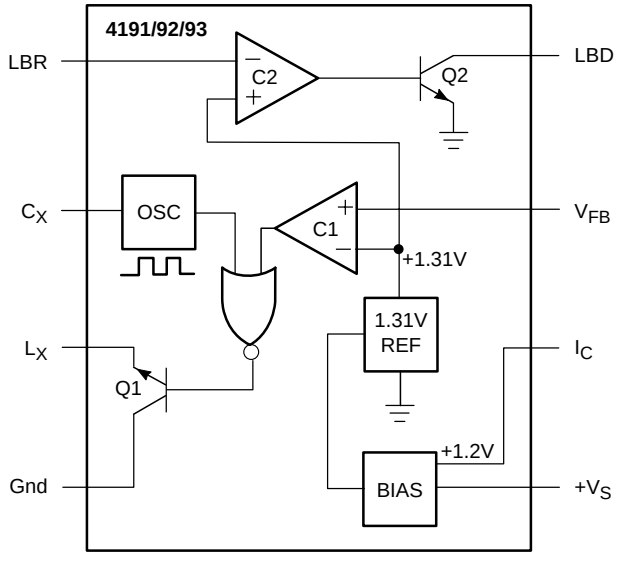
These regulators can achieve up to 85% efficiency in most applications while operating over a wide supply voltage range, 2.2V to 30V, at a very low quiescent current drain of 215 μA.

The standard application circuit requires just seven external components for step-up operation: an inductor, a steering diode, three resistors, a low value timing capacitor, and an electrolytic filter capacitor. The combination of simple application circuit, low supply current, and small package make the RC4193 adaptable to a wide range of miniature power supply applications.

The RC4193 is most suited for single ended step-up ($V_{OUT} > V_{IN}$) circuits because the NPN internal switch transistor is referenced to ground. It is complemented by Fairchild Semiconductor's micropower switching regulator, the RC4391, which is dedicated to step-down ($V_{OUT} < V_{IN}$) and inverting $V_{OUT} = -V_{IN}$) applications. Between the two devices the ability to create all three basic switching regulator configurations is assured. Refer to the RC4391 data sheet for step-down and inverting applications.

The RC4191/92/93 series of micropower switching regulators consists of three devices, each with slightly different specifications. The RM4191 has a 1.5% maximum output voltage tolerance, 0.2% maximum line regulation, and operation to 30V. The RC4192 has a 3.0% maximum output voltage tolerance, 0.5% maximum line regulation, and operation to 30V. The RC4193 has a 5.0% maximum output voltage tolerance, 0.5% maximum line regulation, and operation to 24V. Other specifications are identical for the RC4191, RC4192 and RC4193. Each type is available in commercial, industrial, and military temperature ranges, and in plastic and ceramic DIPs and S0-8 packages.

Block Diagram



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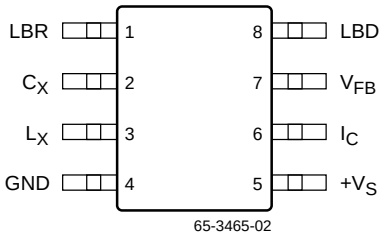
Pin Assignments



Pin Definitions

Pin Name	Pin Number	Pin Function Description
LBR	1	Low Battery (Set) Resistor
C_X	2	Timing Capacitor
L_X	3	External Inductor
Gnd	4	Ground
$+V_S$	5	Positive Supply Voltage
I_C	6	Reference Set Current
V_{FB}	7	Feedback Voltage
LBD	8	Low Battery Detector Output

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min	Typ	Max	Units
Supply Voltage (Without External Transistor)	4191, 4192			30	V
	4193			24	V
$P_D T_A$ < 50°C	SOIC			300	mW
	PDIP			468	mW
	CerDIP			833	mW
Operating Temperature	RM4191/2/3	-55		125	°C
	RV4191/2/3	-25		85	°C
	RC4191/2/3	0		70	°C
Storage Temperature		-65		150	°C
Junction Temperature	SOIC, PDIP		125		°C
	CerDIP		175		°C
Switch Current	Peak			375	mA
For T_A > 50°C Derate at	SOIC		4.17		mW/°C
	PDIP		6.25		mW/°C
	CerDIP		8.33		mW/°C

Note:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter			Min	Typ	Max	Units
θ_{JC}	Thermal resistance	CerDIP		45		°C/W
θ_{JA}	Thermal resistance	SOIC		240		°C/W
		PDIP		160		°C/W
		CerDIP		150		°C/W

Electrical Characteristics

($+V_S$ = +6.0V, I_C = 5.0 μA over the full operating temperature range unless otherwise noted.)

Parameters		Conditions	4191			4192			4193			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$+V_S$	Supply Voltage		2.6		30	2.6		30	2.6		24	V
V_{REF}	Reference Voltage (Internal)		1.25	1.31	1.37	1.23	1.31	1.39	1.20	1.31	1.42	V
I_{SY}	Supply Current	Measure at Pin 5 $I_3 = 0$		225	350		235	350		225	350	μA
	Line Regulation	$0.5\ V_O < V_S < V_O$		0.2	0.5		0.5	1.0		0.5	1.0	% V_O
L_I	Load Regulation	$V_S = 0.5\ V_O$ P_L = 150 mW		0.5	1.0		0.5	1.0		0.5	1.0	% V_O
I_C	Reference Set Current		1.0	5.0	50	1.0	5.0	50	1.0	5.0	50	μA
I_{CO}	Switch Leakage Current	V_3 = 24V (4193) 30V (4191, 4192)			30			30			30	μA
I_{SO}	Supply Current (Disabled)	$V_C \leq 200$ mV			30			30			30	μA
I_{LBD}	Low Battery Output Current	$V_8 = 0.4V$, $V_1 = 1.1V$	400	1200		400	1200		400	1200		μA
	Oscillator Frequency Temperature Drift			±200			±200			±200		ppm/ °C

Electrical Characteristics

(+V_S = +6.0V, I_C = 5.0 μA, and T_A = +25°C unless otherwise noted.)

Parameters		Conditions	4191			4192			4193			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$+V_S$	Supply Voltage		2.2		30	2.2		30	2.2		24	V
V_{REF}	Reference Voltage (Internal)		1.29	1.31	1.33	1.27	1.31	1.35	1.24	1.31	1.38	V
I_{SW}	Switch Current	V_3 = 400 mV	100	200		100	200		100	200		mA
I_{SY}	Supply Current	Measure at Pin 5 I_3 = 0		215	300		215	300		215	300	μA
ef	Efficiency			85			85			85		%
	Line Regulation	0.5 V_O < V_S < V_O		0.04	0.2		0.04	0.5		0.04	0.5	% V_O
L_I	Load Regulation	V_S = +0.5 V_{OUT} P_L = 150 mW		0.2	0.5		0.2	0.5		0.2	0.5	% V_O
F_O	Operating Frequency Range		0.1	25	75	0.1	25	75	0.1	25	75	kHz
I_C	Reference Set Current		1.0	5.0	50	1.0	5.0	50	1.0	5.0	50	μA
I_{CO}	Switch Leakage Current	V_3 = 24V (4193), 30V (4191/2)		0.01	5.0		0.01	5.0		0.01	5.0	μA
I_{SO}	Supply Current (Disabled)	V_C ≤ 200 mV		0.1	5.0		0.1	5.0		0.1	5.0	μA
I_1	Low Battery Bias Current	V_1 = 1.2V		0.7			0.7			0.7		μA
I_{CX}	Capacitor Charging Current			8.6			8.6			8.6		μA
	Oscillator Frequency Tolerance			±10			±10			±10		%
$+V_{THX}$	Capacitor Threshold Voltage +			1.4			1.4			1.4		V
$-V_{THX}$	Capacitor Threshold Voltage –			0.5			0.5			0.5		V
I_{FB}	Feedback Input Current	V_7 = 1.3V		0.1			0.1			0.1		μA
I_{LBD}	Low Battery Output Current	V_8 = 0.4V, V_1 = 1.1V	500	1500		500	1500		500	1500		μA

Typical Performance Characteristics

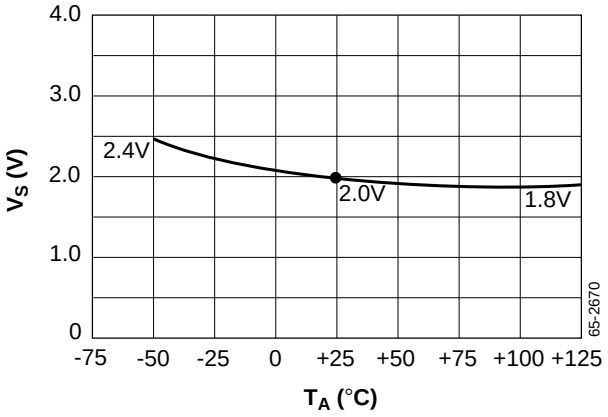


Figure 1. Minimum Supply Voltage vs. Temperature

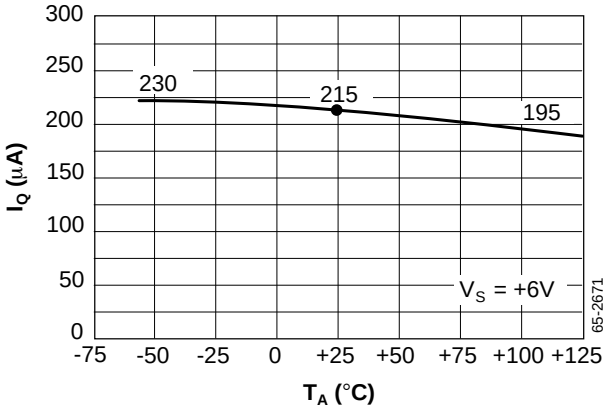


Figure 2. Quiescent Current vs. Temperature

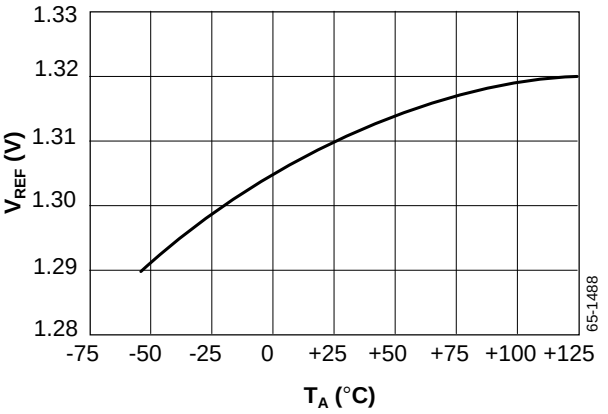


Figure 3. Reference Voltage vs. Temperature

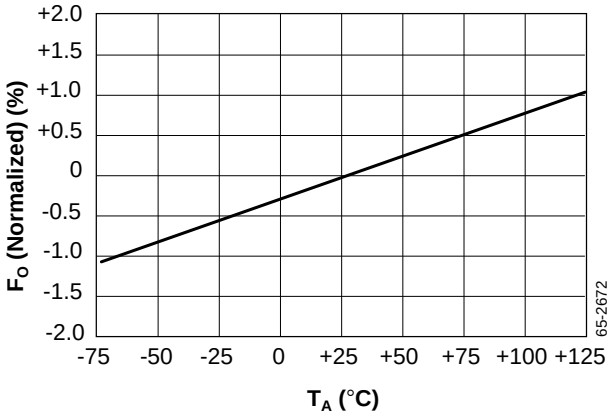


Figure 4. Oscillator Frequency vs. Temperature

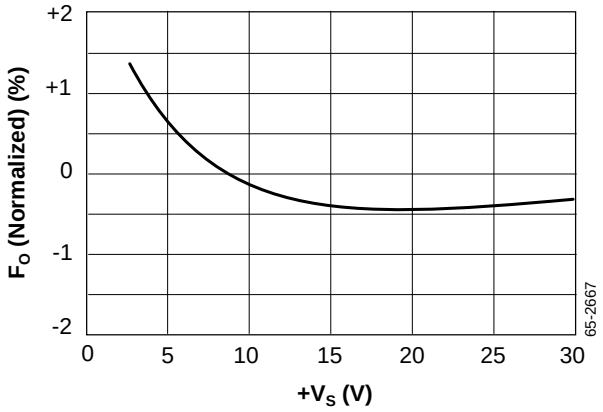


Figure 5. Minimum Supply Voltage vs. Temperature

Applications Discussion

Simple Step-Up Converter

The most common application, the step-up regulator, is derived from a simple step-up ($V_{OUT} > V_{BAT}$) DC-to-EC Converter (Figure 6).

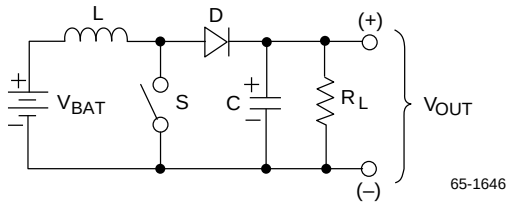


Figure 6. Simple Set-Up Converter

When switch S is closed, the battery voltage is applied across the inductor L. Charging current flows through the inductor, building up a magnetic field, increasing as the switch is held closed. While the switch is closed, the diode D is reverse biased (open circuit) and current is supplied to the load by the capacitor C. Until the switch is opened, the inductor current will increase linearly to a maximum value determined by the battery voltage, inductor value, and the amount of time the switch is held closed ($I_{MAX} = V_{BAT}/L \times T_{ON}$). When the switch is opened, the magnetic field collapses, and the energy stored in the magnetic field is converted into a discharge current which flows through the inductor in the same direction as the charging current. Because there is no path for current to flow through the switch, the current must flow through the switch, the current must flow through the diode to supply the load and charge the output capacitor.

If the switch is opened and closed repeatedly, at a rate much greater than the time constant of the output RC, then a constant DC voltage will be produced at the output.

An output voltage higher than the input voltage is possible because of the high voltage produced by a rapid change of current in the inductor. When the switch is opened, the inductor voltage will instantly rise high enough to forward bias the diode, to $V_{OUT} + V_D$.

In the complete RC4193 regulator, a feedback control system adjusts the on time of the switch, controlling the level of inductor current, so that the average inductor discharge current equals the load current, thus regulating the output voltage.

Complete Step-Up Regulator

A complete schematic of the minimum step-up application is shown in Figure 7. The ideal switch in the DC-to-DC Converter diagram is replaced by an open collector NPN transistor Q1. C_F functions as the output filter capacitor, and D1 and L_X replace D and L.

When power is first applied, the current in R1 supplies bias current to pin 6 (I_C). This current is stabilized by a unity gain current source amplifier and then used as bias current for the 1.31V bandgap reference. A very stable bias current generated by the bandgap is mirrored and used to bias the remainder of the chip. At the same time the RC4193 is starting up, current will flow through the inductor and the diode to charge the output capacitor to $V_{BAT} – V_D$.

At this point, the feedback (pin 7) senses that the output voltage is too low, by comparing a division of the output voltage (set by the ratio of R2 to R3) to the +1.31V reference. If the output voltage is too low then the comparator output changes to a logical zero. The NOR gate then effectively ANDs the oscillator square wave with the comparator signal; if the comparator output is zero AND the oscillator output is low, then the NOR gate output is high and the switch transistor will be forced on. When the oscillator goes high again, the NOR gate output goes low and the switch transistor will turn off. This turning on and off of the switch transistor performs the same function that opening and closing the switch in the simple DC-to-DC Converter does; i.e., it stores energy in the inductor during the on time and releases it into the capacitor during the off time.

The comparator will continue to allow the oscillator to turn the switch on and off until enough charge has been delivered to the capacitor to raise the feedback voltage above 1.31V.

Thereafter, this feedback system will vary the duration of the on time in response to changes in load current or battery voltage (see Figure 8). If the load current increases (waveform C), then the transistor will remain on (waveform D) for a longer portion of the oscillator cycle (waveform B), thus allowing the inductor current (waveform E) to build up to a higher peak value. The duty cycle of the switch transistor varies in response to changes in load and time.

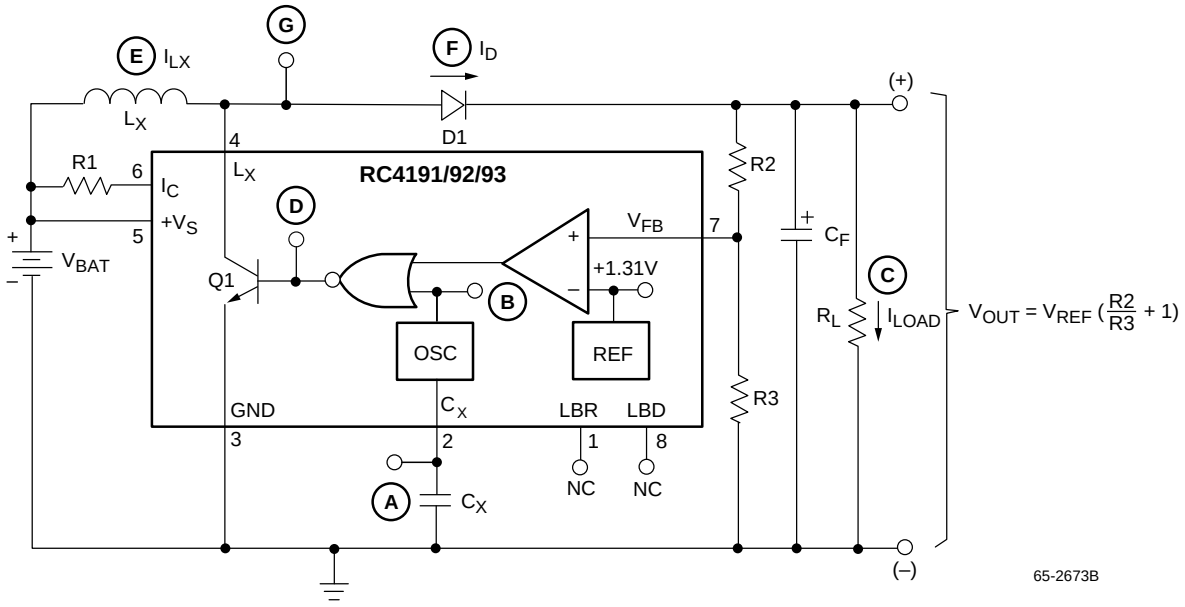


Figure 7. Complete Step-Up Regulator

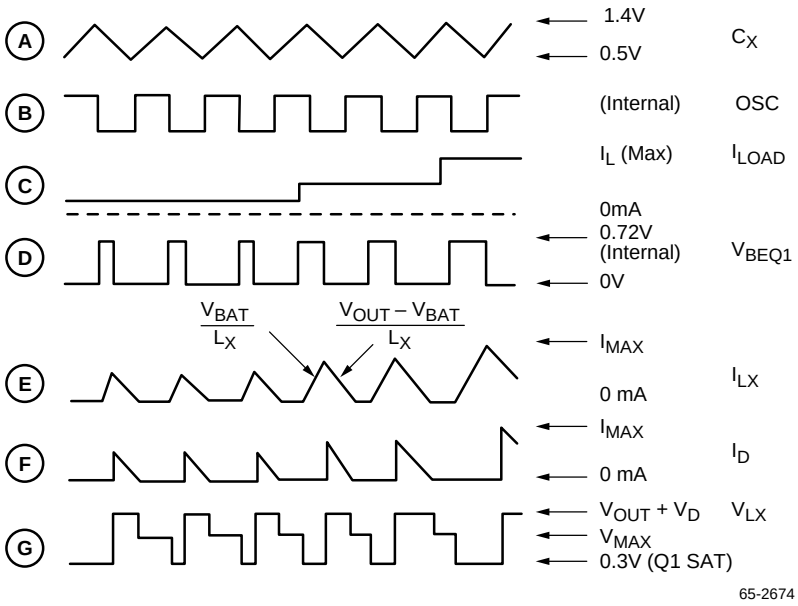
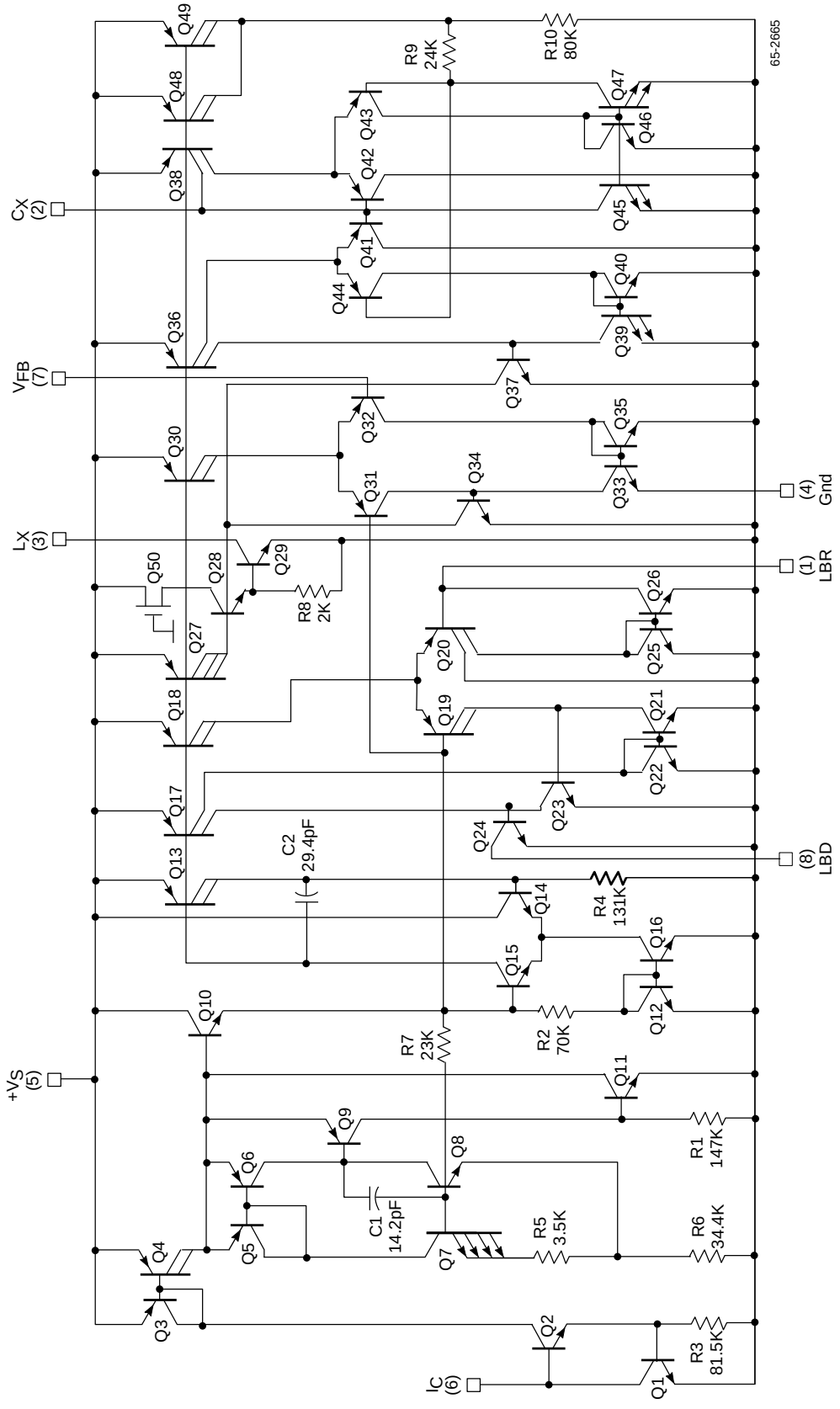


Figure 8. Step-Up Regulator Waveforms

Simplified Schematic Diagram



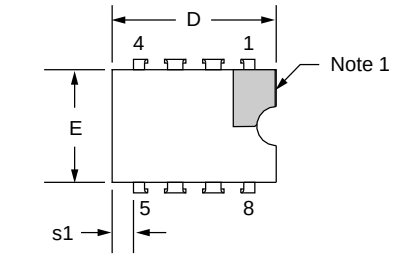
Mechanical DImensions

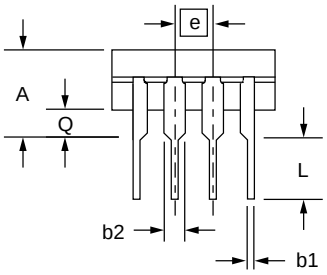
8-Lead Ceramic DIP Package

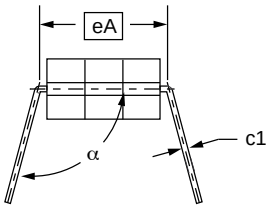
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2, 8
c1	.008	.015	.20	.38	8
D	—	.405	—	10.29	4
E	.220	.310	5.59	7.87	4
e	.100 BSC		2.54 BSC		5, 9
eA	.300 BSC		7.62 BSC		7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 4, 5 and 8 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 8.
6. Applies to all four corners (leads number 1, 4, 5, and 8).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Six spaces.







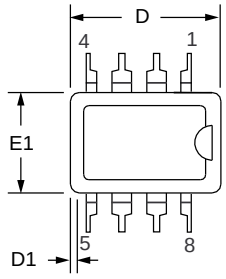
Mechanical DImensions (continued)

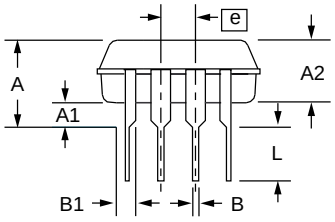
8-Lead Plastic DIP Package

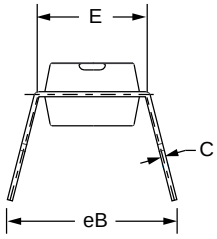
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	.348	.430	8.84	10.92	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.160	2.92	4.06	
N	8°		8°		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.







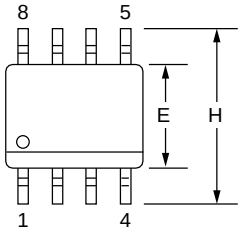
Mechanical DImensions (continued)

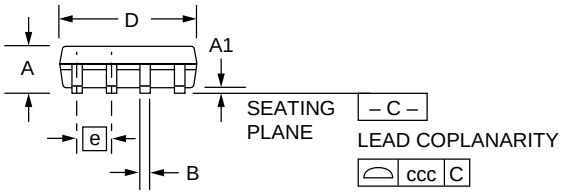
8-Lead SOIC Package

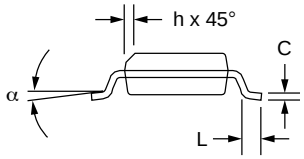
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.20	0.25	5
D	.189	.197	4.80	5.00	2
E	.150	.158	3.81	4.01	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	8		8		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Ordering Information

Product Number	Temperature Range	Screening	Package
RC4191M/2M/3M	0° to +70°C	Commercial	8 Pin Wide SOIC
RC4191N/2N/3N	0° to +70°C	Commercial	8 Pin Plastic DIP
RV4191N/92N/93N	-25° to +85°C		8 Pin Plastic DIP
RM4191D/92D/93D	-55°C to +125°C		8 Pin Ceramic DIP
RM4191D/883	-55°C to +125°C	Military	8 Pin Ceramic DIP

Note:

1. /883 suffix denotes MIL-STD-883, Par. 1.2.1 compliant device.

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RC4194

Dual Tracking Voltage Regulators

Features

- Simultaneously adjustable outputs with one resistor to ±42V
- Load current – ±200 mA with 0.04% load regulation
- Internal thermal shutdown at T_J = +175°C
- External balance for ±V_{OUT} unbalancing
- 3W power dissipations

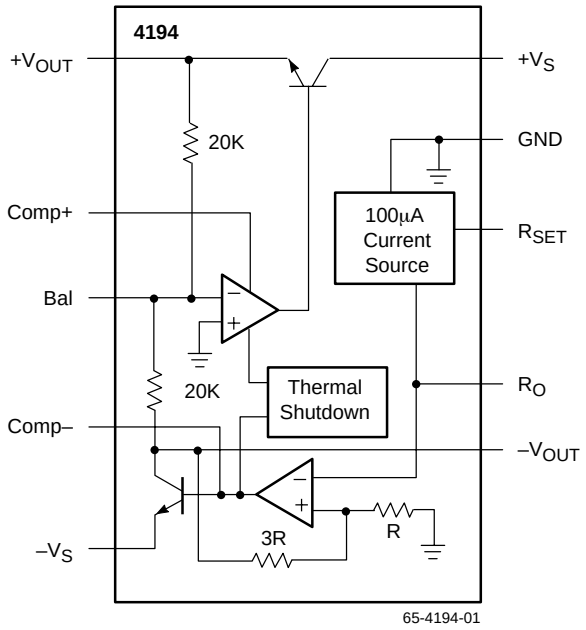
Description

The RC/RM4194 are dual polarity tracking regulators designed to provide balanced or unbalanced positive and negative output voltages at currents to 200 mA.
A single external resistor adjustment can be used to change both outputs between the limits of ±50 mV and ±42V.

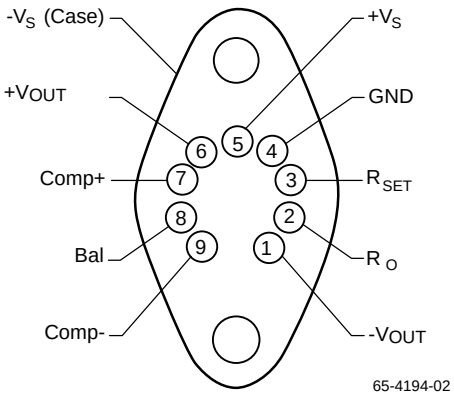
These devices are designed for local “on-card” regulation, eliminating distribution problems associated with single-point regulation. To simplify application the regulators require a minimum number of external parts.

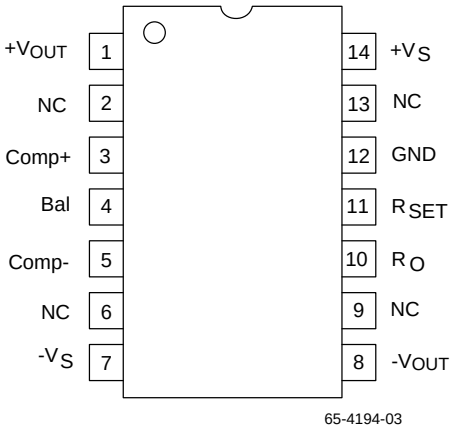
The device is available in three package types to accommodate various power requirements. The K (TO-66) power package can dissipate up to 3W at T_A = +25°C. The D 14-pin dual in-line will dissipate up to 1W and the N 14-pin dual in-line will dissipate up to 625 mW.

Block Diagram



Pin Assignments





Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min	Typ	Max	Units
Supply Voltage	RC4194			±35	V
	RM4194			±45	V
Supply Input to Output Voltage Differential	RC4194			±35	V
	RM4194			±45	V
Load Current	PDIP			100	mA
	CerDIP			150	mA
	TO-66 Metal Can			250	mA
$P_D T_A$ < 50°C	PDIP			468	mW
	CerDIP			1042	mW
	TO-66 Metal Can			2381	mW
Operating Temperature (T_j)	RC4194	0		70	°C
	RM4194	-55		125	°C
Storage Temperature		-65		150	°C
Junction Temperature	PDIP			125	°C
	CerDIP			175	°C
	TO-66 Metal Can			150	°C
Lead Soldering Temperature (60 seconds)				300	°C
For T_A > 50°C Derate at	TO-66 Metal Can		23.81		mW/°C
	PDIP		6.25		mW/°C
	CerDIP		8.38		mW/°C

Note:

1. Functional operation under any of these conditions is NOT implied.

Operating Conditions

Parameter			Min	Typ	Max	Units
θ_{JC}	Thermal Resistance	CerDIP		60		°C/W
		TO-66 Metal Can		7		°C/W
θ_{JA}	Thermal Resistance	PDIP		160		°C/W
		CerDIP		120		°C/W
		TO-66 Metal Can		42		°C/W

Electrical Characteristics

($\pm 5 \le V_{OUT} \le V_{MAX}$; $-V_{IN} \le -8V$; $I_L = \pm 1mA$; RM4194: $-55°C \le T_j \le +125°C$; RC4194: $0°C \le T_j \le +70°C$ unless otherwise specified)

Parameters	Test Conditions	Min	Typ	Max	Units
Line Regulation	$\Delta V_S = 0.1\ V_{IN}$		0.04	0.1	$\%V_{OUT}$
Load Regulation[1]	4194K: $I_L < 200$ mA 4194D: $I_L < 100$ mA $\pm V_S = \pm (V_{OUT} + 5)V$		0.002	0.004	$\%V_{OUT}/I_L$ (mA)
Output Voltage Drift With Temperature[2]					
Positive Output	$V_{OUT} = \pm 5V$		0.002	0.015	%/°C
Negative Output	$V_{OUT} = \pm 5V$		0.003	0.015	%/°C
Supply Current[3] (Positive)	$V_S = \pm V_{MAX}$, $V_{OUT} = 0V$, $I_L = 0$ mA		+0.8	+2.5	mA
Supply Current[4] (Negative)	$V_S = \pm V_{MAX}$, $V_{OUT} = 0V$, $I_L = 0$ mA		-1.8	-4.0	mA
Supply Voltage	RM4194	±9.5		±45	V
	RC4194	±9.5		±35	V
Output Voltage Scale Factor	$R_{SET} = 71.5\ k\Omega$, $T_j = +25°C$, $V_S = \pm V_{MAX}$	2.38	2.5	2.62	kΩ/V
Output Voltage Range	RM4194: $R_{SET} = 71.5\ k\Omega$, $I_L = 25$ mA	0.05		±42	V
	RC4194: $R_{SET} = 71.5\ k\Omega$, $I_L = 25$ mA	0.05		±42	V
Output Voltage Tracking			±0.4	±2.0	%
Ripple Rejection	F = 120 Hz, $T_j = +25°C$		70		dB
Input-Output Voltage Differential	$I_L = 50$ mA, $T_j = +25°C$	3.0			V
Short Circuit Current	$V_S = \pm 30V$, $T_j = +25°C$		300		mA
Output Noise Voltage	$C_L = 4.7\ \mu F$, $V_{OUT} = \pm 15V$, F = 10 Hz to 100 kHz		250		μV_{RMS}
Internal Thermal Shutdown			175		°C

Notes:

1. Measured as $\left(\frac{\Delta V_{OUT}}{V_{OUT}} \times 100\%\right)$ § I_L (mA)
2. Output voltage temperature drift guaranteed by design.
3. The current drain will increase by $50\mu A/V_{OUT}$ on positive side and $100\mu A/V_{OUT}$ on negative side.
4. The specifications above apply for the given junction temperatures since pulse test conditions are used.

Typical Performance Characteristics

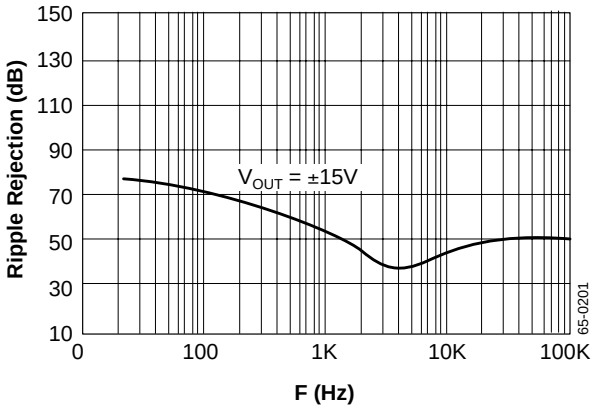


Figure 1. Ripple Rejection vs. Frequency

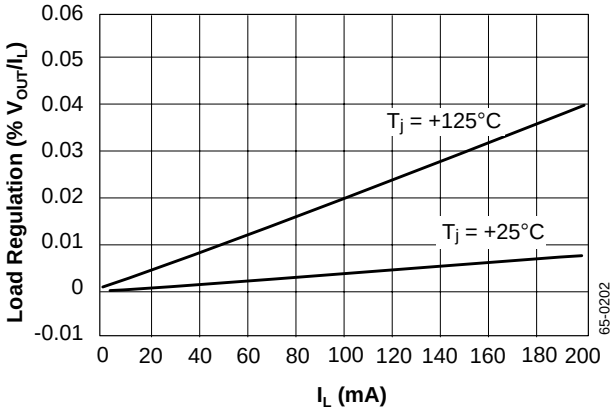
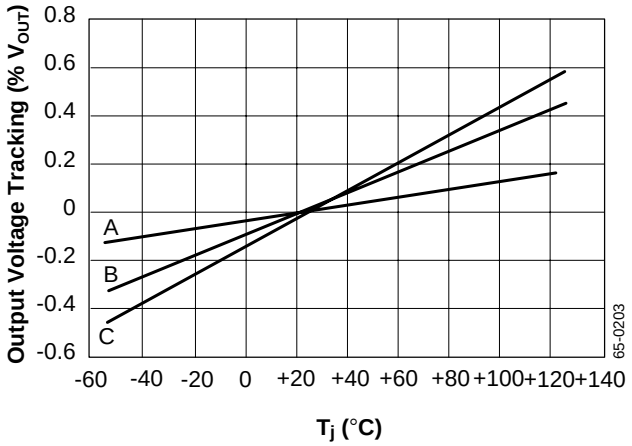


Figure 2. Load Regulation vs. Load Current



A = % Tracking of V_{OUT}
B = T.C. for Positive Regulator
C = T.C. for Negative Regulator

Figure 3. Output Voltage Tracking vs. Temperature

Typical Applications

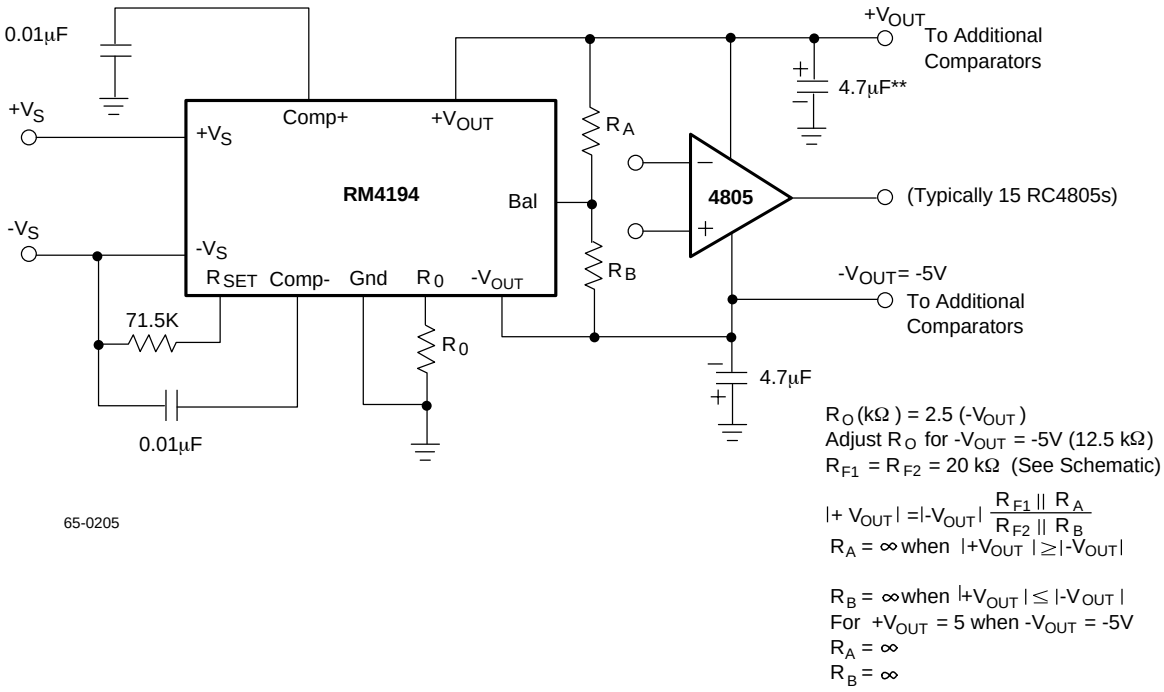
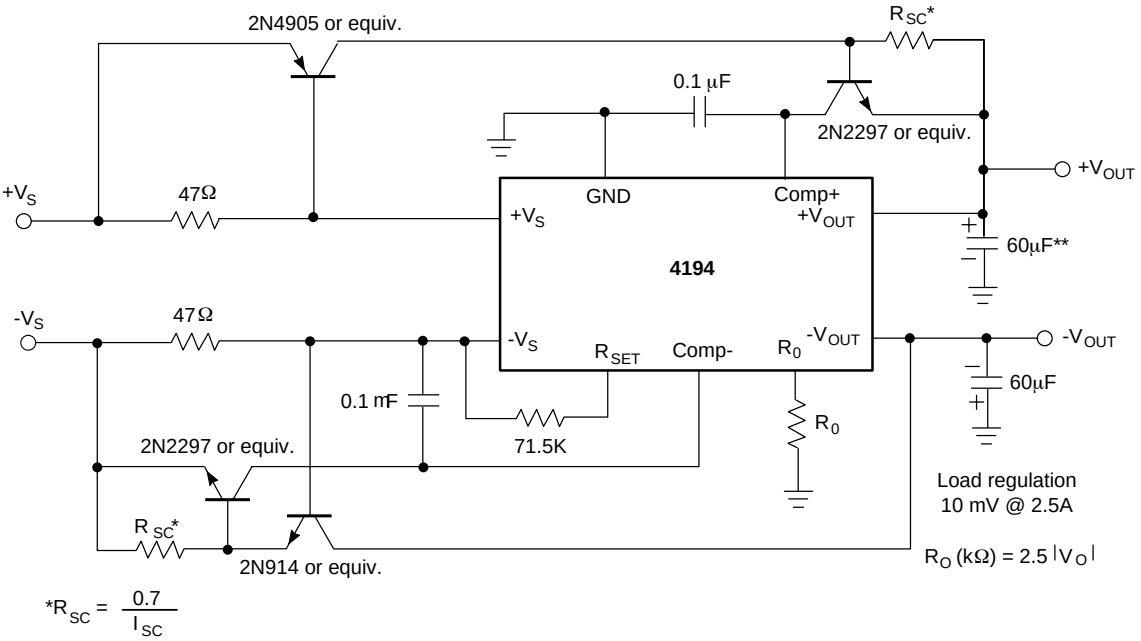


Figure 4. Unbalanced Output Voltage — Comparator Application



*$R_{SC} = \frac{0.7}{I_{SC}}$

**Optional usage - Not as critical as $-V_O$ bypass capacitors.

Note: Compensation and bypass capacitor connections should be close as posibe to the 4194

65-0206

Figure 5. High Output Application

Typical Applications (continued)

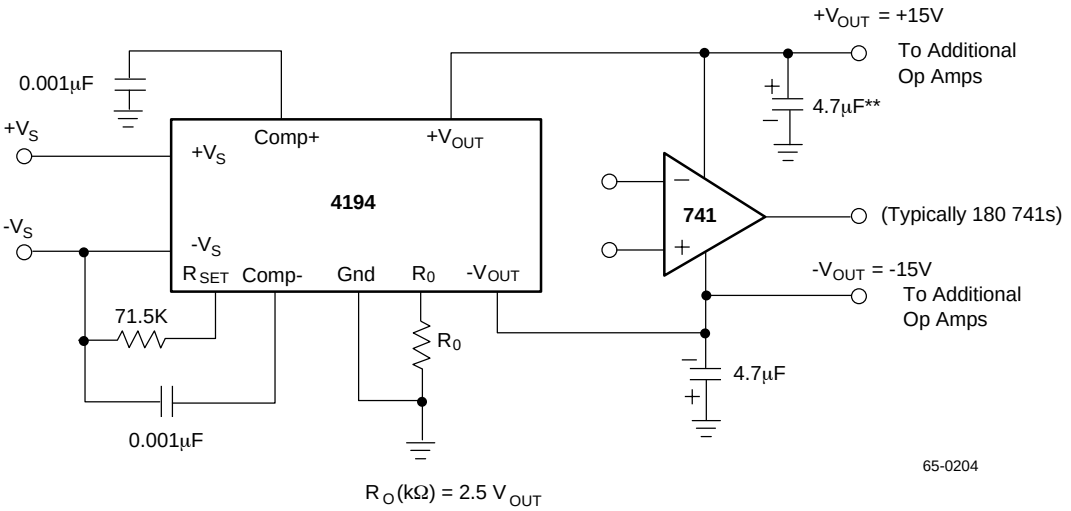


Figure 6. Balanced Output Voltage — Op Amp Application

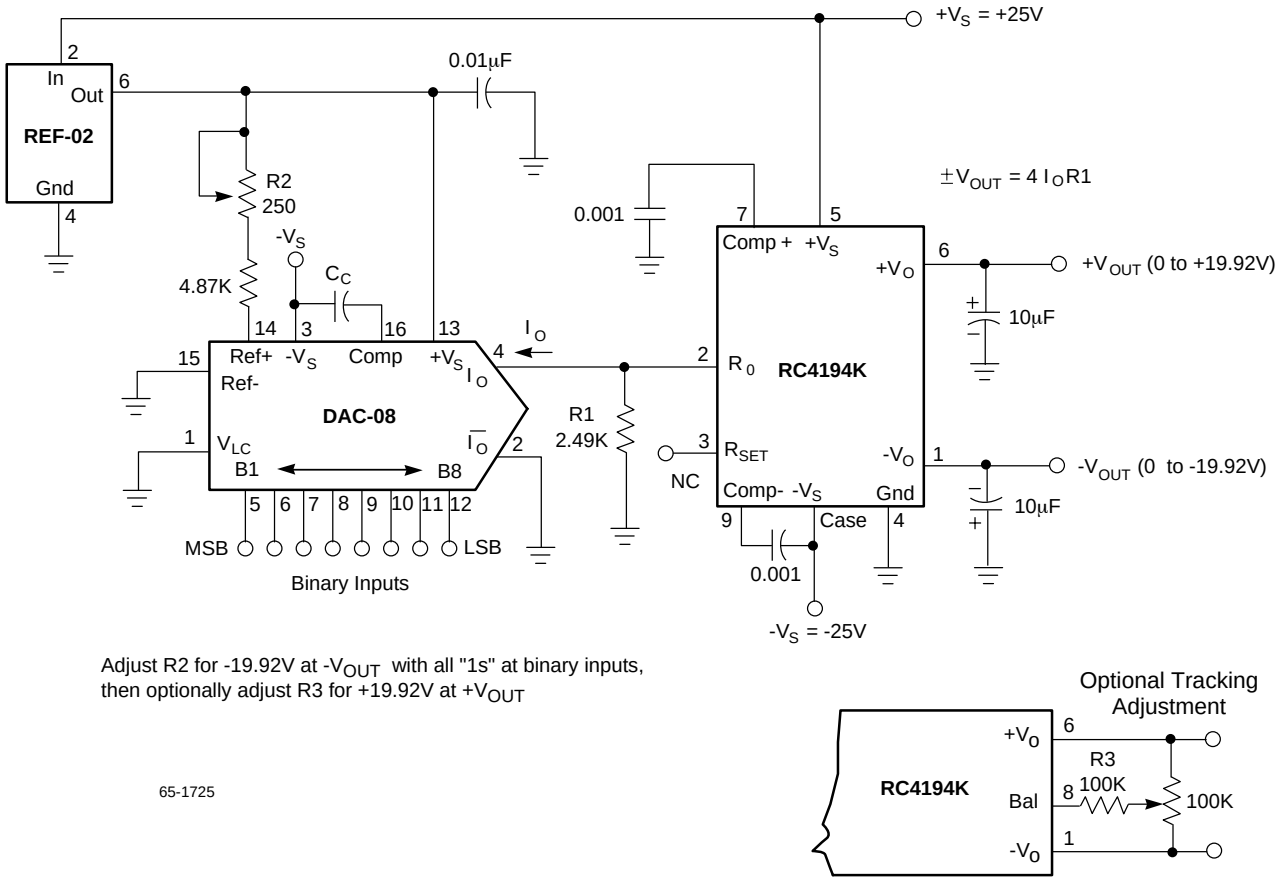


Figure 7. Digitally Controlled Dual 200 mA Voltage Regulator

RC4194 Switchable Power Supply

The outputs of the RC4194 can be simultaneously switched on or off under logic control as shown in Figure 8. In the "off" state, the outputs will be forced to a minimum voltage, or about ±20 mV, rather than becoming open-circuit. The turn-on time, with the outputs programmed to ±12V, is approximately 200 μS. This circuit works by forcing the R0 pin to ground with an analog switch.

Refer to the RC4194 internal schematic diagram. A reference voltage that regulates with respect to $-V_S$ is generated at the RSET pin by the zener diode Q12 and the buffer circuit of Q11 and Q13. When the external 71.5k RSET resistor is connected between the R_{SET} pin and $-V_S$, a precision current of 100 μA is generated which then flows into Q13's collector. Since Q13's collector is tied to the R0 pin, the 100 μA current will develop a ground-referenced voltage drop proportional to the value of R0, which is then amplified by the internal error amplifier. When the analog switch in Figure 8 turns on, it effectively shorts out R0 and causes 0V to be applied to the error amplifier. The output voltage in the off state will be approxi-mately ±20 mV. If a higher value (50 to 100 mV) is acceptable, then the DG201 analog switch can be replaced with a low-cost small signal transistor, as shown in the alternate switch configuration.

Compensation

For most applications, the following compensation technique is sufficient. The positive regulator section of the RC4194 is compensated by a 0.001 μF ceramic disc capacitor from the Comp+ terminal to ground. The negative regulator requires compensation at two points. The first is the Comp– pin, which should have 0.001 μF to the $-V_S$ pin, or case. A ceramic disc is ideal here. The second compen-sation point for the negative side is the $-V_{OUT}$ terminal, which ideally should be a 4.7 μF solid tantalum capacitor with enough reserve voltage capacity to avoid the momentary shorting and reforming which can occur with tantalum caps. For systems where the cost of a solid tantalum capacitor cannot be justified, it is usually sufficient to use an aluminum capacitor with a 0.03 μF ceramic disc in parallel to bypass high frequencies. In addition, if the rectifier filter capacitors have poor high frequency characteristics (like aluminum electrolytics) or if any impedance is in series with the $+V_S$ and $-V_S$ terminals, it is necessary to bypass these two points with 0.01 μF ceramic disc capacitors. Just as with monolithic op amps, some applications may not require these bypass caps, but if in doubt, be sure to include them.

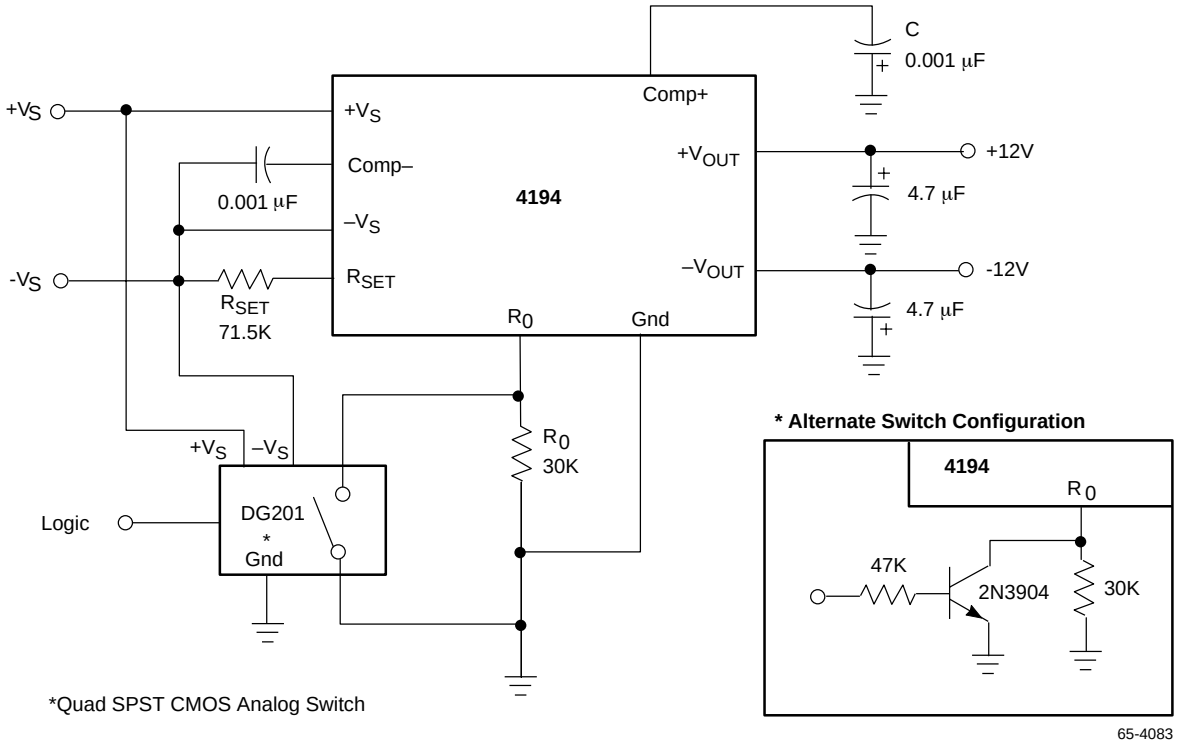


Figure 8. ±12V Switchable Power Supply

All compensation and bypass caps should have short leads, solid grounds, and be located as close to the 4194 as possible. Refer to Figure 9 for recommended compensation circuitry.

Protection

In systems using monolithic voltage regulators, a number of conditions can exist which, left uncorrected, will destroy the regulator. Fortunately, regulators can easily be protected against these potentially destructive conditions. Monolithic regulators can be destroyed by any reversal of input or output voltage polarity, or if the input voltage drops below the output voltage in magnitude. These conditions can be caused by inductive loads at the inputs or outputs of the regulator. Other problems are caused by heavy loads at the unregulated inputs to the regulator, which might cause the input voltage to drop below the output voltage at turn-off. If any of the preceding problem conditions are present in your system, it is recommended that you protect the regulator using diodes. These diodes should be high speed types capable of handling large current surges. Figure 10 shows all six of the possible protection diodes. The diodes at the inputs and outputs prevent voltages at those points from becoming reversed. Diodes from outputs to inputs prevent the output voltage from exceeding the input voltage. Chances are that the system under consideration will not require all six diodes, but if in doubt, be sure to include them.

Brownout Protection

The RC4194 is one of the most easily applied and trouble-free monolithic ICs available. When used within the data sheet ratings (package power dissipation, maximum output current, minimum and maximum input voltages) it provides the most cost-effective source of regulated ±15V for powering linear ICs.

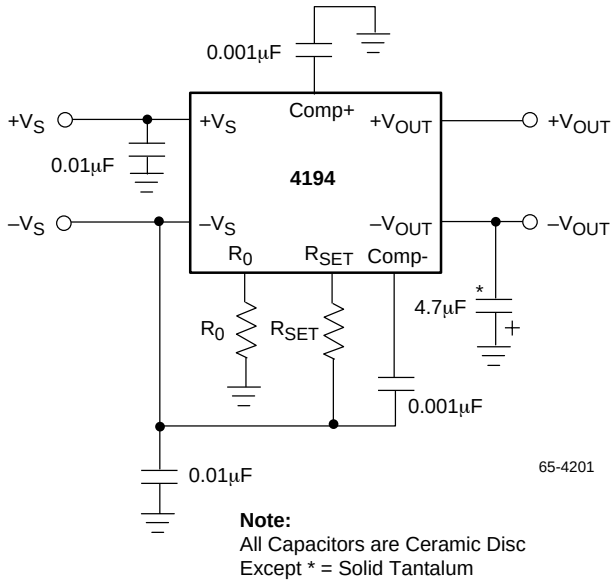


Figure 9. RC4194 Recommended Compensation

Sometimes occasions arise in which the RC4194 ratings must be exceeded. One example is the “brownout.” During a brownout, line voltages may be reduced to as low as 75 VRMS, causing the input voltage to the RC4194 to drop below the minimum dropout voltage. When this happens, the negative output voltage can go to positive. The maximum amount of current available is approximately 5 mA.

In general this is not enough current to damage most ICs which the RC4194 might be supplying, but it is a potentially destructive condition. Fortunately, it is easy to protect against. As shown in the typical application circuit in Figure 11, a diode, D, can be connected to the negative output.

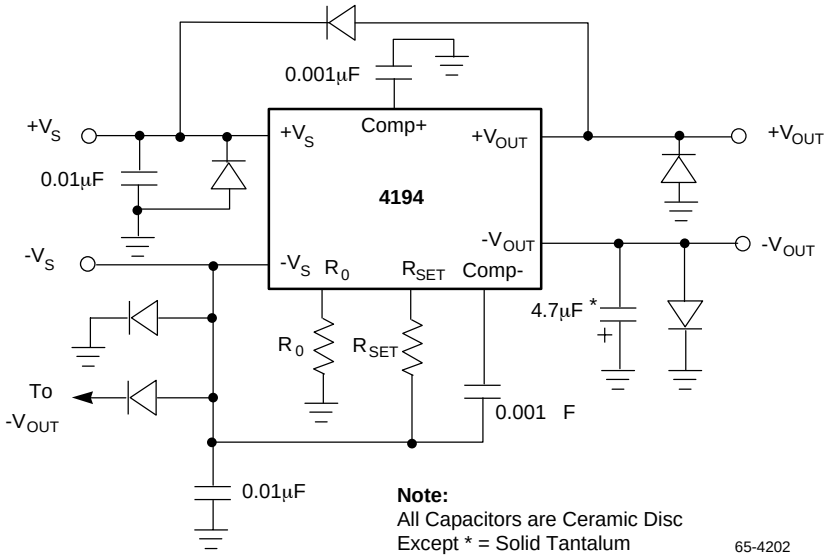


Figure 10. RC4194 Regulator Showing All Protective Diodes

If a small signal silicon diode is used, it will clamp the negative output voltage at about +0.55V. A Schottky barrier or germanium device would clamp the voltage at about +0.3V. Another cure which will keep the negative output negative at all times is the 1 mΩ resistor connected between the +15V output and the Comp- terminal. This resistor will then supply drive to the negative output transistor, causing it to saturate to -1V during the brownout.

Heatsinking

Voltage Regulators are power devices which are used in a wide range of applications.

When operating these devices near their extremes of load current, ambient temperature and input-output differential, consideration of package dissipation becomes important to avoid thermal shutdown at 175°C. The RC4194 has this feature to prevent damage to the device. It typically starts affecting load regulation approximately 2°C below 175°C. To avoid shutdown, some form of heatsinking should be used or one of the above operating conditions would need to be derated.*

The following is the basic equation for junction temperature:

$$T_J = T_A + P_D\theta_{J-A}$$

Equation 1

where

T_J = junction temperature (°C)

T_A = ambient air temperature (°C)

P_D = power dissipated by device (W)

$\theta_{J\text{-}A}$ = thermal resistance from junction to ambient air (°C/W)

The power dissipated by the voltage regulator can be detailed as follows:

$$P_D = (V_{IN} - V_{OUT}) \times I_O + V_{IN} \times I_Q$$

Equation 2

where

V_{IN} = input voltage

V_{OUT} = regulated output voltage

I_O = load current

I_Q = quiescent current drain

Let's look at an application where a user is trying to determine whether the RC4194 in a high temperature environment will need a heatsink.

Given:

T_J at thermal shutdown = 150°C

T_A = 125°C

$\theta_{J\text{-}A}$ = 41.6°C/W, K (TO-66) pkg.

V_{IN} = 40V

V_{OUT} = 30V

I_Q = 1 mA + 75 μA/V_{OUT} x 30V
= 3.25 mA*

$$\theta_{J-A} = \frac{T_J - T_A}{P_D}$$

$$P_D = \frac{T_J - T_A}{\theta_{J-A}}$$

$$= (V_{IN} - V_{OUT}) \times I_O + V_{IN} \times I_Q$$

Solve for I_O,

$$I_O = \frac{T_J - T_A}{\theta_{J-A}(V_{IN} - V_{OUT})} - \frac{V_{IN} \times I_Q}{(V_{IN} - V_{OUT})}$$

$$I_O = \frac{150°C - 125°C}{41.6°C/W \times 10V} - \frac{40 \times 3.25 \times 10^{-3}}{10}$$

= 60 mA – 13 mA ~ 47 mA

If this supply current does not provide at least a 10% margin under worst case load conditions, heatsinking should be employed. If reliability is of prime importance, the multiple regulator approach should be considered.

In Equation 1, $\theta_{J\text{-}A}$ can be broken into the following components:

$\theta_{J\text{-}A} = \theta_{J\text{-}C} + \theta_{C\text{-}S} + \theta_{S\text{-}A}$

where

$\theta_{J\text{-}C}$ = junction-to-case thermal resistance

$\theta_{C\text{-}S}$ = case-to-heatsink thermal resistance

$\theta_{S\text{-}A}$ = heatsink-to-ambient thermal resistance

*The current drain will increase by 50μA/V_{OUT} on positive side and 100μA/V_{OUT} on negative side

In the above example, let's say that the user's load current is 200 mA and he wants to calculate the combined $\theta_{C\text{-}S}$ and $\theta_{S\text{-}A}$ he needs:

Given: I_O = 200 mA,

$$\theta_{J-A} = \frac{T_J - T_A}{(V_{IN} - V_{OUT}) \times I_O + V_{IN} \times I_Q}$$

$$= \frac{50°C - 125°C}{10V \times 200mA + 40 \times 3.25 \times 10^{-3}}$$

= 11.75°C/W

Given $\theta_{J\text{-}C}$ = 7.15°C/W for the 4194 in the K package,

$\theta_{C\text{-}S} + \theta_{S\text{-}A}$ = 11.75°C/W – 7.15°C/W

= 4.6°C/W

When using heatsink compound with a metal-to-metal interface, a typical $\theta_{C\text{-}S}$ = 0.5°C/W for the K package. The remaining $\theta_{S\text{-}A}$ of approximately 4°C/W is a large enough thermal resistance to be easily provided by a number of heatsinks currently available. Table 1 is a brief selection guide to heatsink manufacturers.

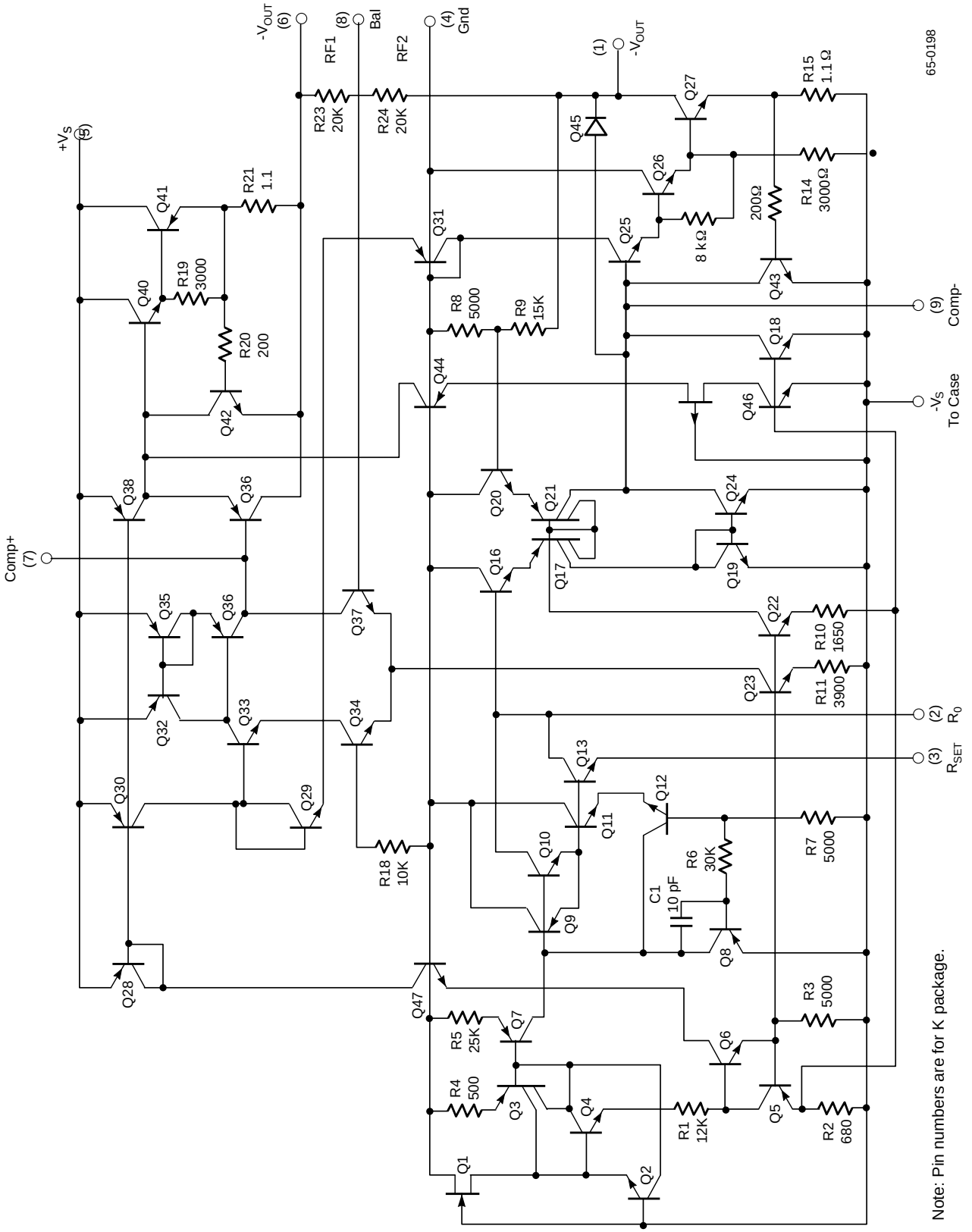
Table 1. Commercial Heatsink Selection Guide

No attempt has been made to provide a complete list of all heatsink manufacturers. This list is only representative.

$\theta_{S\text{-}A}$[1](°C/W)	Manufacturer/Series or Part Number
TO-66 Package	
0.31 – 1.0	Thermalloy — 6441, 6443, 6450, 6470, 6560, 6590, 6660, 6690
1.0 – 3.0	Wakefield — 641
	Thermalloy — 6123, 6135, 6169, 6306, 6401, 6403, 6421, 6423, 6427, 6442, 6463, 6500
3.0 – 5.0	Wakefield — 621, 623
	Thermalloy — 6606, 6129, 6141, 6303
	IERC — HP
	Staver — V3-3-2
5.0 – 7.0	Wakefield — 690
	Thermalloy — 6002, 6003, 6004, 6005, 6052, 6053, 6054, 6176, 6301
	IERC — LB
	Staver— V3-5-2
7.0 – 10.0	Wakefield — 672
	Thermalloy — 6001, 6016, 6051, 6105, 6601
	IERC — LA, uP
	Staver — V1-3, V1-5, V3-3, V3-5, V3-7
10.0 – 25.0	Thermalloy — 6-13, 6014, 6015, 6103, 6104, 6105, 6117
Dual In-line Package	
20	Thermalloy — 6007
30	Thermalloy — 6010
32	Thermalloy — 6011
34	Thermalloy — 6012
45	IERC — LI
60	Wakefield — 650, 651

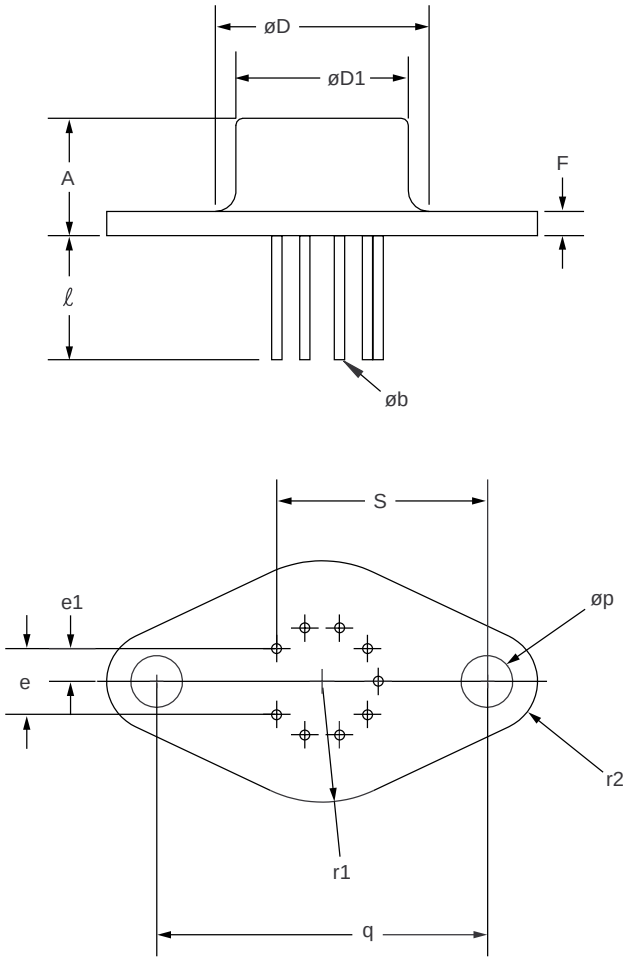
Staver Co., Inc.: 41-51 N Saxon Ave., Bay Shore, NY 11706
IERC: 135 W Magnolia Blvd., Burbank, CA 91502
Thermalloy: P.O. Box 34829, 2021 W Valley View Ln., Dallas, TX
Wakefield Engin Ind: Wakefield, MA 01880
* All values are typical as given by manufacturer or as determined from characteristic curves supplied by manufacturer.

Simplified Schematic Diagram



Mechanical Dimensions

9-Lead Metal Can IC Header Package



Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.250	.340	6.35	8.64	
øb	.028	.034	.71	.86	1
øD	—	.620	—	15.75	
øD1	.470	.500	11.94	12.70	
e	.190	.210	4.83	5.33	
e1	.093	.107	2.36	2.72	
F	.050	.075	1.27	1.91	
ℓ	.360	—	9.14	—	
øp	.142	.152	3.61	3.86	
q	.958	.962	24.33	24.43	
r1	—	.350	—	8.89	
r2	—	.145	—	3.68	
S	.570	.590	14.48	14.99	

Notes:

1. All leads—increase maximum limit by .003 (.08mm) when lead finish is applied.

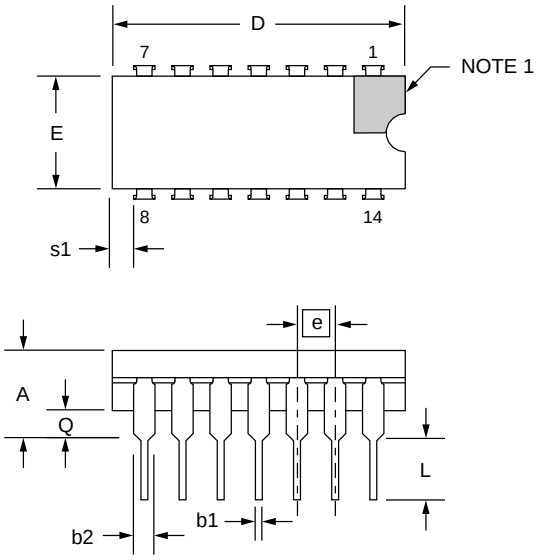
Mechanical Dimensions (continued)

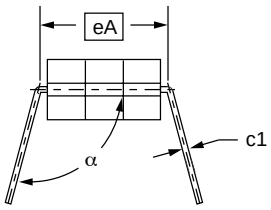
14-Lead Ceramic DIP Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2
c1	.008	.015	.20	.38	8
D	—	.785	—	19.94	4
E	.220	.310	5.59	7.87	4
e	.100 BSC		2.54 BSC		5, 9
eA	.300 BSC		7.62 BSC		7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 7, 8 and 14 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 14.
6. Applies to all four corners (leads number 1, 7, 8, and 14).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Twelve spaces.





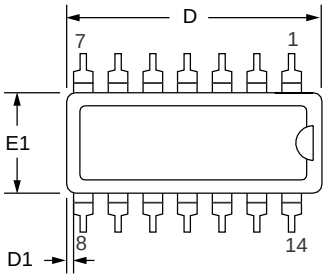
Mechanical Dimensions (continued)

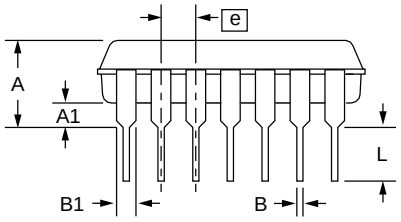
14-Lead Plastic DIP Package

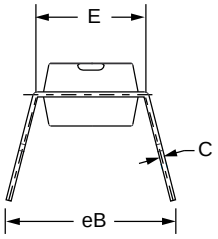
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	.725	.795	18.42	20.19	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.200	2.92	5.08	
N	14		14		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are shown for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.







Ordering Information

Product Number	Temperature Range	Screening	Package	SMD Number
RC4194N	0° to +70°C	Commercial	14 pin Plastic DIP	
RC4194D	0° to +70°C	Commercial	14 pin Ceramic DIP	
RC4194K	0° to +70°C	Commercial	9 pin TO-66	
RM4194D	-55°C to +125°C	Commercial	14 pin Ceramic DIP	
RM4194D/883B	-55°C to +125°C	Military	14 pin Ceramic DIP	7705401CA
RM4194K	-55°C to +125°C	Commercial	9 pin TO-66	

Note:

1. /883B suffix denotes MIL-STD-883, Par. 1.2.1 compliant device.

RC4195

Fixed ±15V Dual Tracking Voltage Regulator

Features

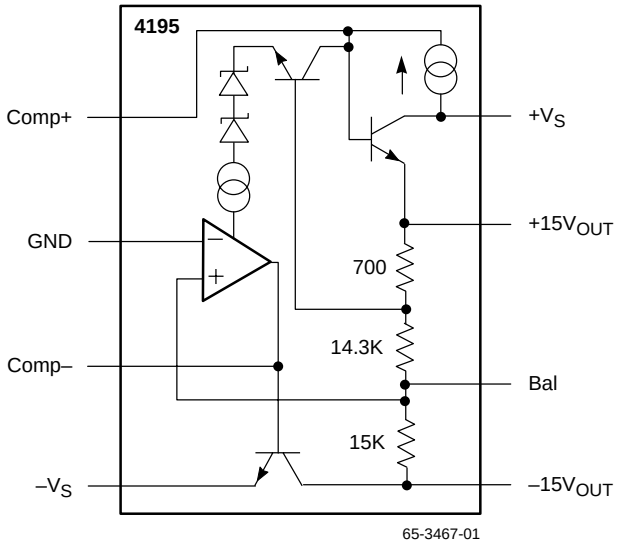
- ±15V operational amplifier power at reduced cost and component density
- Thermal shutdown at T_J = +175°C in addition to short circuit protection
- Output currents to 100 mA
- May be used as single output regulator with up to +50V output
- Available in TO-66, TO-99 and 8-lead mini-DIP

Description

The RM/RC4195 is a dual polarity tracking regulator designed to provide balanced positive and negative 15V output voltages at currents up to 100mA. This device is designed for local "on-card" regulation, eliminating distribution problems associated with single point regulation. The regulator is intended for ease of application. Only two external components are required for operation (two 10 μF bypass capacitors).

The device is available in four package types to accommodate various applications requiring economy, high power, dissipation, and reduced component density.

Block Diagram



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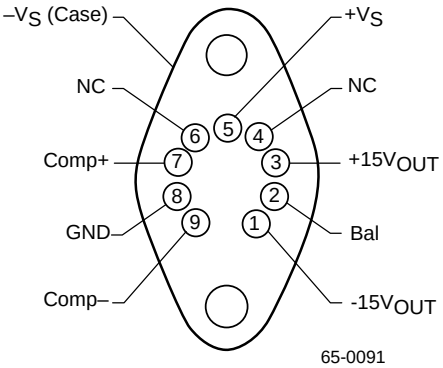
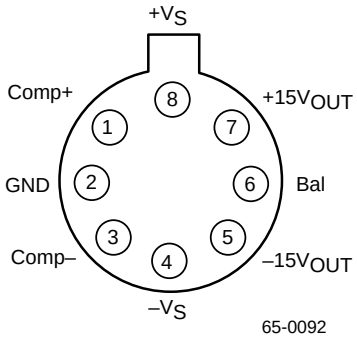
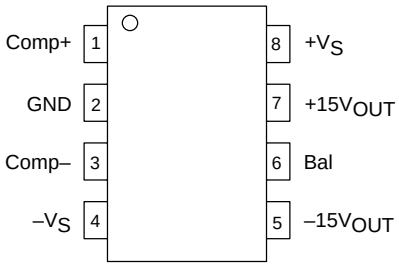
Pin Assignments



65-0091



65-0092



65-0093

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min	Typ	Max	Units
Supply Voltage ($\pm V_S$) to Ground				±30	V
Load Current	PDIP/TO-99			150	mA
	TO-66			100	mA
$P_D T_A$ < 50°C	PDIP			468	mW
	TO-99			658	mW
	TO-66			2381	mW
Junction Temperature	PDIP			125	°C
	TO-99			175	°C
	TO-66			150	°C
Storage Temperature		-65		150	°C
Operating Temperature (T_j)	RC4195	0		70	°C
	RM4195	-55		125	°C
Lead Soldering Temperature (60 sec)				300	°C
For T_A > 50°C Derate at	PDIP		6.25		mW/°C
	TO-99		5.26		mW/°C
	TO-66		23.81		mW/°C

Note:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter			Min	Typ	Max	Units
θ_{JC}	Thermal resistance	TO-99		50		°C/W
		TO-66		7		°C/W
θ_{JA}	Thermal resistance	PDIP		160		°C/W
		TO-99		190		°C/W
		TO-66		42		°C/W

Electrical Characteristics

(I_L = ±1mA; V_S = ± 20V, C_L = 10μF; RM4195: -55°C ≤ T_j ≤ +125°C; RC4195: 0°C ≤ T_j ≤ +70°C unless otherwise specified)[1]

Parameters	Test Conditions	Min	Typ	Max	Units
Line Regulation	V_S = ±18V to ±30V		2	20	mV
Load Regulation	I_L = 1mA to 100mA		5	30	mV
Output Voltage Drift With Temperature			0.005	0.015	%/°C
Supply Current	V_S = ±30V, I_L = 0 mA		±1.5	±4.0	mA
Supply Voltage		±18		±30	V
Output Voltage	T_j = +25°C	14.5	15.0	15.5	V
Output Voltage Tracking			±50	±300	mV
Ripple Rejection	F = 120 Hz, T_A = +25°C		75		dB
Input-Output Voltage Differential	I_L = 50 mA	3.0			V
Short Circuit Current	T_j = +25°C		220		mA
Output Noise Voltage	T_j = +25°C, F = 100Hz to 120 kHz		60		μV_{RMS}
Internal Thermal Shutdown			175		°C

Note:

1. The specifications above apply for the given junction temperatures since pulse test conditions are used.

Typical Performance Characteristics

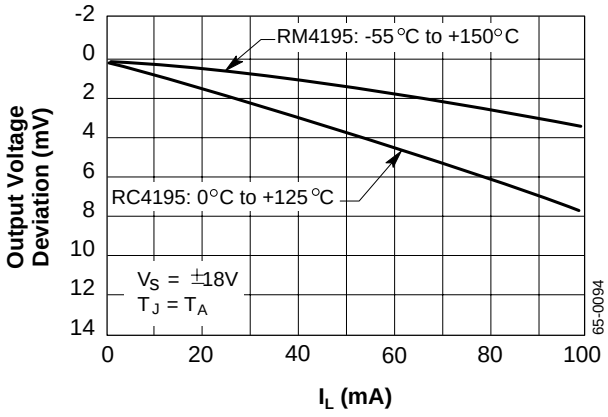


Figure 1. Output Load Regulation

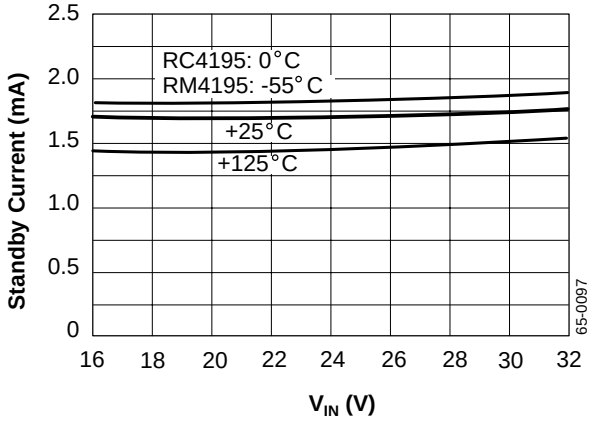


Figure 2. Standby Current Drain

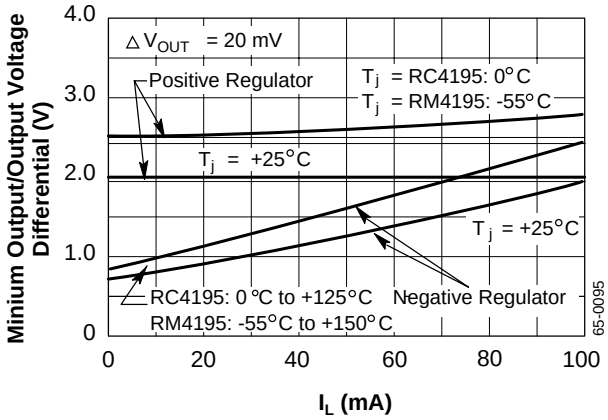


Figure 3. Regulator Dropout Voltage

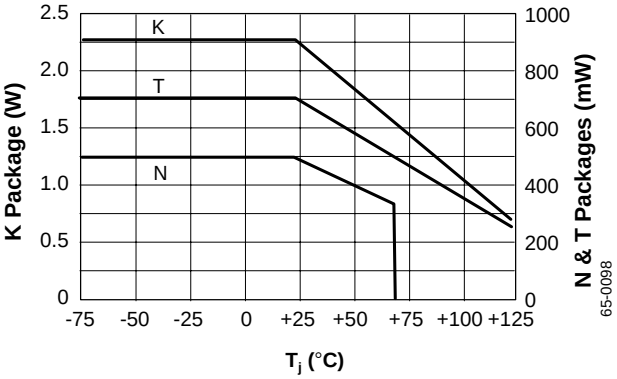


Figure 4. Power Dissipation

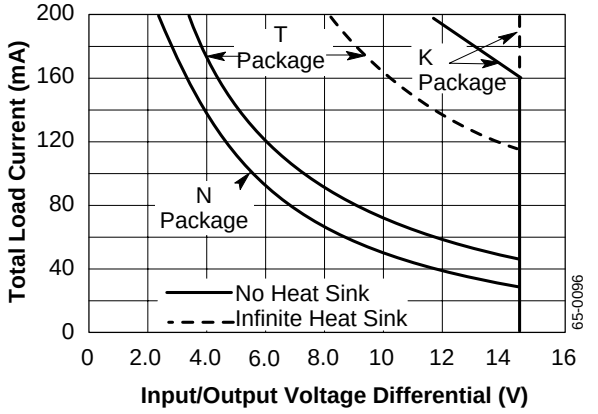


Figure 5. Maximum Current Capability

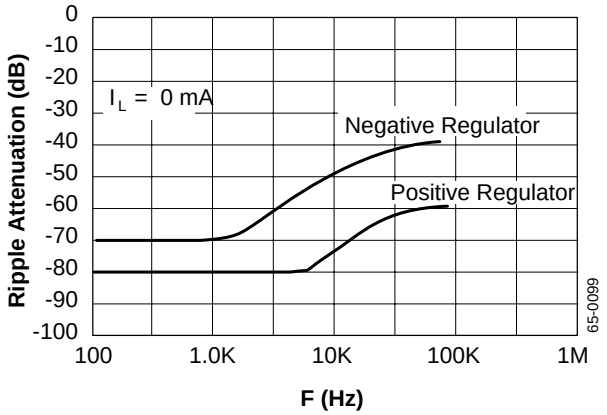


Figure 6. Ripple Rejection

Typical Applications

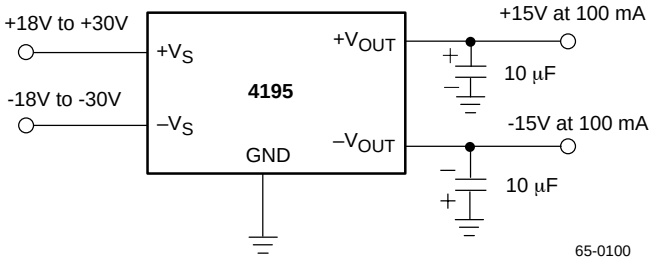


Figure 7. Balanced Output (V_{OUT} = ±15V)

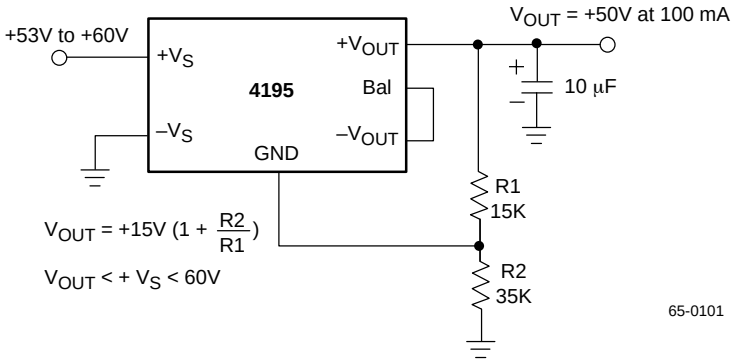


Figure 8. Positive Single Supply (+15V < V_{OUT} < +50V)

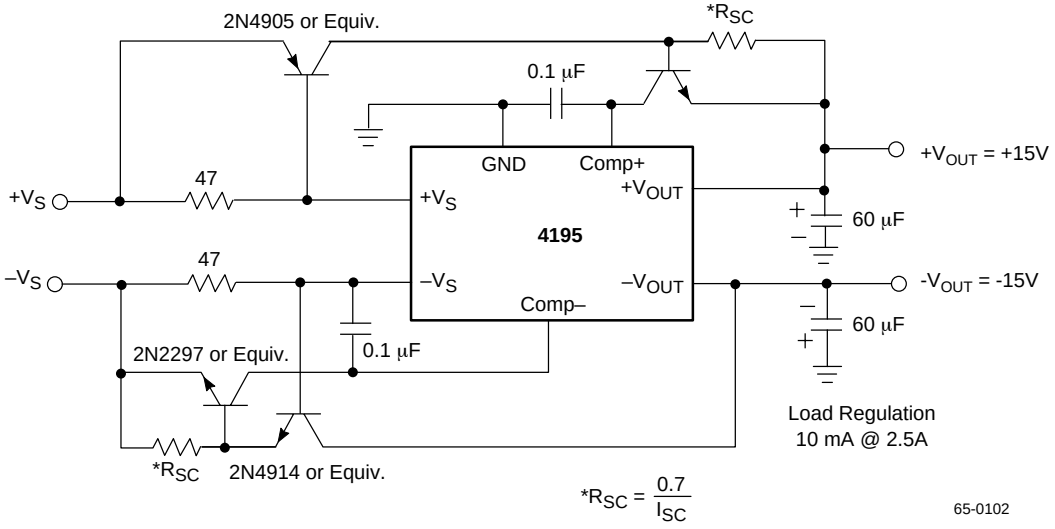


Figure 9. High Output Current

Brownout Protection

The RC4195 is one of the most easily applied and trouble-free monolithic ICs available. When used within the data sheet ratings (package power dissipation, maximum output current, minimum and maximum input voltages) it provides the most cost-effective source of regulated ±15V for powering linear ICs.

Sometimes occasions arise in which the RC4195 ratings must be exceeded. One example is the "brownout". During a brownout, line voltages may be reduced to as low as 75 V_{RMS}, causing the input voltage to the RC4195 to drop below the minimum dropout voltage. When this happens, the negative output voltage can go to positive. The maximum amount of current available is approximately 5 mA.

In general this is not enough current to damage most ICs which the RC4195 might be supplying, but it is a potentially destructive condition. Fortunately, it is easy to protect against. As shown in the typical application circuit, a diode, D, can be connected to the negative output.

If a small signal silicon diode is used, it will clamp the negative output voltage at about +0.55V. A Schottky barrier or germanium device would clamp the voltage at about +0.3V. Another cure which will keep the negative output negative all times is the 1 mΩ resistor connected between the +15V output and the Comp– terminal. this resistor will then supply drive to the negative output transistor, causing it to saturate to -1V during the brownout.

Heatsinking

When operating these devices near their extremes of load current, ambient temperature and input-output differential, consideration of package dissipation becomes important to avoid thermal shutdown at 175°C. The RC4195 has this feature to prevent damage to the device. It typically starts affecting load regulation approximately 2°C below 175°C. To avoid shutdown, some form of heatsinking should be used or one of the above operating conditions would need to be derated.*

The following is the basic equation for junction temperature:

$$T_J = T_A + P_D\theta_{J-A}$$

Equation 1

where

T_J = junction temperature (°C)

T_A = ambient air temperature (°C)

P_D = power dissipated by device (W)

$\theta_{J\text{-}A}$ = thermal resistance from junction to ambient air (˚C/W)

The power dissipated by the voltage regulator can be detailed as follows:

$$P_D = (V_{IN} - V_{OUT}) \times I_O + V_{IN} \times I_Q$$

Equation 2

where

V_{IN} = input voltage

V_{OUT} = regulated output voltage

I_O = load current

I_Q = quiescent current drain

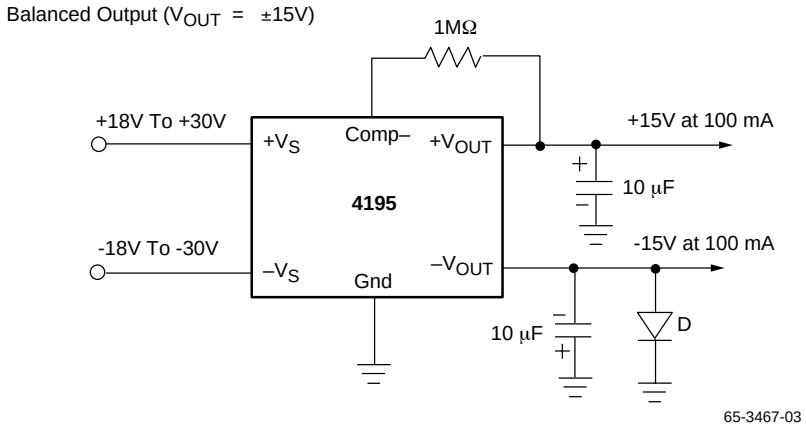


Figure 10. Typical Application Circuit

*In allowing for process deviations, the user should work with a maximum allowable function temperature of 150°C.
**The current drain will increase by 50µA/V_{OUT} on positive side and 100µA/V_{OUT} on negative side

Let's look at an application where a user is trying to determine whether the RC4195 in a high temperature environment will need a heatsink.

Given:

T_J at thermal shutdown = 150°C

T_A = 125°C

$\theta_{J\text{-}A}$ = 41.6°C/W, K (TO-66) pkg.

V_{IN} = 40V

V_{OUT} = 30V

I_Q = 1 mA + 75 μA/V_{OUT} x 30V
= 3.25 mA**

$$\theta_{J-A} = \frac{T_J - T_A}{P_D}$$

$$P_D = \frac{T_J - T_A}{\theta_{J-A}}$$

$$= (V_{IN} - V_{OUT}) \times I_O + V_{IN} \times I_Q$$

Solve for I_O,

$$I_O = \frac{T_J - T_A}{\theta_{J-A}(V_{IN} - V_{OUT})} - \frac{V_{IN} \times I_Q}{(V_{IN} - V_{OUT})}$$

$$I_O = \frac{150°C - 125°C}{41.6°C/W \times 10V} - \frac{40 \times 3.25 \times 10^{-3}}{10}$$

= 60 mA – 13 mA ~ 47 mA

If this supply current does not provide at least a 10% margin under worst case load conditions, heatsinking should be employed. If reliability is of prime importance, the multiple regulator approach should be considered.

In Equation 1, $\theta_{J\text{-}A}$ can be broken into the following components:

$$\theta_{J\text{-}A} = \theta_{J\text{-}C} + \theta_{C\text{-}S} + \theta_{S\text{-}A}$$

where

$\theta_{J\text{-}C}$ = junction-to-case thermal resistance

$\theta_{C\text{-}S}$ = case-to-heatsink thermal resistance

$\theta_{S\text{-}A}$ = heatsink-to-ambient thermal resistance

In the above example, let's say that the user's load current is 200 mA and he wants to calculate the combined $\theta_{C\text{-}S}$ and $\theta_{S\text{-}A}$ he needs:

Given: I_O = 200 mA,

$$\theta_{J-A} = \frac{T_J - T_A}{(V_{IN} - V_{OUT}) \times I_O + V_{IN} \times I_Q}$$

$$= \frac{50°C - 125°C}{10V \times 200mA + 40 \times 3.25 \times 10^{-3}}$$

= 11.75°C/W

Given $\theta_{J\text{-}C}$ = 7.15°C/W for the 4194 in the K package,

$\theta_{C\text{-}S} + \theta_{S\text{-}A}$ = 11.75°C/W – 7.15°C/W

= 4.6°C/W

When using heatsink compound with a metal-to-metal interface, a typical $\theta_{C\text{-}S}$ = 0.5°C/W for the K package. The remaining $\theta_{S\text{-}A}$ of approximately 4°C/W is a large enough thermal resistance to be easily provided by a number of heatsinks currently available. Table 1 is a brief selection guide to heatsink manufacturers.

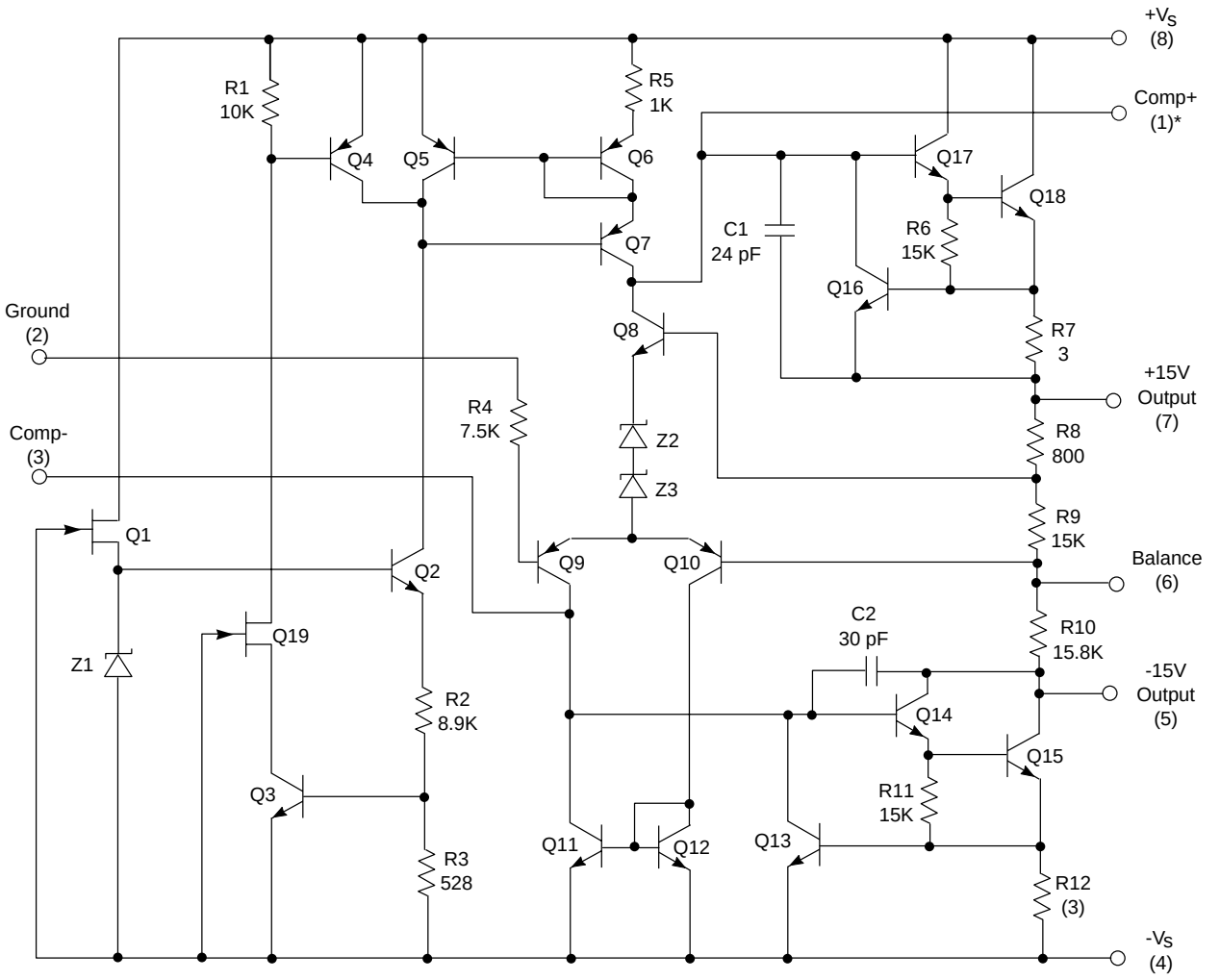
Table 1. Commercial Heatsink Selection Guide

No attempt has been made to provide a complete list of all heatsink manufacturers. This list is only representative.

θ_{S-A}* (°C/W)	Manufacturer/Series or Part Number
TO-66 Package	
0.31 – 1.0	Thermalloy — 6441, 6443, 6450, 6470, 6560, 6590, 6660, 6690
1.0 – 3.0	Wakefield — 641
	Thermalloy — 6123, 6135, 6169, 6306, 6401, 6403, 6421, 6423, 6427, 6442, 6463, 6500
3.0 – 5.0	Wakefield — 621, 623
	Thermalloy — 6606, 6129, 6141, 6303
	IERC — HP
	Staver — V3-3-2
5.0 – 7.0	Wakefield — 690
	Thermalloy — 6002, 6003, 6004, 6005, 6052, 6053, 6054, 6176, 6301
	IERC — LB
	Staver— V3-5-2
7.0 – 10.0	Wakefield — 672
	Thermalloy — 6001, 6016, 6051, 6105, 6601
	IERC — LA, uP
	Staver — V1-3, V1-5, V3-3, V3-5, V3-7
10.0 – 25.0	Thermalloy — 6-13, 6014, 6015, 6103, 6104, 6105, 6117
TO-99 Package	
12.0 – 20.0	Wakefield — 260
	Thermalloy — 1101, 1103
	Staver — V3A-5
20.0 – 30.0	Wakefield — 209
	Thermalloy — 1116, 1121, 1123, 1130, 1131, 1132, 2227, 3005
	IERC — LP
	Staver — F5-5
3.0 – 50.0	Wakefield — 207
	Thermalloy — 2212, 2215, 225, 2228, 2259, 2263, 2264
Dual In-line Package	
20	Thermalloy — 6007
30	Thermalloy — 6010
32	Thermalloy — 6011
34	Thermalloy — 6012
45	IERC — LI
60	Wakefield — 650, 651

Staver Co., Inc.: 41-51 N Saxon Ave., Bay Shore, NY 11706
IERC: 135 W Magnolia Blvd., Burbank, CA 91502
Thermalloy: P.O. Box 34829, 2021 W Valley View Ln., Dallas, TX
Wakefield Engin Ind: Wakefield, MA 01880
* All values are typical as given by manufacturer or as determined from characteristic curves supplied by manufacturer.

Simplified Schematic Diagram



*Pin numbers are for 8-pin packages.

65-0090

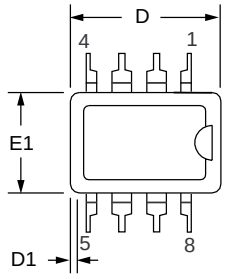
Mechanical Dimensions

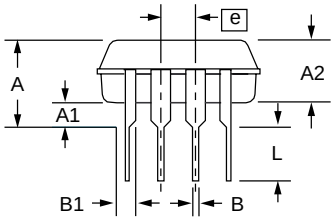
8-Lead Plastic DIP Package

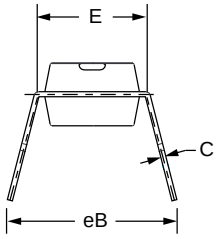
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	.348	.430	8.84	10.92	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.160	2.92	4.06	
N	8°		8°		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.

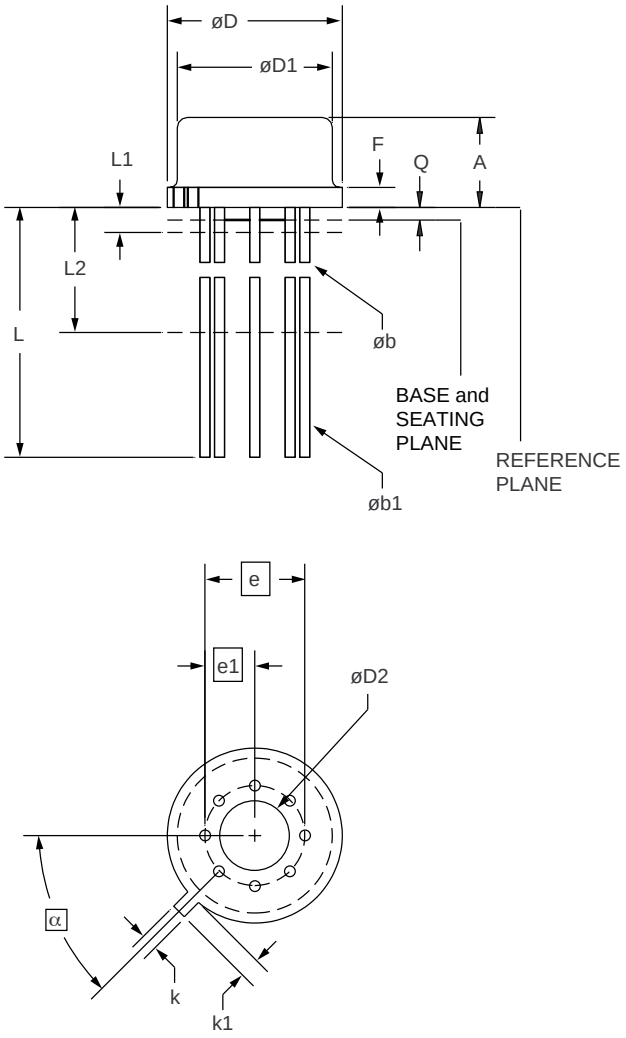






Mechanical Dimensions (continued)

8-Lead Metal Can IC Header Package



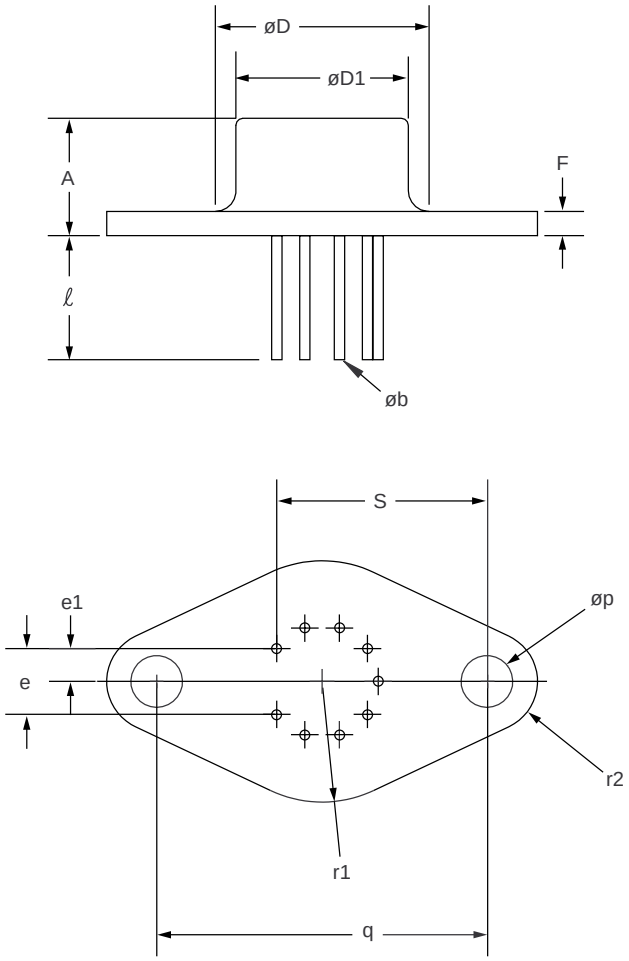
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.185	4.19	4.70	
øb	.016	.019	.41	.48	1, 5
øb1	.016	.021	.41	.53	1, 5
øD	.335	.375	8.51	9.52	
øD1	.305	.335	7.75	8.51	
øD2	.110	.160	2.79	4.06	
e	.200 BSC		5.08 BSC		
e1	.100 BSC		2.54 BSC		
F	—	.040	—	1.02	
k	.027	.034	.69	.86	
k1	.027	.045	.69	1.14	2
L	.500	.750	12.70	19.05	1
L1	—	.050	—	1.27	1
L2	.250	—	6.35	—	1
Q	.010	.045	.25	1.14	
α	45° BSC		45° BSC		

Notes:

1. (All leads) øb applies between L1 & L2. øb1 applies between L2 & .500 (12.70mm) from the reference plane. Diameter is uncontrolled in L1 & beyond .500 (12.70mm) from the reference plane.
2. Measured from the maximum diameter of the product.
3. Leads having a maximum diameter .019 (.48mm) measured in gauging plane, .054 (1.37mm) +.001 (.03mm) –.000 (.00mm) below the reference plane of the product shall be within .007 (.18mm) of their true position relative to a maximum width tab.
4. The product may be measured by direct methods or by gauge.
5. All leads – increase maximum limit by .003 (.08mm) when lead finish is applied.

Mechanical Dimensions (continued)

9-Lead Metal Can IC Header Package



Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.250	.340	6.35	8.64	
øb	.028	.034	.71	.86	1
øD	—	.620	—	15.75	
øD1	.470	.500	11.94	12.70	
e	.190	.210	4.83	5.33	
e1	.093	.107	2.36	2.72	
F	.050	.075	1.27	1.91	
ℓ	.360	—	9.14	—	
øp	.142	.152	3.61	3.86	
q	.958	.962	24.33	24.43	
r1	—	.350	—	8.89	
r2	—	.145	—	3.68	
S	.570	.590	14.48	14.99	

Notes:

1. All leads—increase maximum limit by .003 (.08mm) when lead finish is applied.

Ordering Information

Product Number	Temperature Range	Screening	Package
RC4195N	0° to +70°C	Commercial	8 Pin Plastic DIP
RC4195T	0° to +70°C	Commercial	8 Pin TO-99 Metal Can
RC4195K	0° to +70°C	Commercial	9 Pin TO-66 Metal Can
RM4195T	-55°C to +125°C	Commercial	8 Pin TO-99 Metal Can
RM4195T/883B	-55°C to +125°C	Military	8 Pin TO-99 Metal Can
RM4195K	-55°C to +125°C	Commercial	9 Pin TO-66 Metal Can

Note:

1. /883B suffix denotes MIL-STD-883, Par. 1.2.1 compliant device.

RC4200

Analog Multiplier

Features

- High accuracy
- Nonlinearity – 0.1%
  Temperature coefficient – 0.005%/°C
- Multiple functions
- Multiply, divide, square, square root, RMS-to-DC conversion, AGC and modulate/demodulate
- Wide bandwidth – 4 MHz
- Signal-to-noise ratio – 94 dB

Applications

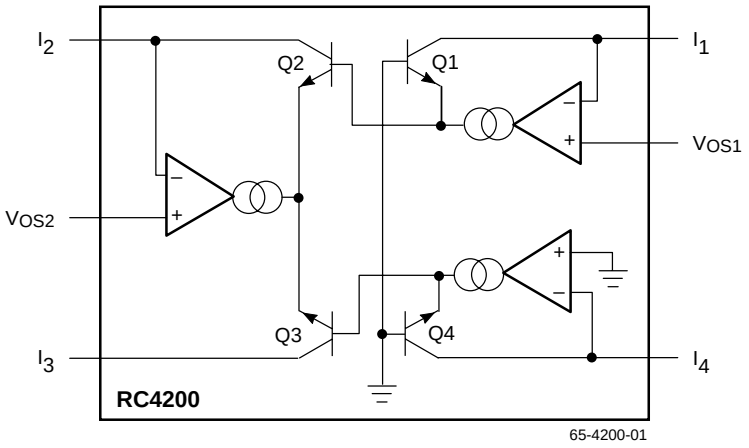
- Low distortion audio modulation circuits
- Voltage-controlled active filters
- Precision oscillators

Description

The RC4200 analog multiplier has complete compensation for nonlinearity, the primary source of error and distortion. This multiplier also has three onboard operational amplifiers designed specifically for use in multiplier logging circuits. These amplifiers are frequency compensated for optimum AC response in a logging circuit, the heart of a multiplier, and can therefore provide superior AC response.

The RC4200 can be used in a wide variety of applications without sacrificing accuracy. Four-quadrant multiplication, two-quadrant division, square rooting, squaring and RMS conversion can all be easily implemented with predictable accuracy. The nonlinearity compensation is not just trimmed at a single temperature, it is designed to provide compensation over the full temperature range. This nonlinearity compensation combined with the low gain and offset drift inherent in a well-designed monolithic chip provides a very high accuracy and a low temperature coefficient.

Block Diagram



65-4200-01

Functional Description

The RC4200 multiplier is designed to multiply two input currents (I_1 and I_2) and to divide by a third input current (I_4). The output is also in the form of a current (I_3). A simplified circuit diagram is shown in the Block Diagram. The nominal relationship between the three inputs and the output is:

$$I_3 = \frac{I_1 I_2}{I_4} \quad (1)$$

The three input currents must be positive and restricted to a range of 1 μA to 1 mA. These currents go into the multiplier chip at op amp summing junctions which are nominally at zero volts. Therefore, an input voltage can be easily converted to an input current by a series resistor. Any number of currents may be summed at the inputs. Depending on the application, the output current can be converted to a voltage by an external op amp or used directly. This capabilty of combining input currents and voltages in various combinations provides great versatility in application.

Inside the multiplier chip, the three op amps make the collector currents of transistors Q1, Q2 and Q4 equal to their respective input currents (I_1, I_2, and I_4). These op amps are designed with current source outputs and are phase-compensated for optimum frequency response as a multiplier. Power drain of the op amps was minimized to prevent the introduction of undesired thermal gradients on the chip. The three op amps operate on a single supply voltage (nominally -15V) and total quiescent current drain is less than 4 mA. These special op amps provide significantly improved performance in comparison to 741-type op amps.

The actual multiplication is done within the log-antilog configuration of the Q1-Q4 transistor array. These four transistors, with associated proprietary circuitry, were specially designed to precisely implement the relationship.

$$V_{BEN} = \frac{kT}{Q} \ln \frac{I_{CN}}{I_{SN}} \quad (2)$$

Previous multiplier designs have suffered from an additional undesired linear term in the above equation; the collector current times the emitter resistance. The I_{CrE} term introduces a parabolic nonlinearity even with matched transistors. Fairchild Semiconductor has developed a unique and proprietary means of inherently compensating for this undesired I_{CrE} term. Furthermore, this Fairchild Semiconductor developed circuit technique compensates linearity error over temperature changes. The nonlinearity versus temperature is significantly improved over earlier designs.

From equation (2) and by assuming equal transistor junction temperatures, summing base-to-emitter voltage drops around the transistor array yields:

$$\frac{KT}{q}\left[\ln\frac{I_1}{I_{S1}} = \ln\frac{I_2}{I_{S2}} - \ln\frac{I_3}{I_{S3}} - \ln\frac{I_4}{I_{S4}}\right] = 0 \quad (3)$$

This equation reduces to:

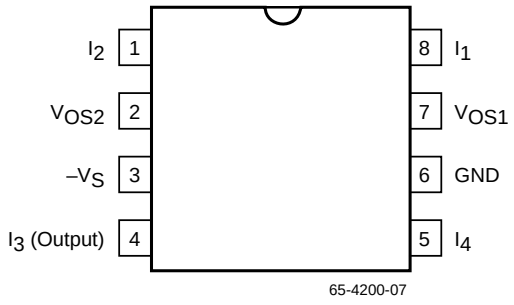
$$\frac{I_1 I_2}{I_3 I_4} = \frac{I_{S1} I_{S2}}{I_{S3} I_{S4}} \quad (4)$$

The rate of reverse saturation current $I_{S1}I_{S2}/I_{S3}I_{S4}$, depends on the transistor matching. In a monolithic multiplier this matching is easily achieved and the rate is very close to unity, typically 1.0±1%. The final result is the desired relationship:

$$I_3 = \frac{I_1 I_2}{I_4} \quad (5)$$

The inherent linearity and gain stability combined with low cost and versatility makes this new circuit ideal for a wide range of nonlinear functions.

Pin Assignments



65-4200-07

Absolute Maximum Ratings

Parameter		Min.	Max.	Unit
Supply Voltage[1]			-22	V
Input Current			-5	mA
Storage Temperature Range	RM4200/4200A	-65	+150	°C
	RC4200/4200A	-55	+125	°C
Operating Temperature Range	RM4200/4200A	-55	+125	°C
	RC4200/4200A	0	+70	°C

Notes:

1. For a supply voltage greater than -22V, the absolute maximum input voltage is equal to the supply voltage.
2. Observe package thermal characteristics.

Thermal Characteristics

(Still air, soldered into PC board)

	8-Lead Plastic DIP	8-Lead SOIC	8-Lead Ceramic DIP
Maximum Junction Temperature	+125°C	+125˚C	+175°C
Maximum P_D T_A < 50°C	468mW	300mW	833mW
Thermal Resistance θ_{JC}	—	—	45°C/W
Thermal Resistance θ_{JA}	160°C/W	240˚C/W	150°C/W
For T_A > 50°C Derate at	6.25mW/°C	4.17mW/˚C	8.33mW/°C

Electrical Characteristics

(Over operating temperature range, V_S = -15V unless otherwise noted)

Parameters	Test Conditlons	4200A			4200			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Total Error as Multiplier	TA = +25°C							
	Untrimmed[1]			±2.0			±3.0	%
	With External Trim		±0.2			±0.2		%
	Versus Temperature		±0.005			±0.005		%/°C
	Versus Supply (-9 to -18V)		±0.1			±0.1		%/V
Nonlinearity[2]	50μA ≤ $I_{1,2,4}$ ≤ 250 μA, T_A = +25°C			±0.1			±0.3	%
Input Current Range (I_1, I_2 and I_4)		1.0		1000	1.0		1000	μA
Input Offset Voltage	I_1 = I_2 = I_4 = 150 μA T_A = +25°C			±5.0			±10	mV
Input Bias Current	I_1 = I_2 = I_4 = 150 μA T_A = +25°C			300			500	nA
Average Input Offset Voltage Drift	I_1 = I_2 = I_4 = 150 μA			±50			±100	μV/°C
Output Current Range (I_3)[3]		1.0		1000	1.0		1000	μA

Electrical Characteristics (continued)

(Over operating temperature range, V_S = -15V unless otherwise noted)

Parameters	Test Conditlons	4200A			4200			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency Response, -3dB point			4.0			4.0		MHz
Supply Voltage		-18	-15	-9.0	-18	-15	-9.0	V
Supply Current	$I_1 = I_2 = I_4 = 150\ \mu A$ $T_A = +25°C$			4.0			4.0	mA

Notes:

1. Refer to Figure 6 for example.
2. The input circuits tend to become unstable at I_1, I_2, $I_4 < 50\ \mu A$ and linearity decreases when I_1, I_2, $I_4 > 250\ \mu A$ (eq. @ $I_1 = I_2 = 500\ \mu A$, nonlinearity error ≈ 0.5%).
3. These specifications apply with output (I_3) connected to an op amp summing junction. If desired, the output (I_3) at pin (4) can be used to drive a resistive load directly. The resistive load should be less than 700Ω and must be pulled up to a positive supply such that the voltage on pin (4) stays within a range of 0 to +5V.

Applications Discussion

Current Multiplier/ Divider

The basic design criteria for all circuit configurations using the RC4200 multiplier is contained in equation (1), that is,

$$I_3 = \frac{I_1 I_2}{I_4}$$

The current-product-balance equation restates this as:

$$I_1 I_2 = I_3 I_4 \quad (6)$$

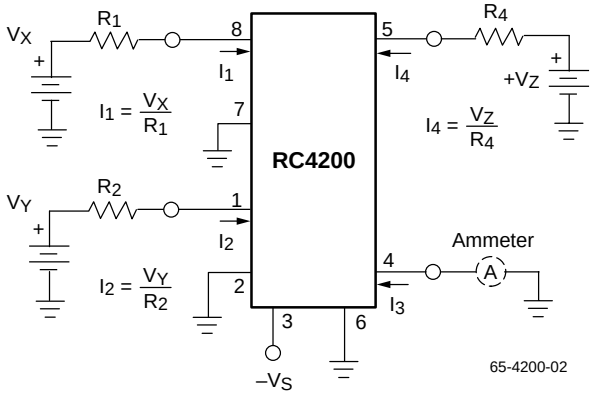


Figure 1. Current Multiplier/Divider

Dynamic Range and Stability

The precision dynamic range for the RC4200 is from +50 μA to +250 μA inputs for I_1, I_2 and I_4. Stability and accuracy degrade if this range is exceeded.

To improve the stability for input currents less than 50 μA, filter circuits (R_SC_S) are added to each input (see Figure 2).

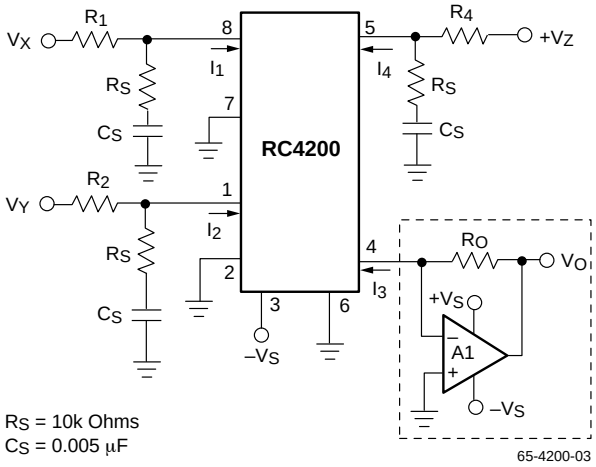


Figure 2. Current Multiplier/Divider with Filters

Amplifier A1 is used to convert the I_3 current to an output voltage.

Multiplier: Vz = constant ≠ 0
Divider: Vy = constant ≠ 0

Voltage Multiplier/Divider

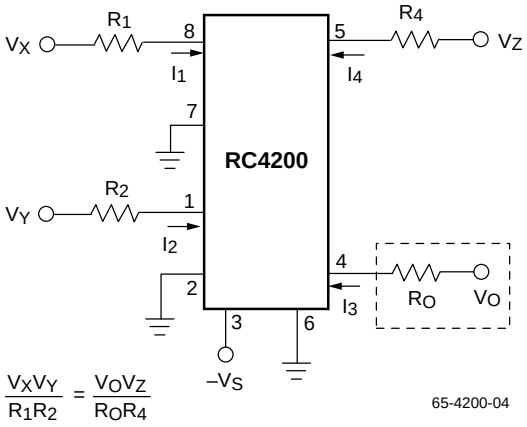


Figure 3. Voltage Multiplier/Divider

Solving for $V_0 = \frac{V_X V_Y}{V_Z} \frac{R_0 R_4}{R_1 R_2}$

For a multiplier circuit $V_Z = V_R = \text{constant}$

Therefore: $V_0 = V_X V_Y K$ where $K = \frac{R_0 R_4}{V_R R_1 R_2}$

For a divider circuit $V_Y = V_R = \text{constant}$

Therefore: $V_0 = \frac{V_X}{V_Z} K$ where $K = \frac{V_R R_0 R_4}{R_1 R_2}$

Extended Range

The input and output voltage ranges can be extended to include 0 and negative voltage signals by adding bias currents. The RSCS filter circuits are eliminated when the input and biasing resistors are selected to limit the respective currents to 50 μA min. and 250 μA max.

Extended Range Multiplier

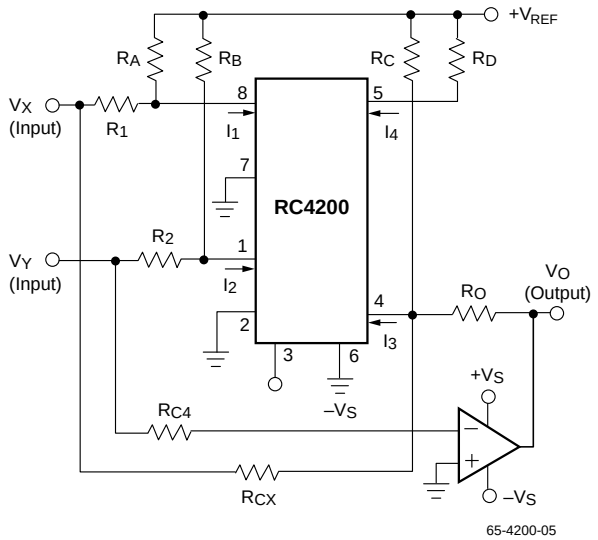


Figure 4. Extended Range Multiplier

Resistors R_a and R_b extend the range of the V_X and V_Y inputs by picking values such that:

$$I_1(\text{min.}) = \frac{V_X(\text{min.})}{R_1} + \frac{V_{REF}}{R_a} = 50\ \mu A,$$

$$\text{and } I_1(\text{max.}) = \frac{V_X(\text{max.})}{R_1} + \frac{V_{REF}}{R_a} = 250\ \mu A,$$

$$\text{also } I_2(\text{min.}) = \frac{V_Y(\text{min.})}{R_2} + \frac{V_{REF}}{R_b} = 50\ \mu A,$$

$$\text{and } I_2(\text{max.}) = \frac{V_Y(\text{max.})}{R_2} + \frac{V_{REF}}{R_b} = 250\ \mu A.$$

Resistor R_C supplies bias current for I_3 which allows the output to go negative.

Resistors R_{CX} and R_{CY} permit equation (6) to balance, ie.:

$$\left(\frac{V_X}{R_1} + \frac{V_{REF}}{R_a}\right)\left(\frac{V_Y}{R_2} + \frac{V_{REF}}{R_b}\right) = \left(\frac{V_0}{R_0} + \frac{V_{REF}}{R_C} + \frac{V_X}{R_{CX}} + \frac{V_Y}{R_{CY}}\right)\left(\frac{V_{REF}}{R_D}\right)$$

$$\frac{V_Y V_X}{R_1 R_2} + \frac{V_X V_{REF}}{R_1 R_b} + \frac{V_Y V_{REF}}{R_2 R_a} + \frac{V_{REF}}{R_a R_b} =$$

$$\frac{V_0 V_{REF}}{R_0 R_d} + \frac{V_X V_{REF}}{R_{cx} R_d} + \frac{V_Y V_{REF}}{R_{CY} R_d} + \frac{V_{REF}^2}{R_c R_d}$$

Cross-Product Cancellation

Cross-products are a result of ths $V_X V_R$ and $V_Y V_R$ terms. To the extend that $R_1 R_b = R_{CX} R_D$, and $R_2 R_a = R_{CY} R_d$ cross-product cancellation will occur.

Arithmetic Offset Cancellation

The offset caused by the V_{REF}^2 term will cancel to the extent that $R_a R_b = R_0 R_d$, and the result is:

$$\frac{V_Y V_X}{R_1 R_2} = \frac{V_0 V_{REF}}{R_0 R_d} \text{ or } V_0 = V_X V_Y K$$

$$\text{where } K = \frac{R_0 R_d}{V_{REF} R_1 R_2}$$

Resistor Values

Inputs:

$$V_X(\text{min.}) \le V_X \le V_X(\text{max.})$$

$$\Delta V_X = V_X(\text{max.}) - V_X(\text{min.})$$

$$V_Y(\text{min.}) \le V_Y \le V_Y(\text{max.})$$

$$\Delta V_Y = V_Y(\text{max.}) = V_Y(\text{min.})$$

$$V_{REF} = \text{Constant (+7V to +18V)}$$

$$K = \frac{V_0}{V_X V_Y}(\text{Design Requirements})$$

$$R_1 = \frac{\Delta V_X}{200\mu A},\ R_2 = \frac{\Delta V_Y}{200\mu A},\ R_d = \frac{V_{REF}}{250\mu A}$$

$$R_a = \frac{\Delta V_X V_{REF}}{250\mu A \Delta V_X - 200\mu A\ V_X(\text{max.})}$$

$$R_b = \frac{\Delta V_X V_{REF}}{250\mu A \Delta V_Y - 200\mu A\ V_Y(\text{max.})}$$

$$R_c = \frac{R_a R_b}{R_d},\ R_{CX} = \frac{R_1 R_b}{R_d},\ R_{cy} = \frac{R_2 R_a}{R_d}$$

$$R_0 = \frac{\Delta V_X \Delta V_Y K}{160\mu A}$$

Multiplying Circuit Offset Adjust

$10K \le R_5 = R_9 = R_{16} \le 50K$

$R_7 = R_{11} = R_{14}, = 100\Omega$

$R_6 = R_{10} = 100\Omega\ (V_S/0.05)$

$R_{15} = 100\Omega\ (V_S/0.10)$

$R_8 = R_1 \,||\, R_a$

$R_{12} = R_2 \,||\, R_b$

$R_{13} = R_0 \,||\, R_C \,||\, R_{CX} \,||\, R_{CY}$

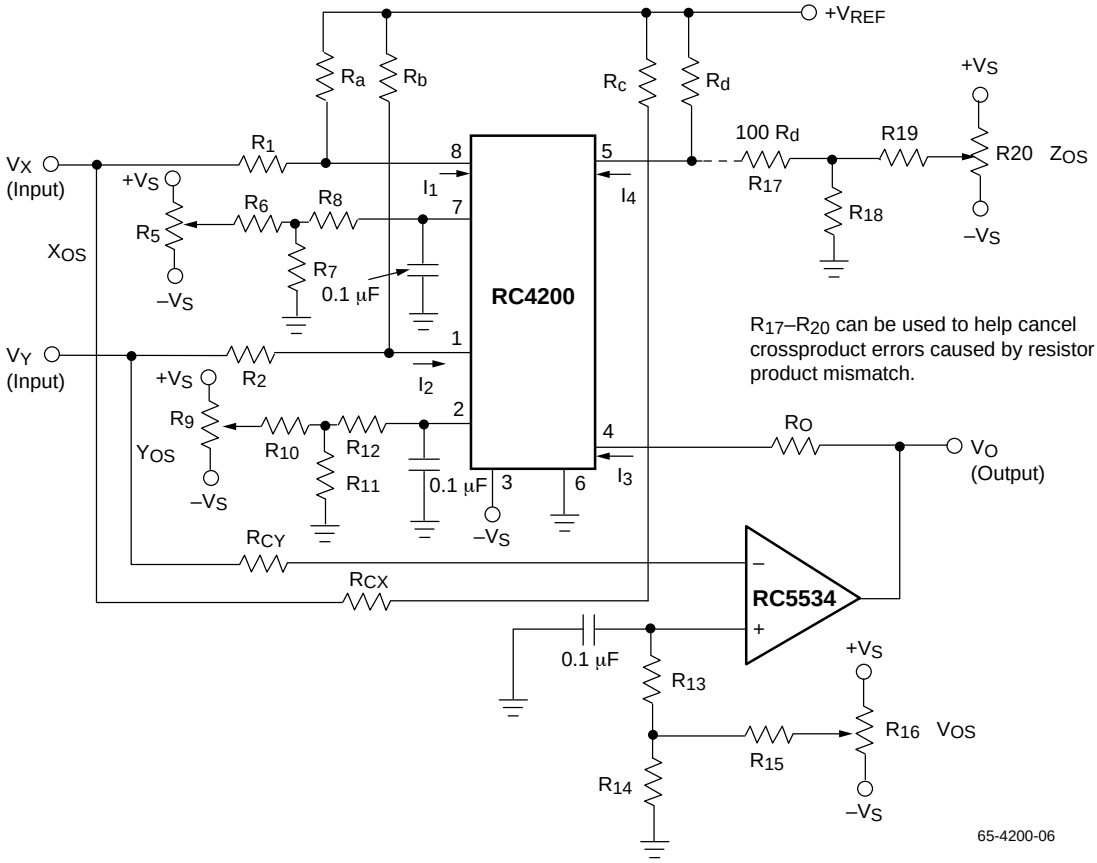


Figure 5. Multiplying Circuit Offset Adjust

Procedure

1. 1.Set all trimmer pots to 0V on the wiper.
2. 2.Connect V_X input to ground. Put in a full scale square wave on V_Y input. Adjust $X_{OS}(R_5)$ for no square wave on V_0 output (adjust for 0 feedthrough).
3. 3.Connect V_Y input to ground. Put in a full scale square wave on V_X input. Adjust $Y_{OS}(R_9)$ for no square wave on V_0 output (adjust for 0 feedthrough).
4. 4.Connect V_X and V_Y to ground. Adjust $V_{OS}(R_{16})$ for 0V on V_0 output.

Extended Range Divider

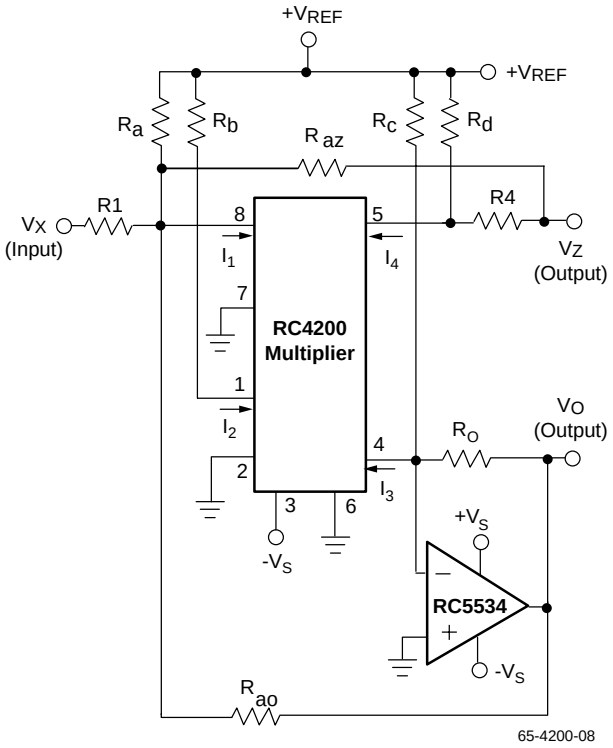


Figure 6. Extended Range Divider

As with the extended range multiplier, resistors R_{az} and R_{ao} are added to cancel the cross-product error caused by the biasing resistors, i.e.

$$\left(\frac{V_X}{R_1}+\frac{V_0}{R_{ao}}+\frac{V_Z}{R_{az}}+\frac{V_{REF}}{R_a}\right)\left(\frac{V_{REF}}{R_b}\right)=\left(\frac{V_0}{R_0}+\frac{V_{REF}}{R_C}\right)\left(\frac{V_Z}{R_4}+\frac{V_{REF}}{R_D}\right)$$

$$\frac{V_X V_{REF}}{R_1 R_b}+\frac{V_0 V_{REF}}{R_{ao} R_b}+\frac{V_Z V_{REF}}{R_{az} R_b}+\frac{{V_{REF}}^2}{R_a R_b}=$$

$$\frac{V_0 V_Z}{R_0 R_4}+\frac{V_0 V_{REF}}{R_0 R_d}+\frac{V_Z V_{REF}}{R_4 R_c}+\frac{{V_{REF}}^2}{R_c R_d}$$

To cancel cross-product and arithmetic offset:

$R_{ao}R_b = R_0R_d$, $R_{az}R_b = R_4R_c$ and $R_aR_b = R_cR_d$

and the result is:

$$\frac{V_X V_{REF}}{R_1 R_b}=\frac{V_0 V_Z}{R_0 R_4} \quad \text{or} \quad V_0=\frac{V_X}{V_Z K}$$

where $K=\dfrac{V_{REF} R_0 R_4}{R_1 R_b}$

Notice that it is necessary to match the above resistor cross-products to within the amount of error tolerable in the output offset, i.e., with a 10V F.S. output, 0.1% resistor cross-product match will give 0.1% x 10V. untrimmable output offset voltage.

Resistor Values

Inputs:

$V_X(\text{min.}) \le V_X \le V_X(\text{max.})$

$\Delta V_X = V_X(\text{max.}) = V_X(\text{min.})$

$V_Z(\text{min.}) \le V_Z \le V_Z(\text{max.})$

$\Delta V_Z = V_Z(\text{max.}) = V_Z(\text{min.})$

V_{REF} = Constant (+7V to +18V)

Outputs:

$V_0(\text{min.}) \le V_0 \le V_0(\text{max.})$

$\Delta V_0 = V_0(\text{max.}) = V_0(\text{min.})$

$$K = \frac{V_0 V_Z}{V_X}(\text{Design Requirement})$$

$$R_0 = \frac{\Delta V_0}{750\mu A},\ R_b = \frac{\Delta V_{REF}}{250\mu A},\ R_4 = \frac{\Delta V_Z}{200\mu A}$$

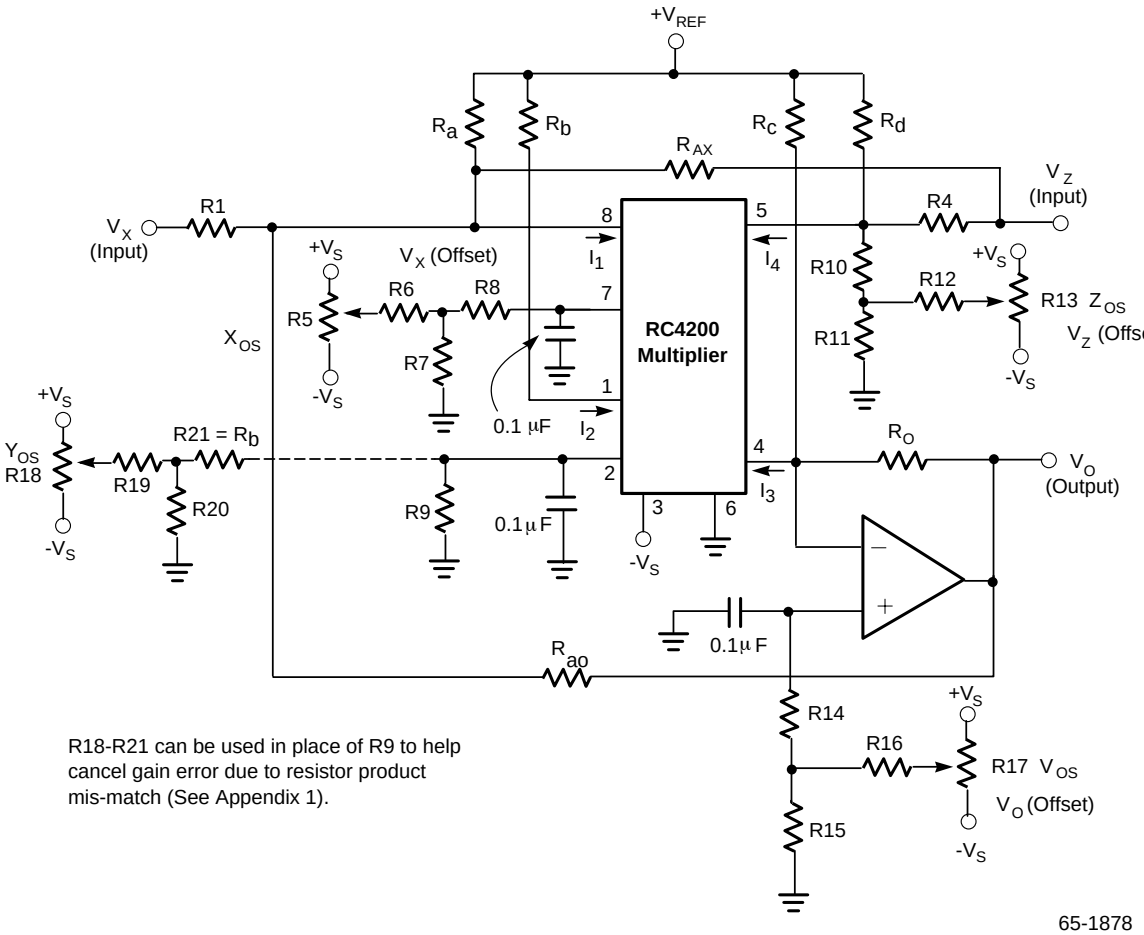
$$R_c = \frac{\Delta V_0 V_{REF}}{750\mu A \Delta V_0 - 700\mu A\ V_0(\text{max.})}$$

$$R_d = \frac{\Delta V_X V_{REF}}{250\mu A \Delta V_Z - 200\mu A\ V_Z(\text{max.})}$$

$$R_a = \frac{R_c R_d}{R_b},\ R_{az} = \frac{R_c R_4}{R_b},\ R_{ao} = \frac{R_0 R_d}{R_b}$$

$$R_1 = \frac{\Delta V_0 \Delta V_Z}{600\mu A K}$$

Divider Circuit with Offset Adjustment



General

$10K \le R_5 = R_{13} = R_{17} \le 50K$

$R_7 + R_8 \approx R_1 \,||\, R_a \,||\, R_{az} \,||\, R_{ao}$

$R_6 \approx R_7 (V_S/0.05)$

$R_9 = R_b$

$R_{10} \approx 100 \times R_4$

$R_{11} = 20K$

$R_{12} = 100K$

$R_{14} + R_{15} \approx R_0 \,||\, R_c$

$R_{16} \approx R_{15} (V_S/0.10)$

Example: Two-Quad Divider

$V_0 = K(V_X/V_Z)$, $K = k$, $V_{REF} = +V_S = +15V$

$-10 \le V_X \le +10$, therefore $\Delta V_X = 20$

$0 \le V_Z \le +10$, therefore $\Delta V_Z = 20$

$-10 \le V_0 \le +10$, therefore $\Delta V_0 = 20$

$R_0 = 26.7K$

$R_b = 60K$

$R_4 = 50K$

$R_c = 37.5K$

$R_d = 300K$

$R_a = 187.5K$

$R_{az} = 31.25$

$R_{ao} = 133K$

$R_1 = 333K$

$R_5, R_{13}, R_{17} = 10K$

$R_7, R_{15} = 1K$

$R_8, R_{11} = 20K$

$R_6, R_9, R_{16} = 300K$

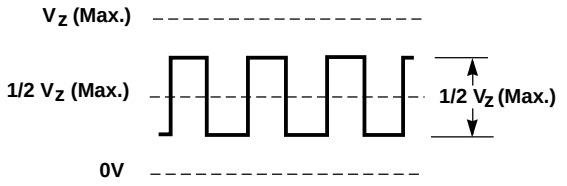
$R_{10} = 4.7M$

$R_{12} = 100K$

Figure 7. Divider Circuit with Offset Adjustment

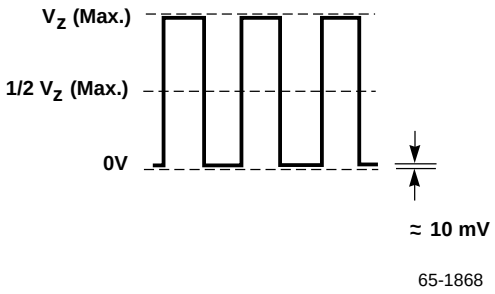
Divider Circuit Offset Adjustment Procedure

1. Set each trimmer pot to 0V on the wiper.
2. Connect V_X (input) to ground. Put a DC voltage of approximatey 1/2 V_Z (max.) DC on the V_Z (input) with an AC (squarewave is easiest) voltage of 1/2 V_Z (max.) peak-to-peak superimposed on it. Adjust X_{OS} (R5) for zero feedthrough. (No AC at V_0)



3. Connect V_X (input) to V_Z (input) and put in the 1/2 V_Z(max.) DC with an AC of approximately 20 mV less than V_Z(max.).

   Adjust Z_{OS} (R_{13}) for zero feedthrough.



4. Return V_X (Input) to ground and connect V_Z(max.) DC on V_Z(input). Adjust output V_{OS}(R_{17}) for V_O = 0V_O
5. Connect V_X (input) to V_Z (input) and and in V_Z (max.) DC. (The output will equal K.) Decrease the input slowly until the output (V_0 - K) deviates beyond the desired accuracy. Adjust Z_{OS} to bring it back into tolerance and return to Step 4. Continue steps 4 and 5 until V_Z reduces to the lowest value desired.

Notice that as the input to VX and VZ gets closer to zero (an illegal state) the system noise will predominate so much that an integrating voltmeter will be very helpful.

Square Root Circuit $V_0 = N\sqrt{V_X}$

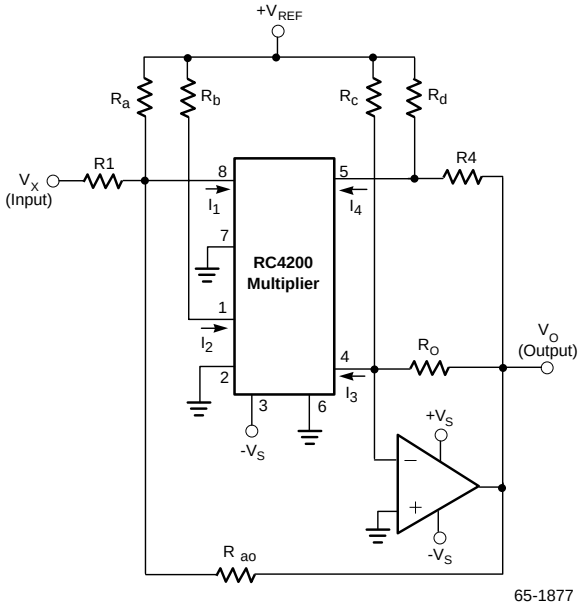


Figure 8.

$$\frac{V_X V_{REF}}{R_1 R_b} + \frac{V_{REF}^2}{R_a R_b} + \frac{V_0 V_{REF}}{R_{ao} R_b} = \frac{V_0^2}{R_0 R_4} + \frac{V_0 V_{REF}}{R_c R_4} + \frac{V_0 V_{REF}}{R_0 R_d} + \frac{V_{REF}^2}{R_c R_d}$$

If $R_a R_b = R_c R_d$ and $R_{ao} R_b R_0 R_d + R_{ao} R_b R_c R_4 = R_c R_d R_0 R_4$

Then $\frac{V_0^2}{R_0 R_4} = \frac{V_X V_{REF}}{R_1 R_b}$ or $V_0^2 = V_X K$ where $K = \frac{V_{REF} R_0 R_4}{R_1 R_b}$

and $V_0 = N\sqrt{V_X}$ where $N = \sqrt{K}$

$0 \le V_X \le V_X(\text{max.})$ and $V_0(\text{max.}) = N\sqrt{V_X(\text{max.})}$

$N = \frac{V_0}{\sqrt{V_X}}$ (Design Requirements)

$R_1 = \frac{V_0(\text{max.})^2}{74\mu A\, N^2}$

$R_a = R_d = \frac{V_{REF}}{50\mu A}$

$R_b = R_c = \frac{V_{REF}}{150\mu A}$

$R_4 = \frac{V_0(\text{max.})}{50\mu A}$

$R_{ao} = \frac{V_0(\text{max.})}{125\mu A}$

$R_0 = \frac{V_0(\text{max.})}{225\mu A}$

Square Root Circuit Offset Adjust

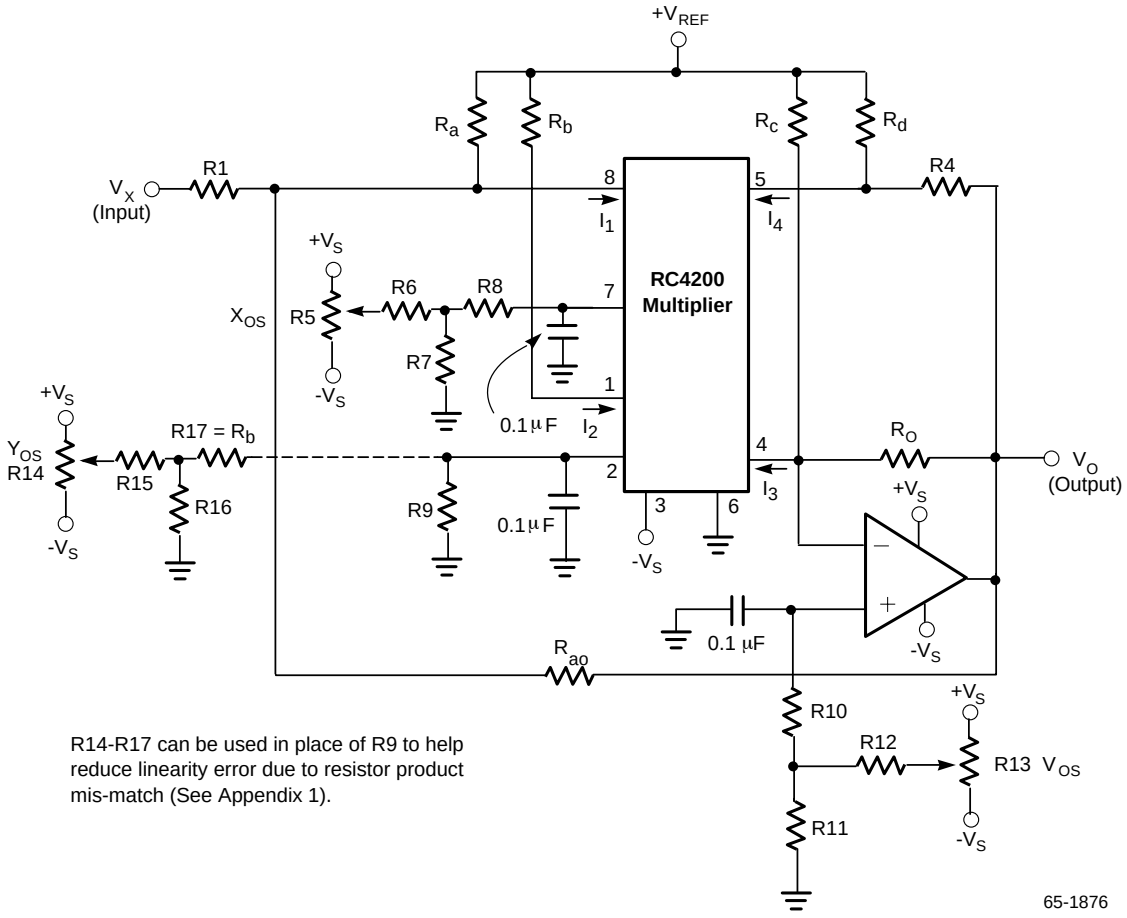


Figure 9. Square Root Circuit Offset Adjust

$10K \leq R_5 = R_{13} \leq 50K$

$R_7 = 100\Omega$

$R_6 = R_7 \frac{V_S}{0.05}$

$R_8 = R_1 \| R_a \| R_{ao}$

$R_9 = R_b$

$R_{10} = R_0 \| R_C$

$R_{11} = 100\Omega$

$R_{12} = R_{11} \frac{V_S}{0.1}$

Procedure

1. Set both trimmer pots to 0V on the wiper.
2. Put in a full scale (0 to V_X(max.) squarewave on V_X input. Adjust X_{OS}(R5) for proper peak-to-peak amplitude on V_0 output. (Scaling adjust)
3. Connect V_X input to ground. Adjust V_{OS}(R13) for 0V on V_0 output.

Squaring Circuits $V_0 = K V_X^2$

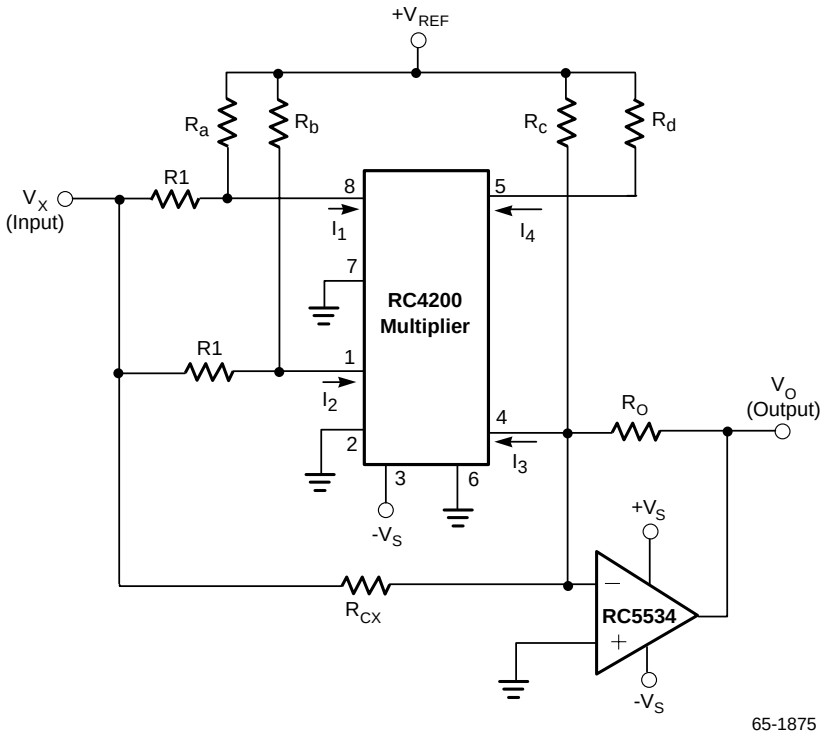


Figure 10. Squaring Circuit

$$\frac{V_X^2}{R_1^2} + \frac{2V_X V_{REF}}{R_1 R_a} + \frac{V_{REF}^2}{R_a^2} = \frac{V_0 V_{REF}}{R_0 R_d} + \frac{V_{REF}^2}{R_c R_d} + \frac{V_X V_{REF}}{R_c R_d}$$

if $R_a^2 = R_c R_d$ and $R_1 R_a = 2R_{CX} R_D$

then $\frac{V_0 V_{REF}}{R_0 R_d} = \frac{V_X^2}{R_1^2}$ or $V_0 = K V_X^2$ where $K = \frac{R_0 R_d}{V_{REF} R_1^2}$

$V_X(\text{min.}) \le V_X \le V_X(\text{max.})$ $\Delta V_X = V_X(\text{max.}) - V_X(\text{min.})$

$K = \frac{V_0}{V_X^2}$ (Design Requirement)

$R_1 = \frac{\Delta V_X}{200\mu A}$

$R_a = \frac{\Delta V_X V_{REF}}{250\mu A \Delta V_X - 200\mu A\ V_X(\text{max.})}$

$R_d = \frac{V_{REF}}{250\mu A}$

$R_c = \frac{R_a^2}{R_d}$

$R_{cx} = \frac{R_1 R_a}{2R_d}$

$R_0 = \frac{\Delta V_X^2 K}{160\mu A}$

Squaring Circuits Offset Adjust

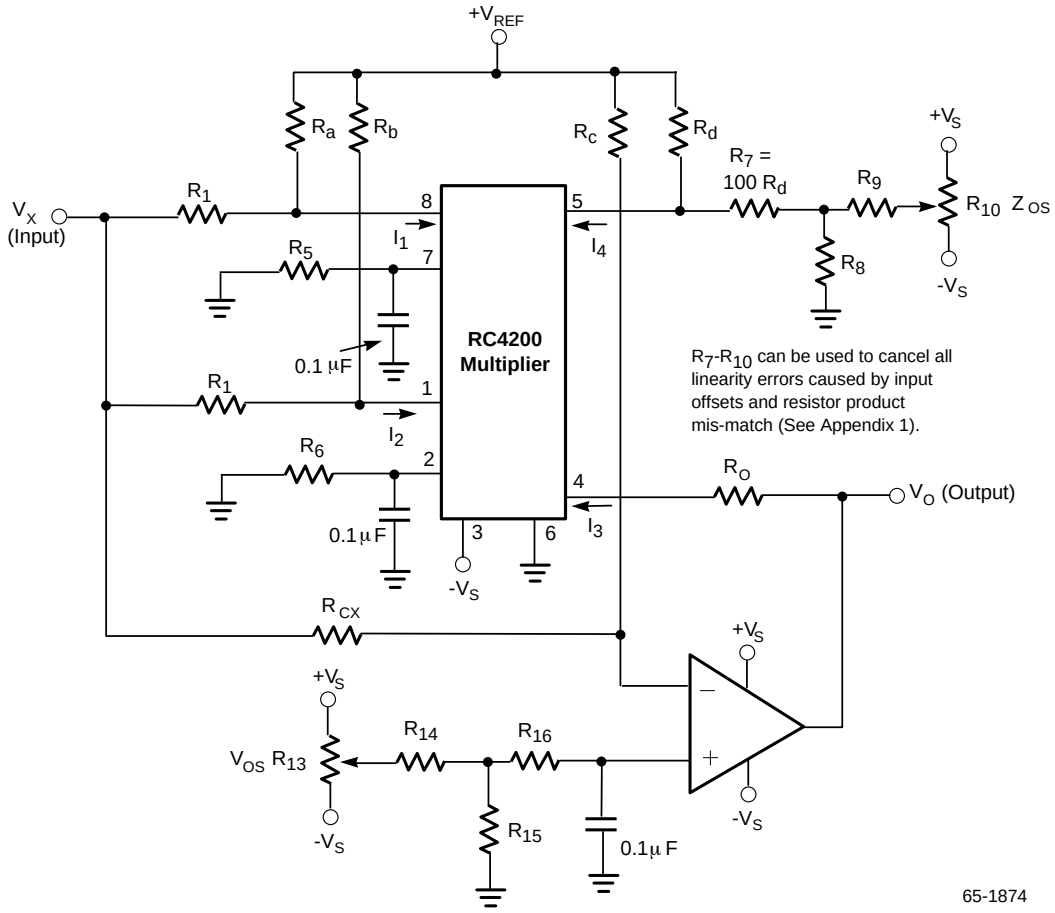


Figure 11. Squaring Circuit Offset Adjust

$10K \leq R_{10} = R_{11} \leq 50K$

$R_8,\ R_{15} = 100\Omega$

$R_9,\ R_{14} = 100\Omega\frac{V_S}{0.1}$

$R_5,\ R_6 = R_1 \parallel R_a$

$R_{16} = R_0 \parallel R_c \parallel R_a$

Procedure

1. 1.Set both trimmer pots to 0V on the wiper.
2. 2.Put in a full scale ($\pm V_X$) squarewave on V_X input. Adjust Z_{OS}(R10) for uniform output.
3. 3.Connect V_X input to ground. Adjust V_{OS}(R_{11}) for 0V on V_0 outputs.

Appendix 1—System Errors

There are four types of accuracy errors which affect overall system performance. They are:

- Nonimearity—Incremental deviation from absolute accuracy. See Note 1.
- Scaling Error—Linear deviation from absolute accuracy.
- Output Offset—Constant deviation from absolute accuracy.
- Feedthrough.—Cross-product errors caused by input offsets and external circuit limitations. See Note 2.

This nonlinearity error in the transfer function of the RC4200 is ±0.1% maximum (±0.03 maximum for the RC4200A). That is,

$$I_3 = \frac{I_1 I_2}{I_4} \pm 0.1\%\ \text{F.S.}^{(4)}$$

The other system errors are caused by voltage offsets on the inputs of the RC4200 and can be as high as ±3.0% (±2.0% for RC4200A).

$$V_0 = \frac{V_X V_Y}{V_Z} \frac{R_0 R_4}{R_1 R_2} \pm 3.0\%\ \text{F.S.}^{(3)(4)}$$

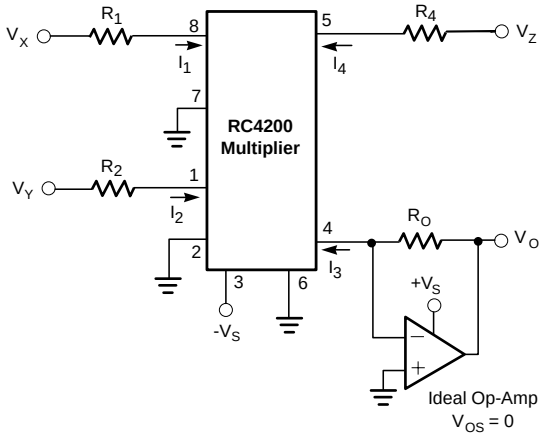


Figure 12.

Notes:

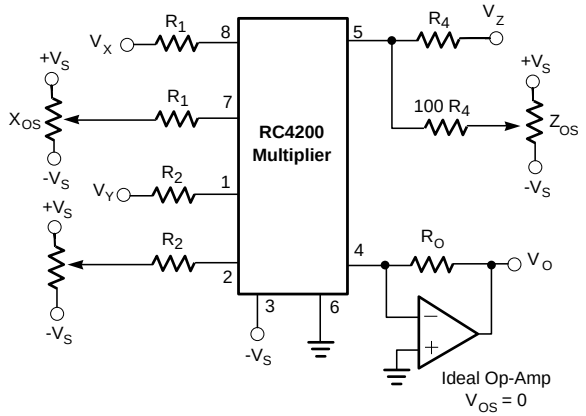
1. The input circuits tend to become unstable at I_1, I_2, I_4 < 50 μA and linearity decreases when I_1, I_2, I_4 > 250 μA (e.g., @ $I_1 = I_2 = 500$μA nonlinearity error ≈ 0.5%).
2. This section will not deal with feedthrough which is proportional to frequency of operation and caused by stray capacitance and/or bandwidth limitations. (refer to Figure 12.)
3. Not including resistor tolerance or output offset on the operational amplifier.
4. For 50 μA ≤ I_1, I_2, I_4 ≤ 250 μA.

Errors Caused by Input Offsets

$$V_0 = \frac{R_0 R_4}{R_0 R_4}\left[\frac{V_X V_Y}{V_Z} \pm \frac{1}{V_Z}\ \underbrace{V_Y V_{OSX}} \pm \underbrace{V_X V_{OSY}} \pm \underbrace{V_0 V_{OSZ}} \pm \underbrace{V_{OSX} V_{OSY}}\right]$$

V_Y Feedthrough
V_X Feedthrough
Scaling Error
Output Offset Error

System errors can be greatly reduced by externally trimming the input offset voltages of the RC4200. (±3.0% F.S. for RC4200 and ±0.1% for RC4200A.)



If $X_{OS} = X_{OSX}$, $Y_{OS} = Y_{OSY}$, $Z_{OS} = -V_{OSZ}$,

$$\text{then } V_O \frac{V_X V_Y}{V_Z} \frac{R_0 R_4}{R_1 R_2} \pm 0.3\%\ \text{F.S.}^{(3)}$$

Figure 13. RC4200 with Input Offset Adjustment

Extended Range Circuit Errors

The extended range configurations have a disadvantage in that additional accuracy errors may be introduced by resistor product mismatching.

Multiplier

An error in resistor product matching will cause an equivalent feedthrough or output offset error. See Figure 6.

$R_1R_b = R_CXR_d \pm \alpha$, V_X feedthrough ($V_Y = 0$) = $I\alpha V_X$

$R_2R_a = R_CYR_d \pm \beta$, V_Y feedthrough ($V_X = 0$) = $\pm\beta V_Y$

$R_aR_b = R_CR_d \pm \gamma$, V_0 offset ($V_X = V_Y = 0$) = $\pm\gamma V_{REF}$*

Note:

* Output offset errors can always be trimmed out with the output op amp offset adjust, VOS (R16).

Reducing Mismatch Errors

You need not use 0.01% resistors to reduce resistor product mismatch errors. Here are a couple of ways to obtain maximum accuracy out of the extended range multiplier (see Figure 4) using 1% resistors.

Method 1

V_X feedthrough, for example, occurs when $V_Y = 0$ and $V_{OSY} \neq 0$. This V_X feedthrough will equal $\pm V_X V_{OSY}$. Also, if $V_{OSZ} \neq 0$, there is a V_X feedthrough equal to $V_X V_{OSZ}$. A resistor-product error of α will cause a V_X feedthrough of $\pm\alpha V_X$. Likewise, V_Y feedthrough errors are: $\pm V_Y V_{OSX}$, $\pm V_Y V_{OSZ}$ and $\pm\beta V_Y$

Total feedthrough:
$\pm V_X V_{OSY} \pm V_Y V_{OSX} \pm\alpha V_X \pm\beta V_Y \pm(V_X + V_Y) V_{OSZ}$

By carefully abusing $X_{OS}(R_5)$, $Y_{OS}(R_9)$ and $Z_{OS}(R_{20})$ this equation can be made to very nearly equal zero and the feedthrough error will practically disappear.

A residual of set will probably remain which can be trimmed outwith $V_{OS}(R_{16})$ at the output of amp.

Method 2

Notice that the ratios of R_1R_b:$R_{CX}R_d$ and R_2R_a:$R_{CY}R_d$ are both dependent of R_d also that R_1, R_2, R_a and R_b are all functions of the maximum input requirements. By designing a multiplier for the same input ranges on both V_X and V_Y then $R_1 = R_2$, $R_{CX} = R_{CY}$ and $R_a = R_b$. (Note: it is acceptable to design a four quadrant multiplier and use only two quadrants of it.)

Select R_d to be 1% or 2% below (or above) the calculated value. This will cause α and β to both be positive (or negative) by nearly the same amount. Now the effective value of R_d can be trimmed with an offset adjustment $Z_{OS}(R_{20})$ on pin 5.

This technique causes: a slight gain error which can be compensated with the R_0 value, and an output of offset error that can be trimmed with $V_{OS}(R_{16})$ on the output op amp.

Extended Range Divider

The only cross-product error of interest is the V_Z feedthrough ($V_X = 0$ and $V_{OSX} \neq 0$) which is easily adjusted with $X_{OS}(R_5)$. See Figure 6.

Resistor product mismatch will cause scaling errors (gain) that could be a problem for very low values of V_Z. Adjustments to $Y_{OS}(R_{18})$ can be made to improve the high gain accuracy.

Square Root and Squaring

These circuits are functions of single variables so feedthrough, as such, is not a consideration. Cross product errors will effect incremental accuracy that can be corrected $Y_{OS}(R_{14})$ or $Z_{OS}(R_{10})$. See Figure 9 and Figure 11.

Appendix 2—Applications

Design Considerations for RMS-to-DC Circuits

Average Value

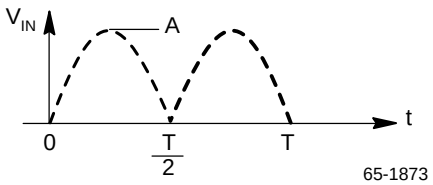
Consider $V_{in} = A\sin\omega\tau$. By definition,

$$V_{AG} = \int_0^{\frac{T}{2}} V_{IN}\,dt$$

Where T = Period

$\omega = 2\pi f$

$$= \frac{2\pi}{T}$$



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$$V_{AG} = \frac{2}{T}\int_0^{\frac{T}{2}} A\sin\omega t\,dt$$

$$= \frac{2A}{T}\left[-\frac{1}{\omega}\cos\,\omega t\right]_0^{\frac{T}{2}}$$

$$= \frac{2A}{2\pi}[-\cos(\pi) + \cos(0)]$$

Average Value of $A\sin\omega t$ is $\frac{2}{\pi}A$

RMS Value

Again, consider $V_{IN} = A\sin\omega t$

$$V_{rms} = \sqrt{V_{AVG}} = \sqrt{\frac{1}{T}\int_0^T [V_{IN}]^2 dt}$$

V_{rms} for $A\sin\omega t dt$:

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T A^2\sin^2\omega t\,dt}$$

$$V_{rms} = \sqrt{\frac{A^2}{T}\int_0^T \left[\frac{1}{2} - \frac{1}{2}\cos 2\cos 2\,\omega t\right]dt}$$

$$V_{rms} = \sqrt{\frac{A^2}{2}\left[\frac{T}{2} - \frac{1}{4\omega}\sin 2\,\omega t\right]_0^T}$$

$$V_{rms} = \sqrt{\frac{A^2}{2}\left[\frac{T}{2}\right]}$$

$$V_{rms} = \sqrt{\frac{A^2}{2}}$$

Therefore, the rms value of $A\sin\omega t$ becomes:

$$V_{rms} = \frac{A}{\sqrt{2}}$$

RMS Value for Rectified Sine Waves

Consider $V_{in} = |A\sin\omega t|$, a rectified wave. To solve, integrate of each half cycle.

$$\text{i.e. } \frac{1}{T}\int_0^T V_{in}^2\,dt =$$

$$\frac{1}{T}\left[\int_0^{\frac{T}{2}} A^2\sin^2\omega t\,dt + \int_{\frac{T}{2}}^T (-A\sin\omega t)^2 dt\right]$$

$$\text{This is the same as } \frac{1}{1}\int_0^T A^2\sin^2\omega t\,dt$$

$$\text{so, } |A\sin\omega t|_{rms} = A\sin\omega t_{rms}$$

Practical Consideration: $|A\sin\omega t|$ has high-order harmonics; $A\sin\omega t$ does not. Therefore, non-ideal integrators may cause different errors for two approaches.

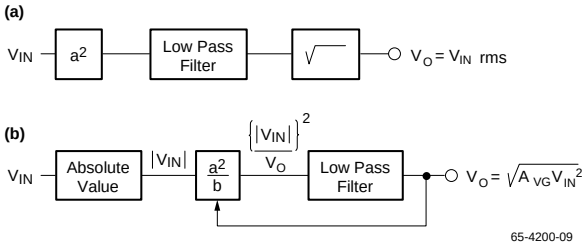

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Figure 14.

$$\text{Avg}\left[\frac{V_{IN}^2}{V_0}\right] = V_0$$

$$\text{implies } V_0 = \sqrt{\text{Avg}(|V_{IN}^2|)}$$

$$V_0 = \sqrt{\text{Avg}\ V_{IN}^2}$$

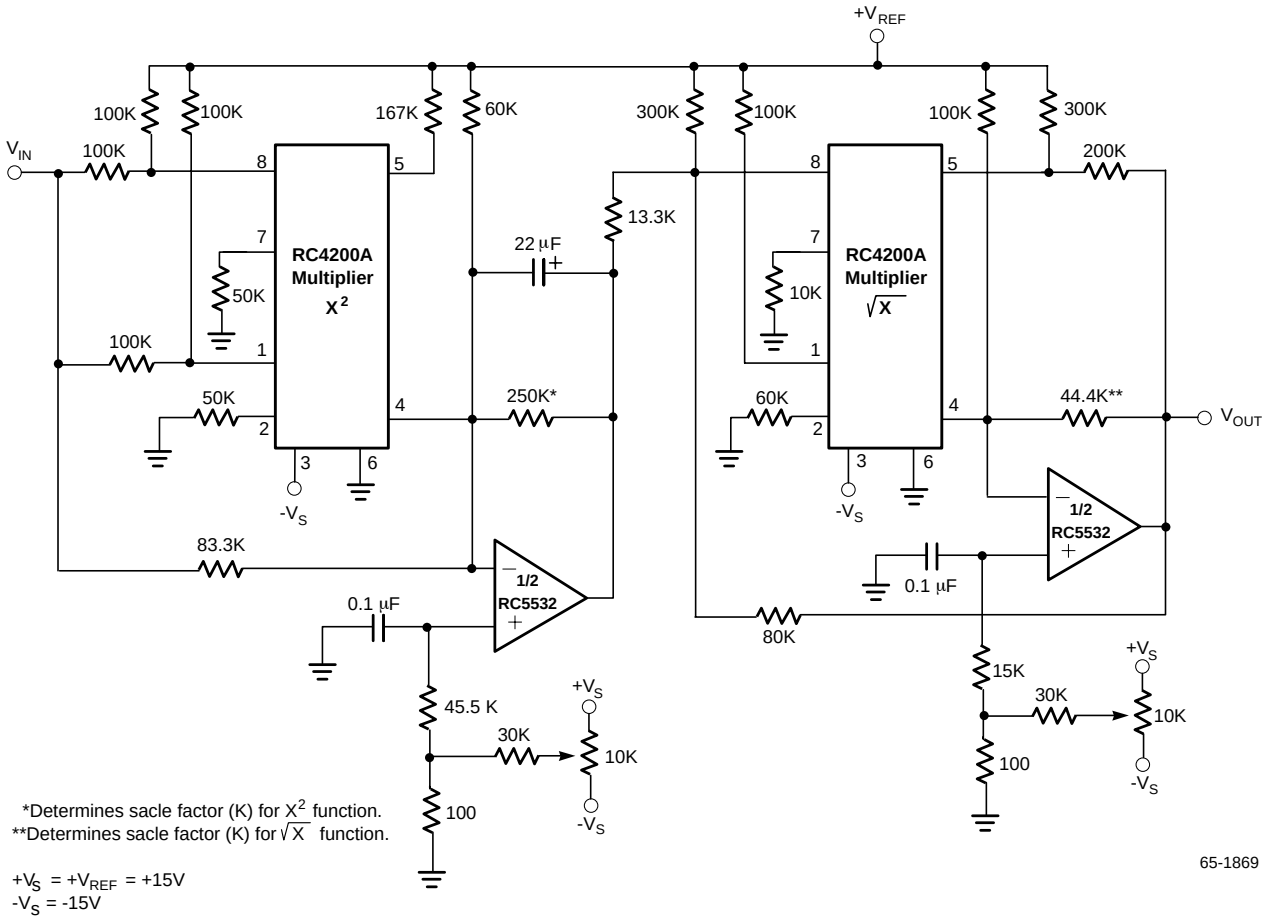


Figure 15. RMS to DC Converter $V_{OUT}=\sqrt{V_{IN}^2}$

Amplitude Modulator with A.G.C.

In many AC modulator applications, unwanted output modulation is caused by variations in carrier input amplitude. The versatility of the RC4200 multiplier can be utilizes to eliminate this undesired fluctuation. The extended range multiplier circuit (Figure 4) shows an output amplitude inversely proportional to the reference voltage V_{REF}.

$$\text{i.e., } V_0 = \frac{V_X V_Y}{V_{REF}} \frac{R_0 R_d}{R_1 R_2}$$

By making V_{REF} proportional to V_Y (where V_Y is the carrier input) such that:

$$V_{REF} = V_H = \int(|V_Y|)$$

Then the denominator becomes a variable value that automatically provides constant gain, such that the modulating input (V_X) modulates the carrier (V_Y) with a fixed scale factor even though the carrier varies in amplitude.

If V_H is made proportional to the average value of Asinωt (i.e., 2A/π) and scaled by a value of π/2 then:

V_H=A

and if: V_X = Modulating input (V_M)

and: V_Y Carrier input (Asinωt)

Then: $V_0 = K V_M \sin\omega t$ where $K = \frac{R_0 R_d}{R_1 R_2}$

The resistor scaling is determined by the dynamic range of the carrier variation and modulating input.

The resistor values are solved, as with the other extended range circuits, in terms of the input voltages.

Input voltages:

Modulation voltage (V_M): $0 \le V_M \le V_X$(max.)
Carrier (V_Y): V_Y = Asinωt
Carrier amplitude fluctuation (ΔA):
A(min.) sint ≤ V_Y ≤ A(max.) sinΩωt
Dynamic Range (N): A(max.)/A(min.),
A(max.) = V_H(max.) and A(min.) = V_H(min.)

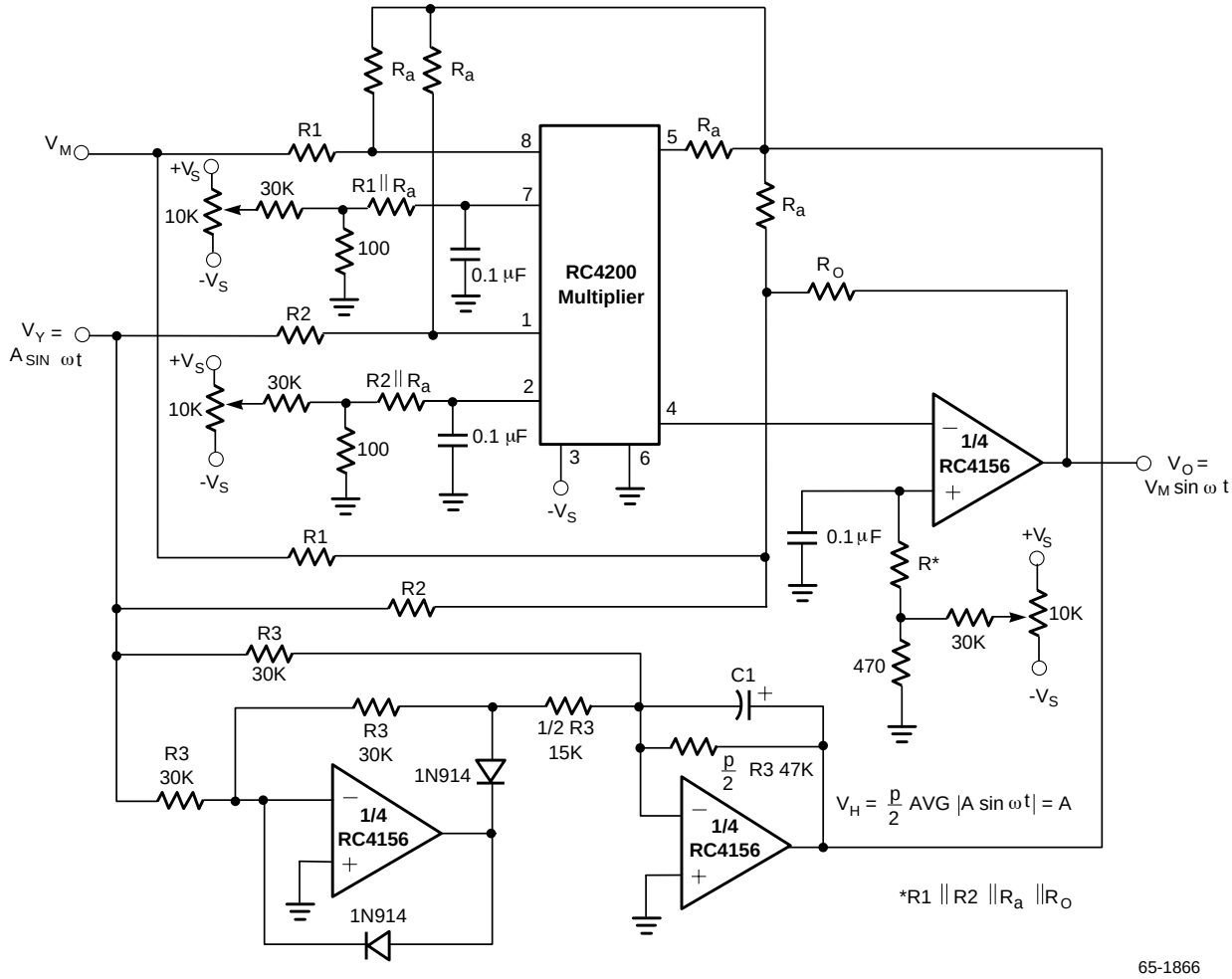


Figure 16. Amplitude Modulator with A.G.C.

The maximum and minimum values for I_1 and I_2 lead to:

$$I_1(\text{max.}) = \frac{V_X(\text{max.})}{R_1} + \frac{V_H(\text{max.})}{R_a} = 250\mu A$$

$$I_1(\text{min.}) = \frac{V_H(\text{min.})}{R_a} = 50\mu A \; V_M(\text{min.}) = 0$$

$$I_2(\text{max.}) = \frac{A(\text{max.})}{R_2} + \frac{V_H(\text{max.})}{R_a} = 250\mu A$$

$$I_2(\text{min.}) = \frac{V_H(\text{min.})}{R_a} = 50\mu A$$

For a dynamic range of N, where

$$N = \frac{A(\text{max.})}{A(\text{min.})} < 5,$$

These equations combine to yield:

$$R_1 = \frac{V_X(\text{max.})}{(5-N)50\mu A}, \; R2\frac{A(\text{max.})}{(5-N)50\mu A},$$

$$R_a = \frac{A(\text{min.})}{50\mu A} \text{ and } R_O = K\frac{R_1R_2}{R_a},$$

Example 1

$V_Y = A\sin\omega t$ 2.5V ≤ A ≤ 10V, therefore N = 4
0V ≤ V_M ≤ 10V, therefore V_X(max.) = 10V
K = 1, therefore $V_0 = V_M \sin\omega t$

$$R_1 = \frac{V_X(\text{max.})}{50\mu A} = \frac{10V}{50\mu A} = 200K$$

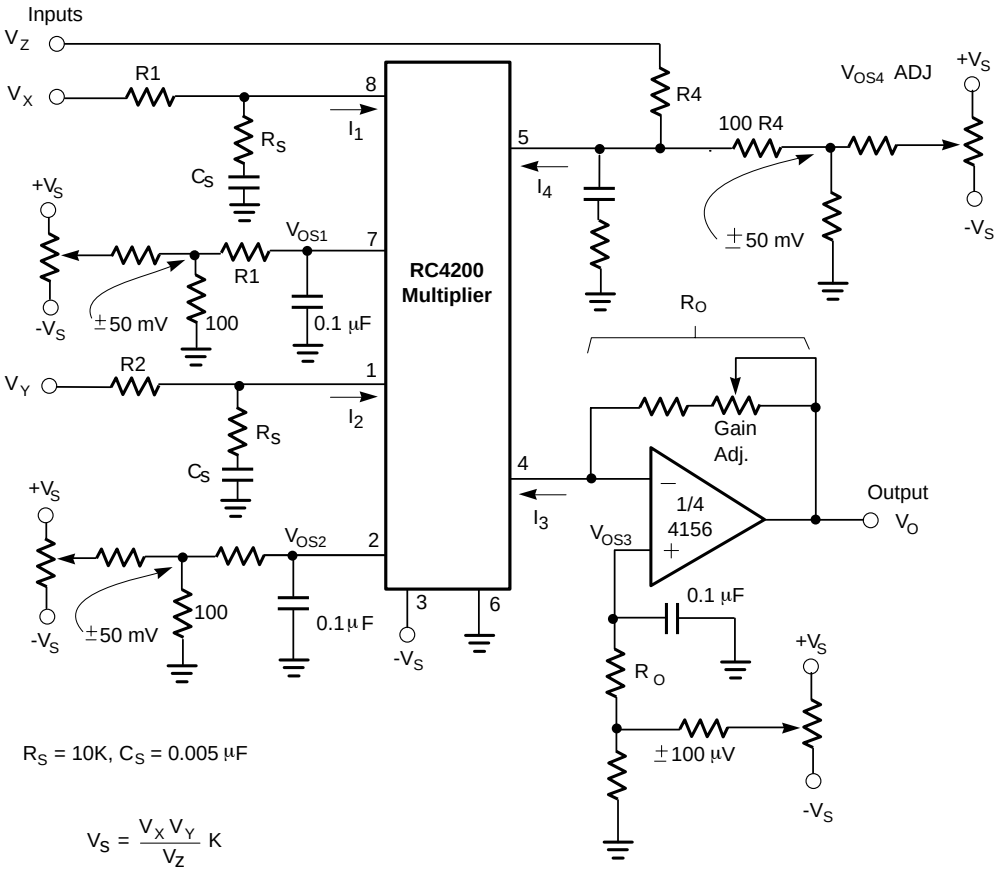
$$R_1 = \frac{A(\text{max.})}{50\mu A} = \frac{10V}{50\mu A} = 200K$$

$$R_a = \frac{A(\text{min.})}{50\mu A} = \frac{2.5V}{50\mu A} = 50K$$

$$R_O = K\frac{R_1R_2}{R_a} = 1\frac{200K \times 200K}{50K} = 800K$$

Example 2

$V_Y = A\sin\omega t$ 3 ≤ A ≤ 6, therefore N = 2
0V ≤ V_M ≤ 8V, therefore V_X(max.) = 8V
K = 0.2, therefore $V_0 = 0.2\, V_M \sin wt$
so:
R_1 = 53.3K, R_2 = 40K
R_a = 60K and R_0 = 7.11K



R_S = 10K, C_S = 0.005 µF

$$V_S = \frac{V_X V_Y}{V_Z} K$$

Where $K = \frac{R_O R4}{R1\ R2}$

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Limited Range, First Quadrant Applications

The following circuit has the advantage that cross-product errors are due only to input offsets and nonlinearity error is sightly error is slightly less for lower input currents.

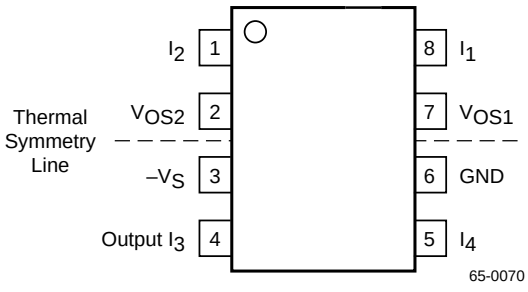
The circuit also has no standby current to add to the noise content, although the signal-to-noise ratio worsens at very low input currents (1-5 µA) due to the noise current of the input stages.

The $R_S C_S$ filter circuits are added to each input to improve the stability for input currents below 50 µA.

Caution!

The bandpass drops off significantly for lower currents (<50 µA) and non-symmetrical rise and fall times can cause second harmonic distortion.

Thermal Symmetry



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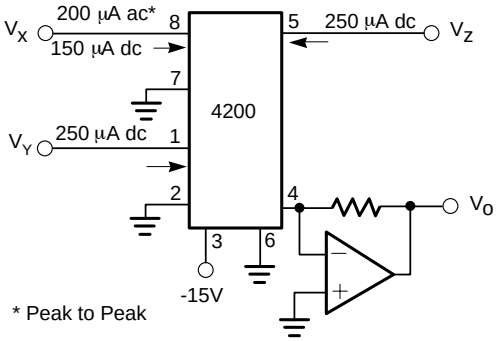
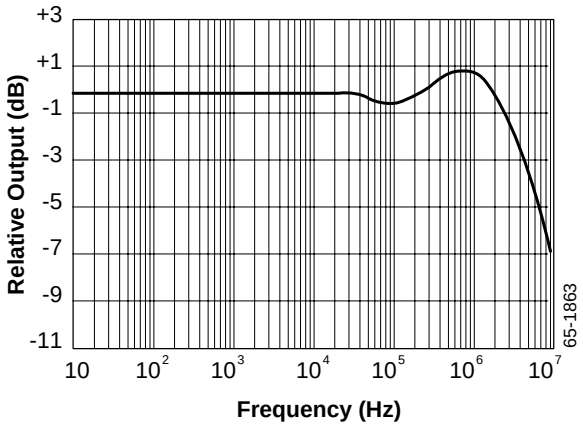
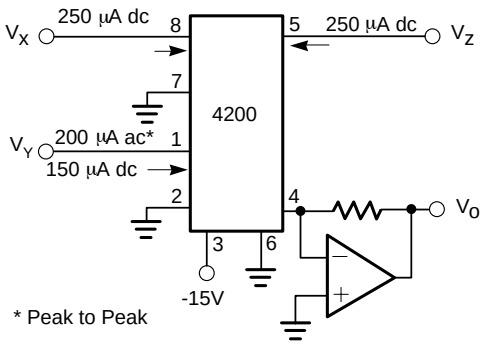
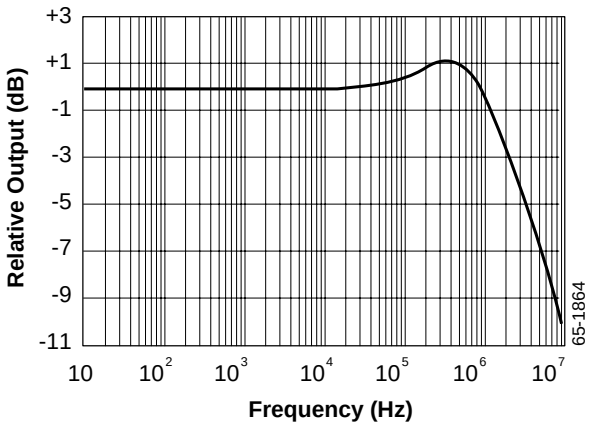
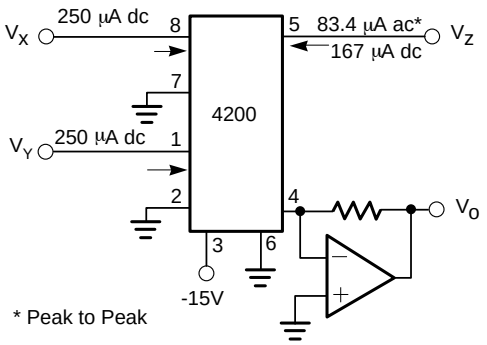
The scale factor is sensitive to temperature gradients across the chip in the lateral direction. Where possible, the package should be oriented such that forces generating temperature gradients are located physically on the line of thermal symmetry. This will minimize scale-factor error due to thermal gradients.











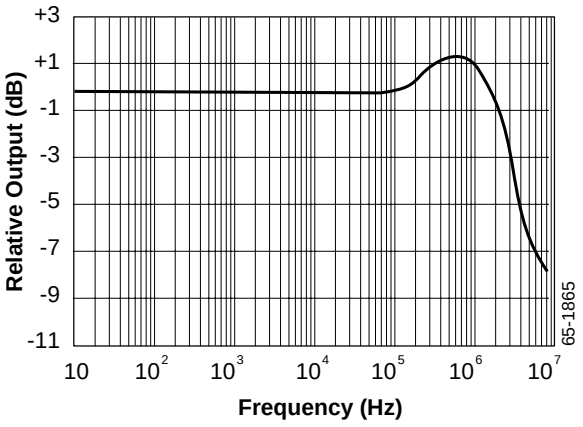


Figure 18. Outputs

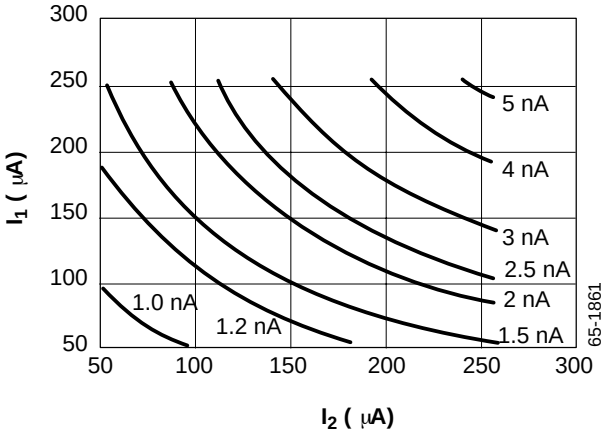


Figure 19a. Output Noise Current (I_3) vs. Input Currents (I_1, I_2) for I_4 = 250μA

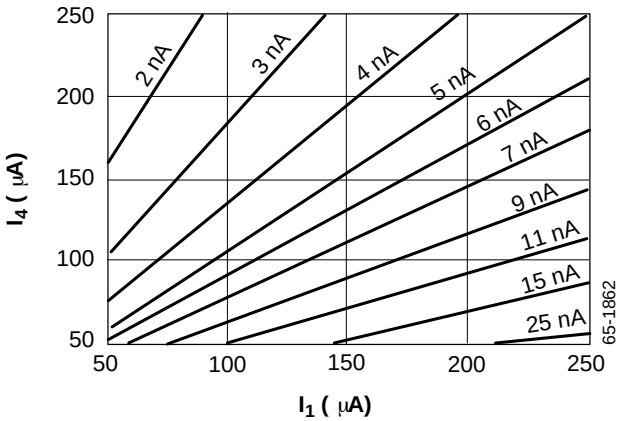


Figure 19b. Output Noise Current (I_3) vs. Input Currents (I_4, I_1) for I_2 = 250μA

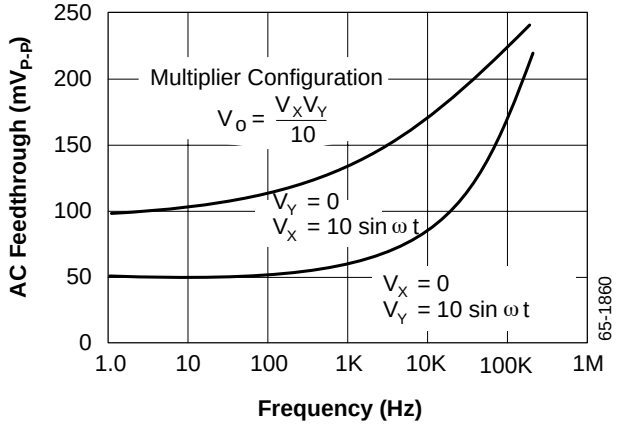


Figure 20. AC Feedthrough vs. Frequency

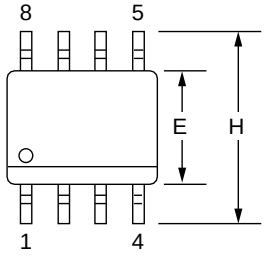
Mechanical Dimensions

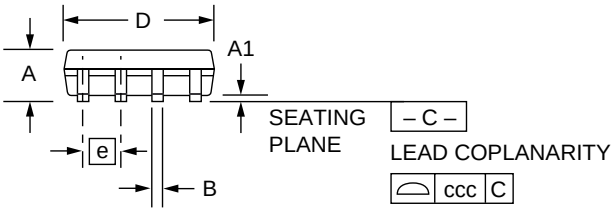
8-Lead SOIC Package

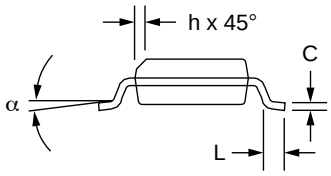
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.20	0.25	5
D	.189	.197	4.80	5.00	2
E	.150	.158	3.81	4.01	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	8		8		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







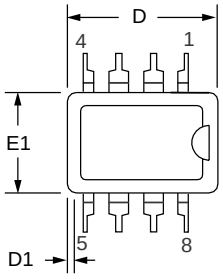
Mechanical Dimensions (continued)

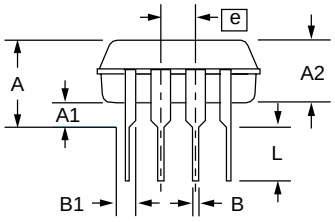
8-Lead Plastic DIP Package

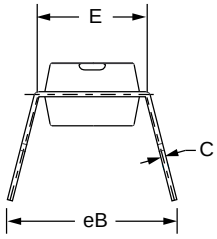
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	.348	.430	8.84	10.92	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.160	2.92	4.06	
N	8°		8°		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.







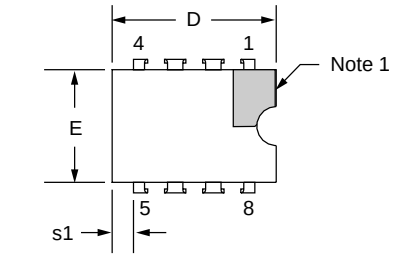
Mechanical Dimensions (continued)

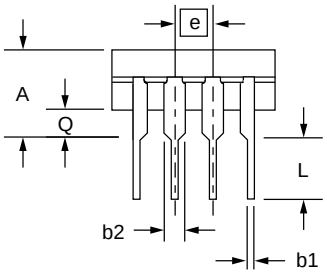
8-Lead Ceramic DIP Package

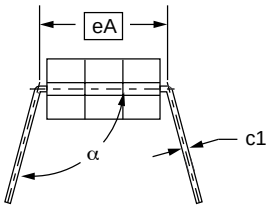
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2, 8
c1	.008	.015	.20	.38	8
D	—	.405	—	10.29	4
E	.220	.310	5.59	7.87	4
e	.100 BSC		2.54 BSC		5, 9
eA	.300 BSC		7.62 BSC		7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 4, 5 and 8 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 8.
6. Applies to all four corners (leads number 1, 4, 5, and 8).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Six spaces.







Ordering Information

Part Number	Package	Operating Temperature Range
RC4200N	8-Lead Plastic DIP	0°C to +70°C
RC4200AN	8-Lead Plastic DIP	0°C to +70°C
RC4200M	8-Lead SOIC	0°C to +70°C
RC4200AM	8-Lead SOIC	0°C to +70°C
RM4200D	8-Lead Ceramic DIP	-55°C to +125°C
RM4200AD	8-Lead Ceramic DIP	-55°C to +125°C
RM4200AD/883B	8-Lead Ceramic DIP	-55°C to +125°C

Note:
/883B suffix denotes MIL-STD-883, Level B processing

5/20/98 0.0m 001
Stock#DS30004200

RC4207

Precision Monolithic Dual Operational Amplifier

Features

- Low Noise – 0.35 μV_{p-p} (0.1 Hz to 10 Hz)
- Ultra-low V_{OS} – 75 μV
- Ultra-low V_{OS} drift – 1.3 $\mu V/°C$
- Long term V_{OS} stability – 0.2 $\mu V/Mo$
- Low input bias and offset currents – ±5 nA
- High gain – 400 V/mV
- Fits 4558 socket
- Industry standard pinout
- 8-lead mini-DIP

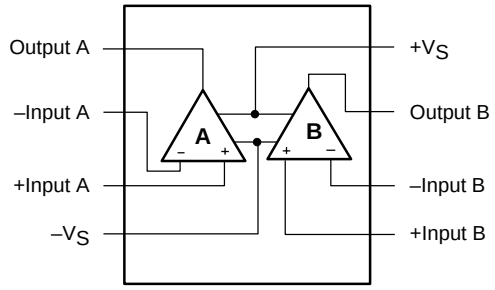
Description

Designed for low level signal conditioning and instrumentation applications, the 4207 is a precision dual amplifier combining excellent DC input specifications with low input noise characteristics. Ultra low input offset voltage, low drift, high CMRR, and low input bias currents serve to reduce input related errors to less than 0.01% in a typical high gain instrumentation amplifier system (A_V = 1000). The 4207 contains two separate amplifiers with a high degree of isolation between them; each is complete requiring no external compensation capacitors or offset nulling potentiometers.

The inherent V_{OS} is typically less than 150 μV, resulting in superior temperature drift, and this low initial offset is further reduced by "Zener-zap" nulling when the wafers are tested.

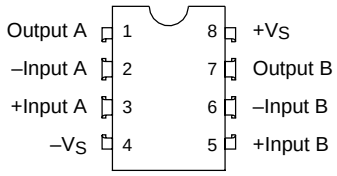
Advanced thin film and nitride dielectric processing allows the 4207 to achieve its high performance and small size (the 4207 is offered in 8-lead DIPs). The 4207 fits the industry standard 8-lead op amp pin-out.

Block Diagram



65-3468-01

Pin Assignments



65-4207-02

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min	Typ	Max	Units
Supply Voltage				±18	V
Input Voltage[2]				±18	V
Differential Input Voltage				30	V
Internal Power Dissipation[3]				500	mW
$P_D T_A$ < 50°C				468	mW
Output Short Circuit Duration		Indefinite			
Junction Temperature				125	°C
Storage Temperature		-65		150	°C
Operating Temperature		0		70	°C
Lead Soldering Temperature (60 sec)				300	°C
For T_A > 50°C Derate at			6.25		mW/°C

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.
3. Observe package thermal characteristics.

Operating Conditions

Parameter		Min	Typ	Max	Units
θ_{JA}	Thermal resistance		160		°C/W

Electrical Characteristics

(V_S = ±15V, 0°C ≤ T_A ≤ +70˚C unless otherwise noted)

Parameters	Test Conditions	4207F			4207G			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage			45	150		85	250	μV
Average Input Offset Voltage Drift[2]			0.3	1.3		0.7		μV/°C
Input Offset Current			±2.0	±10		±1.6	±15	nA
Average Input Offset Current Drift			8.0			12		pA/°C
Input Bias Current			±2.0	±10		±3.0	±15	nA
Average Input Bias Current Drift			13			18		pA/°C
Input Voltage Range		±10	±13.5		±10	±13.5		V
Common Mode Rejection Ratio	V_{CM} = ±10V	94	120		92	106		dB
Power Supply Rejection Ratio	V_S = ±4.0V to ±16.5V	94	115		92	100		dB
Large Signal Voltage Gain	R_L > 2.0kΩ, V_{OUT} = ±10V	200	450		75	400		V/mV
Maximum Output Voltage Swing	R_L > 2.0kΩ	±11	±12.6		±11	±12.6		V
Power Consumption	R_L = ∞		150	240		150	240	mW

Electrical Characteristics

(V_S = ±15V, and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	4207F			4207G			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[3]			30	75		60	150	μV
Long Term V_{OS} Stability[1]			0.2			0.5		μV/Mo
Input Offset Current			±0.5	±5		±2	±10	nA
Input Bias Current			±0.5	±5		±2	±10	nA
Input Noise Voltage	0.1 Hz to 10 Hz		0.35			0.35		μVp-p
Input Noise Voltage Density	F_O = 10 Hz		10.3			10.3		$\frac{nV}{\sqrt{Hz}}$
	F_O = 100 Hz		10			10		
	F_O = 1000 Hz		9.6			9.6		
Input Noise Current	0.1 Hz to 10 Hz		14			14		pA_{p-p}
Input Noise Current Density	F_O = 10 Hz		0.32			0.32		$\frac{pA}{\sqrt{Hz}}$
	F_O = 100 Hz		0.14			0.14		
	F_O = 1000 Hz		0.12			0.12		
Input Resistance (Diff. Mode)			60			31		MΩ
Input Resistance (Com. Mode)			200			120		GΩ
Input Voltage Range[4]		±11	±14		±11	±14		V
Common Mode Rejection Ratio	V_{CM} = ±11V	100	126		94	110		dB
Power Supply Rejection Ratio	V_S = ±4.0V to ±16.5V	100	110		94	104		dB
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	400	600		250	400		V/mV
	V_{OUT} = ±1.0V, R_L = 1KΩ, V_S = ±4.0V	200	400		100	200		
Output Voltage Swing	$R_L \geq 10k\Omega$	±12.5	±13		±12.5	±13		V
	$R_L \geq 2k\Omega$	±12	±12.8		±12	±12.8		
	$R_L \geq 1k\Omega$	±11	±12		±11	±12		
Slew Rate	$R_L \geq 2k\Omega$	0.1	0.3		0.1	0.3		V/μs
Closed Loop Bandwidth	A_{VOL} = +1.0		1.5			1.5		MHz
Open Loop Output Resistance	V_{OUT} = 0, I_{OUT} = 0		60			60		Ω
Power Consumption	V_S = ±15V, R_L = ∞		150	200		160	240	mW
	V_S = ±4.0V, R_L = ∞		35	50		48	64	
Crosstalk	DC	126	155		126	155		dB

Notes:

1. Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 μV.
2. Guaranteed by design.
3. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
4. The input protection diodes do not allow the device to be removed or inserted into the circuit without first removing power.

Typical Performance Characteristics

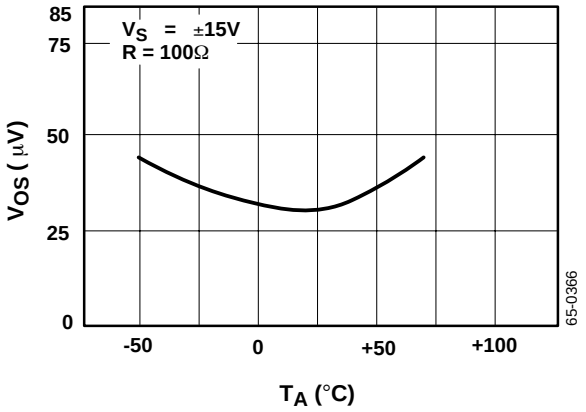


Figure 1. Input Offset Voltage vs. Temperature

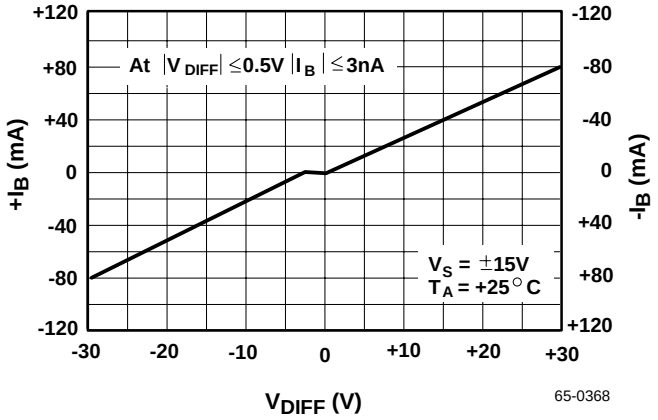


Figure 2. Input Bias Current vs. Differential Input Voltage

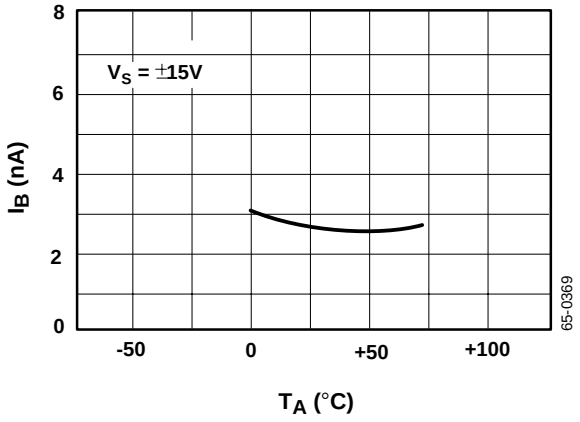


Figure 3. Input Bias Current vs. Temperature

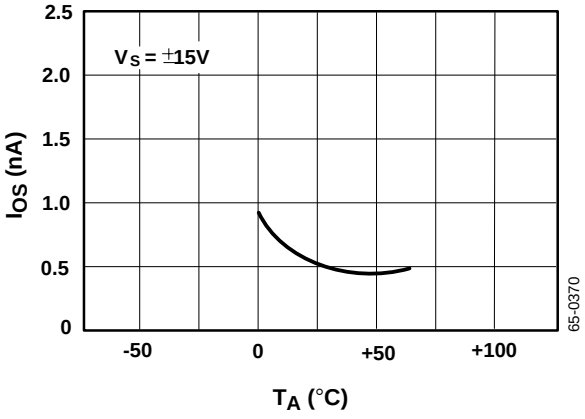


Figure 4. Input Offset Current vs. Temperature

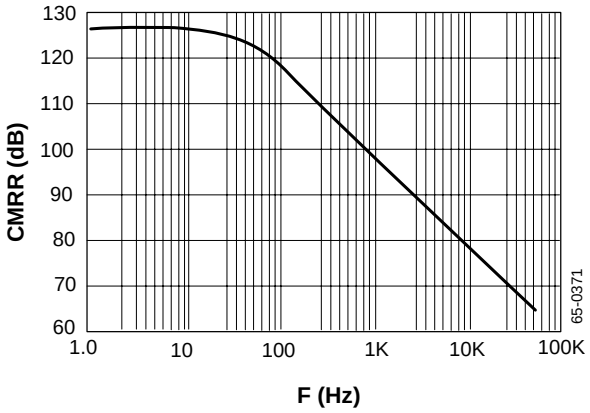


Figure 5. CMRR vs. Frequency

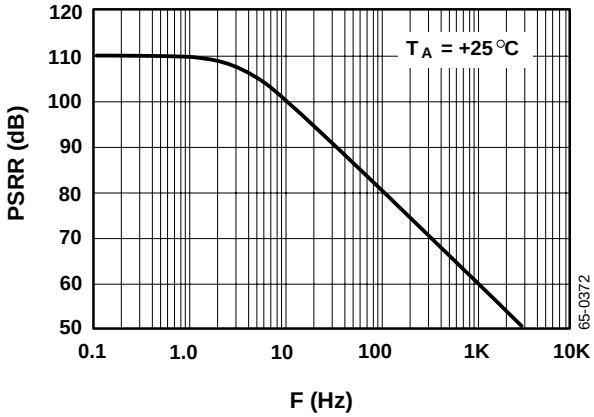


Figure 6. PSRR vs. Frequency

Typical Performance Characteristics (continued)

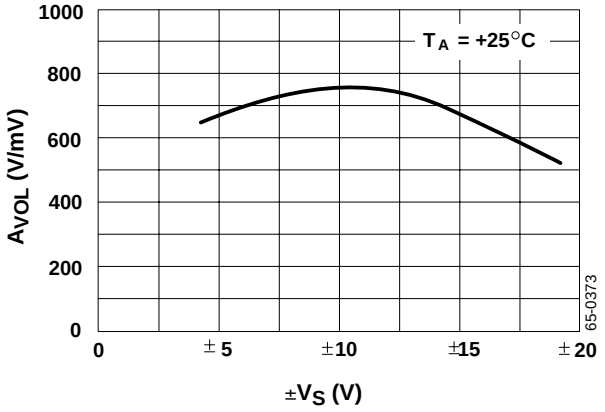


Figure 7. Open Loop Gain vs. Supply Voltage

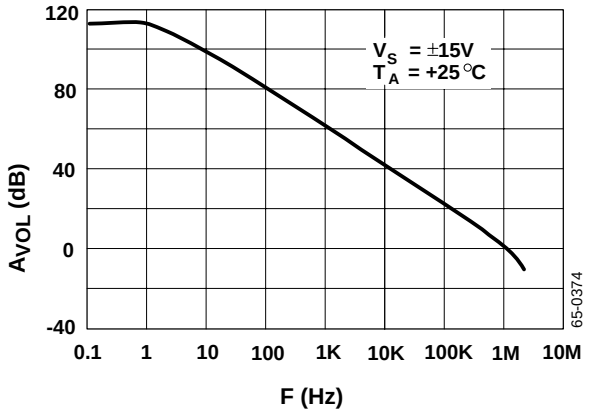


Figure 8. Open Loop Gain vs. Frequency

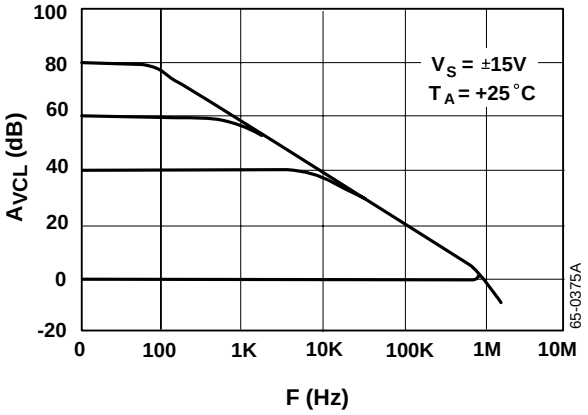


Figure 9. Closed Loop Response for Various Gain Configurations

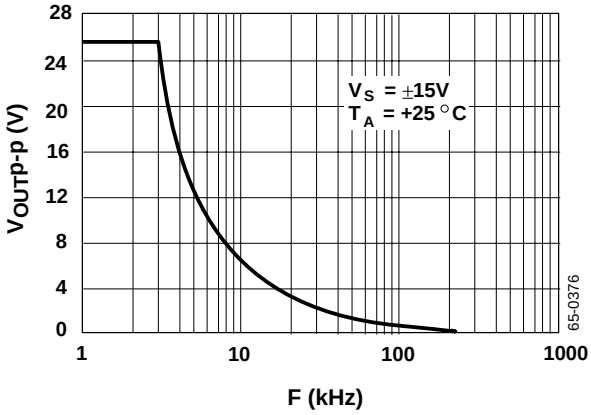


Figure 10. Maximum Undistorted Output vs. Frequency

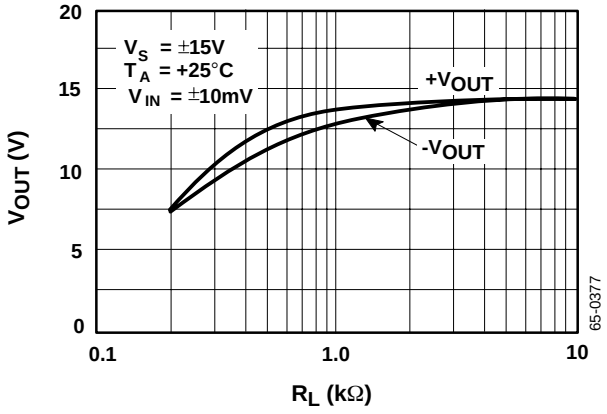


Figure 11. Output Voltage vs. Load Resistance to Ground

Typical Performance Characteristics (continued)

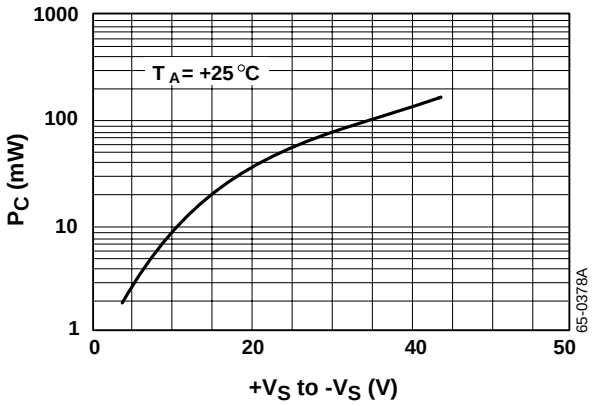


Figure 12. Power Consumption vs. Total Supply Voltage

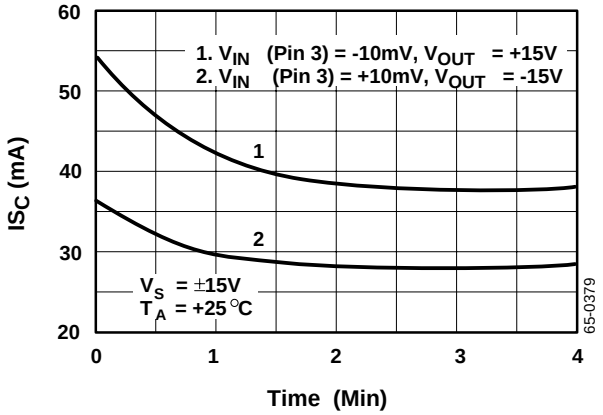


Figure 13. Output Short Circuit Current vs. Time

Typical Applications

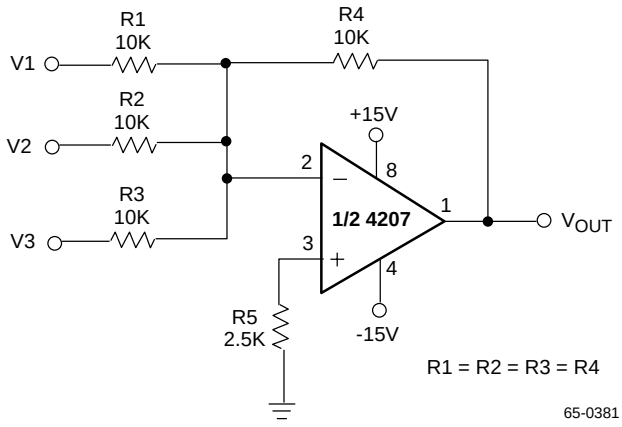


Figure 14. Adjustment-Free Precision Summing Amplifier

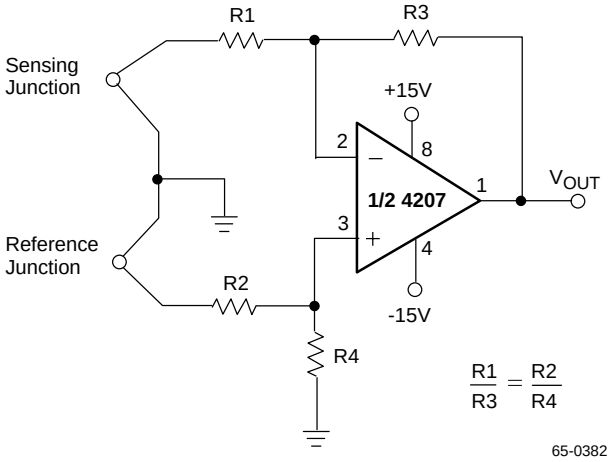


Figure 15. High Stability Thermocouple Amplifier

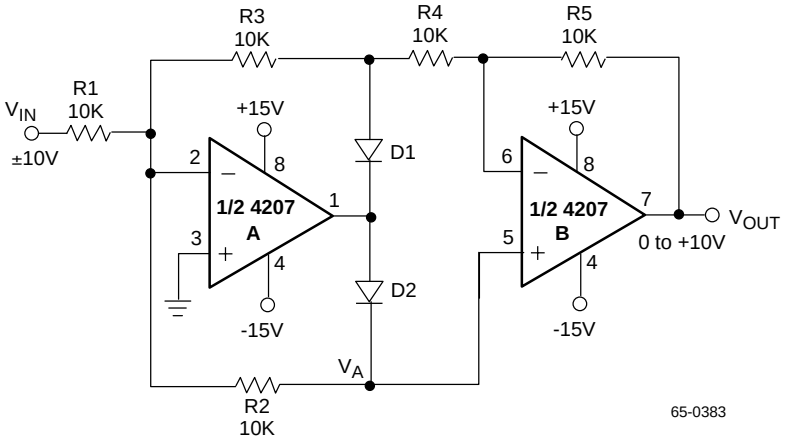
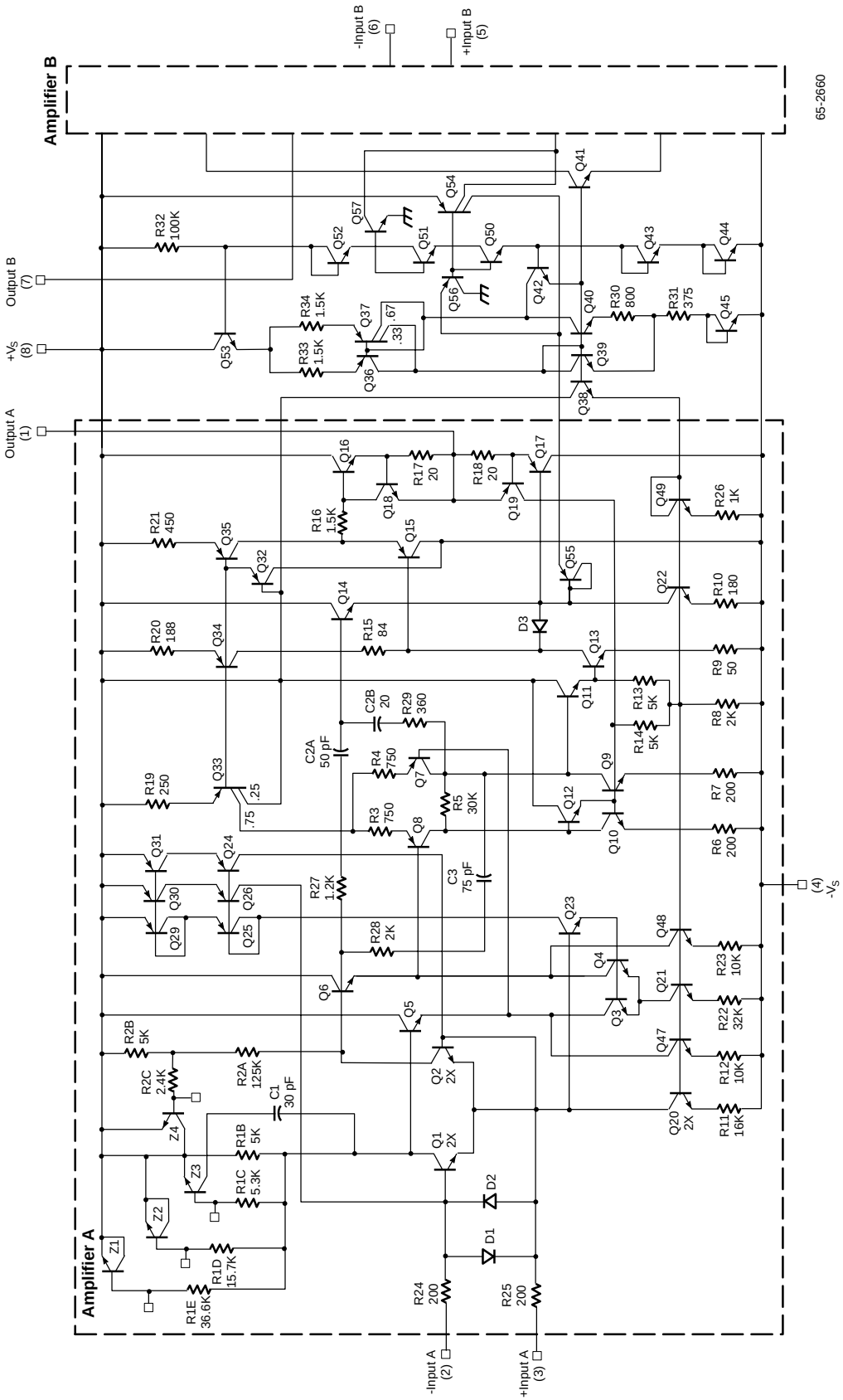


Figure 16. Precision Absolute Value Circuit

Schematic Diagram

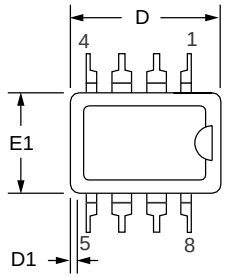


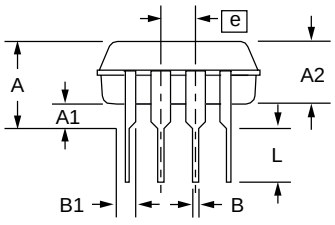
Mechanical Dimensions – 8-Lead Plastic DIP Package

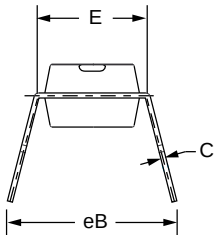
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	.348	.430	8.84	10.92	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.160	2.92	4.06	
N	8°		8°		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.







Ordering Information

Product Number	Temperature Range	Screening	Package
RC4207FN	0° to +70°C	Commercial	8 Pin Plastic DIP
RC4207GN	0° to +70°C	Commercial	8 Pin Plastic DIP

RC4227

Dual Precision Operational Amplifier

Features

- Very low noise
  Spectral noise density – 3.8 nV/√Hz
  1/F noise corner frequency – 2.7 Hz
- Very low VOS drift – 0.3 μV/Mo; 0.3 μV/˚C
- High gain – 500 V/mV
- High output drive capability – ±10V into 1K load
- High slew rate – 2.7 V/μS
- Wide gain bandwidth product – 8 MHz
- High common mode rejection ratio – 104 dB
- Low input offset voltage – 75 μV
- Low frequency noise – 0.08 μV_{p-p} (0.1 Hz to 10 Hz)
- Low input offset current – 2.5 nA
- Industry standard pinout
- 8-Lead DIP

Description

The RC4227, a dual version of the OP-27, is designed for instrumentation grade signal conditioning where low noise (both spectral density and burst), wide bandwidth, and high slew rate are required along with low input offset voltage, low input offset temperature coefficient, and low input bias currents. These features are all available in a device which is internally compensated for excellent phase margin (70˚) in a unity gain configuration. Digital nulling techniques performed at wafer sort make it feasible to guarantee temperature stable input offset voltages as low as 75 μV max. Input bias current cancellation techniques are used to obtain ±45 nA max. input bias currents.

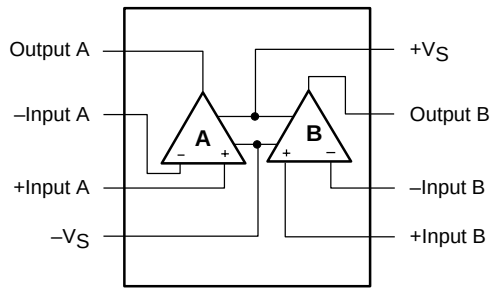
In addition to providing superior performance for audio frequency range applications, the RC4227 design uniquely addresses the needs of the instrumentation designer. Power supply rejection and common mode rejection are both in excess of 100 dB. A phase margin of 70˚ at unity gain guards against peaking (and ringing) in low gain feedback circuits. Stable operation can be obtained with capacitive loads up to 2000 pF[1]. The drift performance is, in fact, so good that the system designer must be cautioned that stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals are enough to degrade its performance. For this reason it is also important to keep both input terminals at the same relative temperature.

The performance of the RC4227 is achieved using precision amplifier design techniques coupled with a process that combines nitride transistors and capacitors with precision thin-film resistors. The die size savings of nitride capacitors and thin film resistors allow the RC4227 to be offered in an 8-pin mini-dip package and fit the industry standard dual op amp pinout.

Note:

1. By decoupling the load capacitance with a series resistor of 50Ω or more, load capacitances larger than 2000 pF can be accommodated.

Block Diagram



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Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min	Typ	Max	Units
Supply Voltage				±18	V
Input Voltage[2]				±18	V
Differential Input Voltage				0.7	V
Internal Power Dissipation[3]				658	mW
$P_D T_A$ < 50°C	PDIP			468	mW
	CerDIP			833	
Output Short Circuit Duration		Indefinite			
Junction Temperature	PDIP			125	°C
	CerDIP			175	
Storage Temperature		-65		150	°C
Operating Temperature	RM4227B	-55		125	°C
	RC4227F/G	0		70	
Lead Soldering Temperature (60 sec)				300	°C
For T_A > 50°C Derate at	PDIP		6.25		mW/°C
	CerDIP		8.33		

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.
3. Observe package thermal characteristics.

Operating Conditions

Parameter			Min	Typ	Max	Units
θ_{JC}	Thermal resistance	CerDIP		45		°C/W
θ_{JA}	Thermal resistance	PDIP		160		°C/W
		CerDIP		150		°C/W

Electrical Characteristics

(V_S = ±15V, and $T_A \leq$ +25°C unless otherwise noted)

Parameters	Test Conditions	4227B/F			4227G			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[3]			20	150		30	180	μV
Long Term V_{OS} Stability[1]			0.3			0.4		μV/Mo
Input Offset Current			±2.5	±10		±5	±15	nA
Input Bias Current			±5	±15		±7.5	±25	nA
Input Noise Voltage	0.1 Hz to 10 Hz		0.08			0.08		μV_{p-p}
Input Noise Voltage Density	F_O = 10 Hz		3.8			3.8		$\frac{nV}{\sqrt{Hz}}$
	F_O = 30 Hz		3.3			3.3		
	F_O = 1000 Hz		3.2			3.2		
Input Noise Current Density	F_O = 10 Hz		1.7			1.7		$\frac{pA}{\sqrt{Hz}}$
	F_O = 30 Hz		1.0			1.0		
	F_O = 1000 Hz		0.4			0.4		
Input Resistance (Diff. Mode)			5.0			4.0		MΩ
Input Resistance (Com. Mode)			2.5			2.0		GΩ
Input Voltage Range[2, 4]		±11	±12.3		±11	±12.3		V
Common Mode Rejection Ratio	V_{CM} = ±11V	104	123		100	120		dB
Power Supply Rejection Ratio	V_S = ±4.0V to ±16.5V	104	120		100	118		dB
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	500	1000		400	800		V/mV
	V_{OUT} = ±10V, R_L = 1KΩ	400	800		300	600		
	V_{OUT} = ±1.0V V_S = ±4.0V, $R_L \geq 1.0k\Omega$	250	500		200	400		
Output Voltage Swing	$R_L \geq 2.0k\Omega$	±12	±13.8		±12	±13.8		V
	$R_L \geq 1k\Omega$	±11	±12		±11	±12		
Slew Rate[2]	$R_L \geq 2.0k\Omega$	1.5	2.7		0.1	0.3		V/μs
Gain Bandwidth Product		5.0	8.0		5.0	8.0		MHz
Open Loop Output Resistance	V_{OUT} = 0, I_{OUT} = 0		70			70		Ω
Power Consumption	$R_L = \infty$		160	200		180	240	mW
Crosstalk		126	155		126	155		dB

Notes:

1. Long Term Input Offset Voltage Stability refers to the averaged trend line of VOS vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in VOS during the first 30 operating days are typically 2.5 μV.
2. Guaranteed by design.
3. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
4. The input protection diodes do not allow the device to be removed or inserted into the circuit without first removing power.

Electrical Characteristics

(V_S = ±15V, -55˚C ≤ T_A ≤ +125˚C unless otherwise noted)

Parameters	Test Conditions	4227B			Units
		Min	Typ	Max	
Input Offset Voltage[1]			120	400	μV
Average Input Offset Voltage Drift[2]			0.3	3.5	μV/˚C
Input Offset Current			±10	±35	nA
Input Bias Current			±15	±45	nA
Input Voltage Range		±10	±11.5		V
Common Mode Rejection Ratio	V_{CM} = ±10V	100	119		dB
Power Supply Rejection Ratio	V_S = ±4.0V to ±16.5V	100	114		dB
Large Signal Voltage Gain	R_L ≥ 2 kΩ, V_{OUT} = ±10V	350	650		V/mV
Output Voltage Swing	R_L ≥ 2.0 kΩ	±11	±13.2		V
Power Consumption	R_L = ∞		200	280	mW

Notes:

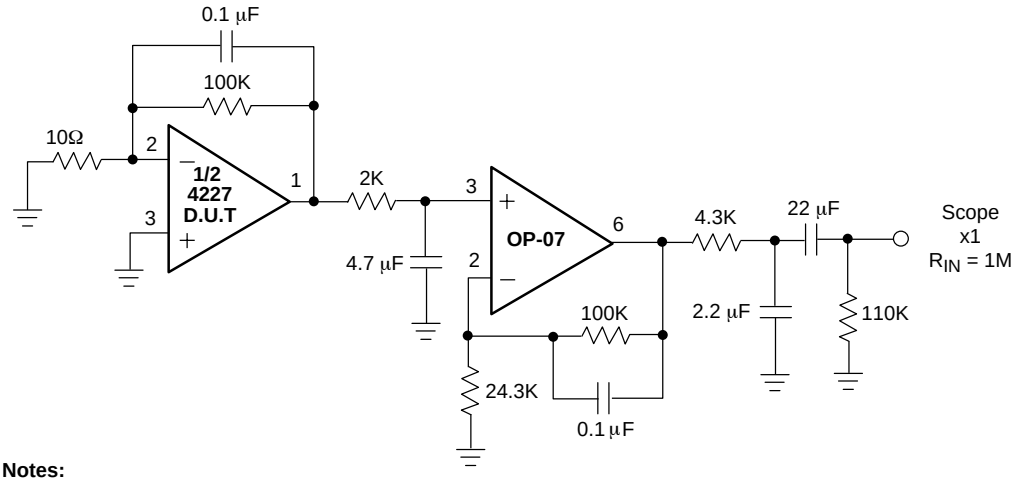
1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. This parameter is tested on a sample basis only.

Electrical Characteristics

(V_S = ±15V, 0°C ≤ T_A ≤ +70˚C unless otherwise noted)

Parameters	Test Conditions	4227F			4227G			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage			45	150		85	250	μV
Average Input Offset Voltage Drift[2]			0.3	1.3		0.4		μV/°C
Input Offset Current			±8	±15		±10	±35	nA
Input Bias Current			±10	±30		±15	±45	nA
Input Voltage Range		±10	±11.8		±10	±11.8		V
Common Mode Rejection Ratio	V_{CM} = ±10V	100	121		92	118		dB
Power Supply Rejection Ratio	V_S = ±4.0V to ±16.5V	100	116		92	114		dB
Large Signal Voltage Gain	R_L > 2.0kΩ, V_{OUT} = ±10V	350	700		250	500		V/mV
Output Voltage Swing	R_L > 2.0kΩ	±11	±13.5		±11	±13.5		V
Power Consumption	R_L = ∞		180	240	200	280		mW

Typical Performance Characteristics



Notes:
1. Peak-to-peak noise measured in a 10-second interval.
2. The device under test should be warmed up for 3 minutes and shielded from air currents.
3. Voltage gain = 50,000.

65-3469-01

Figure 1. 0.1 Hz to 10 Hz Noise Test Circuit (1/2 Shown)

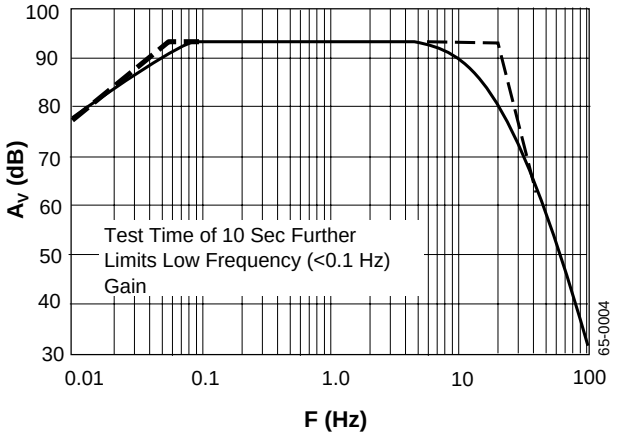


Figure 2. 0.1Hz to 10Hz Noise Gain vs. Frequency

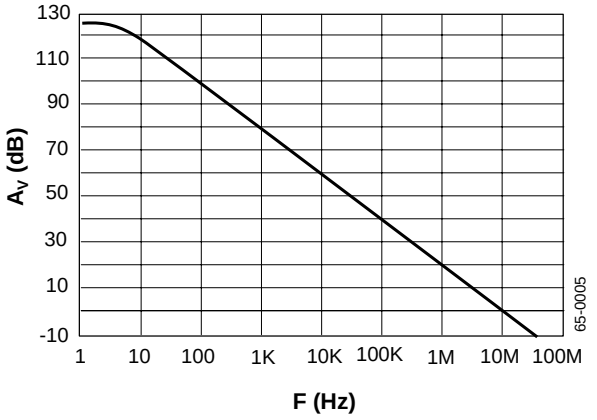


Figure 3. Open Loop Gain vs. Frequency

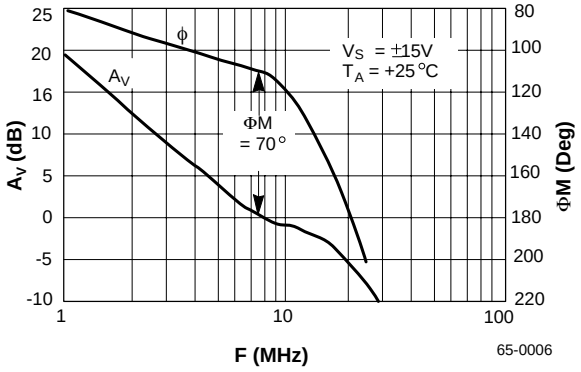


Figure 4. Gain, Phase Shift vs. Frequency

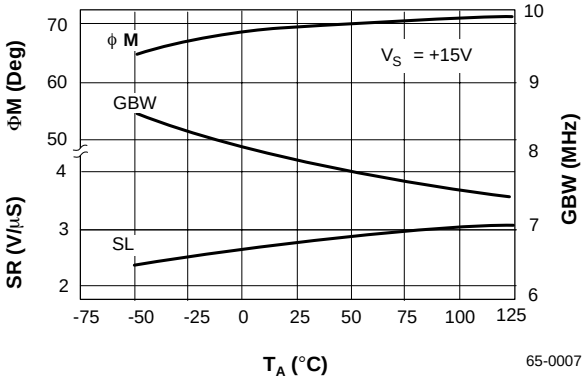


Figure 5. Slew Rate, Gain Bandwidth Product, Phase Margin vs. Temperature

Typical Performance Characteristics (continued)

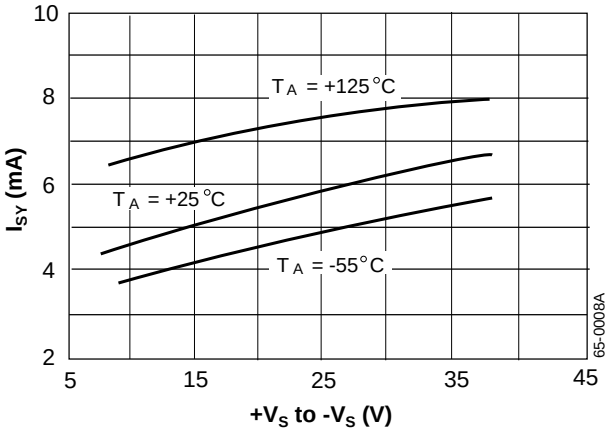


Figure 6. Supply Voltage vs. Total Supply Voltage

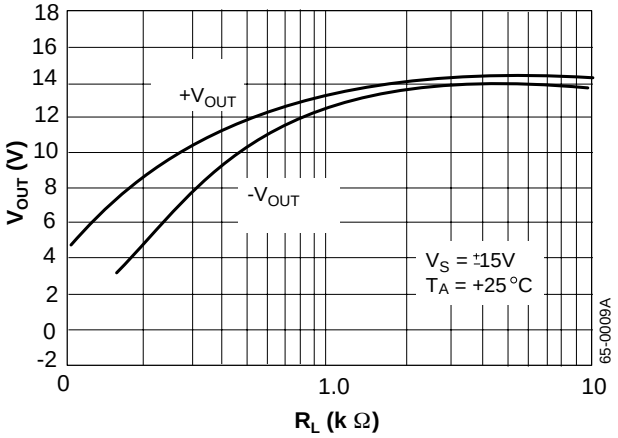


Figure 7. Maximum Output Swing vs. Load Resistance

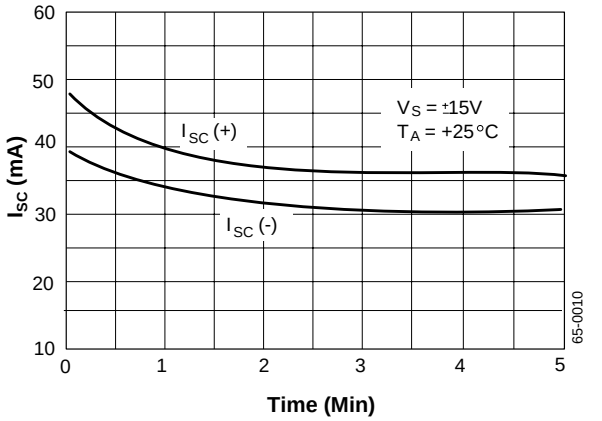


Figure 8. Short Circuit vs. Time

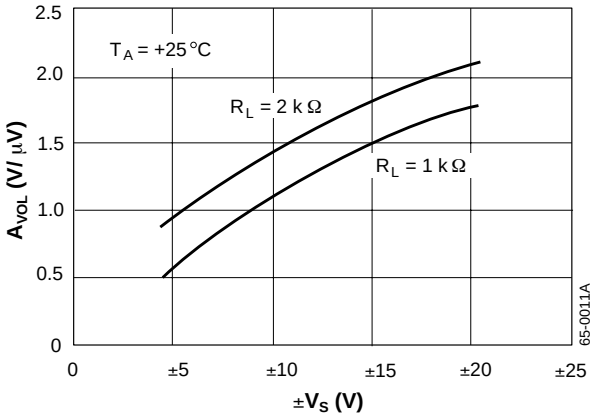


Figure 9. Open-Loop Gain vs. Total Supply Voltage

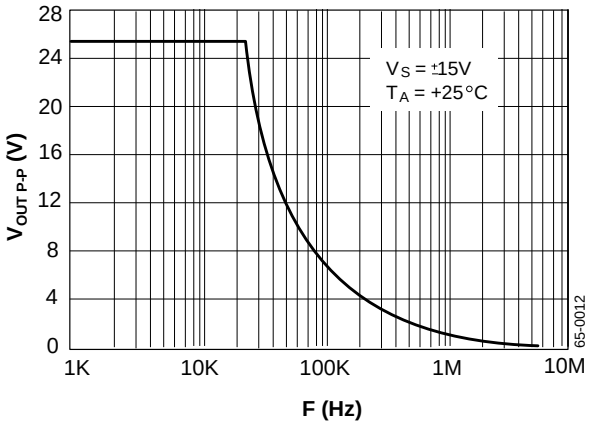


Figure 10. Maximum Undistorted Output vs. Frequency

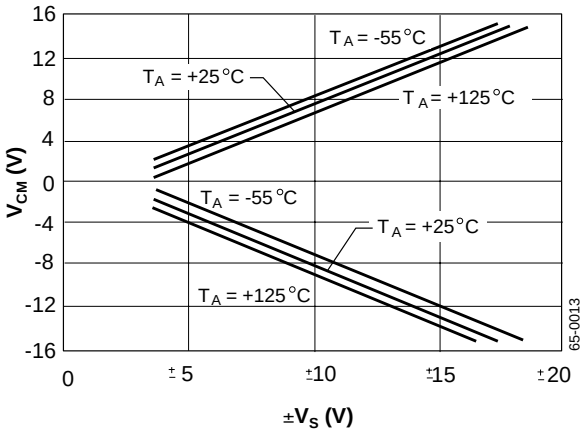


Figure 11. Common-Mode Input Range vs. Supply Voltage

Typical Performance Characteristics (continued)

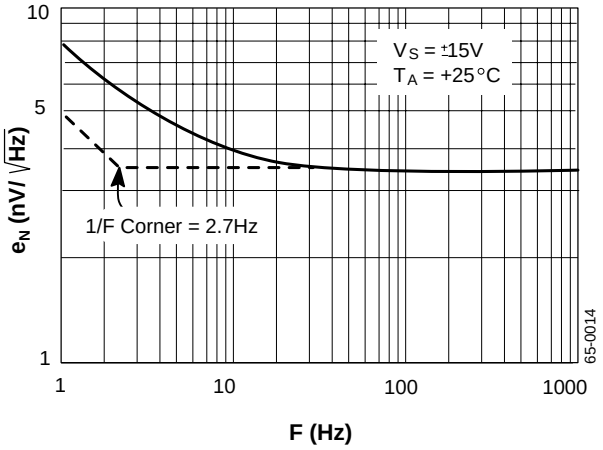


Figure 12. Input Noise Voltage Density vs. Frequency

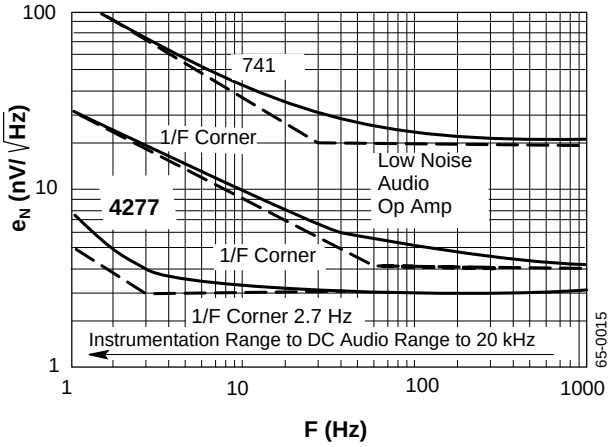


Figure 13. Op Amp Compensation Input Noise Voltage Density vs. Frequency

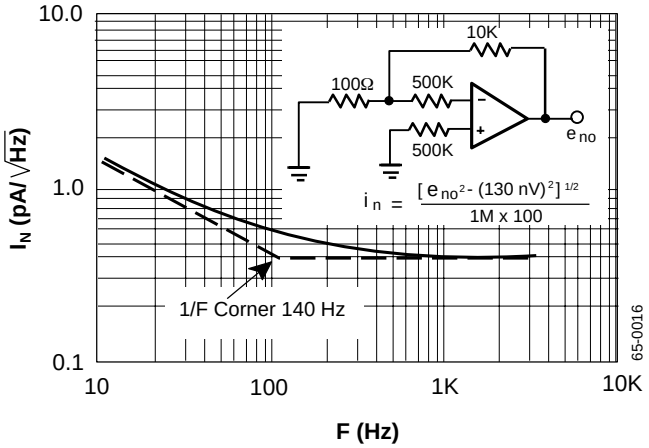
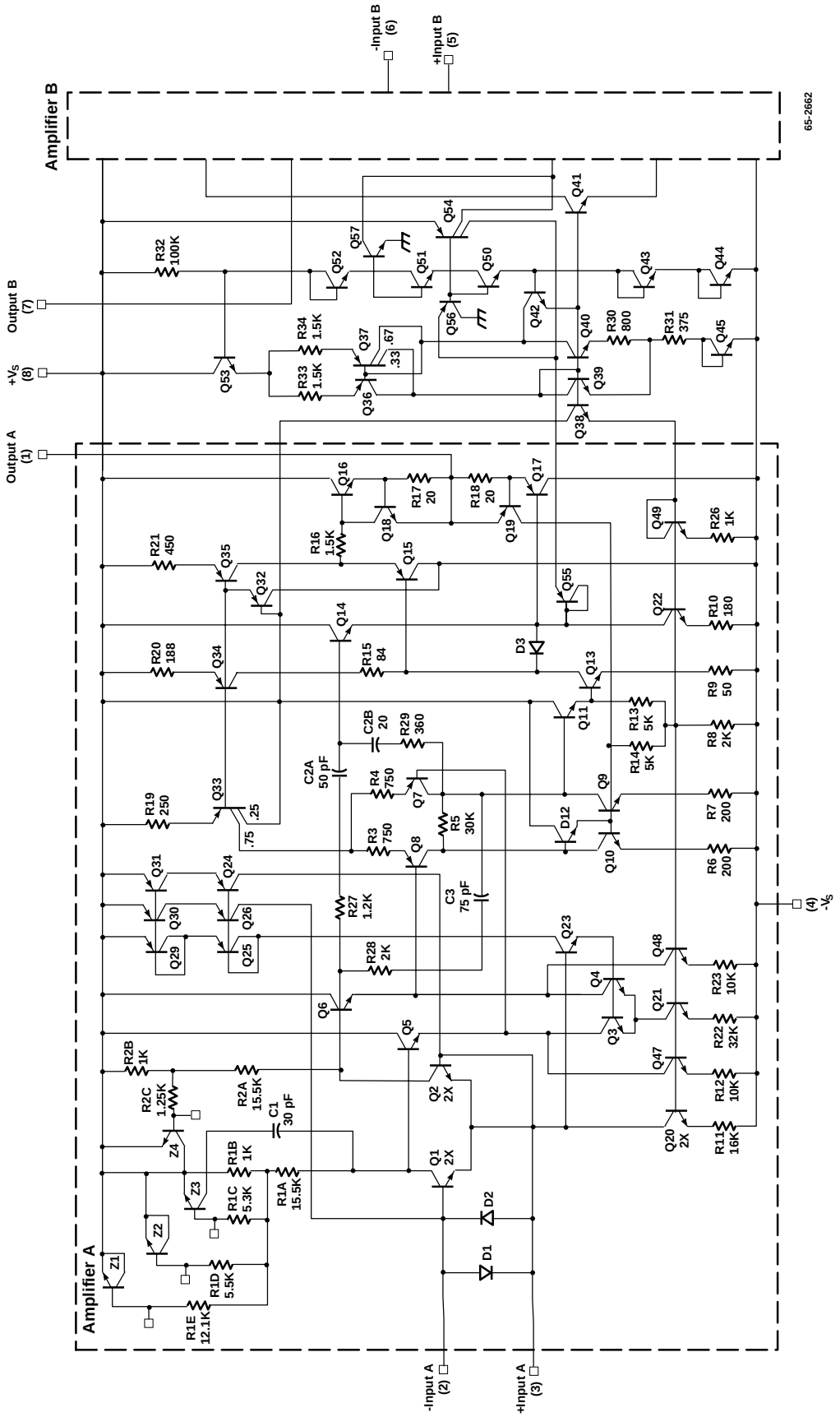


Figure 14. Input Noise Current Density vs Frequency

Simplified Schematic Diagram



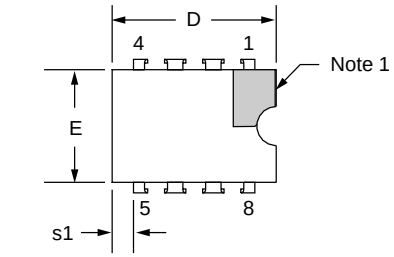
Mechanical Dimensions

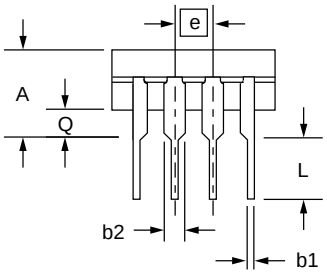
8-Lead Ceramic DIP Package

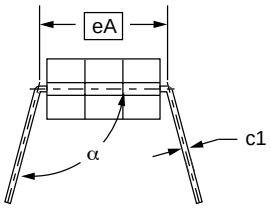
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2, 8
c1	.008	.015	.20	.38	8
D	—	.405	—	10.29	4
E	.220	.310	5.59	7.87	4
e	.100 BSC		2.54 BSC		5, 9
eA	.300 BSC		7.62 BSC		7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 4, 5 and 8 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 8.
6. Applies to all four corners (leads number 1, 4, 5, and 8).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Six spaces.







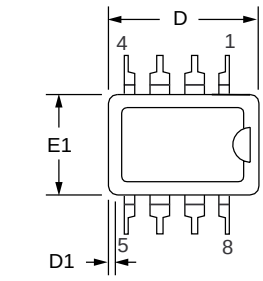
Mechanical Dimensions (continued)

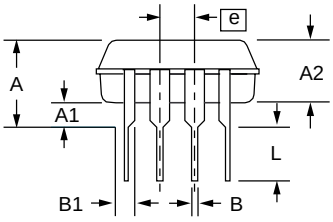
8-Lead Plastic DIP Package

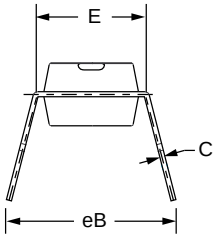
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	.348	.430	8.84	10.92	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.160	2.92	4.06	
N	8°		8°		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.







Ordering Information

Product Number	Temperature Range	Screening	Package
RC4227FN	0° to +70°C	Commercial	8 Pin Plastic DIP
RC4227GN	0° to +70°C	Commercial	8 Pin Plastic DIP
RM4227BD	-55°C to +125°C		8 Pin Ceramic DIP
RM4227BD/883[1]	-55°C to +125°C	Military	8 Pin Ceramic DIP

Note:

1. /883 suffix denotes MIl-STD-883, Par. 1.2.1 compliant device.

RC4277

Dual Precision Operational Amplifier

Features

- High DC precision
- Very low VOS – 30 μV
- Very low VOS drift – 0.3 μV/˚C
- High open-loop gain – 5000 V/mV
- High CMRR – 120 dB
- High PSRR – 120 db
- Low noise – 0.35 μV_{p-p} (0.1 Hz to 10 Hz)
- Low input bias current – 3.0 nA
- Low power consumption – 140 mW

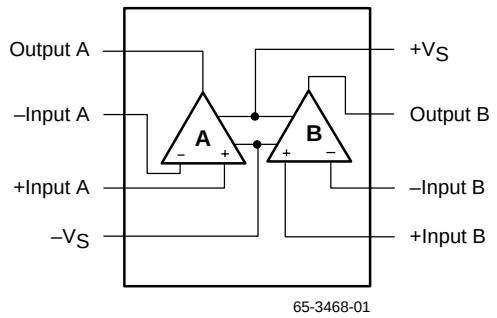
Description

The RC4277 provides the highest precision available in a dual bipolar operational amplifier. A monolithic dual version of the RC4077, the RC4277 is designed to replace OP-07 and OP-77 type amplifiers in applications requiring high PC board layout density. The RC4277 has a well-balanced, mutually supporting set of input specifications. Low V_{OS}, low I_B, high open-loop gain, and excellent matching characteristics combine to raise the performance level of many instrumentation, low-level signal conditioning, and data conversion applications. PSRR, CMRR, V_{OS} drift, and noise levels also support high precision operation.

The high performance of the RC4277 results from two innovative and unconventional manufacturing steps, plus careful circuit layout and design. The key steps are SiCr thin-film resistor deposition and post-package trimming of the input offset voltage characteristic. The low 75 μV max V_{OS} specification is maintained in high-volume production by way of the post-package trim procedure, where internal resistors are trimmed through the device input leads at the final test operation. Devices retain this low offset through the stability and accuracy of the trimmed thin-film resistors.

The RC4277 is available in 8-lead plastic and ceramic DIPs.

Block Diagram



Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min	Typ	Max	Units
Supply Voltage				±22	V
Input Voltage[2]				±22	V
Differential Input Voltage				30	V
Internal Power Dissipation[3]				500	mW
$P_D T_A$ < 50°C	PDIP			468	mW
	CerDIP			833	
Output Short Circuit Duration		Indefinite			
Junction Temperature	PDIP			125	°C
	CerDIP			175	
Storage Temperature		-65		150	°C
Operating Temperature	RV4277	-25		85	°C
	RC4277	0		70	
Lead Soldering Temperature (60 sec)				300	°C
For T_A > 50°C Derate at	PDIP		6.25		mW/°C
	CerDIP		8.33		

Notes:

1. Functional operation under any of these conditions is NOT implied.
2. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
3. Observe package thermal characteristics.

Operating Conditions

Parameter			Min	Typ	Max	Units
θ_{JC}	Thermal resistance	CerDIP		45		°C/W
θ_{JA}	Thermal resistance	PDIP		160		°C/W
		CerDIP		150		°C/W

Electrical Characteristics

(V_S = ±15V, and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	Min	Typ	Max	Units
Input Offset Voltage[3]			30	75	μV
Input Voltage Offset Match			25	150	μV
Long Term V_{OS} Stability[1]			0.3		μV/Mo
Input Offset Current			0.5	5.0	nA
Input Bias Current			±0.5	±5.0	nA
Input Noise Voltage	0.1 Hz to 10 Hz		0.35		μV_{p-p}
Input Noise Voltage Density	F_O = 10 Hz		10.3		$\frac{nV}{\sqrt{Hz}}$
	F_O = 100 Hz		10		
	F_O = 1000 Hz		9.6		
Input Noise Current Density	F_O = 10 Hz		0.32		$\frac{pA}{\sqrt{Hz}}$
	F_O = 100 Hz		0.14		
	F_O = 1000 Hz		0.12		
Input Voltage Range[2, 4]		±11	±14		V
Common Mode Rejection Ratio	V_{CM} = ±11V	110	132		dB
Power Supply Rejection Ratio	V_S = ±4V to ±16.5V	110	132		dB
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	1300	350		V/mV
Output Voltage Swing	$R_L \geq 10k\Omega$	±12.5	±13		V
	$R_L \geq 2k\Omega$	±12	±12.8		
	$R_L \geq 1k\Omega$	±11	±12		
Slew Rate	$R_L \geq 2k\Omega$	0.1	0.3		V/μs
Closed Loop Bandwidth	A_{VCL} = +1.0		0.8		MHz
Open Loop Output Resistance	V_{OUT} = 0, I_{OUT} = 0		60		Ω
Power Consumption	V_S = ±15V, R_L = ∞		60	100	mW
Crosstalk		126	155		dB

Notes:

1. Long Term Input Offset Voltage Stability refers to the averaged trend line of VOS vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in VOS during the first 30 operating days are typically 2.5 μV.
2. Guaranteed by design.
3. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
4. The input protection diodes do not allow the device to be removed or inserted into the circuit without first removing power.

Electrical Characteristics

(V_S = ±15V, 0°C ≤ T_A ≤ +70°C unless otherwise noted)

Parameters	Test Conditions	Min	Typ	Max	Units
Input Offset Voltage	0°C ≤ T_A ≤ +70°C		50	120	µV
	-25°C ≤ T_A ≤ +85°C		50	135	
Average Input Offset Voltage Drift[2]			0.3	1.0	µV/°C
Input Offset Current			1.5	5.0	nA
Input Bias Current			±1.5	±5.0	nA
Input Voltage Range		±10	±13.5		V
Common Mode Rejection Ratio	V_{CM} = ±10V	110	124		dB
Power Supply Rejection Ratio	V_S = ±4V to ±16.5V	110	124		dB
Large Signal Voltage Gain	R_L > 2kΩ, V_{OUT} = ±10V	1300	3000		V/mV
Output Voltage Swing	R_L > 2kΩ	±11	±12.6		V
Power Consumption	R_L = ∞		70	120	mW

Notes:

1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. This parameter is tested on a sample basis only.

Typical Applications

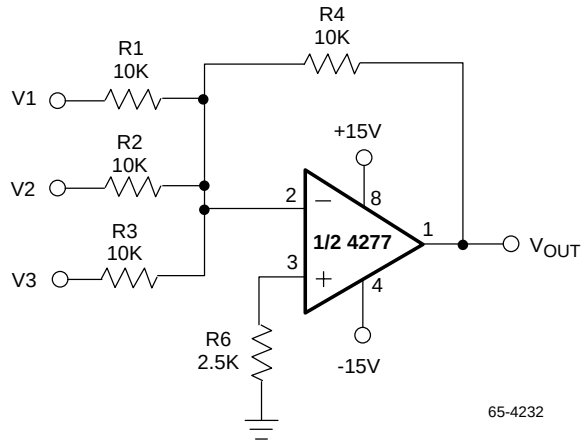


Figure 1. Adjustment-Free Precision Summing Amplifier

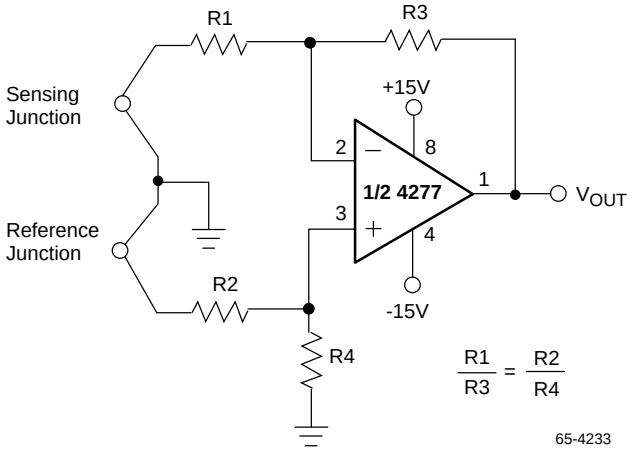


Figure 2. High Stability Thermocouple Amplifier

Typical Applications (continued)

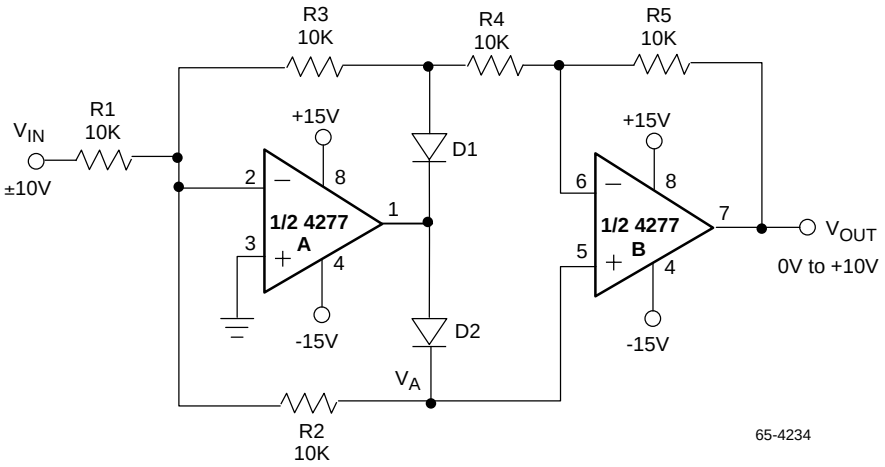
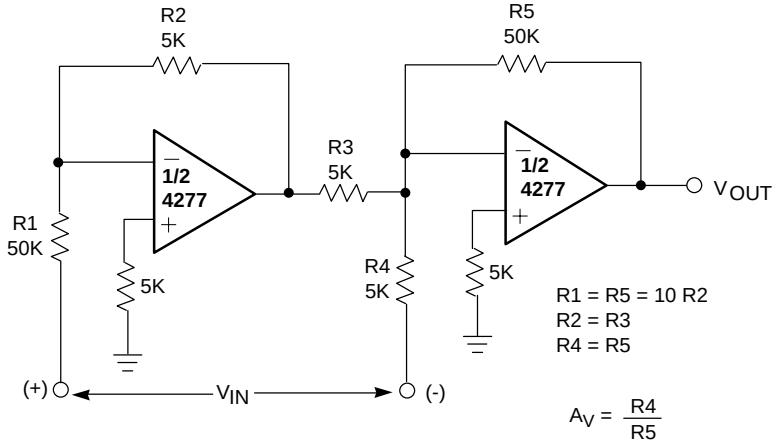


Figure 3. Precision Absolute Value Circuit



Note: This circuit can tolerate input voltages that exceed the 4277's supply voltage rating as long as the slew rate do not exceed the op amp's slew rate.

Figure 4. High Voltage Differential Amplifier

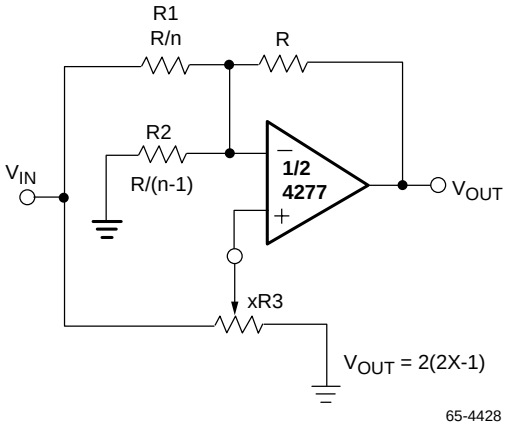


Figure 5. Polarity Changing Gain Controlled Amplifier

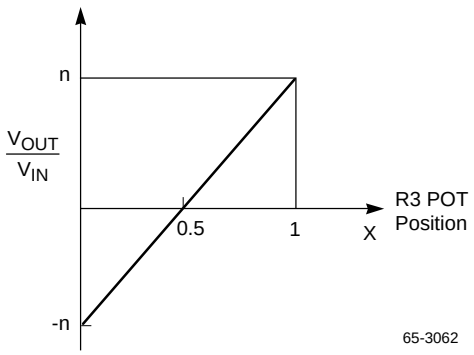


Figure 6. Gain Controlled Amplifier Transfer Function

Typical Applications (continued)

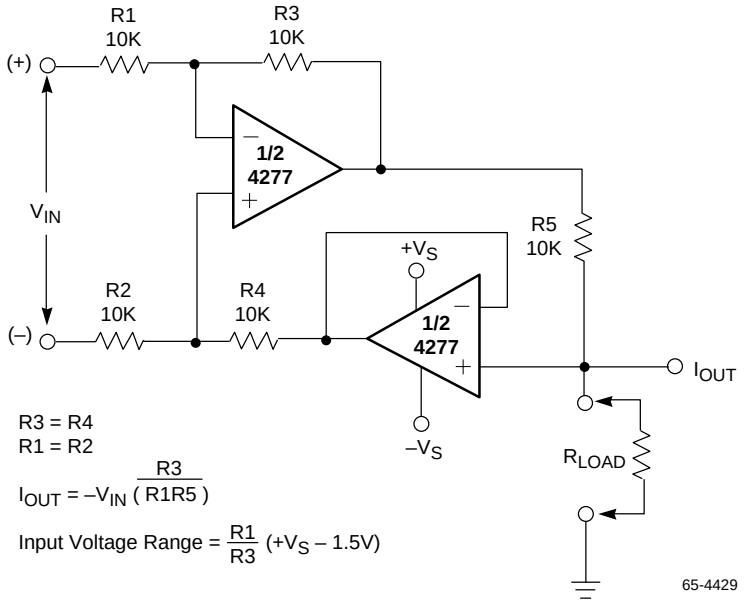


Figure 7. Differential Input Current Source

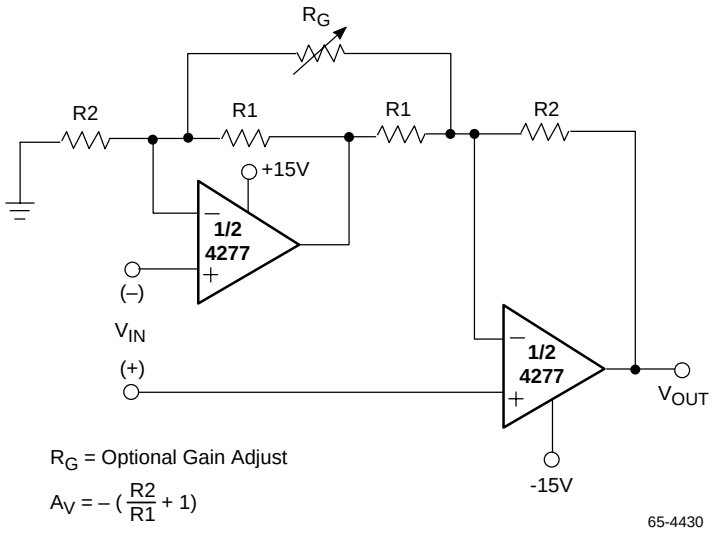


Figure 8. High Input Impedance Subtractor

Typical Applications (continued)

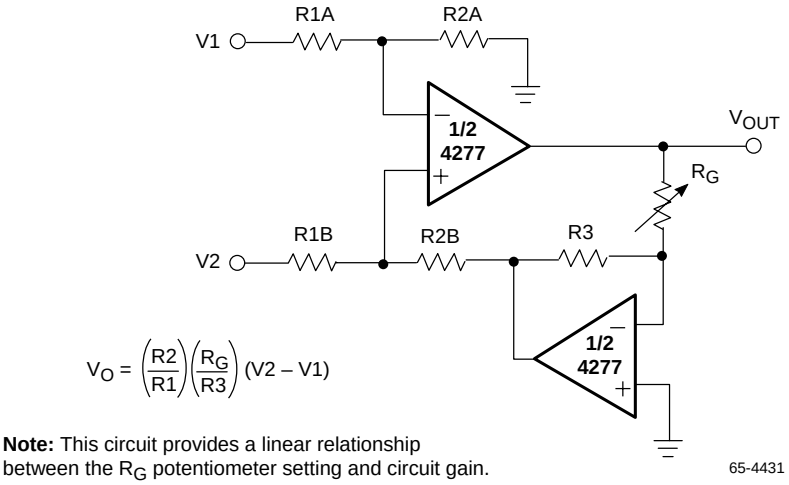


Figure 9. Difference Amplifier with Linear Gain Control

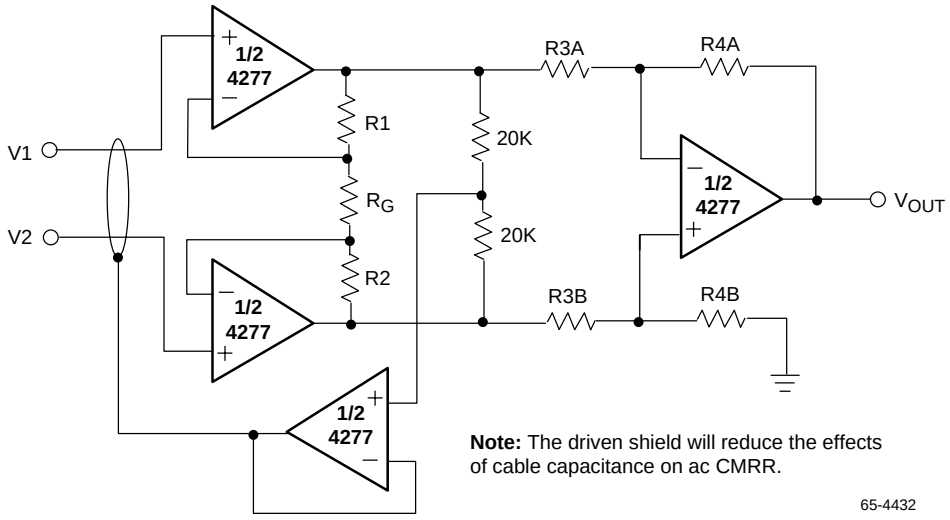
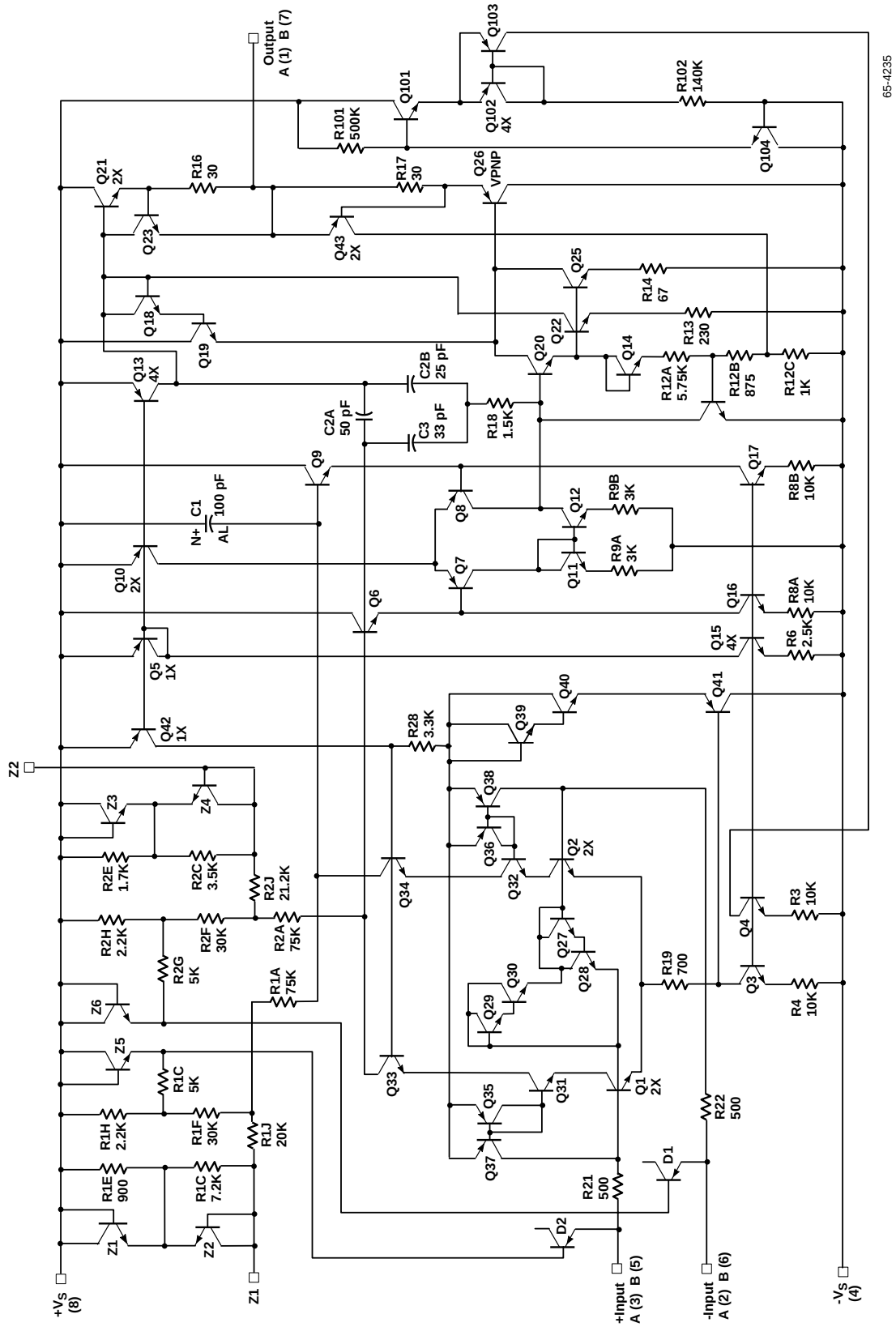


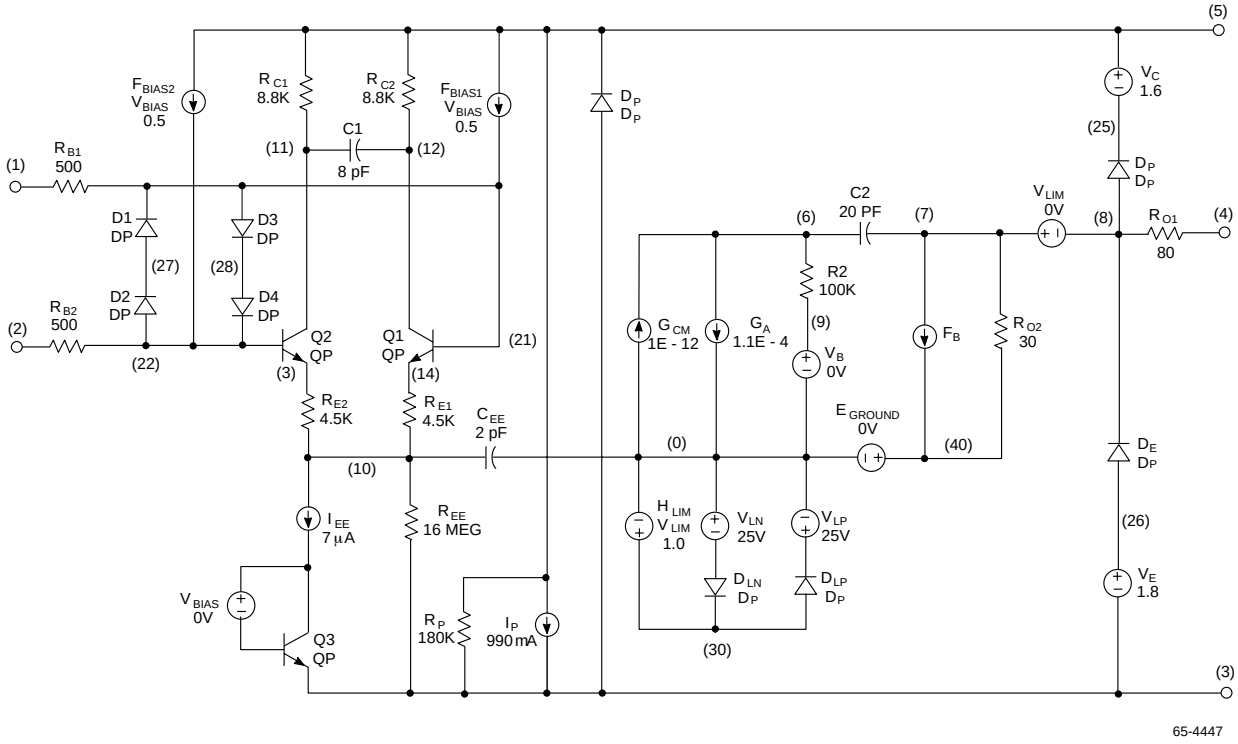
Figure 10. Three Op Amp Instrumentation Amplifier with Driven Shield

Schematic Diagram



RM4277 SPICE Macro Model

This circuit models AC and DC characteristics including slew rate, bandwidth, V_{OS}, I_B, I_{OS}, CMRR, output voltage range, and gain. The circuit produces typical values for these parameters.



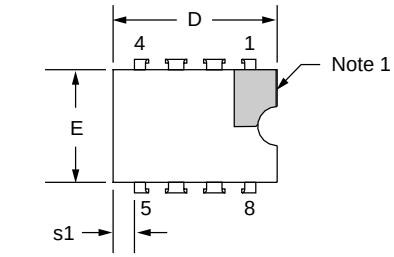
Mechanical Dimensions

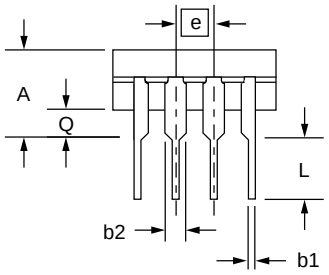
8-Lead Ceramic DIP Package

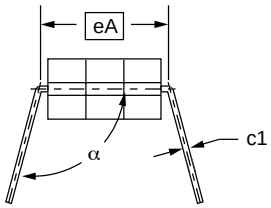
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2, 8
c1	.008	.015	.20	.38	8
D	—	.405	—	10.29	4
E	.220	.310	5.59	7.87	4
e	.100 BSC		2.54 BSC		5, 9
eA	.300 BSC		7.62 BSC		7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 4, 5 and 8 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 8.
6. Applies to all four corners (leads number 1, 4, 5, and 8).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Six spaces.







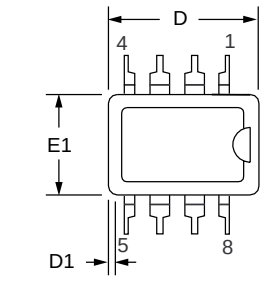
Mechanical Dimensions (continued)

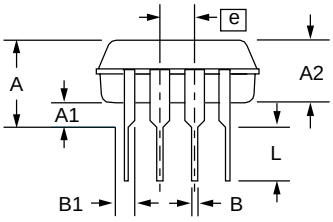
8-Lead Plastic DIP Package

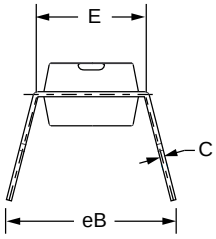
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	.348	.430	8.84	10.92	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.160	2.92	4.06	
N	8°		8°		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.







Ordering Information

Product Number	Temperature Range	Screening	Package
RC4277FN	0°C to +70°C	Commercial	8 Pin Plastic DIP
RV4277FD	0°C to 70°C	Commercial	8 Pin Ceramic DIP

5/20/98 0.0m 001
Stock#DS30004277

RC431A

Low-Voltage Adjustable Precision Shunt Regulator

Features

- Low voltage operation to 1.24V
- 1% reference voltage tolerance
- Output voltage adjustable from V_{ref} to 12V
- Low 80μA operational cathode current
- 0.25Ω typical output impedance
- TO-92 and SOT23-5 packages

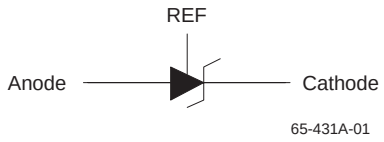
Applications

- Voltage reference for discrete power circuits

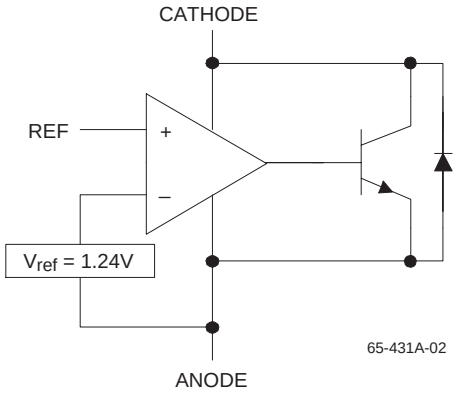
Description

The RC431A is a low-voltage 3-terminal adjustable precision voltage reference regulator. It has an excellent thermal stability over the standard commercial temperature range. The output voltage can be set to any value between Vref (1.24V) and 12V using two external resistors. The RC431A operates from a lower voltage (1.24V) than the traditional shunt regulator references which operate from 2.5V. When used with an optocoupler, the RC431A will be an ideal voltage reference in an isolated feedback circuit for use in switched-mode power supplies and modular DC-DC converters. The RC431A has a low output impedance of active output circuitry offering a very sharp turn-on characteristic. The RC431A will be an excellent replacement for low-voltage zener diodes in many applications such as on-board regulation and adjustable power supplies.

Symbol

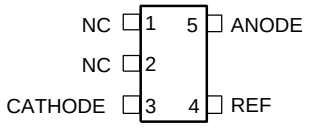


Block Diagram



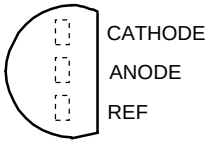
Pin Assignments

SOT-23 PACKAGE (TOP VIEW)



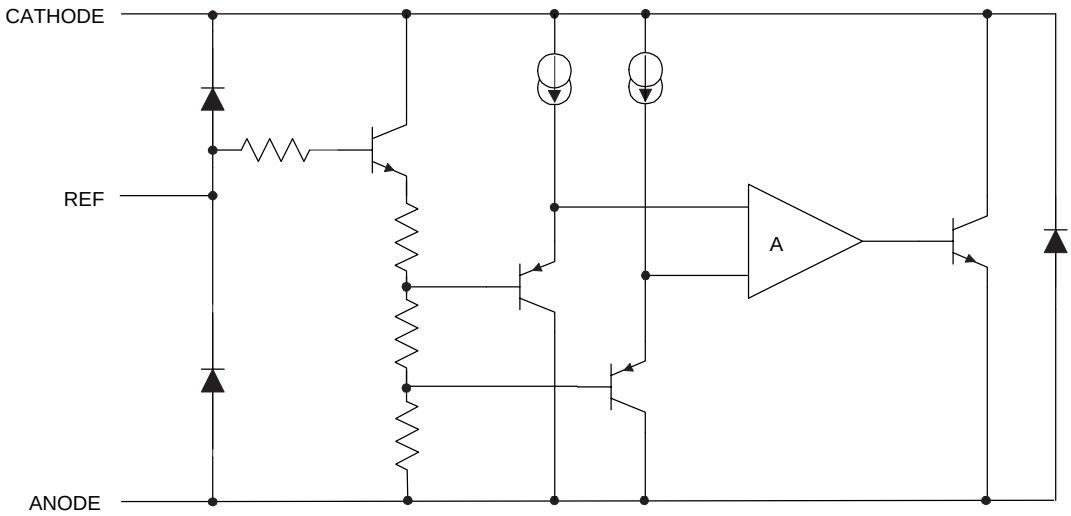
NC = No internal connection

TO-92 PACKAGE (TOP VIEW)



65-431A-03

Equivalent Schematic



65-431A-04

Absolute Maximum Ratings

Ratings are over full operating free-air temperature range unless otherwise noted.

Cathode voltage, V_{KA}	13.2V
Continuous cathode current I_K	–20mA to 20mA
Reference current, I_{ref}	–0.05mA to 3mA
Power dissipation	See Dissipation Rating Table
Storage temperature range	-65° to 150°C

Notes:

1. Functional operation under these conditions is not implied. Permanent damage may occur if the device is subjected to conditions outside these ratings.

Recommended Operating Conditions

Parameter	Min.	Max.	Units
Cathode voltage, V_{KA}	V_{REF}	12	V
Cathode current, I_K	0.1	15	mA
Operating temperature range in free-air, T_A	0	70	°C

Dissipation Rating Table

Package	Power Rating $T_A \le 25°C$	Derating Factor $T_A \ge 25°C$	Power Rating $T_A = 70°C$
TO-92	775mW	6.2mW/°C	496mW
SOT23-5	150mW	1.2mW/°C	96mW

Electrical Specifications

T_A = 25°C (unless otherwise noted), at free-air

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{ref}	Reference Voltage	$V_{KA} = V_{ref}$, T_A = 25°C	1.228	1.24	1.252	V
		I_K = 10mA, T_A = 0 to 70°C	1.221		1.259	
$V_{ref\ (dev)}$	V_{ref} deviation over full temperature range (see note 2)	$V_{KA} = V_{ref}$, I_K = 10mA, See note 2 and Figure 1.		4	12	mV
$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	Ratio of V_{ref} change in cathode voltage change	I_K = 10mA, $\Delta V_{KA} = V_{ref}$ to 6V. See figure 2.		-1.5	-2.7	$\frac{mV}{V}$
I_{ref}	Reference terminal current	I_K = 10mA, R1 = 10KΩ, R2 = ∞ See figure 2.		0.15	0.5	μA
$I_{ref(dev)}$	I_{ref} deviation over full temperature range (see note 2)	I_K = 10mA, R1 = 10KΩ, R2 = ∞ See note 1 & figure 2.		0.05	0.3	μA
$I_{K(min)}$	Minimum cathode current for regulation	$V_{KA} = V_{ref}$ See figure 1.		55	80	μA
I_{off}	Off-state cathode current	V_{KA} = 6V, V_{ref} = 0 See figure 3.		0.001	0.1	μA
$\lvert Z_{KA} \rvert$	Dynamic impedance (see note 3)	$V_{KA} = V_{ref}$, f ≤ 1KHz I_K = 0.1mA to 15mA, See figure 1.		0.25	0.4	Ω

Notes:

1. Functional operation under these conditions is not implied. Permanent damage may occur if the device is subjected to conditions outside these ratings.
2. Full temperature range is 0°C to 70°C.
3. The deviation parameters $V_{ref(dev)}$ and $I_{ref(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage, ∞V_{ref}, is defined as:

$$\lvert \infty V_{ref} \rvert \langle ppm/°C \rangle = \frac{\{V_{ref(dev)} / V_{ref} \langle T_A = 25°C \rangle\} \times 10^6}{\Delta T_A}$$

   where ΔT_A is the rated operating free-air temperature range of the device.

   ∞V_{ref} can be positive or negative depending on whether minimum V_{ref} or maximum V_{ref}, respectively, occurs at the lower temperature.

4. The dynamic impedance is defined as: $\lvert Z_{KA} \rvert = \Delta V_{KA} / \Delta I_K$

   When the device is operating with two external resistors (see Figure 2), the total dynamic impedance of the circuit is given by:

$$\lvert Z_{KA} \rvert = \frac{\Delta V}{\Delta I} \approx \lvert Z_{KA} \rvert \times \left(1 + \frac{R_1}{R_2}\right)$$

Parameter Measurement Information

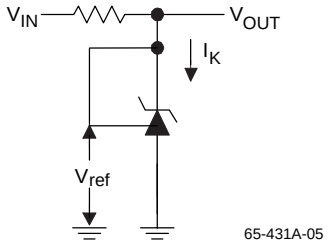


Figure 1. Test Circuit for $V_{KA} = V_{REF}$, $V_{OUT} = V_{KA} = V_{REF}$

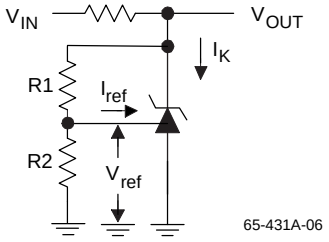


Figure 2. Test Circuit for $V_{KA} > V_{REF}$, $V_{OUT} = V_{KA} = V_{REF} \times (1+R1/R2) + I_{REF} \times R1$

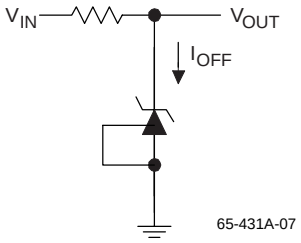


Figure 3. Test Circuit for I_{OFF}

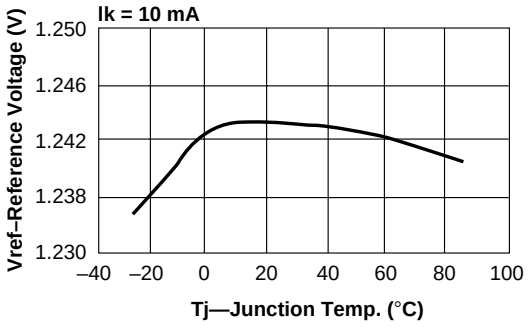


Figure 4. Reference Voltage vs. Junction Temp.

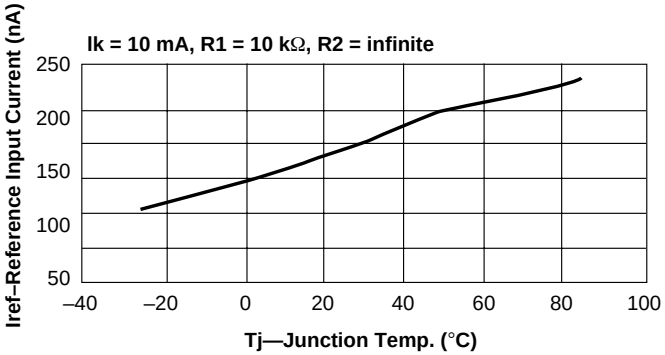


Figure 5. Reference Input Current vs. Junction Temp.

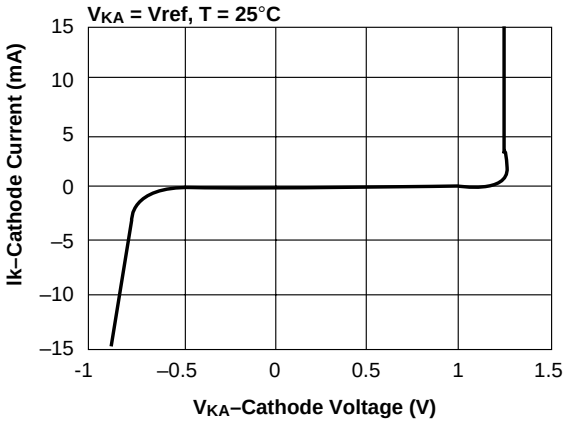


Figure 6. Cathode Current vs. Cathode Voltage

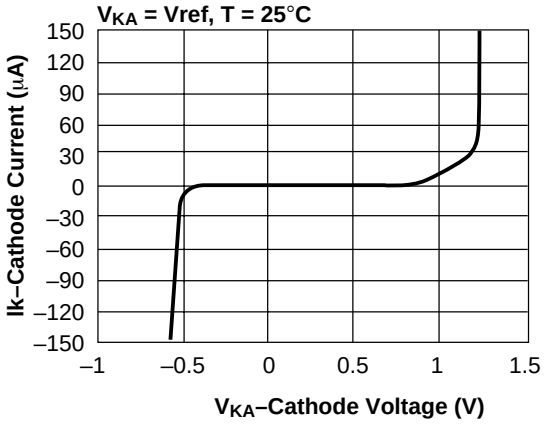


Figure 7. Cathode Current vs. Cathode Voltage

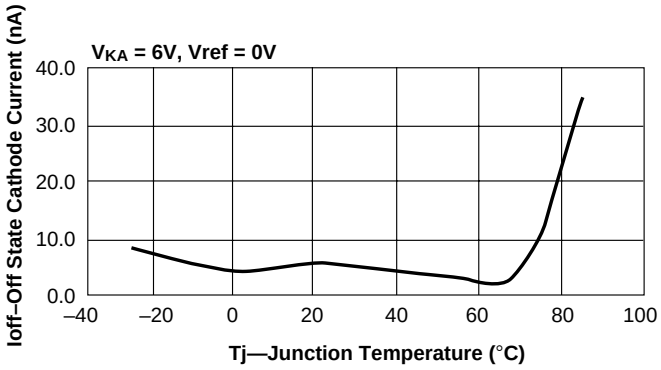


Figure 8. Off-State Cathode Current vs. Junction Temperature

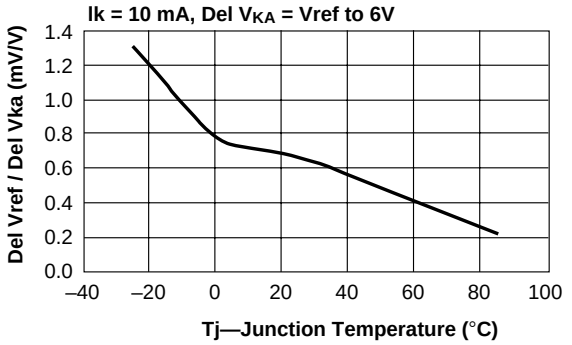


Figure 9. Ratio of Delta Reference Voltage to Delta Cathode Voltage vs. Junction Temperature

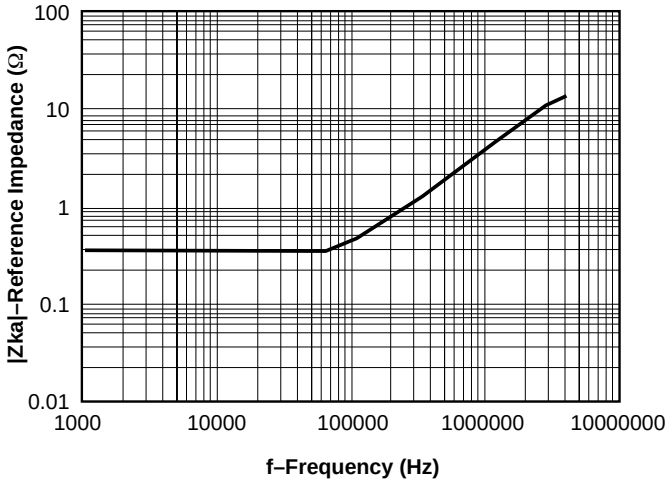


Figure 10. Reference Impedance vs. Frequency

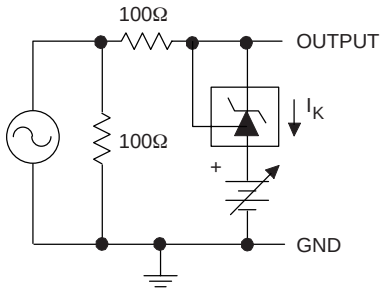


Figure 11. Test Circuit for Reference Impedance

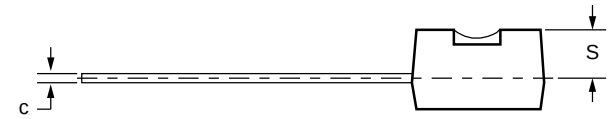
Mechanical Dimensions

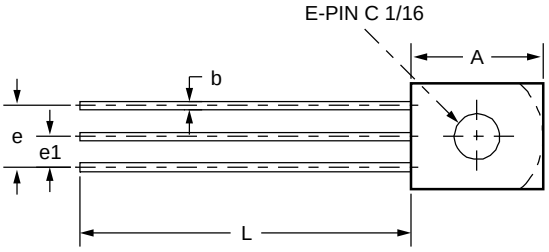
TO-92 Package

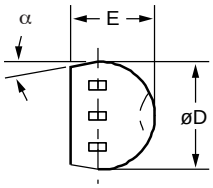
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.170	.210	4.32	5.33	
b	.015	.021	.38	.53	
c	.014	.020	.36	.51	
øD	.175	.205	4.45	5.21	
E	.125	.165	3.18	4.19	
e	.095	.105	2.41	2.67	
e1	.045	.055	1.14	1.40	
L	.500	—	12.70	—	
S	.080	.115	2.03	2.92	
α	4°	6°	4°	6°	

Notes:

1. Package outline exclusive of any mold flashes dimension.
2. Package outline exclusive of burr dimension.







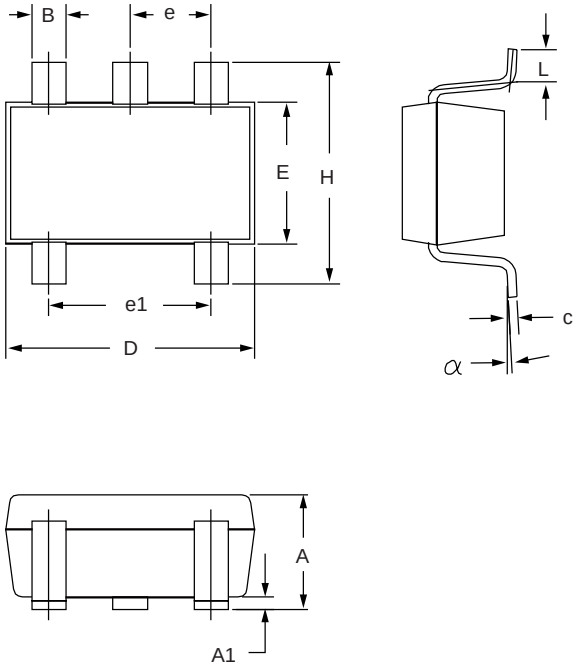
Mechanical Dimensions (continued)

SOT23-5 Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.170	.195	.90	1.45	
A1	.014	.020	.00	.15	
B	.008	.020	.20	.50	
c	.003	.010	.08	.25	
D	.106	.122	2.70	3.10	
E	.059	.071	1.50	1.80	
e	.037 BSC		.95 BSC		
e1	.075 BSC		1.90 BSC		
H	.087	.126	2.20	3.20	
L	.004	.024	.10	.60	
α	0°	10°	0°	10°	

Notes:

1. Package outline exclusive of mold flash & metal burr.
2. Package outline exclusive of solder plating.
3. EIAJ Ref Number SC-74A.



Ordering Information

Product Number	Package
RC431AM	SOT23-5
RC431AT	TO-92

RC4391

Inverting and Step-Down Switching Regulator

Features

- Versatile —
  Inverting function (+ to -)
  Step-down function
  Adjustable output voltage
  Regulates supply changes
- Micropower —
  Low quiescent current — 170 μA
  Wide supply range — 4V to 30V
- High performance —
  High switch current — 375 mA
  High efficiency — 70% typically
- Low battery detection capability
- 8-lead mini-DIP or S.O. package

Description

Fairchild Semiconductor's RC4391 is a monolithic switch mode power supply controller for micropower circuits. The RC4391 integrates all the active functions needed for low power switching supplies, including oscillator, switch, reference and logic, into a small package. Also, the quiescent supply current drawn by the RC4391 is extremely low; this combination of low supply current, function, and small package make it adaptable to a variety of miniature power supply applications.

The RC4391 complements another Fairchild Semiconductor switching regulator IC, the RC4190. The RC4190 is dedicated to step-up ($V_{OUT} > V_{IN}$) applications, while the RC4391 was designed for inverting ($V_{OUT} = -V_{IN}$) and step-down ($V_{OUT} < V_{IN}$) applications. Between the two devices the ability to create all three basic switching regulator configurations is assured. Refer to the RC4190 data sheet for information on step-up applications.

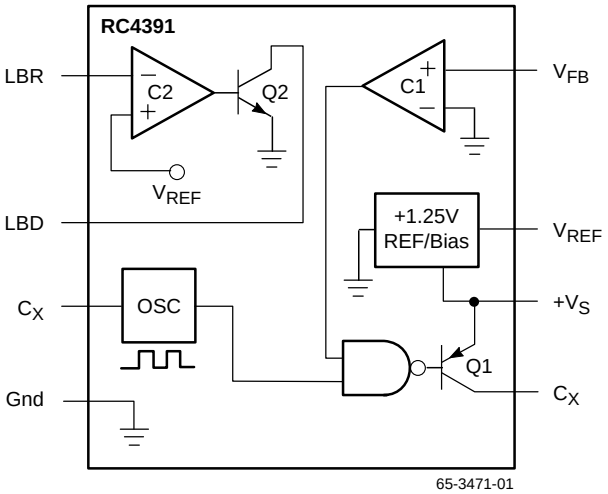
The functions provided are:

- Squarewave oscillator (adjustable externally)
- Bandgap voltage reference
- High current PNP switch transistor
- Feedback comparator
- Logic for gating the comparator
- Circuitry for detecting a discharged battery condition (in battery powered systems)

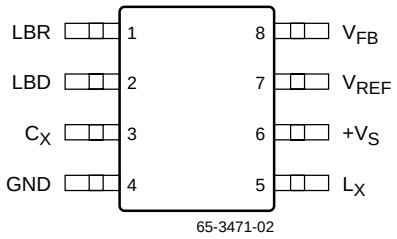
Few external components are required to build a complete DC-to-DC converter:

- Inductor
- Low value capacitor to set the oscillator frequency
- Electrolytic filter capacitor
- Steering diode
- Two resistors

Block Diagram



Pin Assignments



Pin Descriptions

Pin Number	Pin Function Description
1	Low Battery Resistor (LBR)
2	Low Battery Detector (LBD)
3	Timing Capacitor (C_X)
4	Ground
5	External Inductor (L_X)
6	+Supply Voltage ($+V_S$)
7	+1.25V Reference Voltage (V_{REF})
8	Feedback Voltage (V_{FB})

Absolute Maximum Ratings

Parameter	Conditions	Min	Typ	Max	Unit
Internal Power Dissipation				500	mW
Supply Voltage[1]	(Pin 6 to Pin 4 or Pin 6 to Pin 5)			+30	V
Operating Temperature	RC4391	0		70	°C
	RV4391	-25		85	°C
	RM4391	-55		125	°C
Storage Temperature		-65		150	°C
Junction Temperature	PDIP, SOIC			125	°C
	CerDIP			175	°C
Switch Current (I_{MAX})	Peak			375	mA
P_D T_A <50˚C	PDIP			468	mW
	CerDIP			833	mW
	SOIC			300	mW
Lead Soldering Temperature	(10 seconds)			300	°C

Note:

1. The maximum allowable supply voltage ($+V_S$) in inverting applications will be reduced by the value of the negative output voltage, unless an external power transistor is used in place of Q1.

Thermal Characteristics

	8-Lead Plastic DIP	8-Lead Ceramic DIP	Small Outline SO-8
Therm. Res θ_{JC}	—	45°C/W	—
Therm. Res. θ_{JA}	160°C/W	150°C/W	240°C/W
For T_A >50˚C Derate at	6.25 mW/°C	8.33 mW/°C	4.17 mW/°C

Electrical Characteristics

(V_S = +6.0V, over the full operating temperature range unless otherwise noted)

Symbol	Parameters	Condition	Min	Typ	Max	Units
$+V_S$	Supply Voltage	(Note 1)	4.0		30	V
I_{SY}	Supply Current	V_S = +25V		300	500	μA
V_{REF}	Reference Voltage		1.13	1.25	1.36	V
V_{OUT}	Output Voltage	$V_{OUT\ nom}$ = -5.0V	-5.5	-5.0	-4.5	V
		$V_{OUT\ nom}$ = -15V	-16.5	-15.0	-13.5	
LI_1	Line Regulation	$V_{OUT\ nom}$ = -5.0V, C_X = 150pF V_S = +5.8V to +15V		2.0	4.0	$\%V_{OUT}$
		$V_{OUT\ nom}$ = -15V, C_X = 150pF V_S = +5.8V to +15		1.5	3.0	
$L0_1$	Load Regulation	$V_{OUT\ nom}$ = -5.0V, C_X = 350pF, V_S = +4.5V, P_{LOAD} = 0mW to 75mW		0.2	0.5	$\%V_{OUT}$
		$V_{OUT\ nom}$ = -15V, C_X = 350pF, V_S = +4.5V, P_{LOAD} = 0mW to 75mW		0.2	0.3	
I_{CO}	Switch Leakage Current	Pin 5 = -20V		0.1	30	μA

Note:

1. The maximum allowable supply voltage ($+V_S$) in inverting applications will be reduced by the value of the negative output voltage, unless an external power transistor is used.

Electrical Characteristics

(V_S = +6.0V, T_A = +25°C unless otherwise noted)

Symbol	Parameters	Condition	Min	Typ	Max	Units
I_{SY}	Supply Voltage	V_S = +4.0V, No External Loads		170	250	µA
		V_S = +25V No External Loads		300	500	
V_{OUT}	Output Voltage	$V_{OUT\ nom}$ = -5.0V	-5.35	-5.0	-4.65	V
		$V_{OUT\ nom}$ = -15V	-15.85	-15.0	-14.15	
LI_1	Line Regulation	$V_{OUT\ nom}$ = -5.0V C_X = 150pF, V_S = +5.8V to +15V		1.5	3.0	%V_{OUT}
		$V_{OUT\ nom}$ = -15V, C_X = 150pF V_S = +5.8V to +15V		1.0	2.0	
$L0_1$	Load Regulation	$V_{OUT\ nom}$ = -5.0V, C_X = 350pF, V_S = +4.5V, P_{LOAD} = 0mW to 75mW		0.2	0.4	%V_{OUT}
		$V_{OUT\ nom}$ = -15V, C_X = 350pF, V_S = +4.5V, P_{LOAD} = 0mW to 75mW		0.07	0.14	
V_{REF}	Reference Voltage		1.18	1.25	1.32	V
I_{SW}	Switch Current	Pin 5 = 5.5V	75	100		mA
I_{CO}	Switch Leakage Current	Pin 5 = -24V		0.01	5.0	µA
I_{CX}	Cap. Charging Current	Pin 3 = 0V	6.0	10	14	µA
I_{LBDL}	LBD Leakage Current	Pin 1 = 1.5V, Pin 2 = 6.0V		0.01	5.0	µA
I_{LBD0}	LBD On Current	Pin 1 = 1.1V, Pin 2 = 0.4V	210	600		µA
I_{LBRB}	LBR Bias Current	Pin 1 = 1.5V		0.7		µA

Typical Performance Characteristics

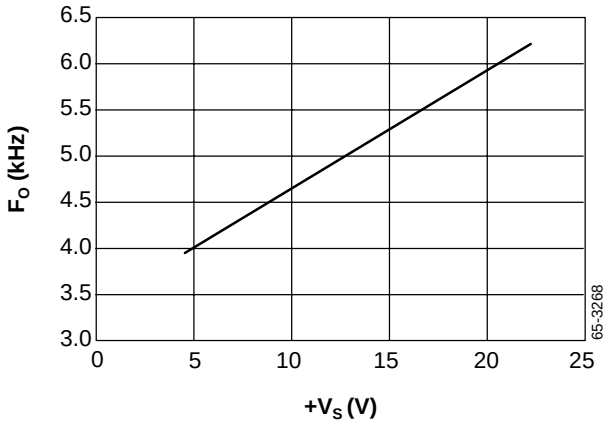


Figure 1. Oscillator Frequency vs. Supply Voltage

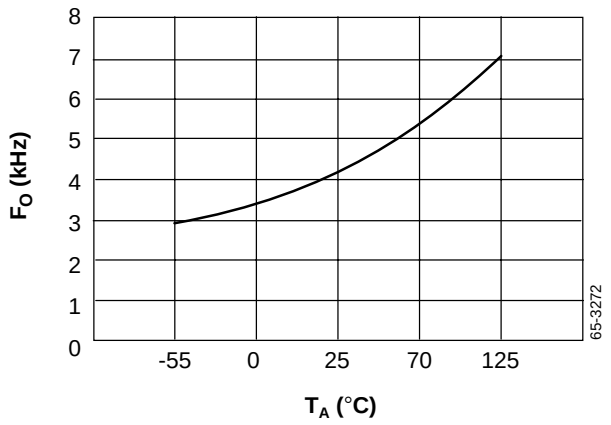


Figure 2. Oscillator Frequency vs. Temperature

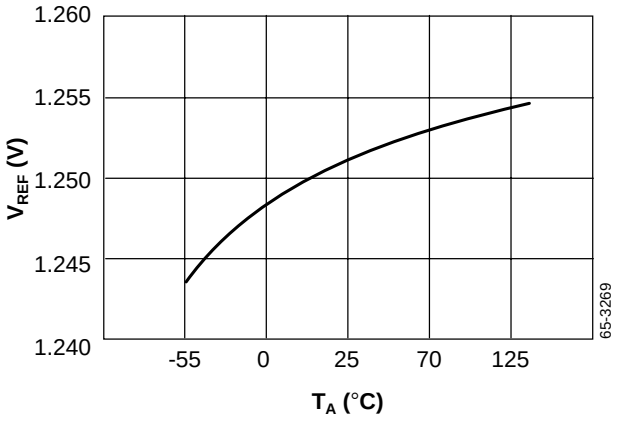


Figure 3. Reference Voltage vs. Temperature

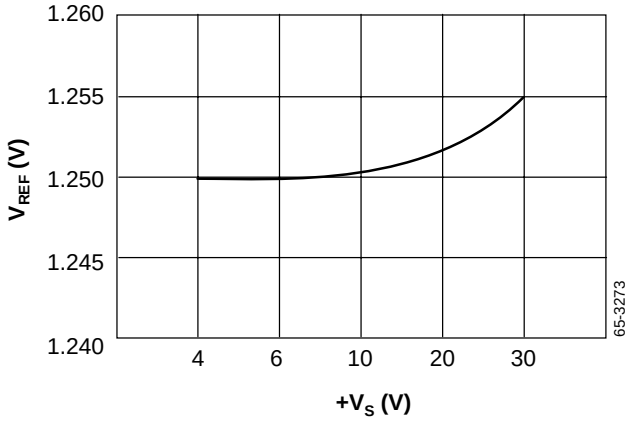


Figure 4. Reference Voltage vs. Supply Voltage

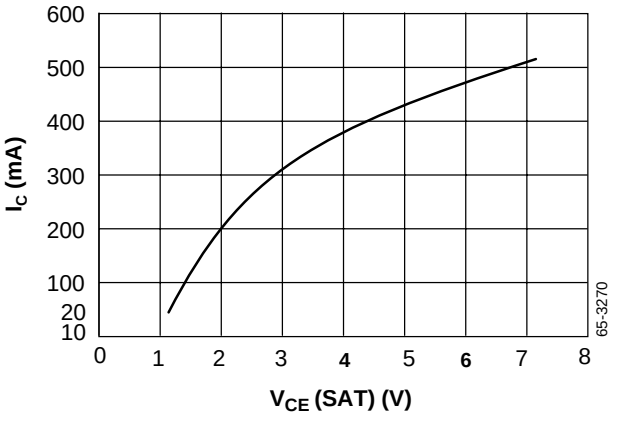


Figure 5. Collector Current vs. Q1 Saturation Voltage

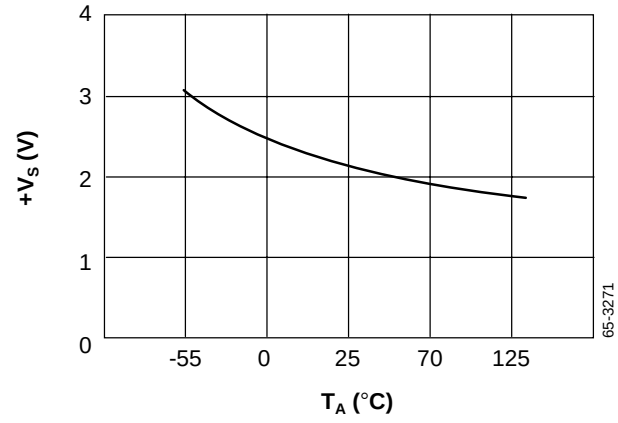


Figure 6. Minimum Supply Voltage vs. Temperature

Principles of Operation

The basic switching inverter circuit is the building block on which the complete inverting application is based.

A simplified diagram of the voltage inverter circuit with ideal components and no feedback circuitry is shown in Figure 7. When the switch S is closed, charging current from the battery flows through the inductor L, which builds up a magnetic field, increasing as the switch is held closed. When the switch is opened, the magnetic field collapses, and the energy stored in the magnetic field is converted into a current which flows through the inductor in the same direction as the changing current. Because there is no path for this current to flow through the switch, the current must flow through the diode to charge the capacitor C. The key to the inversion is the ability of the inductor to become a source when the charging current is removed.

The equation V = L (di/dt) gives the maximum possible voltage across the inductor; in the actual application, feedback circuitry and the output capacitor will decrease the output voltage to a regulated fixed value.

A complete schematic for the standard inverting application is shown in Figure 8. The ideal switch in the simplified diagram is replaced by the PNP transistor switch between pins 5 and 6. C_F functions as the output filter capacitor, and D1 and L_X replace D and L.

When power is first applied, the ground sensing comparator (pin 8) compares the output voltage to the +1.25V voltage reference. Because C_F is initially discharged a positive voltage is applied to the comparator, and the output of the comparator gates the squarewave oscillator. This gated squarewave signal turns on, then off, the PNP output transistor. This turning on and off of the output transistor performs the same function as opening and closing the ideal switch in the simplified diagram; i.e., it stores energy in the inductor during the on time and releases it into the capacitor during the off time.

The comparator will continue to allow the oscillator to turn the switch transistor on and off until enough energy has been stored in the output capacitor to make the comparator input voltage decrease to less than 0V. The voltage applied to the comparator is set by the output voltage, the reference voltage, and the ratio of R1 to R2.

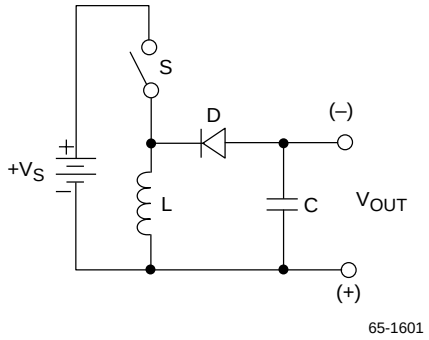
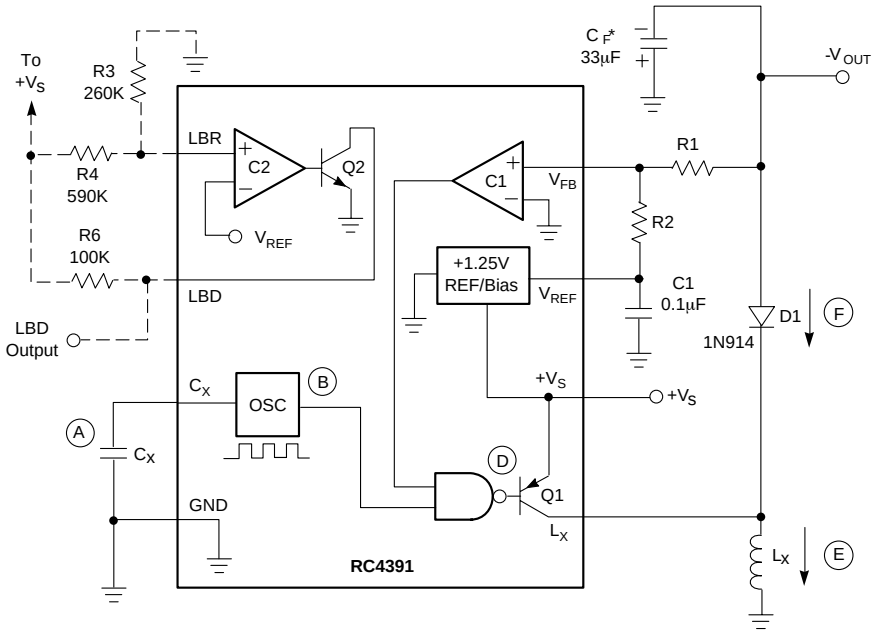


Figure 7. Simple Inverting Regulator



Parts List	-5.0V Output	-15V Output
R1 =	300 kΩ	900 kΩ
R2 =	75 kΩ	75 kΩ
C_X =	150 pF	150 pF
L_X =	1.0 mH Dale TE3 Q4 TA	

– – – – – – = Optional

$-V_{OUT} = (1.25V)\ (\frac{R1}{R2})$

*Caution: Use current limiting protection circuit for high values of C_F (Figure 13)

Figure 8. Inverting Regulator – Standard Circuit

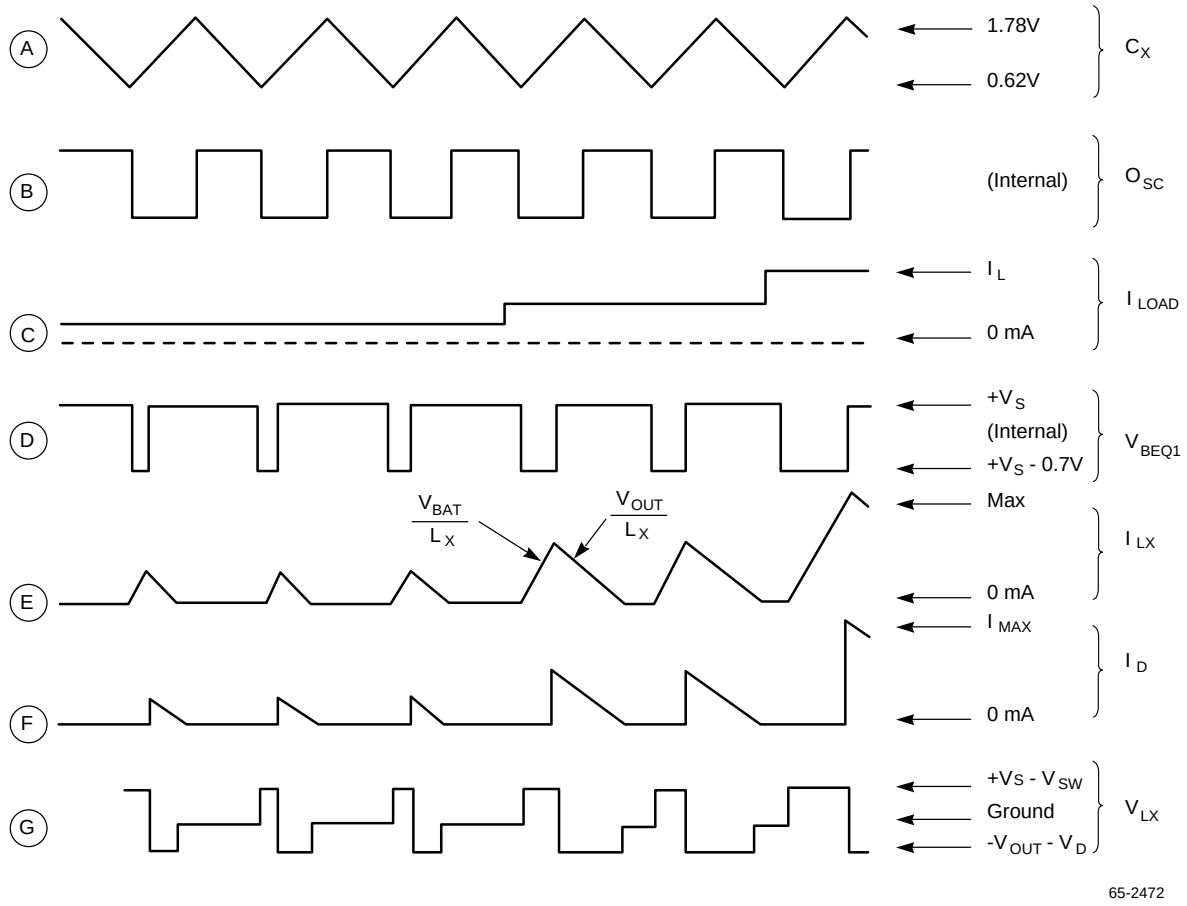


Figure 9. Inverting Regulator Waveforms

This feedback system will vary the duration of the on time in response to changes in load current or battery voltage (see Figure 9). If the load current increases (waveform C), then the transistor will remain on (waveform D) for a longer portion of the oscillator cycle, (waveform B) to build up to a higher peak value. The duty cycle of the switch transistor varies in response to changes in load and line.

Step-Down Regulator

The step-down circuit function is similar to inversion; it uses the same components (switch, inductor, diode, filter capacitor), and charges and discharges the inductor by closing and opening the switch. The great difference is that the inductor is in series with the load; therefore, both the charging current and the discharge current flow into the load. In the inverting circuit only the discharge current flows into the load. Refer to Figure 10.

When the switch S is closed, current flows from the battery, through the inductor, and through the load resistor to ground. After the switch is opened, stored energy in the inductor causes current to keep flowing through the load, the circuit being completed by the catch diode D. Since current flows to the load during charge and discharge, the average load current will be greater than in an inverting circuit. The significance of that is that for equal load currents the step-down circuit will require less peak inductor current than an inverting circuit. Therefore, the inductor will not require as large of a core, and the switch transistor will not be stressed as heavily for equal load currents.

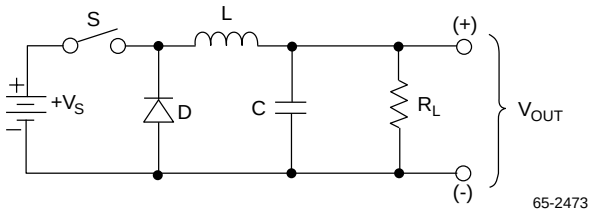


Figure 10. Simple Step-Down Regulator

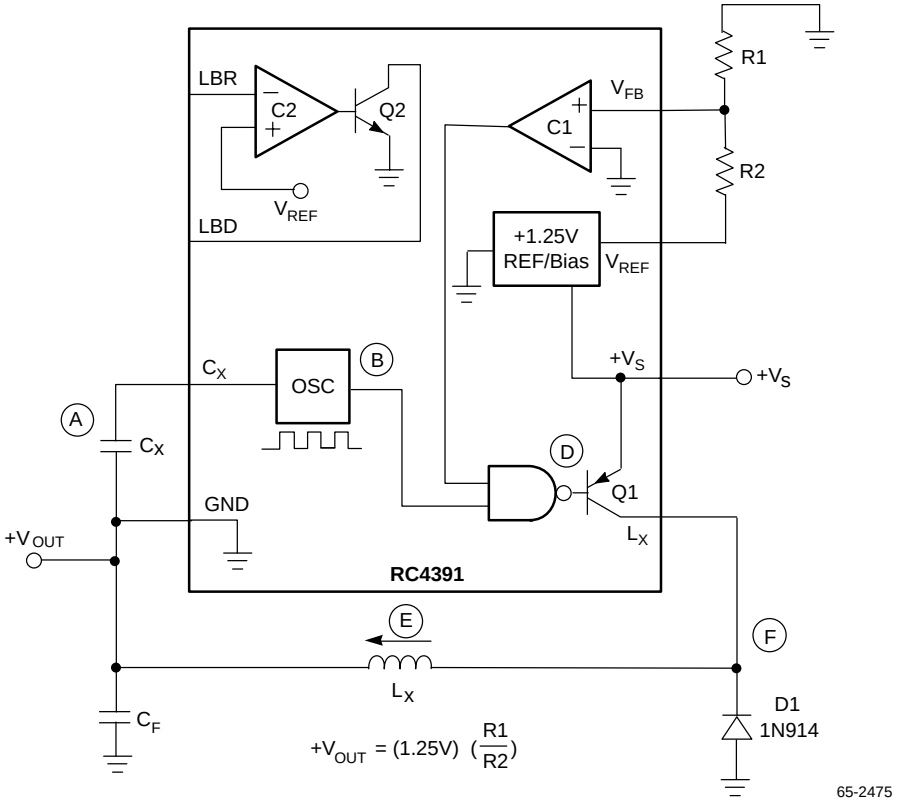
Figure 11 depicts a complete schematic for a step-down circuit using the RC4391. Observe that the ground lead of the 4391 is **not** connected to circuit ground; instead, it is tied to the output voltage. It is by this rearrangement that the feedback system, which senses voltages more negative than the ground lead, can be used to regulate a non-negative output voltage.

When power is first applied, the output filter capacitor is discharged so the ground lead potential starts at 0V. The reference voltage is forced to +1.25V above the ground lead and pulls the feedback input (pin 8) more positive than the ground lead. This positive voltage forces the control network to begin pulsing the switch transistor. As the switching action pumps up the output voltage, the ground lead rises with the output until the voltage on the ground lead is equal to the feedback voltage. At that point, the control network reduces the time on time of the switch to maintain a constant output.

This control network will vary the on time of the switch in response to changes in load current or battery voltage (see Figure 12). If the load current increases (waveform C), then the transistor will remain on (waveformD) for a longer portion of the oscillator cycle, (waveform B), thus allowing the inductor current (waveform E) to build up to a higher peak value. The duty cycle of the switch transistor varies in response to changes in load and line.

Design Equations

The inductor value and timing capacitor (C_X) value must be carefully tailored to the input voltage, input voltage range, output voltage, and load current requirements of the application. The key to the problem is to select the correct inductor value for a given oscillator frequency, such that the inductor current rises to a high enough peak value (I_{MAX}) to meet the average load current drain. The selection of this inductor value must take into account the variation of oscillator frequency from unit to unit and the drift of frequency over temperature. Use ±30% as a maximum variation of oscillator frequency.



Important Note: This circuit must have a minimum load ≥ 1 mA always connected.

Figure 11. Step-Down Regulator – Standard Circuit

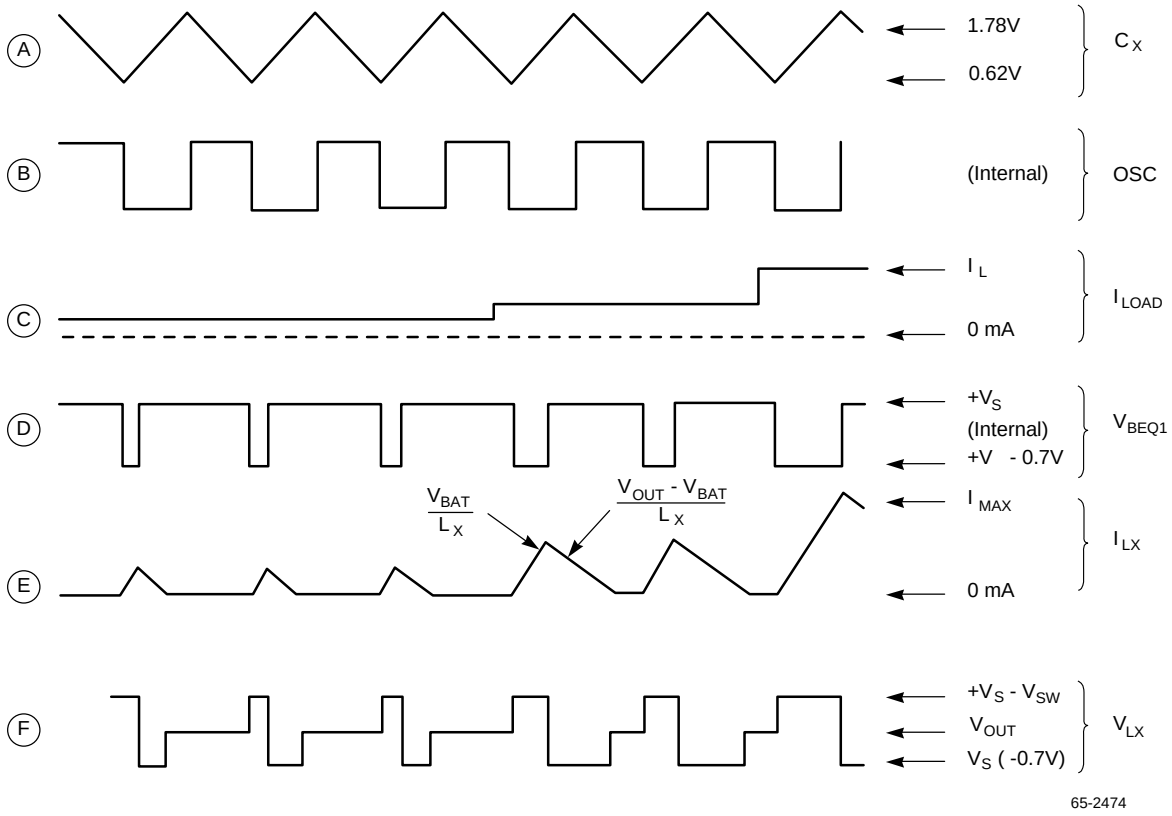


Figure 12. Step-Down Regulator Waveforms

The oscillator creates a squarewave using a method similar to the 555 timer IC, with a current steering flip-flop controlled by two voltage sensing comparators. The oscillator frequency is set by the timing capacitor (C_X) according to the following equation.

$$F_O(Hz) = \frac{4.1x10^{-6}}{C_x(pF)}$$

The squarewave output of the oscillator is internal and cannot be directly measured, but is equal in frequency to the triangle waveform measurable at pin 3. The switch transistor is normally on when the triangle waveform is ramping up and off when ramping down. Capacitor selection depends on the application; higher operating frequencies will reduce the output voltage ripple and will allow the use of an inductor with a physically smaller inductor core, but excessively high frequencies will reduce load driving capability and efficiency.

Inverting Design Procedure

1. Select an operating frequency and timing capacitor value as shown above (frequencies from 10kHz to 50kHz are typical).
2. Find the maximum on time T_{ON} (add 3µS for the turn off base recombination delay of Q1):

   $$T_{ON} = \frac{1}{2F_O} + 3\mu S$$

3. Calculate the peak inductor current IMAX (if this value is greater than 375mA then an external power transistor must be used in place of Q1):

   $$I_{MAX} = \frac{(V_{OUT} + V_D)2I_L}{(F_O)(T_{ON})(V_S - V_{SW})}$$

   Where:

   V_S = Supply Voltage
   V_{SW} = Saturation Voltage of Q1 (typically 0.5V)
   V_D = Diode Forward Voltage (typically 0.7V)
   I_L = DC Load Current

4. Find an inductance value for LX:

   $$L_X(Henries) = \left(\frac{V_S - V_{SW}}{I_{MAX}}\right)(T_{ON})$$

The inductor chosen must exhibit this value of inductance and have a current rating equal to I_{MAX}.

Step-Down Design Procedure

1. Select an operating frequency.

2. Determine the maximum on time T_{ON} as in the inverting design procedure.

3. Calculate I_{MAX}:

$$I_{MAX} = \frac{2I_L}{(F_O)(T_{ON})\left[\frac{(V_S - V_{OUT})}{(V_{OUT} - V_D)} + 1\right]}$$

4. Calculate L_X:

$$L_X(\text{Henries}) = \left(\frac{V_S - V_{SW}}{I_{MAX}}\right)(T_{ON})$$

Alternate Design Procedure

The design equations above will not work for certain input/output voltage ratios, and for these circuits another method of defining component values must be used. If the slope of the current discharge waveform is much less than the slope of the current charging waveform, then the inductor current will become continuous (never discharging completely), and the equations will become extremely complex. So, if the voltage applied across the inductor during the charge time is greater than during the discharge time, use the design procedure below. For example, a step-down circuit with 20V input and 5V output will have approximately 15V across the inductor when charging, and approximately 5V when discharging. So in this example the inductor current will be continuous and the alternate procedure will be necessary. The alternate procedure may also be used for discontinuous circuits.

1. Select an operating frequency based on efficiency and component size requirements (a value between 10kHz and 50kHz is typical).

2. Build the circuit and apply the worst case conditions to it, i.e., the lowest battery voltage and the highest load current at the desired output voltage.

3. Adjust the inductor value down until the desired output voltage is achieved, then decrease its value by 30% to cover manufacturing tolerances.

4. Check the output voltage with an oscilloscope for ripple, at high supply voltages, at voltages as high as are expected. Also check for efficiency by monitoring supply and output voltages and currents:

$$\left(\text{eff} = \frac{(V_{OUT})(I_{OUT})}{(+V_S)(I_{SY})x100}\right)$$

5. If the efficiency is poor, go back to Step 1 and start over. If the ripple is excessive, then increase the output filter capacitor value or start over.

Compensation

When large values (> 50 kΩ) are used for the voltage setting resistors (R1 and R2 of Figure 8) stray capacitance at the V_{FB} input can add lag to the feedback response, destabilizing the regulator, increasing low frequency ripple, and lowering efficiency. This can often be avoided by minimizing the stray capacitance at the V_{FB} node. It can also be remedied by adding a lead compensation capacitor of 100 pF to 10 nF. In inverting applications, the capacitor connects between $-V_{OUT}$ and V_{FB}; for step-down circuits it connects between ground and V_{FB}. Most applications do not require this capacitor.

Inductors

Efficiency and load regulation will improve if a quality high Q inductor is used. A ferrite pot core is recommended; the wind-yourself type with an air gap adjustable by washers or spacers is very useful for bread-boarding prototypes. Care must be taken to choose a core with enough permeability to handle the magnetic flux produced at I_{MAX}. If the core saturates, then efficiency and output current capability are severely degraded and excessive current will flow through the switch transistor. A pot core inductor design section is provided later in this datasheet.

An isolated AC current probe for an oscilloscope (example: Tektronix P6042) is an excellent tool for saturation problems; with it the inductor current can be monitored for nonlinearity at the peaks (a sign of saturation).

Low Battery Detector

An open collector signal transistor Q2 with comparator C2 provides the designer with a method of signaling a display or computer whenever the battery voltage falls below a programmed level (see Figure 13). This level is determined by the +1.25V reference level and by the selection of two external resistors according to the equation:

$$V_{TH} = V_{REF}\left(\frac{R4}{R5} + 1\right)$$

When the battery drops below this threshold Q2 will turn on and sink typically 600μA. The low battery detection circuit can also be used for other less conventional applications such as the voltage dependent oscillator circuit of Figure 18.

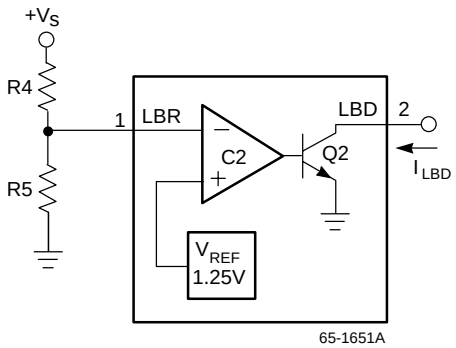


Figure 13. Low Battery Detector

Device Shutdown

The entire device may be shut down to an extremely low current non-operating condition by disconnecting the ground (pin 4). This can be easily done by putting an NPN transistor in series with ground pin and switching it with an external signal. This switch will not affect the efficiency of operation, but will add to and increase the reference voltage by an amount equal to the saturation voltage of the transistor used. A mechanical switch can also be used in series between circuit ground and pin 4, without introducing any reference offset.

Power Transistor Interfaces

The most important consideration in selecting an external power transistor is the saturation voltage at $I_C = I_{MAX}$. The lower the saturation voltage is, the better the efficiency will be. Also, a higher beta transistor requires less base drive and therefore less power will be.

Also, a higher beta transistor requires less base drive and therefore less power will be consumed in driving it, improving efficiency losses in the interface. The part numbers given in the following applications are recommended, but other types may be more appropriate depending on voltage and power levels.

When troubleshooting external power transistor circuits, ensure that clean, sharp-edged waveforms are driving the interface and power transistors. Monitor these waveforms with an oscilloscop—disconnect the inductor, and tie the V_{FB} input (pin 8) high through a 10K resistor. This will cause the regulator to pulse at maximum duty cycle without drawing excessive inductor currents. Check for expected on time and off time, and look for slow rise times that might cause the power transistor to enter its linear operating region.

The following external power transistor circuits may demand some adjustment to resistor values to satisfy various power levels and input/output voltages. C_X and L_X values must be selected according to the design equations (pages 2-213 and 2-214).

Inverting Medium Power Application

Figure 8 is a schematic of an inverting medium power supply (250mW to 1W) using an external PNP switch transistor. Supply voltage is applied to the IC via R3: when the internal switch transistor is turned on current through R4 is also drawn through R3; creating a voltage drop from base to emitter of the external switch transistor. This drop turns on the external transistor.

Voltage pulses on the supply lead (pin 6) do not affect circuit operation because the internal reference and bias circuitry have good supply rejection capabilities. A power Schottky diode is used for higher efficiency.

Inverting High Power Application

For higher power applications (500mW to 5W), refer to Figure 9. This circuit uses an extra external transistor to provide well controlled drive current in the correct phase to the power switch transistor. The value of R3 sets the drive current to the switch by making the interface transistor act as a current source. R4 and R5 must be selected such that the RC time constant of R4 and the base capacitance of Q2 do not slow the response time (and affect duty cycle), but not so low in value that excess power is consumed and efficiency suffers. The resistor values chosen should be proportional to the supply voltage (values shown are for +5V).

Step-Down Power Applications

Figures 16 and 17 show medium and high power interfaces modified to perform step-down functioning. The design

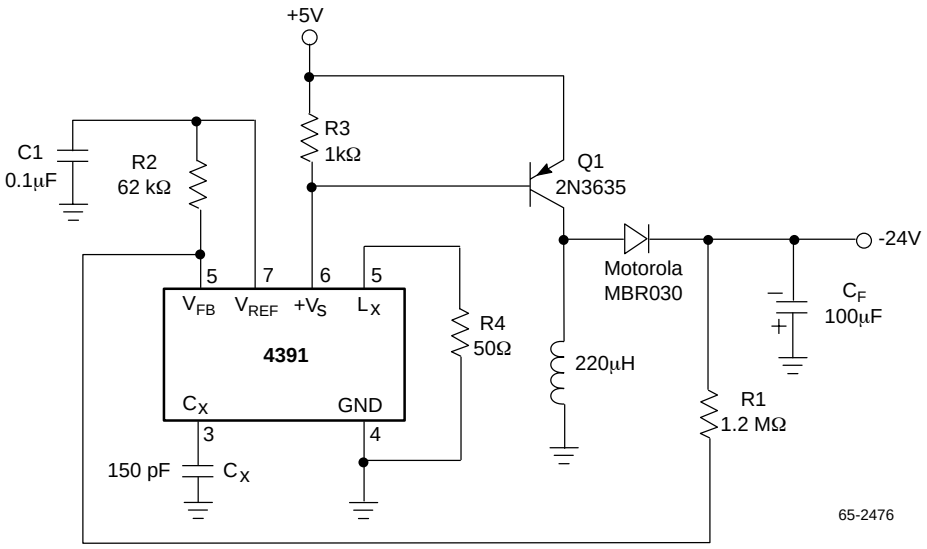


Figure 14. Inverting Medium Power Application

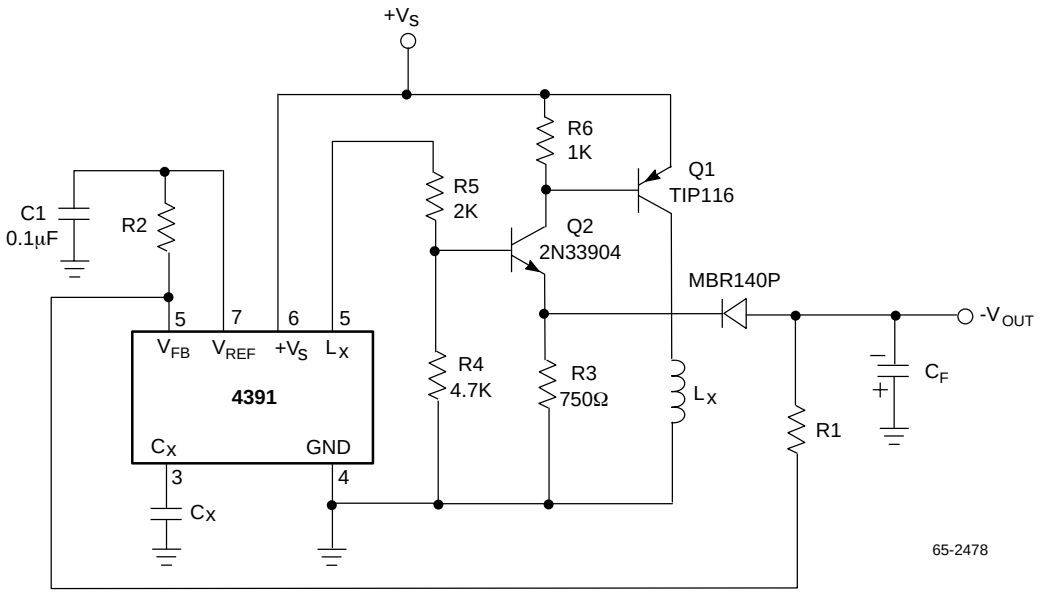


Figure 9. Inverting High Power Application

equations and suggestions for the circuits of Figures 14 and 15 also apply to these circuits. For a certain range of load power, the RC4193 can be used for step-sown applications. A load range from 400mW to 2W can be sustained with fewer components (especially when stepping down greater than 30V) than the comparable RC4391 circuit. Refer to Fairchild Semiconductor's RC4191/4192/4193 data sheet for a schematic of this medium power step-down application.

Voltage Dependent Oscillator

The RC4391's ability to supply load current at low battery voltages depends on the inductor value and the oscillator frequency. Low values of inductance or a low oscillator frequency will cause a higher peak inductor current and therefore increase the load current capability. A large inductor current is not necessarily best , however, because the large amount of energy delivered with each cycle will cause a large voltage ripple at the output, especially at high input voltages. This trade-off between load current capability and output ripple can be improved with the circuit connection shown in Figure 18. This circuit uses the low battery detector to sense for a low battery voltage condition and will decrease the oscillator frequency after a pre- programmed threshold is reached.

The threshold is programmed exactly as the normal low battery detector connection:

$$V_{TH} = V_{REF}\left(\frac{R4}{R5} + 1\right)$$

When the battery voltage reaches this threshold the comparator will turn on the open collector transistor at pin 2, effectively pulling C_Y in parallel with C_X. This added capacitance will reduce the oscillator frequency, according to the following equation:

$$F_O(Hz) = \frac{4.1x10^{-6}}{C_X(pF) + C_Y(pF)}$$

Current Limiting

The oscillator (C_X) pin can be used to add short circuit protection and to protect against over current at start-up (when using large values for the output filter capacitor —greater than 100 μF). A transistor V_{BE} is used as a current sensing comparator which resets the oscillator upon sensing an over current condition, thus providing cycle-by-cycle current limiting. Figure 19 shows how this is applied.

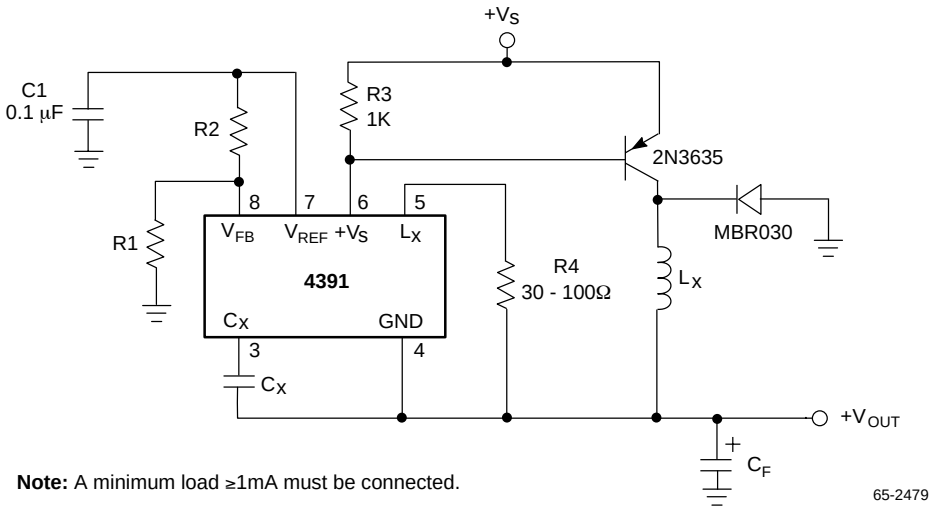


Figure 16. Step-Down Medium Power Application

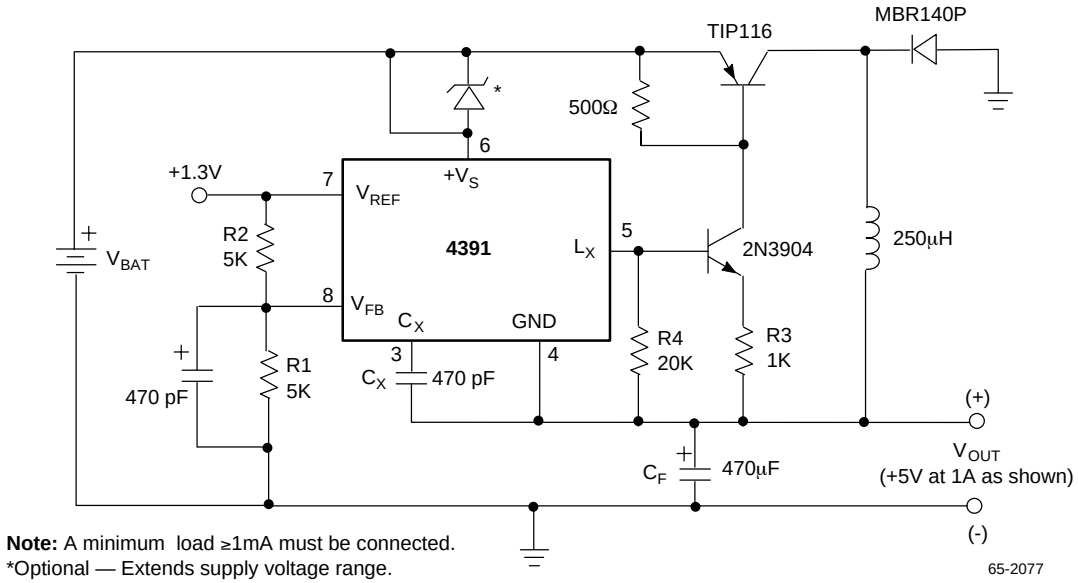


Figure 17. Step-Down High Power Application

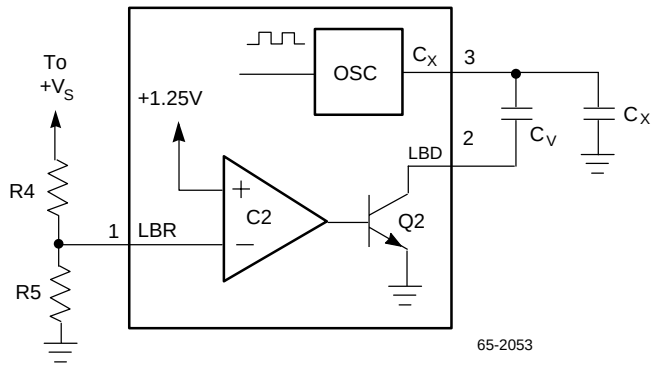


Figure 18. Voltage Dependent Oscillator

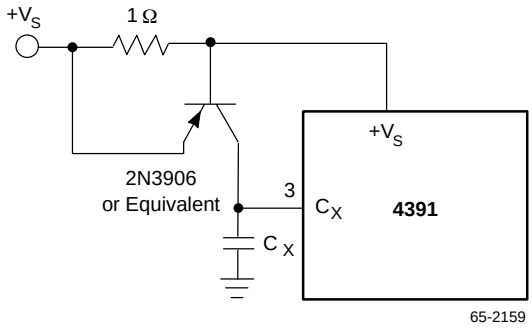
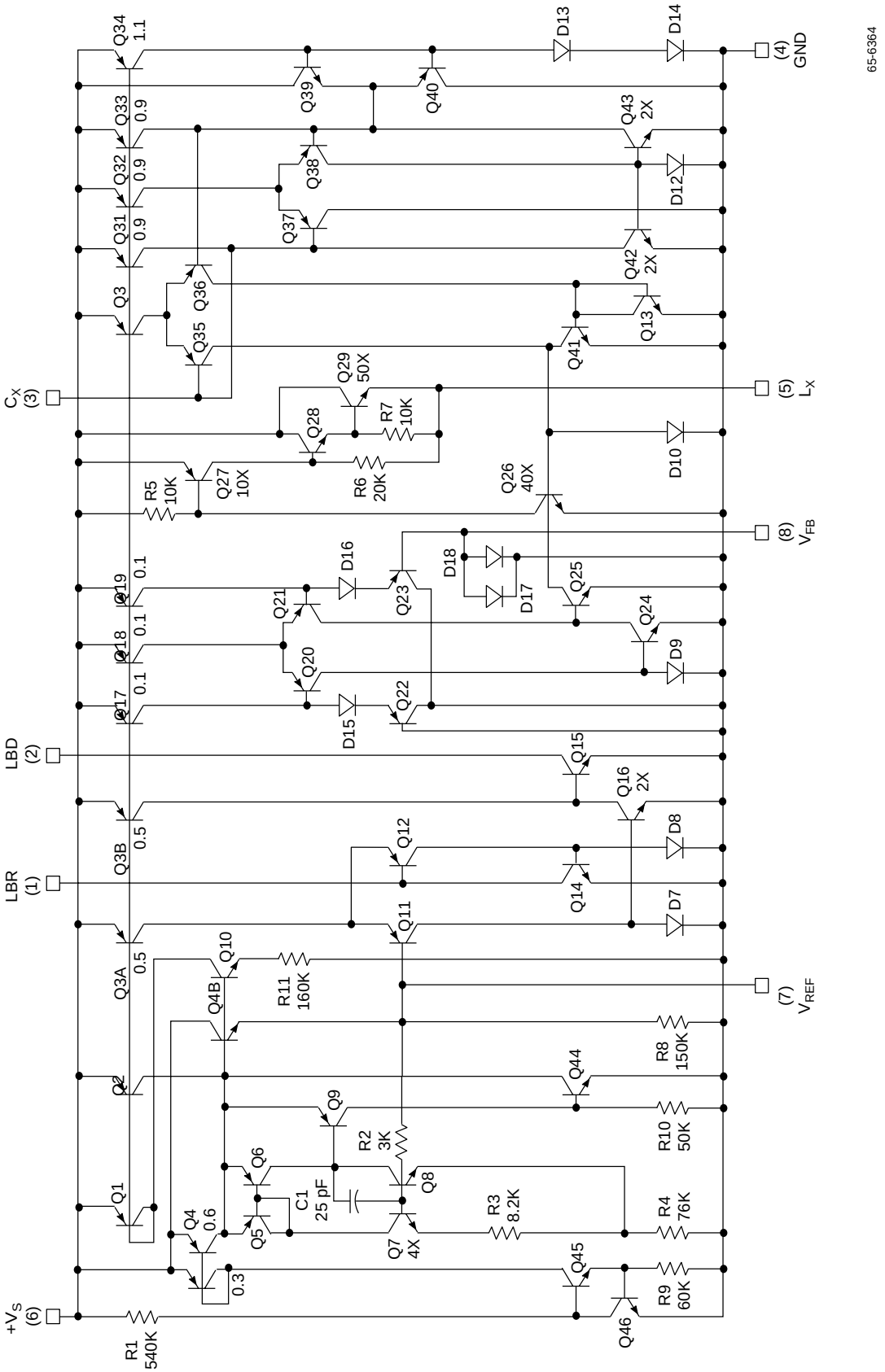
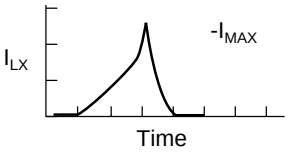
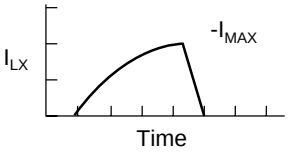
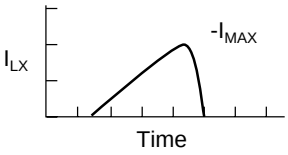


Figure 18. Current Limiting

Simplified Schematic Diagram



Troubleshooting Chart

Symptom	Possible Problems
Draws excessive supply current on star-up.	Inductance value too low. Output frequency (F_O) too low. Combination of low resistance inductor and high value filter capacitor — needs current limiting circuit (Figure 13).
Output voltage is low.	Inductance value too high for F_O or core saturating.
Inductor "sings" with audible hum.	Not potted well or bolted loosely.
L_X pin appears noisy — scope will not synchronize.	Normal operating condition.
 Inductor current shows nonlinear waveform.	Inductor is saturating: 1. Core too small. 2. Core too hot. 3. Operating frequency too low.
 Inductor current shows nonlinear waveform.	Waveform has resistive component: 1. Wire size too small. 2. Power transistor lacks base drive. 3. Components not rated high enough. 4. Battery has high series resistance.
 Inductor current is linear until high current is reached.	External transistor lacks base drive or beta is too low.
Poor efficiency.	Core saturating. Diode or transistor: 1. Not fast enough. 2. Not rated for current level (high $V_{CE}SAT$). High series resistance. Operating frequency too high.
Motorboating (erratic current pulses).	Loop stability problem — needs feedback from V_{OUT} to V_{FB} (pin 8), 100pF to 1000pF

Pot Core Inductor Design

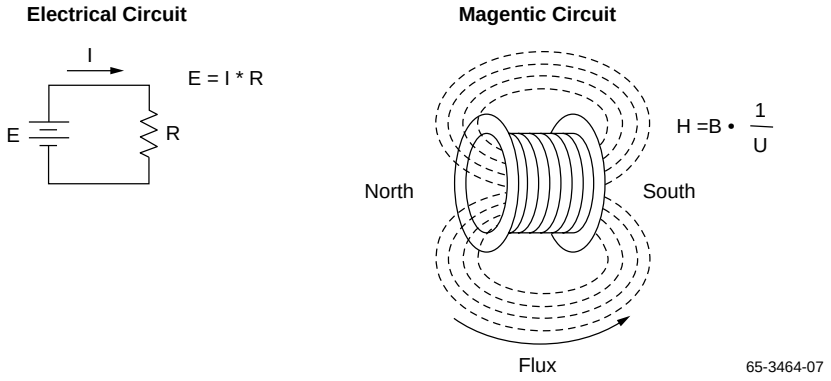


Figure 20. Electricity vs. Magnetism

Electricity Versus Magnetism

Electrically the inductor must meet just one requirement, but that requirement can be hard to satisfy. The inductor must exhibit the correct value of inductance (L, in Henrys) as the inductor current rises to its highest operating value (I_{MAX}). This requirement can be met most simply by choosing a very large core and winding it until it reaches the correct inductance value, but that brute force technique wastes size, weight and money. A more efficient design technique must be used.

Question: What happens if too small a core is used?

First, one must understand how the inductor's magnetic field works. The magnetic circuit in the inductor is very similar to a simple resistive electrical circuit. There is a magnetizing force (H, in oersteds), a flow of magnetism, or flux density (B, in Gauss), and a resistance to the flux, called permeability (U, in Gauss per oersted). H is equivalent to voltage in the electrical model, flux density is like current flow, and permeability is like resistance (except for two important differences discussed to the right).

First Difference: Permeability instead of being analogous to resistance, is actually more like conductance (1/R). As permeability increases, flux increases.

Second Difference: Resistance is a linear function. As voltage increases, current increases proportionally, and the resistance value stays the same. In a magnetic circuit the value of permeability varies as the applied magnetic force varies. This nonlinear characteristic is usually shown in graph form in ferrite core manufacturer's data sheet.

As the applied magnetizing force increases, at some point the permeability will start decreasing, and therefore the amount of magnetic flux will not increase any further, even as the magnetizing force increases. The physical reality is that, at the point where the permeability decreases, the magnetic field has realigned all of the magnetic domains in the core material. Once all of the domains have been aligned the core will then carry no more flux than just air, it becomes as if there were no core at all. This phenomenon is called saturation. Because the inductance value, L, is dependent on the amount of flux, core saturation will cause the value of L to decrease dramatically, in turn causing excessive and possibly destructive inductor current.

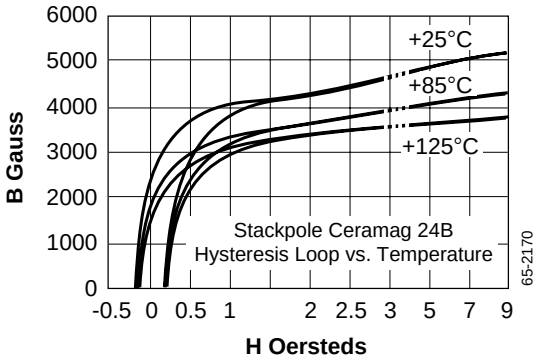


Figure 21. Typical Manufacturer's Curve Showing Saturation Effects

Pot Cores for RC4391

Pot core inductors are best suited for the RC4391 switching regulator for several reasons:

1. **They are available in a wide range of sizes.** RC4391 applications are usually low power with relatively low peak currents (less than 500mA). A small inexpensive pot core can be chosen to meet the circuit requirements.

2. **Pot cores are easily mounted.** They can be bolted directly to the PC card adjacent to the regulator IC.

3. **Pot cores can be easily air-gapped.** The length of the gap is simply adjusted using different washer thicknesses. cores are also available with predetermined air gaps.

4. **Electromagnetic interference (EMI) is kept to a minimum.** the completely enclosed design of a pot core reduces stray electromagnetic radiation—an important consideration if the regulator circuit is built on a PC card with other circuitry.

Not quite. Core size is dependent on the amount of energy stored, not on load power. Raising the operating frequency allows smaller cores and windings. Reduction of the size of the magnetics is the main reason switching regulator design tends toward higher operating frequency. Designs with the RC4391 should use 75 kHz as a maximum running frequency, because the turn off delay of the power transistor and stray capacitive coupling begin to interfere. Most applications are in the 10 to 50 kHz range, for efficiency and EMI reasons.

The peak inductor current (I_{MAX}) must reach a high enough value to meet the load current and simultaneously the inductor value is decreased, then the core can be made smaller. For a given core size and winding, an increase in air gap spacing (an air gap is a break in the material in the magnetic path, like a section broken off a doughnut) will cause the inductance to decrease and I_{MAX} (the usable peak current before saturation)to increase.

The curves shown are typical of the ferrite manufacturer's power HF material, such as Siemens N27 or Stackpole 24B, which are usually offered in standard millimeter sizes including the sizes shown.

Use of the Design Aid Graph

1. From the application requirement, determine the inductor value (L) and the required peak current (I_{MAX}).

2. Observe the curves of the design aid graph and determine the smallest core that meets both the L and I requirements.

3. Note the approximate air gap at IMAX for the selected core, and order the core with the gap. (If the gapping is done by the user, remember that a washer lspacer results in an air gap of twice the washer thickness, because two gaps will be created, one at the center post and one at the rim, like taking two bites from a doughnut.)

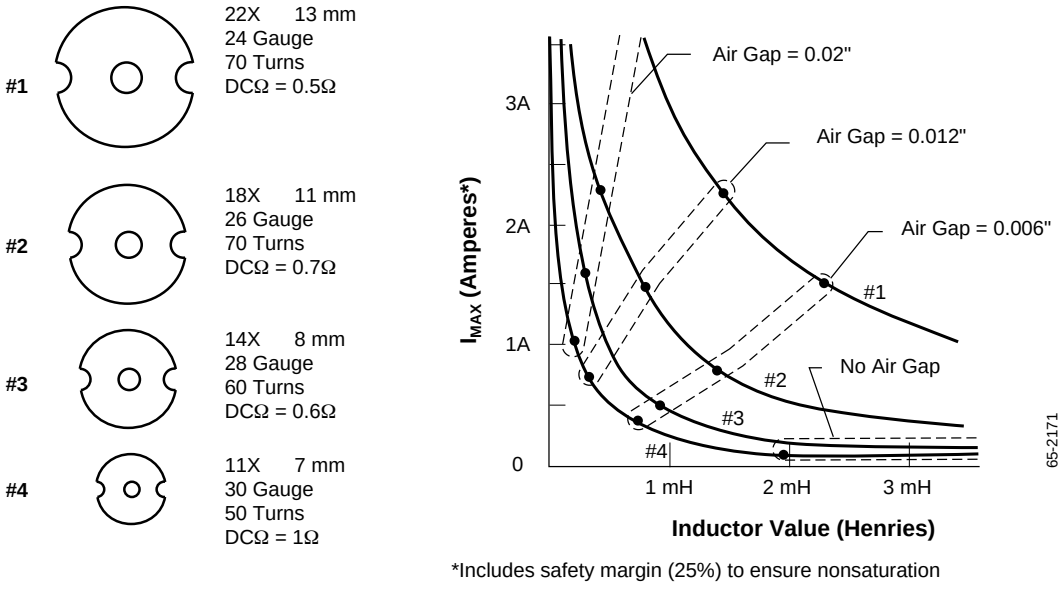
4. If the required inductance is equal to the indicated value on the graph, then wind the core with the number of turns shown in the table of sizes. The turns given are the maximum number for that gauge of wire that can be easily wound in cores winding area.

5. If the required inductance is less than the value indicated on the graph, a simple calculation must be done to find the adjusted number of turns. Find A_L (inductance index) for a specific air gap.

$$\frac{L(indicated)}{Turns^2} = A_L\left(\frac{inHenries}{Turn^2}\right)$$

Then divide the required inductance value by A_L to give the actual turns squared, and take the square root to find the actual turns needed.

$$ActualTurns = \frac{L(required)}{A_L}$$



*Includes safety margin (25%) to ensure nonsaturation

Figure 22. Inductor Design Aid

If the actual number of turns is significantly less than the number from the table then the wire size can be increased to use up the leftover winding area and reduce resistive losses.

6. Wind and gap the core as per calculations, and measure the value with an inductance meter. Some adjustment of the number of turns may be necessary.

The saturation characteristics may be checked with the inductor wired into the switching regulator application circuit. To do so, build and power up the circuit. Then clamp an oscilloscope current probe (recommend Tektronix P6042 or equivalent) around the inductor lead and monitor the current in the inductor. Draw the maximum load current from the application circuit so that the regulator is running at close to full duty cycle. Compare the waveform you see to those pictured.

Check for saturation at the highest expected ambient temperature.

7. After the operation in circuit has been checked, reassemble and pot the core using a potting compound recommended by the manufacturer.

   If the core material differs greatly in magnetic characteristics from the standard power material shown in Figure 16, then the following general equation can be used to help in winding and gapping. This equation can be used for any core geometry, such as an E-E core.

$$L_X = \frac{(1.26)(N^2)(Ae)(10^8)}{g = (le/ue)}$$

Where:

N = number of turns
Ae = core area from data sheet (in cm2)
le = magnetic path length from data sheet (in cm)
ue =permeability of core from manufacturer's graph
g = center post air gap (in cm)

Manufacturers

Below is a list of several pot core manufacturers:

Ferroxcube Company
5083 Kings Highway
Saugerties, NY 12477

Indiana General Electronics
Keasley, NJ 08832

Siemens Company
186 Wood Avenue South
Iselin, NJ 08830

Stackpole Company
201 Stackpole Street
St. Mary, PA 15857

TDK Electronics
13-1, 1-Chrome
Nihonbaski, Chuo-ku, Tokyo

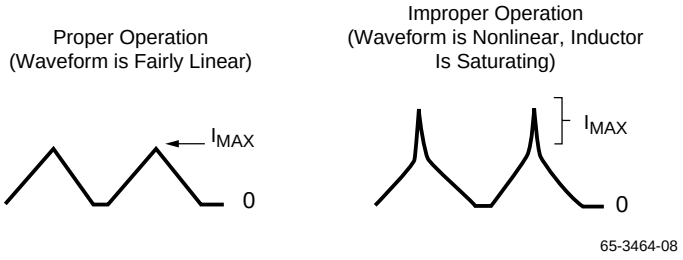


Figure 23. Inductor Current Waveforms

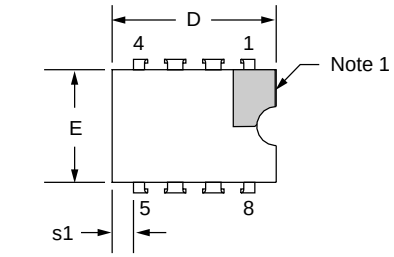
Mechanical Dimensions

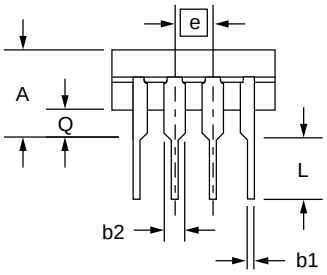
8-Lead Ceramic DIP Package

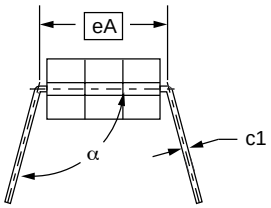
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2, 8
c1	.008	.015	.20	.38	8
D	—	.405	—	10.29	4
E	.220	.310	5.59	7.87	4
e	.100 BSC		2.54 BSC		5, 9
eA	.300 BSC		7.62 BSC		7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 4, 5 and 8 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 8.
6. Applies to all four corners (leads number 1, 4, 5, and 8).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Six spaces.







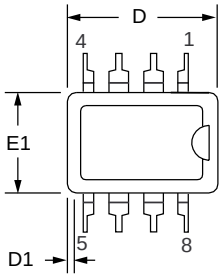
Mechanical Dimensions (continued)

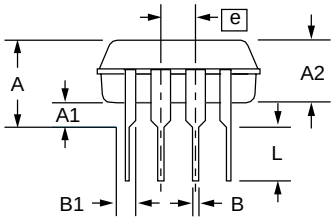
8-Lead Plastic DIP Package

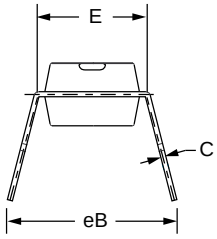
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	.348	.430	8.84	10.92	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.160	2.92	4.06	
N	8°		8°		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.







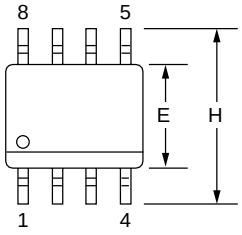
Mechanical Dimensions (continued)

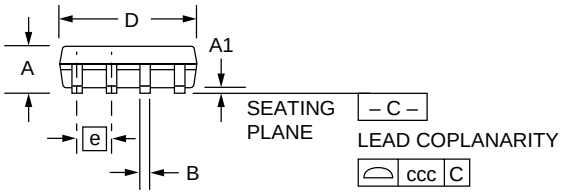
8-Lead SOIC Package

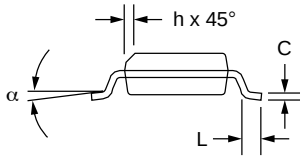
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.20	0.25	5
D	.189	.197	4.80	5.00	2
E	.150	.158	3.81	4.01	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	8		8		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Ordering Information

Part Number	Package	Operating Temperature Range
RC4391N	8 Lead Plastic DIP	0˚C to +70°C
RC4391M	8 Lead Plastic SOIC	0˚C to +70°C
RV4391N	8 Lead Plastic DIP	-25°C to +85°C
RM4391D	8 Lead Ceramic DIP	-55˚C to +125°C

RC4558

Dual High-Gain Operational Amplifier

Features

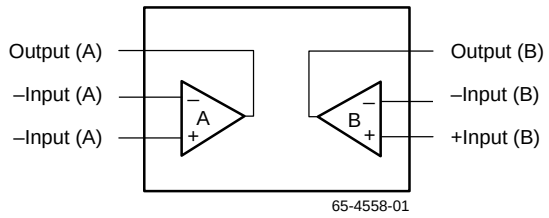
- 2.5 MHz unity gain bandwidth
- Supply voltage ±22V for RM4558 and ±18V for RC/RV4558
- Short-circuit protection
- No frequency compensation required
- No latch-up
- Large common-mode and differential voltage ranges
- Low power consumption
- Parameter tracking over temperature range
- Gain and phase match between amplifiers

Description

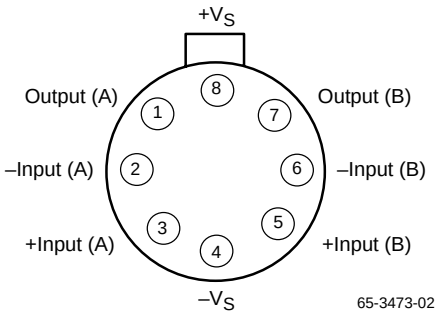
The RC4558 integrated circuit is a dual high-gain operational amplifier internally compensated and constructed on a single silicon IC using an advanced epitaxial process.

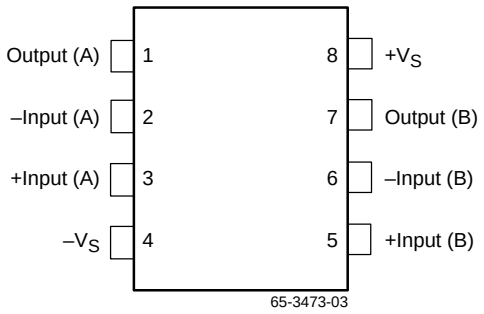
Combining the features of the 741 with the close parameter matching and tracking of a dual device on a monolithic chip results in unique performance characteristics. Excellent channel separation allows the use of this dual device in dense single 741 operational amplifier applications. It is especially well suited for applications in differential-in, differential-out as well as in potentiometric amplifiers and where gain and phase matched channels are mandatory.

Block Diagram



Pin Assignments





Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min	Typ	Max	Units
Supply Voltage	RM4558			±22	V
	RC4558			±18	
Input Voltage[2]				±15	V
Differential Input Voltage				30	V
$P_D T_A$ < 50°C	SOIC			300	mW
	PDIP			468	
	CerDIP			833	
	TO-99			658	
Junction Temperature	SOIC, PDIP			125	°C
	CerDIP, TO-99			175	
Operating Temperature	RM4558	-55		125	°C
	RC4558	0		70	
Lead Soldering Temperature	PDIP, CerDIP, TO-99 (60 sec)			300	°C
	SOIC (10 sec)			260	
Output Short Circuit Duration[3]		Indefinite			

Notes:

1. Functional operation under any of these conditions is NOT implied.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground on one op amp only. Rating applies to +75°C ambient temperature.

Matching Characteristics

(V_S = ±15V, T_A = +25°C unless otherwise specified)

Parameter	Test Conditions	Typ	Units
Voltage Gain	$R_L \geq 2\ k\Omega$	±1.0	dB
Input Bias Current	$R_L \geq 2\ k\Omega$	±15	nA
Input Offset Current	$R_L \geq 2\ k\Omega$	±7.5	nA

Electrical Characteristics

(V_S = ±15V and T_A = +25°C unless otherwise specified)

Parameters	Test Conditions	RM4558			RC4558			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \le 10k\Omega$		1.0	5.0		2.0	6.0	mV
Input Offset Current			5.0	200		5.0	200	nA
Input Bias Current			40	500		40	500	nA
Input Resistance		0.3	1.0		0.3	1.0		MΩ
Large Signal Voltage Gain	$R_L \ge 2k\Omega$, V_{OUT} = ±10V	50	300		20	300		V/mV
Output Voltage Swing	$R_L \ge 10k\Omega$	±12	±14		±12	±14		V
	$R_L \ge 2k\Omega$	±10	±13		±10	±13		V
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \le 10k\Omega$	70	100		70	100		dB
Power Supply Rejection Ratio	$R_S \le 10k\Omega$	76	100		76	100		dB
Power Consumption	$R_L = \infty$		100	170		100	170	mW
Transient Response	V_{IN} = 20 mV							
Rise Time	R_L = 2kΩ		0.3			0.3		μS
Overshoot	$C_L \le 100pF$		35			35		%
Slew Rate	$R_L \ge 2k\Omega$		0.8			0.8		V/μS
Channel Separation	F = 10kHz, R_S = 1kΩ		90			90		dB
Unity Gain Bandwidth (Gain = 1)		2.5	3.0		2.0	3.0		MHz

The following specifications apply for RM = -55°C ≤ T_A ≤ +125°C, RC = 0° ≤ T_A ≤ +70°C

Parameters	Test Conditions	RM4558			RC4558			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \le 10k\Omega$			6.0			7.5	mV
Input Offset Current								
RC4558				500			300	nA
Input bias Current								
RC4558				1500			800	nA
Large Signal Voltage Gain	$R_L \ge 2k\Omega$, V_{OUT} = ±10	25			15			V/mV
Output Voltage Swing	$R_L \ge 2k\Omega$	±10			±10			V
Power Consumption	$R_L = \infty$		120	200		120	200	mW

Typical Performance Characteristics

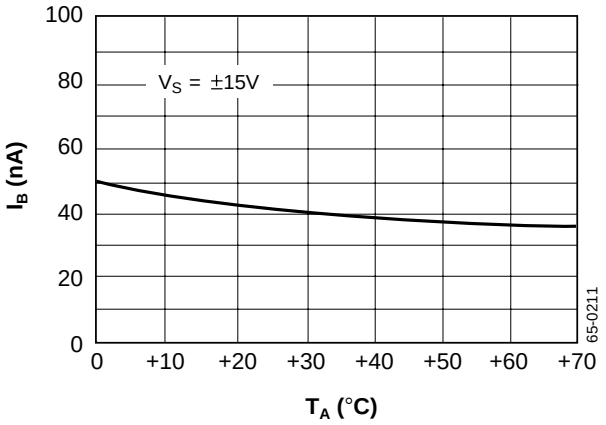


Figure 1. Input Bias Current vs. Temperature

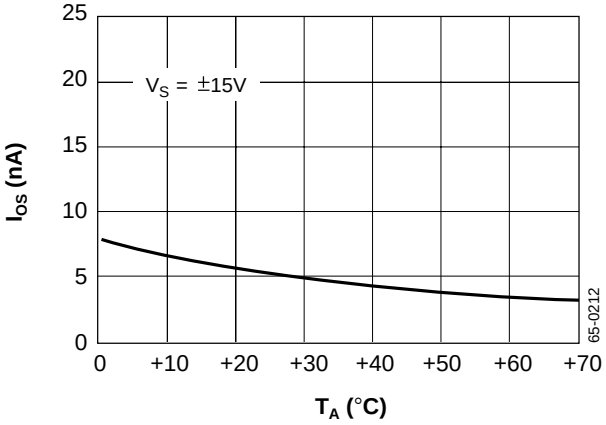


Figure 2. Input Offset Current vs. Temperature

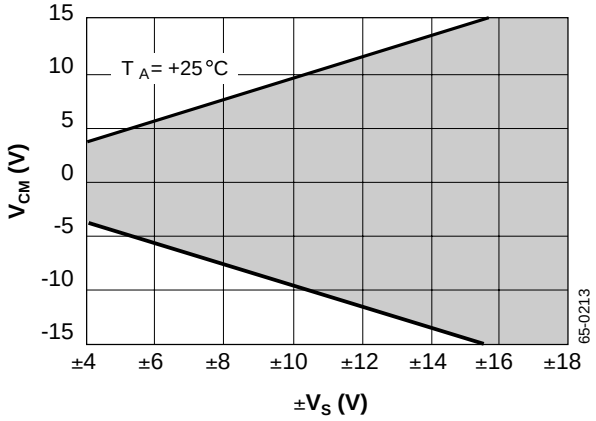


Figure 3. Input Common Mode Voltage Range vs. Supply Voltage

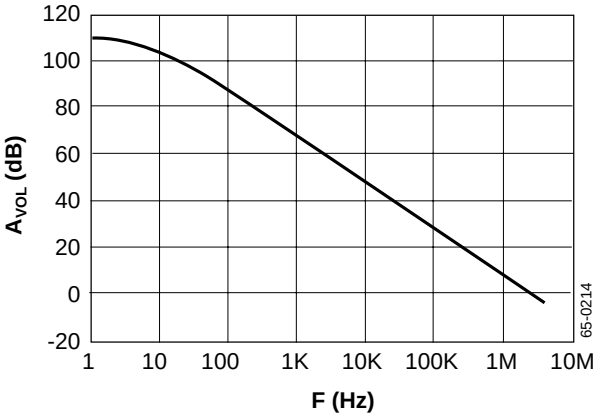


Figure 4. Open Loop Voltage Gain vs. Frequency

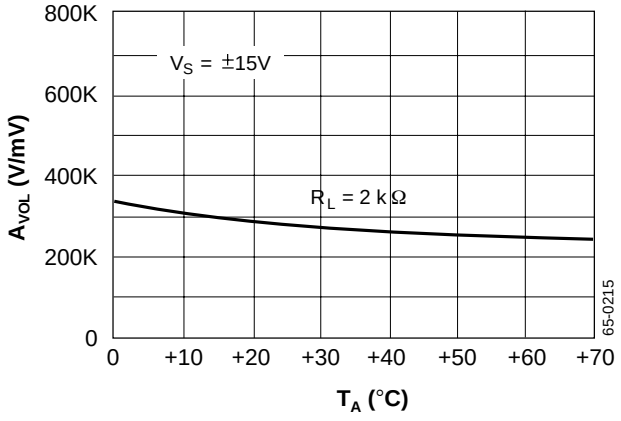


Figure 5. Open Loop Voltage Gain vs. Temperature

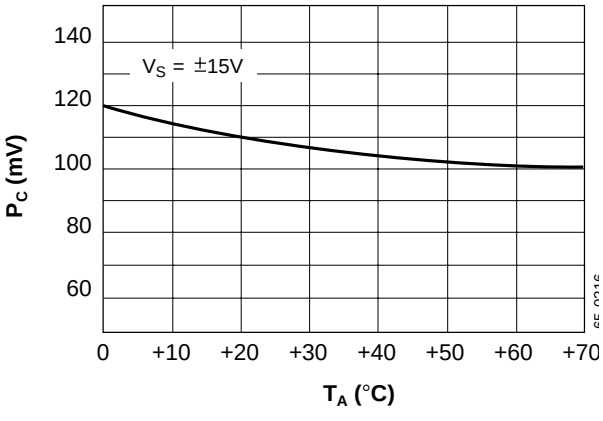


Figure 6. Power Consumption vs. Temperature

Typical Performance Characteristics (continued)

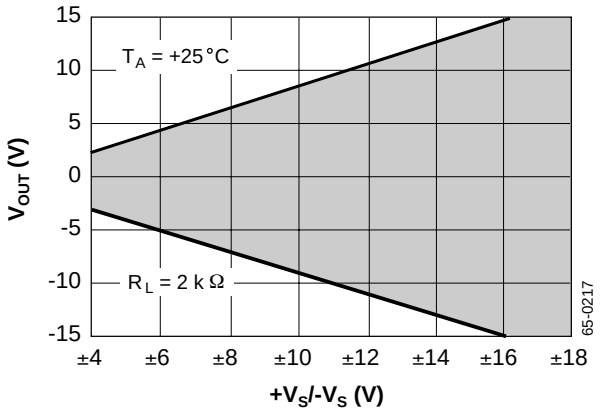


Figure 7. Output Voltage Swing vs. Supply Voltage

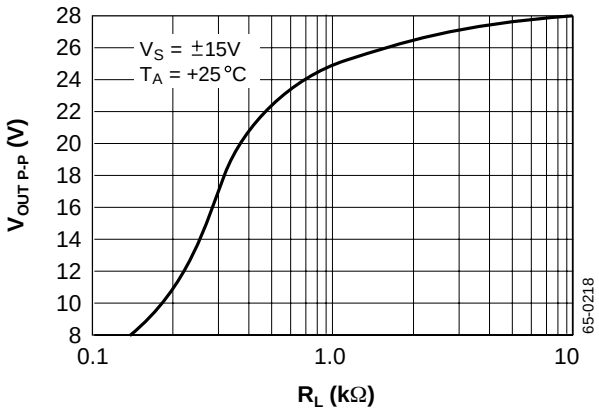


Figure 8. Output Voltage Swing vs. Load Resistance

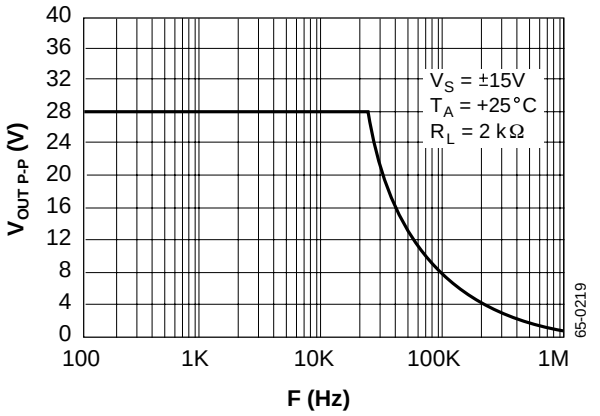


Figure 9. Output Voltage Swing vs. Freqeuncy

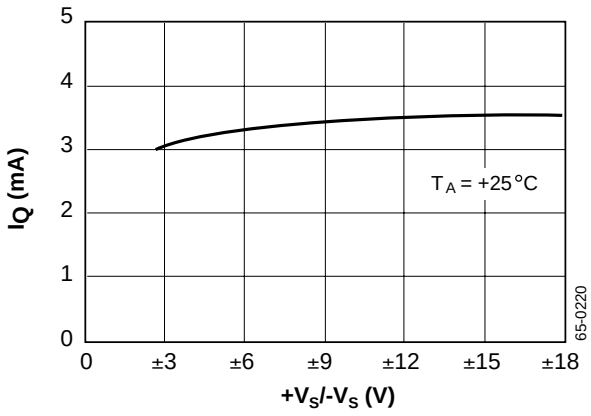


Figure 10. Quiescent Current vs. Supply Voltage

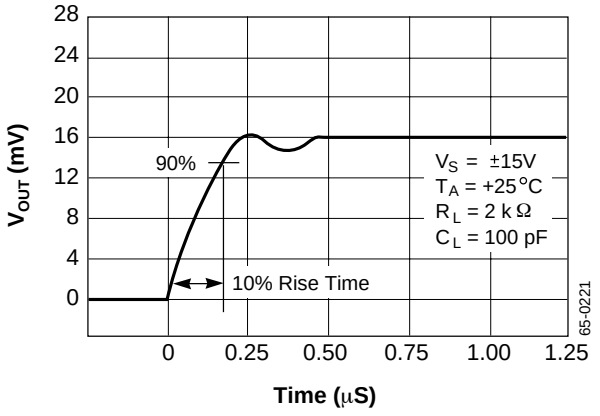


Figure 11. Transient Response Output Voltage vs. Time

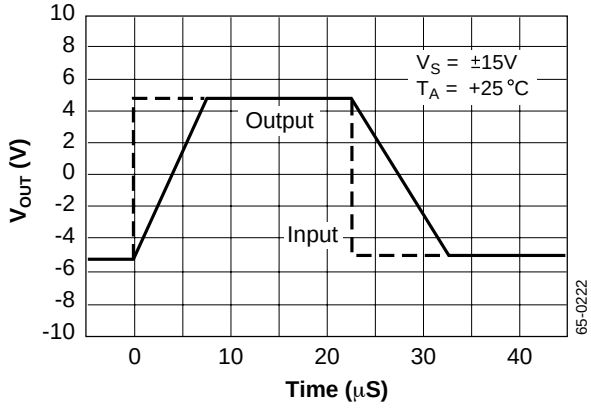


Figure 12. Follower Large Signal Pulse Response Output Voltage vs. Time

Typical Performance Characteristics (continued)

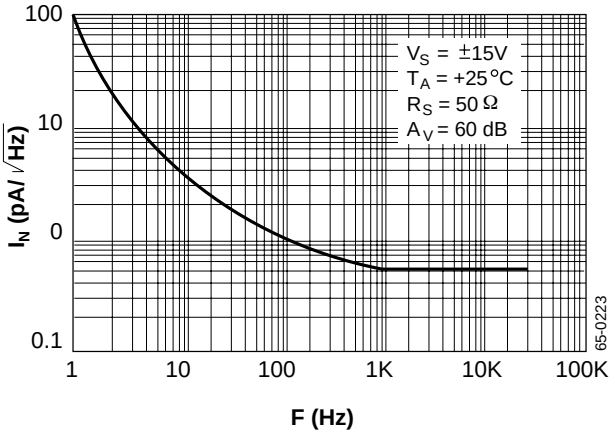


Figure 13. Input Noise Current Density vs. Frequency

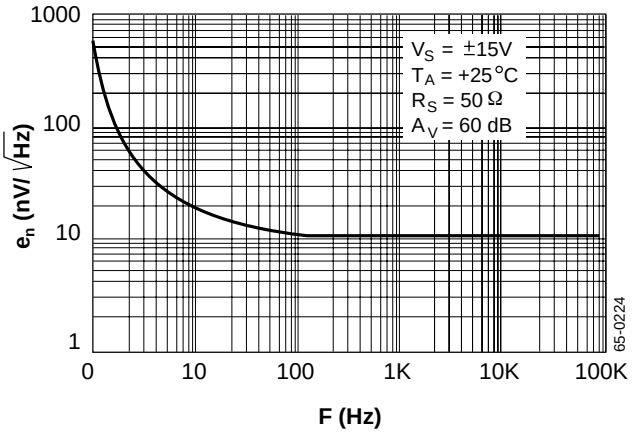


Figure 14. Input Noise Voltage Density vs. Frequency

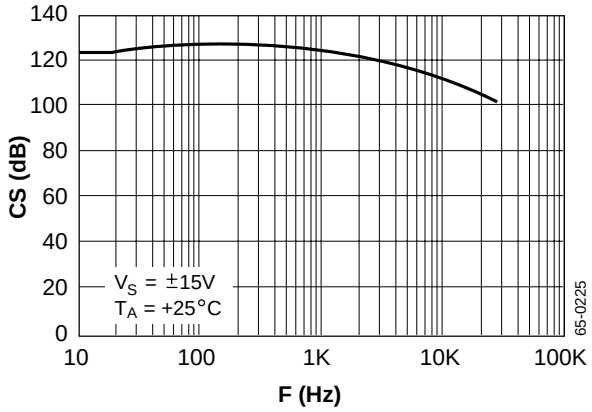


Figure 15. Channel Separation vs. Frequency

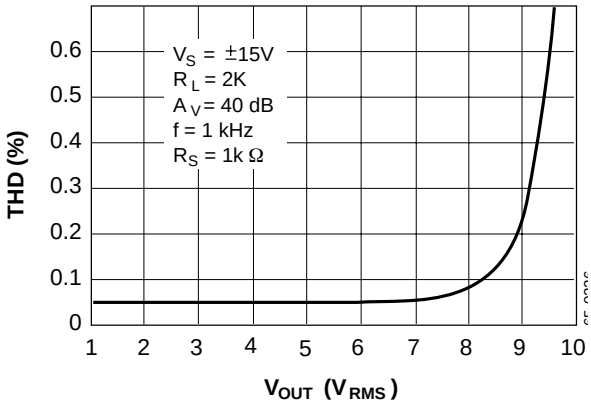


Figure 16. Total Harmonic Distortion vs Output Voltage

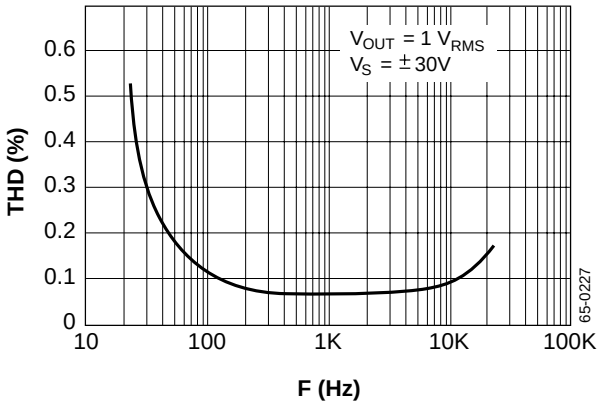


Figure 17. Distortion vs. Frequency

Typical Applications

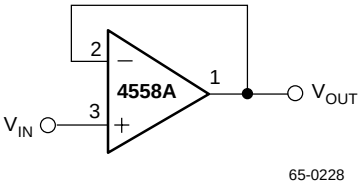


Figure 18. Voltage Follower

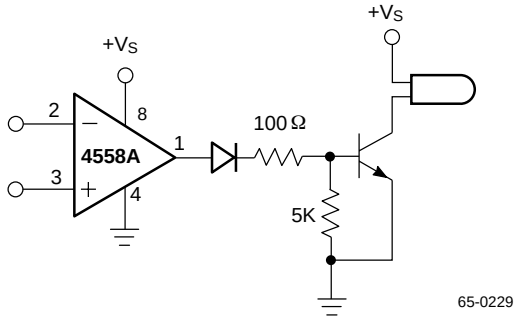


Figure 19. Lamp Driver

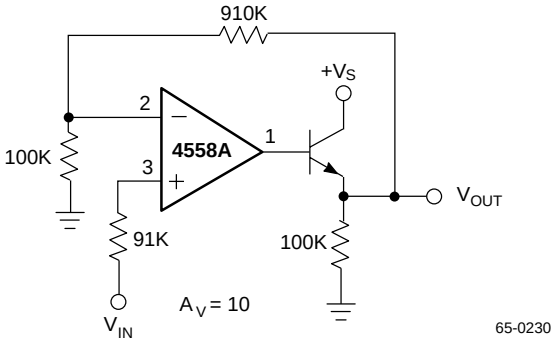


Figure 20. Power Amplifier

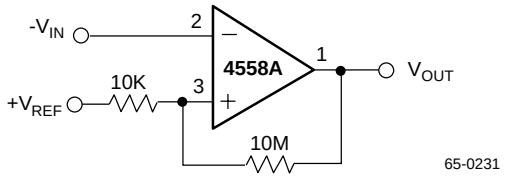


Figure 21. Comparator With Hysteresis

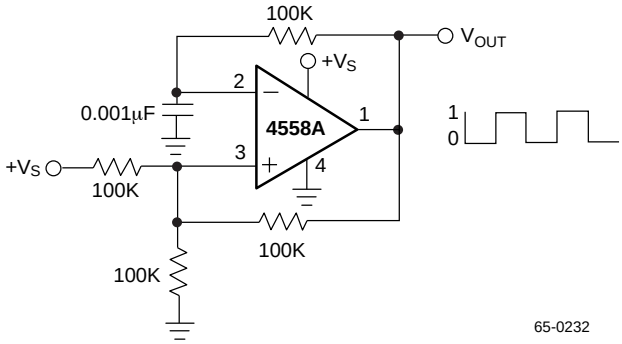


Figure 22. Squarewave Oscillator

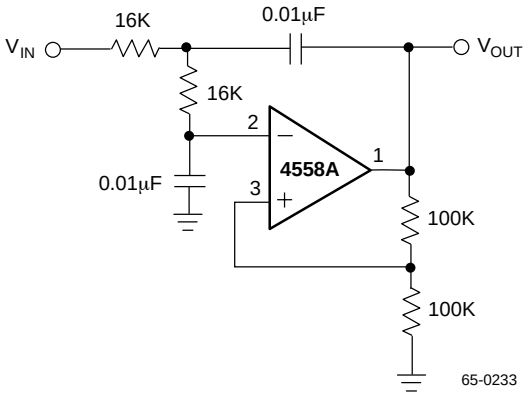


Figure 23. DC Coupled 1kHz Low-Pass Active Filter

Typical Applications (continued)

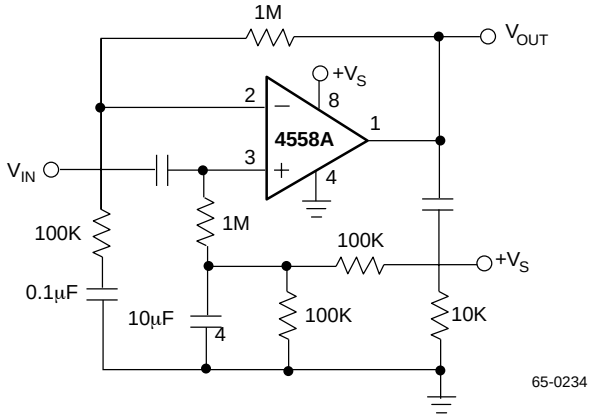


Figure 24. AC Coupled Non-Inverting Amplifier

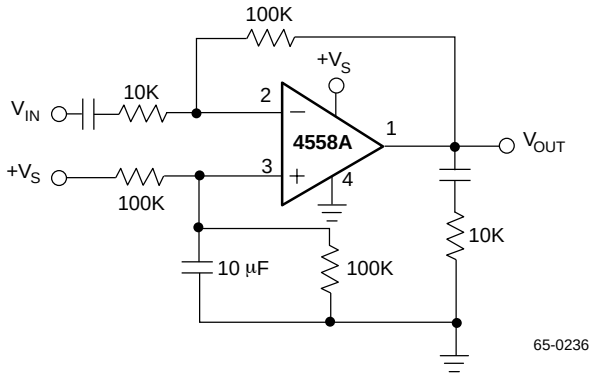


Figure 25. AC Coupled Inverting Amplifier

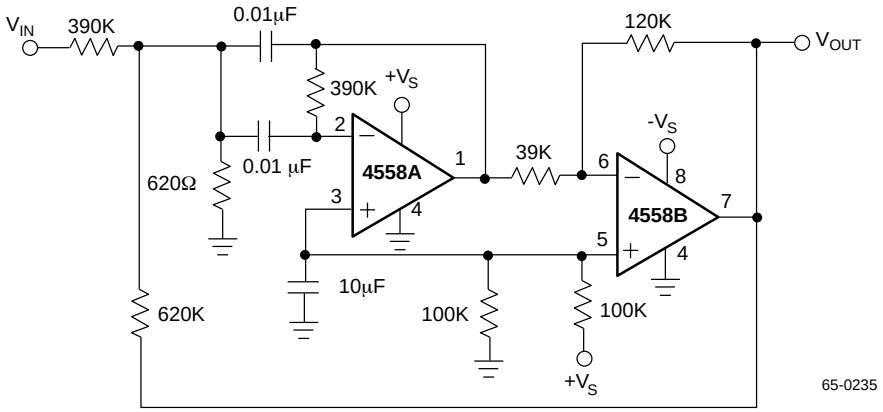


Figure 26. 1kHz Bandpass Active Filter

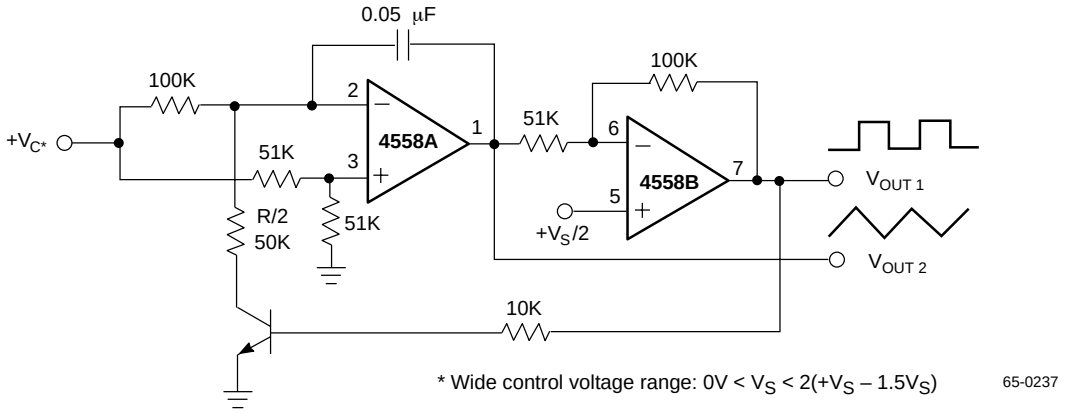
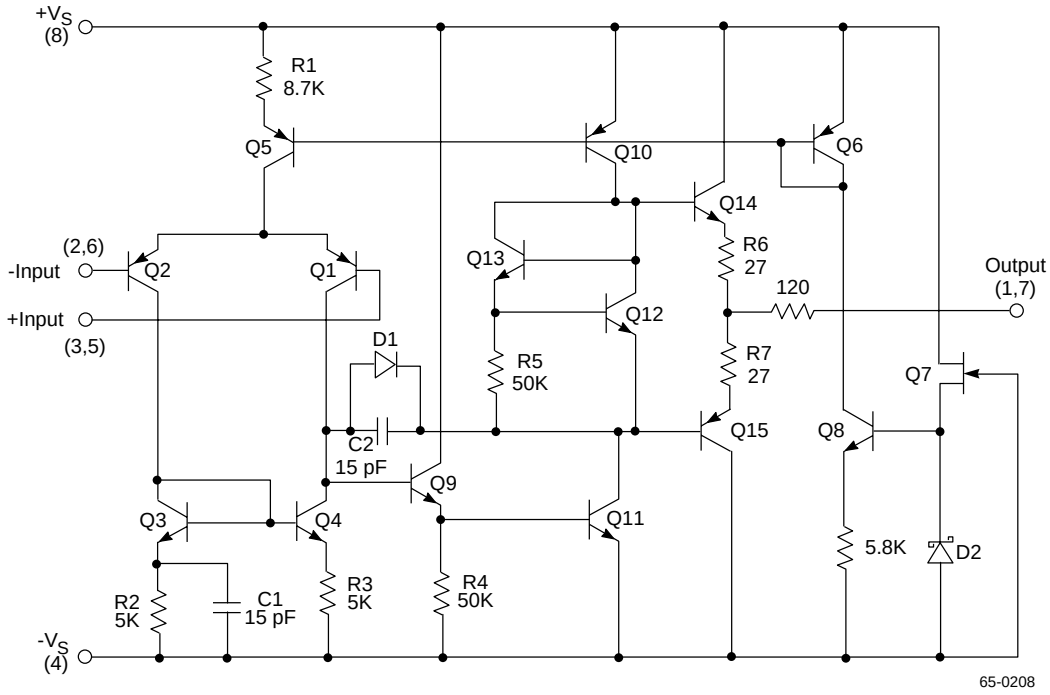


Figure 27. Voltage Controlled Oscillator (VCO)

Simplified Schematic Diagram



Ordering Information

Product Number	Temperature Range	Screening	Package
RC4558M	0° to 70°C	Commercial	8 Pin Wide SOIC
RC4558N	0° to 70°C	Commercial	8 Pin Plastic DIP
RM4558D	0° to 70°C	Commercial	8 Pin Ceramic DIP
RM4558D/883B	-55°C to +125°C	Military	8 Pin Ceramic DIP

Note:

1. /883B suffix denotes MIL-STD-883, Par. 1.2.1 compliant device.

5/20/98 0.0m 001
Stock#DS30004558

RC4559

Dual High-Gain Operational Amplifier

Features

- Unity gain bandwidth – 4.0 MHz
- Slew rate – 2.0 V/μS
- Low noise voltage – 1.4 μVRMS
- Supply voltage – ±22V for RM4559 and ±18V for RC4559
- No frequency compensation required
- No latch up
- Large common mode and differential voltage ranges
- Low power consumption
- Parameter tracking over temperature range
- Gain and phase match between amplifiers

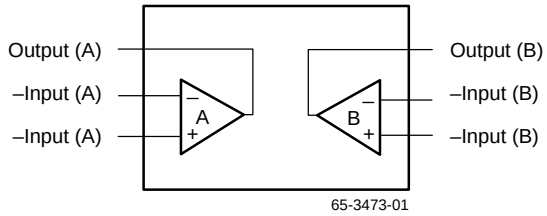
Description

The RC4559 integrated circuit is a high performance dual operational amplifier internally compensated and constructed on a single silicon chip using an advanced epitaxial process.

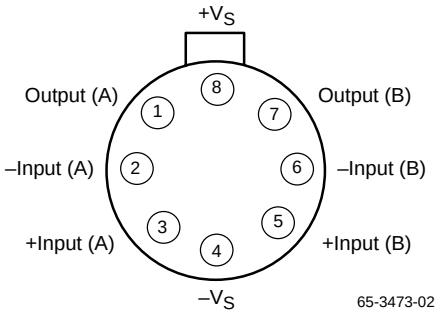
These amplifiers feature improved AC performance which far exceeds that of the 741-type amplifiers. The specially designed low-noise input transistors allow the RC4559 to be used in low-noise signal processing applications such as audio preamplifiers and signal conditioners.

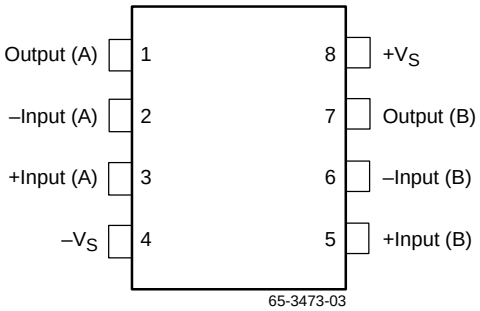
The RC4559 also has more output drive capability than 741-type amplifiers and can be used to drive a 600Ω load.

Block Diagram



Pin Assignments





Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min	Typ	Max	Units
Supply Voltage	RM4559			±22	V
	RC4559			±18	
Input Voltage[2]				±15	V
Differential Input Voltage				30	V
$P_D T_A$ < 50°C	SOIC			300	mW
	PDIP			468	
	CerDIP			833	
	TO-99			658	
Junction Temperature	SOIC, PDIP			125	°C
	CerDIP, TO-99			175	
Operating Temperature	RM4559	-55		125	°C
	RC4559	0		70	
Lead Soldering Temperature	PDIP, CerDIP, T0-99 (60 sec)			300	°C
	SOIC (10 sec)			260	
Output Short Circuit Duration[3]		Indefinite			

Notes:

1. Functional operation under any of these conditions is NOT implied.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground on one op amp only. Rating applies to +75°C ambient temperature.

Matching Characteristics

(V_S = ±15V, T_A = +25°C unless otherwise specified)

Parameter	Test Conditions	Typ	Units
Voltage Gain	$R_L \geq 2$ kΩ	±1.0	dB
Input Bias Current		±15	nA
Input Offset Current		±7.5	nA

Electrical Characteristics

(V_S = ±15V and T_A = +25°C unless otherwise specified)

Parameters	Test Conditions	RM4559			RC4559			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \le 10k\Omega$		1.0	5.0		2.0	6.0	mV
Input Offset Current			5.0	100		5.0	100	nA
Input Bias Current			40	250		40	250	nA
Input Resistance (Differential Mode)		0.3	1.0		0.3	1.0		MΩ
Large Signal Voltage Gain	$R_L \ge 2k\Omega$, V_{OUT} = ±10V	50	300		20	300		V/mV
Output Voltage Swing	$R_L \ge 10k\Omega$	±12	±14		±12	±14		V
	$R_L \ge 2k\Omega$	±10	±13		±10	±13		
	$R_L \ge 600\Omega$	±9.5	±10		±9.5	±10		
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \le 10k\Omega$	80	100		80	100		dB
Power Supply Rejection Ratio	$R_S \le 10k\Omega$	82	100		82	100		dB
Supply Current	$R_L = \infty$		3.3	5.6		3.3	5.6	mA
Transient Response								
Rise Time	V_{IN} = 20 mV, R_L = 2kΩ		80			80		μS
Overshoot	$C_L \le 100pF$		35			35		%
Slew Rate		1.5	2.0		1.5	2.0		V/μS
Unity Gain Bandwidth		3.0	4.0		3.0	4.0		MHz
Power Bandwidth	$V_{OUT} = 20V_{p-p}$	24	32		24	32		kHz
Input Noise Voltage[1]	F=20Hz to 20kHz		1.4	5.0		1.4	5.0	μV_{RMS}
Input Noise Current	F=20Hz to 20kHz		25			25		pA_{RMS}
Channel Separation	Gain = 100, F = 10kHz, R_S = 1kΩ		90			90		dB
The following specifications apply for RM = -55°C ≤ T_A ≤ +125°C, RC = 0° ≤ T_A ≤ +70°C								
Input Offset Voltage	$R_S \le 10k\Omega$			6.0			7.5	mV
Input Offset Current				300			200	nA
Input Bias Current				500			300	nA
Large Signal Voltage Gain	$R_L \ge 2k\Omega$, V_{OUT} = ±10V	25			15			V/mV
Output Voltage Swing	$R_L \ge 2k\Omega$	±10			±10			V
Supply Current	$R_L = \infty$		4.0	6.6		4.0	6.6	mA

Note:

1. Sample tested only.

Typical Performance Characteristics

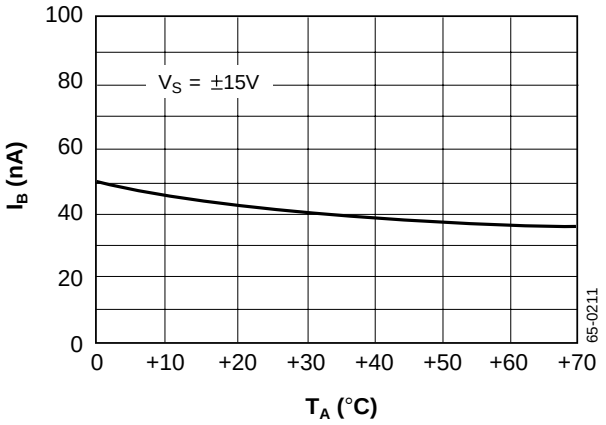


Figure 1. Input Bias Current vs. Temperature

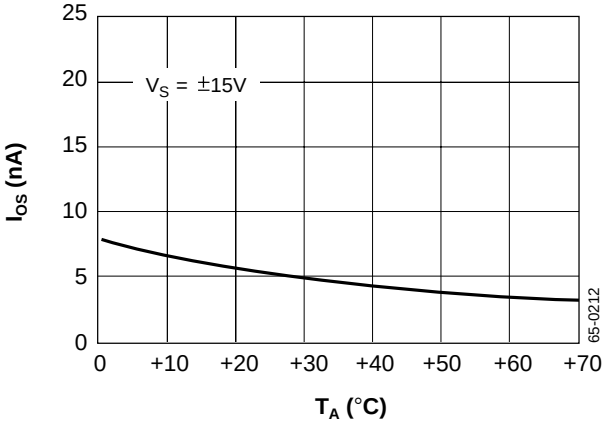


Figure 2. Input Offset Current vs. Temperature

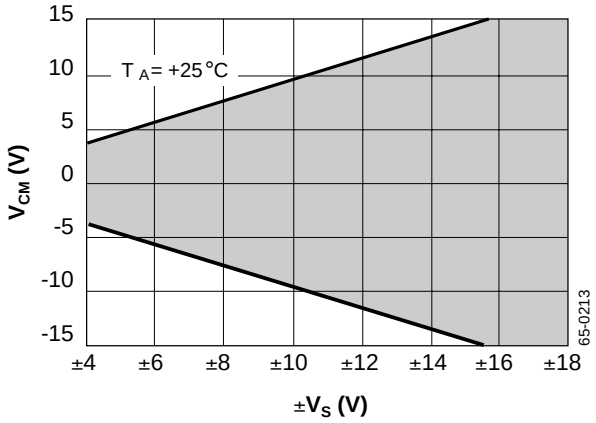


Figure 3. Input Common Mode Voltage Range vs. Supply Voltage

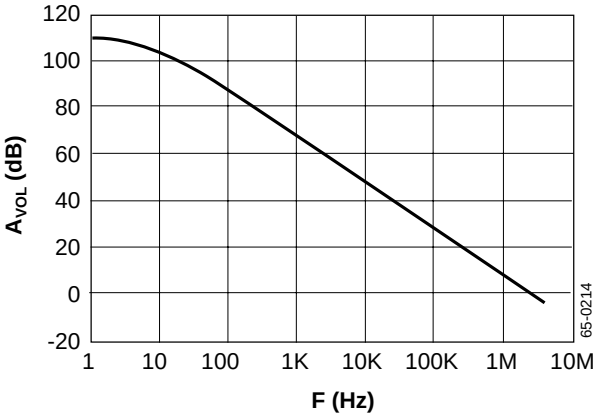


Figure 4. Open Loop Gain Voltage vs. Frequency

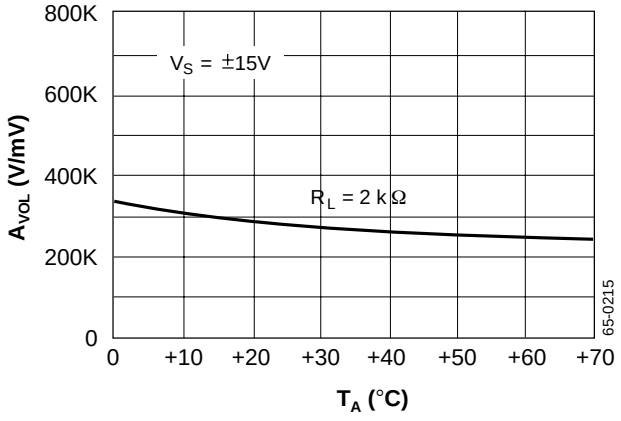


Figure 5. Open Loop Voltage Gain vs. Temperature

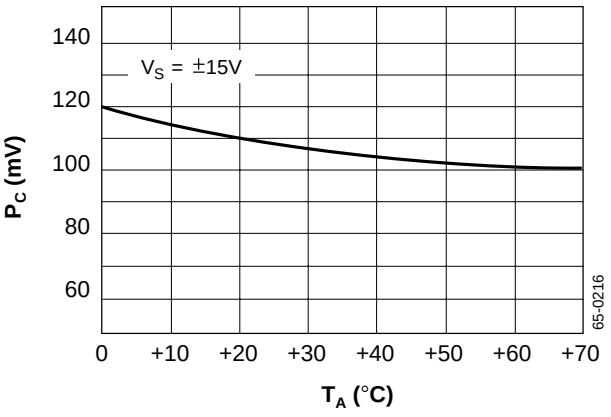


Figure 6. Power Consumption vs. Temperature

Typical Performance Characteristics (continued)

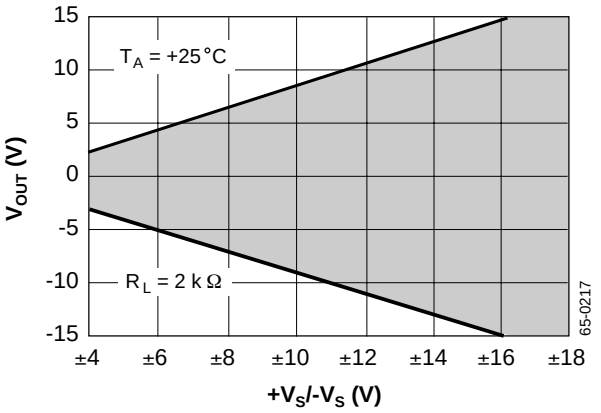


Figure 7. Output Voltage SWing vs. Supply Voltage

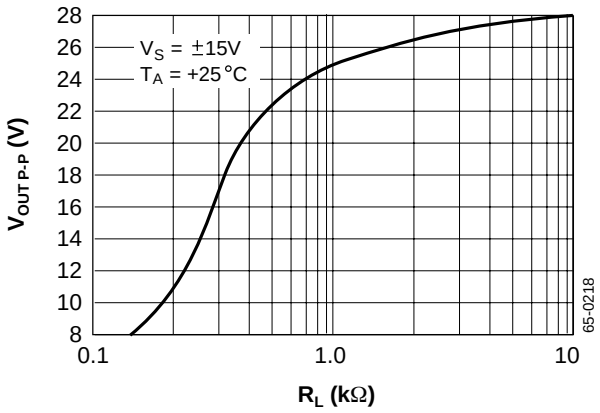


Figure 8. Output Voltage Swing vs. Load Resistance

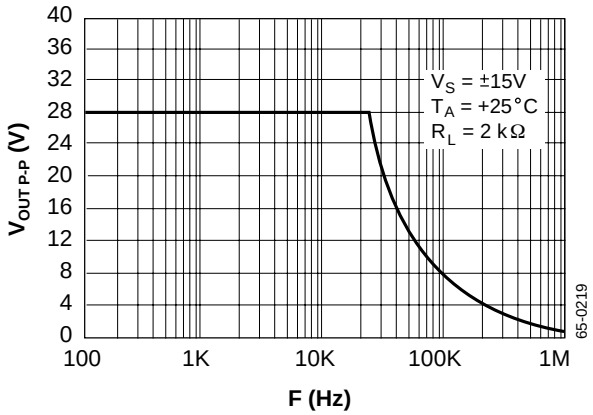


Figure 9. Output Voltage Swing vs. Frequency

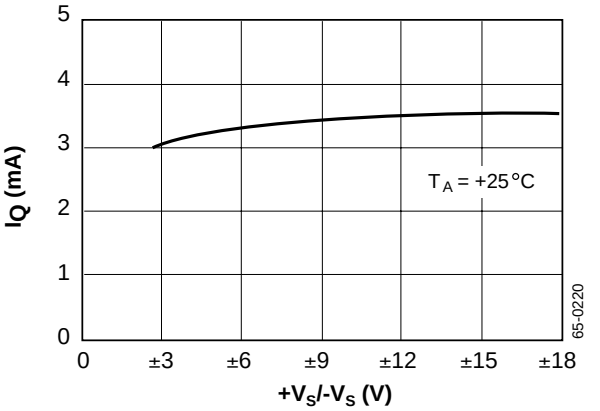


Figure 10. Quiescent Current vs. Supply Voltage

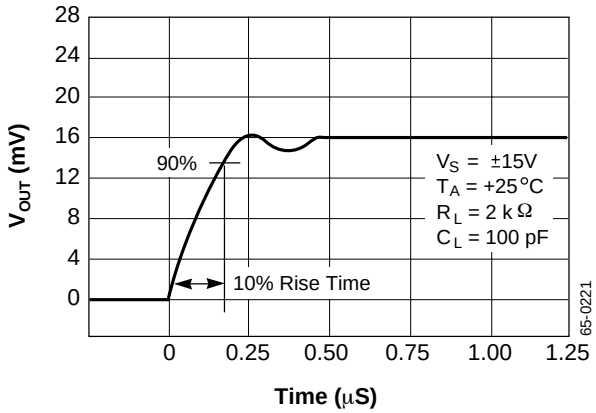


Figure 11. Transient Response Output Voltage vs. Time

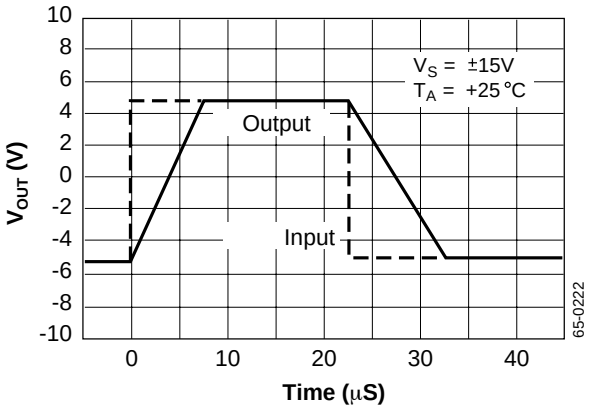


Figure 12. Follower Large Signal Pulse Response Output Voltage vs. Time

Typical Performance Characteristics (continued)

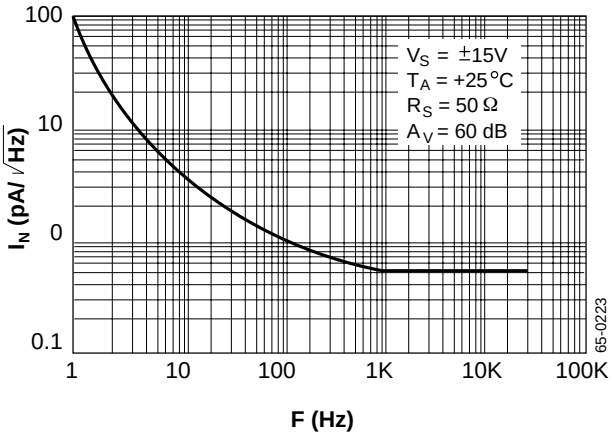


Figure 13. Input Noise Current Density vs. Frequency

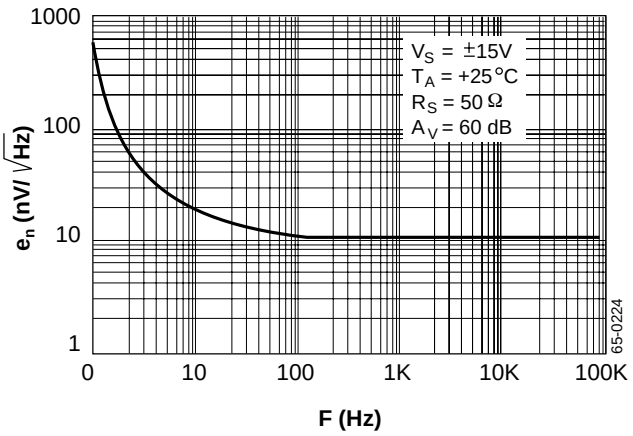


Figure 14. Input Noise Voltage Density vs. Frequency

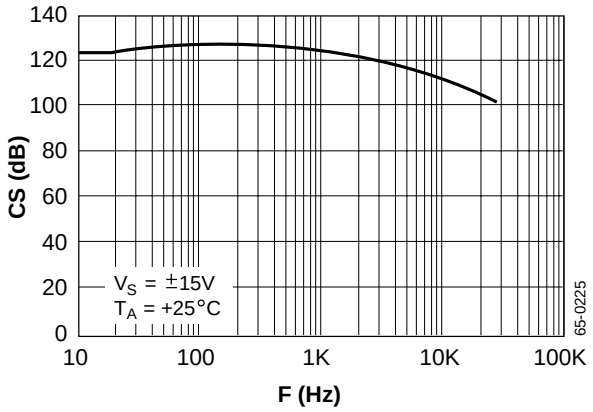


Figure 15. Channel Separation vs. Frequency

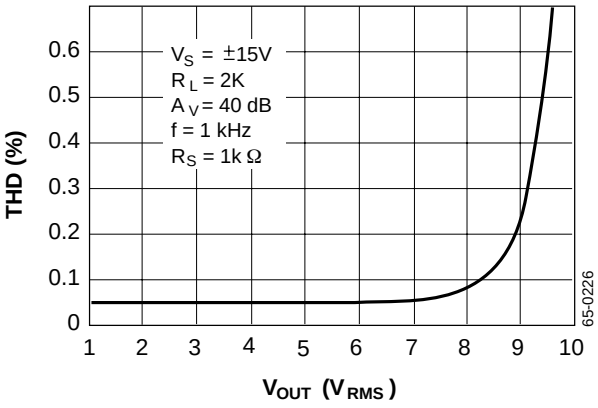


Figure 16. Total Harmonic Distortion vs. Output Voltage

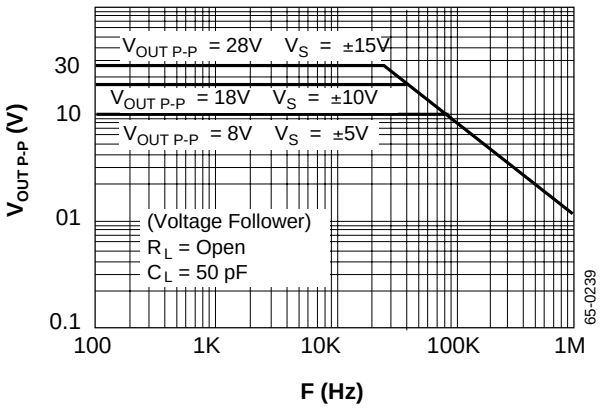


Figure 17. Output Voltage Swing vs. Frequency

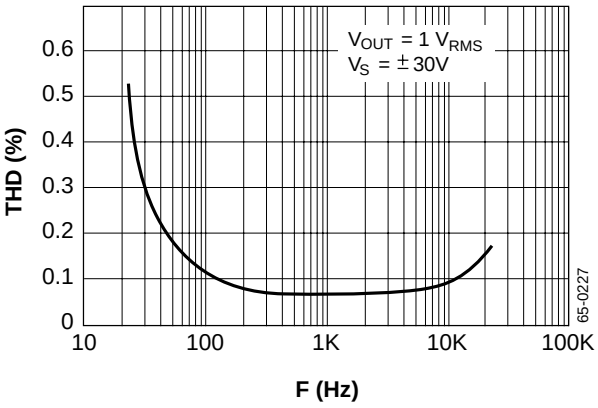


Figure 18. Distortion vs. Frequency

Typical Applications

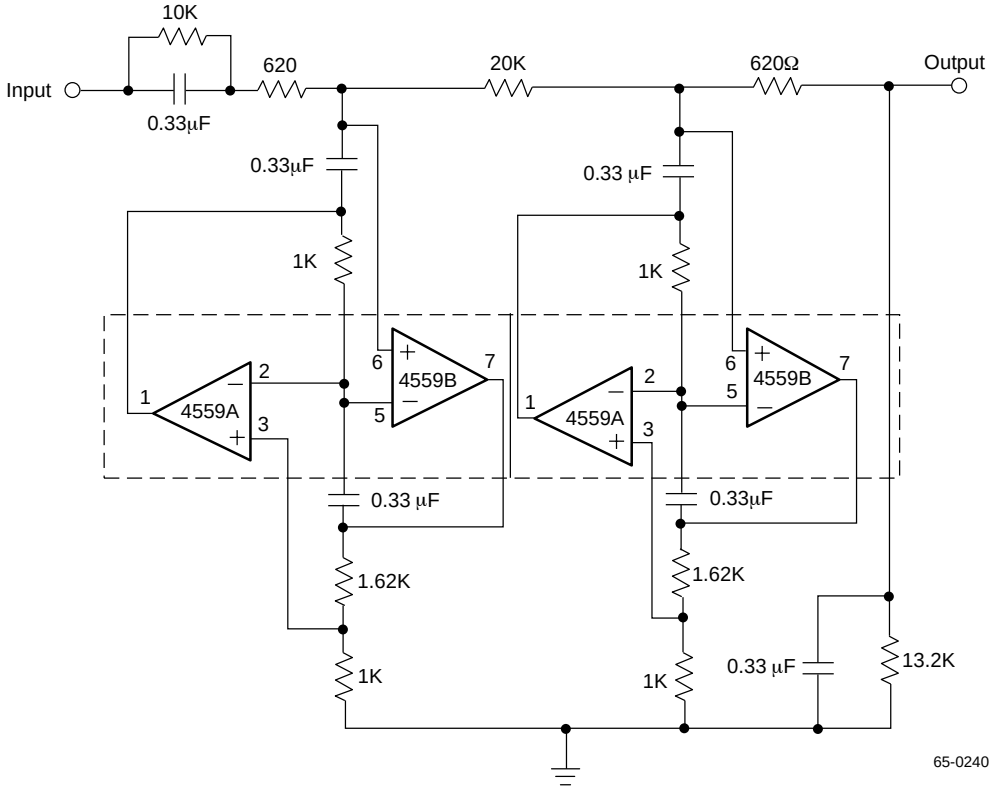


Figure 19. 400Hz Lowpass Butterworth Active Filter

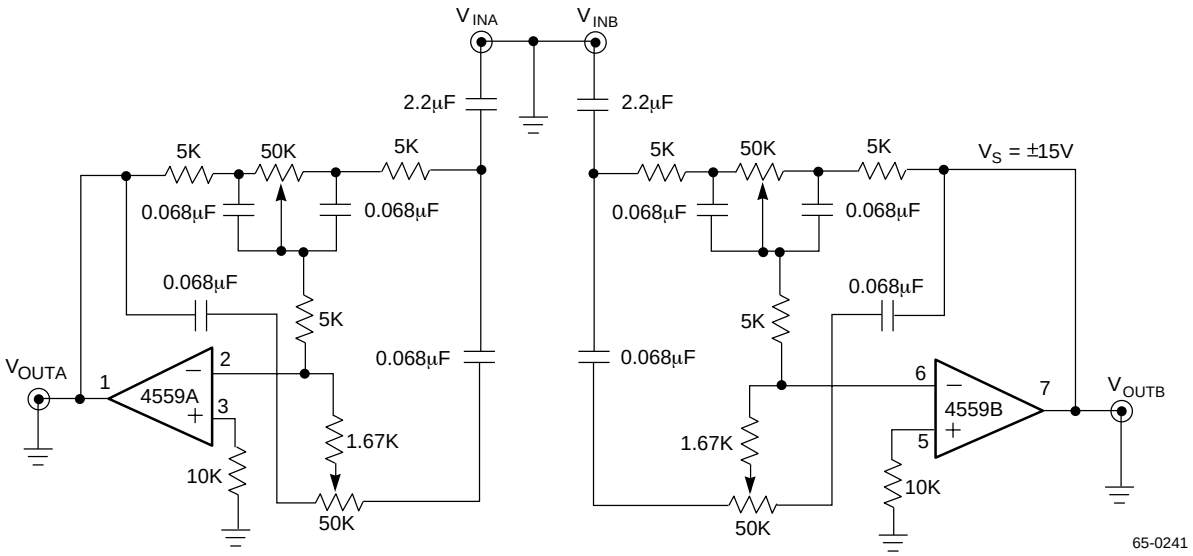


Figure 20. Stereo Tone Control

Typical Applications (continued)

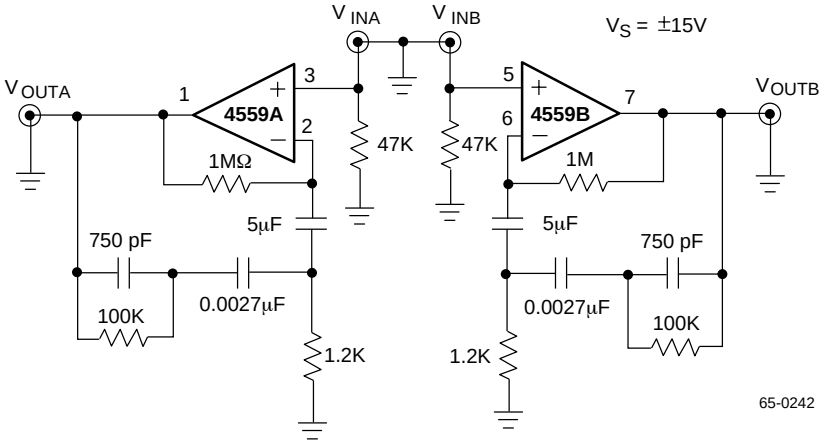


Figure 21. RIAA Preamplifier

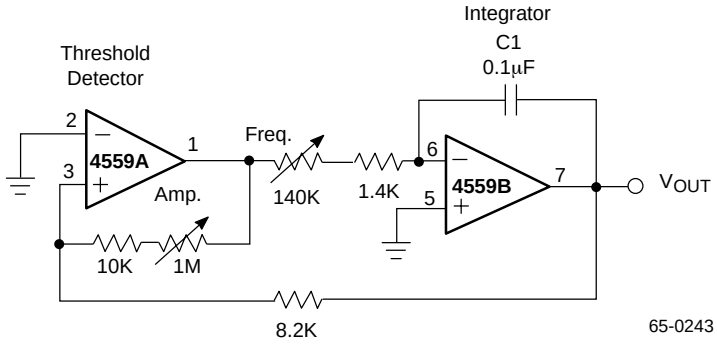


Figure 22. Triangular-Wave Generator

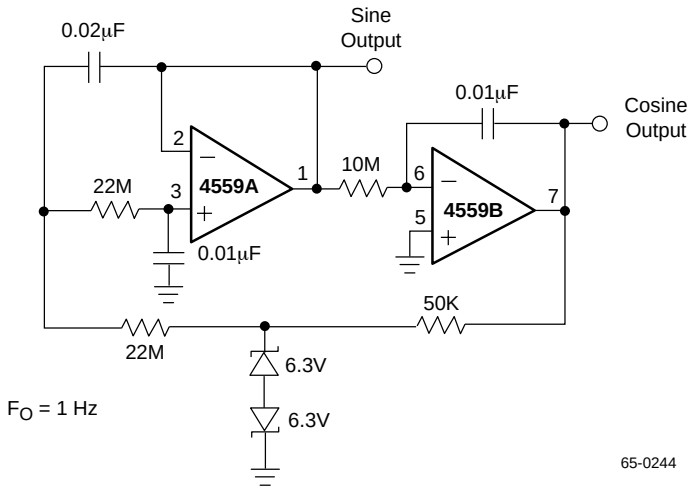
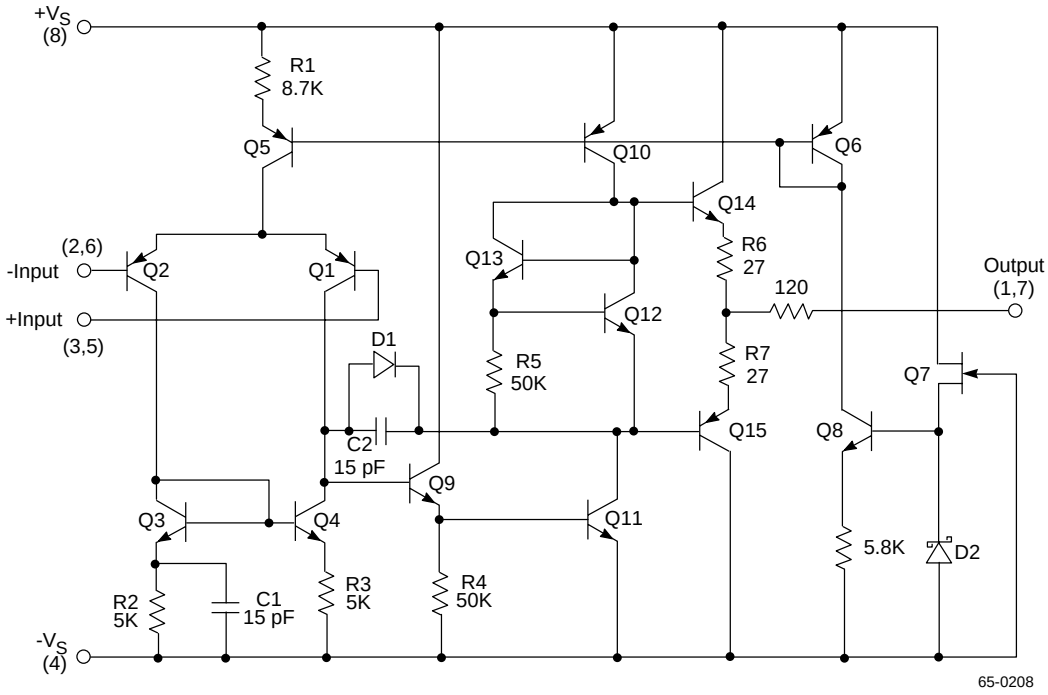


Figure 23. Low Frequency Sine Wave Generator with Quadrature Output

Simplified Schematic Diagram



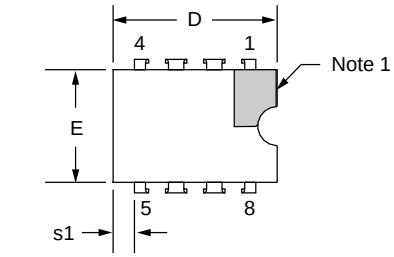
Mechanical Dimensions

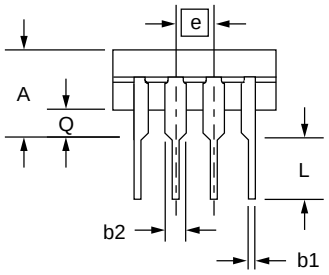
8-Lead Ceramic DIP Package

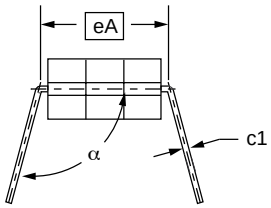
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2, 8
c1	.008	.015	.20	.38	8
D	—	.405	—	10.29	4
E	.220	.310	5.59	7.87	4
e	.100 BSC		2.54 BSC		5, 9
eA	.300 BSC		7.62 BSC		7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 4, 5 and 8 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 8.
6. Applies to all four corners (leads number 1, 4, 5, and 8).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Six spaces.







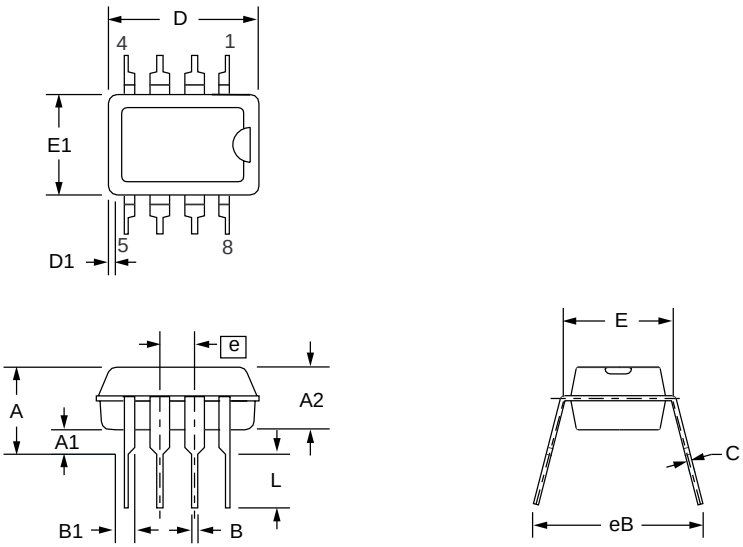
Mechanical Dimensions (continued)

8-Lead Plastic DIP Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	.348	.430	8.84	10.92	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.160	2.92	4.06	
N	8°		8°		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.



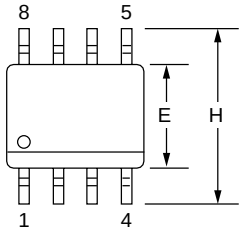
Mechanical Dimensions (continued)

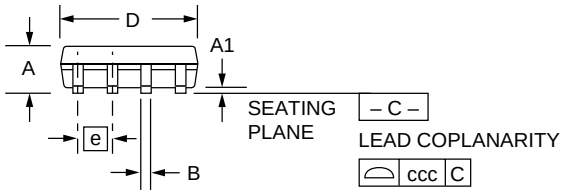
8-Lead SOIC Package

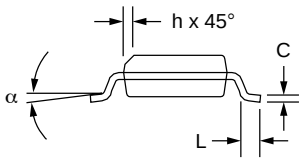
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.20	0.25	5
D	.189	.197	4.80	5.00	2
E	.150	.158	3.81	4.01	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	8		8		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.

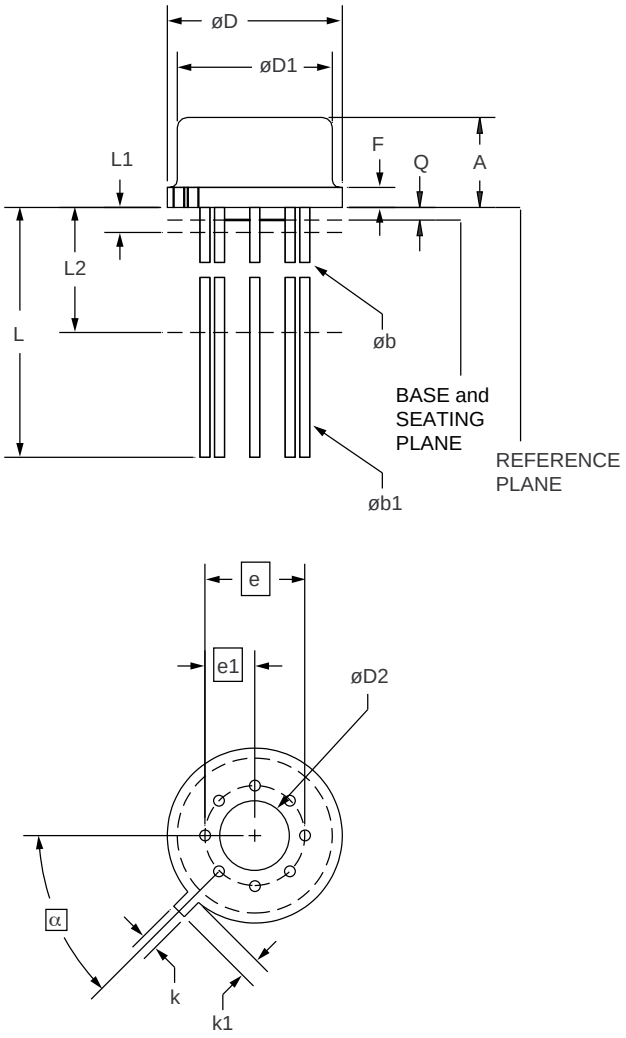






Mechanical Dimensions (continued)

8-Lead Metal Can IC Header Package



Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.185	4.19	4.70	
øb	.016	.019	.41	.48	1, 5
øb1	.016	.021	.41	.53	1, 5
øD	.335	.375	8.51	9.52	
øD1	.305	.335	7.75	8.51	
øD2	.110	.160	2.79	4.06	
e	.200 BSC		5.08 BSC		
e1	.100 BSC		2.54 BSC		
F	—	.040	—	1.02	
k	.027	.034	.69	.86	
k1	.027	.045	.69	1.14	2
L	.500	.750	12.70	19.05	1
L1	—	.050	—	1.27	1
L2	.250	—	6.35	—	1
Q	.010	.045	.25	1.14	
α	45° BSC		45° BSC		

Notes:

1. (All leads) øb applies between L1 & L2. øb1 applies between L2 & .500 (12.70mm) from the reference plane. Diameter is uncontrolled in L1 & beyond .500 (12.70mm) from the reference plane.
2. Measured from the maximum diameter of the product.
3. Leads having a maximum diameter .019 (.48mm) measured in gauging plane, .054 (1.37mm) +.001 (.03mm) –.000 (.00mm) below the reference plane of the product shall be within .007 (.18mm) of their true position relative to a maximum width tab.
4. The product may be measured by direct methods or by gauge.
5. All leads – increase maximum limit by .003 (.08mm) when lead finish is applied.

Ordering Information

Product Number	Temperature Range	Screening	Package
RC4559M	0° to 70°C	Commercial	8 Pin Wide SOIC
RC4559N	0° to 70°C	Commercial	8 Pin Plastic DIP
RC4559D	0° to 70°C	Commercial	8 Pin Ceramic DIP
RM4559D	-55°C to +125°C	Commercial	8 Pin Ceramic DIP
RM4559D/883B	-55°C to +125°C	Military	8 Pin Ceramic DIP
RM4559T	-55°C to +125°C	Commercial	8 Pin TO-99 Metal Can
RM4559T/883B	-55°C to +125°C	Military	8 Pin TO-99 Metal Can

Note:

1. /883B suffix denotes MIL-STD-883, Par. 1.2.1 compliant device.

5/20/98 0.0m 001
Stock#DS30004559

RC4560

Wide-Bandwidth Dual Operational Amplifier

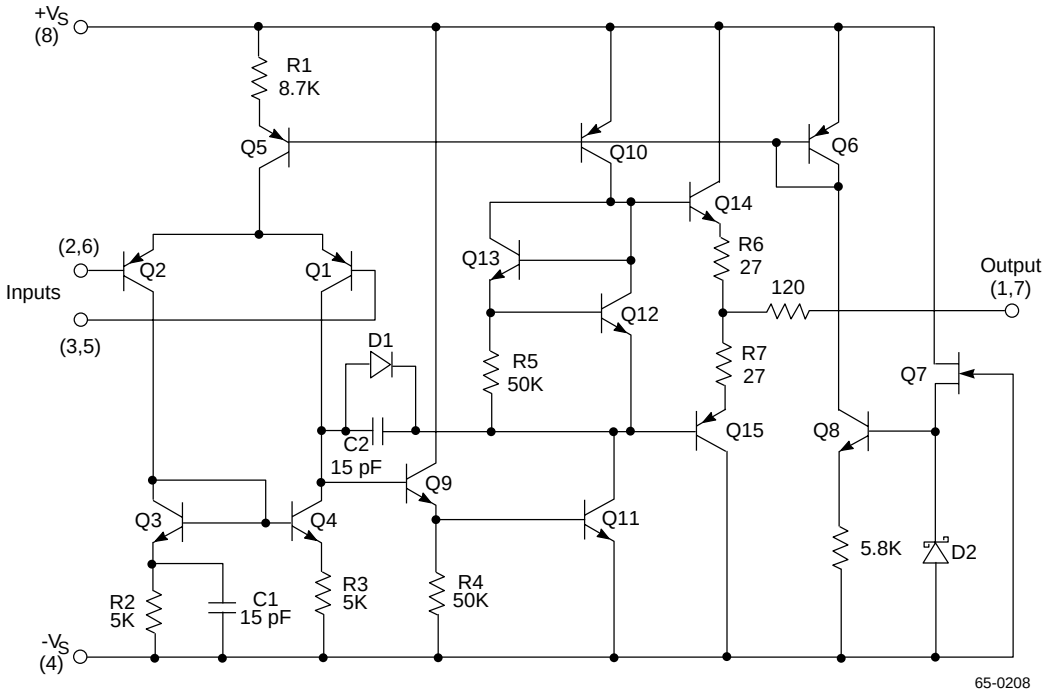
Features

- Unity gain bandwidth (A_V = 1) — 10 MHz
- Slew rate — 4.0V/μS
- Noise voltage at 1 kHz — 7.0nV/$\sqrt{Hz}$
- Noise voltage current at 1 kHz — 0.4pA/$\sqrt{Hz}$
- ±10V Output into 400Ω loads (±25mA)
- Supply current per amplifier — 1.8mA
- Input offset voltage — 2.0mV
- Input offset current — 5.0nA
- Unity gain frequency compensated
- Output short circuit protected

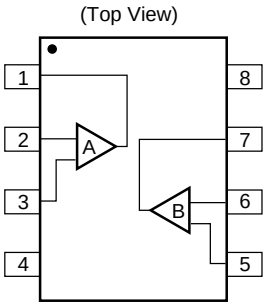
Description

The RC4560 integrated circuit is a high-gain, wide-bandwidth, dual operational amplifier capable of driving 20V peak-to-peak into 400Ω loads. The RC4560 combines many of the features of the RC4558 as well as providing the capability of wider bandwidth, and higher slew rate make the RC4560 ideal for active filters, data and telecommunications, and many instrumentation applications. The availability of the RC4560 in the surface mounted SOIC package allows it to be used in critical applications requiring very high packing densities.

Schematic Diagram (1/2 Shown)



Pin Assignments



Pin Descriptions

Pin	Function
1	A Output
2	A –Input
3	A +Input
4	$+V_S$
5	B +Input
6	B –Input
7	B Output
8	$–V_S$

Thermal Characteristics

	SOIC	Plastic DIP
Max. Junction Temp.	125°C	125°C
Max. $P_D T_A < 50°C$	300mW	468mW
Therm. Res. Θ_{JC}	—	—
Therm. Res. Θ_{JA}	240°C/W	160°C/W
For $T_A > 50°C$ Derate at	4.17mW/°C	6.25mW/°C

Absolute Maximum Ratings

(beyond which the device may be damaged)

Parameter		Max.
Supply Voltage		±18V
Input Voltage[1]		±15V
Differential Input Voltage		30V
Output Short Circuit Duration[2]		Indefinite
Operating Temperature Range		–20°C to +75°C
Lead Soldering Temperature	RC4560N	+300°C
	RC4560M	+260°C

Notes:

1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Short circuit may be to ground on one amp only. Rating applies to +75°C ambient temperature.

Matching Characteristics

(V_S = ±15V, T_A = +25°C)

Parameter	Conditions	Typ.	Units
Voltage Gain	$R_L \geq 2$ kΩ	±1.0	dB
Input Bias Current		±15	nA
Input Offset Current		±7.5	nA
Input Offset Voltage	$R_S \geq 10$ kΩ	±0.2	mV

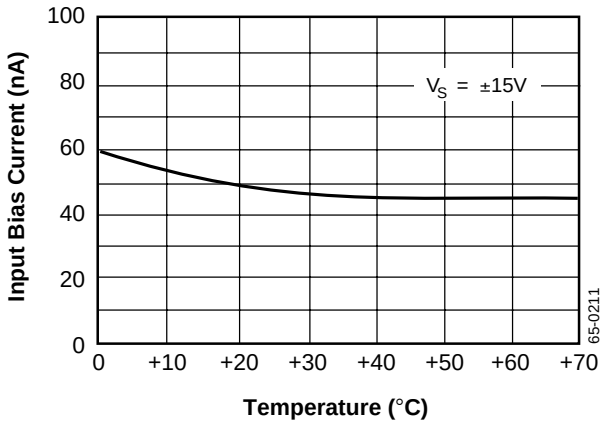
Electrical Characteristics

(V_S = ±15V and T_A = +25°C unless otherwise specified)

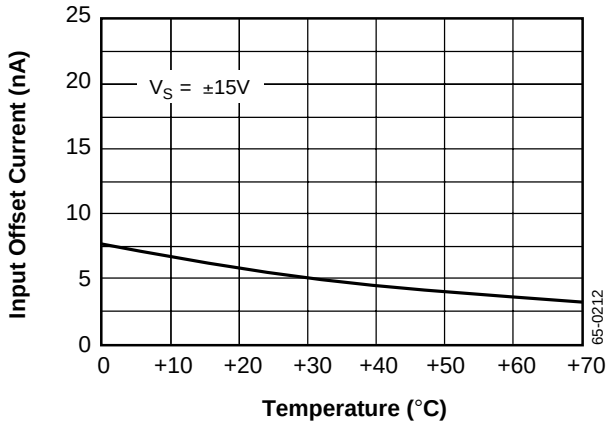
Parameters		Test Conditions	Min.	Typ.	Max.	Units
Input Offset Voltage		$R_S \le 10k\Omega$		2.0	6.0	mV
Input Offset Current				5.0	200	nA
Input Bias Current				50	500	nA
Input Resistance (Differential Mode)			0.3	0.1		MΩ
Large Signal Voltage Gain		$R_L \ge 2k\Omega$, V_{OUT} = ±10V	20	300		V/mV
Output Voltage Swing		$R_L \ge 10k\Omega$	±12	±14		V
		$I_O \ge 25mA$	±10	±11.5		
Input Voltage Range			±12	±13		V
Common Mode Rejection Ratio		$R_S \le 10k\Omega$	70	90		dB
Power Supply Rejection Ratio		$R_S \le 10k\Omega$	76	90		dB
Power Consumption		$R_L = \infty$		135	200	mW
Transient Response	Rise Time	V_{IN} = 20 mV, R_L = 2kΩ		0.05		µS
	Overshoot	$C_L \le 100pF$		35		%
Slew Rate		$R_L \le 2k\Omega$, Gain = 1		4.0		V/µS
Channel Separation		f = 10kHz R_S = 1kΩ, Gain = 100		100		dB
Unity Gain Bandwidth		A_V = +1, V_O = -3dB		10		MHz
The following specifications apply for -20°C ≤ T_A ≤ +75°C						
Input Offset Voltage		$R_S \le 10k\Omega$			7.0	mV
Input Offset Current					300	nA
Input Bias Current					800	nA
Large Signal Voltage Gain		$R_L \ge 2k\Omega$, V_{OUT} = ±10V	15			V/mV
Output Voltage Swing		$R_L \ge 2k\Omega$	±10			V
Power Consumption		T_A = +75°C		135	200	mW
		T_A = –20°C		165	230	

Typical Performance Characteristics

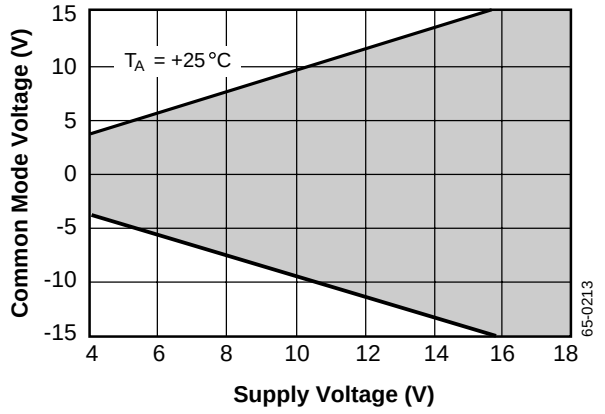
Input Bias Current vs. Ambient Temperature



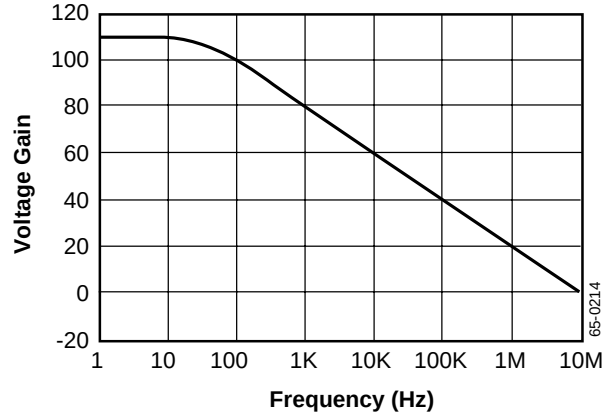
Input Offset Current vs. Ambient Temperature



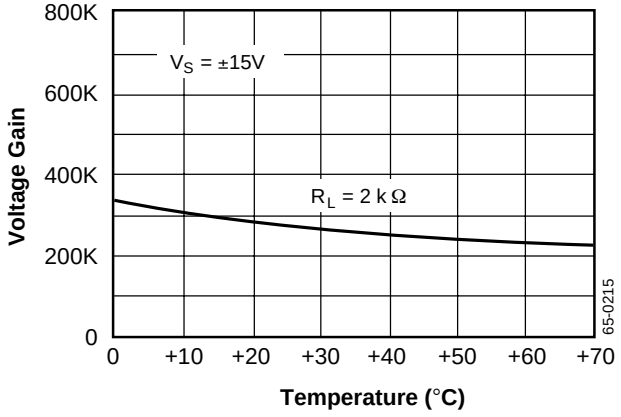
Common Mode Range vs. Supply Voltage



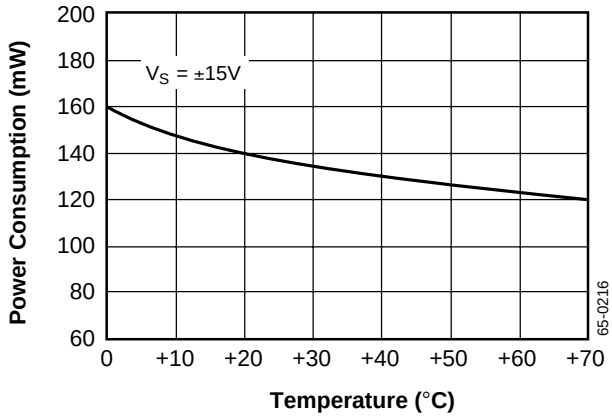
Open Loop Voltage Gain vs. Frequency



Open Loop Gain vs. Temperature

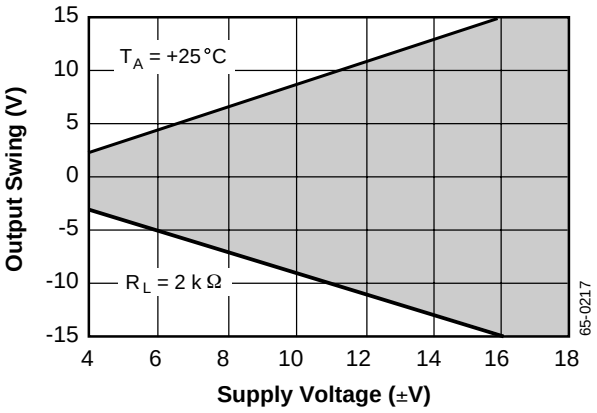


Power Consumption vs. Ambient Temperature

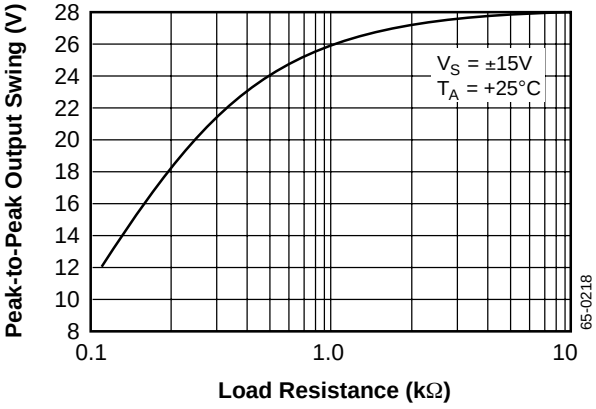


Typical Performance Characteristics (continued)

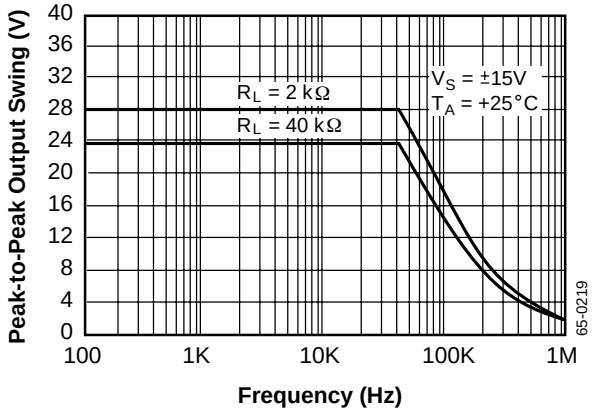
Typical Output Voltage vs. Supply Voltage



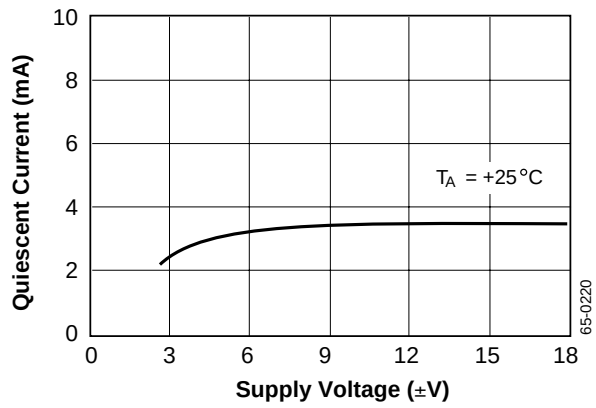
Output Voltage Swing vs. Load Resistance



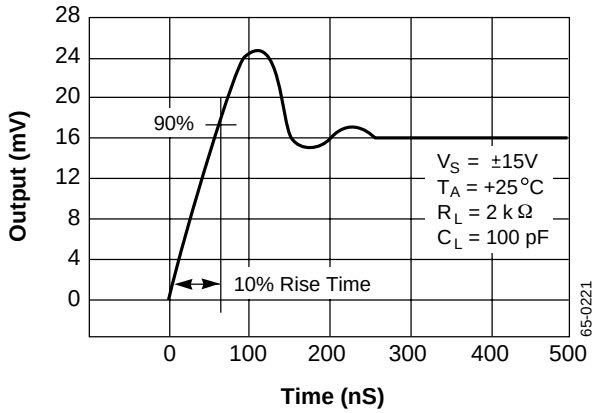
Output Voltage vs. Frequency



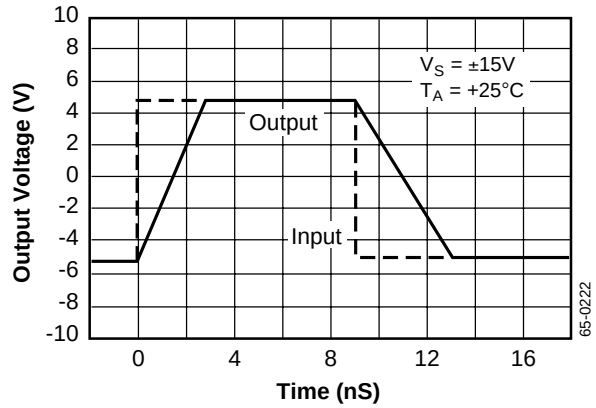
Quiescent Current vs. Supply Voltage



Transient Response

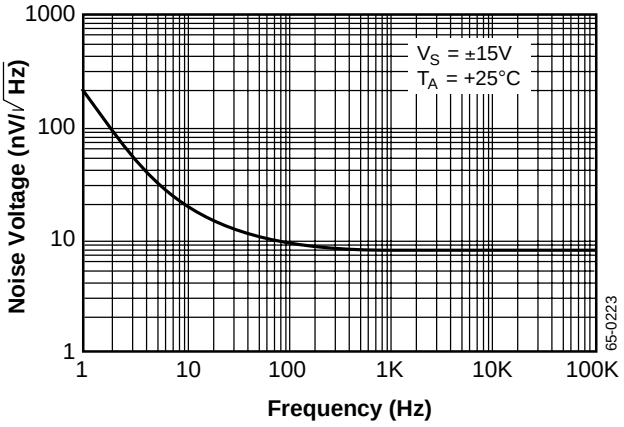


Voltage Follower Large Signal Pulse Response

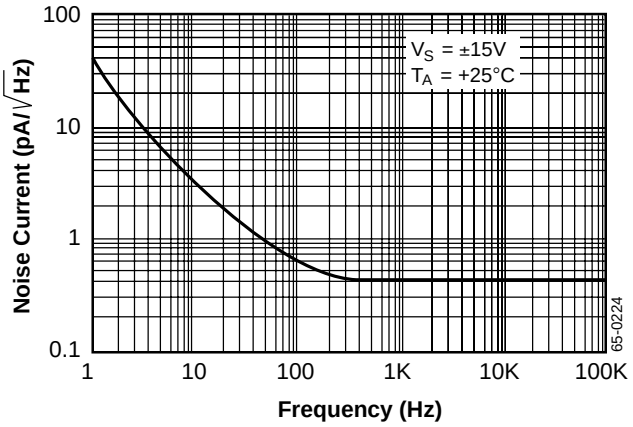


Typical Performance Characteristics (continued)

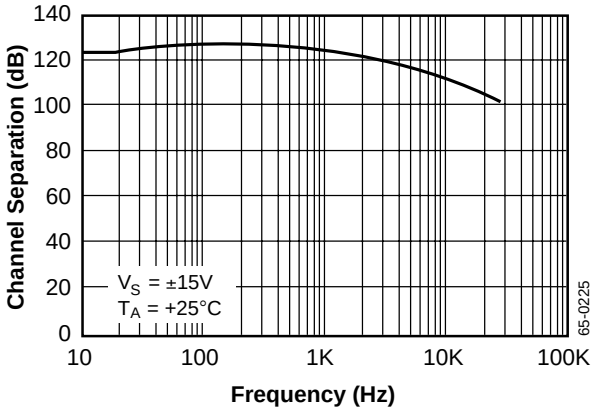
Input Noise Voltage vs. Frequency



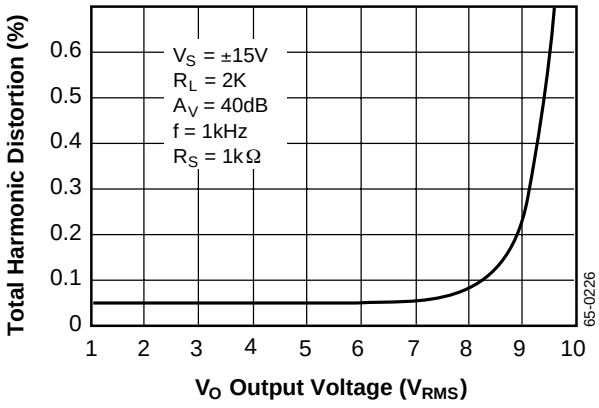
Input Noise Current vs. of Frequency



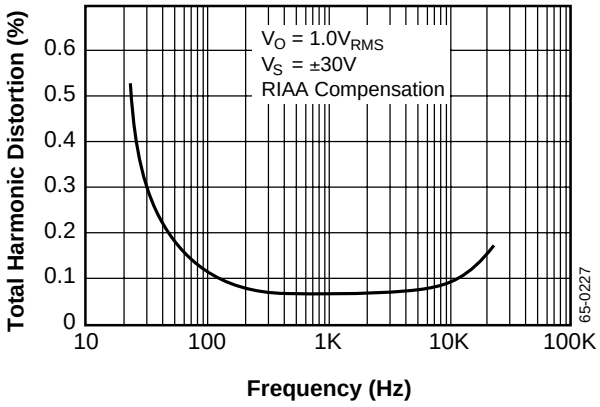
Channel Separation



Total Harmonic Distortion vs. Output Voltage



Distortion vs. Frequency



Notes

Notes

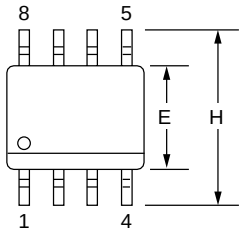
Notes

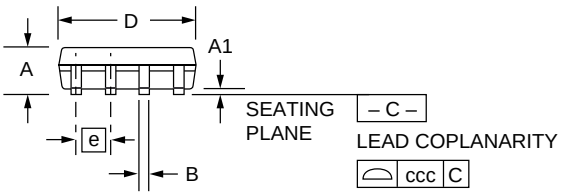
Mechanical Dimensions

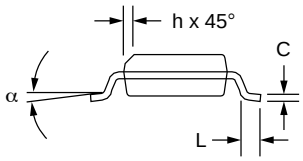
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.20	0.25	5
D	.189	.197	4.80	5.00	2
E	.150	.158	3.81	4.01	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	8		8		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







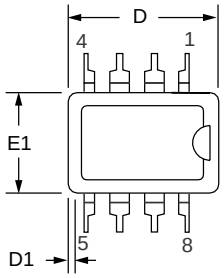
Mechanical Dimensions

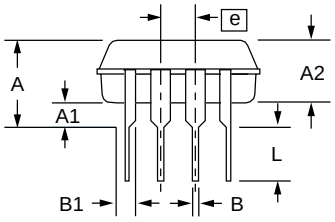
8-Lead Plastic DIP Package

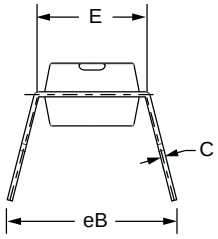
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	.348	.430	8.84	10.92	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.160	2.92	4.06	
N	8°		8°		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.







Ordering Information

Product Number	Temperature Range	Package
RC4560M	-20° to +75°C	8-Lead SOIC
RC4560N	-20° to +75°C	8-Lead Plastic DIP

5/20/98 0.0m 001
Stock#DS30004560

RC4741

General Purpose Operation Amplifier

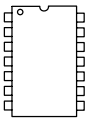
Features

- Unity gain bandwidth — 3.5 MHz
- High slew rate — 1.6 V/μS
- Low noise voltage — 9 nV/$\sqrt{Hz}$
- Input offset voltage — 0.5 mV
- Input bias current — 60 nA
- Indefinite short circuit protection
- No crossover distortion
- Internal compensation
- Wide power supply range — ±2V to ±20V

Applications

- Universal active filters
- Audio amplifiers
- Battery powered equipment

Package



14 pin DIP

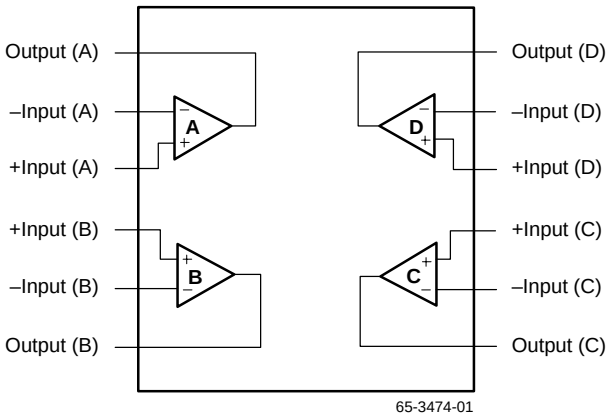
Description

The RC4741 is a monolithic integrated circuit, consisting of four independent operational amplifiers constructed with the planar epitaxial process.

These amplifiers feature AC and DC performance which exceed that of the 741 type amplifiers. Its superior bandwidth, slew rate and noise characteristics make it an excellent choice for active filter or audio amplifier applications.

A wide range of supply voltages (±2V to ±20V) can be used to power the RC4741, making it compatible with almost any system including battery powered equipment.

Block Diagram



65-3474-01

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min	Typ	Max	Units
Supply Voltage				±20	V
Input Voltage[2]				±15	V
Differential Input Voltage				30	V
$P_D T_A$ < 50°C	PDIP			468	mW
	CerDIP			1042	
	SOIC			300	
Output Short Circuit Duration[3]		Indefinite			
Junction Temperature	PDIP, SOIC			125	°C
	CerDIP			175	
Storage Temperature		-65		150	°C
Operating Temperature	RM4741	-55		125	°C
	RC4741	0		70	
Lead Soldering Temperature	60 sec, DIP			300	°C
	10 sec, SOIC			260	

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit to ground on one amplifier only.

Operating Conditions

Parameter			Min	Typ	Max	Units
θ_{JC}	Thermal resistance	CerDIP		60		°C/W
θ_{JA}	Thermal resistance	PDIP		160		°C/W
		CerDIP		120		
		SOIC		200		
For T_A > 50°C Derate at		PDIP		6.25		mW/°C
		CerDIP		8.38		
		SOIC		5.0		

Electrical Characteristics

(V_S = ±15V and T_A = 25°C unless otherwise specified)

Parameters	Test Conditions	RM4741			RC4741			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	R_S ≤10kΩ		0.5	3.0		1.0	5.0	mV
Input Offset Current			15	30		30	50	nA
Input Bias Current			60	200		60	300	nA
Input Resistance			0.5			0.5		MΩ
Large Signal Voltage Gain	R_L ≥ 2kΩ, V_{OUT} ±10V	50	100		25	50		V/mV
Input Voltage Range		±12			±12			V
Output Resistance			300			300		Ω
Output Current	V_{OUT} ±10V	±5	±15		±5	±15		mA
Common Mode	R_S ≤10kΩ	80			80			dB
Rejection Ratio	ΔV = ±5							
Supply Current (All Amplifiers)			4.5	5.0		5.0	7.0	mA
Transient Response	Rise Time		75			75		nS
	Overshoot		25			25		%
	Slew Rate		1.6			1.6		V/μS
Unity Gain Bandwidth			3.5			3.5		MHz
Power Bandwidth	V_{OUT} = 20V_{p-p}, R_L = 2k		25			25		kHz
Input Noise Voltage Density	F = 1kHz		9.0			9.0		nV/$\sqrt{Hz}$
Channel Separation			108			108		dB

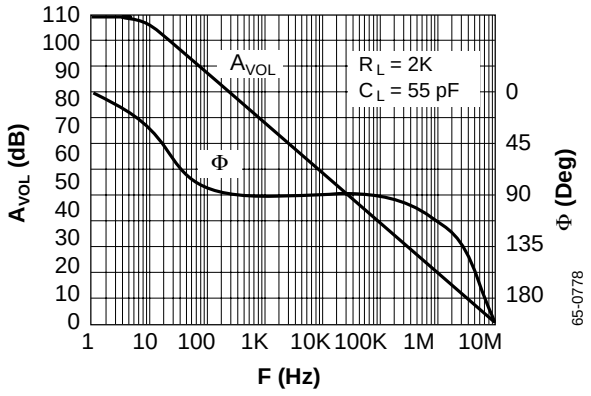
Electrical Characteristics

(V_S = ±15V, RM = -55° C ≤T_A ≤ +125° C, R_C = 0°C ≤ T_A + 70°C)

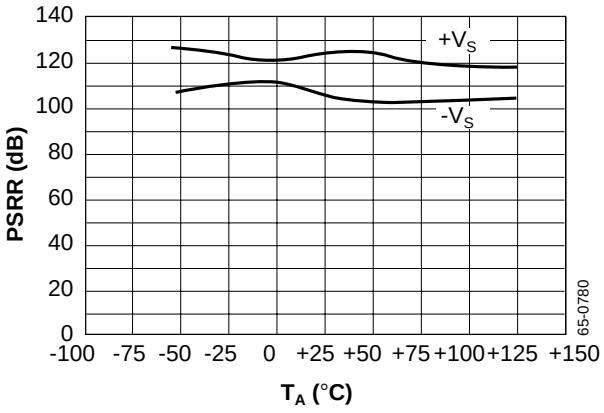
Parameters	Test Conditions	RM4741			RC4741			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	R_S ≤ 10kΩ		4.0	5.0		5.0	6.5	mV
Input Offset Current				75			100	nA
Input Bias Current				325			400	nA
Large Signal	R_L ≥ 2kΩ	25			15			V/mV
Voltage Gain	V_{OUT} ±10V							
Output Voltage Swing	R_L ≥ 10kΩ	±12	±13.7		±12	±13.7		
	R_L ≥ 2kΩ	±10	±12.5		±10	±12.5		
Supply Current (All Amplifiers)			10			10		mA
Average Input Offset								
Voltage Drift			5.0			5.0		μV/°C
Common Mode Rejection Ratio	R_S ≤ 10kΩ, ΔV ± 5.0V	74			74			dB
Power Supply Rejection Ratio	R_S ≤ 10kΩ, ΔV ± 5.0V	80			80			dB

Typical Performance Characteristics

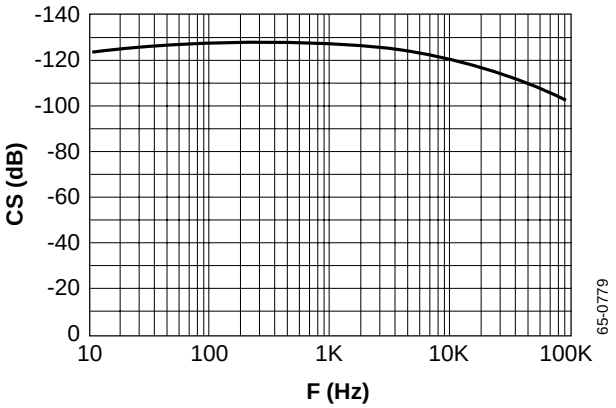
Open Loop Gain, Phase vs. Frequency

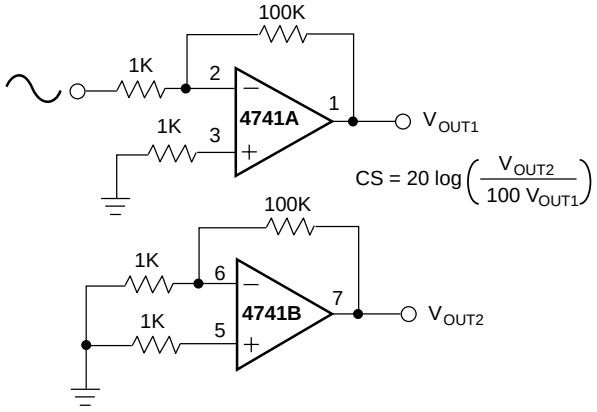


PSRR vs. Temperature

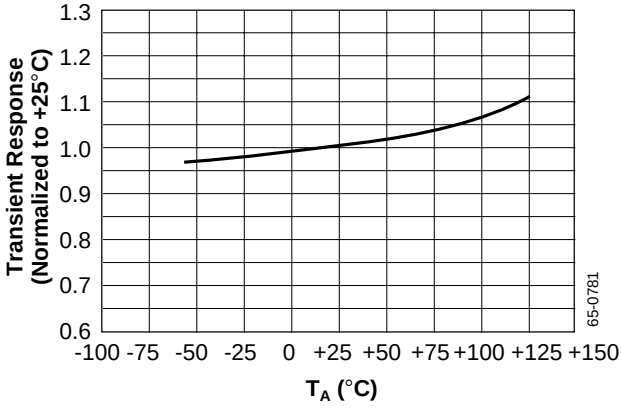


Channel Separation vs. Frequency

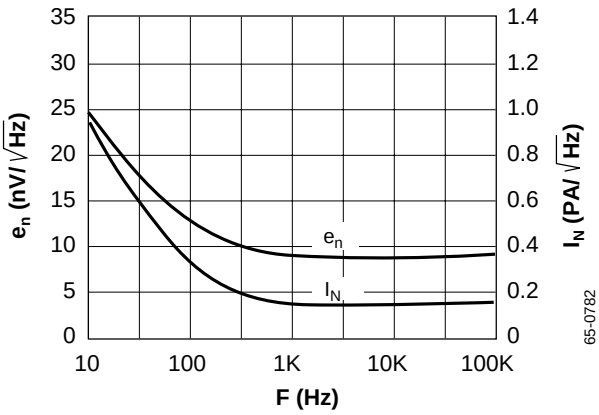




Transient Response vs. Temperature



Input Noise Voltage vs. Frequency



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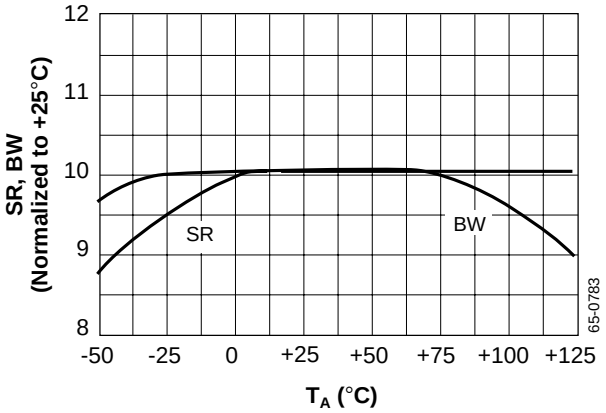
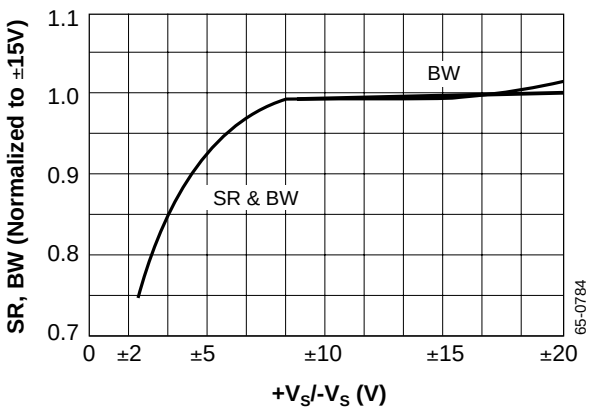
Typical Performance Characteristics (continued)

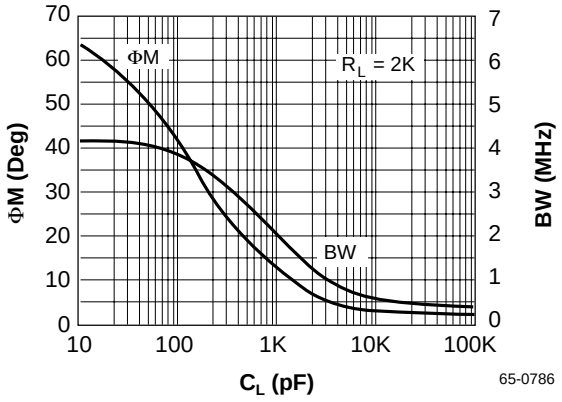
Slew Rate, Bandwidth vs. Temperature



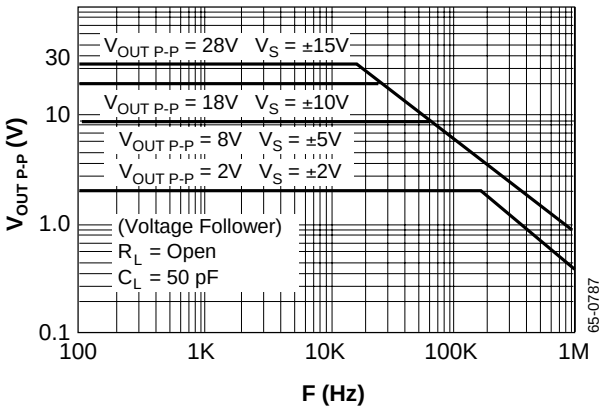
Slew Rate, Bandwidth vs. Supply Voltage



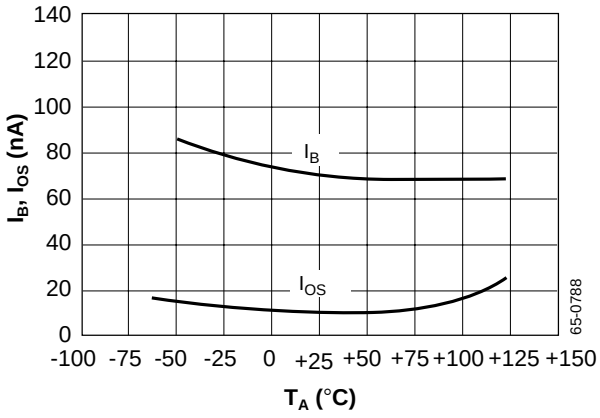
Small Signal Phase Margin, Unity Gain Bandwidth vs. Load Capacitance



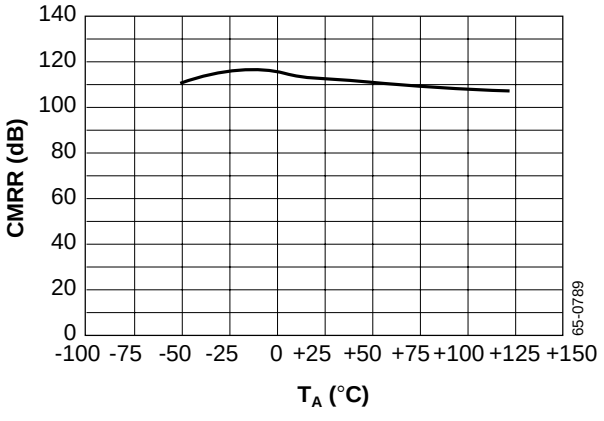
Output Voltage Swing vs. Frequency



Input Bias, Offset Current vs. Temperature



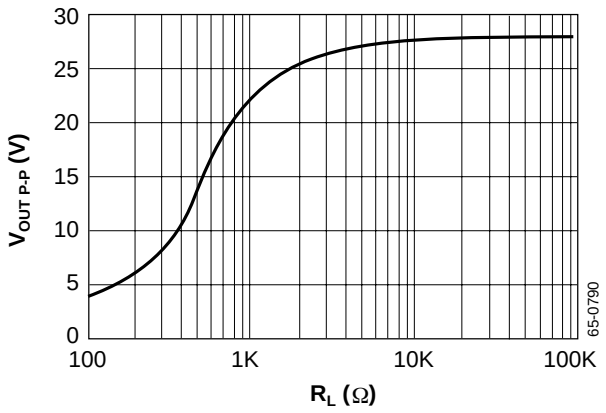
CMRR vs. Temperature



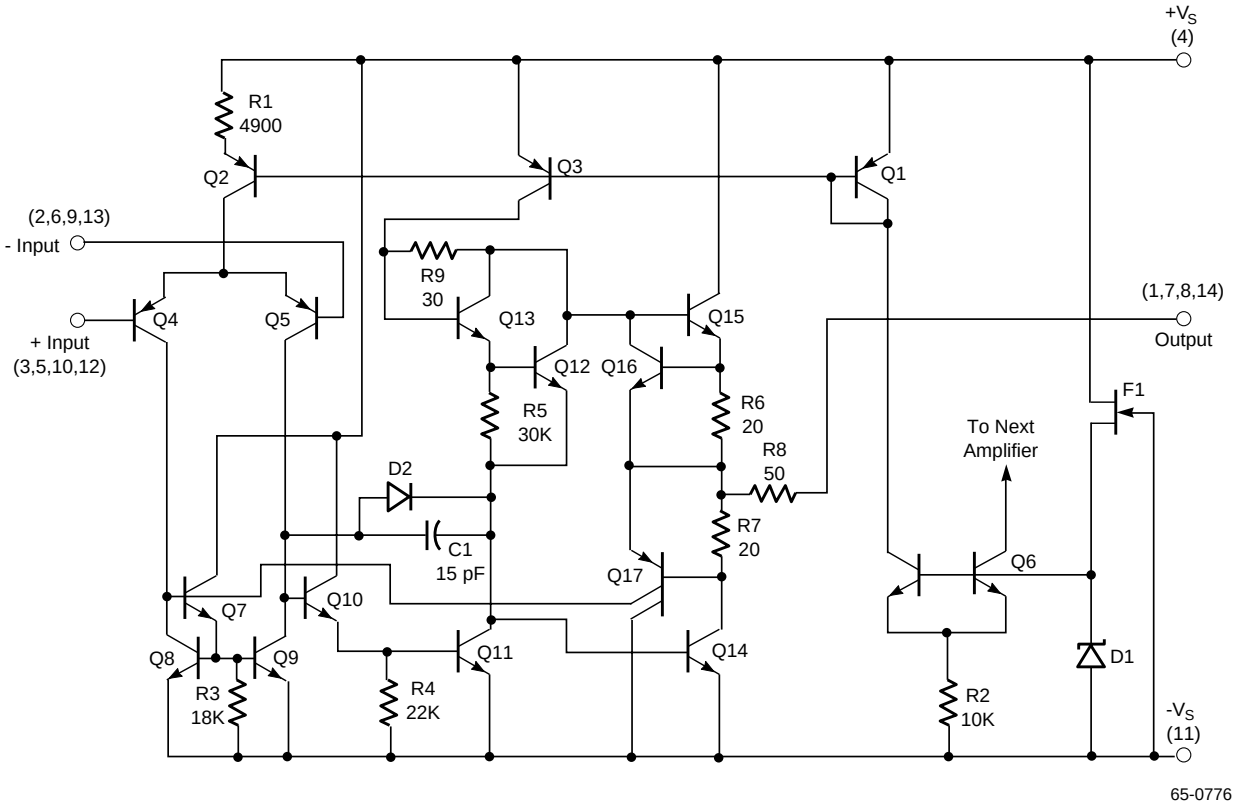
65-3474-03

Typical Performance Characteristics (continued)

Output Voltage Swing vs. Frequency



Schematic Diagram (1/4 shown)



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
RC4741M	0°C to +70°C	Commercial	14 pin Small Outline IC	
RC4741N	0°C to +70°C		14 pin Plastic DIP	
RM4741D	-55°C to +125°C		14 pin Ceramic DIP	
RM 4741D/883B	-55°C to +125°C	Military	14 pin Ceramic DIP	

Note: /883B suffix denotes Mil-Std-883, Level B processing.

7/24/98 0.0m 002
Stock#DS30004741

RC4861

1/2W Audio Power Amplifier with Shutdown

Features

- Low VOS, typically 2mV
- THD 0.3% typically at 0.5W output power
- Drives 8Ω and 4Ω non-powered speakers
- User programmable gain
- Internal thermal limiting circuitry
- 8 pin SOIC package

Applications

- Multimedia PC motherboards and add-in sound cards
- Companion chip to sigma-delta sound codecs
- Low power portable systems
- Toys and games
- Cellular phones

Description

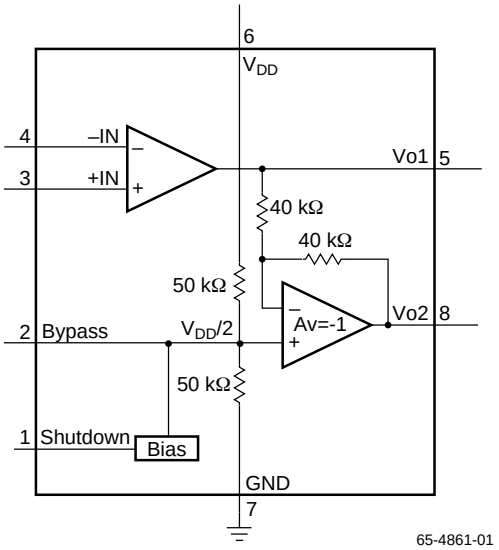
The RC4861 sound driver is an audio device that can be used on PC motherboards and add-in sound cards. It consists of H-bridge connected output drivers for headphones or speakers.

The output drivers can deliver up to 0.5 Watt of continuous average output power into 8Ω speaker from a 5V source. The drivers use class AB amplifiers and maintain a low bias current. A shut down function disables the device for power savings when not in use.

The thermal limiting circuitry becomes active if the chip temperature exceeds 150°C.

Preliminary Information

Block Diagram



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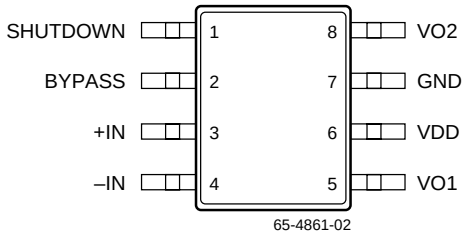
Pin Assignments



Absolute Maximum Ratings

Supply Voltage, V_{DD}	6.0V
Junction Temperature, T_J	150°C
Storage Temperature, T_S	–65 to +150°C
Lead Soldering Temperature, 10 seconds	300°C
ESD Threshold, ESD (Human Body Model)	2000V

Note:

1. Functional operation under any of these conditions is not implied. Performance is guaranteed only if Operating Conditions are not exceeded

Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Power Supply, V_{DD}		2.7	5.0	5.5	V
Input Voltage Logic High, V_{IH}		V_{DD}–0.8		V_{DD}	V
Input Voltage Logic Low, V_{IL}				0.8	V
Ambient Operating Temperature, T_A		0		70	°C

Preliminary Information

Electrical Characteristics

V_{DD} = 5V, f = 1kHz, R_L = 8Ω, unless otherwise specified.

Parameter		Conditions	Min.	Typ.	Max.	Units
A_V	Voltage Gain, Open Loop			90		dB
I_{SS}	Shutdown current	Shutdown pin HIGH, V_{DD} = 5V		0.6	10	μA
I_{total}	Power Supply Current,	No load		6.5	10	mA
V_{OS}	Output Offset Voltage	V_{IN} = 0V		2	20	mV
P_O	RMS Output Power	R_L = 8Ω, V_{DD} = 5V	0.5			W
THD	Total Harmonic Distortion	f_O = 1kHz, P_O = 0.5W		0.3	1	%
PSRR	Power Supply Rejection Ratio Input Referenced	f_O = 1kHz, ΔV_{DD} = 0.2Vp-p 0.1 μF bypass cap	65	75		dB

Typical Application Circuit

(Demo board is available for circuit in Figure 1).

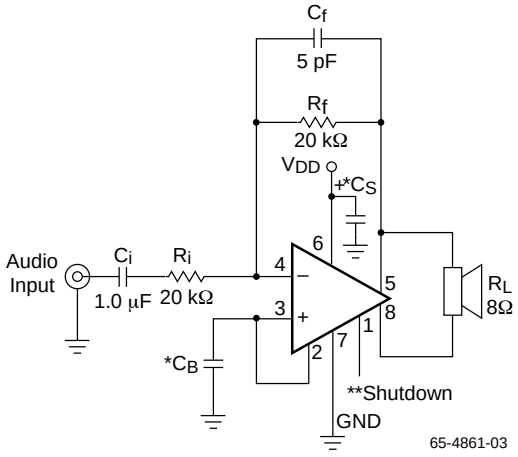


Figure 1. Audio Amplifier with A_{VD} = 2

* C_S and C_B size depend on specific application requirements and constraints. Typical values of C_S and C_B are 0.1 μF

**Pin 1 should be connected to V_{DD} to disable the amplifier or to GND to enable the amplifier. This pin should not be left floating.

Preliminary Information

Single Ended Application Circuit

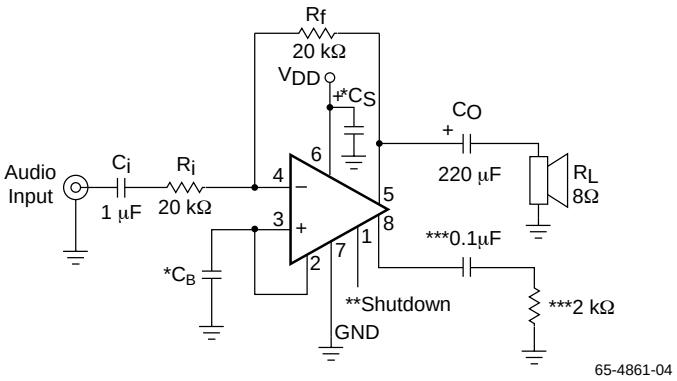


Figure 2. Single Ended Amplifier with A_V= –1

* C_S and C_B size depend on specific application requirements and constraints. Typical values of C_S and C_B are 0.1 μF
**Pin 1 should be connected to V_{DD} to disable the amplifier or to GND to enable the amplifier. This pin should not be left floating.
***These components create a “dummy” load for pin 8 for stability purposes.

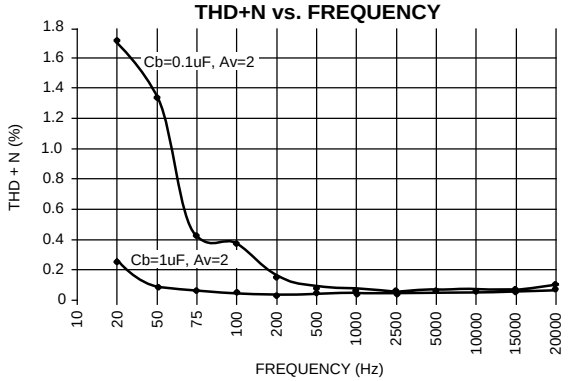
External Components Description (for Figure 1)

Components	Functional Description
R_i	Inverting input resistance which sets the closed-loop gain in conjunction with R_f . This resistor also forms a high pass filter with C_i at $f_C = 1/(2\pi R_i C_i)$.
C_i	Input coupling capacitor which blocks DC voltage at the amplifier's input terminals. Also creates a highpass filter with R_i at $f_C = 1/(2\pi R_i C_i)$.
R_f	Feedback resistance which sets closed-loop gain in conjuncticn with R_i. Av = -R_f/R_i
C_S	Supply bypass capacitor which provides power supply filtering.
C_B	Bypass pin capacitor which provides half supply filtering.
C_f	Used when a differential gain of over 10 is desired. C_f in conjunction with R_f creates a low-pass filter which bandwidth limits the amplifier and prevents high frequency oscillation bursts. $f_C = 1/(2\pi R_f C_f)$

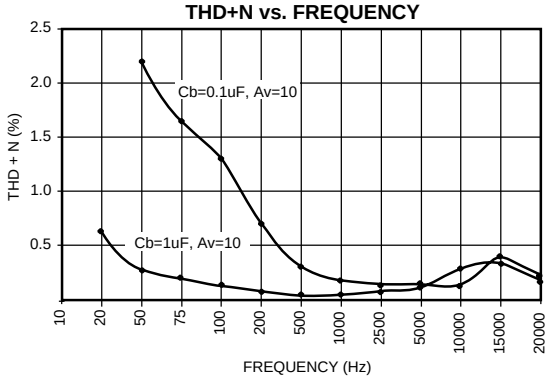
Preliminary Information

Typical Performance Characteristics

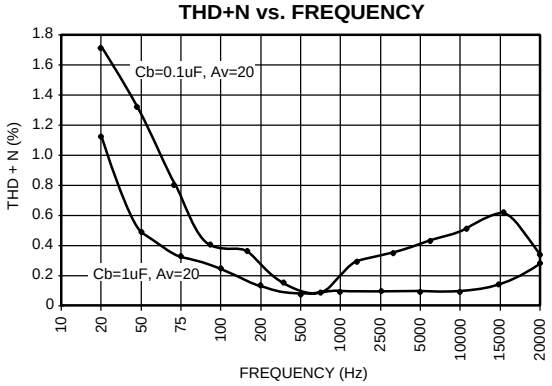
THD+N vs. FREQUENCY



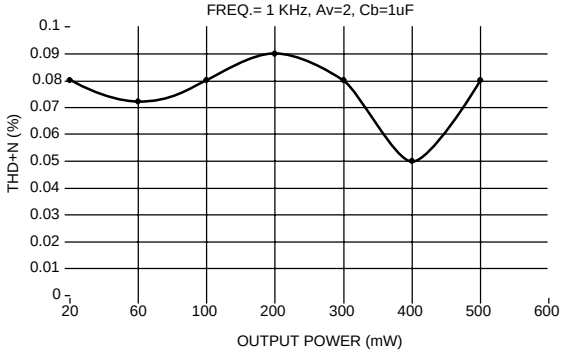
THD+N vs. FREQUENCY



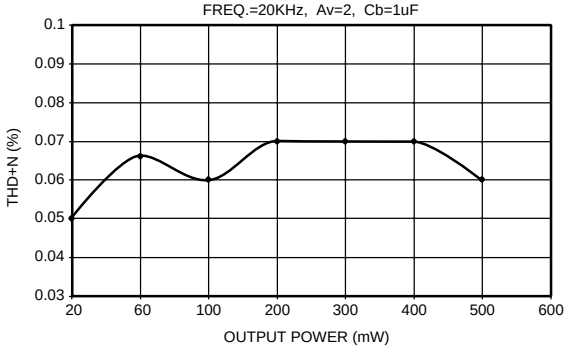
THD+N vs. FREQUENCY



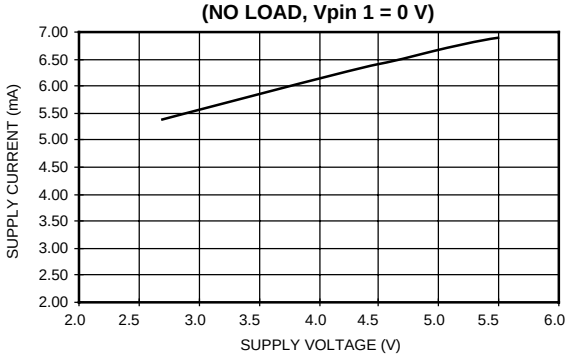
THD+N vs. OUTPUT POWER
FREQ.= 1 KHz, Av=2, Cb=1uF



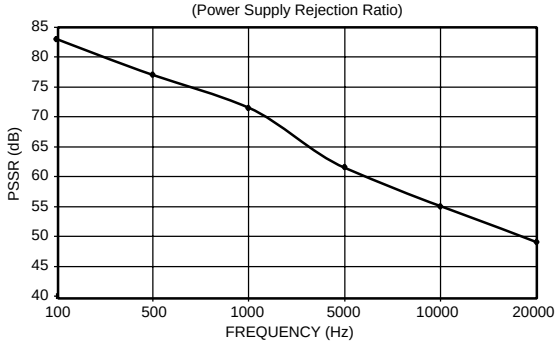
THD+N vs. OUTPUT POWER
FREQ.=20KHz, Av=2, Cb=1uF



SUPPLY CURRENT vs. SUPPLY VOLTAGE
(NO LOAD, Vpin 1 = 0 V)



PSRR vs. FREQ.
(Power Supply Rejection Ratio)



Preliminary Information

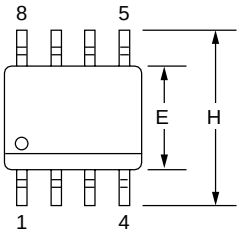
Notes:

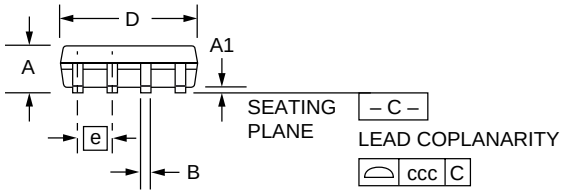
Mechanical Dimensions – 8-Lead SOIC Package

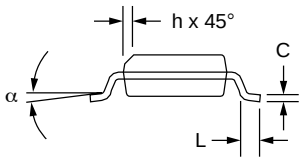
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.20	0.25	5
D	.189	.197	4.80	5.00	2
E	.150	.158	3.81	4.01	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	8		8		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Preliminary Information

Ordering Information

Product Number	Package
RC4861M	8 pin SOIC

Preliminary Information

LIFE SUPPORT POLICY

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RC5011

Step-up Regulator for Notebook Computers

Features

- Combines 5V precision linear regulator and boost-mode DC-DC converter
- High efficiency – 85% typical
- 6V to 22V input range (30V peak)
- Independent output enable control
- 10μA shutdown current
- Operates with companion RC5023 to form complete notebook computer power supply
- 8 pin SOIC package

Applications

- Complete notebook PC power supply when combined with RC5023 triple output DC-DC converter
- Sub-notebooks and PDAs
- PCMCIA and LCD panels

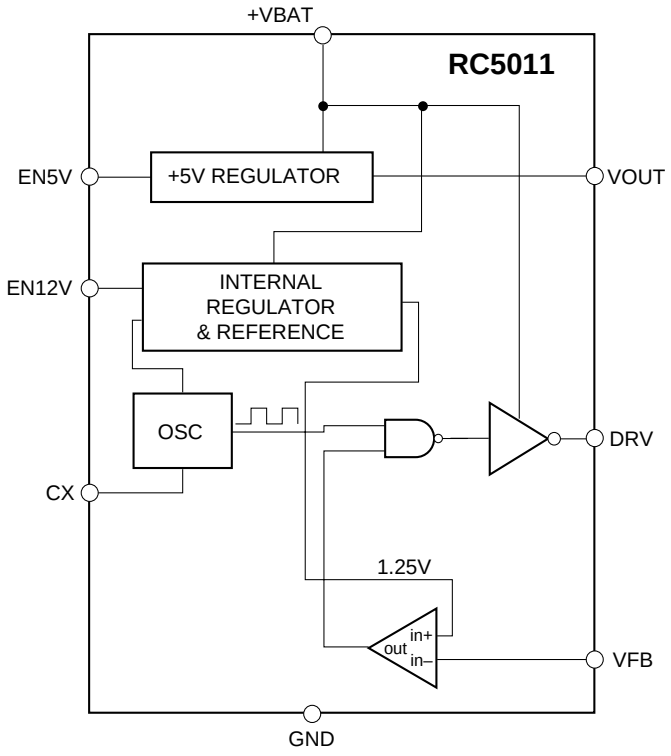
Description

The RC5011 is a combination 5V precision linear regulator and switch-mode boost converter suitable for use in notebook PC power supplies. The 5V regulator can drive loads in excess of 40mA, while the boost converter can be used to provide 12V for Flash BIOS or PCMCIA requirements.

Operating over a 6V to 22V (30V peak) input range, the RC5011 can be used as a standalone IC acheiving switch mode efficiencies of up to 85%. The RC5011 can also be used with the Fairchild Semiconductor RC5023 triple output DC-DC converter to generate the 5V, 3.3V, 12V and 2.xV required for typical Pentium® notebook computers. When used with the RC5023, the RC5011 acts as an input stage that provides 5V for the RC5023 Vcc as well as 12V for BIOS or PCMCIA. Using this scheme, system efficiencies of 88% can be realized for the entire 4-output solution.

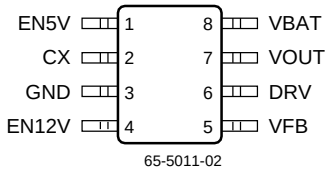
Advanced Information

Block Diagram



Rev. 0.5.1

Pin Assignments



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Pin Descriptions

Pin Number	Pin Name	Pin Function Description
1	EN5V	**5V output enable**. TTL-compatible input disables 5V linear regulator when set to logic LOW. Serves as system global enable/disable when used with RC5023 companion IC.
2	CX	**Oscillator timing capacitor**. Connecting an external capacitor to this pin sets the internal oscillator frequency.
3	GND	**Ground**. Connect this pin to system ground so that ground loops are avoided.
4	EN12V	**12V output enable**. TTL-compatible input disables the switch-mode converter when set to logic LOW.
5	VFB	**Voltage feedback**. Input for the voltage feedback control loop.
6	DRV	**FET Driver output for switch-mode converter**. Connect this pin to the gate of an N-channel MOSFET. The trace from this pin to the MOSFET gate should be as short as possible (<0.5").
7	VOUT	**5V linear regulator output**. Connect this pin to loads up to 40mA or to VCCL pin of RC5023 when used in the notebook computer power supply system.
8	VBAT	**Battery Supply Voltage**. Connect to system battery or other 6V to 30V source.

Absolute Maximum Ratings[1]

Supply Voltage, VBAT	32V
Power Dissipation, T_A < 50°C[2]	300mW
Storage Temperature	-65 to 150°C
Junction Temperature	125°C
Lead Soldering Temperature, 10 seconds	300°C

Notes:

1. Functional operation under any of these conditions is not implied. Performance is guarenteed only if Operating Conditions are not exceeded.
2. For T_A > 50°C, derate at 4.2mW/°C.

Operating Conditions

Parameter	Min	Typ	Max	Units
Supply Voltage, VBAT	6		30	V
Input Logic HIGH	2			V
Input Logic LOW			0.8	V
Ambient Temp	0		70	°C

Advanced Information

Electrical Characteristics – Switch-mode Converter

V_{BAT} = 6V, Fosc = 50KHz, T_A = 0 to 70°C using circuit in Figure 1, unless otherwise noted.

Parameter	Conditions	Min.	Typ.	Max.	Units
Output Voltage	Set by external resistors	12		30	V
Output Driver Voltage Swing		4.5			V
Line Regulation	V_{BAT} = 6V to 22V		0.2	0.4	%
Load Regulation	I_L = 0 to 200mA		0.1	0.2	%
Output Ripple/Noise	I_L = 200mA, BW = 20MHz		100	250	mV
Reference Voltage	Internal Reference	1.19	1.25	1.37	V
Efficiency		80	85		%
Operating Frequency Range		1.0		75	KHz
Oscillator Frequency Precision			±10		%
Capacitor Charging Current		4.0	8.0		μA
Capacitor Threshold Voltage +			1.4		V
Capacitor Threshold Voltage –			0.5		V
Feedback Input Current	VFB = 1.25V		0.1		μA

Electrical Characteristics - Linear Regulator

V_{BAT} = 6V, T_A = 0 to 70°C using circuit in Figure 1, unless otherwise noted.

Parameter	Conditions	Min.	Typ.	Max.	Units
Output Setpoint Accuracy	No Load		±3		%
Line Regulation	V_{BAT} = 6V to 22V		+0.4	+0.8	%
Load Regulation	I_L = 0 to 40mA		-1.0	-2.5	%
Output Temperature Drift	I_L = 40mA		+100	+150	ppm/°C
Cumulative DC Accuracy[1]				±5	%
Output Drive Current				40	mA

Note:

1. Cumulative DC Accuracy includes Setpoint Accuracy, Line/Load Regulation and Temperature Drift.

Electrical Characteristics – Common

V_{BAT} = 6V, Fosc = 50KHz, T_A= 25°C using circuit in Figure 1, unless otherwise noted.

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Current	VBAT = 6 to 22V, No load VBAT = 6V, EN5V LOW VBAT = 6V, EN12V = LOW Vbat = 6V, EN5V = EN12V = LOW		1.5 0.8 0.5 0.5	2.5 1.5 1.5 1.5	mA mA mA μA

Advanced Information

Test Circuit

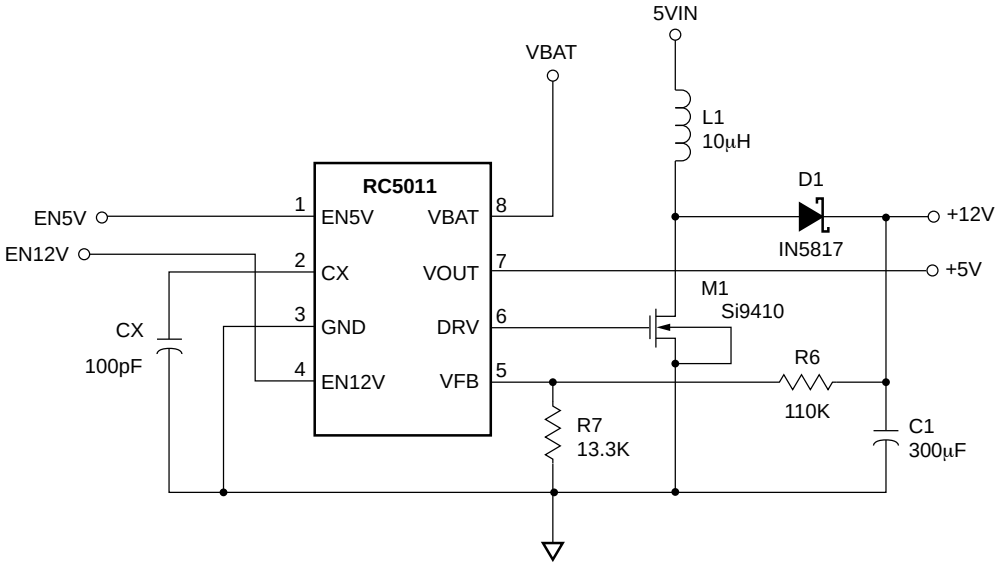

Figure 1. Standard Test Circuit Schematic

Application Information

Step-Up (Boost mode) Converter

A complete schematic of the minimum step-up converter application is shown in Figure 1. Upon application of power (V_{BAT}) and a logic high signal on the EN5V pin, the fixed 5V precision bandgap reference will become active and source up to 40mA of load current. If the 5V regulator is not needed, a logic low on the EN5V pin will disable the 5V regulator and reduce the supply current, thus minimizing power consumption. A 1μF capacitor connected from the 5V output to ground is recommended to reduce noise on the 5V output.

A logic high signal placed on the EN12V pin enables the switch mode regulator. Included in the switch-mode controller is a precision bandgap regulator that generates both a 1.25V reference and a 4V reference internally. The 4V reference is effectively "filtered " from the V_{BAT} supply to increase the power supply rejection of the IC, thus making it less susceptable to changes in the battery voltage and noise. The 1.25V reference is used for comparison against the divided down output voltage occuring at the voltage feedback (VFB) input.

A voltage supply connected to one side of the inductor as shown will cause the filter capacitor to instantaneously charge to V_{BAT} -V_F, where V_F is the forward voltage of the blocking diode. The voltage on the output capacitor C1 is also applied to resistor voltage divider R6 and R7, where the ratio of these resistors determines the final output voltage. The VFB node is connected to one side (-input) of a voltage comparator and the other side (+input) is connected to the 1.25V reference. If the voltage across C1 is less than the programmed value set by the ratio of R6 and R7, the output of the comparator will be at logic high.

One input of a NAND logic gate is connected to the comparator output, while the other NAND input is connected to the oscillator output. A logic high will allow the NAND output to respond to the oscillator input, thus allowing the totem-pole inverter to pulse the gate of the external N-channel MOSFET. The totem-pole inverter is referenced to V_{BAT} since this higher voltage will allow a higher gate drive and reduce the $R_{DS,ON}$ value of the MOSFET. When the FET is turned on, the inductor conducts current to ground through the FET. When the FET is turned off, diode D1 charges the output capacitor C1.

The VFB node will continuously monitor the output voltage and allow the oscillator to drive the MOSFET until the voltage at VFB surpasses the internal 1.25V reference voltage. At this time the output of the comparator switches to a logic low state, which forces the NAND output high. The totem-pole inverter will then transition low and turn off the MOSFET. Because the output voltage is now higher than V_{BAT}, the blocking diode prevents any further current flow into the output capcitor or the load. This condition will remain until the output voltage drops enough to lower the VFB node below 1.25V, at which time the process starts again. Using this system, the feedback network will vary the MOSFET duty cycle in response to changes in load current or battery voltage.

The inductor value and oscillator frequency must be carefully tailored to the battery voltage, output current, and ripple requirements of the application. If either the inductor value or the oscillator frequency is too high, the inductor current will never reach a value high enough to meet the load current drain and the output voltage will collapse. If the inductor value or the oscillator frequency is too low, the inductor current will become excessive, causing higher output voltage ripple, inductor core saturation, or MOSFET destruction due to over-stress.

Advanced Information

Design Equations

The inductor (L1) and timing capacitor (CX) values must be tailored to the input voltage range, output voltage, and load current requirements of the application. The key to the problem is to select the correct inductor value for a given oscillator frequency such that the inductor current rises to a peak value (Imax) sufficient to meet the average load current drain. The worst-case conditions for calculating its ability to supply load current are found at the minimum supply voltage. Therefore, $V_{BAT,MIN}$ is used to calculate the inductor value. Conversely, the worst-case condition for output voltage ripple will occur at $V_{BAT,MAX}$.

The value of the timing capacitor is set according to the following equation:

$F_O(Hz) = (5 \times 10^{-6})/Cx$

The output of the oscillator is measured at pin 2 (CX) and the voltage at the CX pin will be a triangle waveform. By pulling the VFB pin above 1.25V, the oscillator square wave output can be measured directly at pin 6 (DRV). Capacitor selection will depend on the specific application; higher operating frequencies will reduce the output voltage ripple and will allow the use of an inductor with a physically smaller inductor core, but excessively high frequencies will reduce load driving capability and efficiency.

Maximum on time of the MOSFET is calculated as follows:

$Ton = 1/2F_O + 0.5\mu S$

The 0.5µS term is added to represent the MOSFET gate-discharge time, although it is an approximation only and should be checked for the specific MOSFET used.

The peak inductor current is:

$$I_{MAX} = \left(\frac{V_{OUT} + V_F - V_{BAT}}{(F_O)T_{on}[V_{BAT} - V_{DS,ON}]}\right) 2I_{DC}$$

where:

V_{BAT} = supply voltage
V_F = diode forward voltage
I_{DC} = dc load current
$V_{DS,ON}$ = drain-source on voltage of MOSFET

Inductor value:

$$LX(Henries) = \left(\frac{V_{BAT} - V_{DS,ON}}{I_{MAX}}\right) T_{ON}$$

Output filter capacitor:

$$C1(\mu F) = \frac{T_{ON}\left(\frac{V_{BAT}I_{MAX}}{V_{OUT}} + I_{DC}\right)}{V_{RIPPLE}}$$

where V_{RIPPLE} = Peak output voltage ripple

To reduce system power consumption when the switch-mode section is not in use, the circuit shown in Figure 2 is recommended. This circuit prevents any load connected to V_{OUT} from drawing current out of V_{BAT}.

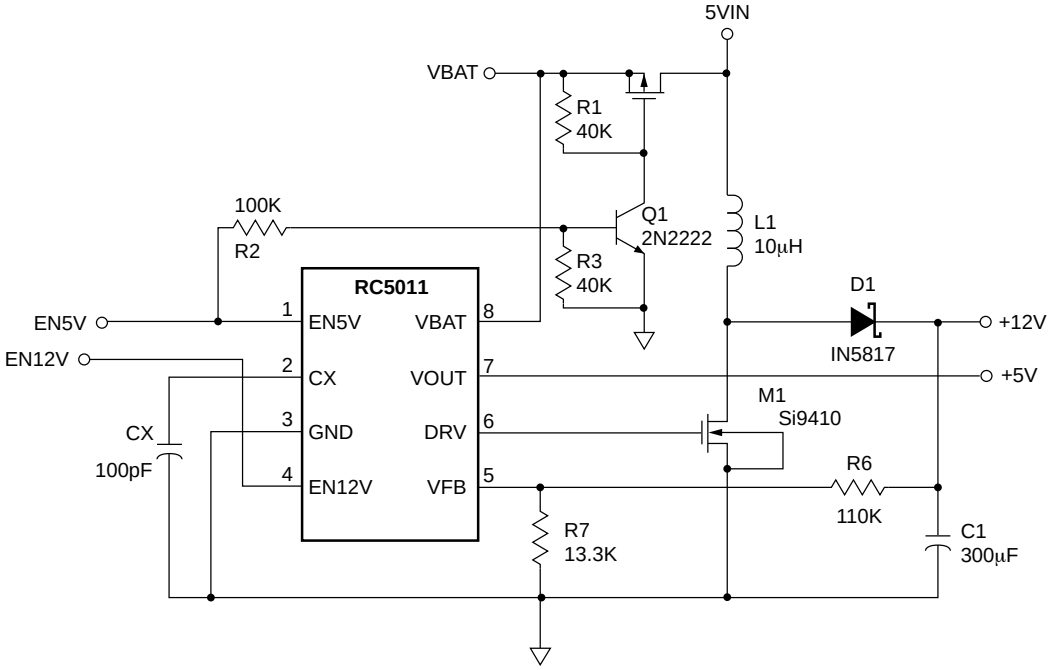

Figure 2. Standard Test Schematic with 12V Shutdown Circuit added

Advanced Information

Notebook Power Supply Application

RC5011/RC5023 System

The RC5011/RC5023 Portable Power Supply System is designed to cost-effectively address the notebook computer power supply requirements. The RC5011 generates the +12V power supply while also providing the startup 5V supply current for the RC5023. The RC5011 is designed on a high voltage technology which can support battery voltages as high as 32V. The 5V linear regulator from the RC5011 rejects the large potential battery voltage changes and provides a well-regulated +5V to power the RC5023. To optimize efficiency, the RC5023 utilizes an internal 5V switch to remove the +5V supply coming from the RC5011 and to then utilize the efficient +5V switcher output to supply the power for the digital logic, analog control circuitry, and output drivers of the RC5023.

The RC5023 has an internal comparator which senses the difference between the regulator 5V from the RC5011 and the output of the 5V switch-mode regulator. When the switch-mode regulator output exceeds 4.5V, the comparator commands the analog switch within the RC5023 to convert the +5V supply source from the RC5011 to the +5V switch-mode output. Thus, power is now drawn from the 88% efficient switch-mode regulator rather than the less efficient 5V linear regulator in the RC5011. The 5V linear regulator in the RC5011 remains connected to the RC5023 and continues to power both the bandgap reference as well as the 5Vswitch comparator; however the current consumption of these blocks is small and will not have a significant effect on the overall efficiency of the power supply system.

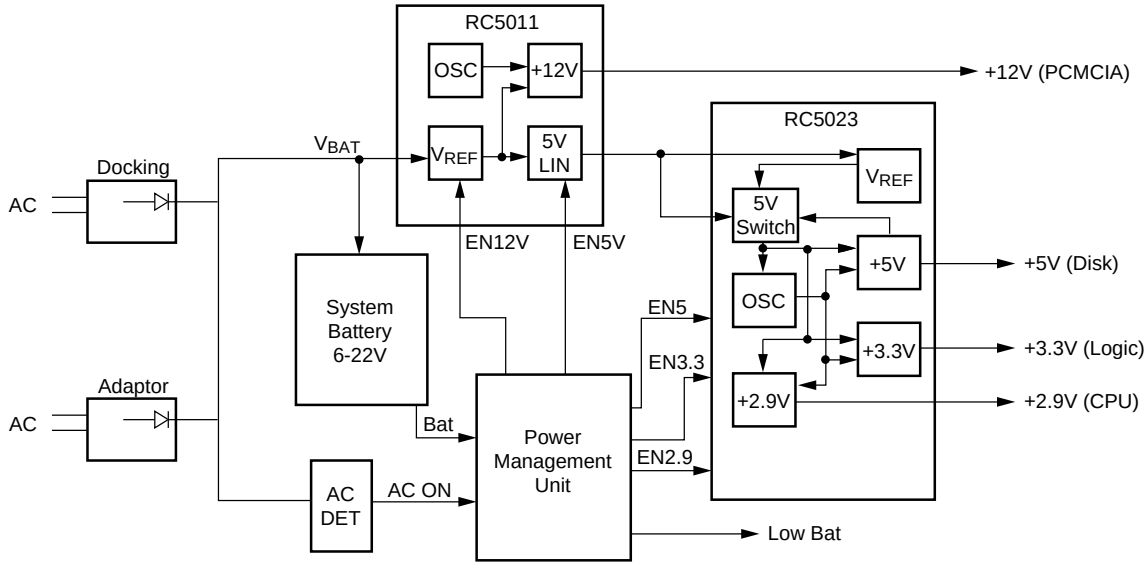

Figure 3. Notebook Computer Power Supply System using the RC5011 and RC5023

Advanced Information

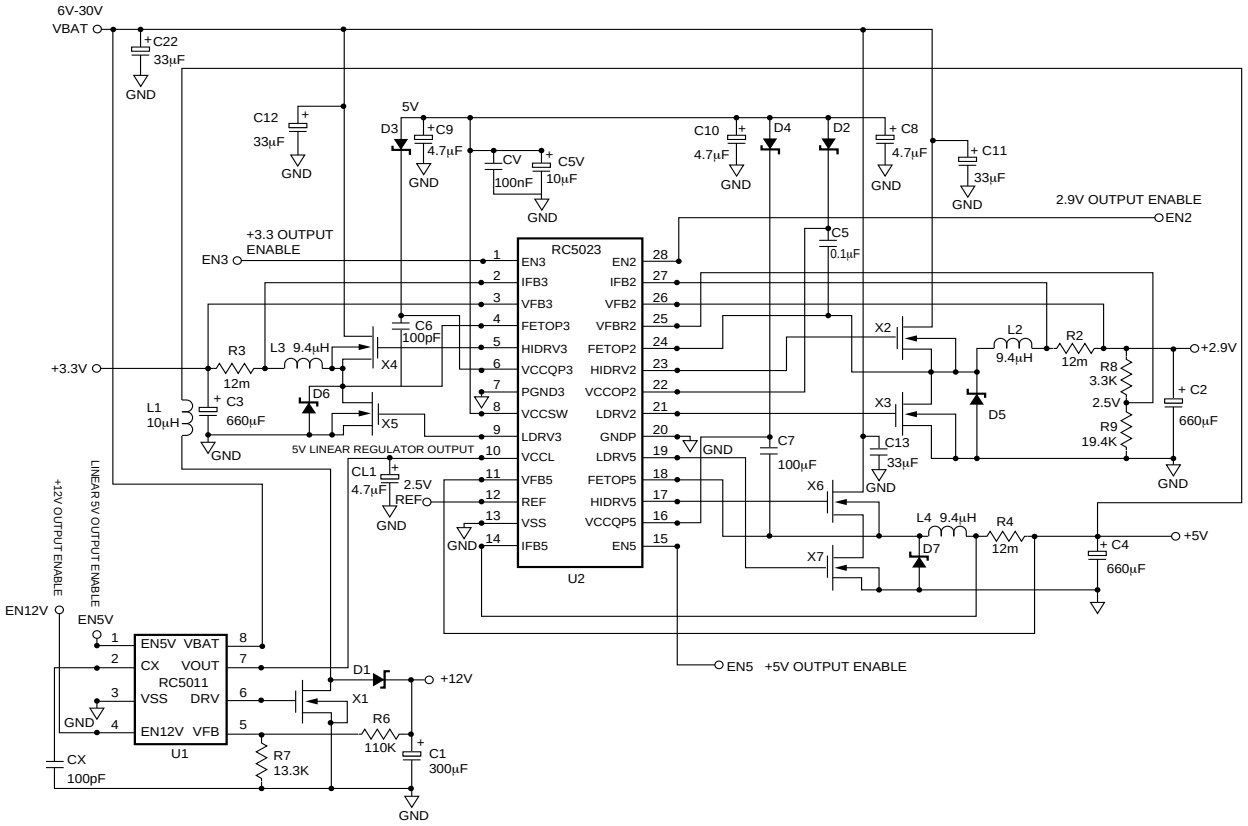

Figure 4.

RC5023/RC5011 Power Supply System Bill of Materials

Reference	Qty	Specification	Part No.	Manufacturer
L2-L4	3	9.4µH, 2.8A Inductors	PE-53631	Pulse Engineering
X2-X7, X1	7	N-channel MOSFETs	Si4410DY	Siliconix
D5-D7	3	3.3A, 20V SMT diodes	NSQ03A02L	Nihon
D2-D4, D1	4	1.1A, 20V SMT diodes	EC10QS02L	Nihon
R2-R4	3	1 watt 12m ohm, 1% resistors	LRC-2512	IRC
C2-C4	6	330µF, 10V tantalum capacitors	595D337X0010R2T	Sprague
C5-C7, CV	4	0.1µF, 16V ceramic capacitors	GRM40X7R104K025BL	Murata
C8-C10, CLI	4	4.7µF, 10V tantalum capacitors	NR Series	NEC
C11-C13, C22	4	33µF, 35V tantalum capacitors	595D336X0035R2T	Sprague
C5V	1	10µF, 10V tantalum capacitors	NR Series	NEC
R8	1	3.3K ohm, 0.1% resistor		Panasonic
R9	1	19.4K ohm, 0.1% resistor		Panasonic
RC5023	1	Triple-Output DC-DC Converter		Fairchild Semiconductor
L1	1	10µH, 2.65A inductor	CDRH125	Sumida
C1	2	100µF, 20V tantalum capacitor	595D107X0020R2T	Sprague
CX	1	100pF, 16V ceramic capacitor	GRM40C0G101J050BD	Murata
R6	1	110K ohm, 1% resistor		Panasonic
R7	1	133K ohm, 1% resistor		Panasonic
RC5011	1	12V Complement of RC5023		Fairchild Semiconductor

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Ordering Information

RC5011M	8 pin SOIC

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RC5011/RC5023 Demonstration Board

Power Supply Solution for Notebook Computers

Features

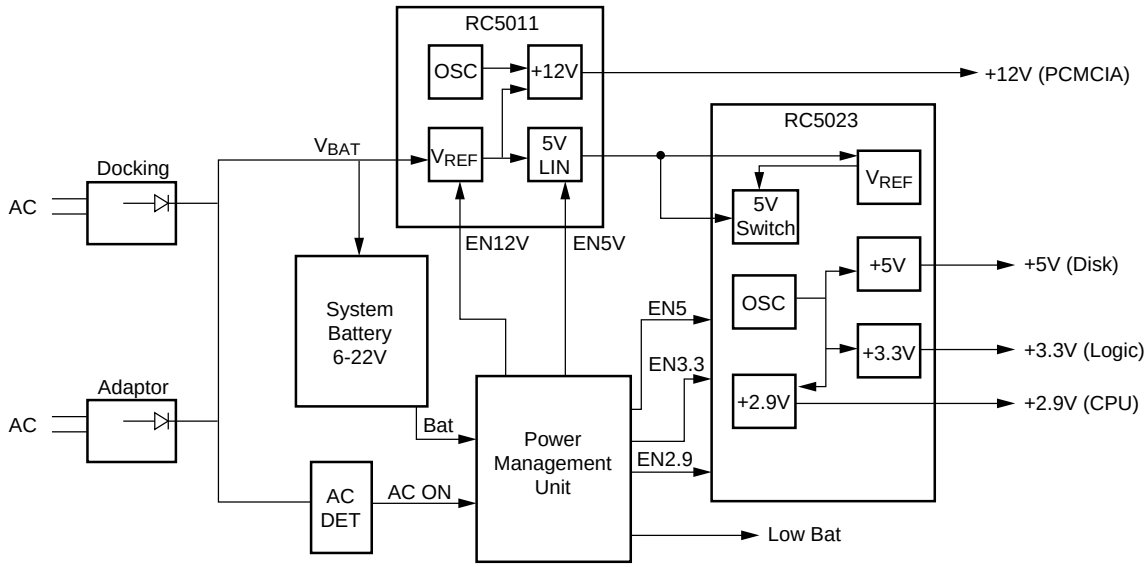
- Output voltages 5V, 12V, 3.3V and 2.9V
- >93% System efficency
- 6V to 30V operation
- Independent output enable/disable
- Global power-down for low power sleep mode

Description

The RC5011/RC5023 demonstration board is intended to assist designers in developing an efficient, low cost power system for notebook computers using the RC5011 and RC5023 voltage regulator ICs. The demo board accepts an input voltage from 6V to 30V for battery operation. Using both regulators, the demo board outputs four unique voltages required by most portable PC systems; 12V for flash bios, 5V for digital logic, 3.3V for RAM and other logic and 2.9V for the CPU. Using synchronous operation on all but the 12V output, the system can realize efficiencies in excess of 93% for extended battery life. Independent output enable functions as well as a global power-down allow for a multitude of low power sleep modes.

Advanced Information

Block Diagram



Jumper Settings

The board is fitted with several jumpers to enable each output as well as the entire power supply system. The jumper settings are presented in Table 1 and their locations are illustrated in Figure 2. Each jumper has three posts mounted perpendicular to the board. The middle post is connected to appropriate the IC control pin, with the outer two pins connected to VCC and GND, respectively. The output is disabled by connecting the jumper between the center post and VCC and is disabled by connecting it between the center post and GND. The absence of a jumper will disable the output.

Table 1. Jumper Settings for RC5011 + RC5023 Demonstration Board

Active Output	Jumper Designation	Jumper Position
2.9V	EN2	VCC
3.3V	EN3	VCC
5V	EN5	VCC
12V	EN12V EN5	VCC VCC

NOTE: Both the EN12V and the EN5 jumpers must be connected to Vcc in order to enable the 12V output.

Precautions

- Beware of ESD! It is recommended that this demonstration board be used only in an ESD-controlled location to reduce the risk of damage resulting from ESD-related stress.
- Use Kelvin connected test points. Voltage drops in the main current path can greatly reduce the observed efficiency characteristics of this demonstration board.
- Do not attempt to draw more than 200mA from the 12V output. Overloading this output will result in permanent damage to the RC5011.

Power-up Check List

1. Set up the jumpers as illustrated in Table 1, above.
2. Connect the positive power lead to the Vbat terminal.
3. Connect the positive lead of external 5V source to the single post between the EN12V jumper and the +3.3V OUT posts.
4. Connect the negative power lead to one pair of GND terminals (two pairs exist).
5. Connect the negative lead of the external 5V to a pair of GND terminals.
6. Connect loads to desired outputs. Returns from the loads may be connected to either pair of GND terminals.
7. Apply power and check for correct output voltages. If no output is observed, turn off power and check all connections again.

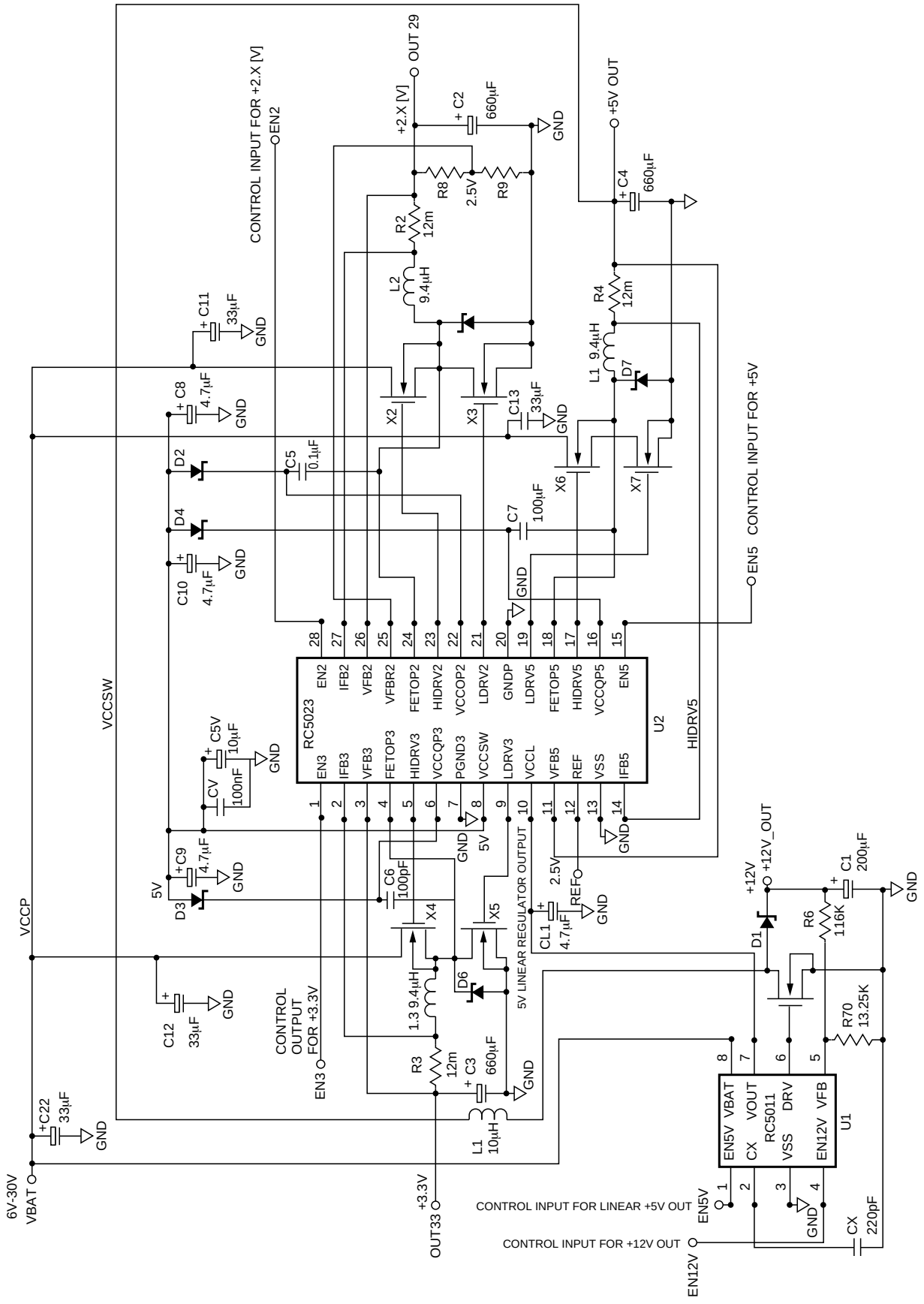


Figure 1. RC5011/5023 Demo Board Application Schematic

Advanced Information

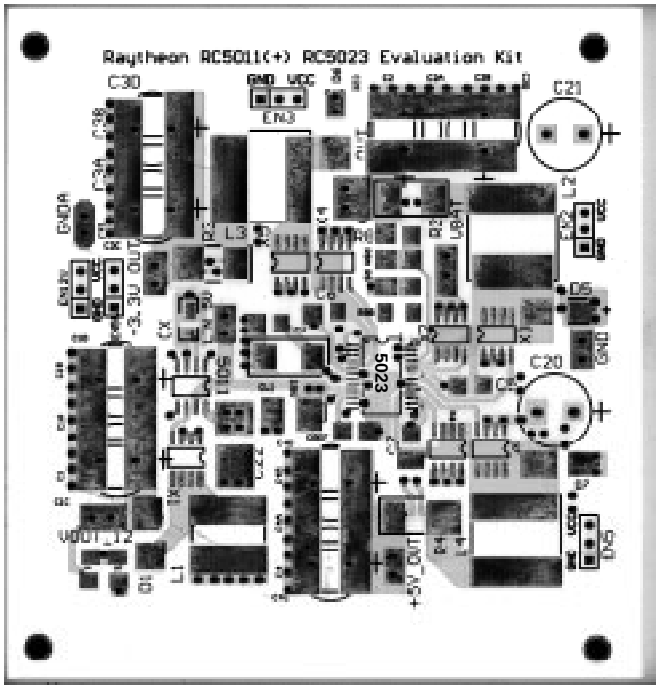


Figure 2. RC5011/RC5023 Demo Board Layout

Table 2. RC5011/5023 Demo Board Application Bill of Materials

Reference	Description	Part No.	Manufacturer	Qty
L2 – L4	9.4uH, 2.8A Inductors	PE-53631	Pulse Engineering	3
X2 – X7, X1	N-channel MOSFETs	Si4410DY	Siliconix	7
D5 – D7	3.3A, 20V SMT diodes	NSQ03A02L	Nihon	3
D1 – D4	1.1A, 20V SMT diodes	EC10QS02L	Nihon	4
R2 – R4	1 watt, 12mΩ, 1% resistors	LRC-2512	IRC	3
C2 – C4	330μF, 10V tantalum capacitors	595D337X0010R2T	Sprague	6
C5 – C7,CV	0.1μF, 16V ceramic capacitors	GRM40X7R104K025	muRata	4
C8 – C10,CLI	4.7μF, 10V tantalum capacitors	NR Series	NEC	4
C11– C13,C22	33μF, 35V tantalum capacitors	595D336X0035R2T	Sprague	4
C5V	10uF, 10V tantalum capacitor	NR Series	NEC	1
R8	20KΩ, 0.1% resistor		Panasonic	1
R9	100KΩ, 0.1% resistor		Panasonic	1
RC5023	Triple DC-DC controller IC		Fairchild Semiconductor	1
L1	10μH, 2.65A inductor	CDRH125	Sumida	1
C1	100μF, 20V tantalum capacitor	595D107X0020R2T	Sprague	2
CX	100pF, 16V ceramic capacitor	GRM40C0G101J050	muRata	1
R6	116KΩ, 1% resistor		Panasonic	1
R7	13.25KΩ, 1% resistor		Panasonic	1
RC5011	12V step-up controller IC		Fairchild Semiconductor	1

Additional Information

For technical assistance regarding this demonstration board, please contact Fairchild Semiconductor Applications department at (415) 966-7779. For additional product information, please contact Fairchild Semiconductor Marketing at (415) 962-7982. Individual product data sheets can also be obtained by calling Fairchild Semiconductor' automated RayFAX system at (415) 988-2123.

Notes:

Notes:

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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RC5031

Adjustable Switching Regulator

Features

- High power switched-mode DC-DC controller can source in excess of 13A
- Output voltage adjustable from 1.5V to 3.6V
- 85% efficiency
- Cumulative accuracy < 3% over line, load, temperature and transient variations
- Overvoltage and short circuit protection
- Built-in soft start

Applications

- Precision 2.xV CPU core regulator for Intel Pentium® MMX™ processors
- Precision 2.xV or 3.xV CPU core regulator for AMD-K6™ MMX and Cyrix 6x86MX™ (M2) processors

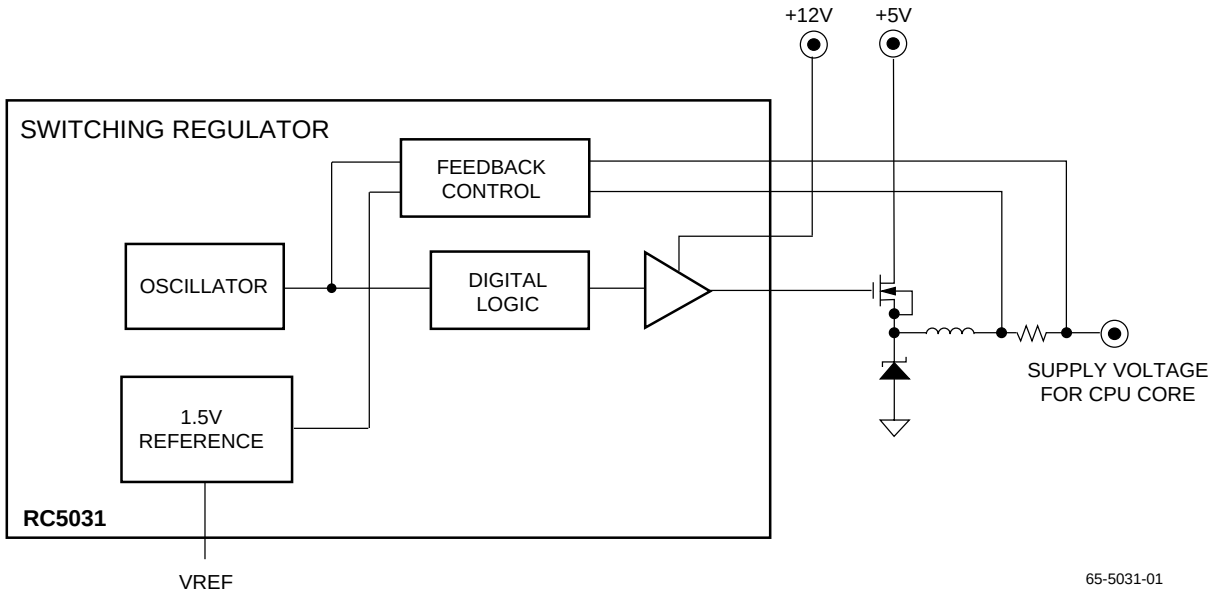
Description

The RC5031 is a high power, switch-mode DC-DC controller that provides an accurate, adjustable output for high-end microprocessors requiring unique supply voltages. The RC5031 has built-in Soft Start feature which offers system protection during power-up by reducing both inrush current and output overshoot. When combined with the appropriate external circuitry, the RC5031 can deliver load currents as high as 13A at efficiencies as high as 88%. Through the use of external resistors, the RC5031 can generate output voltages from 1.5V up to 3.6V.

The RC5031 is designed to operate in a “constant on-time” (patent pending) control mode under all load conditions. Its accurate low TC reference eliminates the need for precision external components in order to achieve the tight tolerance voltage regulation required by most CPU-based applications. Short circuit current protection is provided through the use of a current sense resistor, while overvoltage protection is provided internally.

The RC5031 is a highly efficient switched-mode DC-DC converter that can select a 3.5V or user-adjustable output. With the appropriate external components, the RC5031 can be configured to implement a switchable power supply system for Pentium and K6 processors.

Block Diagram



65-5031-01

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MMX is a trademark of Intel Corporation.
K6 is a trademark of AMD Corporation.
6x86MX is a trademark of Cyrix Corporation.

Functional Description

The RC5031 contains a precision trimmed zero TC voltage reference, a constant-on-time architecture controller, a high current switcher output driver, a low offset op-amp, and switches for selecting various output modes. The block diagram in Figure 1 shows how the RC5031 in combination with the external components achieves a switchable power supply.

Switch-Mode Control Loop

The main control loop for the switch-mode converter consists of a current conditioning amplifier and one of the two voltage conditioning amplifiers that take the raw voltage and current information from the regulator output, compare them against the precision reference and present the error signal to the input of the constant-on-time oscillator. The two voltage conditioning amplifiers act as an analog switch to select between the internal resistor divider network (set for 3.5V) or an external resistor divider network (adjustable for 1.5V to 3.6V.) The switch-mode select pin determines which of the two amplifiers is selected. The current feedback signals come across the Iout sense resistor to the IFBH and IFBL inputs of the RC5031. The error signals from both the current feedback loop and the voltage feedback loop are summed together and used to control the off-time duration of the oscillator. The current feedback error signal is also used as part of the RC5031 short-circuit protection.

High Current Output Drivers

The RC5031 switching high current output driver (SDRV) contains high speed bipolar power transistors configured in a push-pull configuration. The output driver is capable of supplying 0.5A of current in less than 100ns. The driver's power and ground are separated from the overall chip power and ground for added switching noise immunity.

Internal Reference

The reference in the RC5031 is a precision band-gap type reference. Its temperature coefficient is trimmed to provide a near zero TC. For guaranteed stable operation under all loading conditions, a 0.1µF capacitor is recommended on the VREF output pin.

Constant-On-Time Oscillator

The RC5031 switch-mode oscillator is designed as a fixed on-time, variable off-time oscillator. The constant-on-time oscillator consists of a comparator, an external capacitor, a fixed current source, a variable current source, and an analog switch that selects between two threshold voltages for the comparator. The external timing capacitor is alternately charged and discharged through the enabling and disabling of the fixed current source. The variable current source is controlled from the error inputs that are received from the current and voltage feedback signals. The oscillator off-time is controlled by the amount of current that is available from the variable current source to charge the external capacitor up to the high threshold level of the comparator. The on-time is set be the constant current source that discharges the external capacitor voltage down to the lower comparator threshold.

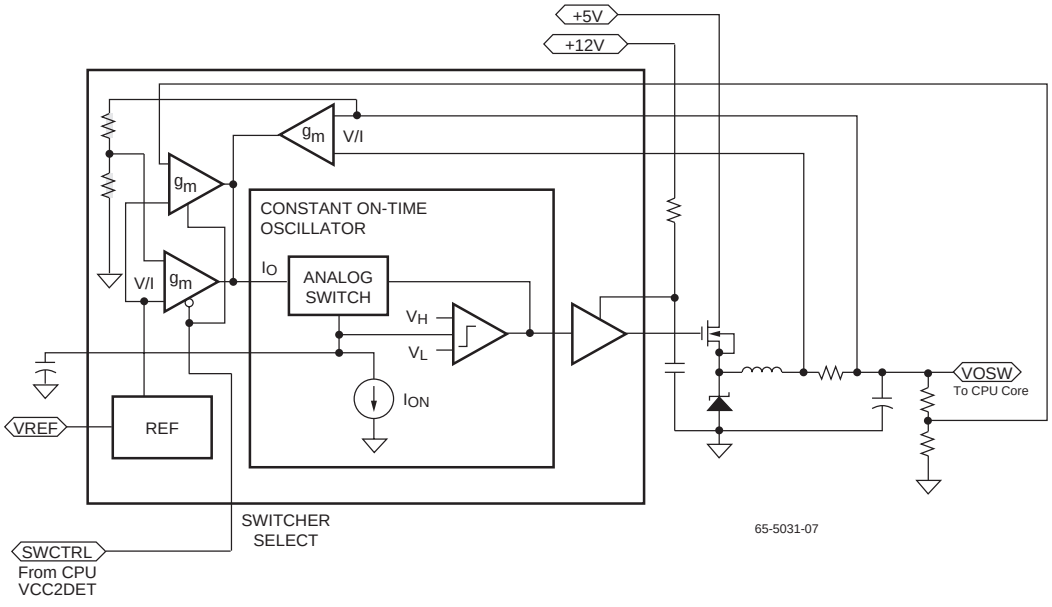
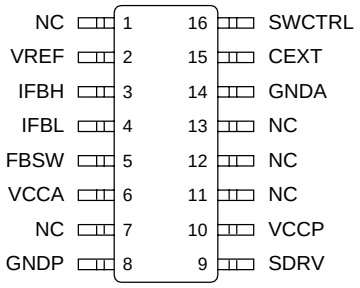


Figure 1. RC5031 Block Diagram

Pin Assignments



Pin Descriptions

Pin Name	Pin Number	Pin Function Description
NC	1	**No connection.**
VREF	2	**Voltage reference test point.** This pin provides access to the internal precision 1.5V bandgap reference and should be decoupled to ground using a 0.1μF ceramic capacitor. No load should be connected to this pin.
IFBH	3	**High side current feedback for switching regulator.** Pins 3 and 4 are used as the inputs for the current feedback control loop and as the short circuit current sense points. Careful layout of the traces from these pins to the current sense resistor is critical for optimal performance of the short circuit protection scheme. See Applications Information for details.
IFBL	4	**Low side current feedback for switching regulator.** See Applications Information for details.
FBSW	5	**Voltage feedback for switching regulator.** This input is active when a logic level LOW is input on pin 16 (SWCTRL). Using two external resistors, it sets the output voltage level for the switching regulator. See Applications Information for details.
VCCA	6	**Switching Regulator V_{CC}.** Power supply for switching regulator control circuitry and voltage reference. Connect to system 5V supply and decouple to ground with 0.1μF ceramic capacitor.
NC	7	**No connection.**
GNDP	8	**Power Ground.** Return pin for high currents flowing in pins 9, 10 and 12 (SDRV, VCCP and LDRV). Connect to a low impedance ground. See Application Information for details.
SDRV	9	**FET driver output for switching regulator.** Connect this pin to the gate of the N-channel MOSFET M1 as shown in Figure 11. The trace from this pin to the MOSFET gate should be kept as short as possible (less than 0.5"). See Applications Information for details.
VCCP	10	**Switching regulator gate drive V_{CC}.** Power supply for SDRV output driver. Connect to system 12V supply with R-C filter shown in Figure 11. See Applications Information for details.
NC	11–13	**No connection.**
GNDA	14	**Analog ground.** All low power internal circuitry returns to this pin. This pin should be connected to system ground so that ground loops are avoided. See Applications Information for details.
CEXT	15	**External capacitor.** A 180pF capacitor is connected to this pin as part of the constant on-time pulse width circuit. Careful layout of this pin is critical to system performance. See Applications Information for details.
SWCTRL	16	**Switching regulator control input.** Accepts TTL/open collector input levels. A logic level HIGH on this pin presets the switching regulator output voltage at 3.5V using internal resistors. A logic level LOW on this pin will select the output voltage set by two external resistors and the voltage feedback control pin 5 (VFBSW). See Applications Information for details.

Preliminary Information

Absolute Maximum Ratings

Supply Voltages, VCCA, VCCP	13V
Junction Temperature, T_J	+150°C
Storage Temperature, T_S	-65 to +150°C
Lead Soldering Temperature, 10 seconds	300°C

Note:
1. Functional operation under any of these conditions is not implied. Performance is guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Switching Regulator V_{CC}, VCCA		4.75	5	5.25	V
Logic Inputs, SWCTRL	Logic HIGH Logic LOW	2.4		 0.8	V V
Ambient Operating Temperature, T_A		0		70	°C
Drive Gate Supply, VCCP		9	12	13	V

Electrical Characteristics

(VCCA = 5V, VCCP = 12V, T_A = 25°C using circuit of Figure 11, unless otherwise noted)

The • denotes specifications which apply over the full ambient operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
Output Voltage, V_{OUT}	SWCTRL = High	•		3.5		V
Output Voltage, V_{OUT}[1]	SWCTRL = Low Set by external resistors	•	1.5		3.6	V
Setpoint Accuracy[2]	I_{SW} = 5A, using 0.1% resistors		-1.2		+1.2	%
Output Temperature Drift				40		ppm
Output Current, I_{SW}		•			13	A
Line Regulation	VCCA = 4.75 to 5.25V, I_{SW}= 5A			0.10	0.15	%Vo
Load Regulation	I_{SW} = 0 to 5A or 5A to 10A			±0.9	±1.3	%Vo
Output Ripple, peak-peak	20MHz BW, I_{SW} = 5A			15		mV
Cumulative DC Accuracy[3]		•		±55	±100	mV
Efficiency	I_{SW} = 5A, VOSW[1] = 2.8V	•	80	85		%
Output Driver Current	Open Loop	•	0.5			A
Short Circuit Threshold Voltage		•	80	90	100	mV
On Time Pulse Width[4]	C_{EXT} = 180pF			3.5		µs
Reference Voltage, VREF			1.485	1.5	1.515	V
VREF PSRR			60			dB
Thermal Impedance, θ_{JA}		•		150		°C/W
VCCA Supply Current	Independent of load	•		5	10	mA

Preliminary Information

Parameter	Conditions		Min.	Typ.	Max.	Units
VCCP Supply Current	I_{SW} = 5A	•		20	25	mA
Internal Power Dissipation	I_{SW} = 5A, using Figure 11	•		125		mW

Notes:

1. When the SWCTRL pin is HIGH or left open, the switch-mode regulator output will be preset at 3.5V using internal precision resistors. When the SWCTRL pin is LOW, the output voltage may be programmed with external resistors. Please refer to the Applications Section for output voltage selection information.
2. Setpoint accuracy is the initial output voltage variability under the specified conditions. When SWCTRL is LOW, the matching of the external resistors will have a major influence on this parameter.
3. Cumulative DC accuracy includes setpoint accuracy, temperature drift, line and load regulation, and output ripple.
4. The on-time pulse width of the oscillator is preset via external capacitor C_{EXT}. See Typical Operating Characteristics curves.

Typical Operating Characteristics

(VCCA = 5V, and T_A = +25°C using circuit in Figure 11, unless otherwise noted)

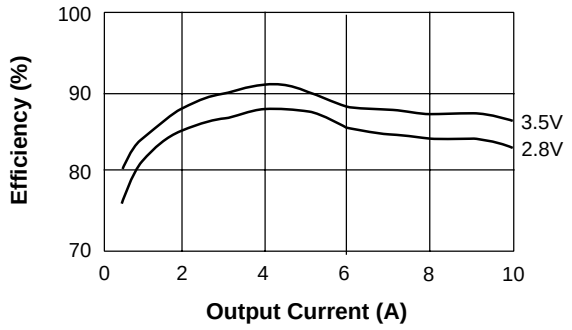


Figure 2. Switcher Efficiency vs. Output Current

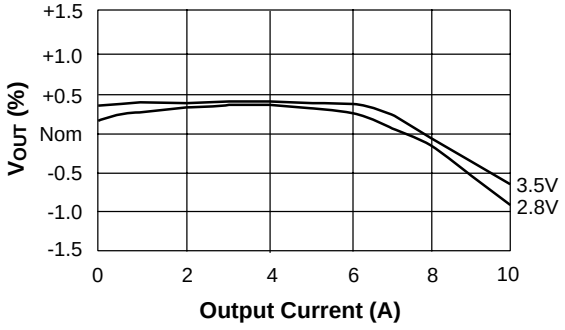


Figure 3. Switcher Output Voltage vs. Load

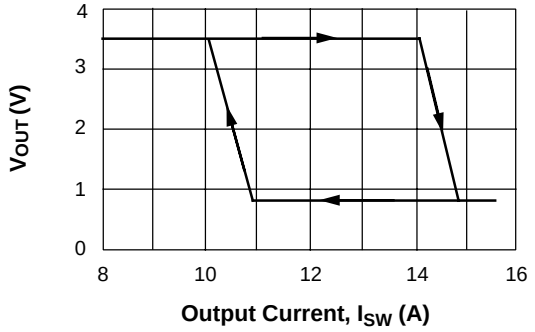


Figure 4. Switcher Output vs Output Current

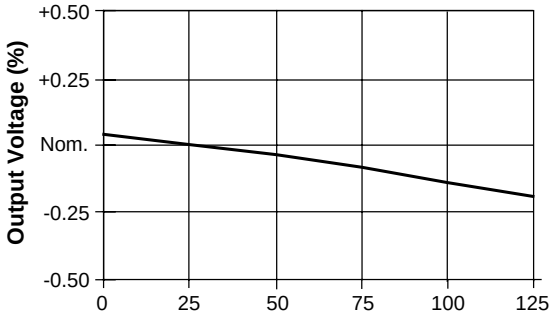


Figure 5. Output Voltage vs. Temperature (I_{SW} or I_L = 5A)

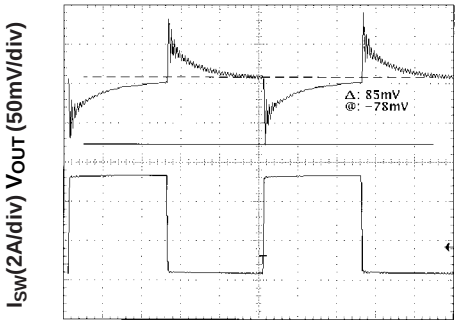


Figure 6. Switcher Transient Response (0.5 to 5.5A Load Step)

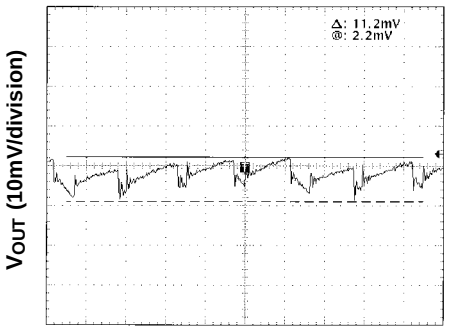


Figure 7. Switcher Output Ripple (BW = 20MHz, I_{SW} = 5A)

Preliminary Information

Typical Operating Characteristics (continued)

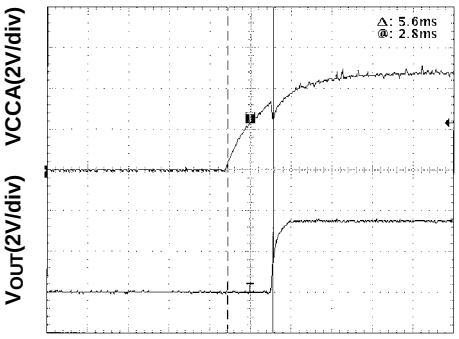


Figure 8. Switcher Turn-on Response

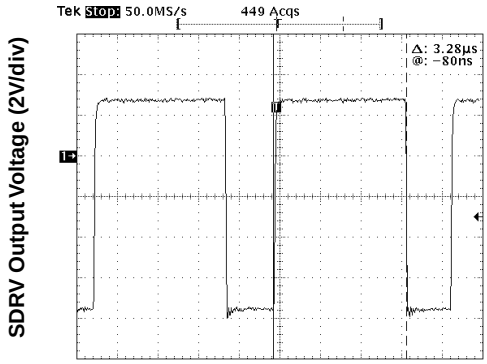


Figure 9. Pin 9 (SDRV) at a 5 Amp Load

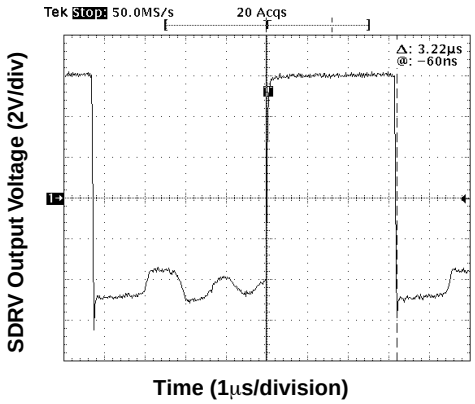


Figure 10. Pin 9 (SDRV) at a 0.1 Amp Load

Preliminary Information

Test Circuit Configurations

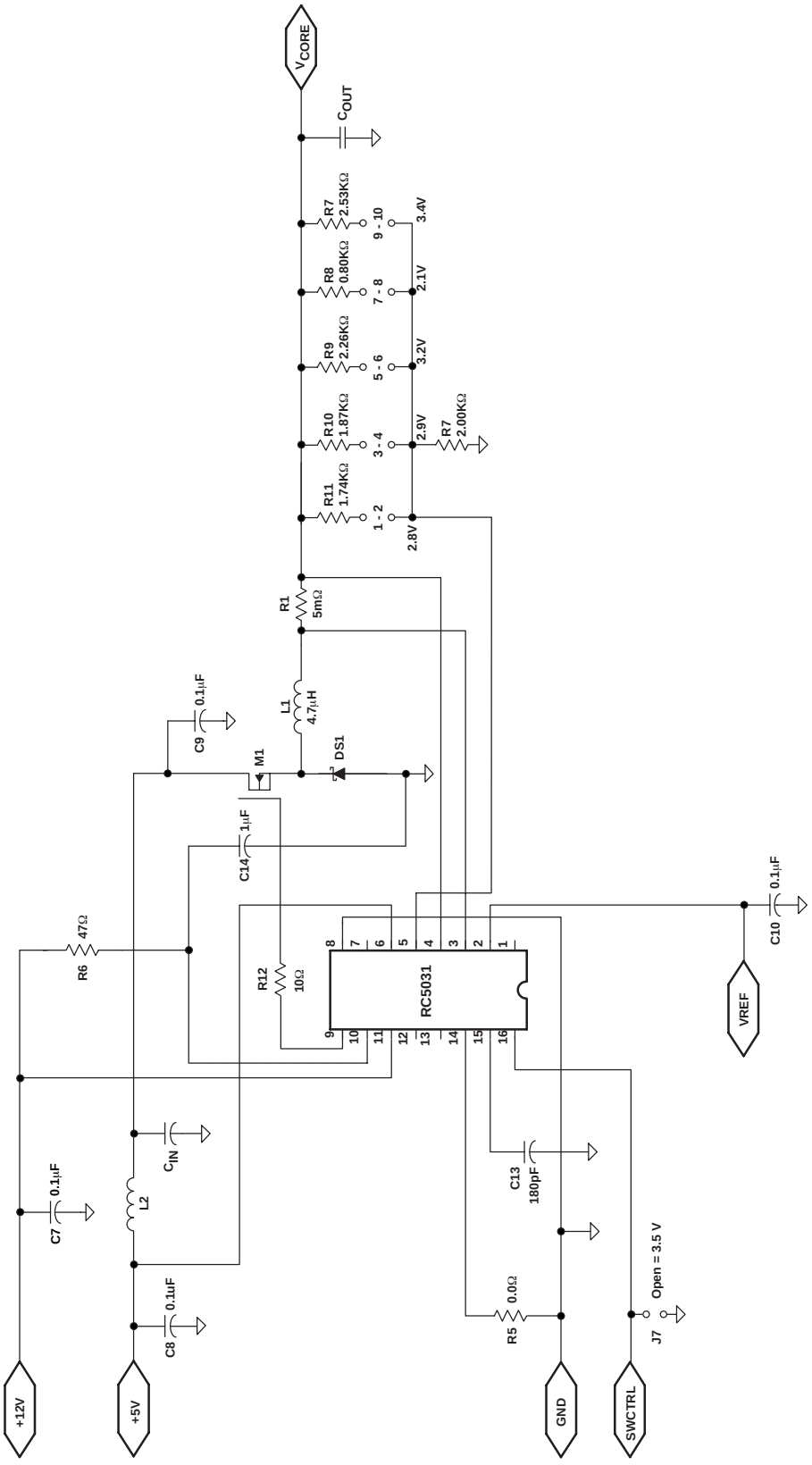


Figure 11. P54/P55C, K6, or M2 Switching Power Supply Application Schematic

Table 1. Bill of Materials for a RC5031 P55C, K6, or M2 Application

Qty.	Reference	Manufacturer Part Order #	Description	Requirements and Comments
4	C7, C8, C9, C10	Panasonic ECU-V1H104ZFX	0.1μF 50V SMT 0805 capacitors	
1	C13	Panasonic ECU-V1H181JCG	180pF 50V SMT0805 capacitor	
1	C14	Panasonic ECSH1CY105R	1μF 16V SMT 0805 Capacitor	
See Table 2	C_{OUT}	Sanyo 6MV1500GX	1500μF 6.3V electrolitic capacitor, 10mm x 20mm	ESR < 0.044Ω
See Table 2	C_{IN}	Sanyo 10MB1200GX	1200μF 10 B electrolytic capacitor, 10mm x 20mm	
1	DS1	Motorola MBR1545CT	Schottky Diode	V_f < 0.57V at I_f = 7.5A
1	L1	Pulse Engineering PE-53682	4.7μH inductor	
1	L2	Beads Inductor	2 Beads, 3.5 x 8mm wire, diameter = 0.6mm	Optional—Helps reduce ripple on the 5V line
1	M1	IRL3103	N-Channel Logic Level Enhancement Mode MOSFET	$R_{DS(ON)}$ < 20mΩ, V_{GS} < 4.5V, I_D > 20A
1	R1	R_{SENSE} (SW)	5mΩ MnCu or Copel resistor	
1	R8	Panasonic ERJ-6ENF 0.80KV	0.80KΩ 1% resistor	0.1% resistor desirable for accuracy
1	R9	Panasonic ERJ-6ENF2.26KV	2.26KΩ 1% resistor	0.1% resistor desirable for accuracy
1	R10	Panasonic ERJ-6ENF1.87KV	1.87KΩ 1% resistor	0.1% resistor desirable for accuracy
1	R11	Panasonic ERJ-6ENF1.74KV	1.74KΩ 1% resistor	0.1% resistor desirable for accuracy
1	R7	Panasonic ERJ-6ENF2.00KV	2.00KΩ 1% resistor	0.1% resistor desirable for accuracy
1	R5	Panasonic ERJ-6GEY000V	0Ω 5% resistor	Resistor raises V_{OUT} 25mV/5Ω
1	R6	Panasonic ERJ-6GEY047V	47Ω 5% resistor	
1	U1	Fairchild Semiconductor RC5031M	Adjustable Switching Regulator	

Table 2. Switching Regulator Components Selection Table

Output Voltage	Output Current	C_{IN} Sanyo 10MV1200GX	C_{OUT} Sanyo 6M1500GX	Power MOSFET (M1)
3.5	8	1x	2x	IRL3103
2.8	6	1x	2x	IRL3103
2.9	6.25	1x	2x	IRL3103
2.9	7.5	1x	2x	IRL3103
3.2	9.5	2x	4x	IRL3103
3.2	13	3x	6x	IRL3103
2.1	5.6	1x	2x	IRL3103
3.3	3	N/A	1x	MJE15028

Applications Information

The following discussion is intended to be an abbreviated list of design considerations regarding the RC5031 as used in a typical voltage processor motherboard application.
For a more thorough discussion of applicable specifications relating to the Intel Pentium P55C processor, please refer to Application Note 48.

Output Voltage Selection

Feedback Voltage Divider

The RC5031 precision reference is trimmed to be 1.5V nominally. When using the RC5031, the system designer has complete flexibility in choosing the output voltage for each regulator from 1.5V to 3.6V. This is done by appropriately selecting the feedback resistors. These should be 0.1% resistors to realize optimum output accuracy. The following equations determine the output voltages of the two regulators:

Switching Regulator

$$V_{OUT} = 1.5 \times \left(\frac{R2 + R3}{R3}\right)$$

where: $R2 > 1.5k\Omega$ and $(R2 + R3) \leq 25k\Omega$

Example:

For 2.8V,

$$V_{OUT} = 1.5 \times \left(\frac{R2 + R3}{R3}\right) = 1.5 \times \left(\frac{1.6k + 1.85k}{1.85k}\right) = 2.8V$$

Short Circuit Considerations

The RC5031 uses a current sensing scheme to limit the load current if an output fault condition occurs. The current sense resistor carries the peak current of the inductor, which is greater than the maximum load current due to ripple currents flowing in the inductor. The RC5031 will begin to limit the output current to the load by turning off the top-side FET driver when the voltage across the current-sense resistor exceeds the short circuit comparator threshold voltage (V_{th}). When this happens the output voltage will temporarily go out of regulation. As the voltage across the sense resistor becomes larger, the top-side MOSFET will continue to turn off until the current limit value is reached. At this point, the RC5031 will continuously deliver the limit current at a reduced output voltage level. The short circuit comparator threshold voltage is typically 90mV, with a variability of ±10mV. The ripple current flowing through the inductor is typically 0.5A. There needs to be a 29% margin for the sense resistor when using a motherboard PC trace resistor. Refer to Application Note 48 for detailed discussions. The sense resistor value can be approximated as follows:

$$R_{SENSE} = \frac{V_{th,min}}{I_{PK}} \times (1 - TF) = \frac{V_{th,min}}{1.5A + I_{LOAD,MAX}} \times (1 - TF)$$

Where TF = Tolerance Factor for the sense resistor and 1.5A accounts for the inductor ripple current.

There are several different types of sense resistors. Table 3 describes the tolerance, size, power capability, temperature coefficient and cost of various types of sense resistors.

Based on the Tolerance in Table 3:

For an embedded PC trace resistor:

$$R_{SENSE} = \frac{V_{th,min}}{1.5 + I_{LOAD,MAX}} \times (1 - TF)$$

$$= \frac{80mV}{1.5A + 10A} \times (1 - 29\%) = 4.9m\Omega$$

For a discrete resistor:

$$R_{SENSE} = \frac{V_{th,min}}{1.5 + I_{LOAD,MAX}} \times (1 - TF)$$

$$= \frac{80mV}{1.5A + 10A} \times (1 - 5\%) = 6.6m\Omega$$

Table 3. Comparison of Sense Resistors

	Motherboard Trace Resistor	Discrete Iron Alloy resistor (IRC)	Discrete Metal Strip surface mount resistor (Dale)	Discrete MnCu Alloy wire resistor	Discrete CuNi Alloy wire resistor (Copel)
Tolerance Factor (TF)	±29%	±5% (±1% available)	±1%	±10%	±10%
Size (L x W x H)	2" x 0.2" x 0.001" (1 oz Cu trace)	0.45" x 0.065" x 0.2"	0.25" x 0.125" x 0.025"	0.2" x 0.04" x 0.16"	0.2" x 0.04" x 0.1"
Power capability	>50A/in	1 watt (3 and 5 watts available)	1 watt (3 and 5 watts available)	1 watt	1 watt
Temperature Coefficient	+4,000 ppm	+30 ppm	±75 ppm	±30 ppm	±20ppm
Cost@10,000 piece quantity	Low; included in motherboard	$0.31	$0.47	$0.09	$0.09

Table 4 lists recommended values for sense resistors for various load currents using an embedded PC trace resistor or a discrete resistor.

Table 4. R_{SENSE} for Various Load Currents, Switching Regulator

$I_{LOAD, MAX}$ (A)	R_{SENSE} PC Trace Resistor (mΩ)	R_{SENSE} Discrete Resistor (mΩ)
5	8.7	11.7
6	7.6	10.1
7	6.7	8.9
8	6.0	8.0
9	5.4	7.0
10	4.9	6.6

Since the value of the sense resistor is often less than 10mΩ, care should be taken in the layout of the PCB. Trace resistance can contribute significant errors. The traces to the IFBH and IFBL pins of the RC5031 should be Kelvin connected to the pads of the current-sense resistor. To minimize the influence of noise, the two traces should be run next to each other.

Thermal Design Considerations

Good thermal management is critical in the design of high current regulators. System reliability will be degraded if the component temperatures become excessive. The following guide should serve as a reference for proper thermal management.

MOSFET Temperature

The maximum power dissipation of the MOSFET can be calculated by using the following formula:

$$P_D = \frac{T_{J(MAX)} - T_A}{\Theta_{JA}}$$

For IR 3103, Θ_{JA} is 42°C/W. For reliability the junction temperature of the MOSFET should not exceed 120°C. Assuming that the ambient temperature is 40°C, then the maximum power dissipation is calculated as:

$$P_D = \frac{120 - 40}{42} = 1.905W$$

The power that the MOSFET dissipates at the rated 6A load is calculated as follows:

$$P_{MOSFET} = I_{LOAD}^{\ 2} \times R_{DS(ON)} \times (\text{Duty Cycle}) + \frac{V_{IN} \times I_{LOAD}}{6} \times (t_r + t_f) \times f$$

$$\text{Duty Cycle} = \frac{V_{OUT} + V_D}{V_{IN} + V_D - (I_{LOAD} \times R_{DS(ON)})}$$

where V_D is the forward voltage of the Schottky diode used.

Using the above formula, for V_{out} = 2.8V, I_{LOAD} = 6A

$$\text{Duty Cycle} = \frac{2.8 + 0.57}{2.8 + 0.57 - (6 \times 0.019)} = 61.8\%$$

$$P_{MOSFET} = 6A^2 \times 0.019\Omega \times 61.8\% + \frac{5V \times 6A}{6} \times (210ns + 54ns) \times 300KHz$$

$$P_{MOSFET} = 0.82W$$

Since the power at 6A is within the thermal guideline, a heat sink is not required other than the PCB.

Schottky Diode

In Figure 11, MOSFET M1 and flyback diode DS1 are used as complementary switches in order to maintain a constant current through the output inductor L1. As a result, DS1 will have to carry the full current of the output load when the power MOSFET is turned off. The power in the diode is a direct function of the forward voltage at the rated load current during the off time of the FET. The following equation can be used to estimate the diode power:

$$P_{DIODE} = I_D \times V_D \times (1 - DutyCycle)$$

where I_D is the forward current of the diode, V_D is the forward voltage of the diode, and DutyCycle is defined the same as above.

For the Motorola MBR2030CTL Rectifier in Figure 11,

$$P_{DIODE} = 10A \times 0.57 \times (1 - 64.8\%) = 2.0W$$

It is recommended that the diode T0-220 package be placed down on the motherboard to utilize the power plane as a heatsink and achieve a thermal resistance of 40°C/W.

Board Design Considerations

RC5031 Placement

The RC5031 should be placed as close to the core voltage supply pins of the P55C as possible, preferably to have the PC layer directly underneath the RC5031 for ground layer. This serves as extra isolation from noisy power planes.

MOSFET Placement

Placement of the power MOSFET is critical in the design of the switch-mode regulator. The FET should be placed in such a way as to minimize the length of the gate drive path from the RC5031 SDRV pin. This trace should be kept under 0.5" for optimal performance. Excessive lead length on this trace will cause high frequency noise resulting from the parasitic inductance and capacitance of the trace. Since this voltage can transition nearly 12V in around 100nsec, the resultant ringing and noise will be very difficult to suppress. This trace should be routed on one layer only and kept well away from the "quiet" analog pins of the device; VREF, CEXT, FBSW, IFBH, IFBL, and VFBL. A10Ω resistor in series with the MOSFET gate can decrease this layout critically. Refer to Figure 12.

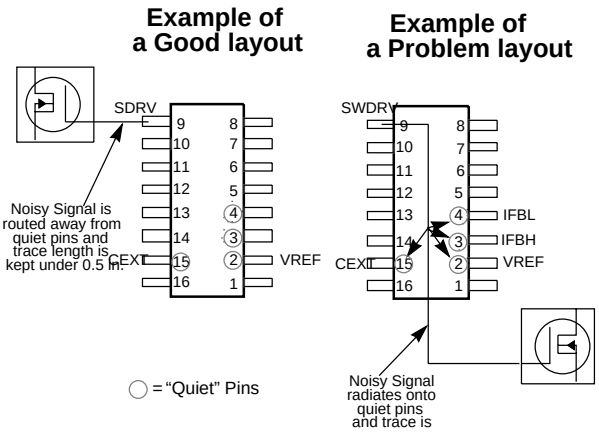


Figure 12. Examples of good and poor layouts

Inductor and Schottky Diode Placement

The inductor and fly-back Schottky diode need to be placed close to the source of the power MOSFET for the same reasons stated above. The node connecting the inductor and Schottky diode will swing between the drain voltage of the FET and the forward voltage of the Schottky diode. It is recommended that this node be converted to a plane if possible. This node will be part of the high current path in the design, and as such it is best treated as a plane in order to minimize the parasitic resistance and inductance on that node. Since most PC board manufacturers utilize 1/2 oz copper on the top and bottom signal layers of the PCB, it is not recommended to use these layers to rout the high current portions of the regulator design. Since it is more common to use 1 oz. copper on the PCB inner layers, it is recommended to use those layers to route the high current paths in the design.

Capacitor Placement

One of the keys to a successful switch-mode power supply design is correct placement of the low ESR capacitors. Decoupling capacitors serve two purposes; first there must be enough bulk capacitance to support the expected transient current of the CPU, and second, there must be a variety of values and capacitor types to provide noise supression over a wide range of frequencies. The low ESR capacitors on the input side (5V) of the FET must be located close to the drain of the power FET. Minimizing parasitic inductance and resistance is critical in supressing the ringing and noise spikes on the power supply. The output low ESR capacitors need to be placed close to the output sense resistor to provide good decoupling at the voltage sense point. One of the characteristics of good low ESR capacitors is that the impedance gradually increases as the frequency increases. Thus for high frequency noise supression, good quality low inductance ceramic capacitors need to be placed in parallel with the low ESR bulk capacitors. These can usually be 0.1µF 1206 surface mount capacitors.

Power and Ground Connections

The connection of VCCA to the 5V power supply plane should be short and bypassed with a 0.1µF directly at the VCCA pin of the RC5031. The ideal connection would be a via down to the 5V power plane. A similar arrangement should be made for the VCCL pin that connects to +12V, though this one is somewhat less critical since it powers only the linear op-amp. Each ground should have a separate via connection to the ground plane below.

A 12V power supply is used to bias the VCCP. A 47Ω resistor is used to limit the transient current into VCCP. A 1uF capacitor filter is used to filter the VCCP supply and source the transient current required to charge the MOSFET gate capacitance. This method provides sufficiently high gate bias voltage to the MOSFET (V_{GS}), and therefore reduces $R_{DS(ON)}$ of the MOSFET and its power loss.

Figure 13 provides about 5V of gate bias which works well when using typical logic-level MOSFETs, as shown in Figure 14. Non-logic-level MOSFETs should not be used because of their higher $R_{DS(ON)}$.

MOSFET Gate Bias

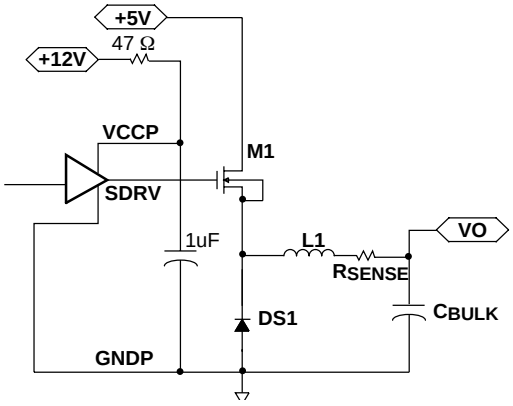


Figure 13. 12V Gate Bias Configuration

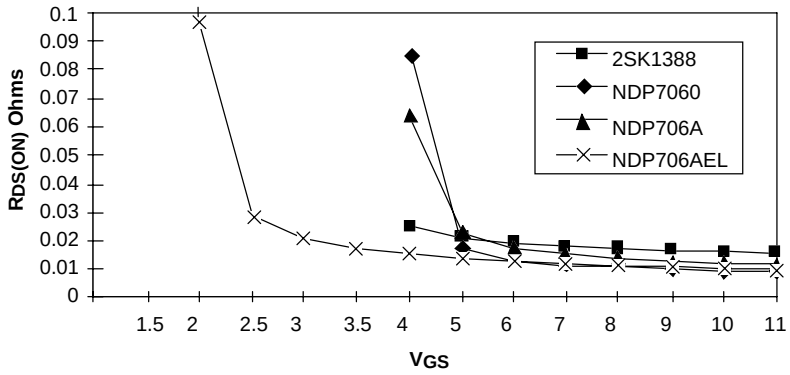


Figure 14. $R_{DS(ON)}$ vs. V_{GS} for Selected Logic-Level MOSFETs

Preliminary Information

Notes:

Notes:

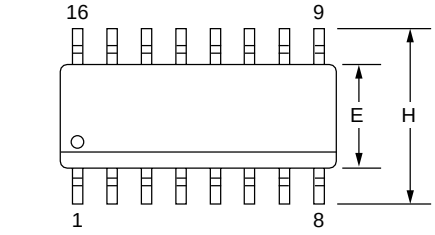
Mechanical Dimensions

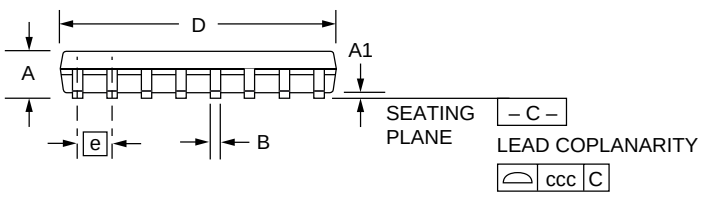
16-Lead SOIC Package

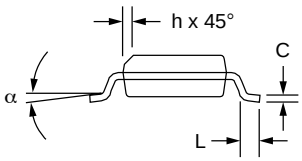
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.19	0.25	5
D	.386	.394	9.80	10.00	2
E	.150	.158	3.81	4.00	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.80	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	16		16		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Preliminary Information

Ordering Information

Product Number	Package
RC5031M	16 pin SOIC

Preliminary Information

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

5/20/98 0.0m 001
Stock#DS30005031

Application Circuit for P55C, K6, and M2

Figure 1. P54/P55C, K6 or M2 Single/Dual Power Supply Application Schematic

Table 1. Bill of Materials for a RC5031 P55C, K6, or M2 Application

Qty.	Reference	Manufacturer Part Order #	Description	Requirements and Comments
4	C7, C8, C9, C10	Panasonic ECU-V1H104ZFX	0.1μF 50V SMT 0805 capacitors	
1	C13	Panasonic ECU-V1H181JCG	180pF 50V SMT0805 capacitor	
1	C14	Panasonic ECSH1CY105R	1μF 16V SMT 0805 Capacitor	
See Table 2	C_{OUT}	Sanyo 6MV1500GX	1500μF 6.3V electrolitic capacitor, 10mm x 20mm	ESR < 0.044Ω
See Table 2	C_{IN}	Sanyo 10MB1200GX	1200μF 10 B electrolytic capacitor, 10mm x 20mm	
1	DS1	Motorola MBR1545CT	Schottky Diode	V_f < 0.57V at I_f = 7.5A
1	L1	Pulse Engineering PE-53682	4.7μH inductor	
1	L2	Beads Inductor	2 Beads, 3.5 x 8mm wire, diameter = 0.6mm	Optional—Helps reduce ripple on the 5V line
1	M1	IRL3103	N-Channel Logic Level Enhancement Mode MOSFET	$R_{DS(ON)}$ < 20mΩ, V_{GS} < 4.5V, I_D > 20A
1	R1	R_{SENSE} (SW)	5mΩ MnCu or Copel resistor	
1	R8	Panasonic ERJ-6ENF 0.80KV	0.80KΩ 1% resistor	0.1% resistor desirable for accuracy
1	R9	Panasonic ERJ-6ENF2.26KV	2.26KΩ 1% resistor	0.1% resistor desirable for accuracy
1	R10	Panasonic ERJ-6ENF1.87KV	1.87KΩ 1% resistor	0.1% resistor desirable for accuracy
1	R11	Panasonic ERJ-6ENF1.74KV	1.74KΩ 1% resistor	0.1% resistor desirable for accuracy
1	R7	Panasonic ERJ-6ENF2.00KV	2.00KΩ 1% resistor	0.1% resistor desirable for accuracy
1	R5	Panasonic ERJ-6GEY000V	0Ω 5% resistor	Resistor raises V_{OUT} 25mV/5Ω
1	R6	Panasonic ERJ-6GEY047V	47Ω 5% resistor	
1	U1	Fairchild Semiconductor RC5031M	Adjustable Switching Regulator	

Table 2. Switching Regulator Components Selection Table

Output Voltage	Output Current	C_{IN} Sanyo 10MV1200GX	C_{OUT} Sanyo 6M1500GX	Power MOSFET (M1)
3.5	8	1x	2x	IRL3103
2.8	6	1x	2x	IRL3103
2.9	6.25	1x	2x	IRL3103
2.9	7.5	1x	2x	IRL3103
3.2	9.5	2x	4x	IRL3103
3.2	13	3x	6x	IRL3103
2.1	5.6	1x	2x	IRL3103
3.3	3	N/A	1x	MJE15028

RC5032

5V to 3.3V Step-Down DC-DC Converter

Features

- >85% Efficiency
- Fast transient response
- Soft control power-up
- Short circuit protection
- Output voltage fixed 3.3V
- Low TC reference voltage
- Adjustable oscillator frequency
- Drives N-Channel MOSFET
- 8 pin SOIC, 8 pin DIP package

Applications

- 3.3V power supply for Pentium™ based desktop CPU motherboards
- Minimum component DC-DC converters

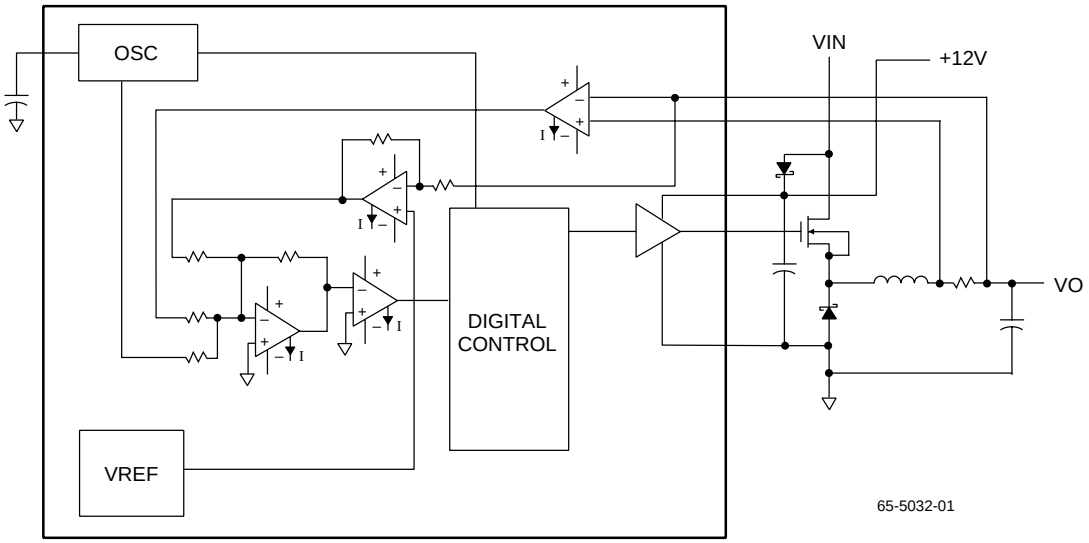
Preliminary Information

Description

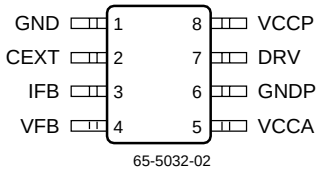
The RC5032 is a step-down DC-DC controller IC dedicated to providing a 5V to 3.3V conversion for various types of CPU power. It can be configured with the proper applications circuitry to deliver load currents greater than 10 Amps. The RC5032 is designed to operate in a standard PWM control mode under heavy load conditions and as a PFM controller in light load conditions. Its highly accurate low TC reference eliminates the need for precision external components in order to achieve tight tolerance voltage regulation.

The programmable oscillator can operate from 200KHz to greater than 1MHz to provide for flexibility in choosing external components such as inductors, capacitors, and Power MOSFETs.

Block Diagram



Pin Assignments



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Pin Definitions

Pin Name	Pin Number	Pin Function Description
GND	1	Ground
CEXT	2	External capacitor for setting oscillator frequency
IFB	3	Current Feedback Input
VFB	4	Voltage Feedback Input
VCCA	5	Analog VCC
GNDP	6	Power ground for high current driver
DRV	7	FET Driver Output
VCCP	8	VCC for FET output drivers

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Conditions	Min	Typ	Max	Units
VCCP	Driver Supply				13	V

Note:

1. Functional operation under any of these conditions is NOT implied. Performance is guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter		Conditions	Min	Typ	Max	Units
VCC	Supply Voltage		4.5	5	7	V
VCCP	Driver Supply		9		13	V
VIH	Input Voltage, Logic HIGH		2			V
VIL	Input Voltage, Logic LOW				0.8	V
	Ambient Temp		0		70	°C

Preliminary Information

DC Electrical Characteristics

(V_{CC} = 5V, Fosc = 650 KHz, and T_A = 0–70˚C)

Parameter		Conditions	Min	Typ	Max	Units
V_O	Output Voltage		3.1	3.4	3.6	V
I_O	Output Current	See Figure 1 for application		7		A
Vref Acc	Reference Accuracy			1	3	%
VTC	Output Voltage TC			40		ppm
LDR	Load Regulation	0.5 to 7A		0.5		%V_O
LIR	Line Regulation	V_{CC} = ±5%		0.07		%V_O
V_R	Output Voltage Ripple			30		mV
Cum Acc	Cumulative Accuracy[1]	T_A = 0–70°C		3	5	%
Eff	Efficiency	Iload > 4A	85	88		%
Iodr	Output Driver I	Open Loop	0.5	0.7		A
Pd	Power Dissipation			0.1		W

Notes:

1. Output Voltage accuracy, Tempco, load regulation, ripple, and transient performance determine the Cumulative Accuracy.

AC Electrical Characteristics

(V_{CC} = 5V, Fosc = 650 KHz, and T_A = 25˚C)

Parameter		Conditions	Min	Typ	Max	Units
Tr	Response Time	Il=0.5A to 7A		10		µs
Fosc	Oscillator Range		0.2		1.2	MHz
Osc Acc	Fosc Accuracy			10		%
Dtc	Max Duty Cycle	PWM mode	90	95		%
Dtcm	Min Duty Cycle	PFM mode			100	ns
Iscp	Short Circuit Prot			250		mV
Trimax	Response to Imax			15	30	µs
Tssp	Soft start response			1		ms

Preliminary Information

Test Circuit

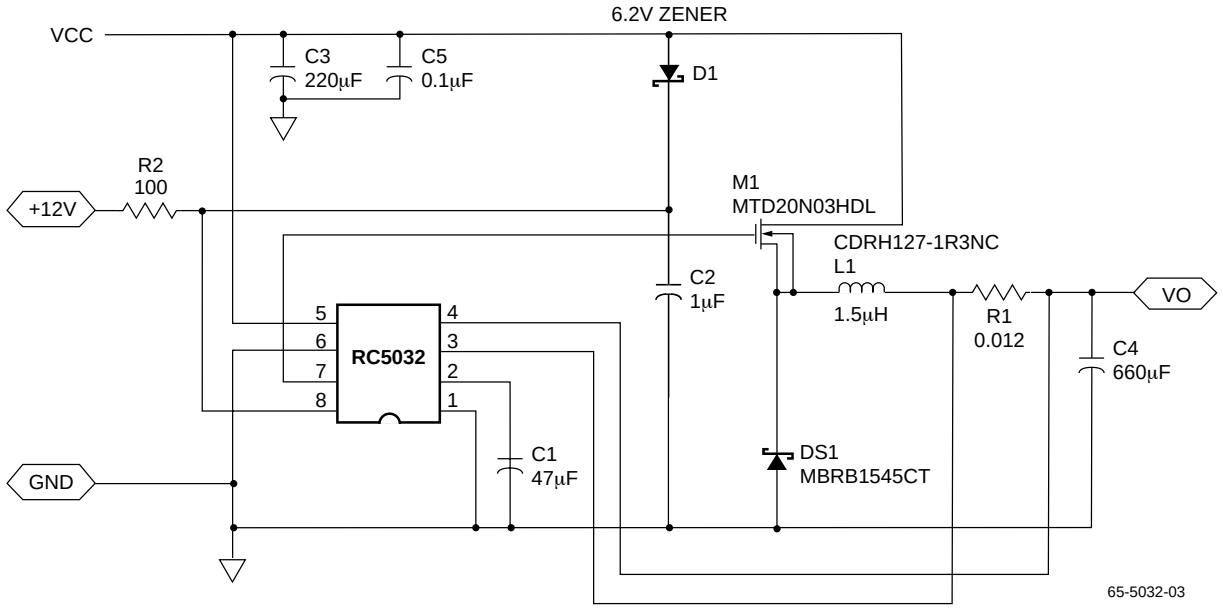


Figure 1. RC5032 7A Schematic

Table 1. Components for RC5032

RC5032 Standard Application Circuit Bill of Materials			
Ref Designator	**Quantity**	**Part No.**	**Manufacturer**
L1	1	CDRH127-1R3NC	Sumida
M1	1	MTD20N03HDL	Motorola
DS1	1	MBRB1545CT	Motorola
D1	1	6.2V Zener	any
R1	1	LRC-2512	IRC
C3	1	OS-CON 10SA220M	Sanyo
C4	2	OS-CON 10SA330M	Sanyo
C2	1	1uF	Monolithic ceramic Cap
C1	1	47pF	SMD Cap
C5	1	0.1uF	SMD Cap
R2	1	100Ω	SMD Res

Notes:

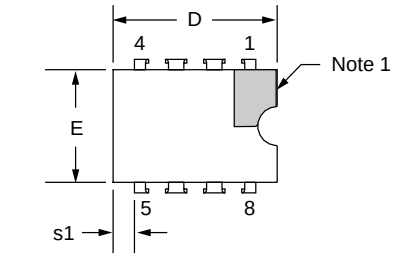
Mechanical Dimensions

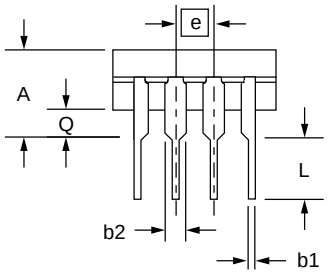
8 Lead Ceramic DIP Package

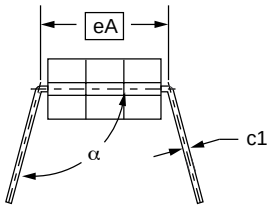
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2, 8
c1	.008	.015	.20	.38	8
D	—	.405	—	10.29	4
E	.220	.310	5.59	7.87	4
e	.100 BSC		2.54 BSC		5, 9
eA	.300 BSC		7.62 BSC		7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 4, 5 and 8 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 8.
6. Applies to all four corners (leads number 1, 4, 5, and 8).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Six spaces.







Preliminary Information

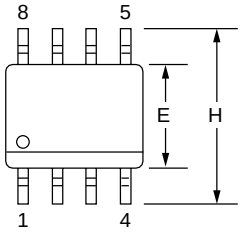
Mechanical Dimensions (continued)

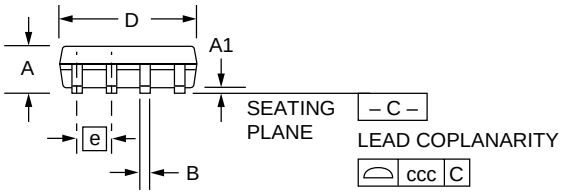
8 Lead SOIC Package

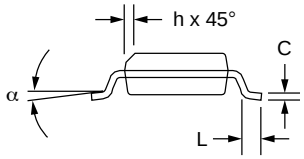
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.20	0.25	5
D	.189	.197	4.80	5.00	2
E	.150	.158	3.81	4.01	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	8		8		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Preliminary Information

Ordering Information

Product Number	Package	θJA
RC5032M	8 SOIC	85°C/W

5/20/98 0.0m 001
Stock#DS30005032

RC5033

Adjustable Synchronous DC-DC Converter

Features

- >85% Efficiency
- 350uA quiescent current in shutdown
- Fast transient response
- Soft control power-up
- Over-Voltage Protection
- Output voltage range from 2.0V to 3.6V
- Factory trimmed low TC reference voltage
- Adjustable oscillator frequency
- Drives N-Channel MOSFETs
- 16 pin SOIC package

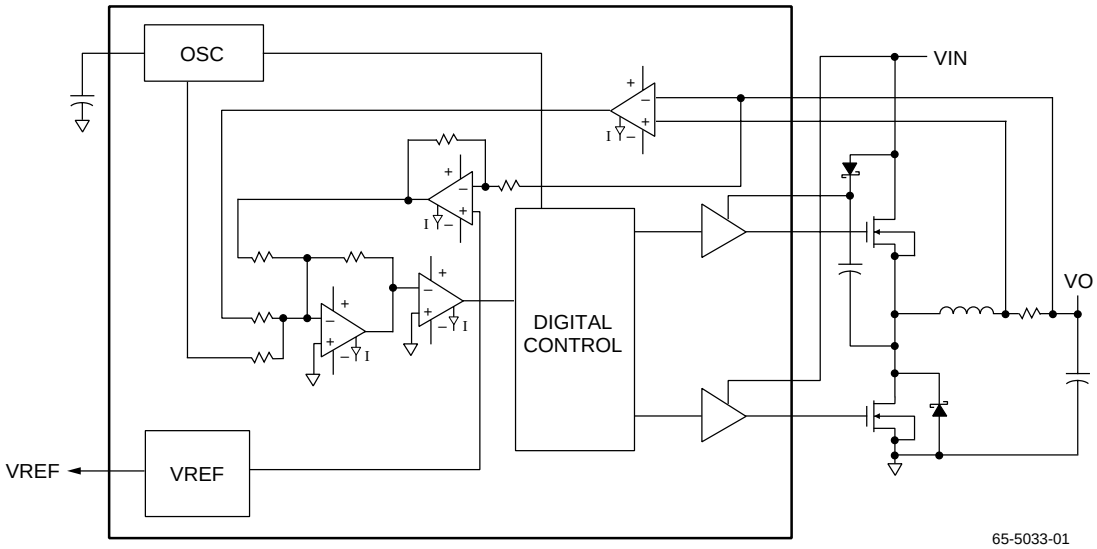
Applications

- 3.3V power supply for Pentium™ based CPU motherboards
- 3.45V power supply for AMD-K5™ CPU
- 2.5V or 3.6V power supply for PowerPC™

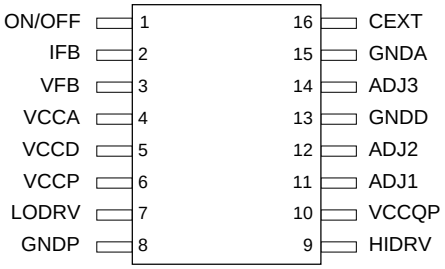
Description

The RC5033 is a synchronous mode DC-DC controller IC dedicated to providing a 5V to 2.0V up to 3.6V conversion for various types of CPU power . It can be configured in both the synchronous and non-synchronous modes and with the proper applications circuitry can be used to deliver load current greater than 10 Amps. The RC5033 is designed to operate in a standard PWM control mode under heavy load conditions and as a PFM controller in light load conditions. Its highly accurate low TC reference eliminates the need for precision external components in order to achieve tight tolerance voltage regulation. Through the use of external resistors, the RC5033 can generate accurate output voltages from 2.0V up to 3.6V. An integrated Over-Voltage protection function constantly monitors the output voltage and shuts down the power to the CPU in the event of a out-of-tolerance voltage situation, thereby protecting the CPU. The programmable oscillator can operate from 200KHz to greater than 1MHz to provide for flexibility in choosing external components such as inductors, capacitors, and Power MOSFETs.

Block Diagram



Pin Assignments



Pin Definitions

Pin Name	Pin Number	Pin Function Description
On/Off	1	A low level on this pin will power down; tie to VCCD if not used.
IFB	2	Current Feedback Input.
VFB	3	Voltage Feedback Input.
VCCA	4	Analog VCC.
VCCD	5	Digital VCC.
VCCP	6	VCC for synchronous FET output drivers.
LODRV	7	Synchronous FET driver output.
GNDP	8	Power ground for high current drivers.
HIDRV	9	High side FET driver output.
VCCQP	10	VCC for High side FET output driver
ADJ1	11	VREF adjust pin.[1]
ADJ2	12	VREF adjust pin.[1]
GNDD	13	Digital ground.
ADJ3	14	VREF adjust pin.[1]
GNDA	15	Analog ground.
CEXT	16	External capacitor for setting oscillator frequency.

Note:
1. See voltage adjust table for function

Output Voltage Selection Table

VOUT	ADJ1	ADJ2	ADJ3
3.5V	N/C	N/C	N/C
3.35V	N/C	[2]	[2]
3.3V	[2]	N/C	[2]
2.9V[1]	3.9K	N/C	N/C
2.5V[1]	2K	N/C	N/C
2.0V[1]	39Ω	N/C	N/C

Note:
1. See Figure 3 for resistor connection.
2. Indicated short pins together.

Preliminary Information

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Conditions	Min	Typ	Max	Units
V_{CCP}	Driver Voltage				13	V
V_{CCQP}	High Driver Supply				13	V
T_J	Junction Temperature				175	°C
T_A	Ambient Operating Temperature		0		70	°C
T_S	Storage Temperature		-65		150	°C
T_L	Lead Soldering Temperature	(10 seconds)			300	°C

Note:

1. Functional operation under any of these conditions is NOT implied.

Operating Conditions

Parameter		Conditions	Min	Typ	Max	Units
V_{CC}	Supply Voltage		4.5	5	7	V
V_{CCP}	Low Driver Supply		4.5	5	12	V
V_{CCQP}	High Driver Supply		9		13	V
V_{IH}	Input Voltage, Logic HIGH		2			V
V_{IL}	Input Voltage, Logic LOW				0.8	V

DC Electrical Characteristics

(V_{CC} = 5V, fosc = 650 KHz, and T_A = +25˚C unless otherwise noted)

Parameter		Conditions	Min	Typ	Max	Units
V_O	Output Voltage	Nominal, Pin 12 conn. Pin 14, T_A = 0–70°C	3.135	3.3	3.465	V
I_O	Output Current	See Figure for application		5		A
Vref Acc	Voltage Reference Accuracy			1		%
VTC	Output Voltage Tempco			-40		ppm
LDR	Load Regulation	0.5 to 7A		1		%Vo
LIR	Line Regulation	V_{CC} = ±5%		0.14		%Vo
V_R	Output Voltage Ripple			30		mV
Cum Acc	Cumulative Accuracy[2]	T_A = 0–70°C		3		%
Eff	Efficiency	Synchronous mode > 1A	80	85		%
Iodr	Output Driver I	Open Loop	0.5	0.7		A
PD	Power Dissipation			0.1	0.2	W

Notes:

1. Functional operation under any of these conditions is not implied. Performance is guaranteed only if Operating Conditions are not exceeded.
2. Output Voltage accuracy, Tempco, load regulation, ripple, and transient performance determine the Cumulative Accuracy.

Preliminary Information

AC Electrical Characteristics[1]

(T_A = +25˚C unless otherwise noted)

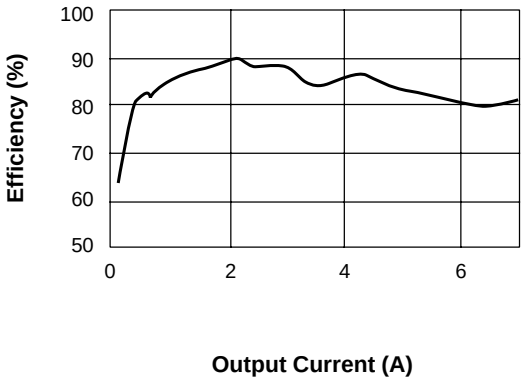
Parameter		Conditions	Min	Typ	Max	Units
Tr	Response Time	Il=0.5A to 5.5A		10		μs
Fosc	Oscillator Range		0.2		1.2	MHz
Osc Acc	Fosc Accuracy			10		%
Dtc	Max Duty Cycle	PWM mode	90	95		%
Dtcm	Min Duty Cycle	PFM mode			100	ns
Imax	Imax Threshold			30		mV
Iscp	Short Circuit Prot			80		mV
Ovp	Over Voltage Prot			20		%Vo
Trimax	Response to Imax			15	30	ns
Tssp	Soft start response			10		μs

Note:

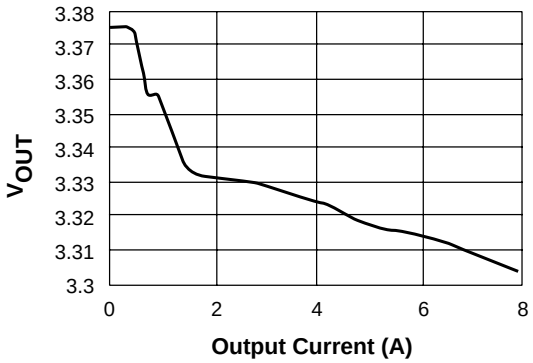
1. Guaranteed by design, not 100% total.

Typical Operating Characteristics[1]

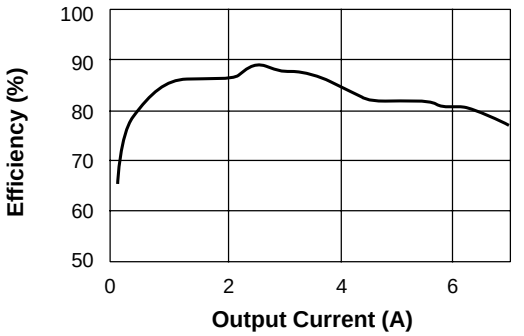
Efficiency vs Output Current (F_{OSC} = 400 KHz)



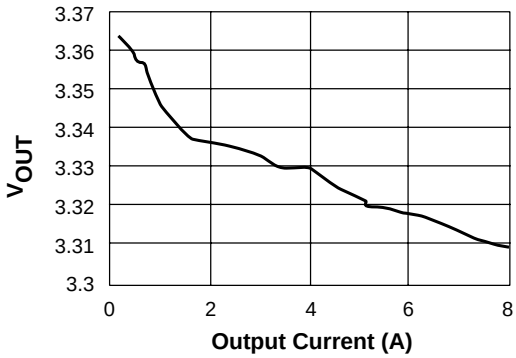
Load Regulation (F_{OSC} = 400 KHz)



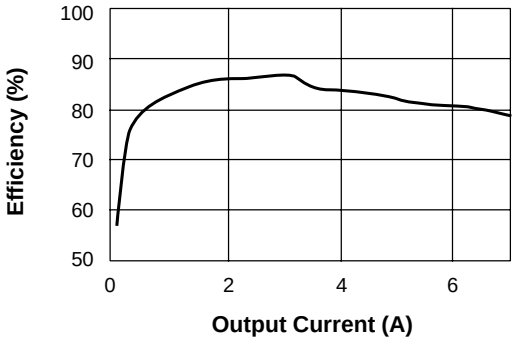
Efficiency vs Output Current (F_{OSC} = 650 KHz)



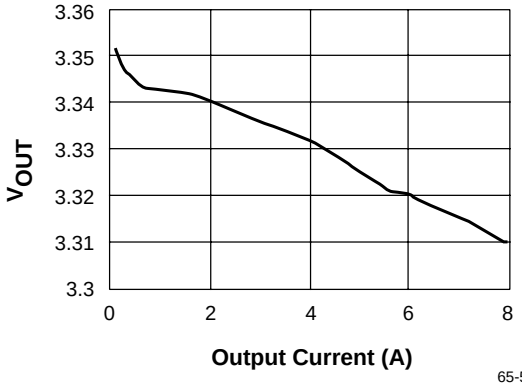
Load Regulation (F_{OSC} = 650 KHz)



Efficiency vs Output Current (F_{OSC} = 1 MHz)



Load Regulation (F_{OSC} = 1 MHz)



65-5033-03

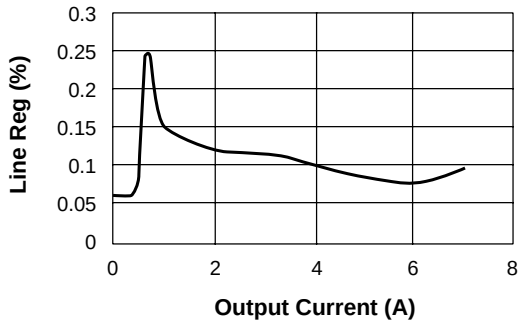
Note:

1. Data taken with circuit of Figure 1.

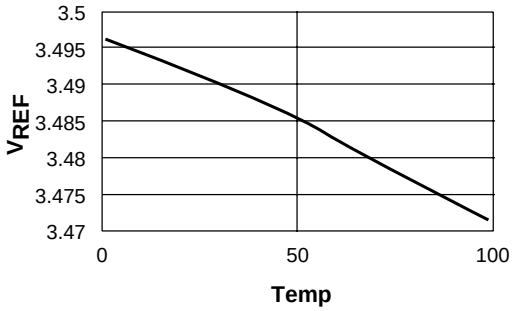
Preliminary Information

Typical Operating Characteristics (continued)

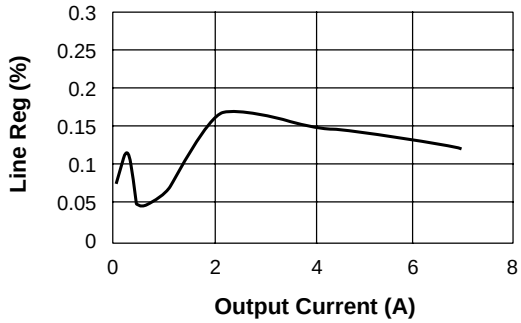
Line Regulation vs. Output Load (F_{OSC} = 400 KHz)



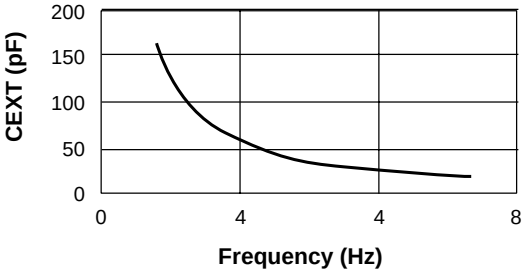
Reference Tempco



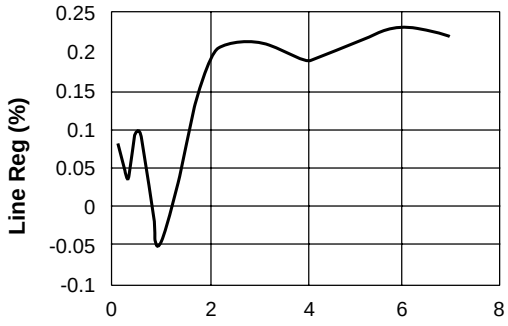
Line Regulation vs. Output Load (F_{OSC} = 650 KHz)



CEXT vs. Oscillator Frequency



Line Regulation vs. Output Load (F_{OSC} = 1 MHz)



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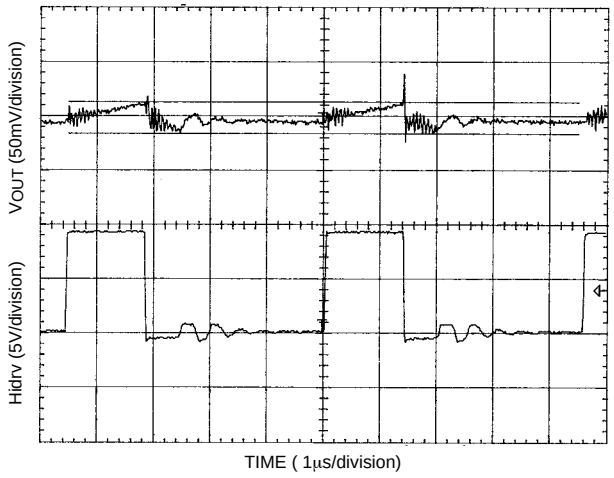
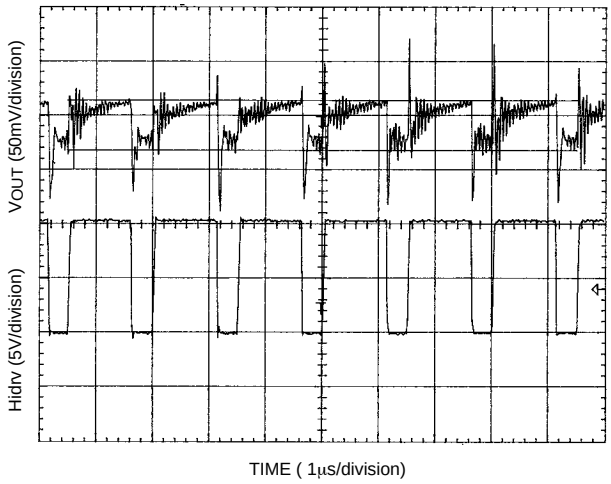
Preliminary Information

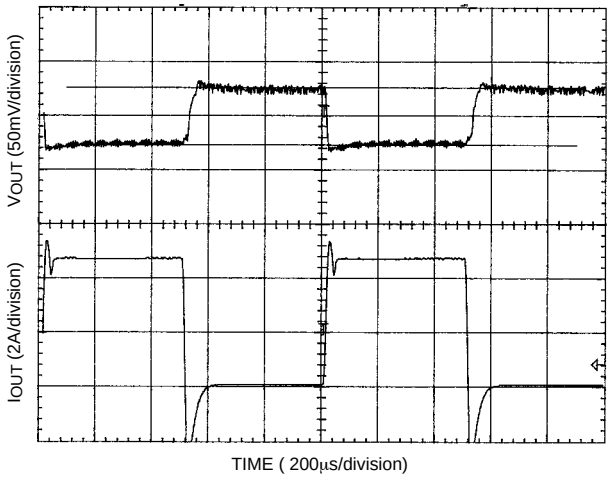
Typical Operating Characteristics (continued)



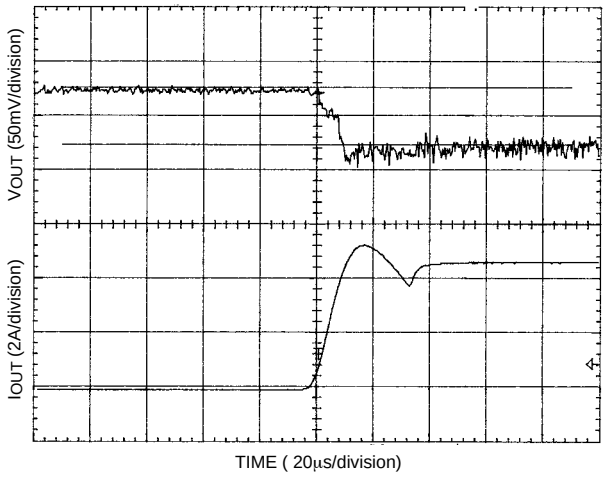
AC Ripple response .2A Load



AC Ripple response 5A Load



Transient Response .2A to 5A Load



Transient Response Magnified

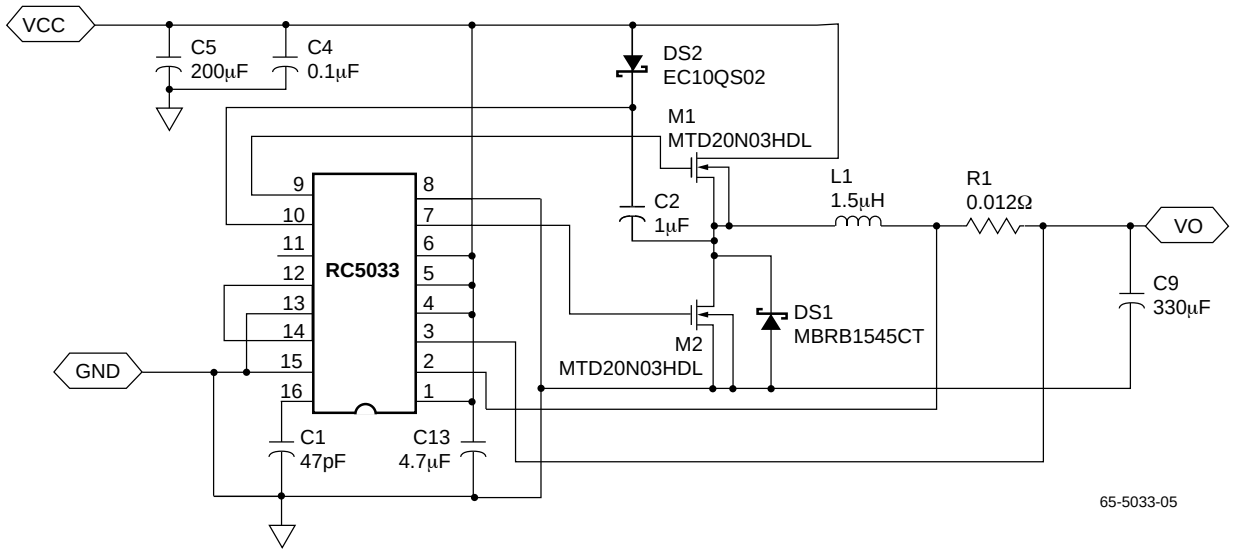


Figure 1. Standard 7A Application Schematic

Preliminary Information

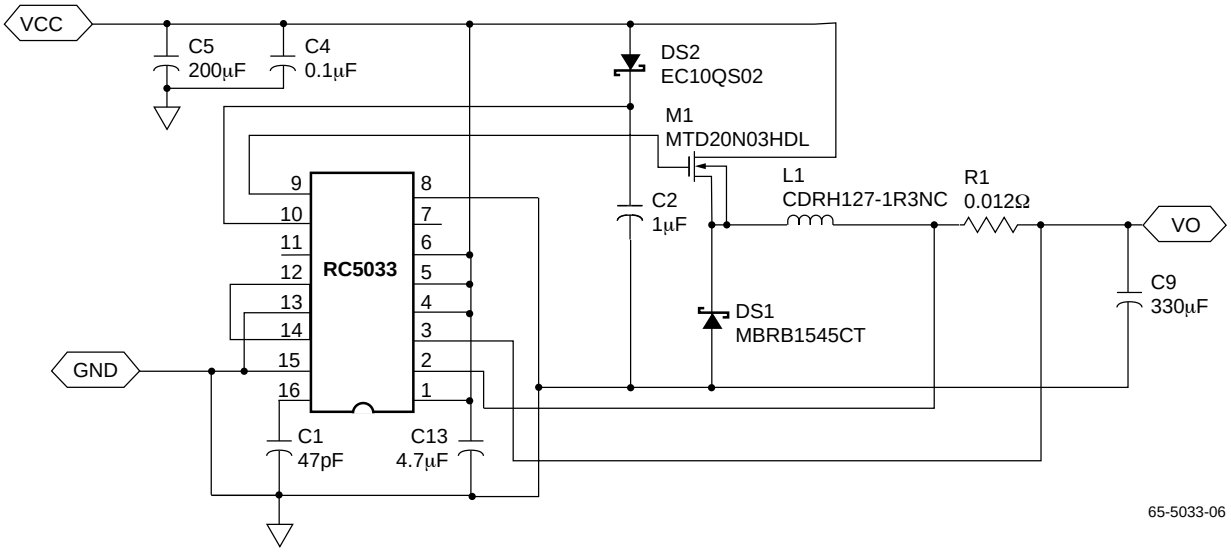


Figure 2. Non-Synchronous 7A Application Circuit

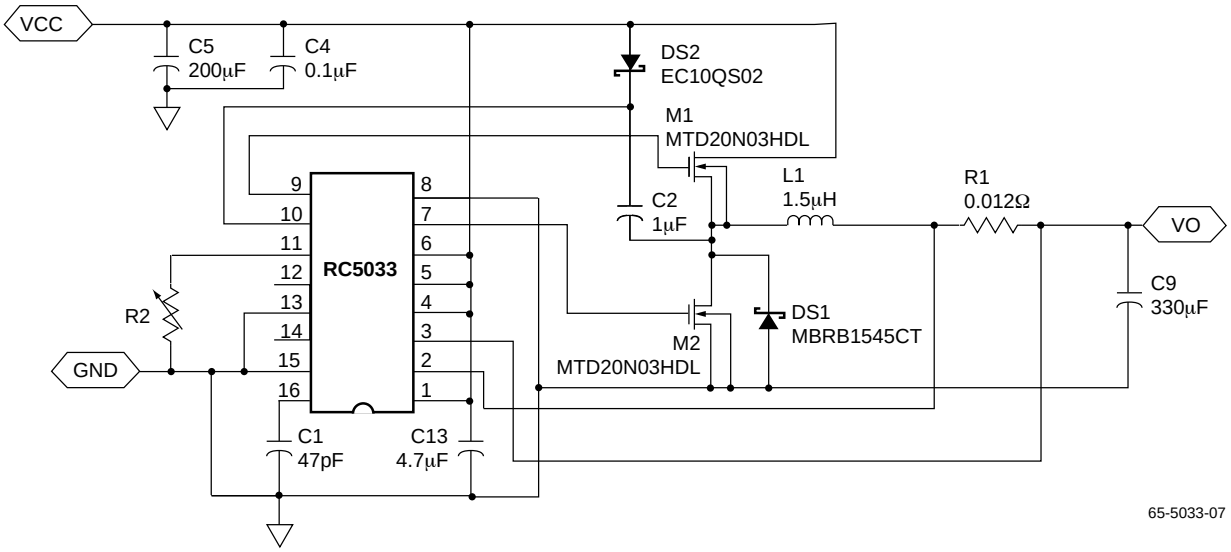


Figure 3. Adjustable Voltage DC-DC Converter

Preliminary Information

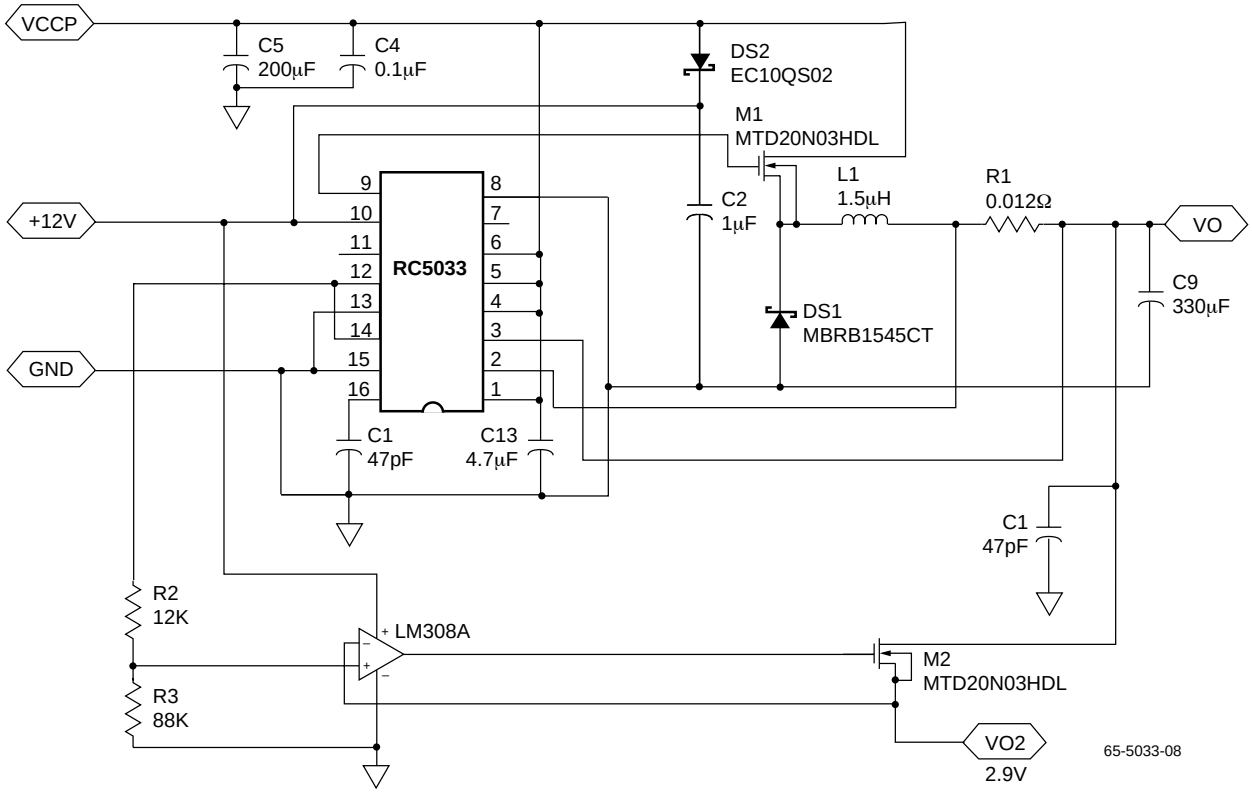
RC5033 Standard Application Circuit Bill of Materials			
Ref Designator	**Quantity**	**Part No.**	**Manufacturer**
L1	1	CDRH127-1R3NC	Sumida
M1,M2	2	MTD20N03HDL	Motorola
DS1	1	MBRB1545CT	Motorola
DS2	1	EC10QS02L	Nihon
R1	1	LRC-2512	IRC
C5	1	OS-CON 10SA220M	Sanyo
C9	1	OS-CON 10SA330M	Sanyo
C2	1	1uF	Monolithic ceramic Cap
C1	1	47pF	SMD Cap
C4	2	0.1uF	SMD Cap

Table 1. Components for RC5033

RC5033 Alternate Suppliers of Components			
Ref Designator	Quantity	Alternate Part No.	Alternate Manufacturer
L1	1	PE-53680	Pulse Engineering
M1,M2	2	2SK1388	Fuji
		IRLZ44N	International Rectifier
		Si4410DY	Temic (Siliconix)
DS1	1	C10T02QL	Nihon
		SR1620C	Rectron
DS2	1	MBRS140T3	Motorola
R1	1	WSL-2512	DALE
C5	1		
C9	1		

Table 2. Alternate Components Selection

Applications Discussion



Dual Power Supply Application

In some CPU power applications there may be a need for a split voltage converter. The circuit in Figure 4 addresses this need with only minimal component count. The basic RC5033 non-synchronous DC-DC converter is augmented with an op-amp, a power MOSFET, and some 1% resistors to provide a dual power supply with one voltage set to 3.3V and the other, slaved off of the 3.3V, set to 2.9V. In this configuration, the RC5033 converts the 5V to 3..3V with high efficiency. By using the op-amp, power FET, and the resistors, a low-dropout linear regulator is realized that can be run off of the 3.3V. The 2.9V linear regulator has a relatively high efficiency just due to the fact that the ratio of 2.9V/3.3V is close to 88%. The power FET is a low Rdson n-channel MOSFET, and thus it is reasonably inexpensive. The opamp can be a garden variety, though the input bias current and output slew rate need to be considered to optimize accuracy and transient response. The overall efficiency of this power supply system will very much depend upon the percentage of power used on each power output. Overall, the efficiency of this system will be lower than if both supplies were implemented as switchers; however, the added savings of the part count reduction may more than compensate for the overall lower efficiency.

Standard Application Circuit

The circuit shown in Figure 1 along with its components and values has been designed as representative of the typical application involving the RC5033 for a Pentium™ CPU. Use of the standard application circuit will deliver the performance curves shown under the Typical Operating Characteristics section of the data sheet. Many users will want to develop their own DC-DC converter solution that is uniquely tailored to a specific application requirement. In that case, the users should review the detailed information in the Design Procedure and Applications Information section of the data sheet.

Detailed Description

The RC5033 is a programmable voltage synchronous controller. When designed around the appropriate external components, it can be configured to deliver more than 10A of output current. During heavy loading conditions the RC5033 functions as a current-mode PWM step down regulator. Under light loading conditions, the regulator functions in the PFM or pulse skipping mode, thereby increasing its efficiency under light loads.

Main Control Loop

The main control loop of the regulator (see Block Diagram) contains two main blocks, the analog control block and the digital control block. The analog control block consists of signal conditioning amplifiers that feed into a set of fast comparators which provide the inputs to the digital control block. The signal conditioning block takes inputs from the IFB(current feedback) and VFB(voltage feedback) pins and then sets up two controlling signal paths. The voltage control path gains up the VFB signal and presents that signal to one of the summing amplifier inputs. The current control path takes the difference between the IFB and VFB pins and presents that signal to another input of the summing amplifier. These two signals are then summed together with the slope compensation input from the oscillator and the output is then presented to a comparator. This comparator provides the main PWM control signal to the digital control block.

There are three other comparators in the analog control block. The first two control the thresholds of where the RC5033 goes into its pulse skipping mode during light loads and the second controls the point at which the max current comparator disables the output drive signal to the upper power MOSFET. The third comparator determines when the synchronous mode bottom side power MOSFET will be enabled and disabled.

The digital controller section is designed to take the comparator inputs along with the main clock signal from the oscillator and provide the appropriate pulses to the HIDRV and LODRV output pins that will in turn control the external power MOSFETs. This digital section was designed in high speed schottky transistor logic which allows the RC5033 to clock up to speeds greater then 1MHz. This section is responsible for providing the break-before-make timing that ensures that both external FETs will not be on at the same time.

High Current Output Drivers

The RC5033 contains two identical high current output drivers. These drivers contain high speed bipolar transistors configured in a push-pull configuration. Each output driver is capable of pumping out 1A of current in less than 100ns. Each driver's power and ground are separated from the overall chip power and ground for added switching noise immunity. The HIDRV driver has a power supply, VCCQP, which can be either derived from an external voltage source or can be boot-strapped from a flying-capacitor as is shown in Figure 1. In the boot-strapped mode, C2 is alternately charged from VCC via the schottky diode DS2 and then boosted up when M1 is turned on. This provides a VCCQP voltage equal to 2*VCC - Vds(DS2); or about 9.5V with VCC=5V. This voltage is sufficient to provide the 9V gate drive to the external MOSFET that will be needed for achieving a low Rdson. Since the low side synchronous FET is referenced to ground, there is no need to boost the gate drive voltage and its VCCP power pin can just be tied to VCC.

Internal Reference

The reference in the RC5033 is a precision band-gap type reference. Its temperature coefficient is trimmed to provide a near zero TC. For applications that require a voltage other than the voltages provided by the fixed jumper connections, an external resistor will change the reference voltage from 2.0V up to 3.6V. For a guaranteed stable operation under all loading conditions, a 0.1μF capacitor is recommended on the VREF output pin.

Over -Voltage Protection

The RC5033 provides a constant monitor of the output voltage for over-voltage protection. Should the voltage at the VFB pin exceed 20% of the selected program voltage, then an overvoltage condition will be assumed to exist and the RC5033 will shut down the output drive signals to the power FETs.

Oscillator

The RC5033 oscillator is designed as a fixed current capacitor charging oscillator. An external capacitor allows for maximum flexibility in choosing the associated external components for the RC5033. The oscillator frequency con be set from less than 200KHz to over 1MHz depending on the application requirements.

Design Procedure and Applications Information

Simple Step-Down Converter

Figure 4 shows a step-down DC-to-DC Converter with no feedback controller. The derivation of the basic step-down converter will serve as a basis for the design equations for the RC5033 in Figure 1. In Figure 5, the basic operation begins by closing the switch, S1. When S1 is closed the input voltage VB is impressed across the inductor L1. The current flowing in the inductor is given by the following equation: IL=(VB- Vo)Ton/L; where Ton is the time duration for S1 to be closed. When S1 is open, the diode will conduct the inductor current and the output current will be delivered to the load according to the equation: IL=Vo(T – Ton)/L; where T- Ton is the time duration for S1 to be off. By solving these two equations we can arrive at the basic relationship for the output voltage of a step-down converter: Vo= VB(Ton/T).

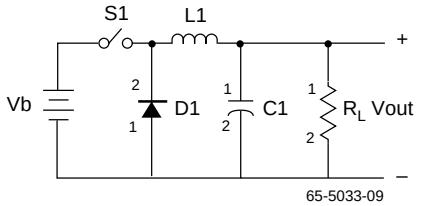


Figure 5. Simple Buck DC-DC Converter

Preliminary Information

Selecting the Inductor

The inductor is one of the most critical components to be selected in the DC-to-DC converter application. The critical parameters are inductance (L), max DC current (Imax), and the coil resistance (Rl). The inductor core material is a critical factor in determining the amount of current that the inductor will be able to handle. As with all engineering designs there are trade- offs for various types of inductor core materials. In general, Ferrites are popular because of their low cost, low EMI, and high frequency (>500kHz) characteristics. Molypermalloy powder (MPP) materials have good saturation characteristics and low EMI with low hysteresis losses; however they tend to be expensive and are more efficiently utilized at frequencies below 400kHz. DC winding resistance is another critical parameter. In general, the DC resistance should be kept as low as possible. The power loss in the DC resistance will degrade the efficiency of the converter by the relationship: Power Loss = (Io)2*Rl.

The value of the inductor is a function of the switching frequency (Ton) and the maximum inductor current. The max inductor current can be calculated from the relationship:

$$I_{MAX} = \frac{2I_L}{F_O T_{ON}\left(\frac{V_{IN}-V_{OUT}}{V_{OUT}-V_D}\right)+1}$$

Where: Fo is the desired clock frequency
Ton is the max on time of the M1 FET
Vd is the forward voltage of the schottky diode D1

Then the inductor value can be calculated with the relationship:

$$L = \frac{V_{IN}-V_{DSON}}{I_{MAX}}(T_{ON})$$

Where: Vdson is the voltage across the drain-source of the M1 FET when switched on.
(this can be calculated by RDSon * Imax)

Current-Sense Resistor

The current sense resistor will carry all of the peak current of the inductor. This current will be more than the designed for load current. The RC5033 will begin to limit the output current to the load by turning off the top-side FET driver when the voltage across the current-sense resistor exceeds 100mV. When this happens the output voltage will temporarily go out of regulation. As the voltage across the resistor becomes larger, the top-side FET will turn off more and more until the current limit value is reached and then the RC5033 will continuously deliver the limit current at a reduced output voltage level. To insure that load transient conditions do not momentarily cause deregulation of the output voltage, a 20% margin in the limit voltage is advisable. Thus the resistor should be set by the relationship:

R = 100 mV/ Ipeak

Where: Ipeak = Imax * 1.33

Since the value of the sense resistor is generally in the miliohm region, care should be taken in the layout of the PCB. Trace resistance can contribute significant errors. The traces to the IFB and VFB pins of the RC5033 should be Kelvin connected to the pads of the current-sense resistor as shown in the sample layout Figure 5. To minimize the influence of noise the two traces should be run next to each other and the pins should be bypassed with a .1uF to GND as close to the device pins as possible.

Filter Capacitors

Good ripple performance and transient response are functions of the filter capacitors. Since the 5V input for a PC motherboard can be located several inches away from the DC-to-DC converter, input capacitance can play an important role in the load transient response of the RC5033. In general, the higher the input capacitance, the more charge storage is available for improving the current transfer through the top-side FET. A good rule of thumb is that for each watt of output power that you wish to deliver, there should be around 10uF of input capacitance. Low “ESR” capacitors are best suited for this application and can have an influence on the converter’s efficiency. The input capacitor should be placed as close to the drain of the top-side FET as possible to reduce the effect of ringing that can be caused by large trace lengths.

The ESR rating of a capacitor is a difficult number to pin down. ESR or Equivalent Series Resistance, is defined at the resonant impedance of that capacitor. Since the capacitor is actually a complex impedance device having resistance, inductance and capacitance, it is quite natural for it to have an associated resonant frequency. As a rule, the lower the ESR, the better suited the capacitor is for use in switching power supply applications. Many capacitor manufacturers do not supply ESR data. A useful estimate of the ESR can be obtained with the following equation: ESR = Pd/2pfC. Where Pd is the capacitor’s dissipation factor and f is the frequency of measure and C is the capacitance in farads.

With this in mind, calculating the output capacitance correctly is crucial to the performance of the DC-to-DC converter. The output capacitor determines the overall loop stability, output voltage ripple, and the transient load response. The calculation uses the following equation:

$$C(\mu F) = \frac{T_{ON}\left(\frac{(V_{IN}-V_{OUT})I_{MAX}}{V_{OUT}}+I_L\right)}{V_r}$$

Where: Vr is the desired output ripple voltage

Schottky Diode Selection

The application circuit diagram shows two schottky diodes, DS1 and DS2. DS1 is used in parallel of M2 in order to prevent the lossy body diode in the FET from turning on. DS2 serves a dual purpose. As it is configured, it allows the VCCQP supply pin of the RC5033 to be bootstrapped up to

9V by using the bootstrap capacitor C2. When the lower FET M2 is turned on, one side of the capacitor C2 is connected to GND while the other side of the cap is being charged up through D2 to a voltage that is Vin - Vd. When the lower FET turns off and the upper one turns on, the voltage that is supplied to the VCCQP pin is 2Vin - Vd. The voltage then that is applied to the gate of the FET is VCCQP - Vsat, typically around 9V. It is important in the selection of DS1 and DS2 that they have a low forward voltage drop as this directly affects the regulator efficiency. The other job that DS2 performs is that of bootstrapping VCCQP during startup. It is possible to cause the output stage to latchup if the VCCQP supply is brought up before the other VCC supplies of the RC5033. It is therefore advisable that DS2 be connected even in applications that do not utilize the bootstrapping technique for VCCQP. An alternate application could tie the VCCQP supply pin to the +12V power supply in the PC, thus eliminating the need for C2 and forcing the Rdson of M1 even lower by increasing its Vgs.

MOSFET Switches

The MOSFET switches in the RC5033 applications circuit are N-channel “logic-level” FETs. This means that they will be fully on with a Vgs of 4V. Many manufacturers make logic-level FETs and the trick is to choose the one with the lowest RDSon at the given Imax current level. The value of RDSon directly enters into the efficiency equation as a power loss. Also influencing the efficiency is the gate charge of the FET and the clock frequency of the RC5033. At higher clocking rates the amount of charge needed to be delivered to the FET is going to lower the overall efficiency. In higher current applications, the upper FET can be paralleled to provide greater current capability; however, the lower FET doesn’t necessarily have to be doubled since it is on only a fraction of the time that the upper FET is on.

PCB Layout and Grounding

As is the case with most analog circuitry, good layout practices are necessary to achieve the optimum in the overall performance of the DC-to-DC converter. In general, it is always a good practice to have a tight layout that attempts to minimize short low inductance wiring to the RC5033.

The use of multilayer PCB is recommended. In particular, it is recommended to have a continuos ground plane beneath the circuit, 2oz copper would be preferred in high current applications. As was stated previously, the current-sense resistor, R1, should be located as close to the RC5033 as possible and the IFB and VFB traces should be Kelvin connected to the pads of R1. To minimize switching losses and noise, place M1, M2, L and DS2 as close together as possible. Also try to keep the HIDRV and LODRV gate drive signal traces as short as possible. It is recommended that the noisy switching part of the circuit be kept away from the low current pins on the chip such as IFB, VFB, ADJ3, ADJ1, and CEXT. Keep the 0.1uF bypass capacitors as close to the chip pins as possible. All of the ground pins should be connected to the ground plane directly under the chip. A sample layout is provided in Figure 6.

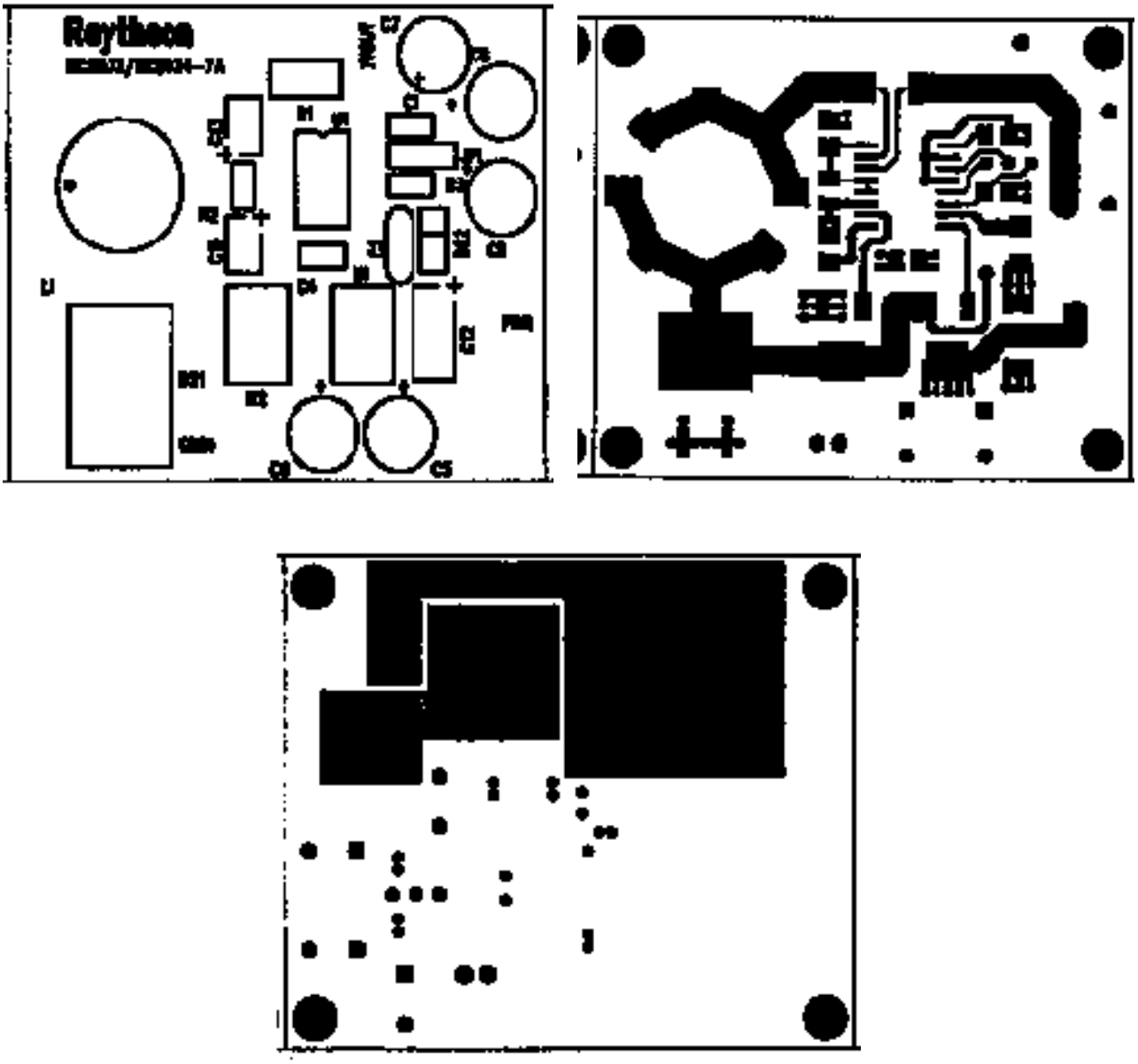


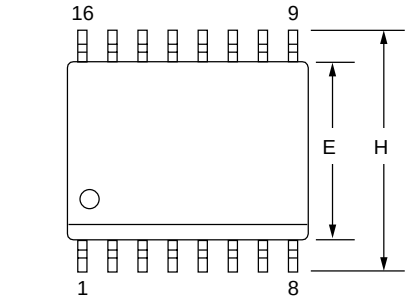
Figure 6. Sample PCB Layout

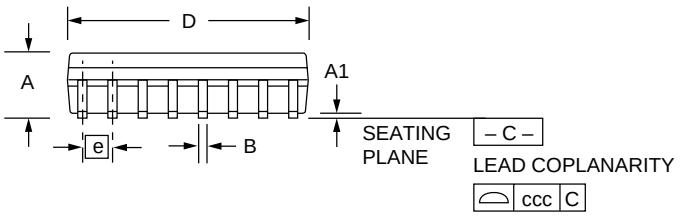
Mechanical Dimensions – 16-Lead SOIC Package

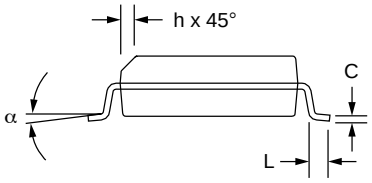
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.398	.413	10.10	10.50	2
E	.291	.299	7.40	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.020	0.25	0.51	
L	.016	.050	0.40	1.27	3
N	16		16		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Preliminary Information

Ordering Information

Product Number	Package	θJA
RC5033M	16 SOIC	85°C/W

Preliminary Information

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

5/20/98 0.0m 001
Stock#DS30005033

RC5034

High Accuracy Synchronous DC-DC Converter

Features

- Pentium™ VREF; 2% accuracy
- >85% Efficiency
- 350uA quiescent current in shutdown
- Fast transient response
- Soft control power-up
- Over-Voltage Protection
- Factory trimmed low TC reference voltage
- Adjustable oscillator frequency
- Drives N-Channel MOSFETs; to 1 MHz
- 16 pin SOIC package

Applications

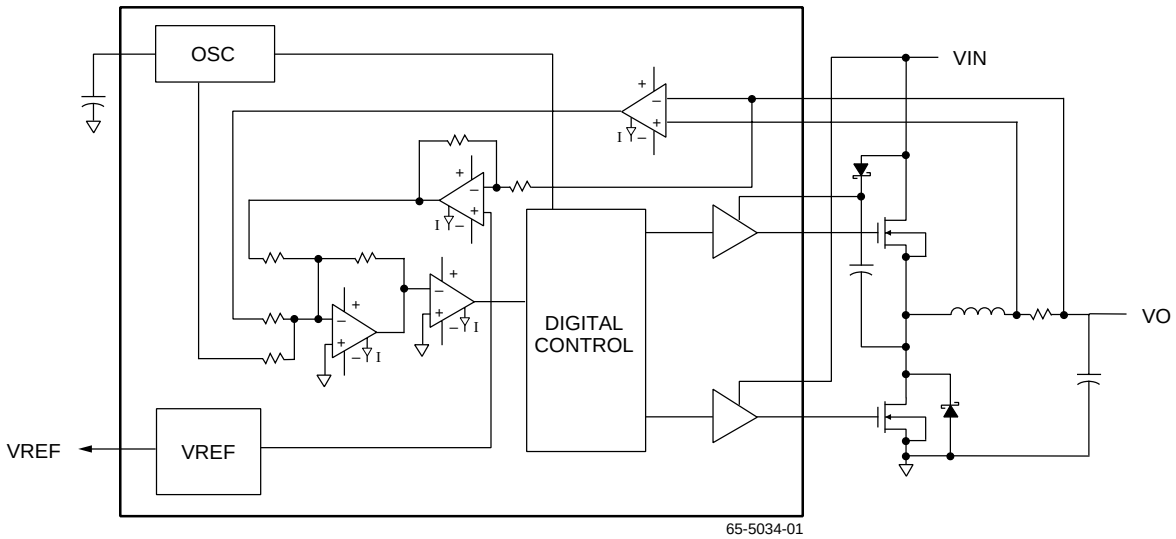
- 3.3V power supply for Pentium™ based CPUs requiring 2% VRE specification motherboards

Preliminary Information

Description

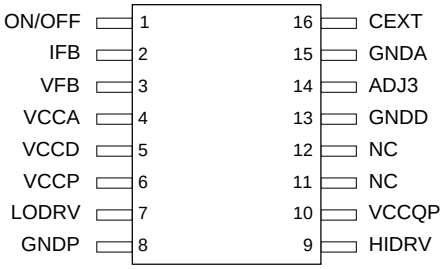
The RC5034 is a synchronous mode DC-DC controller IC dedicated to providing a 5V to 3.52V conversion for Pentium™ CPUs that require the 2% VRE voltage specification. It can be configured in both the synchronous and non-synchronous modes and with the proper applications circuitry can be used to deliver load current greater than 10 Amps. The RC5034 is designed to operate in a standard PWM control mode under heavy load conditions and as a PFM controller in light load conditions. Its highly accurate low TC reference eliminates the need for precision external components in order to achieve tight tolerance voltage regulation. An integrated Over-Voltage protection function constantly monitors the output voltage and shuts down the power to the CPU in the event of a out-of-tolerance voltage situation, thereby protecting the CPU. The programmable oscillator can operate from 200KHz to greater than 1MHz to provide for flexibility in choosing external components such as inductors, capacitors, and Power MOSFETs.

Block Diagram



65-5034-01

Pin Assignments



Pin Definitions

Pin Name	Pin Number	Pin Function Description
On/Off	1	A low level on this pin will power down; tie to VCCD if not used.
IFB	2	Current Feedback Input.
VFB	3	Voltage Feedback Input.
VCCA	4	Analog VCC.
VCCD	5	Digital VCC.
VCCP	6	VCC for synchronous FET output drivers.
LODRV	7	Synchronous FET driver output.
GNDP	8	Power ground for high current drivers.
HIDRV	9	High side FET driver output.
VCCQP	10	VCC for High side FET output driver
NC	11, 12	No Connections leave open
GNDD	13	Digital ground.
ADJ3	14	VREF
GNDA	15	Analog ground.
CEXT	16	External capacitor for setting oscillator frequency.

Preliminary Information

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Conditions	Min	Typ	Max	Units
V_{CCP}	Low Driver Supply				13	V
V_{CCQP}	High Driver Supply				13	V
T_J	Junction Temperature				175	°C
T_A	Ambient Operating Temperature		0		70	°C
T_S	Storage Temperature		-65		150	°C
T_L	Lead Soldering Temperature	(10 seconds)			300	°C

Note:

1. Functional operation under any of these conditions is NOT implied.

Operating Conditions

Parameter		Conditions	Min	Typ	Max	Units
V_{CC}	Supply Voltage		4.5	5	7	V
V_{CCP}	Low Driver Supply		4.5	5	7	V
V_{CCQP}	High Driver Supply		9		13	V
V_{IH}	Input Voltage, Logic HIGH		2			V
V_{IL}	Input Voltage, Logic LOW				0.8	V

DC Electrical Characteristics

(V_{CC} = 5V, fosc = 650 KHz, and T_A = +25˚C unless otherwise noted)

Parameter		Conditions	Min	Typ	Max	Units
V_O	Output Voltage	T_A = 0–70°C	3.45	3.52	3.6	V
I_O	Output Current	See Figure 1 for application		5		A
Vref Acc	Reference Acc			.15	1	%
VTC	Output Voltage TC			-40		ppm
LDR	Load Regulation	0.5 to 7A		0.25		%Vo
LIR	Line Regulation	V_{CC} = ±5%		0.1		%Vo
V_R	Output Voltage Ripple			15		mV
Cum Acc	Cumulative Accuracy[2]	T_A = 0–70°C		1	2.1	%
Eff	Efficiency	Synchronous mode > 2A	85	88		%
Iodr	Output Driver I	Open Loop	0.5	0.7		A
Pd	Power Dissipation			0.1	0.2	W

Notes:

1. Functional operation under any of these conditions is not implied. Performance is guaranteed only if Operating Conditions are not exceeded.
2. Output Voltage accuracy, Tempco, load regulation, ripple, and transient performance determine the Cumulative Accuracy.

AC Electrical Characteristics[1]

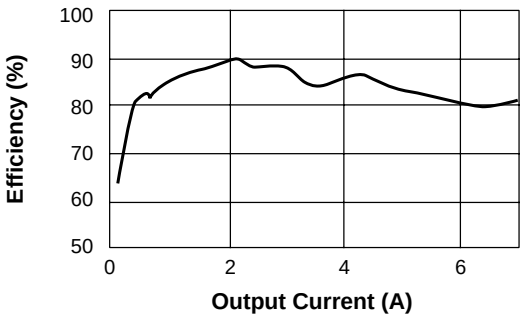
(V_{CC} = 5V, fosc = 650 KHz, and T_A = +25˚C unless otherwise noted)

Parameter		Conditions	Min	Typ	Max	Units
Tr	Response Time	Il=0.5A to 5.5A		10		µs
Fosc	Oscillator Range		0.2		1.2	MHz
Osc Acc	Fosc Accuracy			10		%
Dtc	Max Duty Cycle	PWM mode	90	95		%
Dtcm	Min Duty Cycle	PFM mode			100	ns
Imax	Imax Threshold			30		mV
Iscp	Short Circuit Prot			80		mV
Ovp	Over Voltage Prot			20		%Vo
Trimax	Response to Imax			15	30	ns
Tssp	Soft start response			10		µs

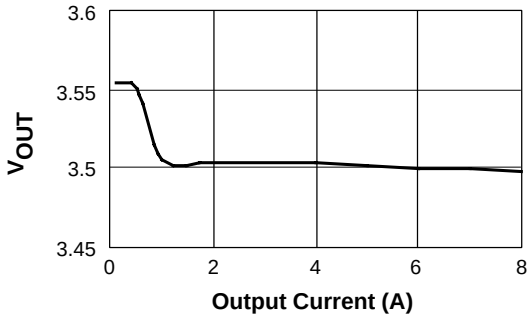
Preliminary Information

Typical Operating Characteristics[1]

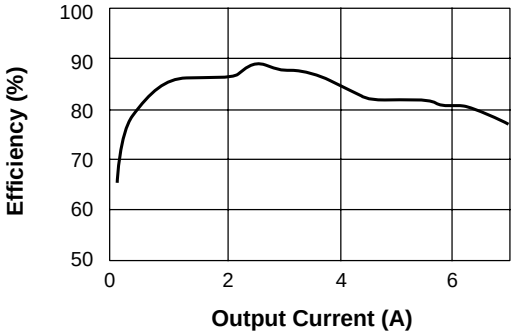
Efficiency vs Output Current (F_{OSC} = 400 KHz)



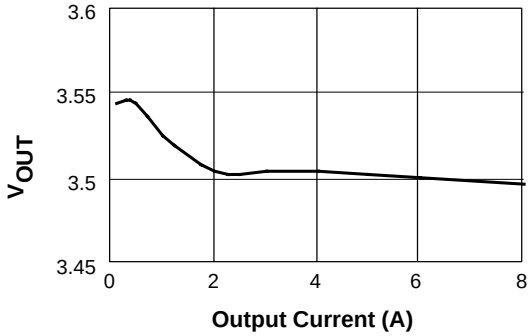
Load Regulation (F_{OSC} = 300 KHz)



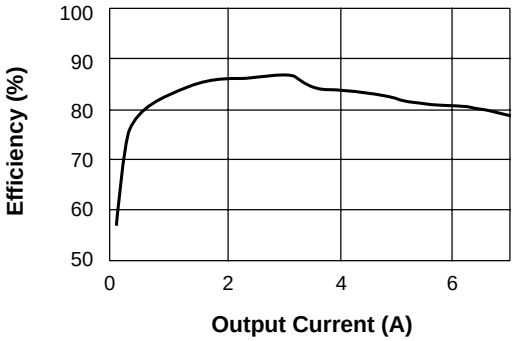
Efficiency vs Output Current (F_{OSC} = 650 KHz)



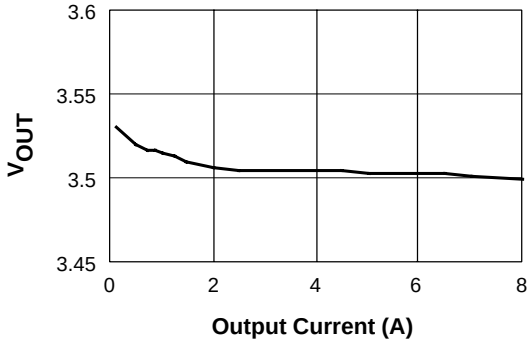
Load Regulation (F_{OSC} = 650 KHz)



Efficiency vs Output Current (F_{OSC} = 1 MHz)



Load Regulation (F_{OSC} = 1 MHz)



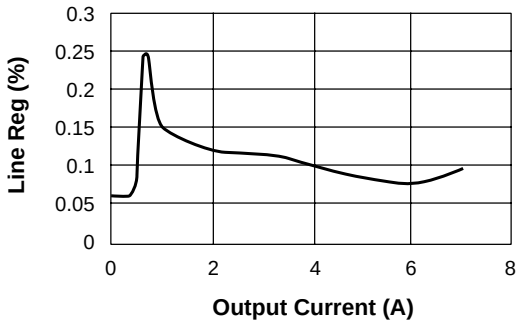
65-5034-03

Note:

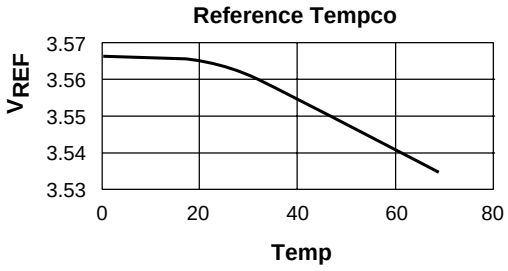
1. Data taken with circuit of Figure 1.

Typical Operating Characteristics (continued)

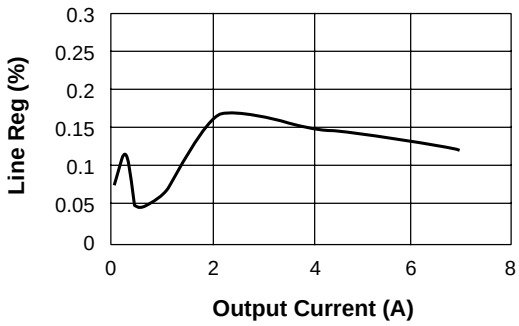
Line Regulation vs. Output Load (F_{OSC} = 400 KHz)



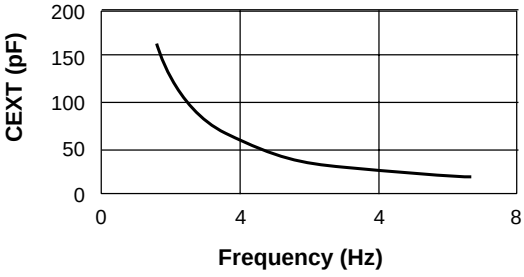
Reference Tempco



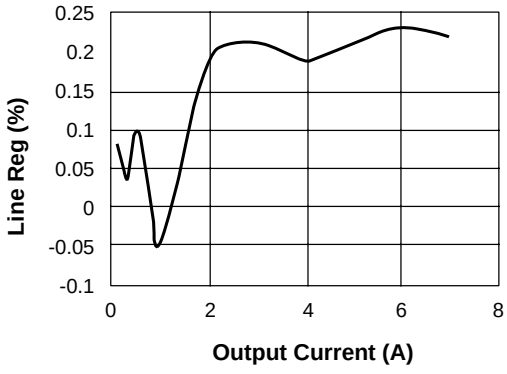
Line Regulation vs. Output Load (F_{OSC} = 650 KHz)



CEXT vs. Oscillator Frequency



Line Regulation vs. Output Load (F_{OSC} = 1 MHz)



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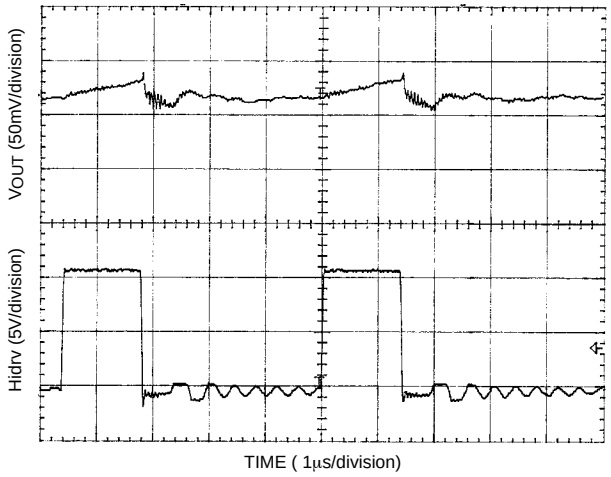
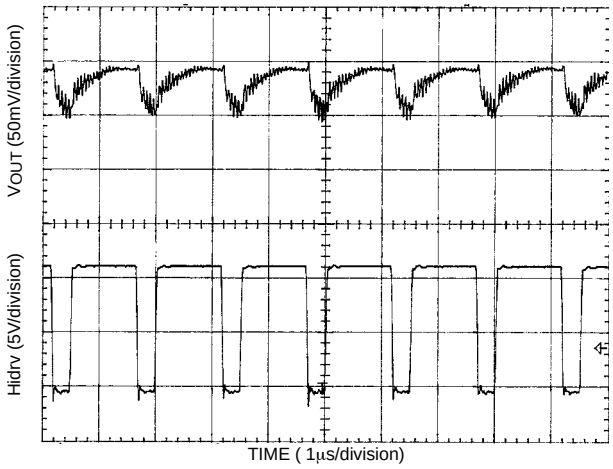
Preliminary Information

Preliminary Information

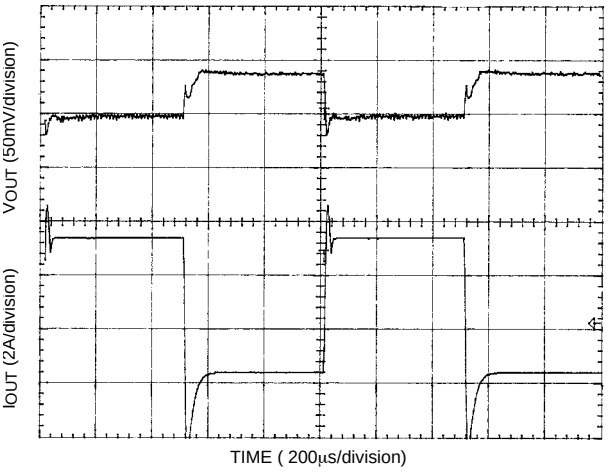
Typical Operating Characteristics (continued)



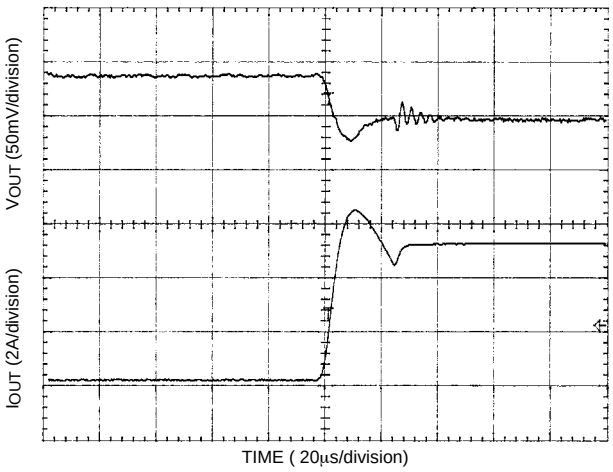
AC Ripple response .2A Load



AC Ripple response 5A Load



Transient Response .2A to 5A Load



Transient Response Magnified

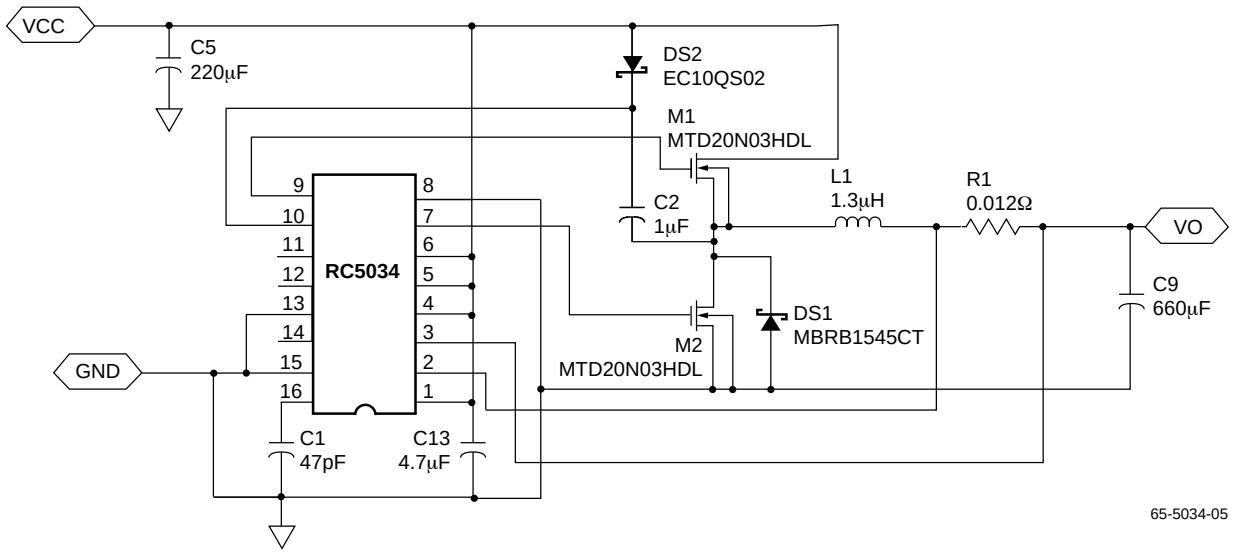


Figure 1. Synchronous 7A Schematic

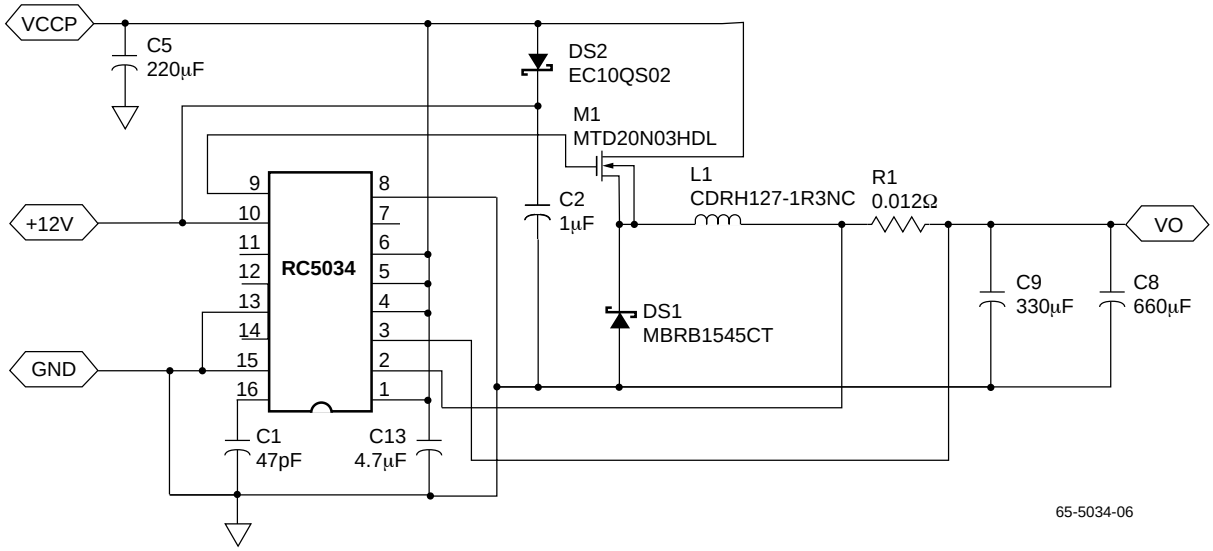


Figure 2. Non-Synchronous 7A Circuit

RC5034 Standard Application Circuit Bill of Materials			
Ref Designator	**Quantity**	**Part No.**	**Manufacturer**
L1	1	1.3 µH CDRH127-1R3NC	Sumida
M1,M2	2	MTD20N03HDL	Motorola
DS1	1	MBRB1545CT	Motorola
DS2	1	EC10QS02L	Nihon
R1	1	.012Ω LRC-2512	IRC
C5	1	220 µF OS-CON 10SA220M	Sanyo
C9	2	330 µF OS-CON 10SA330M	Sanyo
C2	1	1uF	Monolithic ceramic Cap
C1	1	47pF	SMD Cap
C4	2	0.1uF	SMD Cap
C13	1	4.7uF	SMD Cap

Table 1. Components for RC5034

RC5034 Alternate Suppliers of Components			
Ref Designator	Quantity	Alternate Part No.	Alternate Manufacturer
L1	1	1.3 µH PE-53680	Pulse Engineering
M1,M2	2	2SK1388	Fuji
		IRLZ44N	International Rectifier
		Si4410DY	Temic (Siliconix)
DS1	1	C10T02QL	Nihon
		SR1620C	Rectron
DS2	1	MBRS140T3	Motorola
R1	1	.012Ω WSL-2512	DALE

Table 2. Alternate Components Selection

Preliminary Information

Applications Discussion

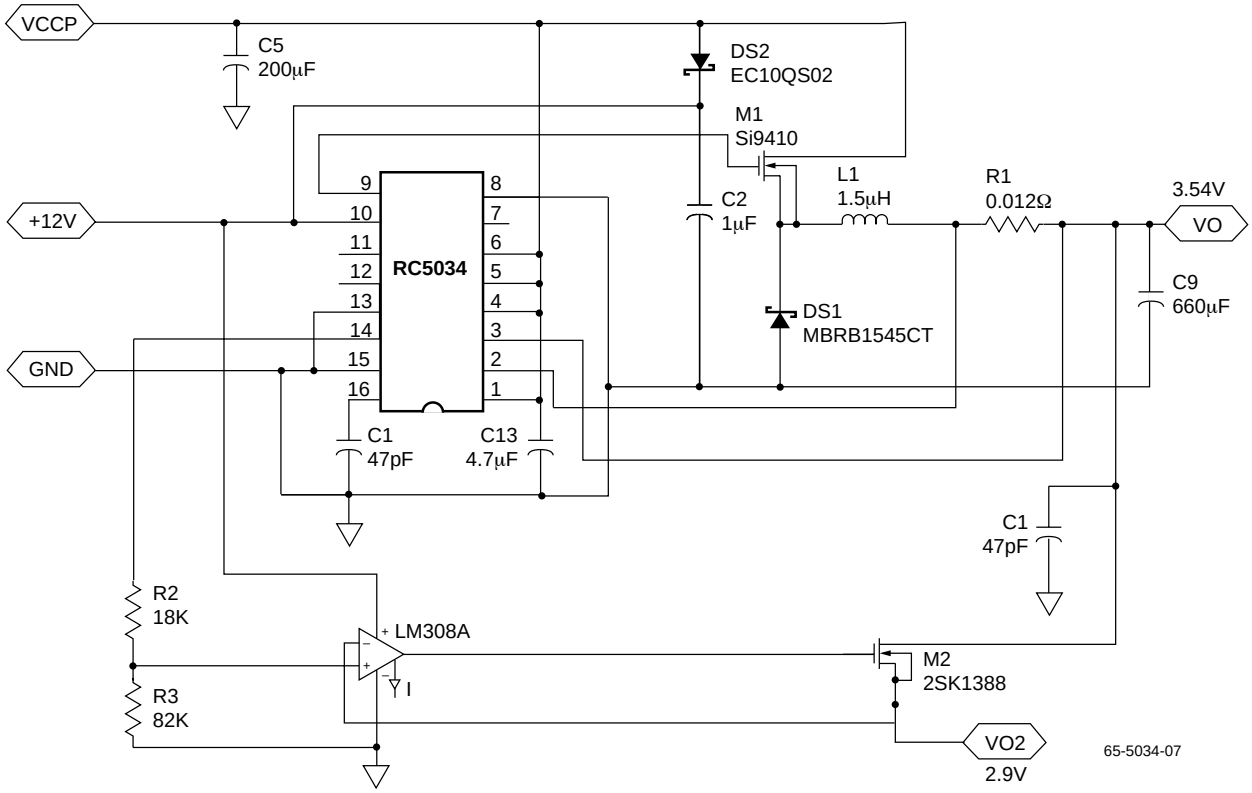


Figure 3. Dual Regulator Applications Circuit

Dual Power Supply Application

In some CPU power applications there may be a need for a split voltage converter. The circuit in Figure 3 addresses this need with only minimal component count. The basic RC5034 non-synchronous DC-DC converter is augmented with an op-amp, a power MOSFET, and some 1% resistors to provide a dual power supply with one voltage set to 3.5V and the other, slaved off of the 3.5V, set to 2.9V. In this configuration, the RC5034 converts the 5V to 3.5V with high efficiency. By using the op-amp, power FET, and the resistors, a low-dropout linear regulator is realized that can be run off of the 3.5V. The 2.9V linear regulator has a relatively high efficiency just due to the fact that the ratio of 2.9V/3.5V is close to 88%. The power FET is a low Rdson n-channel MOSFET, and thus it is reasonably inexpensive. The opamp can be a garden variety, though the input bias current and output slew rate need to be considered to optimize accuracy and transient response. The overall efficiency of this power supply system will very much depend upon the percentage of power used on each power output. Overall, the efficiency of this system will be lower than if both supplies were implemented as switchers; however, the added savings of the part count reduction may more than compensate for the overall lower efficiency.

Standard Application Circuit

The circuit shown in Figure 1 along with its components and values has been designed as representative of the typical application involving the RC5034 for a Pentium™ CPU. Use of the standard application circuit will deliver the performance curves shown under the Typical Operating Characteristics section of the data sheet. Many users will want to develop their own DC-DC converter solution that is uniquely tailored to a specific application requirement. In that case, the users should review the detailed information in the Design Procedure and Applications Information section of the data sheet.

Detailed Description

The RC5034 is a programmable voltage synchronous controller. When designed around the appropriate external components, it can be configured to deliver more than 10A of output current. During heavy loading conditions the RC5034 functions as a current-mode PWM step down regulator. Under light loading conditions, the regulator functions in the PFM or pulse skipping mode, thereby increasing its efficiency under light loads.

Main Control Loop

The main control loop of the regulator (see Block Diagram) contains two main blocks, the analog control block and the digital control block. The analog control block consists of signal conditioning amplifiers that feed into a set of fast comparators which provide the inputs to the digital control block. The signal conditioning block takes inputs from the IFB(current feedback) and VFB(voltage feedback) pins and then sets up two controlling signal paths. The voltage control path gains up the VFB signal and presents that signal to one of the summing amplifier inputs. The current control path takes the difference between the IFB and VFB pins and presents that signal to another input of the summing amplifier. These two signals are then summed together with the slope compensation input from the oscillator and the output is then presented to a comparator. This comparator provides the main PWM control signal to the digital control block.

There are three other comparators in the analog control block. The first two control the thresholds of where the RC5034 goes into its pulse skipping mode during light loads and the second controls the point at which the max current comparator disables the output drive signal to the upper power MOSFET. The third comparator determines when the synchronous mode bottom side power MOSFET will be enabled and disabled.

The digital controller section is designed to take the comparator inputs along with the main clock signal from the oscillator and provide the appropriate pulses to the HIDRV and LODRV output pins that will in turn control the external power MOSFETs. This digital section was designed in high speed schottky transistor logic which allows the RC5034 to clock up to speeds greater then 1MHz. This section is responsible for providing the break-before-make timing that ensures that both external FETs will not be on at the same time.

High Current Output Drivers

The RC5034 contains two identical high current output drivers. These drivers contain high speed bipolar transistors configured in a push-pull configuration. Each output driver is capable of pumping out 1A of current in less than 100ns. Each driver's power and ground are separated from the overall chip power and ground for added switching noise immunity. The HIDRV driver has a power supply, VCCQP, which can be either derived from an external voltage source or can be boot-strapped from a flying-capacitor as is shown in Figure 1. In the boot-strapped mode, C2 is alternately charged from VCC via the schottky diode DS2 and then boosted up when M1 is turned on. This provides a VCCQP voltage equal to 2*VCC - Vds(DS2); or about 9.5V with VCC=5V. This voltage is sufficient to provide the 9V gate drive to the external MOSFET that will be needed for achieving a low Rdson. Since the low side synchronous FET is referenced to ground, there is no need to boost the gate drive voltage and its VCCP power pin can just be tied to VCC.

Internal Reference

The reference in the RC5034 is a precision band-gap type reference. Its temperature coefficient is trimmed to provide a near zero TC. For a guaranteed stable operation under all loading conditions, a 0.1µF capacitor is recommended on the VREF output pin.

Over -Voltage Protection

The RC5034 provides a constant monitor of the output voltage for over-voltage protection. Should the voltage at the VFB pin exceed 20% of the selected program voltage, then an overvoltage condition will be assumed to exist and the RC5034 will shut down the output drive signals to the power FETs.

Oscillator

The RC5034 oscillator is designed as a fixed current capacitor charging oscillator. An external capacitor allows for maximum flexibility in choosing the associated external components for the RC5034. The oscillator frequency can be set from less than 200KHz to over 1MHz depending on the application requirements.

Design Procedure and Applications Information

Simple Step-Down Converter

Figure 4 shows a step-down DC-to-DC Converter with no feedback controller. The derivation of the basic step-down converter will serve as a basis for the design equations for the RC5034 in Figure 1. In Figure 4, the basic operation begins by closing the switch, S1. When S1 is closed the input voltage VB is impressed across the inductor L1. The current flowing in the inductor is given by the following equation: IL=(VB- Vo)Ton/L; where Ton is the time duration for S1 to be closed. When S1 is open, the diode will conduct the inductor current and the output current will be delivered to the load according to the equation: IL=Vo(T – Ton)/L; where T- Ton is the time duration for S1 to be off. By solving these two equations we can arrive at the basic relationship for the output voltage of a step-down converter: Vo=VB(Ton/T).

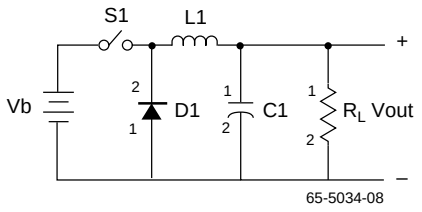


Figure 4. Simple Buck DC-DC Converter

Preliminary Information

Selecting the Inductor

The inductor is one of the most critical components to be selected in the DC-to-DC converter application. The critical parameters are inductance (L), max DC current (Imax), and the coil resistance (Rl). The inductor core material is a critical factor in determining the amount of current that the inductor will be able to handle. As with all engineering designs there are trade- offs for various types of inductor core materials. In general, Ferrites are popular because of their low cost, low EMI, and high frequency (>500kHz) characteristics. Molypermalloy powder (MPP) materials have good saturation characteristics and low EMI with low hysteresis losses; however they tend to be expensive and are more efficiently utilized at frequencies below 400kHz. DC winding resistance is another critical parameter. In general, the DC resistance should be kept as low as possible. The power loss in the DC resistance will degrade the efficiency of the converter by the relationship: Power Loss = (Io)2*Rl.

The value of the inductor is a function of the switching frequency (Ton) and the maximum inductor current. The max inductor current can be calculated from the relationship:

$$I_{MAX} = \frac{2I_L}{F_O T_{ON}\left(\frac{V_{IN}-V_{OUT}}{V_{OUT}-V_D}\right)+1}$$

Where: Fo is the desired clock frequency
Ton is the max on time of the M1 FET
Vd is the forward voltage of the schottky diode D1

Then the inductor value can be calculated with the relationship:

$$L = \frac{V_{IN}-V_{DSON}}{I_{MAX}}(T_{ON})$$

Where: Vdson is the voltage across the drain-source of the M1 FET when switched on.
(this can be calculated by RDSon * Imax)

Current-Sense Resistor

The current sense resistor will carry all of the peak current of the inductor. This current will be more than the designed for load current. The RC5034 will begin to limit the output current to the load by turning off the top-side FET driver when the voltage across the current-sense resistor exceeds 100mV. When this happens the output voltage will temporarily go out of regulation. As the voltage across the resistor becomes larger, the top-side FET will turn off more and more until the current limit value is reached and then the RC5034 will continuously deliver the limit current at a reduced output voltage level. To insure that load transient conditions do not momentarily cause deregulation of the output voltage, a 20% margin in the limit voltage is advisable. Thus the resistor should be set by the relationship:

R = 100 mV/ Ipeak

Where: Ipeak = Imax * 1.33

Since the value of the sense resistor is generally in the miliohm region, care should be taken in the layout of the PCB. Trace resistance can contribute significant errors. The traces to the IFB and VFB pins of the RC5034 should be Kelvin connected to the pads of the current-sense resistor as shown in the sample layout Figure 5. To minimize the influence of noise the two traces should be run next to each other and the pins should be bypassed with a .1uF to GND as close to the device pins as possible.

Filter Capacitors

Good ripple performance and transient response are functions of the filter capacitors. Since the 5V input for a PC motherboard can be located several inches away from the DC-to-DC converter, input capacitance can play an important role in the load transient response of the RC5034. In general, the higher the input capacitance, the more charge storage is available for improving the current transfer through the top-side FET. A good rule of thumb is that for each watt of output power that you wish to deliver, there should be around 10uF of input capacitance. Low “ESR” capacitors are best suited for this application and can have an influence on the converter’s efficiency. The input capacitor should be placed as close to the drain of the top-side FET as possible to reduce the effect of ringing that can be caused by large trace lengths.

The ESR rating of a capacitor is a difficult number to pin down. ESR or Equivalent Series Resistance, is defined at the resonant impedance of that capacitor. Since the capacitor is actually a complex impedance device having resistance, inductance and capacitance, it is quite natural for it to have an associated resonant frequency. As a rule, the lower the ESR, the better suited the capacitor is for use in switching power supply applications. Many capacitor manufacturers do not supply ESR data. A useful estimate of the ESR can be obtained with the following equation: ESR = Pd/2pfC. Where Pd is the capacitor’s dissipation factor and f is the frequency of measure and C is the capacitance in farads.

With this in mind, calculating the output capacitance correctly is crucial to the performance of the DC-to-DC converter. The output capacitor determines the overall loop stability, output voltage ripple, and the transient load response. The calculation uses the following equation:

$$C(\mu F) = \frac{T_{ON}\left(\frac{(V_{IN}-V_{OUT})I_{MAX}}{V_{OUT}}+I_L\right)}{V_r}$$

Where: Vr is the desired output ripple voltage

Schottky Diode Selection

The application circuit diagram shows two schottky diodes, DS1 and DS2. DS1 is used in parallel of M2 in order to prevent the lossy body diode in the FET from turning on. DS2 serves a dual purpose. As it is configured, it allows the VCCQP supply pin of the RC5034 to be bootstrapped up to 9V by using the bootstrap capacitor C2. When the lower FET

M2 is turned on, one side of the capacitor C2 is connected to GND while the other side of the cap is being charged up through D2 to a voltage that is Vin - Vd. When the lower FET turns off and the upper one turns on, the voltage that is supplied to the VCCQP pin is 2Vin - Vd. The voltage then that is applied to the gate of the FET is VCCQP - Vsat, typically around 9V. It is important in the selection of DS1 and DS2 that they have a low forward voltage drop as this directly affects the regulator efficiency. The other job that DS2 performs is that of bootstrapping VCCQP during startup. It is possible to cause the output stage to latchup if the VCCQP supply is brought up before the other VCC supplies of the RC5034. It is therefore advisable that DS2 be connected even in applications that do not utilize the bootstrapping technique for VCCQP. An alternate application could tie the VCCQP supply pin to the +12V power supply in the PC, thus eliminating the need for C2 and forcing the Rdson of M1 even lower by increasing its Vgs.

MOSFET Switches

The MOSFET switches in the RC5034 applications circuit are N-channel “logic-level” FETs. This means that they will be fully on with a Vgs of 4V. Many manufacturers make logic-level FETs and the trick is to choose the one with the lowest RDSon at the given Imax current level. The value of RDSon directly enters into the efficiency equation as a power loss. Also influencing the efficiency is the gate charge of the FET and the clock frequency of the RC5034. At higher clocking rates the amount of charge needed to be delivered to the FET is going to lower the overall efficiency. In higher current applications, the upper FET can be paralleled to provide greater current capability; however, the lower FET doesn’t necessarily have to be doubled since it is on only a fraction of the time that the upper FET is on.

PCB Layout and Grounding

As is the case with most analog circuitry, good layout practices are necessary to achieve the optimum in the overall performance of the DC-to-DC converter. In general, it is always a good practice to have a tight layout that attempts to minimize short low inductance wiring to the RC5034.

The use of multilayer PCB is recommended. In particular, it is recommended to have a continuos ground plane beneath the circuit, 2oz copper would be preferred in high current applications. As was stated previously, the current-sense resistor, R1, should be located as close to the RC5034 as possible and the IFB and VFB traces should be Kelvin connected to the pads of R1. To minimize switching losses and noise, place M1, M2, L and DS2 as close together as possible. Also try to keep the HIDRV and LODRV gate drive signal traces as short as possible. It is recommended that the noisy switching part of the circuit be kept away from the low current pins on the chip such as IFB, VFB, ADJ3, ADJ1, and CEXT. Keep the 0.1uF bypass capacitors as close to the chip pins as possible. All of the ground pins should be connected to the ground plane directly under the chip. A sample layout is provided in Figure 5.

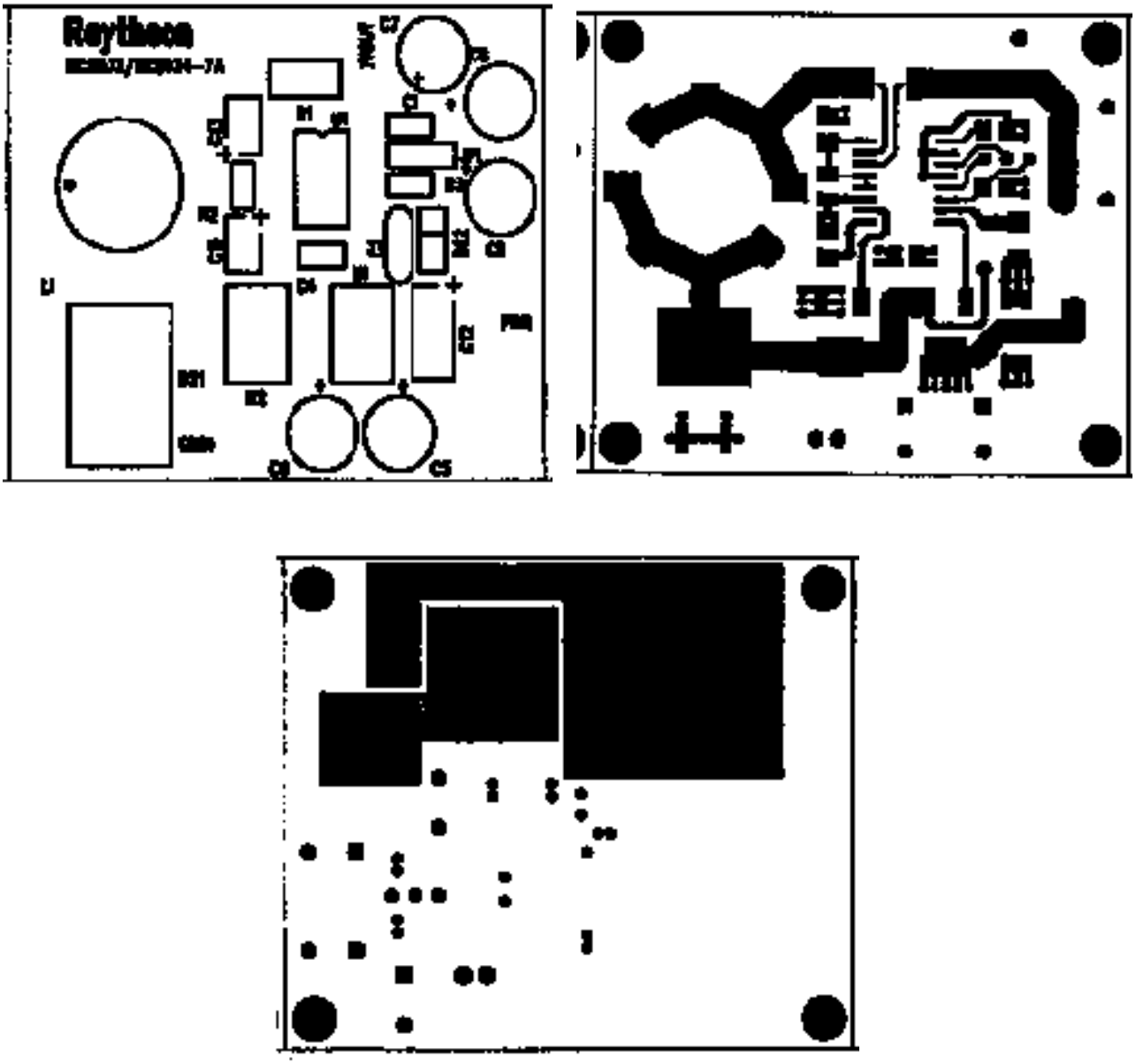


Figure 5. Sample PCB Layout

Notes:

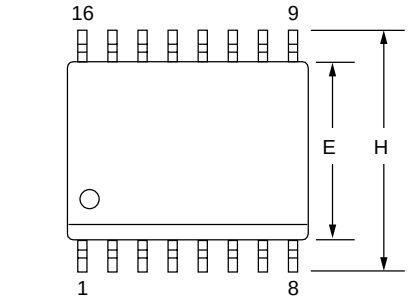
Notes:

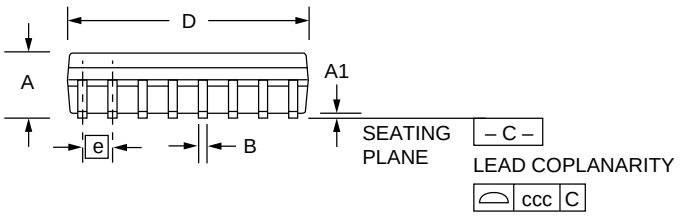
Mechanical Dimensions – 16 Lead SOIC Package

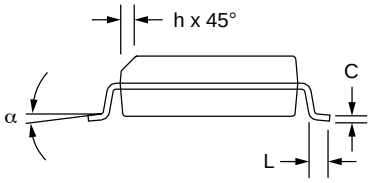
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.398	.413	10.10	10.50	2
E	.291	.299	7.40	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.020	0.25	0.51	
L	.016	.050	0.40	1.27	3
N	16		16		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Preliminary Information

Ordering Information

Product Number	Package	θJA
RC5034M	16 SOIC	85°C/W

Preliminary Information

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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RC5035A

Dual Precision Voltage Regulators

Features

- Combines switching regulator and low dropout linear regulator in single chip
- Enable function switches from single to dual output mode
- Overvoltage and short circuit protection
- Drives N-Channel MOSFETs
- Precision trimmed low TC voltage reference
- Soft start control during power-up
- 88% Efficiency for switching regulator
- 16 pin SOIC package

Applications

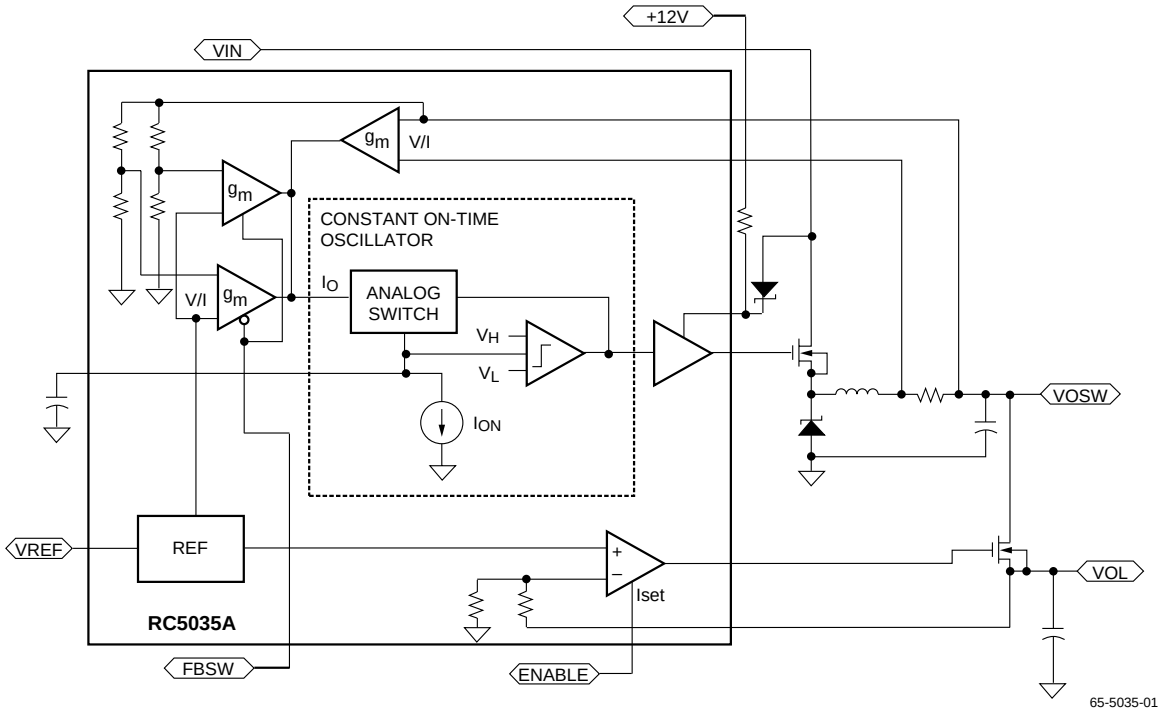
- Switchable single/dual power supply for Pentium® P54C/ P55C flexible motherboard implementation

Advanced Information

Description

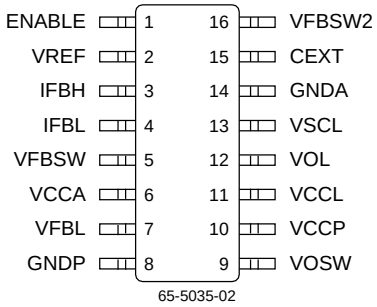
The RC5035 combines a switch-mode DC-DC converter with a low-drop-out linear regulator providing a 5V to 3.3V and 2.8V conversion for CPUs that require split power supplies. It can be configured with the proper applications circuitry to deliver load currents greater than 10 Amps. The RC5035 is designed to operate in a “constant on-time” (patent pending) control mode under all load conditions. Its highly accurate low TC reference eliminates the need for precision external components in order to achieve tight tolerance voltage regulation. Using on-chip precision resistors, the RC5035A can generate the accurate output voltages required by Intel and Cyrix processors. The programmable oscillator can operate up to1MHz for flexibility in choosing external components such as inductors, capacitors, and Power MOSFETs. Short circuit current protection is provided on both the switch mode as well as the linear regulator.

Block Diagram



Rev. 0.5.0

Pin Assignments



Pin Function Description

Pin Number	Pin Name	Pin Function Description
1	ENABLE	Linear regulator enable/V_{OSW} voltage selection
2	V_{REF}	Voltage reference output
3	IF_{BH}	High side current feedback for switching regulator
4	IF_{BL}	Low side current feedback for switching regulator
5	V_{FBSW}	Voltage feedback for switching regulator
6	V_{CCA}	Analog Input supply; Nominally 5V
7	V_{FBL}	Voltage feedback for linear regulator
8	GNDP	Power ground for high current drivers
9	V_{OSW}	FET driver output for switching regulator
10	V_{CCP}	Input supply for FET output driver; see figures 1,2 for typical connection
11	V_{CCL}	Input supply for linear regulator; Nominally 12V
12	V_{OL}	Linear regulator op-amp output
13	V_{SCL}	Short circuit current sense input for linear regulator
14	GNDA	Analog ground
15	C_{EXT}	External capacitor for setting oscillator frequency of switching regulator
16	V_{FBSW2}	Secondary voltage feedback for switching regulator

Advanced Information

Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Control Supply Voltages, V_{CCA}, V_{CCL}			13	V
Output Driver Supply Voltage, VC_{CP}			13	V
Junction Temperature, T_J			+175	˚C
Storage Temperature, T_S	-65		+150	˚C
Lead Soldering Temperature, 10 seconds			300	˚C

Note:

1. Functional operation under any of these conditions is not implied. Performance is guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter	Conditions	Min	Typ	Max	Units
Analog Supply Voltage, V_{CCA}		4.75	5	5.25	V
Linear Supply Voltage, V_{CCL}			12		V
Driver Supply Voltage, V_{CCP}			9	12	V
ENABLE HIGH threshold	Linear Regulator OFF	2.0			V
ENABLE LOW theshold	Linear regulator ON			0.8	V
Ambient Temperature, T_A		0		70	°C

DC Electrical Characteristics – Switch-Mode Regulator

(VCCA = 5V, VCCL = 12V, TA = 0–70°C using circuit of figure 1, unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
Output Voltage, V_{OSW}		1.5		3.6	V
Output Current, I_{SW}			8	10	A
Setpoint Accuracy	Vref = 1.5V, I_{SW}=3.5A		0.5	1	%
Output Temperature Drift, TC	T_A = 0–70°C		24		ppm
Load Regulation	I_{SW} = 0.5A to 3.5A or 3.5A to 7A		0.6		%Vo
Load Regulation	I_{SW} = 0.5A to 3.5A or 3.5A to 8.5A		1.0		%Vo
Line Regulation	V_{CCA} = 5V ±5%		0.03		%Vo
Output Ripple, peak-peak	20MHz BW, I_{SW}=8A		20		mV
Cumulative Accuracy[1]	T_A = 0–70°C		2.0	2.9	%
Efficiency	I_{SW} = 3.5A		88		%
Output Driver Current	Open Loop		0.7		A
Short Circuit Protection Threshold	Rsense = .006Ω		18		A
Power Dissipation	No external components		0.1		W
Thermal Impedance, θ_{JA}			80		˚C/W

Note:

1. Cumulative accuracy includes Setpoint Accuracy, Temperature drift, line and load regulation, ripple and transient performance.

Advanced Information

DC Electrical Characteristics – Linear Regulator

(V_{CCA} = 5V,V_{CCL} = 12V, TA = 0–70°C using circuit in figure 1, unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
Output Voltage, V_{OL}		1.5		3.6	V
Output Current, I_L			3	5	A
Setpoint Accuracy	Vref = 1.5V, I_L=0.5A		0.5	1	%
Output Temperature Drift, TC	T_A = 0–70°C		24		ppm
Load Regulation	I_L = 0.5A to 3A		0.3		%Vo
Line Regulation	V_{CCL} = 5V ±5%		0.03		%Vo
Output Noise	0.1 to 20KHz		1		mV
Cumulative Accuracy[1]			2		%
Crosstalk[2]	I_{SW}=5A		35		mV
Short Circuit Current	Rsense = .005Ω		5		A
Op-amp Output Current			10		mA
Power Dissipation	No external components		110		mW

Note:

1. Cumulative accuracy includes Setpoint Accuracy, Temperature drift, line and load regulation, ripple and transient performance.
2. Crosstalk is defined as the amount of switching noise from the switched-mode regulator that appears on the output of the linear regulator when both outputs are in a static load condition.

AC Electrical Characteristics Switch Mode Regulator

(V_{CCA} = 5V, V_{CCL} = 12V, T_A = 0-70°C using circuit of figure 1, unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
Response Time	I_{SW} = 0.5A to 8A		10		μs
Oscillator Range	C_{EXT} = 50pF	0.2		1	MHz
Minimum On Time			2		us
Response time to short circuit			15	30	us
Soft start response time			100		us

Advanced Information

Application Information

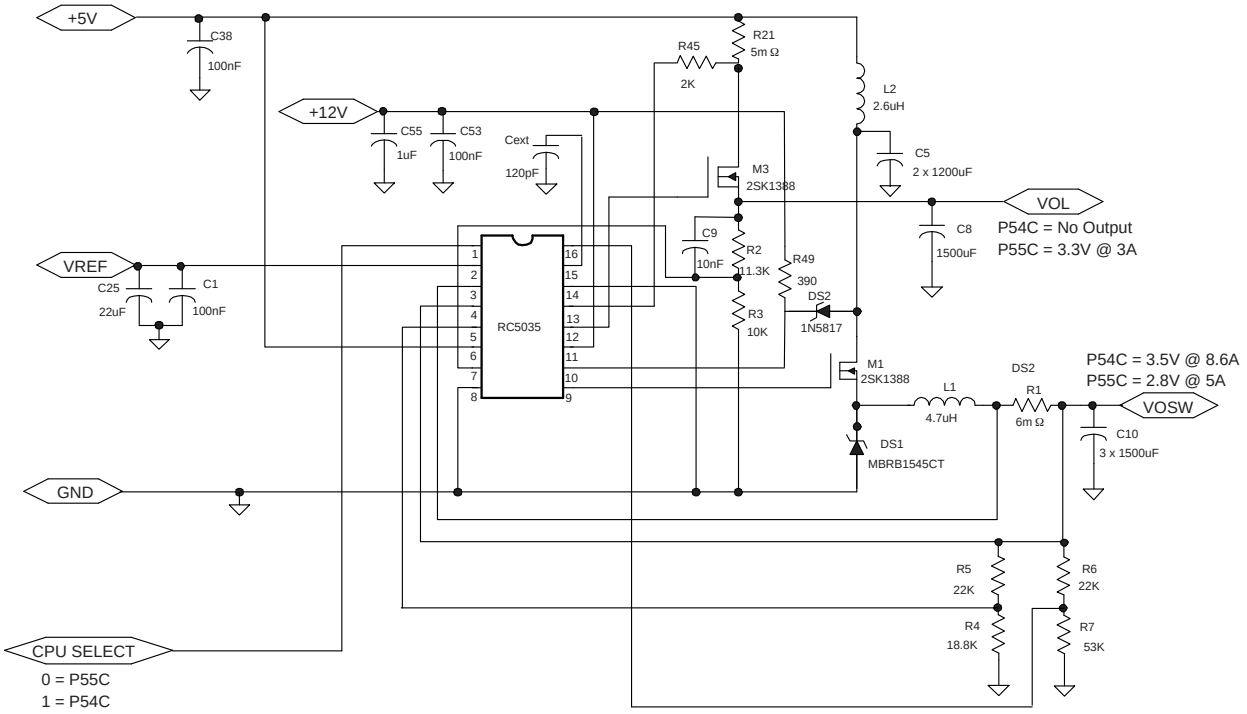


Figure 1: P54C/P55C Single/Dual Output Application Schematic

Table 1. RC5035 P54C/P55C Application Bill of Materials

Ref	Quantity	Part No.	Manufacturer
1	L1	4.7μF	Inductor
2	M1, M3	2SK1388	N-Channel Power MOSFET
1	DS1	MBRB1545CT	Schottky-Motorola, 10A
1	DS2	1N5817	Schottky-General Instruments
3	C1, C38, C53	100nF	Chip Cap
3	C5, C8	6MV1500GX	Sanyo 1500μF Electrolytic, ESR=44mΩ
1	C9	10nF	Chip Cap
3	C10	6MV1500GX	Sanyo 1500μF Electrolytic, ESR=44mΩ
1	C25	22μF	Tantalum Cap
1	C55	1μF	Tantalum Cap
1	Cext	120pF	Chip Cap
1	R1	0.006	MnCu Jumper
1	R2	22K	1% Resistor
1	R3	18.33K	1% Resistor
2	R4, R4S	33K	0.1% Resistor
1	R5	22K	0.1% Resistor
1	R21	0.005K	MnCu Jumper
1	L2	2.6μH	Inductor

Advanced Information

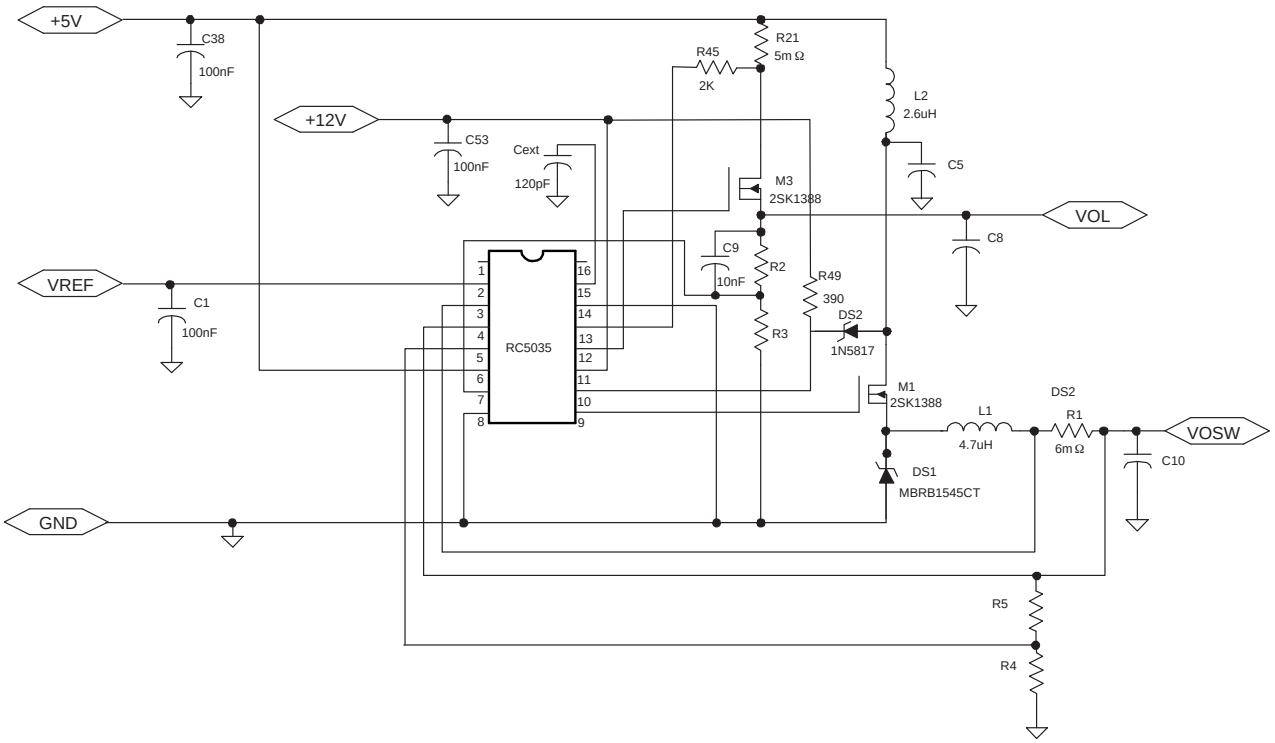


Figure 2. Dual Power Supply Application Schematic

Advanced Information

Dual Power Supply Application

Some CPU power applications such as the Intel Pentium® P55C will require separate voltages for the CPU core and I/O circuitry. Currently, the voltage requirements for this processor are 2.8V for the CPU core and 3.3V for the I/O circuitry. The circuit in figure 1 addresses this requirement using a minimum of external components. The RC5035 includes an internal operational amplifier that can be combined with an external N-channel power MOSFET and 1% resistors (see Design Equations) to form a second power supply. In this configuration, both the switched-mode and linear power supplies can be programmed between 2.0V and 3.6V to meet a variety of dual voltage requirements. In the circuit configuration of figure 1, the switched-mode portion is used for the 5V to 2.8V conversion for the CPU core to realize the optimal package efficiency. The op-amp, power FET and resistors are combined to generate the 3.3V required by the I/O power plane.

Analysis of the linear regulator portion from an efficiency standpoint reveals that for a 5V to 3.3V conversion, the efficiency is roughly 3.3/5, or 66%. For loads of 4A or lower, the power dissipation of the external MOSFET should not pose any thermal design problems if it is chosen wisely. The N-channel MOSFET must exhibit a low Rdson and should still be inexpensive and readily available. The overall efficiency of the dual power supply will vary depending upon the burden on each output. Therefore, the switched-mode supply should typically be utilized as the primary supply with the linear regulator portion being used to provide power for the output that is more lightly loaded.

Design Equations

Linear Regulator

$$V_{OUT} = V_{REF}\left(\frac{R2 + R3}{R3}\right)$$

Switched-mode Regulator

$$V_{OUT} = V_{REF}\left(\frac{R4 + R5}{R4}\right)$$

Autodetecting Single/Dual Power Supply for a Flexible Motherboard Design

Further analysis of the Intel Pentium® processors reveals the requirement for an open-ended motherboard power supply design that can accomodate different CPUs in a single system. As an example, consider the Intel® P54C and P55C Pentium® processors. Although these two processors may occupy the same CPU socket, distinct differences exist in their power supply requirements. The present generation P54C uses a single supply for both the processor core and the I/O. For the higher performance devices, the supply voltage required is 3.5V ±100mV (VRE s-specification).

For the lower performance models, a 3.3V ±5% supply is acceptable. For improved compatibility, Intel has now respecified its 3.3V standard CPUs for operation at the new 3.5V VRE level. The P55C multimedia upgrade processor, due to be released in the latter part of 1996, requires separate voltages for the core and I/O circuitry. The nominal core voltage is currently 2.8V ±100mV, while the I/O supply remains at a nominal 3.3V. It is therefore desirable to implement a power supply design that will automatically detect the CPU model present and program each output voltage accordingly. The circuit in figure 2 directly addresses this requirement. The basic purpose of this design is to provide an automatic switch between a single switched-mode power supply and a dual switching/linear power supply depending upon which CPU occupies the socket.

To ease the task of identifying the CPU, the P55C processor includes a single-bit identification pin, *VCC2DET,* at location AL1, to distinguish itself from the standard Pentium® P54C processor. This pin is always bonded to ground on the P55C CPU, while it is an internal no connect on the P54C. Therefore, the addition of an external pull-up resistor allows the user to easily identify which processor occupies the CPU socket. The circuit in figure 2 also uses the CPU identification pin to select the appropriate output voltage for the CPU core power island and switch off the linear regulator output when only a single output is necessary. To optimize the overall efficiency of the power supply, the switching converter should be used to power the load that is most heavily burdened. Therefore, the obvious choice is to assign the switching converter as the CPU core supply. Using this configuration, the switched-mode supply will always be loaded whereas the linear regulator portion will only be burdened when the dual voltages are required.

Because the I/O circuitry will always operate from a nominal 3.3V supply, the linear regulator output is set at a fixed 3.3V output using resistors R2 and R3. The CPU core supply is thus switched between 2.8V and 3.5V using an external FET and the appropriate combination of resistors. Using this circuit configuration, the switched-mode supply can source up to 10A, while the linear regulator portion can be loaded to 5A. These current ranges will easily accomodate the standard Pentium® P54C/P54C and the P55C as well as other Pentium® compatible processors such as the Cyrix® 6x86.

Detailed Product Description

The RC5035 combines a programmable voltage step-down DC-DC controller with a similarily programmable low dropout linear regulator. When designed around the appropriate external components, it can be configured to deliver more than 5A of load current with both outputs loaded and up to 10A from the switched-mode regulator. During all loading conditions the switched-mode portion of the RC5035 functions as a constant-on-time PWM step-down regulator.

Advanced Information

Main Control Loop

The main control loop of the regulator, see Block Diagram, contains one main control block. The analog control block consists of signal conditioning amplifiers that feed into a set of fast comparators which provide the inputs to control the clock VCO. The signal conditioning block takes inputs from the IF_{BH} and IF_{BL} (current feedback) and VFBSW (voltage feedback) pins and then sets up two controlling signal paths. The voltage control path gains up the VFBSW signal and presents that signal to one of the summing amplifier inputs. The current control path takes the difference between the IFBH and IFBL pins and presents that signal to another input of the summing amplifier. These two signals are then summed together with the slope compensation input from the oscillator and the output is then presented to a comparator. This comparator provides the main PWM control signal to the VCO control block.

There are other comparators in the analog control block that control the point at which the max-current comparator disables the output drive signal to the power MOSFET.

The VCO controller section is designed to take the comparator inputs along with the main clock signal from the oscillator and provide a constant-on-time set of pulses to the VOSW output pin that will in turn control the external power MOSFET. The high speed complementary bipolar process allows the RC5035 to clock at speeds greater then 1MHz.

High Current Output Drivers

The RC5035 high current output driver contains high speed bipolar power transistors configured in a push-pull configuration. Each output driver is capable of pumping out 1A of current in less than 100ns. Each driver's power and ground are separated from the overall chip power and ground for added switching noise immunity. The VOSW driver has a power supply, V_{CCP}, which can be derived from an external 12V source or boot-strapped from a flying-capacitor. In the boot-strapped mode, C2 is connected to the source of M1 and is alternately charged from V_{CC} via the schottky diode DS2 and then boosted up when M1 is turned on. This provides a V_{CCP} voltage equal to $2*V_{CC}$ - Vds(DS2); or about 9.5V with V_{CC}=5V. This voltage is sufficient to provide the 9V gate drive to the external MOSFET that will be needed for achieving a low Rdson. If V_{CCP} is derived from an external 12V source, the Rdson is assured of being low due to the increased gate drive voltage to the power FET M1 .

Internal Reference

The reference in the RC5035 is a precision band-gap type reference. Its temperature coefficient is trimmed to provide a near zero TC. For applications that require a different voltage, a pair external resistors can be used change the output voltage from 2.0V up to 3.6V. For a guaranteed stable operation under all loading conditions, a 0.1µF capacitor is recommended on the VREF output pin.

Over-Voltage Protection

The RC5035 provides a constant monitor of the output voltage for over-voltage protection. Should the voltage at the VFB pin exceed 20% of the selected program voltage, then an overvoltage condition will be assumed to exist and the RC5035 will shut down the output drive signals to the power FETs.

Oscillator

The RC5035 oscillator is designed as a fixed on-time, variable off-time oscillator. It is comprised of a window comparator, a fixed current source, an analog switch and an external timing capacitor. The oscillator will exhibit a fixed on-time, where the off-time will vary proportional to the feedback current from the switched-mode regulator. Therefore, the overall switching frequency of the oscillator will vary with the load current.

The window comparator is used to provide the constant on-time, where the analog switch opens when the upper comparator threshold limit is reached. A fixed current source then discharges the oscillator capacitor until the lower comparator threshold is reached. Therefore, the fixed on-time is derived from a constant current slewing a fixed capacitor through a constant voltage. The comparator output directly feeds the output driver circuitry, eliminating the need for logic circuitry in the PWM. Once the comparator input reaches the low threshold, the comparator output switches levels and enables the analog switch. The feedback current then forces the output to slew up to the comparator upper threshold. Using this implementation, lighter loads and/or smaller error voltages will increase the time to reach the upper comparator threshold and thus increase the overall switching frequency.

Output Enable/Voltage Select Function

The RC5035 includes an ENABLE pin in order to allow the user to enable or disable the linear regulator as well as change the output voltage of the switched-mode regulator using a single logic input. The ENABLE pin is an open collector compatible input. When the ENABLE pin is in the LOW state, the linear regulator is turned on and the RC5035 will operate as a dual output power supply. When the ENABLE pin is switched to the HIGH state, the op-amp portion of the linear regulator will turn off. In addition, an alternate voltage feedback loop from the switched-mode regulator output will be enabled that re-programs its output voltage according to a second set of precision resistors. Using this configuration, the RC5035 can read the $\overline{\text{VCC2DET}}$ output from a Pentium® CPU and program the outputs to deliver the appropriate voltage(s) to the CPU core and I/O circuitry depending upon the processor type.

When using the RC5035 in a Flexible Motherboard application for the Pentium® P54C/P55C processors, a shorting bar must be inserted in the motherboard to join the CPU core and I/O power islands when a single output is

selected. If this shorting bar is not utilized, the two power islands will be joined solely via the internal bonding connections of the CPU and damage to the processor may result.

Design Procedure and Applications Information

Simple Step-Down Converter

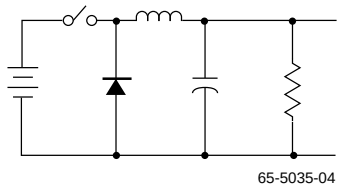


Figure 2. Simple Buck DC-DC Converter

Figure 2 shows a step-down DC-to-DC Converter with no feedback controller. The derivation of the basic step-down converter will serve as a basis for the design equations for the RC5035 in Figure 1. In Figure 2, the basic operation begins by closing the switch, S1. When S1 is closed the input voltage V_B is impressed across the inductor L1. The current flowing in the inductor is given by the following equation: $I_L=(V_B- V_O)Ton/L$; where Ton is the time duration for S1 to be closed. When S1 is open, the diode will conduct the inductor current and the output current will be delivered to the load according to the equation: $I_L=V_O(T - T_{ON})/L$; where $T- T_{ON}$ is the time duration for S1 to be off. By solving these two equations we can arrive at the basic relationship for the output voltage of a step-down converter:

$$V_O = VB(T_{ON}/T)$$

Selecting the Inductor

The inductor is one of the most critical components to be selected in the DC-to-DC converter application. The critical parameters are inductance (L), max DC current (Imax), and the coil resistance (Rl). The inductor core material is a critical factor in determining the amount of current that the inductor will be able to handle. As with all engineering designs there are trade- offs for various types of inductor core materials. In general, Ferrites are popular because of their low cost, low EMI, and high frequency (>500kHz) characteristics. Molypermalloy powder (MPP) materials have good saturation characteristics and low EMI with low hysteresis losses; however they tend to be expensive and are more efficiently utilized at frequencies below 400kHz.
DC winding resistance is another critical parameter.
In general, the DC resistance should be kept as low as possible. The power loss in the DC resistance will degrade the efficiency of the converter by the relationship: Power Loss = (Io)2*Rl.

The value of the inductor is a function of the switching frequency (T_{ON}) and the maximum inductor current.

The max inductor current can be calculated from the relationship:

$$I_{MAX} = \frac{2I_L}{F_O T_{ON}\left(\frac{V_{IN} - V_{OUT}}{V_{OUT} - V_D}\right) + 1}$$

Where:
F_O is the desired clock frequency
T_{ON} is the max on time of the M1 FET
V_Dd is the forward voltage of the schottky diode D1

Then the inductor value can be calculated with the relationship:

$$L = \left(\frac{V_{IN} - V_{DSON}}{I_{MAX}}\right) T_{ON}$$

Where:
V_{DSON} is the voltage across the drain-source of the M1 FET when switched on (calculated by RDSon * I_{MAX})

Current-Sense Resistor

The current sense resistor will carry all of the peak current of the inductor. This current will be more than the designed for load current. The RC5035 will begin to limit the output current to the load by turning off the top-side FET driver when the voltage across the current-sense resistor exceeds 100mV. When this happens the output voltage will temporarily go out of regulation. As the voltage across the resistor becomes larger, the top-side FET will turn off more and more until the current limit value is reached and then the RC5035 will continuously deliver the limit current at a reduced output voltage level. To insure that load transient conditions do not momentarily cause deregulation of the output voltage, a 20% margin in the limit voltage is advisable. Thus the resistor should be set by the relationship:

$$R = 100\ mV/Ipeak$$

Where:
Ipeak = Imax * 1.33

Since the value of the sense resistor is generally in the miliohm region, care should be taken in the layout of the PCB. Trace resistance can contribute significant errors. The traces to the IFBH and IFBL pins of the RC5035 should be Kelvin connected to the pads of the current-sense resistor as shown in the sample layout Figure 4. To minimize the influence of noise the two traces should be run next to each other and the pins should be bypassed with a .1uF to GND as close to the device pins as possible.

Filter Capacitors

Good ripple performance and transient response are functions of the filter capacitors. Since the 5V input for a PC motherboard can be located several inches away from the

DC-to-DC converter, input capacitance can play an important role in the load transient response of the RC5035. In general, the higher the input capacitance, the more charge storage is available for improving the current transfer through the top-side FET. A good rule of thumb is that for each watt of output power that you wish to deliver, there should be around 10uF of input capacitance. Low "ESR" capacitors are best suited for this application and can have an influence on the converter's efficiency. The input capacitor should be placed as close to the drain of the top-side FET as possible to reduce the effect of ringing that can be caused by large trace lengths.

The ESR rating of a capacitor is a difficult number to pin down. ESR or Equivalent Series Resistance, is defined at the resonant impedance of that capacitor. Since the capacitor is actually a complex impedance device having resistance, inductance and capacitance, it is quite natural for it to have an associated resonant frequency. As a rule, the lower the ESR, the better suited the capacitor is for use in switching power supply applications. Many capacitor manufacturers do not supply ESR data. A useful estimate of the ESR can be obtained with the following equation: $ESR = DF/2\pi fC$. Where DF is the capacitor's dissipation factor, f is the frequency of measure and C is the capacitance in farads.

With this in mind, calculating the output capacitance correctly is crucial to the performance of the DC-to-DC converter. The output capacitor determines the overall loop stability, output voltage ripple, and the transient load response. The calculation uses the following equation:

$$C\,(\mu F) = \frac{T\left(\frac{(V_{IN} - V_{OUT})}{V_{OUT}} + I_L\right)}{V_R}$$

Where:
V_R is the desired output ripple voltage

Schottky Diode Selection

The application circuit diagram shows two schottky diodes, DS1 and DS2. As it is configured, DS2 provides the function of bootstrapping the V_{CCP} node during startup. It is possible to cause the output stage to latchup if the V_{CCP} supply is brought up before the other V_{CC} supplies of the RC5035. It is therefore advisable that DS2 be connected. It is important in the selection of DS1 and DS2 that they have a low forward voltage drop as this directly affects the regulator efficiency. During the off time of the power FET, M1, the voltage on the inductor will drop until the diode DS1 clamps and conducts the full current in the inductor. The power in DS1, Vf*IL, is a direct subtraction from the overall efficiency of the DC-DC converter; therefore, it is important for DS1 to have a low Vf in order to minimize the power loss term.

MOSFET Switches

The MOSFET switch in the RC5035 applications circuit is an N-channel "logic-level" FET. This means that it will be fully on with a Vgs of 4V. Many manufacturers make logic-level FETs and the trick is to choose the one with the lowest Rdson at the given Imax current level. The value of Rdson directly enters into the efficiency equation as a power loss. Also influencing the efficiency is the gate charge of the FET and the clock frequency of the RC5035. At higher clocking rates the amount of charge needed to be delivered to the FET is going to lower the overall efficiency.

PCB Layout and Grounding

As is the case with most analog circuitry, good layout practices are necessary to achieve the optimum in the overall performance of the DC-to-DC converter. In general, it is always a good practice to have a tight layout that attempts to minimize short low inductance wiring to the RC5035.

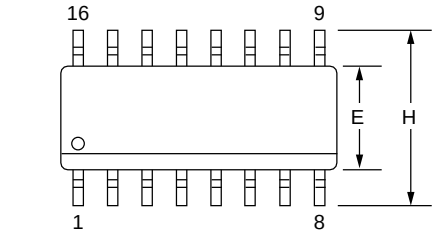
The use of multilayer PCB is recommended. In particular, it is recommended to have a continuos ground plane beneath the circuit, 2oz copper would be preferred in high current applications. As was stated previously, the current-sense resistor, R1, should be located as close to the RC5035 as possible and all voltage and current feedback traces should be Kelvin connected to the pads of R1. To minimize switching losses and noise, place M1, M2, L1 and DS2 as close together as possible. Also try to keep the V_{OSW} and V_{OL} gate drive signal traces as short as possible. It is recommended that the noisy switching part of the circuit be kept away from the low current pins on the chip such as IF_{BH}, IF_{BL}, V_{FBSW}, V_{FBSW2} and C_{EXT}. Keep the 0.1uF bypass capacitors as close to the chip pins as possible. All of the ground pins should be connected to the ground plane directly under the chip. A sample layout is provided in Figure 4.

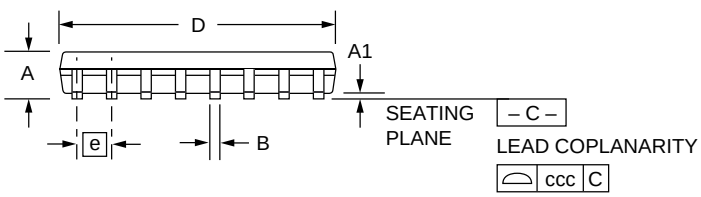
Mechanical Dimensions – 16-Lead SOIC Package

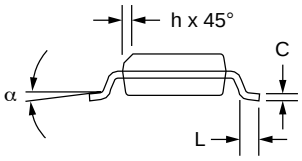
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.19	0.25	5
D	.386	.394	9.80	10.00	2
E	.150	.158	3.81	4.00	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.80	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	16		16		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Advanced Information

Ordering Information

Product Number	Package
RC5035M	16 pin SOIC

Advanced Information

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RC5036

Dual Adjustable Voltage Regulator Controller

Features

- Combines switching regulator and low dropout linear regulator in single chip
- Linear regulator on/off control
- Each output voltage adjustable from 1.5V to 3.6V
- Built-in soft start
- Switcher can be configured for 13A loads, linear for 5A
- Precision trimmed low TC voltage reference
- Constant On-Time oscillator
- Small footprint 16 lead SOIC package

Applications

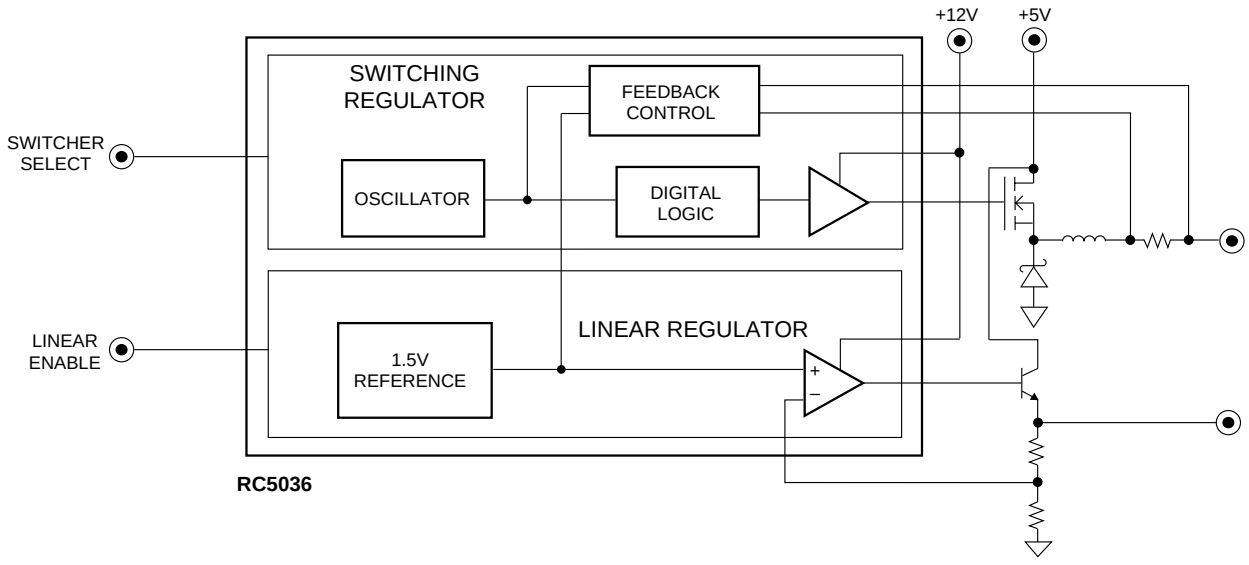
- RAMBUS or SDRAM power with ACPI support
- I/O and AGP power
- High efficiency power for DSPs
- Programmable dual power supply for high current loads

Description

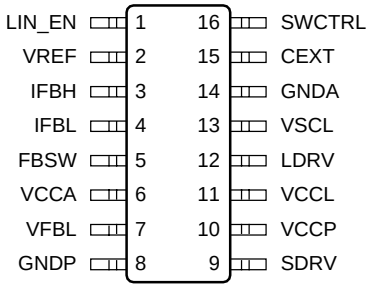
The RC5036 combines a switch-mode DC-DC converter with a low-dropout linear regulator. In addition, it integrates the circuitry required to switch the DC-DC converter output between 3.5V and a user-selectable voltage from 1.5V to 3.6V as well as an enable function to allow the linear regulator to be turned off when not required. RC5036 has built-in soft start feature which offers system protection during power-up by reducing both inrush current and output overshoot.

With the appropriate external components, the DC-DC converter can deliver load current as high as 13A and the linear regulator can provide 5A. The DC-DC converter and the linear regulator can be set independently using two external resistors each to any value between 1.5V and 3.6V. The factory trimmed internal reference achieves tight tolerance voltage regulation on both outputs. Independent short circuit protection is also provided.

Block Diagram



Pin Assignments



Pin Descriptions

Pin Name	Pin Number	Pin Function Description
LIN_EN	1	**Linear regulator enable input.** Accepts TTL/open collector input levels. A logic level HIGH on this pin disables the output of the linear regulator.
VREF	2	**Voltage reference test point.** This pin provides access to the internal precision 1.5V bandgap reference and should be decoupled to ground using a 0.1µF ceramic capacitor. No load should be connected to this pin.
IFBH	3	**High side current feedback for switching regulator.** Pins 3 and 4 are used as the inputs for the current feedback control loop and as the short circuit current sense points. Careful layout of the traces from these pins to the current sense resistor is critical for optimal performance of the short circuit protection scheme. See Applications Discussion for details.
IFBL	4	**Low side current feedback for switching regulator.** See Applications Discussion for details.
FBSW	5	**Voltage feedback for switching regulator.** This input is active when a logic level LOW is input on pin 16 (SWCTRL). Using two external resistors, it sets the output voltage level for the switching regulator. See Applications Discussion for details.
VCCA	6	**Switching Regulator V_{CC}.** Power supply for switching regulator control circuitry and voltage reference. Connect to system 5V supply and decouple to ground with 0.1µF ceramic capacitor.
VFBL	7	**Voltage feedback for linear regulator.** Using two external resistors, this pin sets the output voltage level for the linear regulator. See Applications Discussion for details.
GNDP	8	**Power Ground.** Return pin for high currents flowing in pins 9, 10 and 12 (SDRV, VCCP and LDRV). Connect to a low impedance ground. See Applications Discussion for details.
SDRV	9	**FET driver output for switching regulator.** Connect this pin to the gate of the N-channel MOSFET Q1 as shown in Figure 1. The trace from this pin to the MOSFET gate should be kept as short as possible (less than 0.5"). See Applications Discussion for details.
VCCP	10	**Switching regulator gate drive V_{CC}.** Power supply for SDRV output driver. Connect to system 12V supply with R-C filter shown in Figure 1. See Applications Discussion for details.
VCCL	11	**Linear Regulator Vcc.** Power supply for LDRV output op-amp. Connect to system 12V supply and decouple to ground with 0.1µF ceramic capacitor.
LDRV	12	**Output driver for linear regulator.** Connect this pin to the base of an NPN transistor. When pin 1 (LIN_EN) is pulled HIGH, the linear regulator is disabled and pin 12 will be pulled low internally.
VSCL	13	**Low side current sense for linear regulator.** Connect this pin between the sense resistor and the collector of the power transistor. The high side current sense is internally connected to pin 6 (VCCA). Layout is critical to optimal performance of the linear regulator short circuit protection scheme. See Applications Discussion for details.

Pin Descriptions (continued)

Pin Name	Pin Number	Pin Function Description
GNDA	14	**Analog ground.** All low power internal circuitry returns to this pin. This pin should be connected to system ground so that ground loops are avoided. See Applications Discussion for details.
CEXT	15	**External capacitor.** A 180pF capacitor is connected to this pin as part of the constant on-time pulse width circuit. Careful layout of this pin is critical to system performance. See Applications Discussion for details.
SWCTRL	16	**Switching regulator control input.** Accepts TTL/open collector input levels. A logic level HIGH on this pin presets the switching regulator output voltage at 3.5V using internal resistors. A logic level LOW on this pin will select the output voltage set by two external resistors and the voltage feedback control pin 5 (VFBSW). See Applications Discussion for details.

Absolute Maximum Ratings

Supply Voltages, VCCA, VCCL, VCCP	13V
Junction Temperature, T_J	+150°C
Storage Temperature, T_S	-65 to +150°C
Lead Soldering Temperature, 10 seconds	300°C
Thermal Resistance Junction-to-Ambient, Θ_{JA}	112°C/W

Note:
1. Functional operation under any of these conditions is not implied. Performance is guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Switching Regulator V_{CC}, VCCA		4.75	5	5.25	V
Linear Regulator V_{CC}, VCCL		11.4	12	12.6	V
Logic Inputs, SWCTRL, LIN_EN	Logic HIGH Logic LOW	2.4		 0.8	V V
Ambient Operating Temperature, T_A		0		70	°C
Drive Gate Supply, V_{CCP}		9.5	12	12.6	V

Electrical Characteristics—Switch-Mode Regulator

(VCCA = 5V, VCCL = 12V, T_A = 25°C using circuit of Figure 1, unless otherwise noted)

The • denotes specifications which apply over the full ambient operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
Output Voltage, VOSW[1]	SWCTRL = HIGH Set by internal resistors	•		3.5		V
Output Voltage, VOSW[1]	SWCTRL = LOW Set by external resistors	•	1.5		3.6	V
Setpoint Accuracy[2]	I_{SW} = 5A		-1.2		+1.2	%Vo
Output Temperature Drift	T_A = 0°C–70°C	•		40		ppm
Line Regulation	VCCA = 4.75 to 5.25V I_{SW} = 5A			0.10	0.15	%Vo
Load Regulation	I_{SW} = 0 to 5A or 5A to 10A			±0.9	±1.3	%Vo
Output Ripple, peak-peak	20MHz BW, I_{SW} = 5A			15		mV
Cumulative DC Accuracy[3]		•		±55	±100	mV
Efficiency	I_{SW} = 5A		80	87		%
Output Driver Current	Open Loop	•	0.5			A
Short Circuit Threshold Voltage		•	70	90	100	mV
On Time Pulse Width[4]	C_{EXT} = 180pF			3.5		µs

Notes:

1. When the SWCTRL pin is HIGH or left open, the switch-mode regulator output will be preset at 3.5V using internal precision resistors. When the SWCTRL pin is LOW, the output voltage may be programmed with external resistors. Please refer to the Applications Section for output voltage selection information.
2. Setpoint accuracy is the initial output voltage variability under the specified conditions. When SWCTRL is LOW, the matching of the external resistors will have a major influence on this parameter.
3. Cumulative DC accuracy includes setpoint accuracy, temperature drift, line and load regulation, and output ripple.
4. The on-time pulse width of the oscillator is preset using external capacitor C_{EXT}. See Typical Operating Characteristics curves.

Electrical Characteristics—Linear Regulator

(VCCA = 5V, VCCL = 12V, T_A = 25°C using circuit in Figure 1, unless otherwise noted)

The • denotes specifications which apply over the full ambient operating temperature range.

Parameter	Conditions		Min	Typ	Max	Units
Output Voltage, VOL[1]	Set by external resistors	•	1.5		3.6	V
Setpoint Accuracy[2]	I_L=0.5A, using 0.1% resistors		-1.5		+1.5	%
Output Temperature Drift		•		40		ppm
Line Regulation	VCCL = 11.4V to 12.6V, I_L = 3A			0.1	0.15	%Vo
Load Regulation	I_L = 0 to 5A			±0.7	±1	%Vo
Output Noise	0.1 to 20KHz			1		mV
Cumulative DC Accuracy[3]		•		±1.7	±3	%
Crosstalk[4]	I_{SW} = 5A			35		mVpp
Short Circuit Comparator Threshold		•	40	50	60	mV
Op-amp Output Current	Open Loop		50	70		mA

Notes:

1. When the LIN_EN pin is LOW, the linear regulator output is set with external resistors. When the LIN_EN pin is HIGH, the linear regulator is disabled and will exhibit no output voltage. Please refer to the Application Section for output voltage selection information.
2. Setpoint accuracy is the initial output voltage variability under the specified conditions. The matching of the external resistors will have a major influence on this parameter.
3. Cumulative DC accuracy includes setpoint accuracy, temperature drift, line and load regulation.
4. Crosstalk is defined as the amount of switching noise from the switch-mode regulator that appears on the output of the linear regulator when both outputs are in a static load condition.

Electrical Characteristics—Common

(VCCA = 5V, VCCL = 12V, T_A = 25°C using circuit of Figure 1, unless otherwise noted)

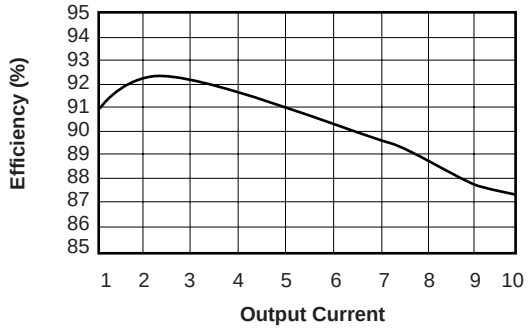
The • denotes specifications which apply over the full ambient operating temperature range.

Parameter	Conditions		Min	Typ	Max	Units
Reference Voltage, VREF			1.485	1.5	1.515	V
VREF PSRR			60			dB
VCCA Supply Current	Independent of load	•		5	15	mA
VCCP Supply Current	I_{SW} = 5A	•		20	25	mA
VCCL Supply Current	I_L = 2A	•		5		mA

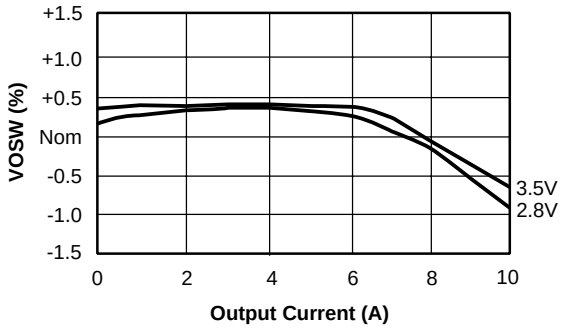
Typical Operating Characteristics

(VCCA = 5V, VCCL = 12V and T_A = +25°C using circuit in Figure 1, unless otherwise noted)

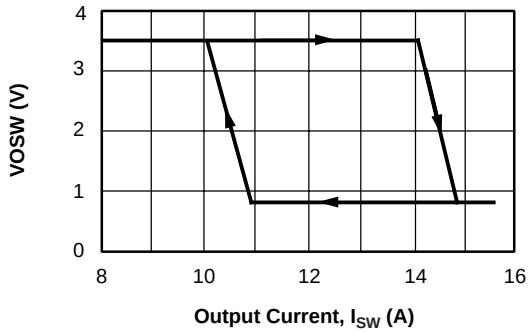
Switcher Efficiency vs. Output Current



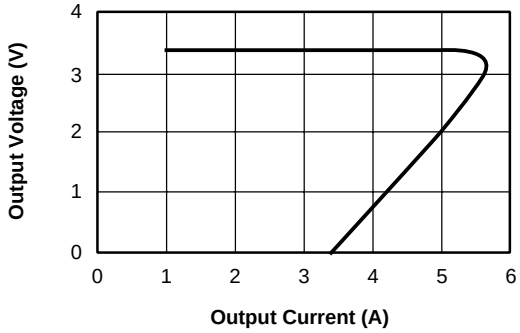
Switcher Output Voltage vs. Load



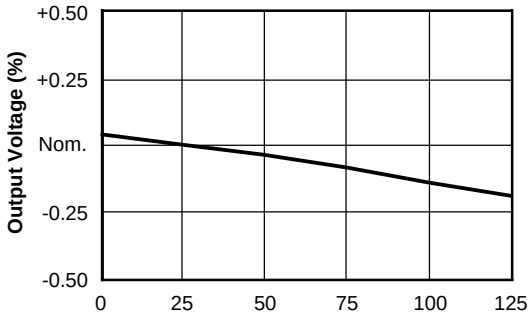
Switcher Output vs. Output Current



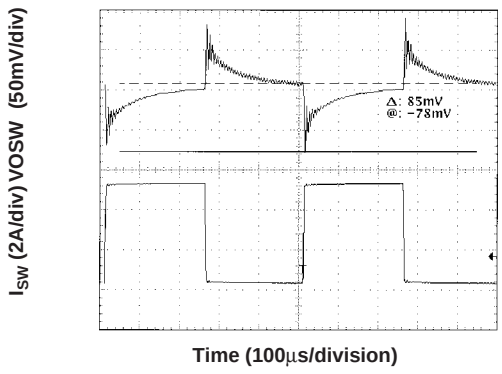
Linear Regulator Output vs. Output Current, Rsense = 7mΩ



Output Voltage vs. Temperature, I_{SW} = 5A or I_{LR} = 5A

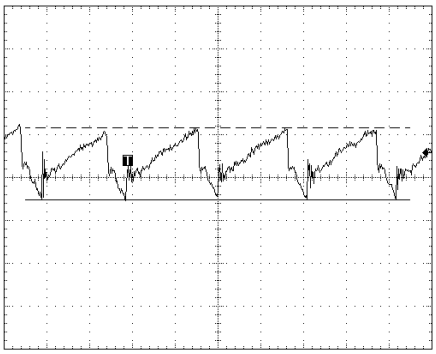


Switcher Transient Response, 0.5A to 5.5A



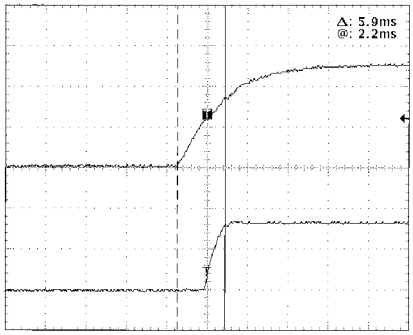
Typical Operating Characteristics (continued)

Switcher Output Ripple, I_{OUT} = 10A



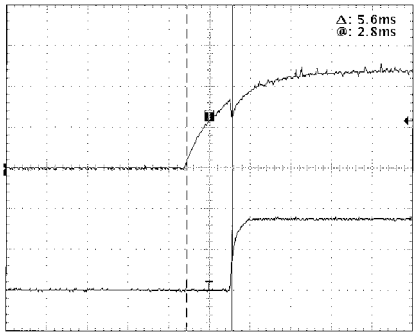
Time (2µs/division)

Linear Output Startup, System Power-Up



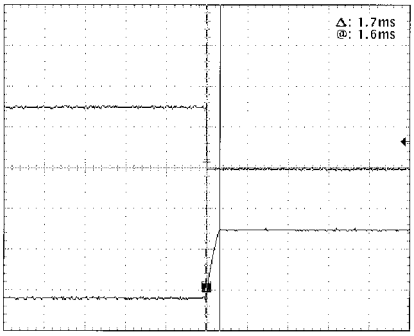
Time (5ms/division)

Switcher Output Startup, System Power-Up



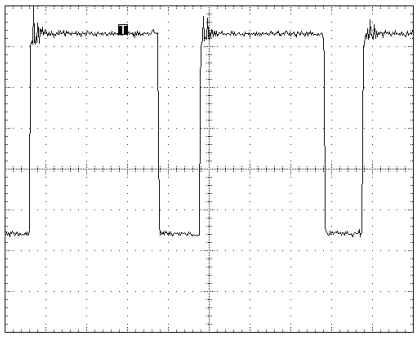
Time (5ms/division)

Linear Output Startup, Using LIM_EN Pin



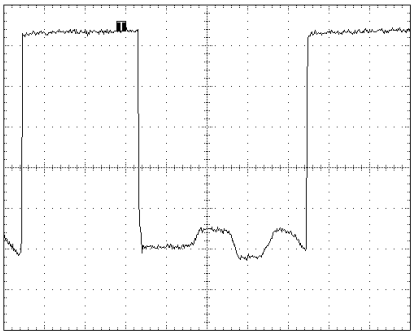
Time (5ms/division)

Pin 9 (SDRV), 10A Load



Time (1µs/division)

Pin 9 (SDRV), 0.1A Load



Time (1µs/division)

Application Circuit

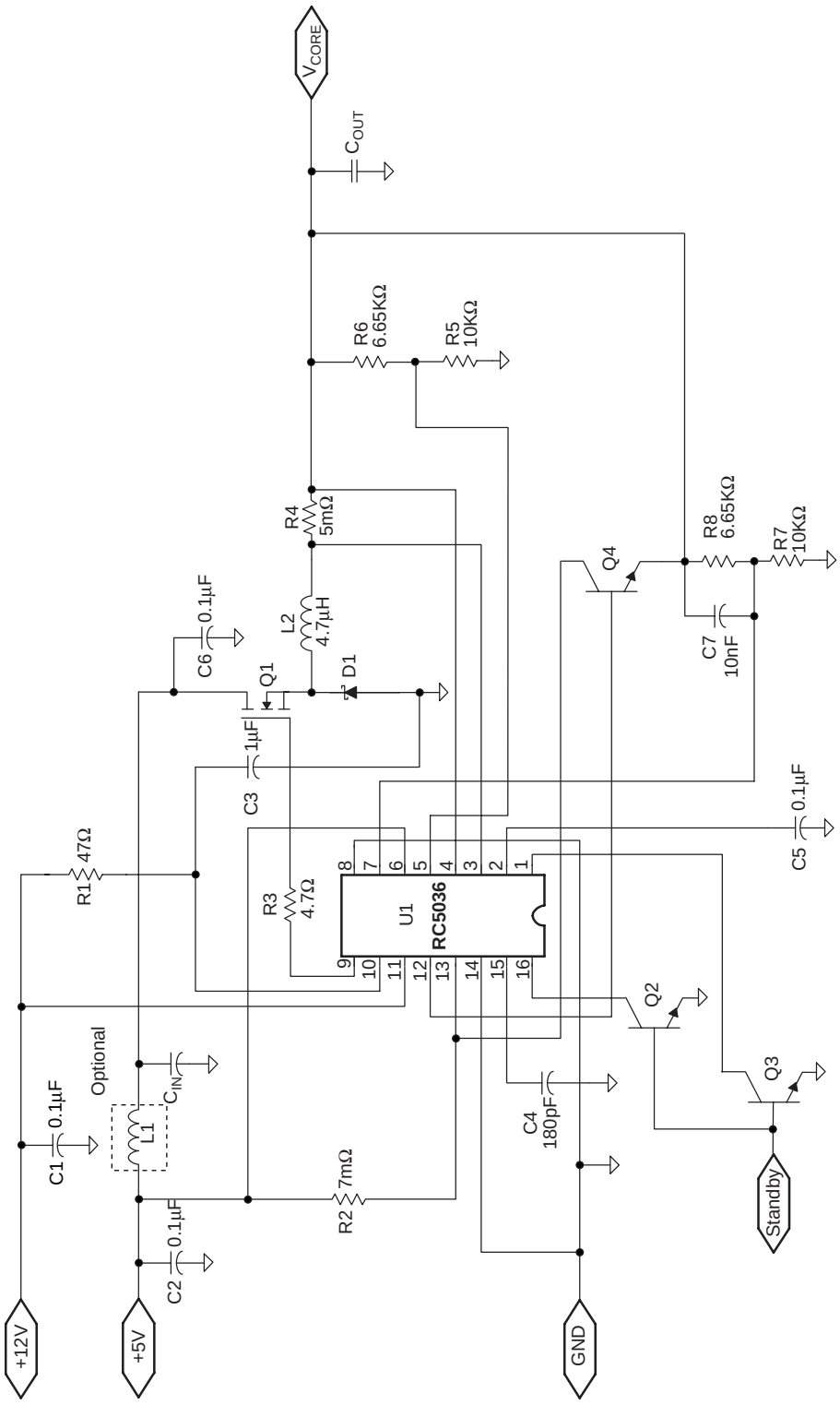


Figure 1. RAMBUS Power with ACPI support, 10A Main, 100mA Standby

Table1. Bill of Materials for a RC5036 RAMBUS Application

Qty.	Reference	Manufacturer Part Order #	Description	Requirements and Comments
4	C1-2, C5-6	Any	100nF, 25V Capacitor	
1	C3	Any	1µF, 25V Capacitor	
1	C4	Any	180pF, 50V Capacitor	C0G
1	C7	Any	10nF, 25V Capacitor	
3	C_{IN}	Sanyo 10MV1200GX	1200µF, 10V Aluminum Capacitor	I_{RMS} = 2A , See Equation (2) in Applications
1	C_{OUT}	Rubycon 6.3ZL1500M	1500µF, 6.3V Aluminum Capacitor	ESR = 23mΩ
1	R1	Any	47.5Ω	
1	R2	N/A	300mΩ	PCB Trace Resistor, see Applications
1	R3	Any	4.75Ω	
1	R4	N/A	5mΩ PCB Trace Resistor, 1W	PCB Trace Resistor, see Applications
2	R5, R7	Any	10KΩ	
2	R6, R8	Any	6.65KΩ	
1	D1	Motorola MBRB1545CT	15A, 45V Schottky	
1	Q1	Fairchild FDB6030L	30V, 14mΩ Logic Level MOSFET	
3	Q2-4	Fairchild MMBT2222A	40V, 1A NPN	
Optional	L1	Any	2.5µH Inductor	I_{SAT} > 8A
1	L2	Any	4.7µH Inductor	I_{SAT} > 13A
1	U1	Fairchild RC5036M	PWM Controller	

Application Information

The RC5036 contains a precision trimmed zero TC voltage reference, a constant-on-time architecture controller, a high current switcher output driver, a low offset op-amp, and switches for selecting various output modes. The block diagram in Figure 2 shows how the RC5036 in combination with the external components achieves a switchable dual power supply.

Switch-Mode Control Loop

The main control loop for the switch-mode converter consists of a current conditioning amplifier and one of the two voltage conditioning amplifiers that take the raw voltage and current information from the regulator output, compare them against the precision reference and present the error signal to the input of the constant-on-time oscillator. The two voltage conditioning amplifiers act as an analog switch to select between the internal resistor divider network (set for 3.5V) or an external resistor divider network (adjustable for 1.5V to 3.6V.) The switch-mode select pin determines which of the two amplifiers is selected. The current feedback signals come across the Iout sense resistor to the IFBH and IFBL inputs of the RC5036. The error signals from both the current feedback loop and the voltage feedback loop are summed together and used to control the off-time duration of the oscillator. The current feedback error signal is also used as part of the RC5036 short-circuit protection.

Linear Control Loop

The low-offset op-amp is configured to be the controlling element in a precision low-drop-out linear regulator. As can be seen from Figure 2, the op-amp is used to compare the divided down output of the linear regulator to the precision reference. The error signal is used to control either an N-channel MOSFET or a power NPN transistor.

High Current Output Drivers

The RC5036 switching high current output driver (SDRV) contains high speed bipolar power transistors configured in a push-pull configuration. The output driver is capable of supplying 0.5A of current in less than 100ns. The driver's power and ground are separated from the overall chip power and ground for added switching noise immunity.

Internal Reference

The reference in the RC5036 is a precision band-gap type reference. Its temperature coefficient is trimmed to provide a near zero TC. For guaranteed stable operation under all conditions, a 0.1µF capacitor is recommended on the VREF output pin. No load may be attached to this pin.

Constant-On-Time Oscillator

The RC5036 switch-mode oscillator is designed as a fixed on-time, variable off-time oscillator. The constant-on-time oscillator consists of a comparator, an external capacitor, a fixed current source, a variable current source, and an analog switch that selects between two threshold voltages for the comparator. The external timing capacitor is alternately charged and discharged through the enabling and disabling of the fixed current source. The variable current source is controlled from the error inputs that are received from the current and voltage feedback signals. The oscillator off-time is controlled by the amount of current that is available from the variable current source to charge the external capacitor up to the high threshold level of the comparator. The on-time is set be the constant current source that discharges the external capacitor voltage down to the lower comparator threshold.

Using SWCTRL and LIM_EN

When the SWCTRL pin is HIGH, the switching regulator will set its output at 3.5V using two internal precision resistors. When this pin is LOW, the switching regulator output can be set to any voltage between 1.5V and 3.6V using external precision resistors. The LIN_EN pin is used to enable or disable the linear regulator. When the LIN_EN pin is HIGH, the linear regulator will be disabled. If this pin is LOW, the linear regulator output can be set from 1.5V to 3.5V using external precision resistors. The linear regulator output can be left on to provide power to other 3.3V components.

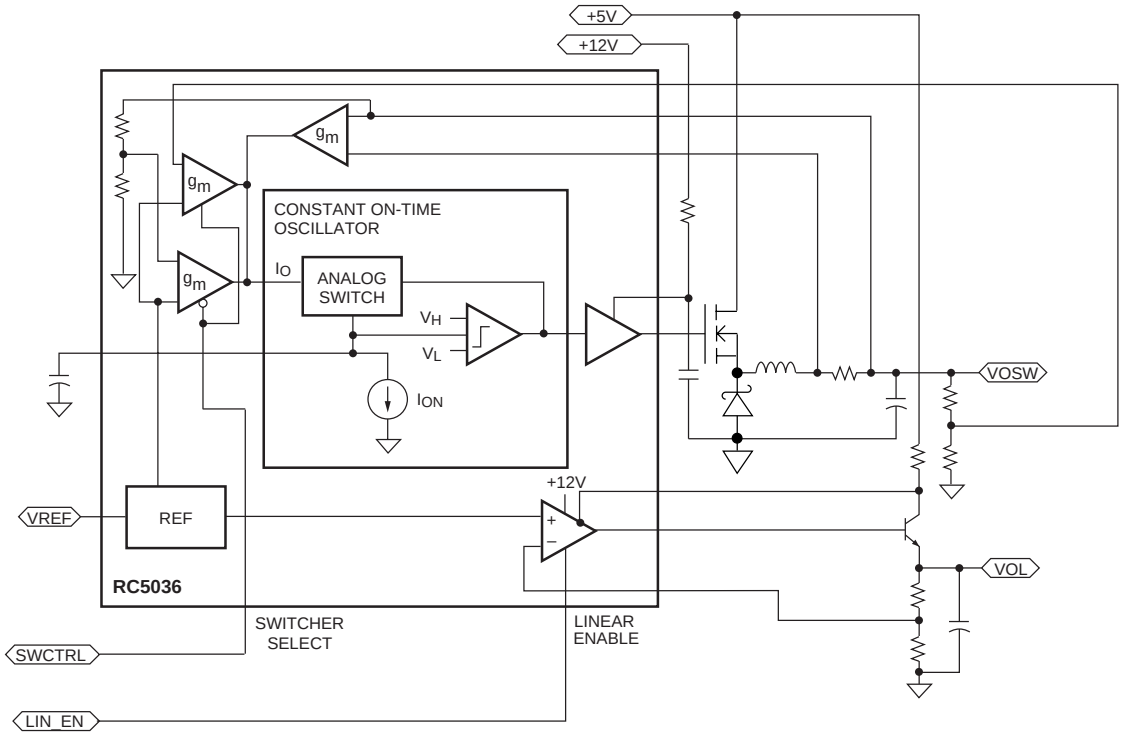


Figure 2. RC5036 Block Diagram

Output Voltage Selection

The RC5036 precision reference is trimmed to be 1.5V nominally. When using the RC5036, the system designer has complete flexibility in choosing the output voltage for each regulator from 1.5V to 3.6V. This is done by appropriately selecting the feedback resistors. These could be 0.1% resistors to realize optimum output accuracy. The following equations determine the output voltages of the two regulators:

Switching Regulator:

$$V_{OUT} = 1.5 \times \left(\frac{R6 + R5}{R5}\right)$$

Linear Regulator:

$$V_{OUT} = 1.5 \times \left(\frac{R8 + R7}{R7}\right)$$

where R6 > 1.5kΩ and (R5 + R6) ≤ 25kΩ and R8 > 1.5kΩ and (R7 + R8) ≤ 25kΩ

Example:

For 3.3V,

$$V_{OUT} = 1.5 \times \left(\frac{R6 + R5}{R5}\right) = 1.5 \times \left(\frac{6.65k + 10k}{10k}\right) = 3.3V$$

Input Capacitors

The number of input capacitors required for the RC5036 is dependent on their ripple current rating, which assures their rated life. The number required may be determined by

$$\text{No. Caps} = \frac{I_{out} \sqrt[*]{DC - DC^2}}{I_{rating}} \qquad (2)$$

where the duty cycle DC = V_{out}/V_{in}. For example, with a 1.5V output at 10A, 5V input, and using the Sanyo capacitors specified in Table 1 which have a 2A ripple current rating, we have DC = 1.5/5 = 0.3, and

$$\text{No. Caps} = \frac{^{10*}\sqrt{0.03 - 0.3^2}}{2} = 2.29$$

so that we need 3 input capacitors.

Linear Regulator Design Considerations

Figure 1 shows the application schematic for the RC5036 with an NPN used for the linear regulator.

Careful consideration must be given to the base current of the power NPN device. The base current to the power NPN device is limited by:

- The RC5036 op-amp output current (50mA)
- The internal power dissipation of the RC5036 package
- The β of the power NPN device.

The internal RC5036 power dissipation is the most severe limitation for this application. For optimum reliability, we require that the junction temperature not exceed 130°C; thus we can calculate the maximum power dissipation allowable for this 16-lead SOIC package as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\Theta JA}}$$

If we assume that the ambient temperature T_A is 70°C and the thermal resistance of the 16-lead SOIC package is 112°C/W, then the maximum power dissipation for the IC is:

$$P_D = \frac{130 - 70}{112} \leq 0.533W$$

$$P_D = P_{SW} + P_{LR} =$$

$$(35mA \times 5.25V) + (12.6V - V_{OUT} - V_{BE}) \times I_{OL} \leq 0.533W$$

where P_{SW} is the internal power dissipation of the switching regulator and P_{LN} is the internal power dissipation of the linear regulator. I_{OL} is the linear regulator op-amp output current. For V_{OUT} = 3.3V nominal, the worst case output will be determined by the current used.

For example, for a worst case V_{OUT} = 3.135V, the maximum op-amp output current is:

$$I_{OL} = \frac{0.533W - (35mA \times 5.25V)}{(12.6V - 3.135V - 0.8V)} \leq 40mV$$

$$\beta \geq \frac{3000mA}{40mA} = 75$$

The power NPN transistor must have a minimum β of 75 at I_L = 3A in order to meet the internal power dissipation limit of the 16-SOIC package.

Short Circuit Considerations

For the Switch-Mode Regulator

The RC5036 uses a current sensing scheme to limit the load current if an output fault condition occurs. The current sense resistor carries the peak current of the inductor, which is greater than the maximum load current due to ripple currents flowing in the inductor. The RC5036 will begin to limit the output current to the load by turning off the top-side FET driver when the voltage across the current-sense resistor exceeds the short circuit comparator threshold voltage (V_{th}). When this happens the output voltage will temporarily go out of regulation. As the voltage across the sense resistor becomes larger, the top-side MOSFET will continue to turn off until the current limit value is reached. At this point, the RC5036 will continuously deliver the limit current at a reduced output voltage level. The short circuit comparator threshold voltage is typically 90mV, with a variability of ±10mV. The ripple current flowing through the inductor is typically 0.5A. Refer to Application Note AM-53 for detailed discussions. The sense resistor value can be approximated as follows:

$$R_{SENSE} = \frac{V_{th,min}}{I_{PK}} \times (1 - TF) = \frac{V_{th,min}}{0.5A + I_{LOAD,MAX}} \times (1 - TF)$$

where TF = Tolerance Factor for the sense resistor and 0.5A accounts for the inductor current ripple.

Since the value of the sense resistor is often less than 10mΩ, care should be taken in the layout of the PCB. Trace resistance can contribute significant errors. The traces to the IFBH and IFBL pins of the RC5036 should be Kelvin connected to the pads of the current-sense resistor. To minimize the influence of noise, the two traces should be run next to each other.

For the Linear Regulator

The analysis for short circuit protection of the linear regulator is much simpler than that of the switching regulator. The formula for the inception point of short-circuit protection for the linear regulator is:

$$R_{SENSE} = \frac{V_{th,min}}{I_{LOAD,MAX}} \times (1 - TF)$$

V_{th} = 45mV ± 8mV and $I_{LOAD,MAX}$ = 5A,

$$R_{SENSE} = \frac{37mV}{5A} \times (1 - 29\%) = 5.3m\Omega$$ for using an embedded PC trace resistor

$$R_{SENSE} = \frac{37mV}{5A} \times (1 - 5\%) = 7.0m\Omega$$ for using a discrete resistor

Schottky Diode

In Figure 1, MOSFET Q1 and flyback diode D1 are used as complementary switches in order to maintain a constant current through the output inductor L1. As a result, D1 will have to carry the full current of the output load when the power MOSFET is turned off. The power in the diode is a direct function of the forward voltage at the rated load current during the off time of the FET. The following equation can be used to estimate the diode power:

$$P_{DIODE} = I_D \times V_D \times (1 - DutyCycle)$$

where I_D is the forward current of the diode, V_D is the forward voltage of the diode, and DutyCycle is defined the same as

$$\text{Duty Cycle} = \frac{Vout}{Vin}$$

For the Motorola MBRB1545CT Power Rectifier used in Figure 1,

$$P_{DIODE} = 10A \times 0.65 \times (1 - 73.1\%) = 1.75W$$

It is recommended that the diode T0-220 package be attached to a heatsink.

Board Design Considerations

RC5036 Placement

Preferably the PC layer directly underneath the RC5036 should be the ground layer. This serves as extra isolation from noisy power planes.

MOSFET Placement

Placement of the power MOSFET is critical in the design of the switch-mode regulator. The FET should be placed in such a way as to minimize the length of the gate drive path from the RC5036 SDRV pin. This trace should be kept under 0.5" for optimal performance. Excessive lead length on this trace causes high frequency noise resulting from the parasitic inductance and capacitance of the trace. Since this voltage can transition nearly 12V in around 100nsec, the resultant ringing and noise will be very difficult to suppress. This trace should be routed on one layer only and kept well away from the "quiet" analog pins of the device: VREF, CEXT, FBSW, IFBH, IFBL, and VFBL. Refer to Figure 3.

Inductor and Schottky Diode Placement

The inductor and fly-back Schottky diode must be placed close to the source of the power MOSFET. The node connecting the inductor and the diode swing between the drain voltage of the FET and the forward voltage of the Schottky diode. It is recommended that this node be converted to a plane if possible. This node is part of the high current path in the design, and is best treated as a plane to minimize the parasitic resistance and inductance on that node.

Most PC board manufacturers utilize 1/2oz copper on the top and bottom signal layers of the PCB; thus, it is not recommended to use these layers to rout the high current portions of the regulator design. Since it is more common to use 1 oz. copper on the PCB inner layers, it is recommended to use those layers to route the high current paths in the design.

Capacitor Placement

One of the keys to a successful switch-mode power supply design is correct placement of the low ESR capacitors. Decoupling capacitors serve two purposes; first there must be enough bulk capacitance to support the expected transient current, and second, there must be a variety of values and capacitor types to provide noise supression over a wide range of frequencies. The low ESR capacitors on the input side (5V) of the FET must be located close to the drain of the power FET. Minimizing parasitic inductance and resistance is critical in supressing the ringing and noise spikes on the power supply. The output low ESR capacitors need to be placed close to the output sense resistor to provide good decoupling at the voltage sense point. One of the characteristics of good low ESR capacitors is that the impedance gradually increases as the frequency increases. Thus for high frequency noise supression, good quality low inductance ceramic capacitors need to be placed in parallel with the low ESR bulk capacitors. These can usually be 0.1µF 1206 surface mount capacitors.

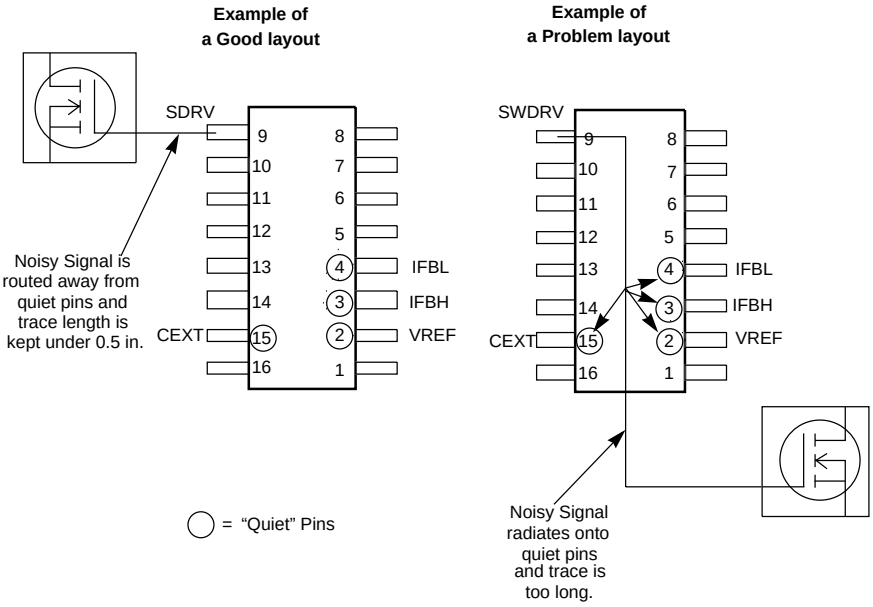


Figure 3. Examples of good and poor layouts

Power and Ground Connections

The connection of VCCA to the 5V power supply plane should be short and bypassed with a 0.1µF directly at the VCCA pin of the RC5036. The ideal connection would be a via down to the 5V power plane. A similar arrangement should be made for the VCCL pin that connects to +12V, though this one is somewhat less critical since it powers only the linear op-amp. Each ground should have a separate via connection to the ground plane below.

MOSFET Gate Bias

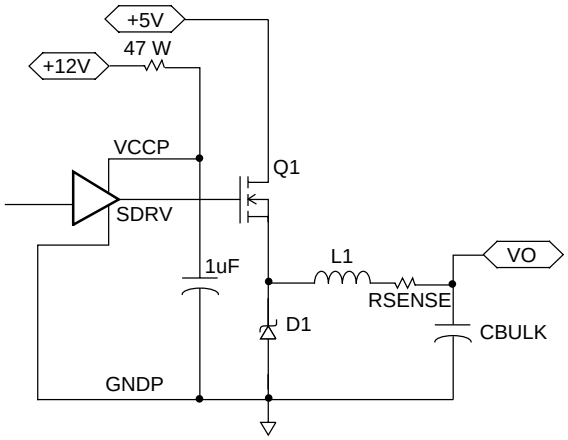


Figure 4. 12V Gate Bias Configuration

A 12V power supply is used to bias the VCCP. A 47Ω resistor is used to limit the transient current into VCCP. A 1uF capacitor filter is used to filter the VCCP supply and source the transient current required to charge the MOSFET gate capacitance. This method provides sufficiently high gate bias voltage to the MOSFET (V_{GS}), and therefore reduces $R_{DS(ON)}$ of the MOSFET and its power loss.

Figure 4 provides about 5V of gate bias which works well when using typical logic-level MOSFETs.

Layout Gerber File and Silk Screen

A reference design for motherboard implementation of the RC5036 along with the Layout Gerber File and the Silk Screen is available. Please call Fairchild Electronics Semiconductor Division's Marketing Departmentat 408-822-2550 to obtain this information.

RC5036 Evaluation Board

Fairchild Electronics Semiconductor Division provides an evaluation board for verifying the system level performance of the RC5036. The evaluation board provides a guide as to what can be expected in performance with the supplied external components and PCB layout. Please call your local Sales Office or Fairchild Electronics Semiconductor Division at 408-822-2550 for an evaluation board.

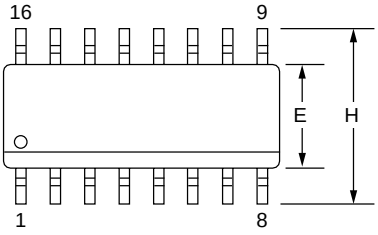
Mechanical Dimensions

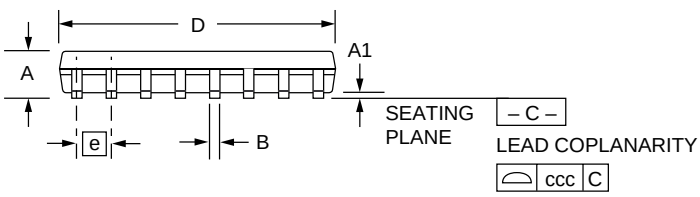
16-Lead SOIC Package

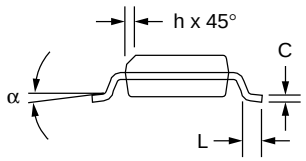
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.19	0.25	5
D	.386	.394	9.80	10.00	2
E	.150	.158	3.81	4.00	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.80	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	16		16		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Ordering Information

Product Number	Package
RC5036M	16 pin SOIC

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

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Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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Application Circuit for P55C, K6, and M2

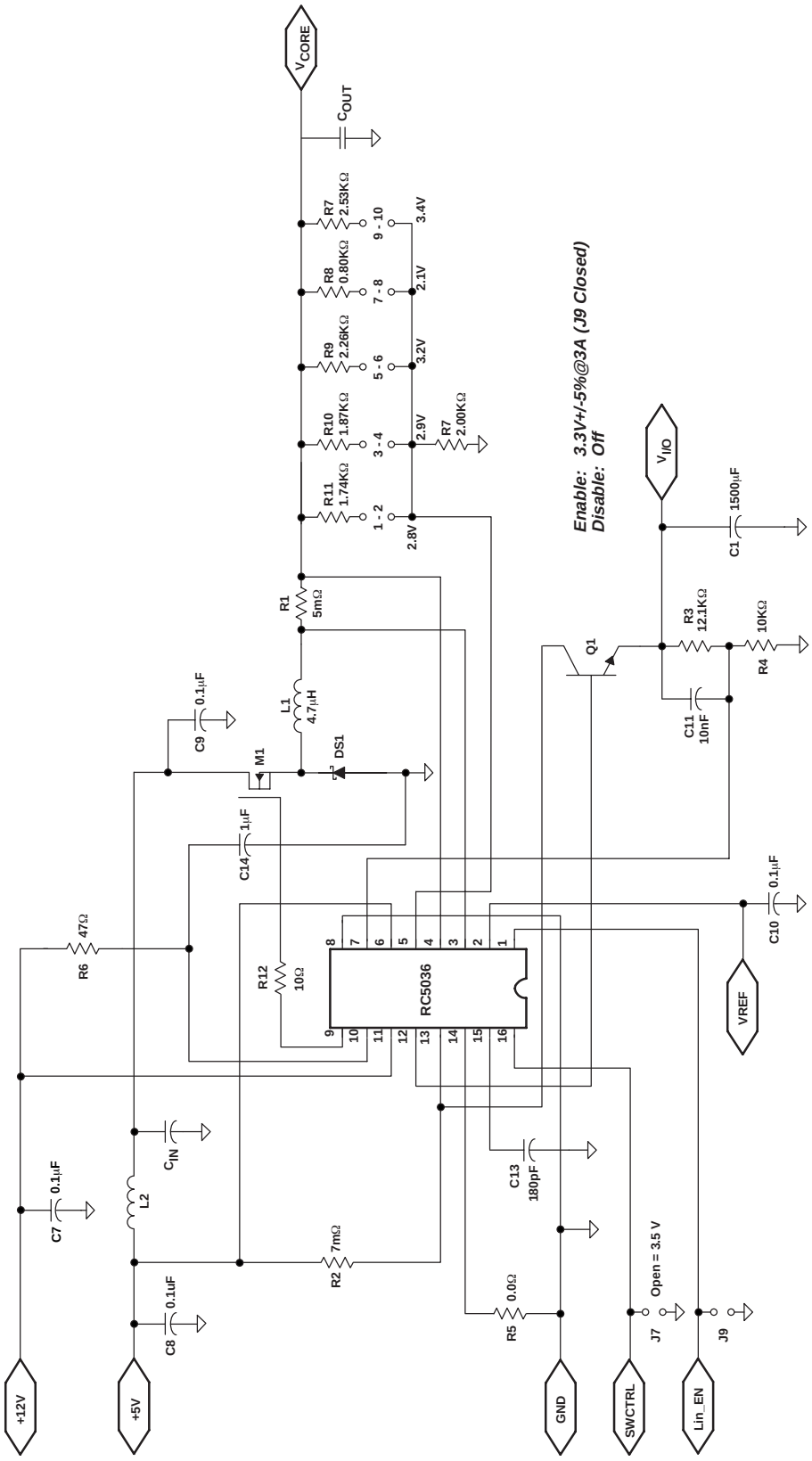


Figure 1. P54/P55C, K6 or M2 Single/Dual Power Supply Application Schematic

Table 1. Bill of Materials for a RC5036 P55C, K6, or M2 Application

Qty.	Reference	Manufacturer Part Order #	Description	Requirements and Comments
4	C7, C8, C9, C10	Panasonic ECU-V1H104ZFX	0.1μF 50V SMT 0805 capacitors	
1	C11	Panasonic ECU-V1H103KBX	10nF 50V SMT 0805 capacitor	
1	C13	Panasonic ECU-V1H181JCG	180pF 50V SMT0805 capacitor	
1	C14	Panasonic ECSH1CY105R	1μF 16V SMT 0805 Capacitor	
See Table 2	C_{OUT}	Sanyo 6MV1500GX	1500μF 6.3V electrolitic capacitor, 10mm x 20mm	ESR < 0.044Ω
See Table 2	C_{IN}	Sanyo 10MB1200GX	1200μF 10 B electrolytic capacitor, 10mm x 20mm	
1	C1	Sanyo 6MV1500GX	1500μF 6.3V electrolytic capacitor, 10mm x 20mm	
1	DS1	Motorola MBR1545CT	Schottky Diode	V_f < 0.57V at I_f = 7.5A
1	L1	Pulse Engineering PE-53682	4.7μH inductor	
1	L2	Beads Inductor	2 Beads, 3.5 x 8mm wire, diameter = 0.6mm	Optional—Helps reduce ripple on the 5V line
1	M1	IRL3103	N-Channel Logic Level Enhancement Mode MOSFET	$R_{DS(ON)}$ < 20mΩ, V_{GS} < 4.5V, I_D > 20A
1	Q1	Motorola MJE15028	NPN power transistor	ß > 80 at 3A
1	R1	R_{SENSE} (SW)	5mΩ MnCu or Copel resistor	
1	R8	Panasonic ERJ-6ENF 0.80KV	0.80KΩ 1% resistor	0.1% resistor desirable for accuracy
1	R9	Panasonic ERJ-6ENF2.26KV	2.26KΩ 1% resistor	0.1% resistor desirable for accuracy
1	R10	Panasonic ERJ-6ENF1.87KV	1.87KΩ 1% resistor	0.1% resistor desirable for accuracy
1	R11	Panasonic ERJ-6ENF1.74KV	1.74KΩ 1% resistor	0.1% resistor desirable for accuracy
1	R7	Panasonic ERJ-6ENF2.00KV	2.00KΩ 1% resistor	0.1% resistor desirable for accuracy
1	R3	Panasonic ERJ-6ENF12.1KV	12.1KΩ 1% resistor	0.1% resistor desirable for accuracy
1	R4	Panasonic ERJ-6ENF10.0KV	10.0KΩ 1% resistor	0.1% resistor desirable for accuracy
1	R5	Panasonic ERJ-6GEY000V	0Ω 5% resistor	Resistor raises V_{OUT} 25mV/5Ω
1	R6	Panasonic ERJ-6GEY047V	47Ω 5% resistor	
1	R2	R_{SENSE} (Lin)	7mΩ MnCu or Copel resistor	
1	U1	Fairchild Semiconductor RC5036M	Dual Regulator for P55—switching regulator + LDO linear regulator	

Table 2. Switching Regulator Components Selection Table

Output Voltage	Output Current	C_{IN} Sanyo 10MV1200GX	C_{OUT} Sanyo 6M1500GX	Power MOSFET (M1)
3.5	8	1x	2x	IRL3103
2.8	6	1x	2x	IRL3103
2.9	6.25	1x	2x	IRL3103
2.9	7.5	1x	2x	IRL3103
3.2	9.5	2x	4x	IRL3103
3.2	13	3x	6x	IRL3103
2.1	5.6	1x	2x	IRL3103
3.3	3	N/A	1x	MJE15028

RC5037

Adjustable Switching Regulator Controller

Features

- High power switch-mode DC-DC controller can provide in excess of 13A
- Output voltage adjustable from 1.5V to 3.6V
- 85% efficiency
- Cumulative accuracy < 3% over line, load, and temperature variations
- Overvoltage and short circuit protection
- Built-in soft start

Applications

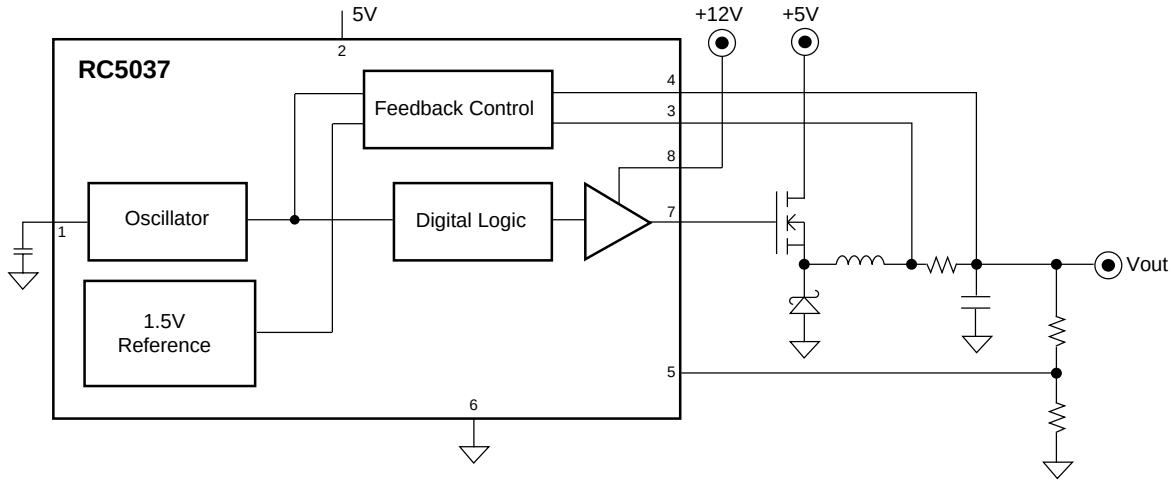
- I/O and AGP power for desktop computers
- High efficiency power for ASICs
- High efficiency power for DSPs
- Adjustable step-down power supplies

Description

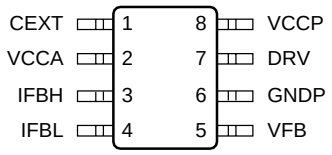
The RC5037 is a high power, switch-mode DC-DC controller that provides efficient power for all low-voltage applications. This controller has a built-in Soft Start feature which offers system protection during power-up by reducing both inrush current and output overshoot. When combined with the appropriate external circuitry, the RC5037 can deliver load currents as high as 13A at efficiencies as high as 88%. The RC5037 can generate output voltages from 1.5V up to 3.6V using external resistors.

The RC5037 is designed to operate in a constant on-time control mode under all load conditions. Its accurate low TC reference eliminates the need for precision external components in order to achieve the tight tolerance voltage regulation required by many applications. Short circuit current protection is provided through the use of a current sense resistor, while overvoltage protection is provided internally.

Block Diagram



Pin Assignments



Pin Descriptions

Pin Name	Pin Number	Pin Function Description
CEXT	1	**External capacitor.** A 180pF capacitor is connected to this pin as part of the constant on-time pulse width circuit. Careful layout of this pin is critical to system performance. See Applications Information for details.
VCCA	2	**Analog V_{CC}.** Power supply for regulator control circuitry and voltage reference. Connect to system 5V supply and decouple to ground with 0.1µF ceramic capacitor.
IFBH	3	**High side current feedback.** Pins 3 and 4 are used as the inputs for the current feedback control loop and as the short circuit current sense points. Careful layout of the traces from these pins to the current sense resistor is critical for optimal performance of the short circuit protection scheme. See Applications Information for details.
IFBL	4	**Low side current feedback.** See Applications Information for details.
VFB	5	**Voltage feedback.** Using two external resistors, this pin sets the output voltage level for the switching regulator.
GNDP	6	**Power Ground.** Connect to a low impedance ground. See Application Information for details.
DRV	7	**MOSFET driver output.** Connect this pin to the gate of the N-channel MOSFET Q1 as shown in Figure 12. The trace from this pin to the MOSFET gate should be kept as short as possible (less than 0.5"). See Applications Information for details.
VCCP	8	**Power V_{CC}.** Power supply for DRV output driver. Connect to system 12V supply with R-C filter shown in Figure 12. See Applications Information for details.

Absolute Maximum Ratings

Supply Voltages, VCCA	7V
Supply Voltages, VCCP	13V
Junction Temperature, T_J	+150°C
Storage Temperature, T_S	-65 to +150°C
Lead Soldering Temperature, 10 seconds	300°C
Thermal Resistance Junction-to-Ambient, Θ_{JA}	163°C/W

Note:
1. Functional operation under any of these conditions is not implied. Performance is guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Switching Regulator Supply, VCCA		4.75	5	5.25	V
Ambient Operating Temperature, T_A		0		70	°C
Gate Drive Supply, VCCP		9.5	12	12.6	V

Electrical Characteristics

(VCCA = 5V, VCCP = 12V, T_A = 25°C using circuit of Figure 1, unless otherwise noted)

The • denotes specifications which apply over the full ambient operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
Output Voltage			1.5		3.6	V
Output Temperature Drift	T_A = 0°C–70°C			40		ppm/°C
Line Regulation	VCCA = 4.75 to 5.25V, I_{LOAD} = 13A			3	5	mV
Load Regulation	I_{LOAD} = 0 to 5A or 5A to 13A			30	43	mV
V_{OUT} PSRR	VCCA = 4.75 to 5.25V		60			dB
Output Ripple, peak-peak	20MHz BW, I_{LOAD} = 13A			15		mV
Total DC Accuracy[1]		•		±55	±100	mV
Efficiency	I_{LOAD} = 5A		80	85		%
Output Driver Current	Open Loop	•	0.5			A
Short Circuit Threshold Voltage		•	70	90	100	mV
On Time Pulse Width[2]	C_{EXT} = 180pF			3.5		µs
VCCA Supply Current	Independent of load	•		5	15	mA
VCCP Supply Current	I_{LOAD} = 13A	•		20	25	mA

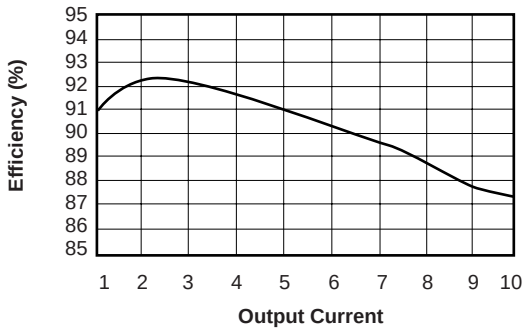
Notes:

1. Total DC accuracy includes setpoint accuracy, temperature drift, line and load regulation.
2. The on-time pulse width of the oscillator is set via external capacitor C_{EXT}.

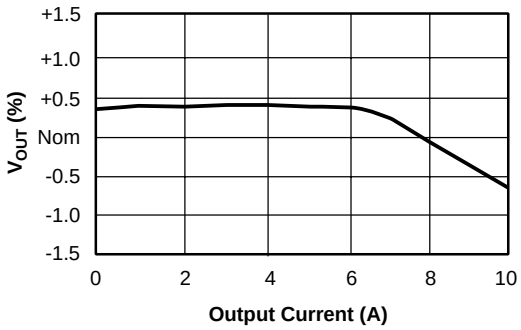
Typical Operating Characteristics

(VCCA = 5V, and T_A = +25°C using circuit in Figure 1, unless otherwise noted)

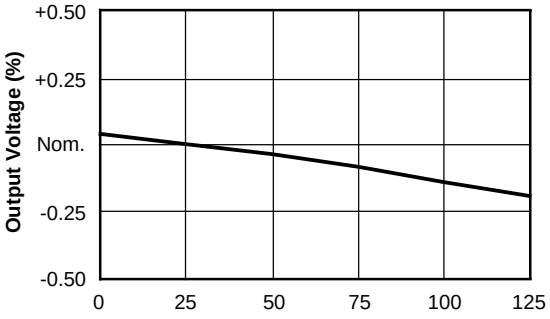
Efficiency vs. Output Current



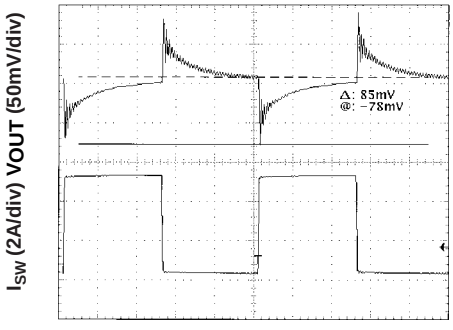
Output Voltage vs. Load



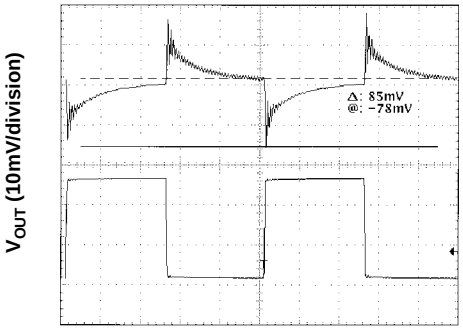
Output Voltage vs. Temperature, I_{OUT} = 10A



Transient Response, 0.5 to 5.5A

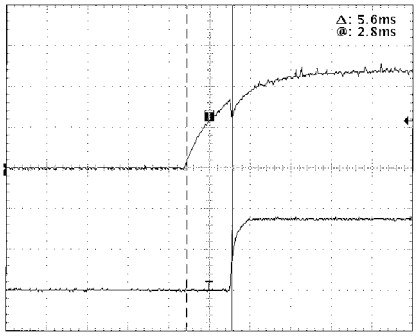


Output Ripple, I_{OUT} = 10A)



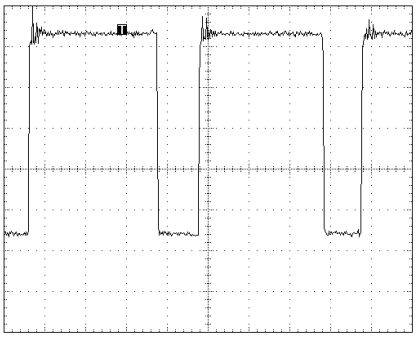
Typical Operating Characteristics (continued)

Output Startup, System Power-Up



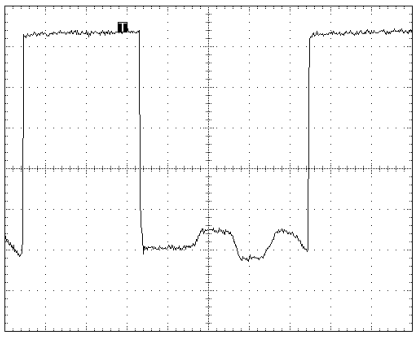
Time (5ms/division)

Pin 7 (DRV), 10A Load



Time (1µs/division)

Pin 7 (DRV), 0.1A Load



Time (1µs/division)

Application Circuit

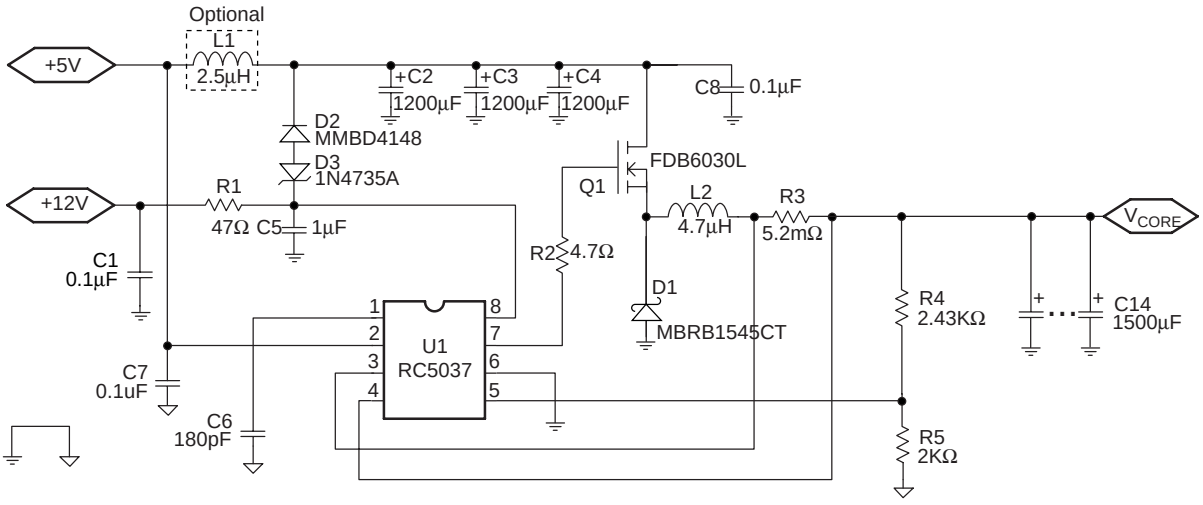


Figure 1. 13A at 3.3V Application Schematic

Table1. Bill of Materials for a RC5037 3.3V, 13A Application

Qty.	Reference	Manufacturer Part Order #	Description	Requirements and Comments
3	C1, C7-8	Any	100nF, 25V Capacitor	
3	C2-4	Sanyo 10MV1200GX	1200µF, 10V Aluminum Capacitor	I_{RMS} = 2A , See Equation (2) in Applications
1	C5	Any	1µF, 25V Capacitor	
1	C6	Any	180pF, 50V Capacitor	C0G
6	C9-14	Sanyo 6MV1500GX	1500µF, 6.3V Aluminum Capacitor	ESR = 44mΩ
1	R1	Any	47.5Ω	
1	R2	Any	4.75Ω	
1	R3	N/A	5.2mΩ, 1W Resistor	PCB Trace Resistor, see Eauation (3) Applications
1	R4	Any	2.43KΩ	
1	R5	Any	2KΩ	
1	D1	Motorola MBRB1545CT	15A, 45V Schottky	
1	D2	Fairchild MMBD4148	Signal Diode	
1	D3	Motorola 1N4735A	6.2V Zener	
1	Q1	Fairchild FDB6030L	30V, 14mΩ Logic Level MOSFET	
Optional	L1	Any	2.5µH Inductor	I_{SAT} > 8A
1	L2	Any	4.7µH Inductor	I_{SAT} > 13A
1	U1	Fairchild RC5037M	PWM Controller	

Application Information

The RC5037 contains a precision trimmed zero TC voltage reference, a constant-on-time architecture controller, a high current output driver, and a low offset error amp. The detailed block diagram in Figure 1 shows how the RC5037 works together with external components to achieve a high-performance switching power supply.

Switch-Mode Control Loop

The main control loop for the switch-mode converter consists of a current conditioning amplifier and a voltage conditioning amplifier. The voltage amplifier compares the voltage from the internal reference with the converter's output voltage divided by an external resistor divider. The current amplifier senses the current by comparing the voltages at the IFBH and IFBL pins, which are attached to either side of the current sense resistor. The signals from the voltage and current amplifiers are summed together, the result being used to control the off-time of the oscillator. The current feedback signal is also used as part of the RC5037 short-circuit protection.

High Current Output Drivers

The RC5037 high current output driver (DRV) contains high speed bipolar power transistors configured in a push-pull configuration. The output driver is capable of supplying 0.5A of current in less than 100ns. The driver's power and ground are separated from the overall chip power and ground for added switching noise immunity.

Internal Reference

The reference in the RC5037 is a precision band-gap type reference. Its temperature coefficient is trimmed to provide a near zero TC.

Constant-On-Time Oscillator

The RC5037 switch-mode oscillator is designed as a fixed on-time, variable off-time oscillator. The constant-on-time oscillator consists of a comparator, an external capacitor, a fixed current source, a variable current source, and an analog switch that selects between two threshold voltages for the comparator. The external timing capacitor is alternately

charged and discharged through the enabling and disabling of the fixed current source. The variable current source is controlled from the error inputs that are received from the current and voltage feedback signals. The oscillator off-time is controlled by the amount of current that is available from the variable current source to charge the external capacitor up to the high threshold level of the comparator. The on-time is set by the constant current source that discharges the external capacitor voltage down to the lower comparator threshold.

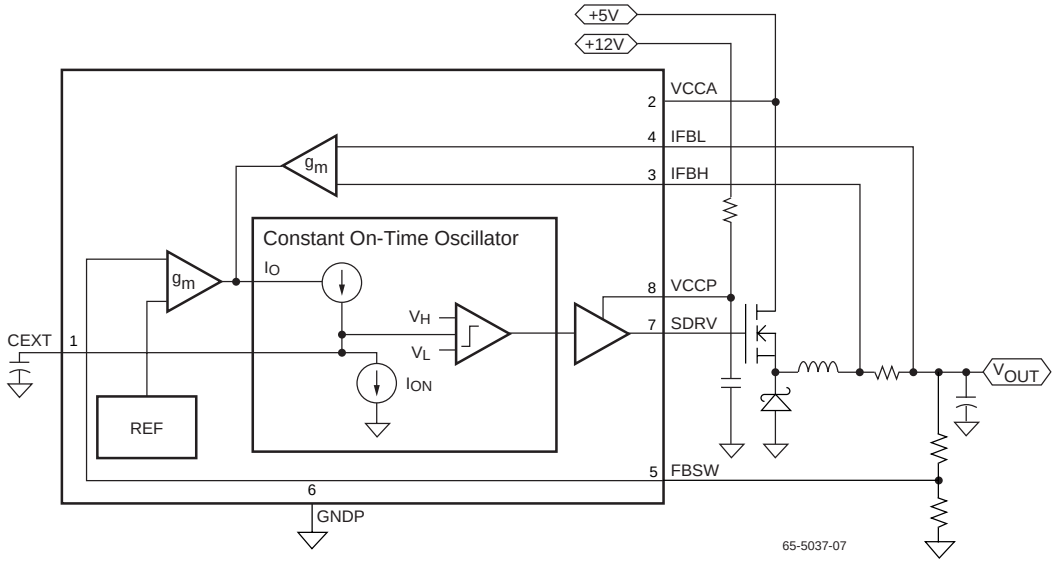


Figure 2. RC5037 Detailed Block Diagram

Output Voltage Selection

The RC5037 precision reference is trimmed to be 1.5V nominally. When using the RC5037, the system designer has complete flexibility in choosing the output voltage for one regulator from 1.5V to 3.6V. This is done by appropriately selecting the feedback resistors. These could be 0.1% resistors to realize optimum output accuracy. The following equations determines the output voltage of the regulator:

$$V_{OUT} = 1.5 \times \left(\frac{R4 + R5}{R5}\right) \quad (1)$$

For example, for 3.3V:

$$V_{OUT} = 1.5 \times \left(\frac{R4 + R5}{R5}\right) = 1.5 \times \left(\frac{2.43k + 2.0k}{2.0k}\right) = 3.3V$$

Input Capacitors

The number of input capacitors required for the RC5037 is dependent on their ripple current rating, which assures their rated life. The number required may be determined by

$$\text{No. Caps} = \frac{I_{out} \overset{*}{\sqrt{DC - DC^2}}}{I_{rating}} \quad (2)$$

where the duty cycle DC = V_{out}/V_{in}. For example, with a 1.5V output at 10A, 5V input, and using the Sanyo capacitors specified in Table 1 which have a 2A ripple current rating, we have DC = 1.5/5 = 0.3, and

$$\text{No. Caps} = \frac{10^{*}\sqrt{0.03 - 0.3^2}}{2} = 2.29$$

so that we need 3 input capacitors.

Short Circuit Considerations

The RC5037 uses a current sensing scheme to limit the load current if an output fault condition occurs. The current sense resistor carries the peak current of the inductor, which is greater than the maximum load current due to ripple current flowing in the inductor. The RC5037 will begin to limit the output current to the load by reducing the duty cycle of the top-side MOSFET driver when the voltage across the current-sense resistor exceeds the short circuit comparator threshold voltage (V_{th}). When this happens the output voltage will temporarily go out of regulation. As the voltage across the sense resistor becomes larger, the duty cycle of the top-side MOSFET will continue to be reduced until the current limit value is reached. At this point, the RC5037 will continuously deliver the limit current at a reduced output voltage level. The short circuit comparator threshold voltage is typically 90mV, with a tolerance of ±10mV. The ripple current flowing through the inductor in Figure 1 is 0.6A. Refer to Application Note AM-53 for detailed discussions. The sense resistor value can be approximated as follows:

$$R_{SENSE} = \frac{V_{th,min}}{I_{PK}} \times (1 - TF) = \frac{V_{th,min}}{0.6A + I_{LOAD,MAX}} \times (1 - TF) \quad (3)$$

where TF = Tolerance Factor for the sense resistor and 0.6A accounts for the inductor ripple current.

Since the value of the sense resistor is often less than 10mΩ, care should be taken in the layout of the PCB. Trace resistance can contribute significant errors. The traces to the IFBH and IFBL pins of the RC5037 should be Kelvin connected to the pads of the current-sense resistor. To minimize the influence of noise, the two traces should be run next to each other.

Schottky Diode

In Figure 1, MOSFET Q1 and flyback diode D1 are used as complementary switches in order to maintain a constant current through the output inductor L2. As a result, D1 will have to carry the full current of the output load when the power MOSFET is turned off. The power in the diode is a direct function of the forward voltage at the rated load current during the off time of the FET. The following equation can be used to estimate the diode power:

$$P_{DIODE} = I_D \times V_D \times (1 - DutyCycle)$$

where I_D is the forward current of the diode, V_D is the forward voltage of the diode, and DutyCycle is defined the same as

$$\text{Duty Cycle} = \frac{Vout}{Vin}$$

For the Motorola MBRB1545CT Rectifier in Figure 1,

$$P_{DIODE} = 10A \times 0.65 \times (1 - 73.1\%) = 1.75W$$

It is recommended that the diode T0-220 package be attached to a heatsink.

Board Design Considerations

MOSFET Placement

Placement of the power MOSFET is critical in the design of the switch-mode regulator. The MOSFET should be placed in such a way as to minimize the length of the gate drive path from the RC5037 SDRV pin. This trace should be kept under 0.5" for optimal performance. Excessive lead length on this trace will cause high frequency noise resulting from the parasitic inductance and capacitance of the trace. Since this voltage can transition nearly 12V in around 100nsec, the resultant ringing and noise would be very difficult to suppress. This trace should be routed on one layer only and kept well away from the “quiet” analog pins of the device: CEXT, IFBH, IFBL, and GND. Refer to Figure 2. A 4.7Ω resistor in series with the MOSFET gate can decrease this layout criticality. Refer to Figure 1.

Inductor and Schottky Diode Placement

The inductor and fly-back Schottky diode need to be placed close to the source of the power MOSFET for the same reasons stated above. The node connecting the inductor and Schottky diode will swing between the drain voltage of the FET and the forward voltage of the Schottky diode. It is recommended that this node be converted to a plane if possible. This node will be part of the high current path in the design, and as such it is best treated as a plane in order to minimize the parasitic resistance and inductance on that node. Since most PC board manufacturers utilize 1/2 oz copper on the top and bottom signal layers of the PCB, it is not recommended to use these layers to route the high current portions of the regulator design. Since it is more common to use 1 oz. copper on the PCB inner layers, it is recommended to use those layers to route the high current paths in the design.

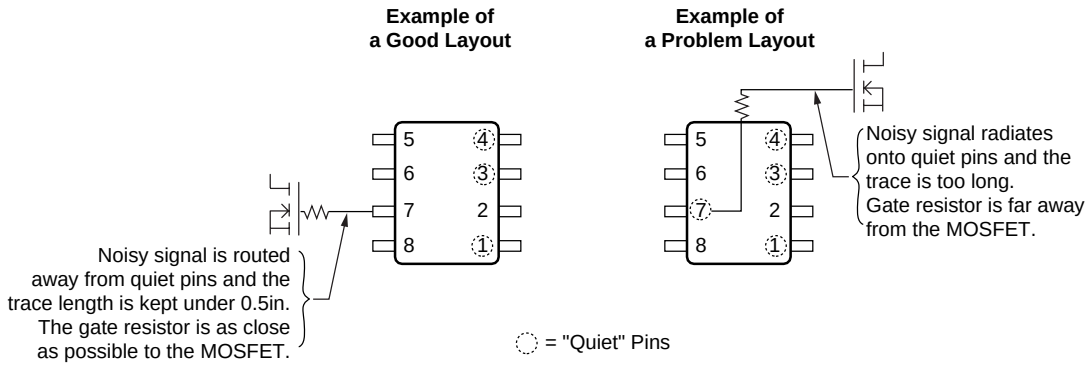


Figure 3. Examples of good and poor layouts

Power and Ground Connections

The connection of VCCA to the 5V power supply plane should be short and bypassed with a 0.1µF directly at the VCCA pin of the RC5037. The ideal connection would be a via down to the 5V power plane. A similar arrangement should be made for the VCCP pin that connects to +12V. Each ground should have a separate via connection to the ground plane below.

A 12V power supply is used to bias the VCCP. A 47Ω resistor is used to limit the transient current into VCCP. A 1uF capacitor filter is used to filter the VCCP supply and source the transient current required to charge the MOSFET gate capacitance. This method provides sufficiently high gate bias voltage to the MOSFET (V_{GS}), and therefore reduces $R_{DS(ON)}$ of the MOSFET and its power loss.

Figure 4 provides about 5V of gate bias which works well when using typical logic-level MOSFETs. Non-logic-level MOSFETs should not be used because of their higher $R_{DS(ON)}$.

MOSFET Gate Bias

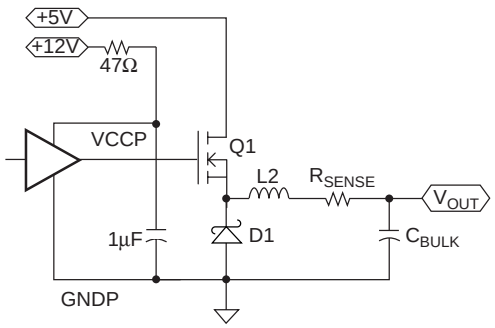


Figure 4. 12V Gate Bias Configuration

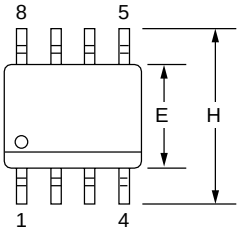
Mechanical Dimensions

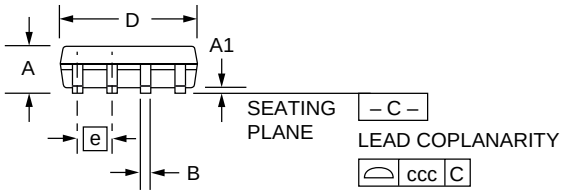
8 Lead SOIC Package

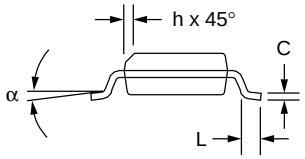
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.20	0.25	5
D	.189	.197	4.80	5.00	2
E	.150	.158	3.81	4.01	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	8		8		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Ordering Information

Product Number	Package
RC5037M	8 pin SOIC

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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

RC5037

Adjustable Switching Regulator

Features

- High power switched-mode DC-DC controller can control in excess of 13A
- Output voltage adjustable from 1.5V to 3.6V
- 85% efficiency
- Cumulative accuracy < 3% over line, load, and temperature variations
- Overvoltage and short circuit protection
- Built-in soft start

Applications

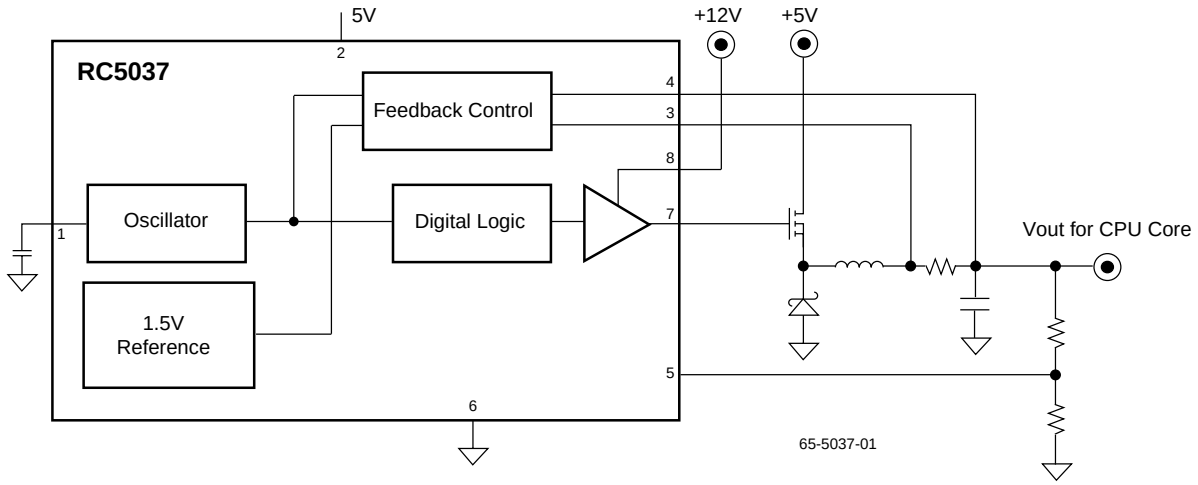
- Precision 2.xV CPU core regulator for Pentium® MMX™ processes
- Precision 2.xV or 3.xV CPU core regulator for AMD-K6™ MMX and Cyrix 6x86MX™ (M2) processors

Description

The RC5037 is a high power, switch-mode DC-DC controller that provides an accurate output for high-end microprocessors CPU voltage. This controller has a built-in Soft Start feature which offers system protection during power-up by reducing both inrush current and output overshoot. When combined with the appropriate external circuitry, the RC5037 can deliver load currents as high as 13A at efficiencies as high as 88%. The RC5037 can generate output voltages from 1.5V up to 3.6V using external resistors.

The RC5037 is designed to operate in a “constant on-time” (patent pending) control mode under all load conditions. Its accurate low TC reference eliminates the need for precision external components in order to achieve the tight tolerance voltage regulation required by most CPU-based applications. Short circuit current protection is provided through the use of a current sense resistor, while overvoltage protection is provided internally.

Block Diagram



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6x86MX is a trademark of Cyrix Corporation.

Functional Description

The RC5037 contains a precision trimmed zero TC voltage reference, a constant-on-time architecture controller, a high current output driver, and a low offset op-amp. The detailed block diagram in Figure 1 shows how the RC5037 works together with external components to achieve a high-performance switching power supply.

Switch-Mode Control Loop

The main control loop for the switch-mode converter consists of a current conditioning amplifier and a voltage conditioning amplifier. The voltage amplifier compares the voltage from the internal reference with the converter's output voltage divided by an internal resistor divider. The current amplifier senses the current by comparing the voltages at the IFBH and IFBL pins, which are attached to either side of the current sense resistor. The signals from the voltage and current amplifiers are summed together, the result being use to control the off-time of the oscillator. The current feedback signal is also used as part of the RC5037 short-circuit protection.

High Current Output Drivers

The RC5037 high current output driver (SDRV) contains high speed bipolar power transistors configured in a push-pull configuration. The output driver is capable of supplying 0.5A of current in less than 100ns. The driver's power and ground are separated from the overall chip power and ground for added switching noise immunity.

Internal Reference

The reference in the RC5037 is a precision band-gap type reference. Its temperature coefficient is trimmed to provide a near zero TC.

Constant-On-Time Oscillator

The RC5037 switch-mode oscillator is designed as a fixed on-time, variable off-time oscillator. The constant-on-time oscillator consists of a comparator, an external capacitor, a fixed current source, a variable current source, and an analog switch that selects between two threshold voltages for the comparator. The external timing capacitor is alternately charged and discharged through the enabling and disabling of the fixed current source. The variable current source is controlled from the error inputs that are received from the current and voltage feedback signals. The oscillator off-time is controlled by the amount of current that is available from the variable current source to charge the external capacitor up to the high threshold level of the comparator. The on-time is set by the constant current source that discharges the external capacitor voltage down to the lower comparator threshold.

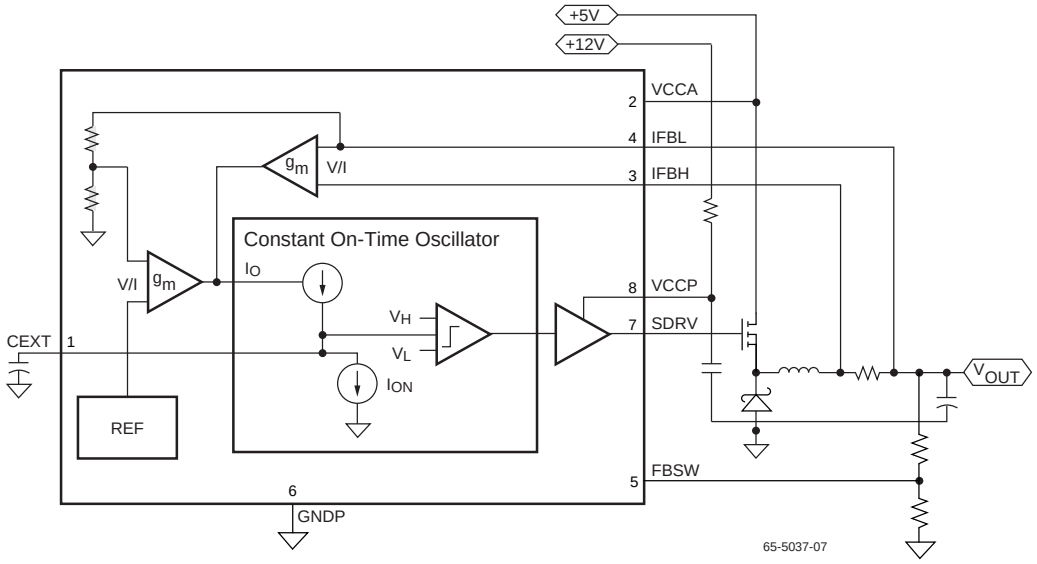
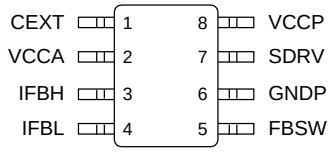


Figure 1. RC5037 Detailed Block Diagram

Pin Assignments



RC5037

Pin Descriptions

Pin Name	Pin Number	Pin Function Description
CEXT	1	**External capacitor.** A 180pF capacitor is connected to this pin as part of the constant on-time pulse width circuit. Careful layout of this pin is critical to system performance. See Applications Information for details.
VCCA	2	**Switching Regulator V_{CC}.** Power supply for switching regulator control circuitry and voltage reference. Connect to system 5V supply and decouple to ground with 0.1μF ceramic capacitor.
IFBH	3	**High side current feedback for switching regulator.** Pins 3 and 4 are used as the inputs for the current feedback control loop and as the short circuit current sense points. Careful layout of the traces from these pins to the current sense resistor is critical for optimal performance of the short circuit protection scheme. See Applications Information for details.
IFBL	4	**Low side current feedback for switching regulator.** See Applications Information for details.
FBSW	5	**Voltage feedback for switching regulator.** Using two external resistors, this pin sets the output voltage level for the switching regulator.
GNDP	6	**Power Ground.** Connect to a low impedance ground. See Application Information for details.
SDRV	7	**FET driver output for switching regulator.** Connect this pin to the gate of the N-channel MOSFET Q1 as shown in Figure 12. The trace from this pin to the MOSFET gate should be kept as short as possible (less than 0.5"). See Applications Information for details.
VCCP	8	**Switching regulator gate drive V_{CC}.** Power supply for SDRV output driver. Connect to system 12V supply with R-C filter shown in Figure 12. See Applications Information for details.

Absolute Maximum Ratings

Supply Voltages, VCCA	7V
Supply Voltages, VCCP	13V
Junction Temperature, T_J	+150°C
Storage Temperature, T_S	-65 to +150°C
Lead Soldering Temperature, 10 seconds	300°C

Note:
1. Functional operation under any of these conditions is not implied. Performance is guaranteed only if Operating Conditions are not exceeded.

Preliminary Information

Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Switching Regulator Supply, VCCA		4.75	5	5.25	V
Ambient Operating Temperature, T_A		0		70	°C
Gate Drive Supply, VCCP		9.5	12	12.6	V

Electrical Characteristics

(VCCA = 5V, VCCP = 12V, T_A = 25°C using circuit of Figure 10, unless otherwise noted)

The • denotes specifications which apply over the full ambient operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
Initial Accuracy[1]	I_{LOAD} = 13A		1.5		3.6	V
Output Temperature Drift	T_A = 0˚C–70˚C			40		ppm/˚C
Line Regulation	VCCA = 4.75 to 5.25V, I_{LOAD} = 13A			3	5	mV
Load Regulation	I_{LOAD} = 0 to 5A or 5A to 13A			30	43	mV
V_{OUT} PSRR			60			dB
Output Ripple, peak-peak	20MHz BW, I_{LOAD} = 13A			15		mV
Cumulative DC Accuracy[2]		•		±55	±100	mV
Efficiency	I_{LOAD} = 5A	•	80	85		%
Output Driver Current	Open Loop	•	0.5			A
Short Circuit Threshold Voltage		•	80	90	100	mV
On Time Pulse Width[3]	C_{EXT} = 180pF			3.5		µs
Thermal Impedance, θ_{JA}		•		140		°C/W
VCCA Supply Current	Independent of load	•		5	10	mA
VCCP Supply Current	I_{LOAD} = 13A	•		20	25	mA
Internal Power Dissipation	I_{LOAD} = 13A	•		125		mW

Notes:

1. Initial accuracy is the initial output voltage variability under the specified conditions.
2. Cumulative DC accuracy includes setpoint accuracy, temperature drift, line and load regulation.
3. The on-time pulse width of the oscillator is set via external capacitor C_{EXT}.

Preliminary Information

Typical Operating Characteristics

(VCCA = 5V, and T_A = +25°C using circuit in Figure 10, unless otherwise noted)

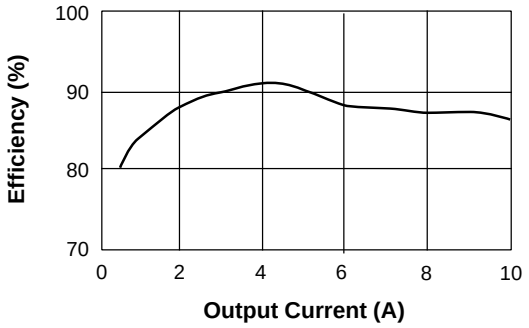


Figure 2. Switcher Efficiency vs. Output Current

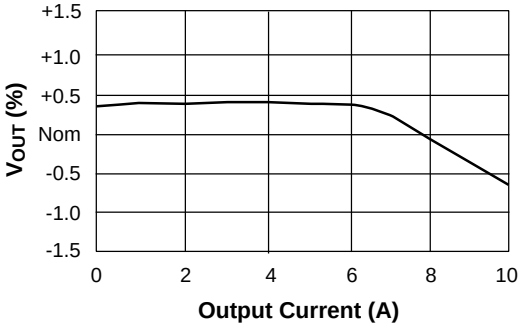


Figure 3. Switcher Output Voltage vs. Load

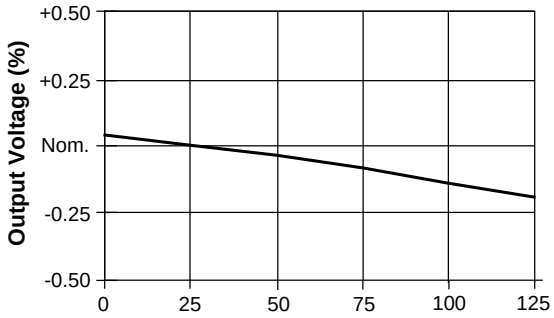


Figure 4. Output Voltage vs. Temperature ($I_{I/O}$ = 10A)

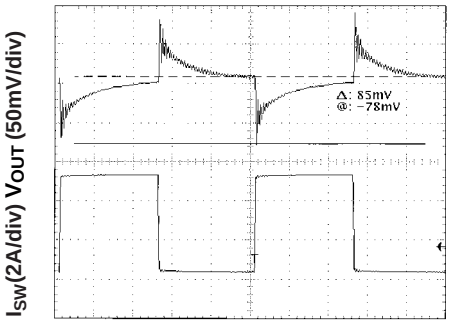


Figure 5. Switcher Transient Response (0.5 to 5.5A Load Step)

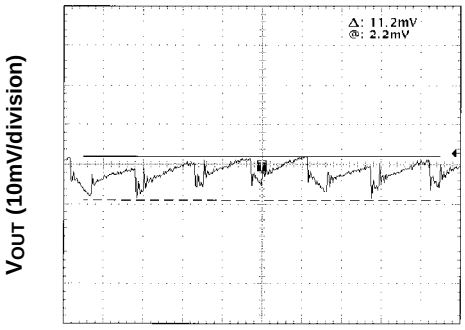


Figure 6. Switcher Output Ripple (BW = 20MHz, $I_{I/O}$ = 10A)

65-5037-03

Preliminary Information

Typical Operating Characteristics (continued)

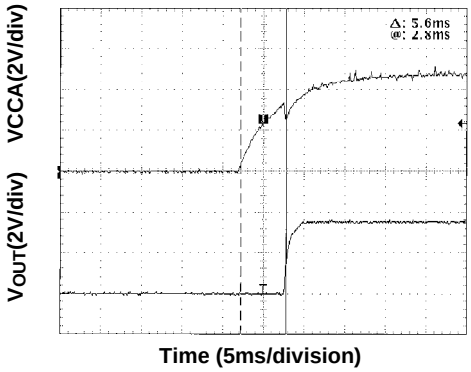


Figure 7. Switcher Turn-on Response

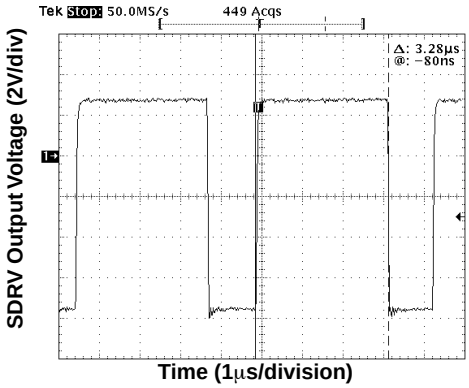


Figure 8. Pin 7 (SDRV) at a 10 Amp Load

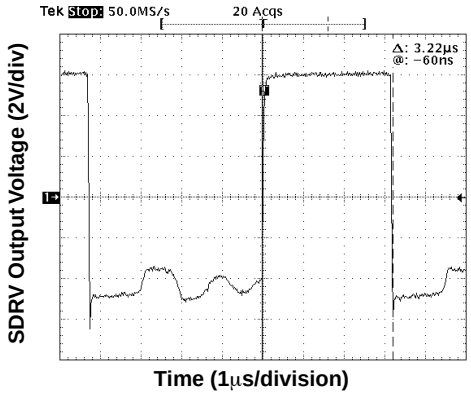


Figure 9. Pin 7 (SDRV) at a 0.1 Amp Load

Test Circuit Configurations

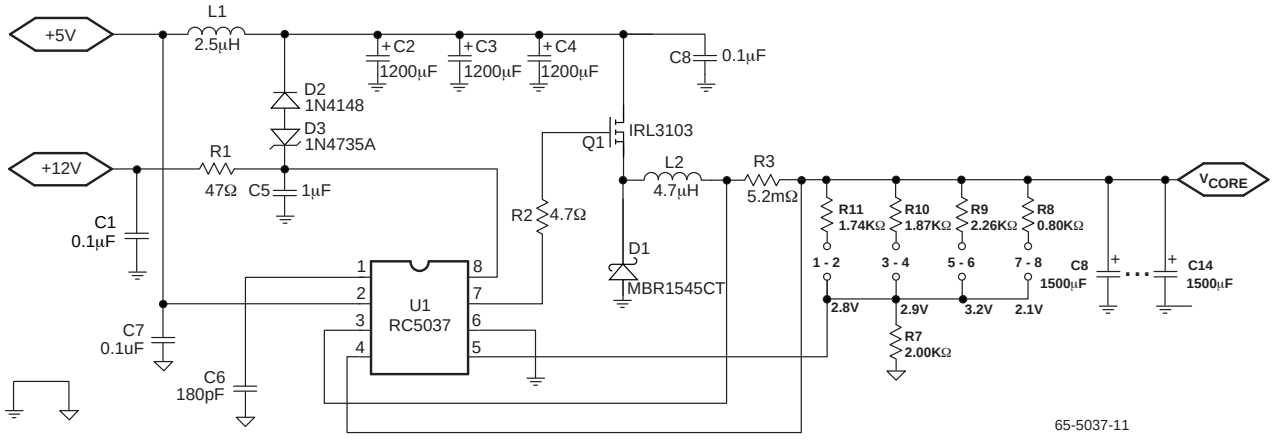


Figure 10. 13A Application Schematic

Table 1. Bill of Materials for a RC5037 13A Application

Qty.	Reference	Manufacturer	Part Number	Description
3	C1, C7, C8	Rohm	MCH212F104ZP	100nF +80/-20%, 25V Z5U Ceramic Capacitor
2	C2, C3, C4	Sanyo	10MV1200GX	1200μF, 10V 44mΩ Aluminum Capacitor
1	C5	Rohm	MCH312F105ZP	1μF +80/-20%, 25V Z5U Ceramic Capacitor
1	C6	Rohm	MCH215A181JK	180pF ± 5%, 50V COG Ceramic Capacitor
2	C9, C10, C11, C12, C13, C14	Sanyo	6MV1500GX	1500μF, 6.3V, 44mΩ Aluminum Capacitor
1	R1	Panasonic	ERJ-6GEYJ470	47Ω ± 5%, 1/10W Resistor
1	R2	Panasonic	ERJ-6GEYJ4R7	4.7Ω ± 5%, 1/10W Resistor
1	R3	Fairchild Semiconductor	RC10-52	5.2mΩ, 1W Resistor
1	R7	Panasonic	ERJ-ENF 2.0 0KV	0.1% resistor desirable for accuracy
1	R8	Panasonic	ERJ-ENF 0.80KV	0.1% resistor desirable for accuracy
1	R9	Panasonic	ERJ-ENF 2.26KV	0.1% resistor desirable for accuracy
1	R10	Panasonic	ERJ-ENF 1.87KV	0.1% resistor desirable for accuracy
1	R11	Panasonic	ERJ-ENF 1.74KV	0.1% resistor desirable for accuracy
1	D1	Motorola	MBR1545CT	15A, 45V Schottky Diode
1	D2	Any	1N4148	Small Signal Diode
1	D3	Motorola	1N4735A	6.2V ± 5%, 1W, Zener Diode
1	Q1	IR	IRL3103	30V, 14mΩ Logic Level MOSFET
1	L1	Panasonic	EXC-ELDR35V	2.5μH Bead Inductor
1	L2	Pulse	PE-53682	4.7μH, I_{SAT} > 10A Inductor
1	U1	Fairchild Semiconductor	RC5037M	Adjustable Switching Regulator

Table 2. Switching Regulator Components Selection Table

Output Voltage	Output Current	C_{IN} Sanyo 10MV1200GX	C_{OUT} Sanyo 6M1500GX	Power MOSFET (M1)
3.5	8	1x	2x	IRL3103
2.8	6	1x	2x	IRL3103
2.9	6.25	1x	2x	IRL3103
2.9	7.5	1x	2x	IRL3103
3.2	9.5	2x	4x	IRL3103
3.2	13	3x	6x	IRL3103
2.1	5.6	1x	2x	IRL3103
3.3	3	N/A	1x	Si9936

Applications Information

The following discussion is intended to be an abbreviated list of design considerations regarding the RC5037 as used in a typical processor motherboard application. For a more thorough discussion of applicable specifications and layout considerations relating to the Intel Pentium P55C processor, please refer to Application Note 48.

Output Voltage Selection

Feedback Voltage Divider

The RC5037 precision reference is trimmed to be 1.5V nominally. When using the RC5037, the system designer has complete flexibility in choosing the output voltage for each regulator from 1.5V to 3.6V. This is done by appropriately selecting the feedback resistors. These should be 0.1% resis tors to realize optimum output accuracy. The following equations determine the output voltages of the two regulators:

Preliminary Information

Switching Regulator

$$V_{OUT} = 1.5 \times \left(\frac{Rx + R7}{R7}\right)$$

where Rx: R8, R9, R10, and R11.

For example, for 2.8V:

$$V_{OUT} = 1.5 \times \left(\frac{R11 + R7}{R7}\right) = 1.5 \times \left(\frac{1.74k + 2.0k}{2.0k}\right) = 2.8V$$

Short Circuit Considerations

The RC5037 uses a current sensing scheme to limit the load current if an output fault condition occurs. The current sense resistor carries the peak current of the inductor, which is greater than the maximum load current due to ripple current flowing in the inductor. The RC5037 will begin to limit the output current to the load by reducing the duty cycle of the top-side FET driver when the voltage across the current-sense resistor exceeds the short circuit comparator threshold voltage (V_{th}). When this happens the output voltage will temporarily go out of regulation. As the voltage across the sense resistor becomes larger, the duty cycle of the top-side MOSFET will continue to be reduced until the current limit value is reached. At this point, the RC5037 will continuously deliver the limit current at a reduced output voltage level. The short circuit comparator threshold voltage is typically 90mV, with a tolerance of ±10mV. The ripple current flowing through the inductor in Figure 10 is 0.6A. There needs to be a 29% margin for the sense resistor when using a motherboard PC trace resistor. Refer to Application Note 48 for detailed discussions. The sense resistor value can be approximated as follows:

$$R_{SENSE} = \frac{V_{th,min}}{I_{PK}} \times (1 - TF) = \frac{V_{th,min}}{0.6A + I_{LOAD,MAX}} \times (1 - TF)$$

Where TF = Tolerance Factor for the sense resistor and 0.6A accounts for the inductor ripple current.

There are several different types of sense resistors. Table 3 describes the tolerance, size, power capability, temperature coefficient and cost of various types of sense resistors.

Based on the Tolerance in Table 3:

For an embedded PC trace resistor:

$$R_{SENSE} = \frac{0.08}{0.6 + I_{LOAD,MAX}} \times .71$$

For a discrete Copel resistor:

$$R_{SENSE} = \frac{0.08}{0.6 + I_{LOAD,MAX}} \times .90$$

Table 4 lists recommended values for sense resistors for various load currents using an embedded PC trace resistor or a discrete resistor. If the calculated value is not available, round down.

Table 4. R_{SENSE} for Various Load Currents, Switching Regulator

$I_{LOAD, MAX}$ (A)	R_{SENSE} PC Trace Resistor (mΩ)	R_{SENSE} Discrete Resistor (mΩ)
3	15.8	20.0

Table 3. Comparison of Sense Resistors

	Motherboard Trace Resistor	Discrete Iron Alloy resistor (IRC)	Discrete Metal Strip surface mount resistor (Dale)	Discrete MnCu Alloy wire resistor	Discrete CuNi Alloy wire resistor (Copel)
Tolerance Factor (TF)	±29%	±5% (±1% available)	±1%	±10%	±10%
Size (L x W x H)	2" x 0.2" x 0.001" (1 oz Cu trace)	0.45" x 0.065" x 0.2"	0.25" x 0.125" x 0.025"	0.2" x 0.04" x 0.16"	0.2" x 0.04" x 0.1"
Power capability	>50A/in	1 watt (3 and 5 watts available)	1 watt (3 and 5 watts available)	1 watt	1 watt
Temperature Coefficient	+4,000 ppm	+30 ppm	±75 ppm	±30 ppm	±20ppm
Cost@10,000 piece quantity	Low; included in motherboard	$0.31	$0.47	$0.09	$0.09

5	10.1	12.9
6	8.6	10.9
7	7.5	9.5
8	6.6	8.4
9	5.9	7.5
10	5.4	6.8
13	4.2	5.3

Since the value of the sense resistor is often less than 10mΩ, care should be taken in the layout of the PCB. Trace resistance can contribute significant errors. The traces to the IFBH and IFBL pins of the RC5037 should be Kelvin connected to the pads of the current-sense resistor. To minimize the influence of noise, the two traces should be run next to each other.

Thermal Design Considerations

Good thermal management is critical in the design of high current regulators. System reliability will be degraded if the component temperatures become excessive. The following guide should serve as a reference for proper thermal management.

MOSFET Temperature

The maximum power dissipation of the MOSFET can be calculated by using the following formula:

$$P_D = \frac{T_{J(MAX)} - T_A}{\Theta_{JA}}$$

For IRL3103, Θ_{JA} is 62°C/W. For reliability the junction temperature of the MOSFET should not exceed 120°C. Assuming that the ambient temperature is 40°C, then the maximum power dissipation without heat sink is calculated as:

$$P_D = \frac{120 - 40}{62} = 1.29W$$

The power that the MOSFET dissipates at 10A load is calculated as follows:

$$P_{MOSFET} = I_{LOAD}^2 \times R_{DS(ON)} \times (\text{Duty Cycle}) + \frac{V_{IN} \times I_{LOAD}}{6} \times (t_r + t_f) \times f$$

$$\text{Duty Cycle} = \frac{V_{OUT} + V_D}{V_{IN} + V_D - (I_{LOAD} \times R_{DS(ON)})}$$

where V_D is the forward voltage of the Schottky diode used.

Using the above formula, for V_{out} = 3.3V, I_{LOAD} = 10A

$$\text{Duty Cycle} = \frac{3.3 + 0.65}{5 + 0.65 - (10 \times 0.023)} = 73.1\%$$

$$P_{MOSFET} = (10A)^2 \times 0.025\Omega \times 73.1\% + \frac{5V \times 10A}{6} \times (210ns + 54ns) \times 300KHz$$

$$P_{MOSFET} = 2.49W$$

Since the power at 10A is higher than the thermal guideline, a heat sink is required.

Schottky Diode

In Figure 10, MOSFET Q1 and flyback diode D1 are used as complementary switches in order to maintain a constant current through the output inductor L2. As a result, D1 will have to carry the full current of the output load when the power MOSFET is turned off. The power in the diode is a direct function of the forward voltage at the rated load current during the off time of the FET. The following equation can be used to estimate the diode power:

$$P_{DIODE} = I_D \times V_D \times (1 - \text{DutyCycle})$$

where I_D is the forward current of the diode, V_D is the forward voltage of the diode, and DutyCycle is defined the same as above.

For the Motorola MBR1545CT Rectifier in Figure 10,

$$P_{DIODE} = 10A \times 0.65 \times (1 - 73.1\%) = 1.75W$$

It is recommended that the diode T0-220 package be attached to a heatsink.

Board Design Considerations

MOSFET Placement

Placement of the power MOSFET is critical in the design of the switch-mode regulator. The FET should be placed in such a way as to minimize the length of the gate drive path from the RC5037 SDRV pin. This trace should be kept under 0.5" for optimal performance. Excessive lead length on this trace will cause high frequency noise resulting from the parasitic inductance and capacitance of the trace. Since this voltage can transition nearly 12V in around 100nsec, the resultant ringing and noise would be very difficult to suppress. This trace should be routed on one layer only and kept well away from the “quiet” analog pins of the device: CEXT, IFBH, IFBL, and GND. A 4.7Ω resistor in series with the MOSFET gate can decrease this layout criticality. Refer to Figure 10.

Inductor and Schottky Diode Placement

The inductor and fly-back Schottky diode need to be placed close to the source of the power MOSFET for the same reasons stated above. The node connecting the inductor and Schottky diode will swing between the drain voltage of the FET and the forward voltage of the Schottky diode. It is recommended that this node be converted to a plane if possible. This node will be part of the high current path in the design, and as such it is best treated as a plane in order to minimize the parasitic resistance and inductance on that node. Since most PC board manufacturers utilize 1/2 oz copper on the

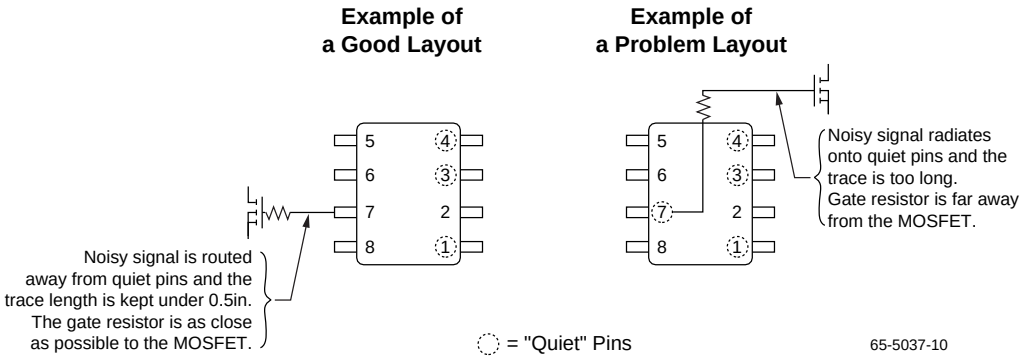


Figure 11. Examples of good and poor layouts

top and bottom signal layers of the PCB, it is not recommended to use these layers to route the high current portions of the regulator design. Since it is more common to use 1 oz. copper on the PCB inner layers, it is recommended to use those layers to route the high current paths in the design.

Power and Ground Connections

The connection of VCCA to the 5V power supply plane should be short and bypassed with a 0.1µF directly at the VCCA pin of the RC5037. The ideal connection would be a via down to the 5V power plane. A similar arrangement should be made for the VCCP pin that connects to +12V. Each ground should have a separate via connection to the ground plane below.

A 12V power supply is used to bias the VCCP. A 47Ω resistor is used to limit the transient current into VCCP. A 1uF capacitor filter is used to filter the VCCP supply and source the transient current required to charge the MOSFET gate capacitance. This method provides sufficiently high gate bias voltage to the MOSFET (V_{GS}), and therefore reduces $R_{DS(ON)}$ of the MOSFET and its power loss.

Figure 12 provides about 5V of gate bias which works well when using typical logic-level MOSFETs, as shown in Figure 13. Non-logic-level MOSFETs should not be used because of their higher $R_{DS(ON)}$.

MOSFET Gate Bias

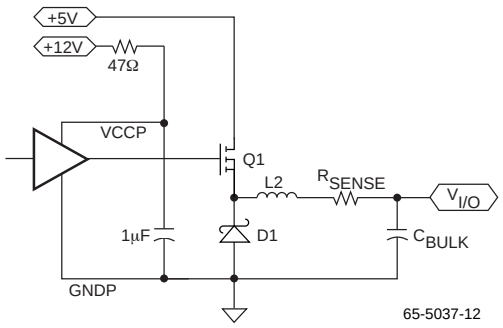


Figure 12. 12V Gate Bias Configuration

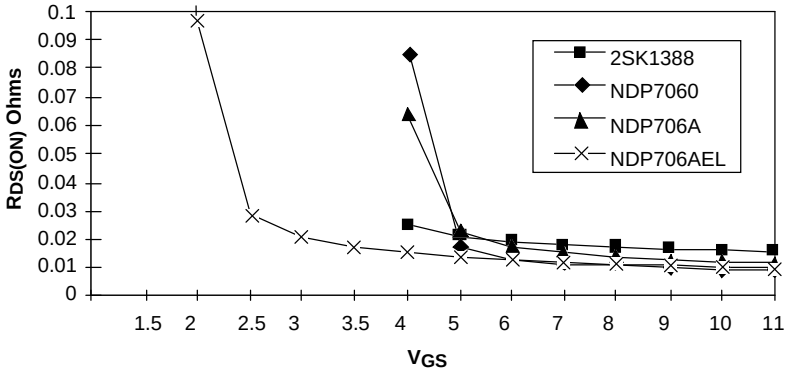


Figure 13. $R_{DS(ON)}$ vs. V_{GS} for Selected Logic-Level MOSFETs

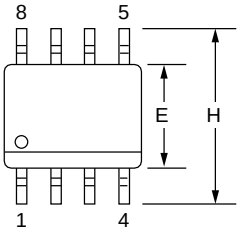
Mechanical Dimensions

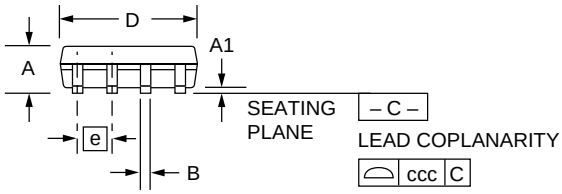
8 Lead SOIC Package

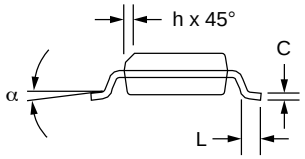
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.20	0.25	5
D	.189	.197	4.80	5.00	2
E	.150	.158	3.81	4.01	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	8		8		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Preliminary Information

Ordering Information

Product Number	Package
RC5037M	8 pin SOIC

Preliminary Information

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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RC5039

Programmable DC-DC Converter for P55C, K6, and M2 processors

Features

- Drives N-Channel MOSFET
- Operates From +5V or +12V V_{CC} Bias
- Operates from +5V Power Input
- Simple Single-Loop Control Design
  - Voltage-Mode PWM Control
- Fast Transient Response
  - High-Bandwidth Error Amplifier
  - Full 0% to 100% Duty Ratio
- Excellent Output Voltage Regulation
  - ±1.5% Over Line Voltage and Temperature
- 4 Bit Digital-to-Analog Output Voltage Selection
  - Wide Range - 2.0VDC to 3.5VDC
  - 0.1V Binary Steps
- Power-Good Output Voltage Monitor
- Over-Voltage and Over-Current Fault Monitors
  - Does Not Require Extra Current Sensing Element, uses MOSFET's $R_{DS(ON)}$
- Small Converter Size
  - Constant Frequency Operation
  - 200kHz Free-Running Oscillator Programmable from 50kHz to 1MHz

Applications

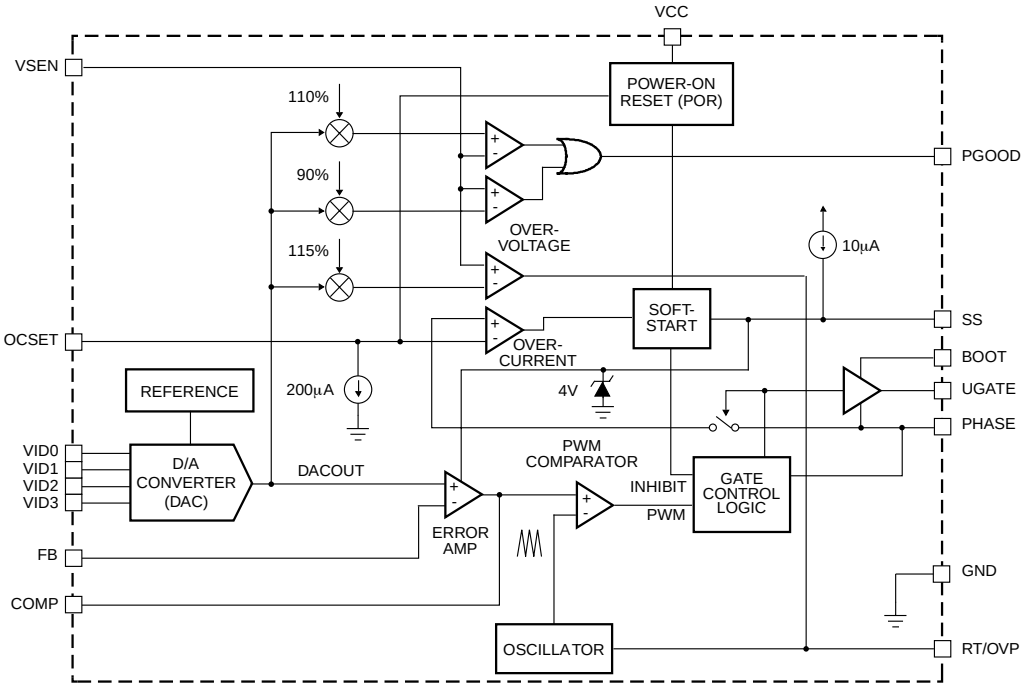
- Power Supply for Pentium®, Pentium® Pro, PowerPC™ and Alpha™ Microprocessors
- High-Power 5V to 3.xV DC-DC Regulators
- Low-Voltage Distributed Power Supplies

Description

The RC5039 provides complete control and protection for a DC-DC converter optimized for high-performance microprocessor applications. It is designed to drive an N-Channel MOSFET in a standard buck topology. The RC5039 integrates all of the control, output adjustment, monitoring and protection functions into a single package.

The RC5039 includes a 4-Input Digital-to-Analog Converter (DAC) that adjusts the output voltage from 2.0VDC to 3.5VDC in 0.1V increments. The precision reference and voltage-mode regulator hold the selected output voltage to within ±1.5% over temperature and line voltage variations.

Block Diagram



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Rev. 0.9.2

PRELIMINARY INFORMATION describes products that are not in full production at the time of printing. Specifications are based on design goals and limited characterization. They may change without notice. Contact Fairchild Semiconductor for current information.

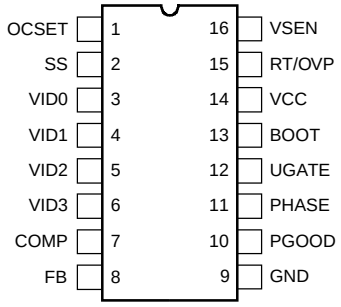
Preliminary Information

The RC5039 provides simple, single feedback loop, voltage-mode control with fast transient response. It includes a 200kHz free-running triangle-wave oscillator that is adjustable from 50kHz to 1MHz. The error amplifier features a 15MHz gain-bandwidth product and 6V/µs slew rate which enables high converter bandwidth for fast transient performance. The resulting PWM duty ratio ranges from 0% to 100%.

The RC5039 monitors the output voltage with a window comparator that tracks the DAC output and issues a Power Good signal when the output is within ±10%. The RC5039 monitors the current by using the $R_{DS(ON)}$ of the upper MOSFET which eliminates the need for a current sensing resistor. The RC5039 protects against over-current conditions by inhibiting PWM operation. Built-in over-voltage protection triggers an exter-nal SCR to crowbar the input supply.

Pin Assignments

RC5039 (SOIC)
TOP VIEW



Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	OCSET	Connect a resistor (R_{OCSET}) from this pin to the drain of the upper MOSFET. R_{OCSET} , an internal 200µA current source (I_{OCS}), and the upper MOSFET on-resistance. ($R_{DS(ON)}$) set the converter over-current (OC) trip point according to the following equation: $I_{PEAK} = \frac{I_{OCS} \bullet R_{OCSET}}{R_{DS(ON)}}$ An over-current trip cycles the soft-start function.
2	SS	Connect a capacitor from this pin to ground. This capacitor, along with an internal 10µA current source, sets the soft-start interval of the converter.
3-6	VID0-3	VID0-3 are the input pins to the 4-bit DAC. The states of these four pins program the internal voltage reference (DACOUT). The level of DACOUT sets the converter output voltage. It also sets the PGOOD and OVP thresholds. Table 1 specifies DACOUT for the 16 combinations of DAC inputs.
7	COMP	COMP and FB are the available external pins of the error amplifier. The FB pin is the inverting input of the error amplifier and the COMP pin is the error amplifier output. These pins are used to compensate the voltage-control feedback loop of the converter.
8	FB	
9	GND	Signal ground for the IC. All voltage levels are measured with respect to this pin.
10	PGOOD	PGOOD is an open collector output used to indicate the status of the converter output voltage. This pin is pulled low when the converter output is not within ±10% of the DACOUT reference voltage.
11	PHASE	Connect the PHASE pin to the upper MOSFET source. This pin is used to monitor the voltage drop across the MOSFET for over-current protection. This pin also provides the return path for the upper gate drive.
12	UGATE	Connect UGATE to the upper MOSFET gate. This pin provides the gate drive for the upper MOSFET.

Preliminary Information

Pin Definitions (continued)

Pin Number	Pin Name	Pin Function Description
13	BOOT	This pin provides bias voltage to the upper MOSFET driver. A bootstrap circuit may be used to create a BOOT voltage suitable to drive a standard N-Channel MOSFET.
14	VCC	Provide a 12V bias supply for the chip to this pin.
15	RT/OVP	This pin is multiplexed, providing two functions. The first function is oscillator switching frequency adjustment. By placing a resistor (R_T) from this pin to GND, the nominal 200KHz switching frequency is increased according to the following equation: $F_S = 200kHz + \frac{5.6E3[KHz \times Kohm]}{R_T[Kohm]}$ (R_T to GND) Conversely, connecting a pull-up resistor (R_T) from this pin to V_{CC} reduces the switching frequency according to the following equation: $F_S = 200kHz - \frac{30.0E3[KHz \times Kohm]}{R_T[Kohm]}$ (R_T to 12V) The second function for this pin is to drive an external SCR in the event of an overvoltage condition.
16	VSEN	This pin is connected to the converters output voltage. The PGOOD and OVP comparator circuits use this signal to report output voltage status and for overvoltage protection.

Absolute Maximum Ratings

Power Input Voltage V_{IN}	6V
Supply Voltage, V_{CC}	+13.5V
Boot Voltage, V_{BOOT} - V_{PHASE}	+13.5V
V_{CC} or I/O Voltage	GND -0.3V to V_{CC} + 0.3V
ESD Classification	Class 2

Recommended Operating Conditions

Supply Voltage, V_{CC}	+12V ±10%
Ambient Temperature Range	0°C to 70°C
Junction Temperature Range	0°C to 100°C

Thermal Information

Thermal Resistance (Typical, Note 1) SOIC Package SOIC Package (with 3 in^2 of Copper)	θ_{JA} (°C/W) 100 90
Maximum Junction Temperature (Plastic Package)	150°C
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) (SOIC - Lead Tips Only)	300°C

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Note:

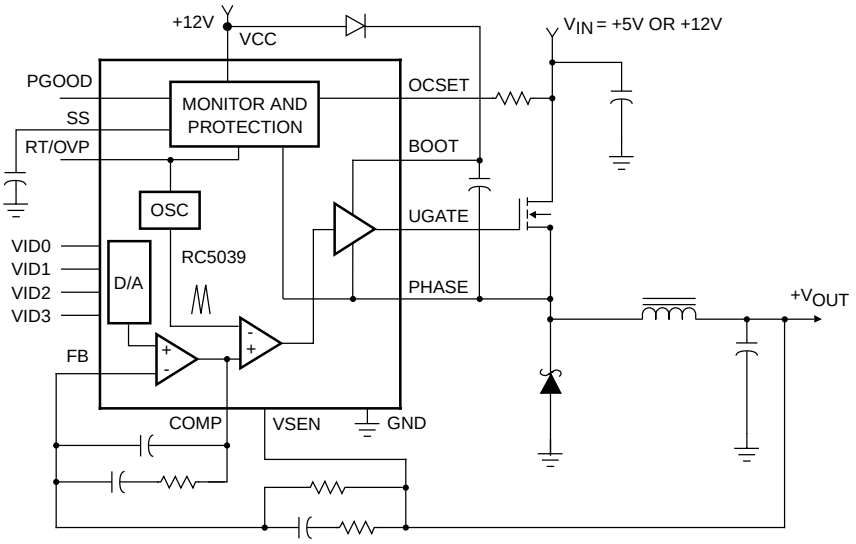
1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Preliminary Information

Electrical Specifications (Recommended Operating Conditions, unless otherwise noted.)

Parameter		Test Conditions	Min.	Typ.	Max.	Units
VCC Supply Current						
I_{CC}	Nominal Supply	UGATE Open	–	22	–	mA
Power-On Reset						
	Rising VCC Threshold	V_{OCSET} = 4.5V	–	–	10.4	V
	Falling VCC Threshold	V_{OCSET} = 4.5V	8.8	–	–	V
	Rising V_{OCSET} Threshold		–	1.26	–	V
Oscillator						
	Free Running Frequency	RT = OPEN	180	200	220	kHz
	Total Variation	6kΩ < RT to GND < 200kΩ	-20	–	+20	%
ΔV_{OSC}	Ramp Amplitude	RT = OPEN	–	1.9	–	V_{P-P}
Reference and DAC						
	DACOUT Voltage Accuracy		-1.5	–	+1.5	%
Error Amplifier						
	DC Gain		–	88	–	dB
GBW	Gain-Bandwidth Product		–	15	–	MHz
SR	Slew Rate	COMP = 10pF	–	6	–	V/μs
Gate Driver						
I_{UGATE}	Upper Gate Source	V_{BOOT} - V_{PHASE} = 12V, V_{UGATE} = 6V	350	500	–	mA
I_{UGATE}	Upper Gate Sink	V_{UGATE} - V_{PHASE} = 1V	–	100	–	mA
Protection						
	Over-Voltage Trip (V_{SEN}/DACOUT)		–	115	120	%
I_{OCSET}	OCSET Current Source	V_{OCSET} = 4.5VDC	170	200	230	μA
I_{OVP}	OVP Sourcing Current	V_{SEN} = 5.5V; V_{OVP} = 0V	60	–	–	mA
I_{SS}	Soft Start Current		–	10	–	μA
Power Good						
	Upper Threshold (V_{SEN} /DACOUT)	V_{SEN} Rising	106	–	111	%
	Lower Threshold (V_{SEN} /DACOUT)	V_{SEN} Falling	89	–	94	%
	Hysteresis (V_{SEN} /DACOUT)	Upper and Lower Threshold	–	2	–	%
V_{PGOOD}	PGOOD Voltage Low	I_{PGOOD} = -5mA	–	0.5	–	V

Typical Application



Functional Description

Initialization

The RC5039 automatically initializes upon receipt of power. Special sequencing of the input supplies is not necessary. The Power-On Reset (POR) function continually monitors the input supply voltages. The POR monitors the bias voltage at the V_{CC} pin and the input voltage (V_{IN}) on the OCSET pin. The level on OCSET is equal to V_{IN} less a fixed voltage drop (see over-current protection). The POR function initiates soft start operation after both input supply voltages exceed their POR thresholds.

Soft Start

The POR function initiates the soft start sequence. An internal 10µA current source charges an external capacitor (C_{SS}) on the SS pin to 4V. Soft start clamps the error amplifier output (COMP pin) and reference input (+ terminal of error amp) to the SS pin voltage. Figure 1 shows the soft start interval with C_{SS} = 0.1µF. Initially the clamp on the error amplifier (COMP pin) controls the converter's output voltage. At t1 in Figure 1, the SS voltage reaches the valley of the oscillator's triangle wave. The oscillator's triangular wave-form is compared to the ramping error amplifier voltage. This generates PHASE pulses of increasing width that charge the output capacitor(s). This interval of increasing pulse width continues to t2. With sufficient output voltage, the clamp on the reference input controls the output voltage. This is the interval between t2 and t3 in Figure 1. At t3 the SS voltage exceeds the DACOUT voltage and the output voltage is in regulation. This method provides a rapid and controlled output voltage rise. The PGOOD signal toggles 'high' when the output voltage (VSEN pin) is within ±5% of DACOUT. The 2% hysteresis built into the power good comparators prevents PGOOD oscillation due to nominal output voltage ripple.

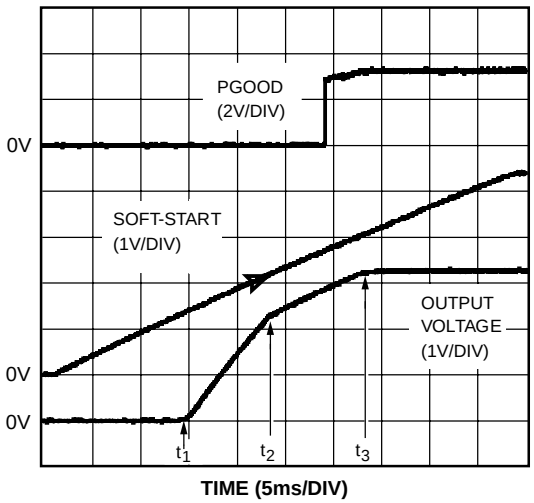


Figure 1. Soft Start Interval

Over-Current Protection

The over-current function protects the converter from a shorted output by using the upper MOSFET's on-resistance, $R_{DS(ON)}$ to monitor the current. This method enhances the converter's efficiency and reduces cost by eliminating a current sensing resistor.

The over-current function cycles the soft-start function in a hiccup mode to provide fault protection. A resistor (R_{OCSET}) programs the over-current trip level. An internal 200µA current sink develops a voltage across R_{OCSET} that is referenced to V_{IN}. When the voltage across the upper MOSFET (also referenced to V_{IN}) exceeds the voltage across R_{OCSET},

Preliminary Information

the over-current function initiates a soft-start sequence. The soft-start function discharges C_{SS} with a 10μA current sink and inhibits PWM operation. The soft-start function recharges C_{SS}, and PWM operation resumes with the error amplifier clamped to the SS voltage. Should an overload occur while recharging C_{SS}, the soft start function inhibits PWM operation while fully charging C_{SS} to 4V to complete its cycle. Figure 2 shows this operation with an overload condition. Note that the inductor current increases to over 15A during the C_{SS} charging interval and causes an over-current trip. The converter dissipates very little power with this method. The measured input power for the conditions of Figure 2 is 2.5W.

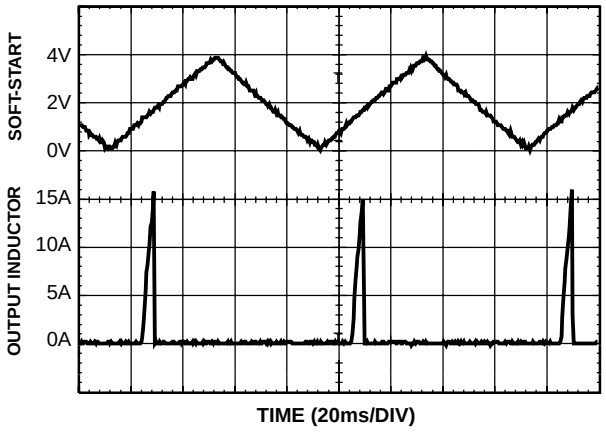


Figure 2. Over-Current Operation

The over-current function will trip at a peak inductor current (I_{PEAK}) determined by:

$$I_{PEAK} = \frac{I_{OCSET} \bullet R_{OCSET}}{r_{DS(ON)}}$$

where I_{OCSET} is the internal OCSET current source (200μA typical). The OC trip point varies mainly due to the MOSFET's $R_{DS(ON)}$ variations. To avoid over-current tripping in the normal operating load range, find the R_{OCSET} resistor from the equation above with:

1. The maximum $R_{DS(ON)}$ at the highest junction temperature.
2. The minimum I_{OCSET} from the specification table.
3. Determine I_{PEAK} for $I_{PEAK} > I_{OUT(MAX)} + (\Delta I)/2$, where ΔI is the output inductor ripple current.

For an equation for the ripple current see the section under component guidelines titled 'Output Inductor Selection'.

A small ceramic capacitor should be placed in parallel with R_{OCSET} to smooth the voltage across R_{OCSET} in the presence of switching noise on the input voltage.

Output Voltage Program

The output voltage of a RC5039 converter is programmed to discrete levels between 2.0VDC and 3.5VDC. The voltage identification (VID) pins program an internal voltage reference (DACOUT) with a 4-bit digital-to-analog converter (DAC). The level of DACOUT also sets the PGOOD and OVP thresholds. Table 1 specifies the DACOUT voltage for the 16 combinations of open or short connections on the VID pins. The output voltage should not be adjusted while the converter is delivering power. Remove input power before changing the output voltage. Adjusting the output voltage during operation could toggle the PGOOD signal and exercise the over-voltage protection.

Table 1. Output Voltage Program

PIN NAME				NOMINAL DACOUT VOLTAGE
VID3	VID2	VID1	VID0	
1	1	1	1	2.0
1	1	1	0	2.1
1	1	0	1	2.2
1	1	0	0	2.3
1	0	1	1	2.4
1	0	1	0	2.5
1	0	0	1	2.6
1	0	0	0	2.7
0	1	1	1	2.8
0	1	1	0	2.9
0	1	0	1	3.0
0	1	0	1	3.1
0	0	1	1	3.2
0	0	1	0	3.3
0	0	0	1	3.4
0	0	0	0	3.5

Note:
1. 0 = Connected to GND or V_{SS}, 1 = OPEN

The DAC function is a precision non-inverting summation amplifier shown in Figure 3. The resistor values shown are only approximations of the actual precision values used. Grounding any combination of the VID pins increases the DACOUT voltage. The 'open' circuit voltage on the VID pins is the band gap reference voltage, 1.26V.

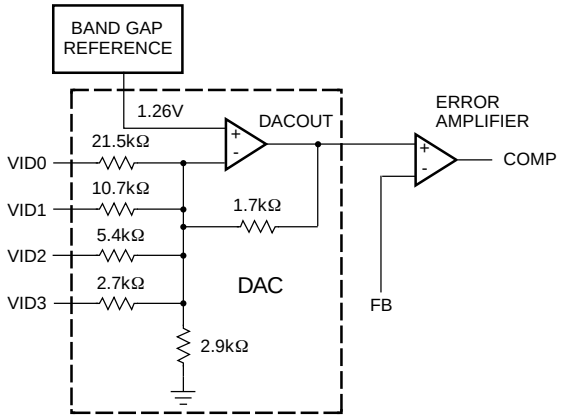


Figure 3. DAC Function Schematic

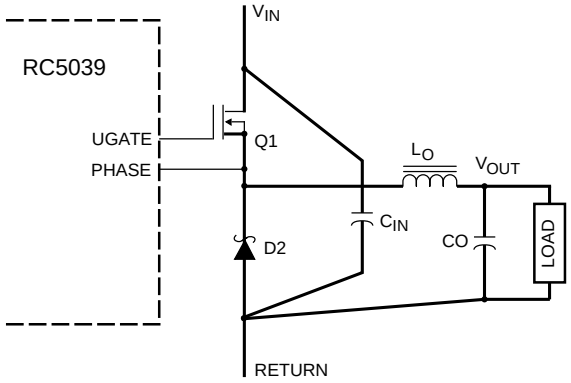


Figure 4. Printed Circuit Board Power and Ground planes or Islands

Application Guidelines

Layout Considerations

As in any high frequency switching converter, layout is very important. Switching current from one power device to another can generate voltage transients across the impedances of the interconnecting bond wires and circuit traces. These interconnecting impedances should be minimized by using wide, short printed circuit traces. The critical components should be located as close together as possible using ground plane construction or single point grounding.

Figure 4 shows the critical power components of the converter. To minimize the voltage overshoot the interconnecting wires indicated by heavy lines should be part of ground or power plane in a printed circuit board. The components shown in Figure 4 should be located as close together as possible. Please note that the capacitors C_{IN} and C_O each represent numerous physical capacitors. Locate the RC5039 within 3 inches of the MOSFET, Q1. The circuit traces for the MOSFET's gate and source connections from the RC5039 must be sized to handle up to 1A peak current.

Figure 5 shows the circuit traces that require additional lay-out consideration. Use single point and ground plane construction for the circuits shown. Minimize any leakage current paths on the SS PIN and locate the capacitor, C_{SS} close to the SS pin because the internal current source is only 10μA. Provide local V_{CC} decoupling between V_{CC} and GND pins. Locate the capacitor, C_{BOOT} as close as practical to the BOOT and PHASE pins.

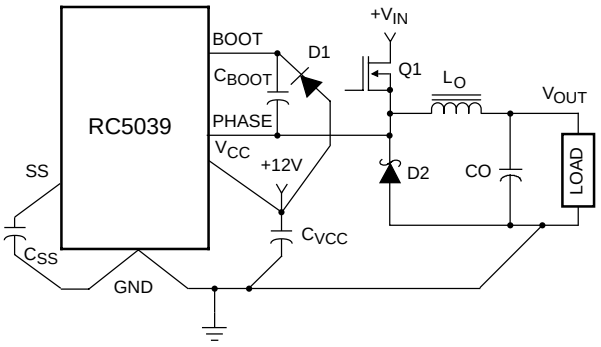


Figure 5. Printed Circuit Board Small Signal Layout Guidelines

Feedback Compensation

Figure 6 highlights the voltage-mode control loop for a buck converter. The output voltage (V_{OUT}) is regulated to the reference voltage level. The error amplifier (Error Amp) output ($V_{E/A}$) is compared with the oscillator (OSC) triangular wave to provide a pulse-width modulated (PWM) wave with an amplitude of V_{IN} at the PHASE node. The PWM wave is smoothed by the output filter (L_O and C_O).

The modulator transfer function is the small-signal transfer function of $V_{OUT}/V_{E/A}$. This function is dominated by a DC Gain and the output filter (L_O and C_O), with a double pole break frequency at F_{LC} and a zero at F_{ESR}. The DC Gain of the modulator is simply the input voltage (V_{IN}) divided by the peak-to-peak oscillator voltage ΔV_{OSC}.

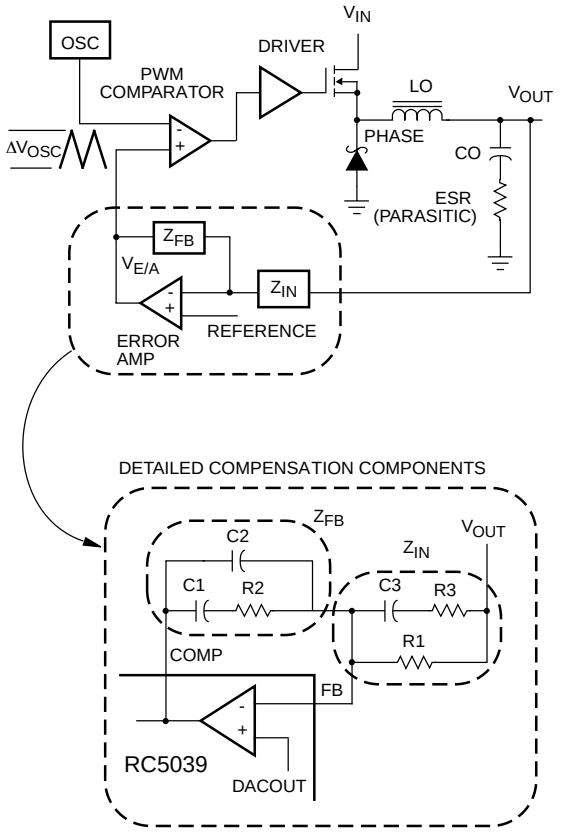


Figure 6. Voltage-Mode Buck Converter Compensation

Modulator Break Frequency Equations

$$F_{LC} = \frac{1}{2\pi \bullet \sqrt{L_O \bullet C_O}} \qquad F_{ESR} = \frac{1}{2\pi \bullet ESR \bullet C_O}$$

The compensation network consists of the error amplifier (internal to the RC5039) and the impedance networks Z_{IN} and Z_{FB}. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency (f_{0dB}) and adequate phase margin. Phase margin is the difference between the closed loop phase at f_{0dB} and 180°. The equations below relate the compensation network's poles, zeros and gain to the components (R1, R2, R3, C1, C2, and C3) in Figure 6. Use these guidelines for locating the poles and zeros of the compensation network:

1. Pick Gain (R2/R1) for desired converter bandwidth
2. Place 1ST Zero Below Filter's Double Pole (~75% F_{LC})
3. Place 2ND Zero at Filter's Double Pole
4. Place 1ST Pole at the ESR Zero
5. Place 2ND Pole at Half the Switching Frequency
6. Check Gain against Error Amplifier's Open-Loop Gain
7. Estimate Phase Margin - Repeat if Necessary

Compensation Break Frequency Equations

$$F_{Z1} = \frac{1}{2\pi \bullet R2 \bullet C1} \qquad F_{P1} = \frac{1}{2\pi \bullet R2 \bullet \left(\frac{C1 \bullet C2}{C1 + C2}\right)}$$

$$F_{Z2} = \frac{1}{2\pi \bullet (R1 + R3) \bullet C3} \qquad F_{P2} = \frac{1}{2\pi \bullet R3 \bullet C3}$$

Figure 7 shows an asymptotic plot of the DC-DC converter's gain vs. frequency. The actual Modulator Gain has a high gain peak due to the high Q factor of the output filter and is not shown in Figure 7. Using the above guidelines should give a Compensation Gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at F_{P2} with the capabilities of the error amplifier. The Closed Loop Gain is constructed on the log-log graph of Figure 7 by adding the Modulator Gain (in dB) to the Compensation Gain (in dB). This is equivalent to multiplying the modulator transfer function to the compensation transfer function and plotting the gain.

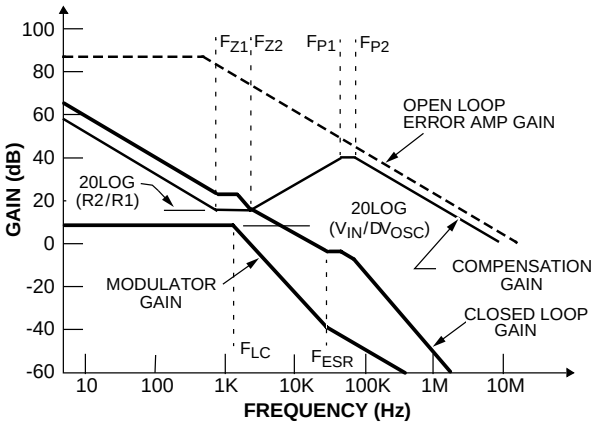


Figure 7. Asymptotic Bode Plot of Converter Gain

The compensation gain uses external impedance networks Z_{FB} and Z_{IN} to provide a stable, high bandwidth (BW) overall loop. A stable control loop has a gain crossing with -20dB/decade slope and a phase margin greater than 45 degrees. Include worst case component variations when determining phase margin.

Component Selection Guidelines

Output Capacitor Selection

An output capacitor is required to filter the output and supply the load transient current. The filtering requirements are a function of the switching frequency and the ripple current. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout.

Modern microprocessors produce transient load rates above 1A/ns. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (Effective Series Resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements. For example, Intel recommends that the high frequency decoupling for the Pentium Pro be composed of at least forty (40) 1µF ceramic capacitors in the 1206 surface-mount package.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the equivalent series inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

Output Inductor Selection

The output inductor is selected to meet the output voltage ripple requirements and minimize the converter's response time to the load transient. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current. The ripple voltage and current are approximated by the following equations:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{FS \times L} \bullet \frac{V_{OUT}}{V_{IN}} \qquad \Delta V_{RIPPLE} = \Delta I \times ESR$$

Increasing the value of inductance reduces the ripple current and voltage. However, the large inductance values reduce the converter's response time to a load transient.

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the RC5039 will provide either 0% or 100% duty cycle in response to a load transient. The response time is the time required to slew the inductor current from an initial current value to the transient current level. During this interval the difference between the inductor current and the transient current level must be supplied by the output capacitor. Minimizing the response time can minimize the output capacitance required.

The response time to a transient is different for the application of load and the removal of load. The following equations give the approximate response time interval for application and removal of a transient load:

$$t_{RISE} = \frac{L_O \times I_{TRAN}}{V_{IN} - V_{OUT}} \qquad t_{FALL} = \frac{L_O \times I_{TRAN}}{V_{OUT}}$$

where: I_{TRAN} is the transient load current step, t_{RISE} is the response time to the application of load, and t_{FALL} is the response time to the removal of load. With a +5V input source, the worst case response time can be either at the application or removal of load and dependent upon the DACOUT setting. Be sure to check both of these equations at the minimum and maximum output levels for the worst case response time.

Input Capacitor Selection

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time Q1 turns on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of Q1 and the anode of Schottky diode D2.

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current rating requirement for the input capacitor of a buck regulator is approximately 1/2 the DC load current.

For a through hole design, several electrolytic capacitors (Panasonic HFQ series or Nichicon PL series or Sanyo MVGX or equivalent) may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up. The TPS series available from AVX, and the 593D series from Sprague are both surge current tested.

MOSFET Selection/Considerations

The RC5039 requires an N-channel power MOSFET. It should be selected based upon $R_{DS(ON)}$, gate supply requirements, and thermal management requirements.

In high-current applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components; conduction loss and switching loss. The conduction losses are the largest component of power dissipation for the MOSFET. Switching losses also contribute to the overall MOSFET power loss (see the equations below). These equations assume linear voltage-current transitions and are approximations. The gate-charge losses are dissipated by the RC5039 and don't heat the MOSFET. However, large gate-charge increases the switching interval, t_{SW}, which increases the upper MOSFET switching losses. Ensure that the MOSFET is within its maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heat-sink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

$$P_{COND} = I_O^2 \times R_{DS(ON)} \times D$$

$$P_{SW} = \frac{1}{2} I_O \times V_{IN} \times t_{SW} \times Fs$$

Where: D is the duty cycle = V_{OUT}/V_{IN},
t_{SW} is the switching interval, and
Fs is the switching frequency

Standard-gate MOSFETs are normally recommended for use with the RC5039. However, logic-level gate MOSFETs can be used under special circumstances. The input voltage, upper gate drive level, and the MOSFET's absolute gate-to-source voltage rating determine whether logic-level MOSFETs are appropriate.

Figure 8 shows the upper gate drive (BOOT pin) supplied by a bootstrap circuit from V_{CC}. The boot capacitor, C_{BOOT}, develops a floating supply voltage referenced to the PHASE pin. This supply is refreshed each cycle to a voltage of V_{CC} less the boot diode drop (V_D) when the Schottky diode, D2, conducts. Logic-level MOSFETs can only be used if the MOSFET's absolute gate-to-source voltage rating exceeds the maximum voltage applied to V_{CC}.

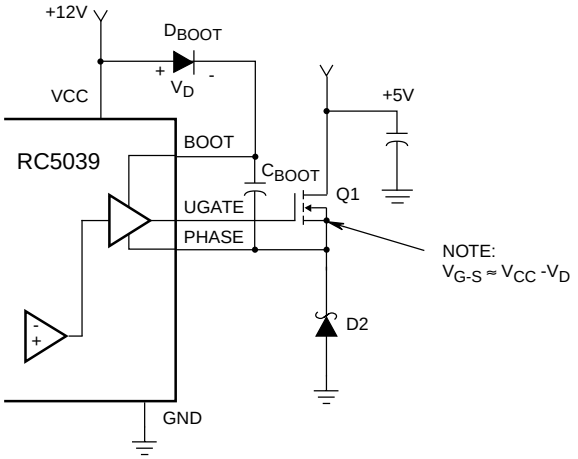


Figure 8. Upper Gate Drive - Bootstrap Option

Figure 9 shows the upper gate drive supplied by a direct connection to VCC . This option should only be used in converter systems where the main input voltage is + 5VDC or less. The peak upper gate-to-source voltage is approximately VCC less the input supply. For +5V main power and + 12VDC for the bias, the gate-to-source voltage of Q1 is 7V. A logic-level MOSFET is a good choice for Q1 under these conditions.

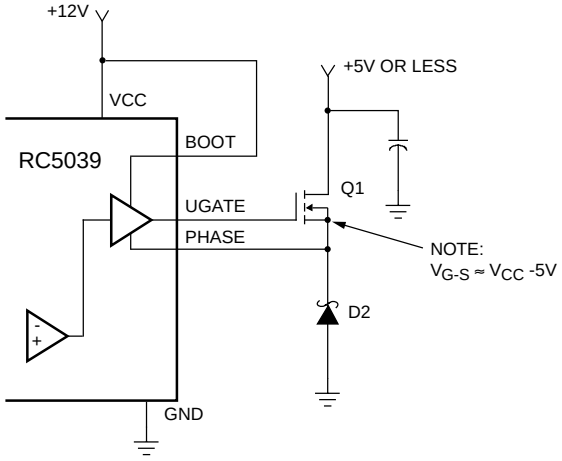


Figure 9. Upper Gate Drive - Direct V_{CC} Drive Option

Schottky Selection

Rectifier D2 conducts when the upper MOSFET Q1 is off. The diode should be a Schottky type for low power losses. The power dissipation in the Schottky rectifier is approximated by:

$$P_D = I_O \times V_f \times (1 - D)$$

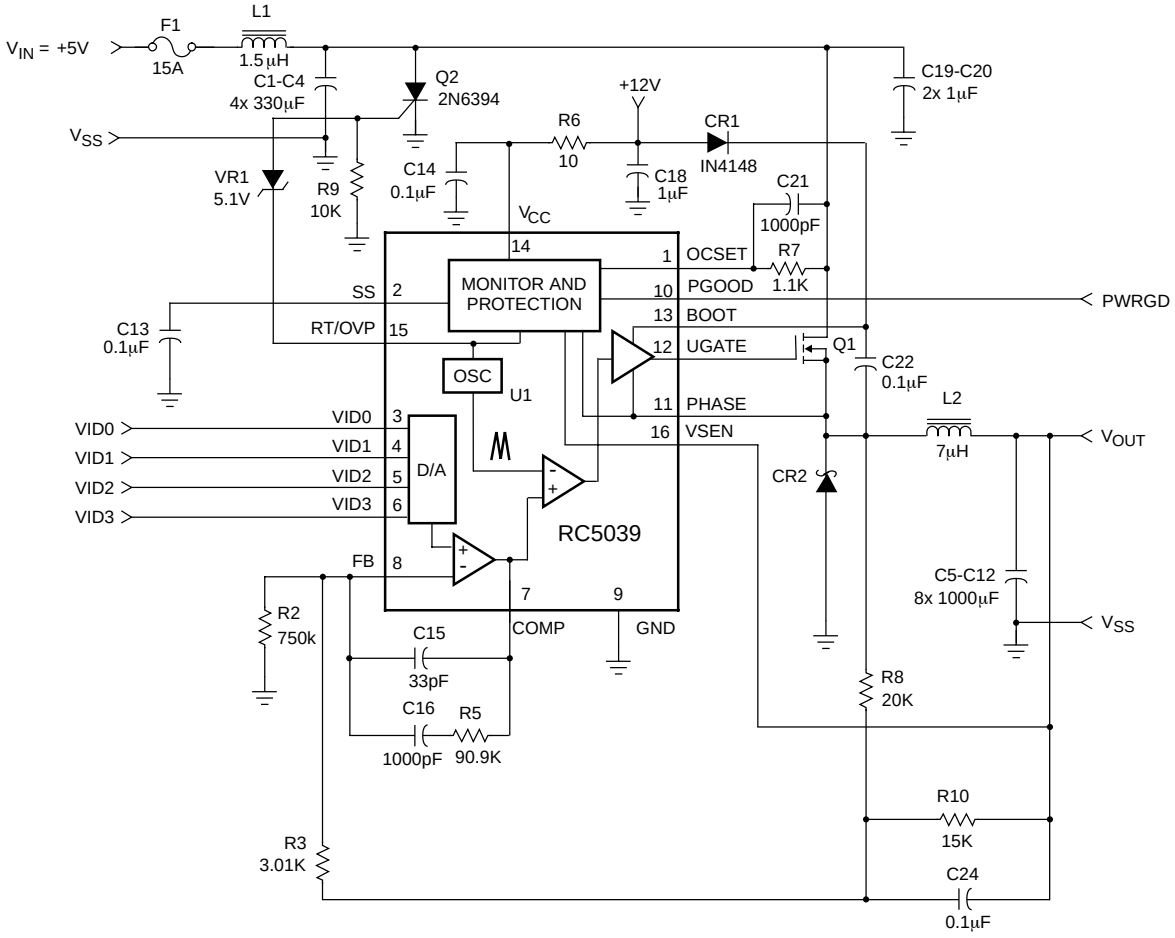
Where: D is the duty cycle = V_O/V_{IN}, and
V_f is the Schottky forward voltage drop

In addition to power dissipation, package selection and heatsink requirements are the main design tradeoffs in choosing the Schottky rectifier. Since the three factors are interrelated,

the selection process is an iterative procedure. The maximum junction temperature of the rectifier must remain below the manufacturer's specified value, typically 125°C. By using the package thermal resistance specification and the Schottky power dissipation equation (shown above), the junction temperature of the rectifier can be estimated. Be sure to use the available airflow and ambient temperature to determine the junction temperature rise.

RC5039 DC-DC Converter Application Circuit

The figure below shows an application circuit of a DC-DC Converter for an Intel Pentium Pro microprocessor.



Component Selection Notes:
C5-C12 - 8 each 1000µF 6.3W VDC, Sanyo MV-GX or Equivalent
C1-C4 - 4 each 330µF 25W VDC, Sanyo MV-GX or Equivalent
L1 - Core: Micrometals T60-52; Each Winding: 14 Turns of 17AWG
L2 - Core: Micrometals T44-52; Winding: 7 Turns of 18AWG
CR1 - 1N4148 or Equivalent
CR2 - 25A, 35V Schottky, Motorola MBR2535CTL or Equivalent
Q1 - Fairchild NDP6030L, heatsink with thermal resistance θ_{SA}<20°C/W should be used

Figure 10. Pentium Pro DC-DC Converter

Preliminary Information

Notes:

Notes:

Notes:

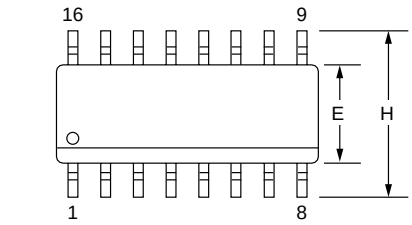
Mechanical Dimensions

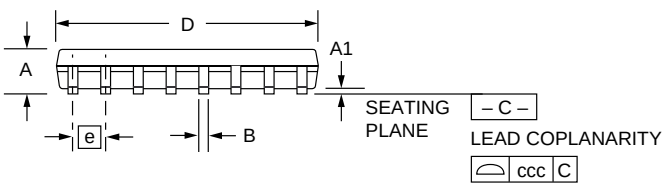
16 Lead SOIC

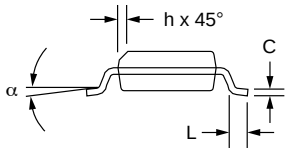
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.19	0.25	5
D	.386	.394	9.80	10.00	2
E	.150	.158	3.81	4.00	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.80	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	16		16		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Preliminary Information

Ordering Information

Part Number	Temperature Range (°C)	Package	Pkg. No.
RC5039CB	0 to 70	16 Lead SOIC	M16.15

Preliminary Information

RC5040

Programmable Synchronous DC-DC Converter

Features

- Programmable output from 2.1V to 3.5V using integrated 4-bit DAC
- 87% efficiency
- Oscillator frequency adjustable from 200KHz to 1MHz
- On-chip Power Good and Output Enable functions
- Excellent transient response
- Over-Voltage Protection
- Short Circuit Protection
- Precision trimmed low TC voltage reference
- 20 pin SOIC package
- Meets Intel Pentium® Pro VRM specifications using minimum number of external components

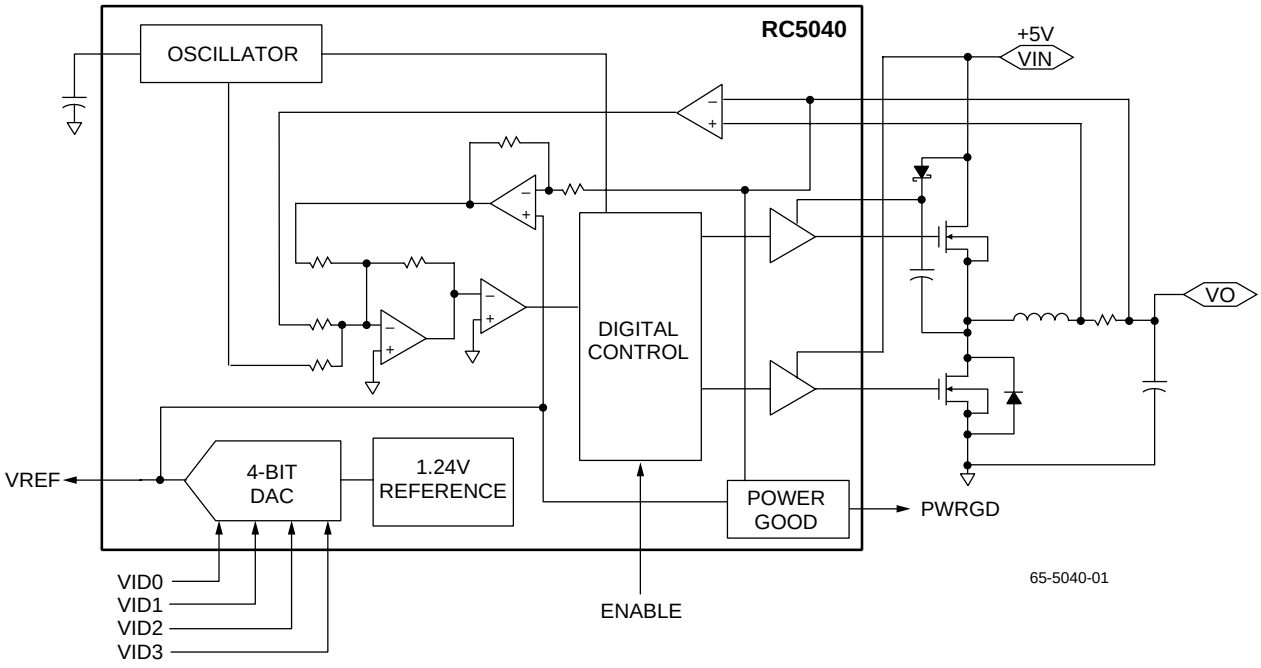
Applications

- Programmable power supply for Pentium® Pro and Pentium® based CPU motherboards
- VRM module for Pentium® Pro CPU
- Programmable power supply for high current microprocessors

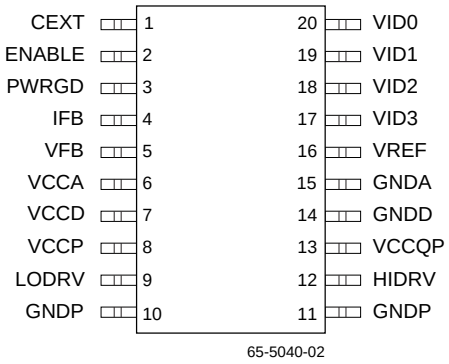
Description

The RC5040 is a synchronous mode DC-DC controller IC which provides an accurate, programmable output for Pentium® Pro CPU applications. Using an integrated 4-bit DAC to accept a voltage identification (VID) code directly from the CPU, the RC5040 can generate precise output voltages between 2.1V and 3.5V in 100mV increments. Output load currents in excess of 12A can be delivered using minimal external circuitry. The RC5040 is designed to operate in a standard PWM control mode under heavy load conditions and in PFM control mode while supplying light loads for optimal efficiency. An on-board precision low TC voltage reference eliminates the requirement for external components in order to achieve tight voltage regulation. The Pentium Pro® CPU is continuously protected by an integrated Power Good function, which sends an active-low interrupt signal to the CPU in the event that the output voltage is out of tolerance. The internal oscillator can be programmed to operate over a range of 200KHz to 1MHz to allow flexibility in choosing external components.

Block Diagram



Pin Assignments



Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	CEXT	**Oscillator capacitor connection.** Connecting an external capacitor to this pin sets the internal oscillator frequency from 200 KHz to 1 MHz. Layout of this pin is critical to system performance. See Application Information for details.
2	ENABLE	**Output Enable.** Open collector/TTL input. Logic LOW will disable output. A 10KΩ internal pull-up resistor assures correct operation if pin is left unconnected.
3	PWRGD	**Power Good output flag.** Open collector output will be at logic HIGH under normal operation. Logic LOW indicates output voltage is not within ±10% of nominal.
4	IFB	**High side current feedback.** Pins short 4 and 5 are used as the inputs for the current feedback control loop and as the short circuit current sense points. Layout of these traces is critical to system performance. See Application Information for details.
5	VFB	**Voltage feedback.** Pin 5 is used as the input for the voltage feedback control loop and as the low side current feedback input. Layout of this trace is critical to system performance. See Application Information for details.
6	VCCA	**Analog V_{CC}.** Connect to system 5V supply and decouple to ground with 0.1μF ceramic capacitor.
7	VCCD	**Digital V_{CC}.** Connect to system 5V supply and decouple to ground with 4.7μF tantalum capacitor.
8	VCCP	**Power V_{CC} for low side FET driver.** Connect to system 5V supply.
9	LODRV	**Low side FET driver output.** Connect this pin to the gate of the N-channel MOSFET M3 in Figure 2. The trace from this pin to the MOSFET gate should be as short as possible (less than 0.5"). See Application Information for details.
10, 11	GNDP	**Power ground.** Return pin for high currents flowing in pins 12 and 13 (HIDRV and VCCQP). Connect to low impedance ground. See Application Information for details.
12	HIDRV	**High side FET driver output.** Connect this pin to the gate of the N-channel MOSFETs M1 and M2 in Figures 1 and 2. The trace from this pin to the MOSFET gates should be kept as short as possible (less than 0.5"). See Application Information for details.
13	VCCQP	**Power V_{CC} for high side FET driver.** VCCQP must be connected to a voltage of at least VCCA + $V_{GS,ON}$ (M1). See Application Information for details.
14	GNDD	**Digital ground.** Return path for digital logic. This pin should be connected to system ground so that ground loops are avoided. See Application Information for details.

Pin Definitions (continued)

Pin Number	Pin Name	Pin Function Description
15	GNDA	**Analog ground.** Return path for low power analog circuitry. Connect to system ground so that ground loops are avoided. See Application Information for details.
16	VREF	**Reference voltage test point.** This pin provides access to the DAC output and should be decoupled to ground using a 0.1μF capacitor. No load should be connected to this pin.
17–20	VID3 – VID0	**Voltage identification (VID) code inputs**. These open collector/TTL compatible inputs will program the output voltage over the ranges specified in Table 1. Internal 10KΩ pull-up resistors assure correct operation if pins are left unconnected.

Absolute Maximum Ratings[1]

Supply Voltages, VCCA, VCCD, VCCP	13V
Supply Voltage for high side FET, VCCQP	13V
Voltage Identification Code Inputs, VID3-VID0	13V
Junction Temperature, T_J	150˚C
Storage Temperature, T_S	-65 to 150˚C
Lead Soldering Temperature, 10 seconds	300˚C

Notes:

1. Functional operation under any of these conditions is not implied. Permanent damage may occur if the device is subjected to conditions outside these ratings.

Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Voltages, VCCA, VCCD, VCCP[1]		4.5	5	7	V
High side FET supply, VCCQP		9	10	12	V
VID Code Input Voltage, Logic HIGH		2			V
VID Code Input Voltage, Logic LOW				0.8	V
PWRGD HIGH Threshold				+7	%VREF
PWRGD LOW Threshold		-7			%VREF
Operating Ambient Temperature, T_A		0		70	˚C

Notes:

1. In non-synchronous operation, VCCP must be connected to GND.

Electrical Specifications

(V_{CCA}, V_{CCD} = 5V, fosc = 650 KHz, and T_A = +25˚C using circuit in Figure 1, unless otherwise noted)
The • denotes specifications which apply over the full operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
Output Voltage	T_A = 0–70°C, See Table 1.	•	2.0		3.5	V
Output Current[1]				12.5	14.5	A
Setpoint Accuracy[2]	I_{LOAD} = 5.25A			1.0	1.5	%
Output Temperature Drift	T_A = 0–70°C	•		+40		ppm/
Load Regulation	I_{LOAD} = 0.5 to 12.5A	•		-1.0		%Vo
Line Regulation	V_{IN} = 4.75–5.25V, I_{LOAD} = 12.5A	•		+0.14		%Vo
Output Ripple/Noise, pk-pk	V_{OUT} = 2.1–3.5V, 20MHz BW	•		30		mV
Cumulative Accuracy[3]	T_A = 0–70°C	•		±3.3	±5.0	%
Efficiency	I_{LOAD} = 12.5A, V_{OUT} = 3.3V	•	80	85		%

Electrical Specifications (continued)

(V_{CCA}, V_{CCD} = 5V, fosc = 650 KHz, and T_A = +25˚C using circuit in Figure 1, unless otherwise noted)
The • denotes specifications which apply over the full operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
Short Circuit Detect Threshold	Internal comparator offset	•	100	120	140	mV
Output Current Driver			0.5	1.0		A
Power Dissipation	No load			0.1	0.2	W
Thermal Impedance, θ_{JA}				80		°C/W
Response Time, Sleep to Full Load				10		µs
Oscillator Frequency Range[4]			0.2		1	MHz
Oscillator Frequency Accuracy	excludes tolerance of C_{EXT}			10		%
Maximum Duty Cycle in PWM Mode			90	95		%
Minimum Pulse Width in PFM Mode					100	ns
Response Time to Short Circuit				15	30	ns
Soft Start Duration at Power-Up				10		µs
Load Transient, 0.5 to 12.5A step	Slew rate = 30A/µs			100		mV

Notes:

1. The maximum output current is limited only by the external components used and their thermal limitations. For loads greater than 12.5A, adequate thermal management is required to achieve optimal performance and reliability.
2. Setpoint Accuracy includes Output Ripple/Noise.
3. Cumulative Accuracy is determined by Setpoint Accuracy, Line and Load Regulation, Output Ripple/Noise, Transient Performance and Temperature Drift.
4. See Typical Operating Characteristics.

Table 1. Voltage Identification Codes[1]

Pentium Pro™ Processor Pins				VID Setpoint	Setpoint Accuracy[2] (mV)	Cumulative Accuracy[3] (mV)
VID3	VID2	VID1	VID0			
1	1	1	1	2.0	—	—
1	1	1	0	2.1	±31	±105
1	1	0	1	2.2	±33	±110
1	1	0	0	2.3	±34	±115
1	0	1	1	2.4	±36	±120
1	0	1	0	2.5	±37	±125
1	0	0	1	2.6	±39	±130
1	0	0	0	2.7	±40	±135
0	1	1	1	2.8	±42	±140
0	1	1	0	2.9	±43	±145
0	1	0	1	3.0	±45	±150
0	1	0	0	3.1	±46	±155
0	0	1	1	3.2	±48	±160
0	0	1	0	3.3	±49	±165
0	0	0	1	3.4	±51	±170
0	0	0	0	3.5	±60	±175

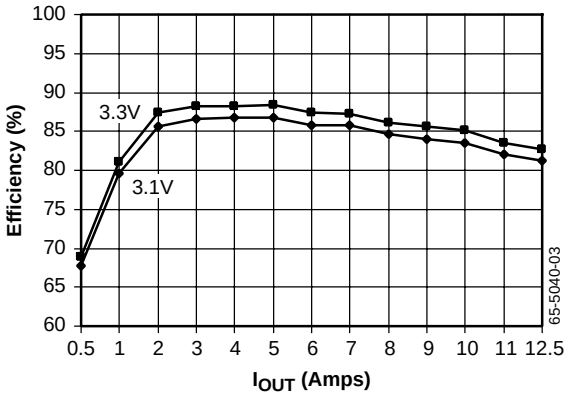
Notes:

1. 0 = processor pin connected to VSS. 1 = Open.
2. Setpoint Accuracy includes Output Ripple/Noise.
3. Cumulative Accuracy includes Setpoint Accuracy, Line & Load Regulation, Transient Effects and Temperature Drift.

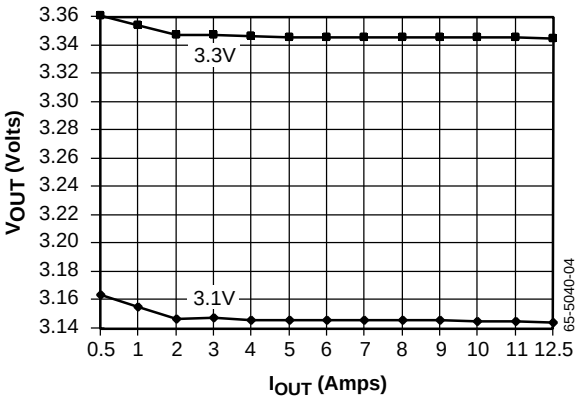
Typical Operating Characteristics

(VCCA, VCCD = 5V, fosc = 650 KHz, and T_A = +25˚C using circuit in Figure 1, unless otherwise noted)

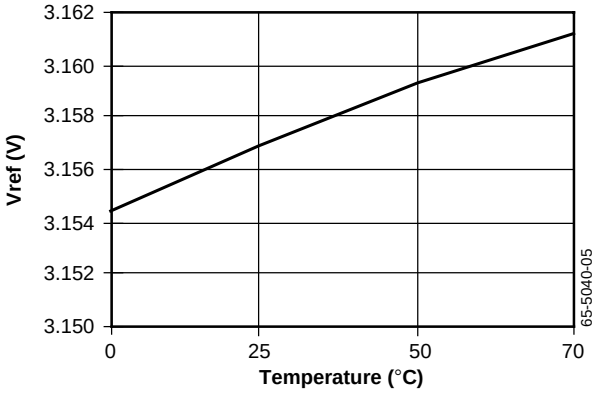
Efficiency vs. Output Current, 650 KHz



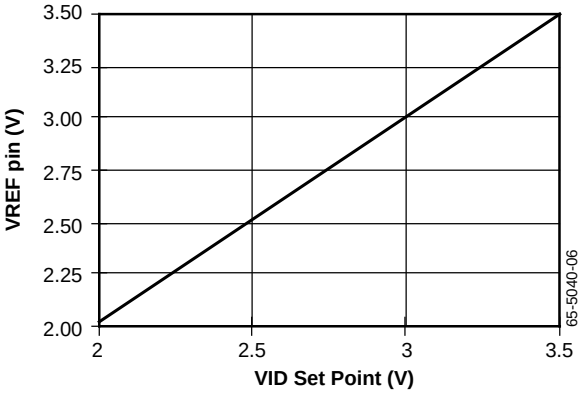
Load Regulation, 650 KHz



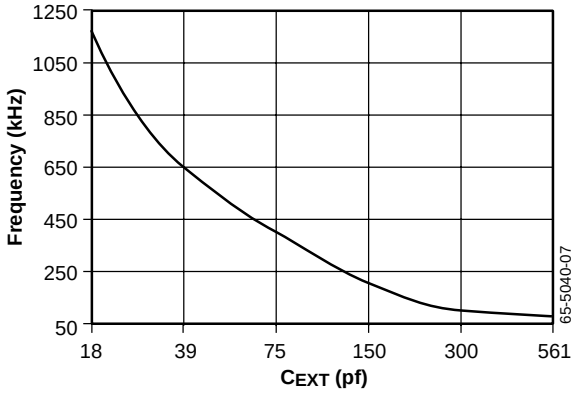
Reference Tempco



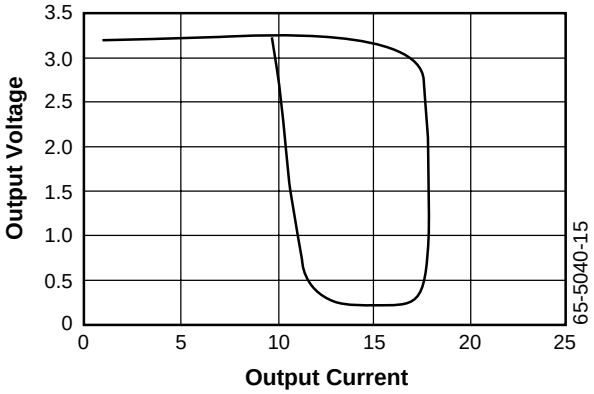
VREF Programming



Oscillator Frequency vs. C_{EXT}

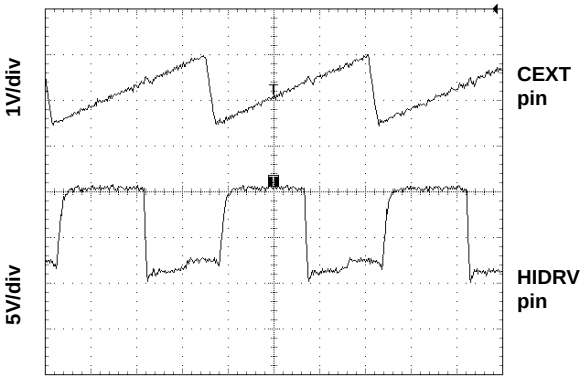


Output Voltage vs. Output Current, R_{SENSE} = 6mΩ



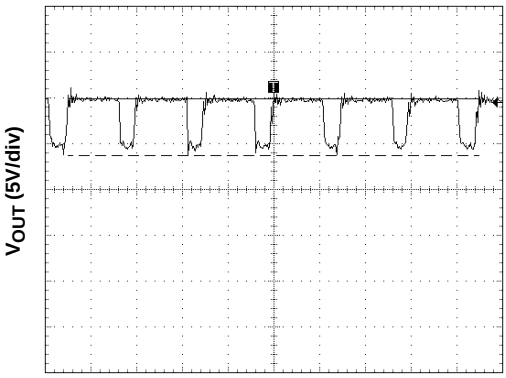
Typical Operating Characteristics (continued)

Switching Waveforms, 12.5A Load



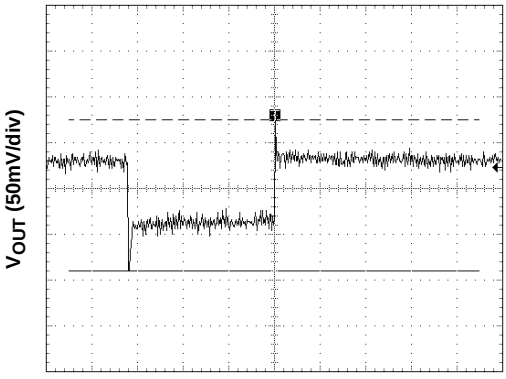
Time (500ns/division)

FET Driver Supply, VCCQP (I_{LOAD} = 12.5A using charge pump)



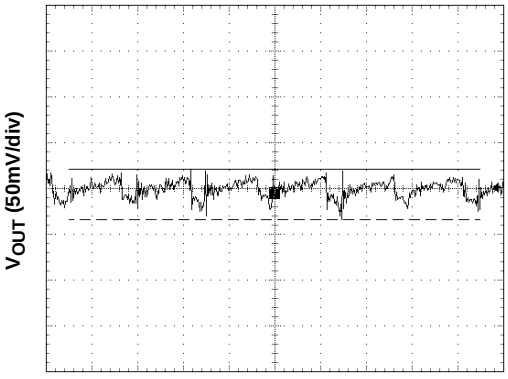
Time (1μs/division)

Transient Response, 0.5A to 12.5A Step



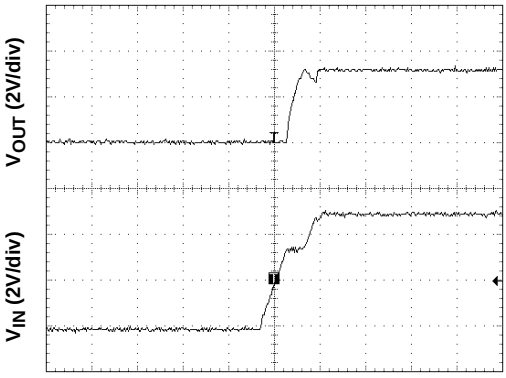
Time (200μs/division)

AC Ripple Response, 12.5A Load



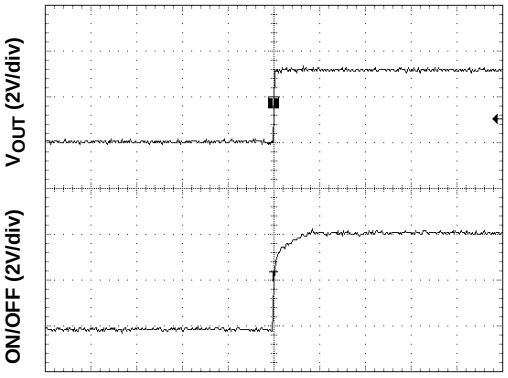
Time (1μs/division)

Output Startup, System Power-Up



Time (50ms/division)

Output Startup from Re-Enable



Time (20ms/division)

65-5040-08

Test Circuits

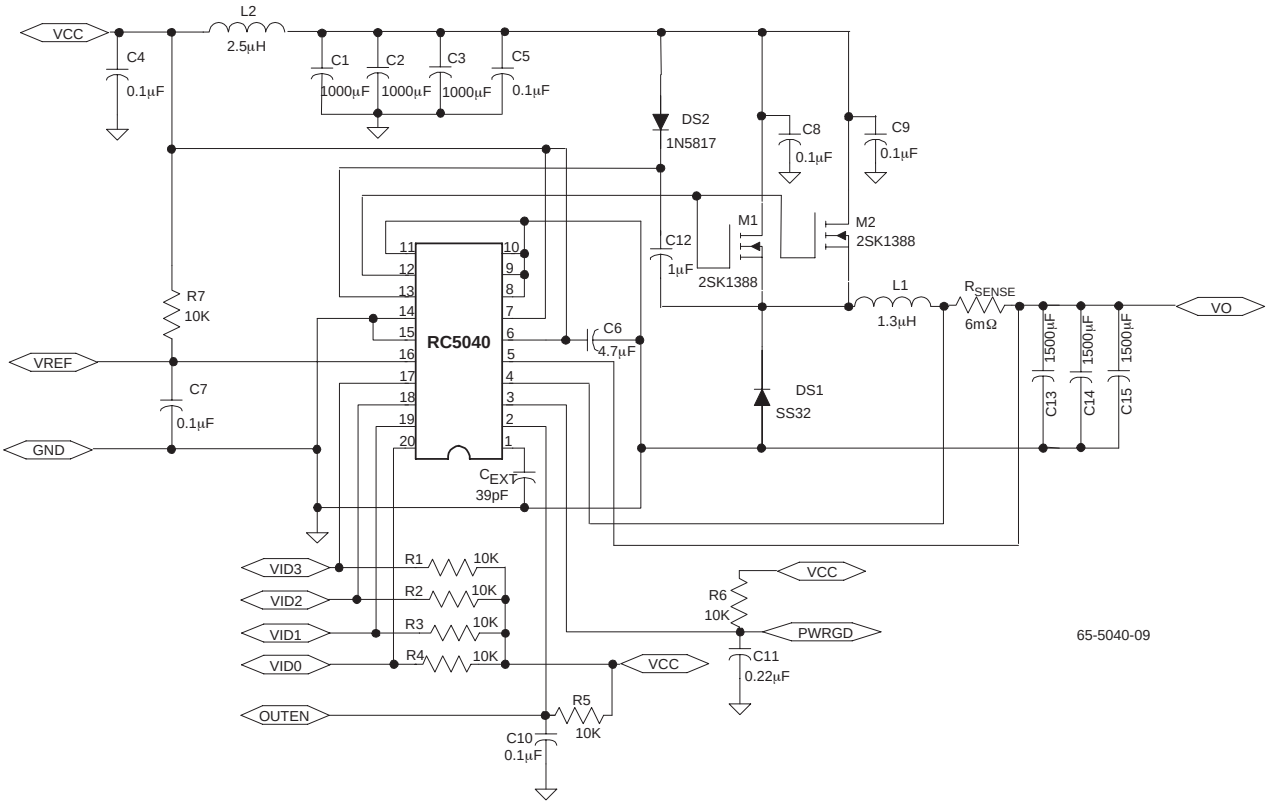


Figure 1. Non-Synchronous DC-DC Converter Application Schematic

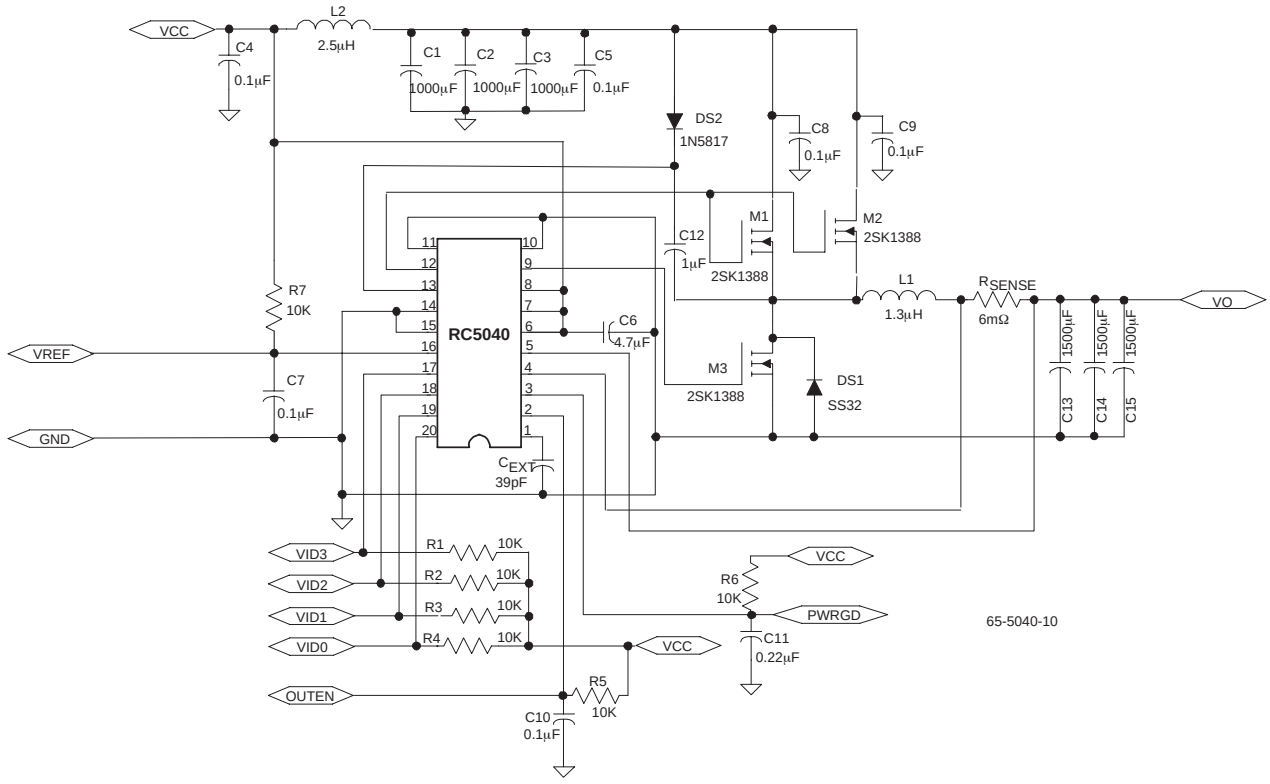


Figure 2. Synchronous DC-DC Converter Application Schematic

Table 2. RC5040 Bill of Materials

Reference	Part Number	Description	Relevant Spec.
C4, C5, C7–C10	Panasonic ECU-V1H104ZFX	0.1μF 50V capacitor	
C6	Panasonic ECSH1CY475R	4.7μF 16V capacitor	
C_{EXT}	Panasonic ECU-V1H121JCG	39pF capacitor	
C12	Panasonic ECSH1CY105R	1μF 16V capacitor	
C1, C2, C3	Sanyo 6MV1000GX	1000μF 6.3V electrolytic capacitor	
C11	Panasonic ECU-V1H224ZFX	0.22μF 50V capacitor	
C13–C15	Sanyo 6MV1500GX	1500μF 6.3 electrolytic capacitor	ESR < 0.047 Ω
DS1	General Instrument SS32	Schottky Diode	3A, 20V
DS2	General Instrument IN5817	7	8
8	Skynet 320-8107	1.3μH inductor	
L2[1]	Skynet 320-6110	2.5μH inductor	
M1, M2[2]	Fuji 2SK1388	N-Channel Logic Level Enhancement Mode MOSFET	$R_{DS(ON)}$ < 37mΩ V_{GS} < 4V, I_D > 20A
R_{SENSE}	Copel A.W.G #18	6 mΩ CuNi Alloy Wire Resistor	
R1–R4, R6, R7	Panasonic ERJ-6ENF10.0KV	10K 5% Resistors	

Notes:

1. The inductor L2 is recommended to isolate the 5V input supply from current surges caused by MOSFET switching. L2 is not required for normal operation and may be omitted if desired.
2. A total of 3 MOSFETs are recommended only for the synchronous DC-DC converter application. For the non-synchronous application, the low side MOSFET M3 is not used.

Application Information

Simple Step-Down Converter

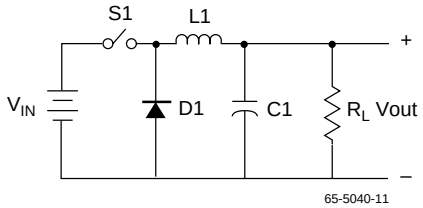


Figure 3. Simple Buck DC-DC Converter

Figure 3 illustrates a step-down DC-DC converter with no feedback control. The derivation of the basic step-down converter will serve as a basis for the design equations for the RC5040. Referring to Figure 3, the basic operation begins by closing the switch S1. When S1 is closed, the input voltage V_{IN} is impressed across inductor L1. The current flowing in this inductor is given by the following equation:

$$I_L = \frac{(V_{IN} - V_{OUT})T_{ON}}{L1}$$

where T_{ON} is the duty cycle (the time when S1 is closed).

When S1 opens, the diode D1 will conduct the inductor current and the output current will be delivered to the load according to the equation:

$$I_L = \frac{V_{OUT}(T_S - T_{ON})}{L1}$$

where: T_S is the overall switching period.
$(T_S - T_{ON})$ is the time during which S1 is open.

By solving these two equations, we can arrive at the basic relationship for the output voltage of a step-down converter:

$$V_{OUT} = V_{IN}\left(\frac{T_{ON}}{T_S}\right)$$

In order to obtain a more accurate approximation for V_{OUT}, we must also include the forward voltage V_D across diode D1 and the switching loss, Vsw. After taking into account these factors, the new relationship becomes:

$$V_{OUT} = (V_{IN} + V_D - V_{SW})\frac{T_{ON}}{T_S} - V_D$$

Overview

The RC5040 is a programmable synchronous DC-DC controller IC. When designed around the appropriate external components, the RC5040 can be configured to deliver more than 14.5A of output current. During heavy loading conditions, the RC5040 functions as a current-mode PWM step-down regulator. Under light loads, the regulator functions in the PFM (pulse frequency modulation), or pulse skipping mode. The controller will sense the load level and switch between the two operating modes automatically, thus optimizing its efficiency under all loading conditions.

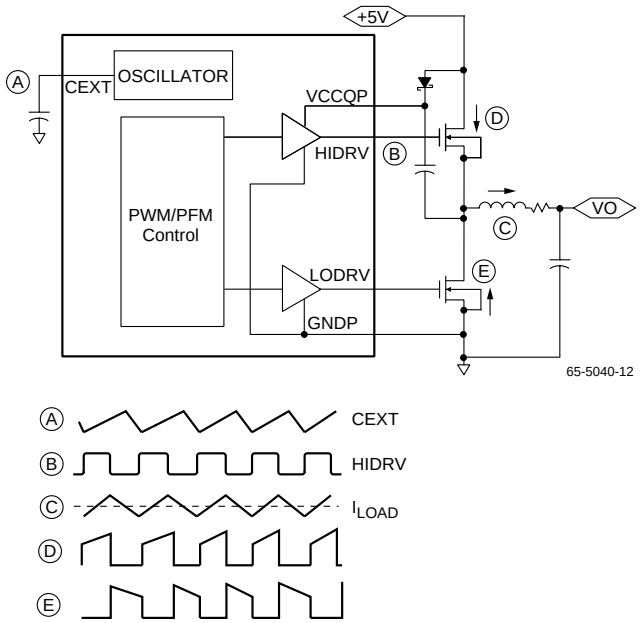


Figure 4. Typical Switching Waveforms

Main Control Loop

Refer to the Block Diagram on page 1. The control loop of the regulator contains two main sections; the analog control block and the digital control block. The analog block consists of signal conditioning amplifiers feeding into a set of comparators which provide the inputs to the digital block. The signal conditioning section accepts inputs from the IFB (current feedback) and VFB (voltage feedback) pins and sets up two controlling signal paths.
The voltage control path amplifies the VFB signal and presents the output to one of the summing amplifier inputs. The current control path takes the difference between the IFB and VFB pins and presents the resulting signal to another input of the summing amplifier. These two signals are then summed together with the slope compensation input from the oscillator. This output is then presented to a comparator, which provides the main PWM control signal to the digital control block.

The additional comparators in the analog control section set the thresholds of where the RC5040 enters its pulse skipping mode during light loads as well as the point at which the maximum current comparator disables the output drive signals to the external power MOSFETs.

The digital control block is designed to take the comparator inputs along with the main clock signal from the oscillator and provide the appropriate pulses to the HIDRV output pin that controls the external power MOSFET. The digital section was designed utilizing high speed Schottky transistor logic, thus allowing the RC5040 to operate at clock speeds as high as 1MHz.

High Current Output Drivers

The RC5040 contains two identical high current output drivers which utilize high speed bipolar transistors arranged in a push-pull configuration. Each driver is capable of delivering 1A of current in less than 100ns. Each driver's power and ground are separated from the overall chip power and ground for additional switching noise immunity. The HIDRV driver has a power supply, VCCQP, which is boot-strapped from a flying capacitor as illustrated in Figure 2. Using this configuration, C12 is alternately charged from VCC via the Schottky diode DS2 and then boosted up when the FET is turned on. This scheme provides a VCCQP voltage equal to 2•VCC – VDS(DS2), or approximately 9.5V with VCC = 5V. This voltage is sufficient to provide the 9V gate drive to the external MOSFET required in order to achieve a low $R_{DS(ON)}$. Since the low side synchronous FET is referenced to ground (refer to Figure 4), there is no need to boost the gate drive voltage and its VCCP power pin can be tied to VCC. See Typical Operating Characteristics for typical full load VCCQP waveform.

Internal Voltage Reference

The reference included in the RC5040 is a 1.24V precision band-gap voltage reference. The internal resistors are precisely trimmed to provide a near zero temperature coefficient (TC). Added to the reference input is the resulting output from an integrated 4-bit DAC. The DAC is provided in accordance with the Pentium Pro specification guideline, which requires the DC-DC converter output to be directly programmable via a 4-bit voltage identification (VID) code. This code will scale the reference voltage from 2.0V (no CPU) to 3.5V in 100mV increments. For guaranteed stable operation under all loading conditions, a 10KΩ pull-up resistor and 0.1µF of decoupling capacitance should be connected to the VREF pin.

Power Good

The RC5040 Power Good function is designed in accordance with the Pentium Pro DC-DC converter specification and provides a constant voltage monitor on the VFB pin. The circuit compares the VFB signal to the VREF voltage and outputs an active-low interrupt signal to the CPU should the power supply voltage exceed ±7% of its nominal setpoint. The Power Good flag provides no other control function to the RC5040.

Output Enable (OUTEN)

The DC-DC converter accepts an open collector signal for controlling the output voltage. A logic low on the ENABLE pin disables the output voltage. When disabled, the PWRGD output is in the low state. This feature is available for the RC5040 only.

Upgrade Present (UP#)

Intel's specifications state that the DC-DC converter must accept an open collector signal, used to indicate the presence of an upgrade processor. The typical state is high (standard CPU). When in the low or ground state (OverDrive processor present), the output voltage must be disabled unless the converter can supply the OverDrive processor's specifications. When disabled, the PWRGD output must be in the low state. Since the RC5040 can supply the OverDrive processor specifications, the UP# signal is not required.

Over-Voltage Protection

The RC5040 provides a constant monitor of the output voltage for protection against overvoltage conditions. If the voltage at the VFB pin exceeds 20% of the selected program voltage, an overvoltage condition will be assumed, and the RC5040 will disable the output drive signal to the MOSFET(s).

Short Circuit Protection

A current sense methodology is implemented to disable the output drive signal to the MOSFET(s) when an over-current condition is detected. The voltage drop created by the output current flowing across a sense resistor is presented to an internal comparator. When voltage developed across the sense resistor exceeds the comparator threshold voltage, the RC5040 will disable the output drive signal to the MOSFET(s).

The DC-DC converter returns to normal operation after the fault has been removed, for either an overvoltage or a short circuit condition.

Oscillator

The RC5040 oscillator section is implemented using a fixed current capacitor charging configuration. An external capacitor (CEXT) is used to preset the oscillator frequency between 200KHz and 1MHz. This scheme allows maximum flexibility in setting the switching frequency as well as choosing external components.

In general, a lower operating frequency will increase the peak ripple current flowing in the output inductor, and thus require the use of a larger inductor value. Operation at lower frequencies also increases the amount of energy storage that must be provided by the bulk output capacitors during load transients due to the slower loop response of the controller.

As the operating frequency is increased, the user should note that the efficiency losses due to switching are relatively fixed per switching cycle. Therefore, as the switching frequency is increased, so is the contribution toward efficiency due to switching losses.

Careful analysis of the RC5040 DC-DC controller has resulted in an optimal operating frequency of 650KHz, which allows the use of smaller inductive and capacitive components while maximizing peak efficiency under all operating conditions.

Design Considerations and Component Selection

MOSFET Selection

This application requires N-channel *Logic Level* Enhancement Mode Field Effect Transistors. Desired characteristics are as follows:

- Low Static Drain-Source On-Resistance, $R_{DS(on)} < 37$ mΩ (lower is better)
- Low gate drive voltage, $V_{GS} < 4V$
- Power package with low thermal resistance
- Drain current rating of 20A minimum
- Drain-Source voltage > 15V

The on-resistance ($R_{DS(ON)}$) is the primary parameter for MOSFET selection. The on-resistance determines the power dissipation of the MOSFET and therefore significantly affects the efficiency of the DC-DC Converter. Table 5 presents a list of suitable MOSFETs for this application.

Table 5. MOSFET Selection Table

Manufacturer & Model #	Conditions[1]		$R_{DS,ON}(m\Omega)$ Typ.	$R_{DS,ON}(m\Omega)$ Max.	Package	Thermal Resistance
Fuji 2SK1388	V_{GS} = 4V, I_D = 17.5A	T_J = 25°C	25	37	TO-220	Φ_{JA} = 75
		T_J = 125°C	37	—		
Siliconix SI4410DY	V_{GS} = 4.5V, I_D = 5A	T_J = 25°C	16.5	20	SO-8 (SMD)	Φ_{JA} = 50
		T_J = 125°C	28	34		
National Semiconductor NDP706AL	V_{GS} = 5V, I_D = 40A	T_J = 25°C	13	15	TO-220	Φ_{JA} = 62.5 Φ_{JC} =1.5
NDP706AEL		T_J = 125°C	20	24		
National Semiconductor NDP603AL	V_{GS} = 4.5V, I_D = 10A	T_J = 25°C	31	40	TO-220	Φ_{JA} = 62.5
		T_J = 125°C	42	54		Φ_{JC} = 2.5
National Semiconductor NDP606AL	V_{GS} = 5V, I_D = 24A	T_J = 25°C	22	25	TO-220	Φ_{JA} = 62.5
		T_J = 125°C	33	40		Φ_{JC} = 1.5
Motorola MTB75N03HDL	V_{GS} = 5V, I_D = 37.5A	T_J = 25°C	6	9	TO-263 (D_2 PAK)	Φ_{JA} = 62.5
		T_J = 125°C	9.3	14		Φ_{JC} = 1.0
Int. Rectifier IRLZ44	V_{GS} = 5V, I_D = 31A	T_J = 25°C	—	28	TO-220	Φ_{JA} = 62.5
		T_J = 125°C	—	46		Φ_{JC} = 1.0
Int. Rectifier IRL3103S	V_{GS} = 4.5V, I_D = 28A	T_J = 25°C	—	19	TO-220	Φ_{JA} = 62.5
		T_J = 125°C		31		Φ_{JC} = 1.0

Note: $R_{DS(ON)}$ values at T_J = 125°C for most devices were extrapolated from the typical operating curves supplied by the manufacturers and are approximations only. Only National Semiconductor offers maximum values at T_J = 125°C.

Two MOSFETs in Parallel

We recommend that two MOSFETs be used in parallel instead of one single MOSFET. Significant advantages are realized using two MOSFETs in parallel:

- **Significant reduction of power dissipation**.

  Maximum current of 14A with one MOSFET:

  $P_{MOSFET} = (I^2 R_{DS(ON)})(\text{Duty Cycle}) = (14)^2(0.050*)(3.3+0.4)/(5+0.4-0.35) = 7.2$ W

  With two MOSFETs in parallel:

  $P_{MOSFET} = (I^2 R_{DS(ON)})(\text{Duty Cycle}) = (14/2)^2(0.037*)(3.3+0.4)/(5+0.4-0.35) = 1.3$W/FET

- *Note: $R_{DS(on)}$ increases with temperature. Assume $R_{DS(on)}$=25mΩ at 25°C. $R_{DS(on)}$ can easily increase to 50mΩ at high temperature when using a single MOSFET. When using two MOSFETs in parallel, the temperature effects should not cause the $R_{DS(on)}$ to rise above the listed maximum value of 37mΩ.

- **Less heat sink required.** With power dissipation down to around one watt and with MOSFETs mounted flat on the motherboard, there will be considerably less heat sink required. The junction-to-case thermal resistance for the MOSFET package (TO-220) is typically at 2°C/W and the motherboard serves as an excellent heat sink.

- **Higher current capability.** With thermal management under control, this on-board DC-DC converter is able to deliver load currents up to 14.5A with no problem at all.

MOSFET Gate Bias

Figure 5 employs a charge pump to provide gate bias. Capacitor CP is the charge pump deployed to boost the voltage of the RC5040 output driver. When the MOSFET switches off, the source of the MOSFET is at -0.6V. VCCQP is charged through the Schottky diode to 4.5V. Thus, the capacitor CP is charged to 5V. When the MOSFET turns on, the source of the MOSFET voltage is equal to 5V. The capacitor voltage follows, and hence provides a voltage at VCCQP equal to 10V. The Schottky is required to provide the charge path when the MOSFET is off. The Schottky reverses bias when the VCCQP goes to 10V. The charge pump capacitor, CP, needs to be a high Q and high frequency capacitor. A 1µF ceramic capacitor is recommended here.

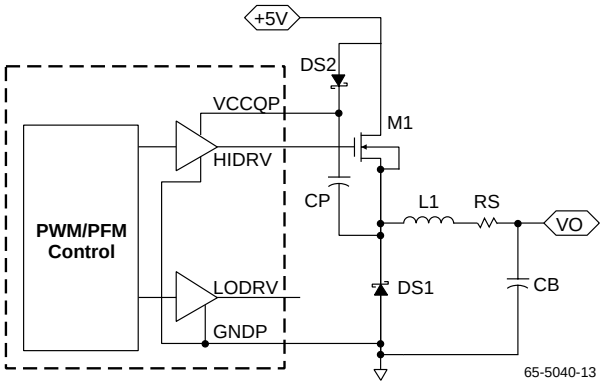


Figure 5. Charge Pump Configuration

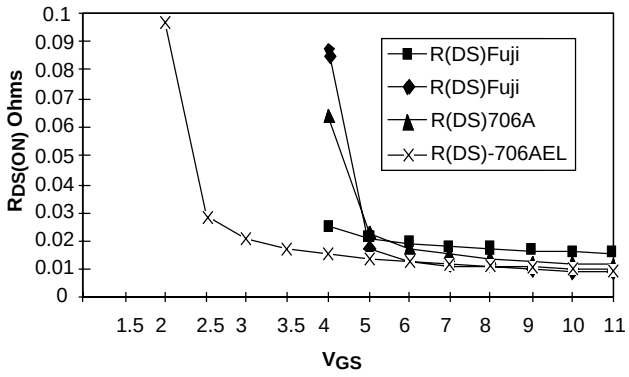


Figure 6. R(DS) vs. V_{GS} for Selected MOSFETs

Converter Efficiency

Losses due to parasitic resistance in the switches, coil, and sense resistor dominate at high load-current level. The major loss mechanisms under heavy loads, in usual order of importance, are:

- MOSFET I^2R Losses
- Inductor Coil Losses
- Sense Resistor Losses
- gate-charge losses
- diode-conduction losses
- transition losses
- Input Capacitor losses
- losses due to the operating supply current of the IC.

Efficiency of the converter under heavy loads can be calculated as follows:

$$\text{Efficiency} = \frac{P_{OUT}}{p_{IN}} = \frac{I_{OUT} \times V_{OUT}}{I_{OUT} \times V_{OUT} + P_{LOSS}},$$

where $P_{LOSS} = PD_{MOSFET} + PD_{INDUCTOR} + PD_{RSENSE} + PD_{GATE} + PD_{DIODE} + PD_{TRAN} + PD_{CAP} + PD_{IC}$

Design Equations:

(1) $PD_{MOSFET} = I_{OUT}^2 \times R_{DS(ON)} \times \text{DutyCycle}$

where $\text{DutyCycle} = \frac{V_{OUT} + V_D}{V_{IN} + V_D - V_{SW}}$

(2) $PD_{INDUCTOR} = I_{OUT}^2 \times R_{INDUCTOR}$

(3) $PD_{RSENSE} = I_{OUT}^2 \times R_{SENSE}$

(4) $PD_{GATE} = q_{GATE} \times f \times 5V$, where q_{GATE} is the gate charge and f is the switching frequency

(5) $PD_{DIODE} = V_f \times I_{OUT}(1 - \text{Dutycycle})$

(6) $PD_{TRAN} = \frac{V_{IN}^2 \times C_{RSS} \times I_{LOAD} \times f}{I_{DRIVE}}$, where C_{RSS} is the reverse transfer capacitance of the high-side MOSFET.

(7) $PD_{CAP} = I_{RMS}^2 \times ESR$

(8) $PD_{IC} = V_{CC} \times I_{CC}$

Example:

$$DutyCycle = \frac{3.3 + 0.5}{5 + 0.5 - 0.3} = 0.73$$

$PD_{MOSFET} = 10^2 \times 0.030 \times 0.73 = 2.19W$

$PD_{INDUCTOR} = 10^2 \times 0.010 = 1W$

$PD_{RSENSE} = 10^2 \times 0.0065 = 0.65W$

$PD_{GATE} = CV \times f \times 5V = 1.75nf \times (9 - 1)V \times 650Khz \times 5V = 0.045W$

$PD_{DIODE} = 0.5 \times 10(1 - 0.73) = 1.35W$

$$PD_{TRAN} = \frac{5^2 \times 400pf \times 10 \times 650khz}{0.7A} \sim 0.010W$$

$PD_{CAP} = (7.5 - 2.5)^2 \times 0.015 = 0.37W$

$PD_{IC} = 0.2W$

$PD_{LOSS} = 2.19W + 1.0W + 0.65W + 0.045W + 1.35W + 0.010W + 0.37W + 0.2W = 5.815W$

$$\therefore \text{ Efficiency} = \frac{3.3 \times 10}{3.3 \times 10 + 5.815} \sim 85\%$$

Selecting the Inductor

The inductor is one of the most critical components to be selected in the DC-DC converter application.. The critical parameters are inductance (L), maximum DC current (Io) and the coil resistance (R1). The inductor core material is a crucial factor in determining the amount of current the inductor will be able to withstand. As with all engineering designs, tradeoffs exist between various types of core materials. In general, Ferrites are popular due to their low cost, low EMI properties and high frequency (>500KHz) characteristics. Molypermalloy powder (MPP) materials exhibit good saturation characteristics, low EMI and low hysteresis losses; however, they tend to be expensive and more effectively utilized at operating frequencies below 400KHz. Another critical parameter is the DC winding resistance of the inductor. This value should typically be reduced as much as possible, as the power loss in the DC resistance will degrade the efficiency of the converter by the relationship: $P_{LOSS} = I_O^2$ x R1. The value of the inductor is a function of the oscillator duty cycle (T_{ON}) and the maximum inductor current (I_{PK}). I_{PK} can be calculated from the relationship:

$$I_{PK} = I_{MIN} + \left(\frac{V_{IN} - V_{SW} - V_D}{L}\right) T_{ON}$$

Where T_{ON} is the maximum duty cycle and V_D is the forward voltage of diode DS1.

Then the inductor value can be calculated using the relationship:

$$L = \left(\frac{V_{IN} - V_{SW} - V_O}{I_{PK} - I_{MIN}}\right) T_{ON}$$

Where V_{SW} (R_{DSON} x I_O) is the drain-to-source voltage of M1 when it is switched on.

Implementing Short Circuit Protection

Intel currently requires all power supply manufacturers to provide continuous protection against short circuit conditions that may damage the CPU. To address this requirement, Fairchild Semiconductor has implemented a current sense methodology to disable the output drive signal to the MOSFET(s) when an over current condition is detected. The voltage drop created by the output current flowing across a sense resistor is presented to one terminal of an internal comparator with hysterisis. The other comparator terminal has the threshold voltage, nominally of 120mV. Table 6 states the limits for the comparator threshold of the Switching Regulator.

Table 6. RC5040 Short Circuit Comparator Threshold Voltage

	Short Circuit Comparator $V_{threshold}$ (mV)
Typical	120
Minimum	100
Maximum	140

When designing the external current sense circuitry, the designer must pay careful attention to the output limitations during normal operation and during a fault condition. If the short circuit protection threshold current is set too low, the DC-DC converter may not be able to continuously deliver the maximum CPU load current. If the threshold level is too high, the output driver may not be disabled at a safe limit and the resulting power dissipation within the MOSFET(s) may rise to destructive levels.

The design equation used to set the short circuit threshold limit is as follows:

$$R_{SENSE} = \frac{V_{th}}{I_{SC}}, \text{ where: } I_{SC} = \text{Output short circuit current}$$

$$I_{SC} \geq I_{inductor} = I_{Load,\,max} + \frac{(I_{PK} - I_{min})}{2}$$

Where I_{pk} and I_{min} are peak ripple current and $I_{load,\,max}$ = maximum output load current

The designer must also take into account the current ($I_{PK} - I_{min}$), or the ripple current flowing through the inductor under normal operation. Figure 7 illustrates the inductor current waveform for the RC5040 DC-DC converter at maximum load.

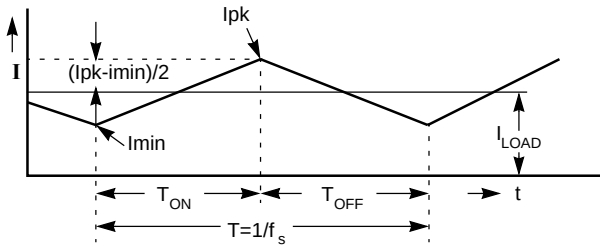


Figure 7. Typical DC-DC Converter Inductor Current Waveform

The calculation of this ripple current is as follows:

$$\frac{(I_{pk} - I_{min})}{2} = \frac{(V_{IN} - V_{SW} - V_{OUT})}{L} \times \frac{(V_{OUT} + V_D)}{(V_{IN} - V_{SW} + V_D)} T$$

where:
- V_{in}= input voltage to Converter
- V_{SW}=voltage across Switcher (MOSFET) =I_{LOAD} x $R_{DS(ON)}$
- V_D= Forward Voltage of the Schottky diode
- T = the switching period of the converter = 1/fs, where f_S = switching frequency.

For an input voltage of 5V, an output voltage of 3.3V, an inductor value of 1.3µH and a switching frequency of 650KHz (using C_{EXT} = 39pF), the inductor current can be calculated as
follows:

$$\frac{(I_{pk} - I_{min})}{2} = \frac{(5.0 - 14.5 \times 0.037 - 3.3)}{1.3 \times 10^{-6}} \times$$

$$\frac{(3.3 + 0.5)}{(5.0 - 14.5 \times 0.037 + 0.5)} \times \frac{1}{650 \times 10^3} = 1.048\text{A}$$

Therefore, the peak current, I_{PK}, through the inductor for a 14.5A load is found to be:

$$I_{SC} \geq I_{inductor} = I_{Load,\,max} + \frac{(I_{PK} - I_{min})}{2} = 14.5 + 1 = 15.5\text{A}$$

As a result, the short circuit detection threshold must be at least 15.5A.

The next step is to determine the value of the sense resistor. Including sense resistor tolerance, the sense resistor value can be approximated as follows

$$R_{SENSE} = \frac{V_{th,min}}{I_{SC}} \times (1 - TF) = \frac{V_{th,min}}{1.0 + I_{Load,max}} \times (1 - TF)$$

Where TF = Tolerance Factor for the sense resistor.

There are several different type of sense resistors. Table 7 describes tolerance, size, power capability, temperature coefficient and cost of various type of sense resistors.

Table 7. Comparison of Sense Resistors[1]

Description	Motherboard Trace Resistor	Discrete Iron Alloy resistor (IRC)	Discrete Metal Strip surface mount resistor (Dale)	Discrete MnCu Alloy wire resistor	Discrete CuNi Alloy wire resistor (Copel)
Tolerance Factor (TF)	±29%	±5% (±1% available)	±1%	±10%	±10%
Size (L x W x H)	2" x 0.2" x 0.001" (1 oz Cu trace)	0.45" x 0.065" x 0.200"	0.25" x 0.125" x 0.025"	0.200" x 0.04" x 0.160"	0.200" x 0.04" x 0.100"
Power capability	>50A/in	1 watt (3W and 5W available)	1 watt	1 watt	1 watt
Temperature Coefficient	+4,000 ppm	+30 ppm	±75 ppm	±30 ppm	±20 ppm
Cost @10,000 piece	Low included in motherboard	$0.31	$0.47	$0.09	$0.09

Notes:
1. Refer to Appendix A for Directory of component suppliers

Based on the Tolerance in the above table,

For Embedded PC Trace Resistor and for $I_{load,max}$=14.5A**:**

$$R_{SENSE} = \frac{V_{th,min}}{1.0A + I_{Load,\,max}} \times (1 - TF)$$

$$= \frac{100mV}{1.0A + 14.5A} \times (1 - 29\%) = 4.6m\Omega$$

For discrete resistor and $I_{load,\,max}$ = 14.5A**:**

$$R_{SENSE} = \frac{V_{th,min}}{1.0A + I_{Load,\,max}} \times (1 - TF)$$

$$= \frac{100mV}{1.0A + 14.5A} \times (1 - 5\%) = 6.1m\Omega$$

For user convenience, Table 8 lists recommended Value for sense resistor for various load current using Embedded PC Trace Resistor or Discrete Resistor.

Table 8. R_{sense} for various load currents

$I_{Load,max}$ (A)	R_{SENSE} PC Trace Resistor (mΩ)	R_{SENSE} Discrete Resistor (mΩ)
10.00	6.5	8.6
11.20	5.8	7.8
12.40	5.3	7.1
13.90	4.8	6.4
14.00	4.7	6.3
14.50	4.6	6.1

RC5040 Short Circuit Current Characteristics

The RC5040 has a short circuit current characteristic that includes a hysteresis function that prevents the DC-DC converter from oscillating in the event of a short circuit. A typical V-I characteristic of the DC-DC converter output with a sense resistor of 6 mΩ is presented in the Typical Operating Characteristics section, page 5. The converter performs with a normal load regulation characteristic until the voltage across the resistor reaches the internal short circuit threshold of 120mV. At this point, the internal comparator trips and sends a signal to the controller to turn off the gate drive to the power MOSFET. This causes a drastic reduction in the output voltage as the load regulation collapses into the short circuit mode of control. The output voltage will not return to the normal load characteristic until the output short circuit current is reduced to within the safe range for the DC-DC converter.

Schottky Diode Selection

The application circuit diagrams of Figures 1 and 2 show two Schottky diodes, DS1 and DS2. In synchronous mode, DS1 is used in parallel with M3 to prevent the lossy diode in the FET from turning on. DS2 serves a dual purpose. As configured, it allows the VCCQP supply pin of the RC5040 to be bootstrapped up to 9V using capacitor C12. When the lower MOSFET M3 is turned on, one side of capacitor C12 is connected to ground while the other side of the capacitor is being charged up to voltage VIN - VD through DS2. The voltage that is then applied to the gate of the MOSFET is VCCQP – VSAT, or typically around 9V. A vital selection criteria for DS1 and DS2 is that they exhibit a very low forward voltage drop, as this parameter can directly affect the regulator efficiency. In non-synchronous mode, DS1 is used as a flyback diode to provide a constant current path for the inductor when M1 is turned off. Table 9 lists several suitable Schottky diodes. Note that the MBR2015CTL has a very low forward voltage drop. This diode is most ideal for application where output voltage is required to be less than 2.8V.

Table 9. Schottky Diode Selection Table

Manufacturer Model #	Conditions	Forward Voltage V_F
Philips	I_F = 20A; T_j = 25°C	< 0.84V
PBYR1035	I_F = 20A; T_j = 125°C	< 0.72V
Motorola	I_F = 20A; T_j = 25°C	< 0.84V
MBR2035CT	I_F = 20A; T_j = 125°C	< 0.72V
Motorola	I_F = 15A; T_j = 25°C	< 0.84V
MBR1545CT	I_F = 15A; T_j = 125°C	< 0.72V
Motorola	I_F = 20A; T_j = 25°C	< 0.58V
MBR2015CTL	I_F = 20A; T_j = 150°C	< 0.48V

Output Filter Capacitors

Optimal ripple performance and transient response are functions of the filter capacitors used. Since the 5V supply of a PC motherboard may be located several inches away from the DC-DC converter, input capacitance can play an important role in the load transient response of the RC5040. The higher the input capacitance, the more charge storage is available for improving the current transfer through the FET. Low “ESR" capacitors are best suited for this type of application and can influence the converter's efficiency if not chosen carefully. The input capacitor should be placed as close to the drain of the FET as possible to reduce the effect of ringing caused by long trace lengths.

The ESR rating of a capacitor is a difficult number to quantify. ESR or Equivalent Series Resistance, is defined as the resonant impedance of the capacitor. Since the capacitor is actually a complex impedance device having resistance, inductance and capacitance, it is quite natural for this device to have a resonant frequency. As a rule, the lower the ESR, the better suited the capacitor is for use in switching power supply applications. Many capacitor manufacturers do not supply ESR data. A useful estimate of the ESR can be obtained using the following equation:

$$ESR = \frac{DF}{2\pi fC}$$

Where:

- DF is the dissipation factor of the capacitor
- f is the operating frequency
- C is the capacitance in farads

With this in mind, correct calculation of the output capacitance is crucial to the performance of the DC-DC converter. The output capacitor determines the overall loop stability, output voltage ripple and load transient response. The calculation is as follows:

$$C(\mu F) = \frac{I_O \times \Delta T}{\Delta V - I_O \times ESR}$$

Where ΔV is the maximum voltage deviation due load transient

ΔT is reaction time of the power source (Loop response time of the RC5040) and it is approximately 8µs

I_O is the output load current

For I_O = 10A, and ΔV = 75mV, the bulk capacitor required can be approximated as follows:

$$C(\mu F) = \frac{I_O \times \Delta T}{\Delta V - I_O \times ESR} = \frac{10A \times 8\mu s}{75mV - 10A \times 5m\Omega} = 3200\mu F$$

Input filter

We recommend that the design include an input inductor between the system +5V supply and the DC-DC converter input described below. This inductor will serve to isolate the +5V supply from noise occurring in the switching portion of the DC-DC converter and to also limit the inrush current into the input capacitors on power up. A value of around 2.5µH is recommended.

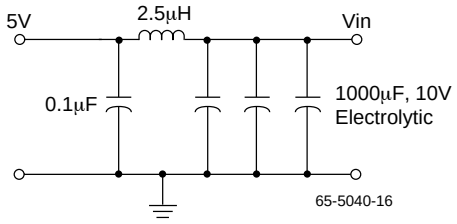


Figure 8. Input Filter

PCB Layout Guidelines and Considerations

PCB Layout Guidelines

1. Placement of the MOSFETs relative to the RC5040 is critical. The MOSFETs (M1 & M2), should be placed such that the trace length of the HIDRV pin from the RC5040 to the FET gates is minimized. A long lead length on this pin will cause high amounts of ringing due to the inductance of the trace combined with the large gate capacitance of the FET. This noise will radiate all over the board, and because it is switching at such a high voltage and frequency, it will be very difficult to suppress.

   Figure 9 below depicts an example of good placement for the MOSFETs in relation to the RC5040 and also an example of problematic placement for the MOSFETs.

   In general, all of the noisy switching lines should be kept away from the quiet analog section of the RC5040. That is to say, traces that connect to pins 12 and 13 (HIDRV and VCCQP) should be kept far away from the traces that connect to pins 1 through 5, and pin 16.

2. Place decoupling capacitors (.1µF) as close to the RC5040 pins as possible. Extra lead length on these will negate their ability to suppress noise.

3. Each VCC and GND pin should have its own via down to the appropriate plane underneath. This will help give isolation between pins.

4. Surround the CEXT timing capacitor with a ground trace as much as possible. Also be sure to keep a ground or power plane underneath the capacitor for further noise isolation. This will help to shield the oscillator pin 1 from the noise on the PCB. Place this capacitor as close to the RC5040 pin 1 as possible.

5. Place MOSFETs, inductor and Schottky as close together as possible for the same reasons as #1 above. Place the input bulk capacitors as close to the drains of MOSFETs as possible. In addition, placement of a 0.1µF decoupling cap right on the drain of each MOSFET will help to suppress some of the high frequency switching noise on the input of the DC-DC converter.

6. The traces that run from the RC5040 IFB (pin 4) and VFB (pin 5) pins should be run together next to each other and be Kelvin connected to the sense resistor. Running these lines together will help in rejecting some of the common noise that is presented to the RC5040 feedback input. Try as much as possible to run the noisy switching signals (HIDRV & VCCQP) on one layer; and use the inner layers for only power and ground. If the top layer is being used to route all of the noisy switching signals, use the bottom layer to route the analog sensing signals VFB and IFB.

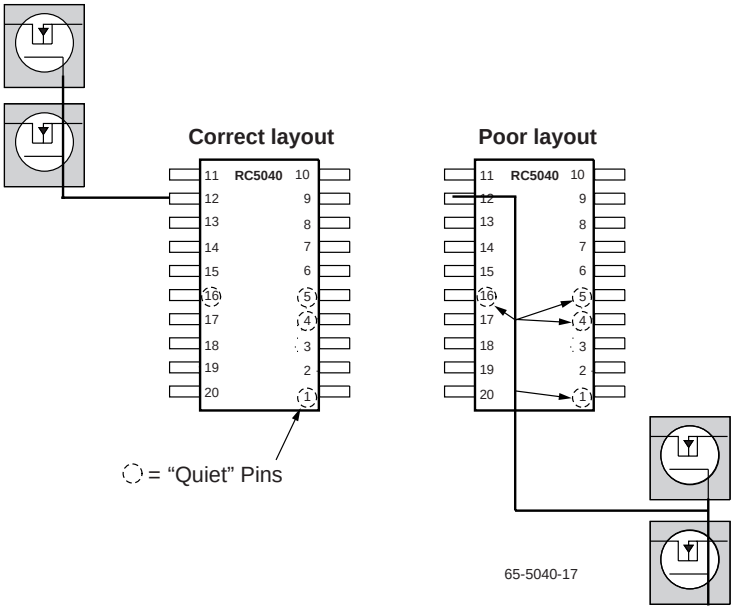


Figure 9. MOSFET Layout Guidelines

Example of a Layout on a PC Motherboard and Gerber File

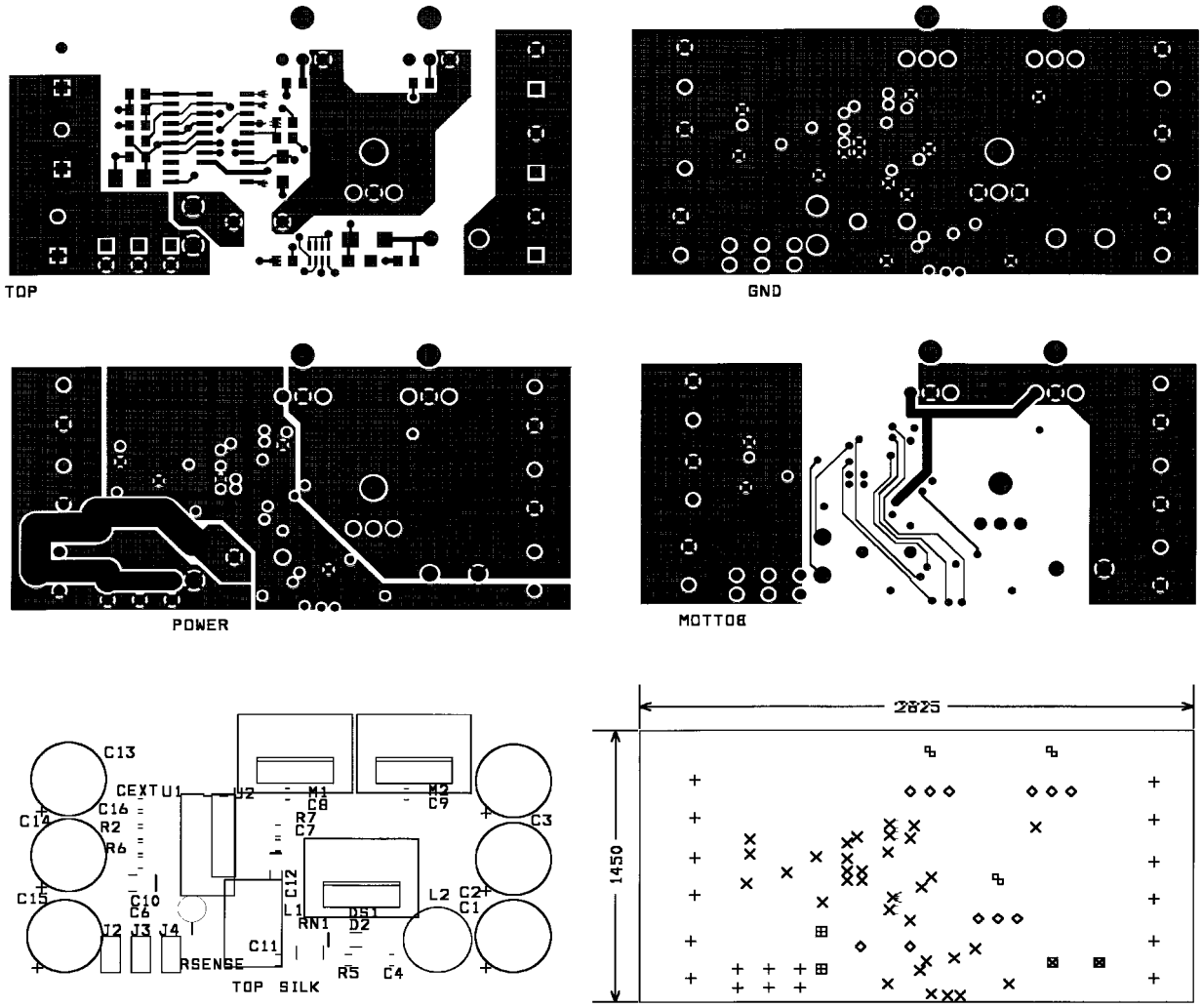
A reference design for motherboard implementation of the RC5040 along with Layout Gerber File and Silk Screen are presented below. The actual Gerber File can be obtained from a Fairchild Semiconductor local Sales Rep Office or from Fairchild Semiconductor Marketing Department at 415-966-7819.

RC5040 Evaluation Board

Fairchild Semiconductor provides an evaluation board for the purpose of verifying the system level performance of the RC5040. The evaluation board serves as a guide as to what can be expected in performance with the supplied external components and PCB layout. Please call your Fairchild Semiconductor local Sales Rep Office or Fairchild Semiconductor Marketing department at 415-966-7819 for an evaluation board.

Additional Application Information

A comprehensive Application Note providing implementation guidelines for the RC5040 and RC5042 DC-DC Converters for Pentium® Pro processors (AP-42) is available from your local Fairchild Semiconductor Sales Rep or from Fairchild Semiconductor Marketing at 415-966-7819. Most application notes and data sheets can also be obtained by calling Fairchild Semiconductor's RAYFAX line at 415-988-2123.

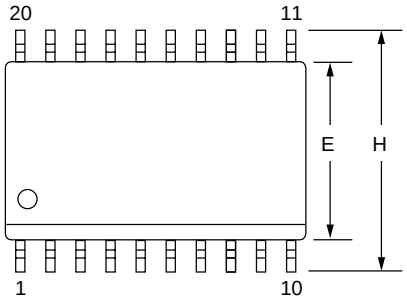


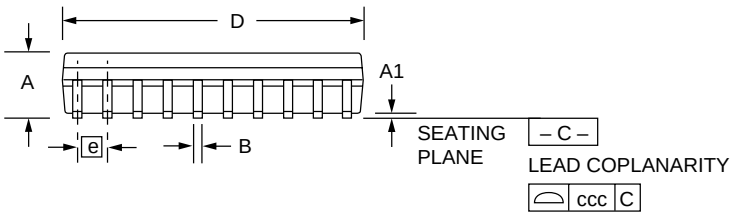
Mechanical Dimensions – 20 Lead SOIC

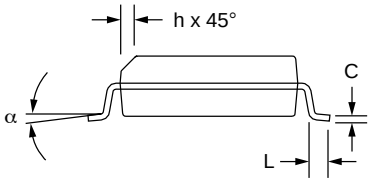
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.496	.512	12.60	13.00	2
E	.291	.299	7.40	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.029	0.25	0.75	
L	.016	.050	0.40	1.27	3
N	20		20		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Ordering Information

Product Number	Package
RC5040M	20 pin SOIC

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

5/20/98 0.0m 001
Stock#DS30005040

RC5041

Programmable DC-DC Converter for Pentium® P55C, K6™, and 6x86MX™ (M2) Processors

Features

- Programmable output from 2.1V to 3.5V using integrated 4-bit DAC
- 87% efficiency
- Oscillator frequency adjustable from 200KHz to 1MHz
- On-chip Power Good function
- Excellent transient response
- Over-Voltage Protection
- Short Circuit Protection
- Power Good Function
- Precision trimmed low TC voltage reference
- 16 pin SOIC package
- Meets Intel Pentium VRM specifications using minimum number of external components

Applications

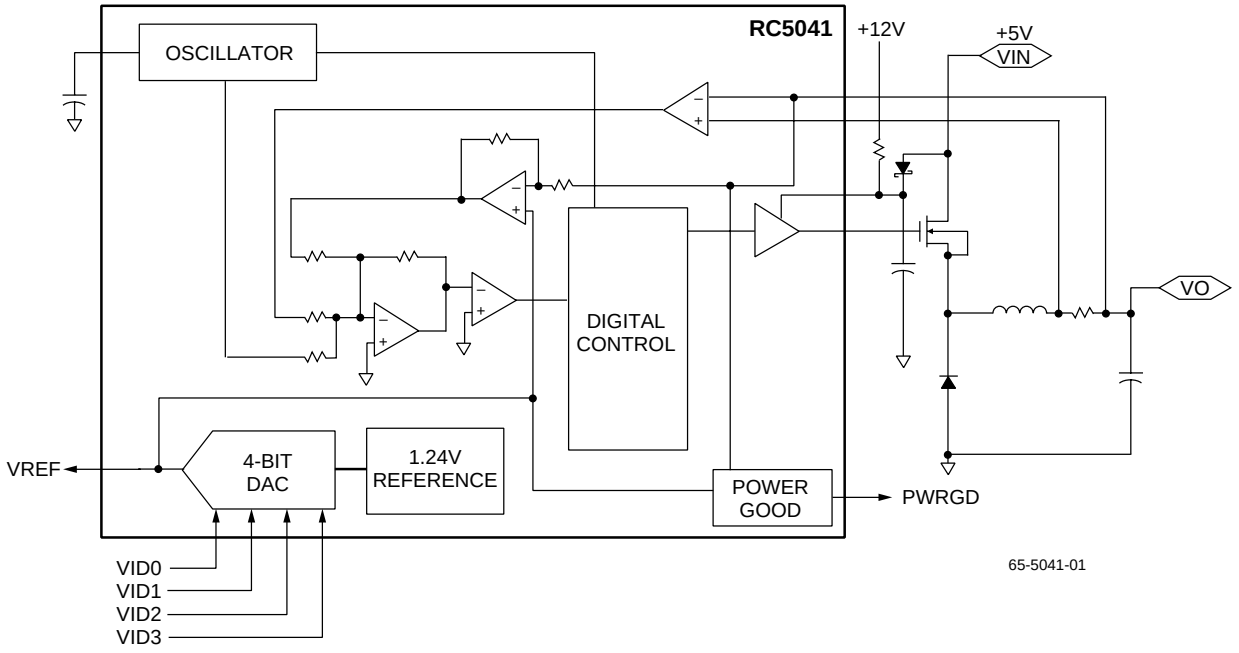
- Programmable power supply for P54C, P55C, K6, and M2 based CPU motherboards
- VRM module for Pentium and equivalent CPU's
- Programmable power supply for high current microprocessors

Description

The RC5041 is a non-synchronous DC-DC controller IC which provides an accurate, programmable output for Pentium CPU applications. Using an integrated 4-bit DAC to accept a voltage identification (VID), the RC5041 can generate precise output voltages between 2.1V and 3.5V in 100mV increments. Output load currents in excess of 10A can be delivered using minimal external circuitry. The RC5041 is designed to operate in a standard PWM control mode under heavy load conditions and in PFM control mode while supplying light loads for optimal efficiency. An on-board precision low TC voltage reference eliminates the requirement for external components in order to achieve tight voltage regulation. The Pentium CPU is continuously protected by an integrated Power Good function, which sends an active-low interrupt signal to the CPU in the event that the output voltage is out of tolerance. The internal oscillator can be programmed to operate over a range of 200KHz to 1MHz to allow flexibility in choosing external components.

Preliminary Information

Block Diagram



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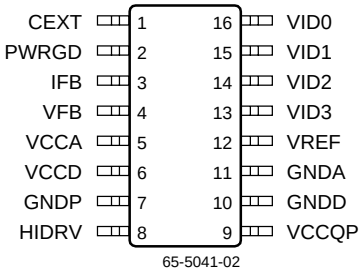
K6 is a trademark of AMD Corporation.
6x86MX is a trademark of Cyrix Corporation.

Pin Assignments



Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	CEXT	**Oscillator capacitor connection.** Connecting an external capacitor to this pin sets the internal oscillator frequency from 200 KHz to 1 MHz. Layout of this pin is critical to system performance. See Application Information for details.
2	PWRGD	**Power Good output flag.** Open collector output will be at logic HIGH under normal operation. Logic LOW indicates output voltage is not within ±10% of nominal.
3	IFB	**High side current feedback.** Pins short 4 and 5 are used as the inputs for the current feedback control loop and as the short circuit current sense points. Layout of these traces is critical to system performance. See Application Information for details.
4	VFB	**Voltage feedback.** Pin 5 is used as the input for the voltage feedback control loop and as the low side current feedback input. Layout of this trace is critical to system performance. See Application Information for details.
5	VCCA	**Analog V_{CC}.** Connect to system 5V supply and decouple to ground with 0.1μF ceramic capacitor.
6	VCCD	**Digital V_{CC}.** Connect to system 5V supply and decouple to ground with 4.7μF tantalum capacitor.
7	GNDP	**Power ground.** Return pin for high currents flowing in pins 8 and 9 (HIDRV and VCCQP). Connect to low impedance ground. See Application Information for details.
8	HIDRV	**FET driver output.** Connect this pin to the gate of the N-channel MOSFETs M1 and M2 in Figures 1 and 2. The trace from this pin to the MOSFET gates should be kept as short as possible (less than 0.5"). See Application Information for details.
9	VCCQP	**Power V_{CC} for FET Driver.** VCCQP must be connected to a voltage of at least VCCA + $V_{GS,ON}$ (M1). See Application Information for details.
10	GNDD	**Digital ground.** Return path for digital logic. This pin should be connected to system ground so that ground loops are avoided. See Application Information for details.
11	GNDA	**Analog ground.** Return path for low power analog circuitry. Connect to system ground so that ground loops are avoided. See Application Information for details.
12	VREF	**Reference voltage test point.** This pin provides access to the DAC output and should be decoupled to ground using a 0.1μF capacitor. No load should be connected to this pin.
13–16	VID3–VID0	**Voltage identification (VID) code inputs.** These open collector/TTL compatible inputs will program the output voltage over the ranges specified in Table 1.

Preliminary Information

Table 1. Voltage Identification Codes for P55/K6

Data Bits				$V_{CC}P$
VID3	VID2	VID1	VID0	(VDC)
1	1	1	1	No CPU
1	1	1	0	2.1
1	1	0	1	2.2
1	1	0	0	2.3
1	0	1	1	2.4
1	0	1	0	2.5
1	0	0	1	2.6
1	0	0	0	2.7

Data Bits				$V_{CC}P$
VID3	VID2	VID1	VID0	(VDC)
0	1	1	1	2.8
0	1	1	0	2.9
0	1	0	1	3.0
0	1	0	0	3.1
0	0	1	1	3.2
0	0	1	0	3.3
0	0	0	1	3.4
0	0	0	0	3.5

Absolute Maximum Ratings[1]

Control Supply Voltages, VCCA and VCCD	7V
FET Supply Voltage, VCCQP	13V
Voltage Identification Code Inputs, VID3-VID0	7V
Junction Temperature, T_J	150˚C
Storage Temperature, T_S	-65 to 150˚C
Lead Soldering Temperature, 10 seconds	300˚C

Notes:

1. Functional operation under any of these conditions is not implied. Permanent damage may occur if the device is subjected to conditions outside these ratings.

Operating Conditions

Parameter	Min.	Typ.	Max.	Units
Control Supply Voltages, VCCA and VCCD	4.75	5	5.25	V
Driver Supply Voltage, VCCQP	9	10	12	V
VID Code Input Voltage, Logic HIGH	2			V
VID Code Input Voltage, Logic LOW			0.8	V
PWRGD HIGH Threshold		±7		%VREF
PWRGD LOW Threshold		±10		%VREF
Ambient Temperature, T_A	0		70	°C

Electrical Specifications

(V_{CCA} = 5V, V_{OUT} = 2.8V, f_{osc} = 300 KHz, and T_A = +25°C using circuit in Figure 1, unless otherwise noted)
The • denotes specifications which apply over the full operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
Output Voltage	See Table 1	•			3.5	V
Output Current				13		A
Initial Voltage Setpoint	I_{LOAD} = 0.8A			±20		mV
Output Temperature Drift	T_A = 0 to 60°C	•		+10		mV
Load Regulation	I_{LOAD} = 0.8A to 10A	•		-20		mV
Line Regulation	V_{IN} = 4.75V to 5.25V	•		±2		mV
Output Ripple/Noise, pk-pk	20MHz BW, I_{LOAD} = 10A			20		mV

Preliminary Information

Electrical Specifications (continued)

(V_{CCA} = 5V, V_{OUT} = 2.8V, f_{osc} = 300 KHz, and T_A = +25°C using circuit in Figure 1, unless otherwise noted)
The • denotes specifications which apply over the full operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
Output Voltage Regulation Steady State[1] Transient[2]	 V_{OUT} = 2.8V, I_{LOAD} = 0 to 10A I_{LOAD} = 0.8 to 9.5A, 30A/µS	 • •	 2.74 2.70	 2.80 2.80	 2.90 2.90	 V V
Efficiency	I_{LOAD} = 10A, V_{OUT} = 2.8V	•	80	85		%
Output Driver Rise and Fall Time	See Figure 2			50		ns
Turn-on Response Time	I_{LOAD} = 0A to 10A				10	ms
Oscillator Range			80	300	1000	KHz
Oscillator Frequency	C_{EXT} = 100 pF			300		KHz
Maximum Duty Cycle			90	95		%

Notes:

1. Steady State Voltage Regulation includes Initial Voltage Setpoint, DC load regulation, outut ripple/noise and temperature drift.
2. These specifications assume a minimum of 20, 1µF ceramic capacitors are placed directly next to the CPU in order to provide adequate high-speed decoupling. For motherboard applications, the PCB layout must exhibit no more than 0.5mΩ parasitic resistance and 1nH parasitic inductance between the converter output and the CPU.

Test Circuits

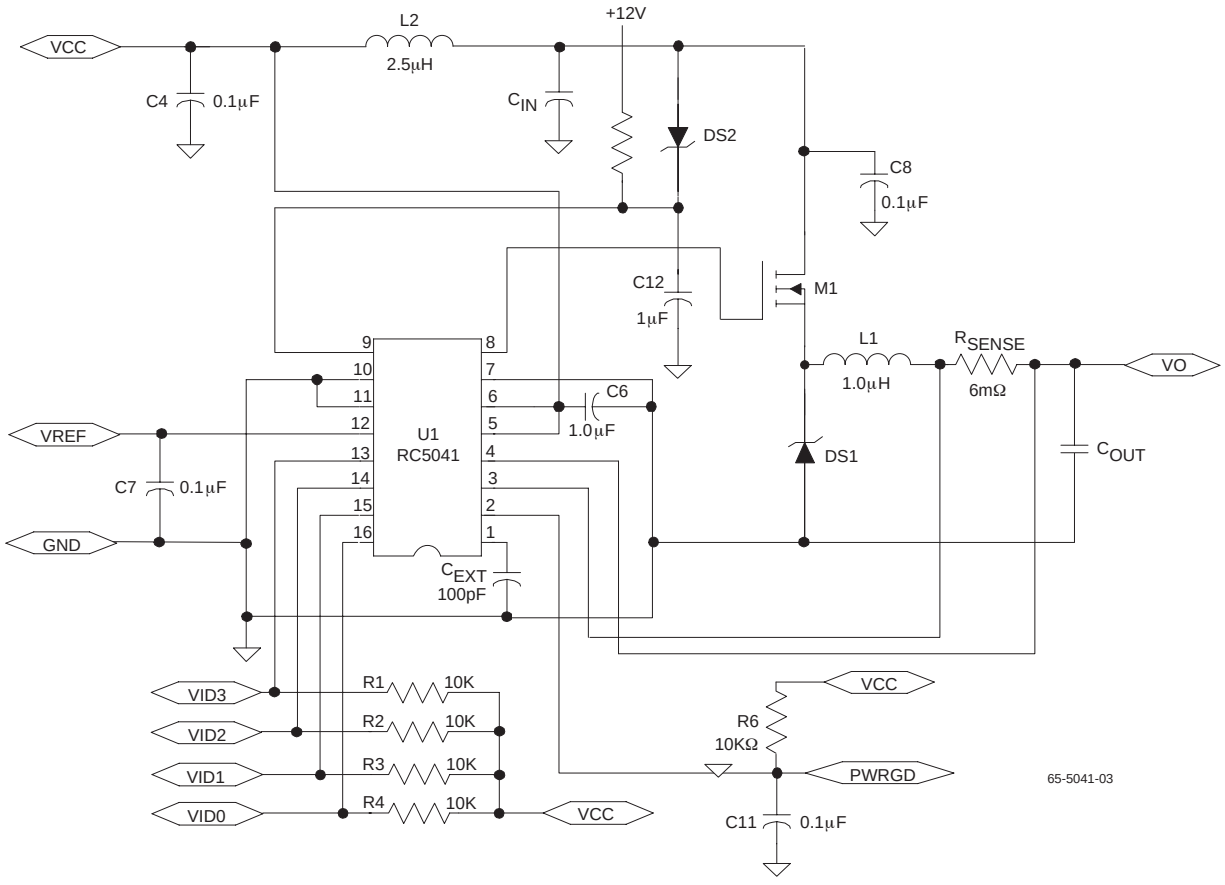


Figure 1. Standard Test or Application Schematic

Preliminary Information

Table 2. Bill of Materials for a 4-Bit Non-Synchronous DC-DC Converter

Item	Description	Comments
C4	Ceramic Capacitor, 0.1μF, X7R, SMT0805	
C12	Ceramic Capacitor, 1μF, X7R, SMT0805	
C8	Ceramic Capacitor, 0.1μF, X7R, SMT0805	
C_{EXT}	Ceramic Capacitor, 100pF, X7R, SMT0805	
C6	Ceramic Capacitor, 1μF, X7R, SMT0805	
C11	Ceramic Capacitor, 0.1μF, X7R, SMT0805	
C7	Capacitor, 0.1μF, X7R, SMT0805	
C_{IN}	Capacitor, Al-Elect, 1200μF, 10v, 10 x 20 radial	See Table 3
C_{OUT}	Capacitor, Al-Elect, 1500μF, 6.3v, 10 x 20 radial	See Table 3
DS1	Schottky Diode, MBR2535CT	
DS2	Zener Diode, 1N5817	
L1	Output Inductor, 1.0μH, Toroid, 6 turns 17AWG	
L2	Input Inductor, 2.5μH, Toroid, 10 turns 17AWG	See Note 1
R_{SENSE}	Sense Resistor, CuNi Allow Wire, 1W, 6mΩ, 10%	
R1	10KΩ Resistor, 1/8W, 5%, SMT0805	
R2	10KΩ Resistor, 1/8W, 5%, SMT0805	
R3	10KΩ Resistor, 1/8W, 5%, SMT0805	
R4	10KΩ Resistor, 1/8W, 5%, SMT0805	
R6	10KΩ Resistor, 1/8W, 5%, SMT0805	
M1	N-ch Power FET	See Table 2
U1	PWM Controller, Fairchild Semiconductor RC5041M	

Note:

1. The inductor L2 is recommended to isolate the 5V ipower supply from current surges caused by the MOSFET switching. This inductor is not required for the proper operation of the DC-DC converter and can be substituted with a ferrite beads inductor or omitter completely.

Table 3. Part Selection Table

K6 CPU	Output Voltage	I_{MAX}	Fairchild Semiconductor DC-DC Converter	CIN Sanyo 10MV1200GX	COUT Sanyo 6MV1500GX	MOSFET
166 MHz	2.9V	6.25A	RC5041	1x	2x	IRL3103
200 MHz	2.9V	7.5A		1x	2x	IRL3103
233 MHz	3.2V	9.5A		2x	4x	IRL3103
266 MHz	3.2V	13.0A		3x	6x	IRL2203
300 MHz+	2.1V	5.6A		1x	2x	IRL3103

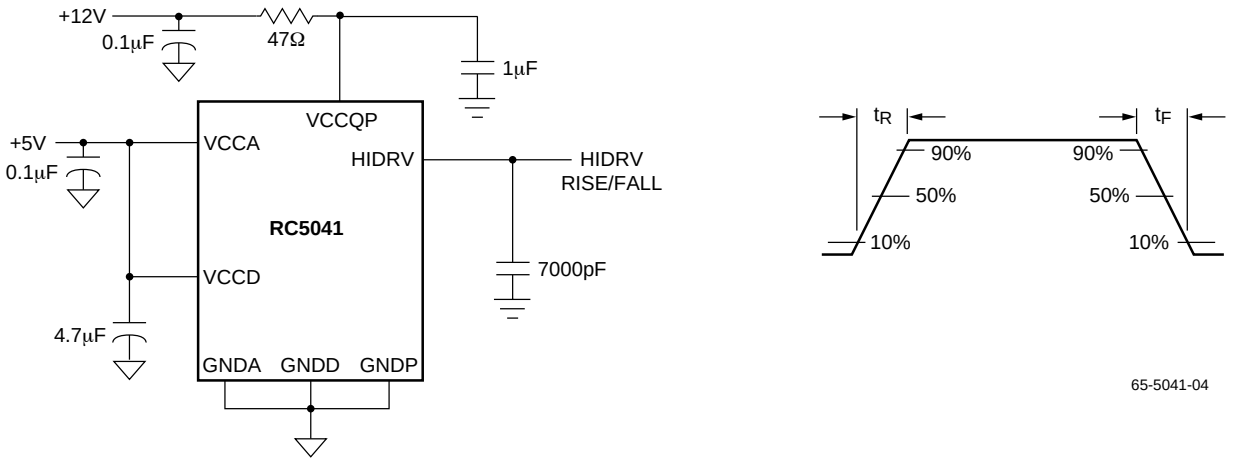


Figure 2. Output Driver Test Circuit

Application Information

Simple Step-Down Converter

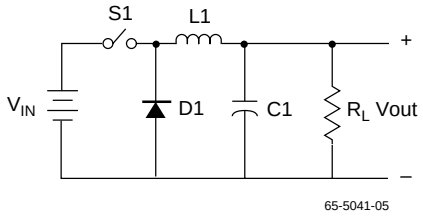


Figure 3. Simple Buck DC-DC Converter

Figure 3 illustrates a step-down DC-DC converter with no feedback control. The derivation of the basic step-down converter will serve as a basis for the design equations for the RC5041. Referring to Figure 3, the basic operation begins by closing the switch S1. When S1 is closed, the input voltage V_{IN} is impressed across inductor L1. The current flowing in this inductor is given by the following equation:

$$I_L = \frac{(V_{IN} - V_{OUT})T_{ON}}{L1}$$

Where T_{ON} is the duty cycle (the time when S1 is closed).

When S1 opens, the diode D1 will conduct the inductor current and the output current will be delivered to the load according to the equation:

$$I_L = \frac{V_{OUT}(T_S - T_{ON})}{L1}$$

Where T_S is the overall switching period, and $(T_S - T_{ON})$ is the time during which S1 is open.

By solving these two equations, we can arrive at the basic relationship for the output voltage of a step-down converter:

$$V_{OUT} = V_{IN}\left(\frac{T_{ON}}{T_S}\right)$$

In order to obtain a more accurate approximation for V_{OUT}, we must also include the forward voltage V_D across diode D1 and the switching loss, Vsw. After taking into account these factors, the new relationship becomes:

$$V_{OUT} = (V_{IN} + V_D - V_{SW})\frac{T_{ON}}{T_S} - V_D$$

Overview

The RC5041 is a programmable DC-DC controller IC. When designed around the appropriate external components, the RC5041 can be configured to deliver more than 14.5A of output current. During heavy loading conditions, the RC5041 functions as a current-mode PWM step-down regulator. Under light loads, the regulator functions in the PFM (pulse frequency modulation), or pulse skipping mode. The controller will sense the load level and switch between the two operating modes automatically, thus optimizing its efficiency under all loading conditions.

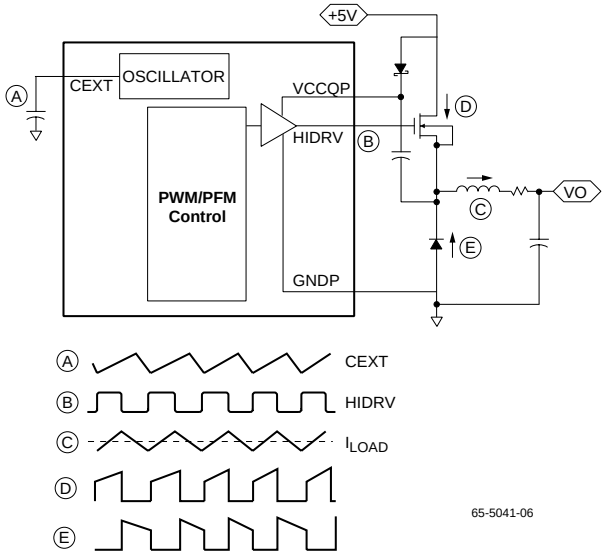


Figure 4. Typical Switching Waveforms

Main Control Loop

Refer to the Block Diagram on page 1. The control loop of the regulator contains two main sections, the analog control block and the digital control block. The analog block consists of signal conditioning amplifiers feeding into a set of comparators which provide the inputs to the digital block. The signal conditioning section accepts inputs from the IFB (current feedback) and VFB (voltage feedback) pins and sets up two controlling signal paths. The voltage control path amplifies the VFB signal and presents the output to one of the summing amplifier inputs. The current control path takes the difference between the IFB and VFB pins and presents the resulting signal to another input of the summing amplifier. These two signals are then summed together with the slope compensation input from the oscillator. This output is then presented to a comparator, which provides the main PWM control signal to the digital control block.

The additional comparators in the analog control section set the thresholds of where the RC5041 enters its pulse skipping mode during light loads as well as the point at which the maximum current comparator disables the output drive signals to the external power MOSFETs.

The digital control block is designed to take the comparator inputs along with the main clock signal from the oscillator and provide the appropriate pulses to the HIDRV output pin that controls the external power MOSFET. The digital section was designed utilizing high speed Schottky transistor logic, thus allowing the RC5041 to operate at clock speeds as high as 1MHz.

High Current Output Drivers

The RC5041 contains one high current output drivers which utilize high speed bipolar transistors arranged in a push-pull configuration. The driver is capable of delivering 1A of current in less than 100ns. The driver's power and ground are separated from the overall chip power and ground for additional switching noise immunity.

Internal Voltage Reference

The reference included in the RC5041 is a 1.24V precision band-gap voltage reference. The internal resistors are precisely trimmed to provide a near zero temperature coefficient (TC). Added to the reference input is the resulting output from an integrated 4-bit DAC. The DAC is provided in accordance with the Pentium Pro specification guideline, which requires the DC-DC converter output to be directly programmable via a 4-bit voltage identification (VID) code. This code will scale the reference voltage from 2.0V (no CPU) to 3.5V in 100mV increments. For guaranteed stable operation under all loading conditions, a 10KΩ pull-up resistor and 0.1µF of decoupling capacitance should be connected to the VREF pin.

Power Good

The RC5041 Power Good function is designed in accordance with the Pentium Pro DC-DC converter specification and provides a constant voltage monitor on the VFB pin. The circuit compares the VFB signal to the VREF voltage and outputs an active-low interrupt signal to the CPU should the power supply voltage exceed ±12% of its nominal setpoint. The Power Good flag provides no other control function to the RC5041.

Over-Voltage Protection

The RC5041 provides a constant monitor of the output voltage for protection against overvoltage conditions. If the voltage at the VFB pin exceeds 20% of the selected program voltage, an overvoltage condition will be assumed, and the RC5041 will disable the output drive signal to the MOSFET(s).

Short Circuit Protection

A current sense methodology is implemented to disable the output drive signal to the MOSFET(s) when an over-current condition is detected. The voltage drop created by the output current flowing across a sense resistor is presented to an internal comparator. When voltage developed across the sense resistor exceeds the comparator threshold voltage, the RC5041 will disable the output drive signal to the MOSFET(s).

The DC-DC converter returns to normal operation after the fault has been removed, for either an overvoltage or a short circuit condition.

Oscillator

The RC5041 oscillator section is implemented using a fixed current capacitor charging configuration. An external capacitor (CEXT) is used to preset the oscillator frequency between 80KHz and 1MHz. This scheme allows maximum flexibility in setting the switching frequency as well as choosing external components.

In general, a lower operating frequency will increase the peak ripple current flowing in the output inductor, and thus require the use of a larger inductor value. Operation at lower frequencies also increases the amount of energy storage that must be provided by the bulk output capacitors during load transients due to the slower loop response of the controller.

The user should note that the efficiency losses due to switching are relatively fixed per switching cycle. Therefore, as the switching frequency is increased, so is the contribution toward efficiency due to switching losses.

Careful analysis of the RC5041 DC-DC controller has resulted in an optimal operating frequency of 300KHz, which allows the use of smaller inductive and capacitive components while maximizing peak efficiency under all operating conditions.

Design Considerations and Component Selection

MOSFET Selection

This application requires N-channel Logic Level Enhancement Mode Field Effect Transistors. Desired characteristics are as follows:

- Low Static Drain-Source On-Resistance, $R_{DS(on)}$ < 20 mΩ (lower is better)
- Low gate drive voltage, V_{GS} < 4V
- Power package with low thermal resistance
- Drain current rating of 20A minimum
- Drain-Source voltage > 15V.

The on-resistance ($R_{DS(ON)}$) is the primary parameter for MOSFET selection. The on-resistance determines the power dissipation of the MOSFET and therefore significantly affects the efficiency of the DC-DC Converter. Table 3 provides a list of suitable MOSFETs for this application.

Table 3. MOSFET Selection Table

Manufacturer & Model #	Conditions[1]		$R_{DS,ON}$(mΩ) Typ.	$R_{DS,ON}$(mΩ) Max.	Package	Thermal Resistance
Megamos MiP30N03A	V_{GS} = 4.5V, I_D = 6A	T_J = 25°C	16	25	TO-220	Φ_{JA} = 62
		T_J = 125°C	—	38		
Fuji 2SK1388	V_{GS} = 4V, I_D = 20A	T_J = 25°C	25	37	TO-220	Φ_{JA} = 75
		T_J = 125°C	37	56		
Int. Rectifier IRL3803	V_{GS} = 4.5V, I_D = 59A	T_J = 25°C	6.1	9	TO-220	Φ_{JA} = 62
		T_J = 125°C		14		
Int. Rectifier IRL2203	V_{GS} = 4.5V, I_D = 50A	T_J = 25°C	8.2	10	TO-220	Φ_{JA} = 62
		T_J = 125°C	—	16		
Int. Rectifier IRL3103	V_{GS} = 4.5V, I_D = 28A	T_J = 25°C	16	19	TO-220	Φ_{JA} = 62
		T_J = 125°C	—	29		
NS NDP706A	V_{GS} = 5.0V, I_D = 40A	T_J = 25°C	13	15	TO-220	Φ_{JA} = 62
		T_J = 125°C	20	24		
NEC 2SK2941	V_{GS} = 4.0V, I_D = 18A	T_J = 25°C	22	33	TO-220	Φ_{JA} = 83
		T_J = 125°C	—	50		
NEC 2SK2984	V_{GS} = 4.0V, I_D = 20A	T_J = 25°C	10.5	15	TO-220	Φ_{JA} = 83
		T_J = 125°C	—	23		
NEC μPA1703	V_{GS} = 4.0V, I_D = 5A	T_J = 25°C	12	17	SO-8	Φ_{JA} = 125
		T_J = 125°C	—	26		
Int. Rectifier IRF7413A	V_{GS} = 4.5V, I_D = 3.3A	T_J = 25°C	—	20	SO-8	Φ_{JA} = 125
		T_J = 125°C	—	30		
Int. Rectifier IRF7413	V_{GS} = 4.5V, I_D = 3.7A	T_J = 25°C	—	18	SO-8	Φ_{JA} = 125
		T_J = 125°C	—	27		
Int. Rectifier IRL3103A	V_{GS} = 4.5V, I_D = 28A	T_J = 25°C	—	19	D^2 PAK	Φ_{JA} = 40
		T_J = 125°C	—	29		

Note:

1. $R_{DS(ON)}$ values at T_J=125°C for most devices were extrapolated from the typical operating curves supplied by the manufacturers and are approximations only. Only National Semiconductor offers maximum values at T_J = 125°C.

Two MOSFETs in Parallel

For high current requirements, we recommend that two MOSFETs be used in parallel instead of one single MOSFET. Significant advantages are realized using two MOSFETs in parallel:

- **Significant reduction of power dissipation**.

  Maximum current of 14A with one MOSFET:

  $P_{MOSFET} = (I^2 R_{DS(ON)})(\text{Duty Cycle})$
  $= (14)^2(0.050^*)(3.3+0.4)/(5+0.4-0.35)$
  $= 7.2\ W$

  With two MOSFETs in parallel:

  $P_{MOSFET} = (I^2 R_{DS(ON)})(\text{Duty Cycle})$
  $= (14/2)^2(0.037^*)(3.3+0.4)/(5+0.4-0.35)$
  $= 1.3W/FET$

  *Note: $R_{DS(on)}$ increases with temperature. Assume $R_{DS(on)}$ = 0.025 at 25°C. $R_{DS(on)}$ can easily increase to 0.050W at high temperature when using a single MOSFET. When using two MOSFETs in parallel, the temperature effects should not cause the $R_{DS(on)}$ to rise above the listed maximum value of 37mW.

- **Less heat sink required.**
  With power dissipation down to around one watt and with MOSFETs mounted flat on the motherboard, there will be considerably less heat sink required. The junction-to-case thermal resistance for the MOSFET package (TO-220) is typically at 2°C/W and the motherboard serves as an excellent heat sink.

- **Higher current capability.**
  With thermal management under control, this on-board DC-DC converter is able to deliver load currents up to 14.5A with no problem at all.

MOSFET Gate Bias

The MOSFET can be biased by one of two methods: Charge Pump and 12V Gate Bias.

Method 1. Charge pump (or Bootstrap) method

Figure 5 employs a charge pump to provide gate bias. Capacitor CP is the charge pump deployed to boost the voltage of the RC5041 output driver. When the MOSFET switches off, the source of the MOSFET is at -0.6V. VCCQP is charged through the Schottky diode to 4.5V. Thus, the capacitor CP is charged to 5V. When the MOSFET turns on, the source of the MOSFET voltage is equal to 5V. The capacitor voltage follows, and hence provides a voltage at VCCQP equal to 10V. The Schottky is required to provide the charge path when the MOSFET is off. The Schottky reverses bias when the VCCQP goes to 10V. The charge pump capacitor, CP, needs to be a high Q and high frequency capacitor. A 1µF ceramic capacitor is recommended here.

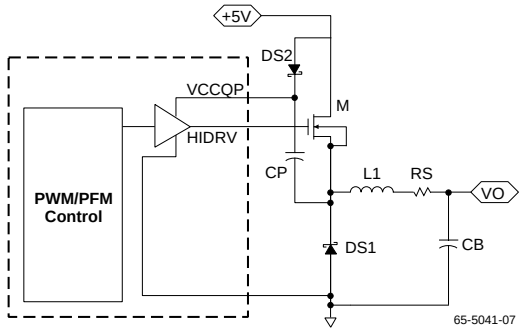


Figure 5. Charge Pump Configuration

Method 2. 12V Gate Bias

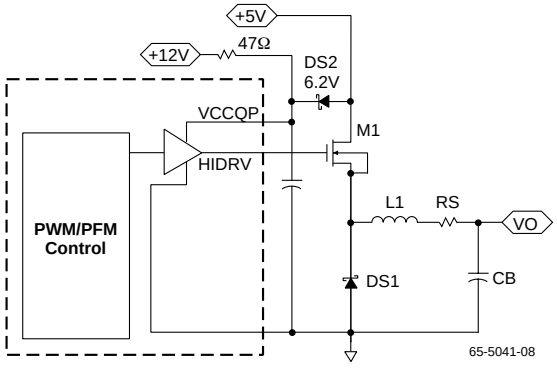


Figure 6. 12V Gate Bias Configuration

Figure 7 uses an external 12V source to bias VCCQP. A 47Ω resistor is used to limit the transient current into the VCCQP pin. A 1µF capacitor filter is used to filter the VCCQP supply. This method provides a higher gate bias voltage to the MOSFET, and therefore reduces the $R_{SD(ON)}$ and resulting power loss within the MOSFET. Figure 8 illustrates how $R_{DS(ON)}$ decreases dramatically as V_{GS} increases. A 6.2V Zener (DS2) is used to clamp the voltage at V_{CCQP} to a maximum of 12V and ensure that the absolute maximum voltage of the IC will not be exceeded.

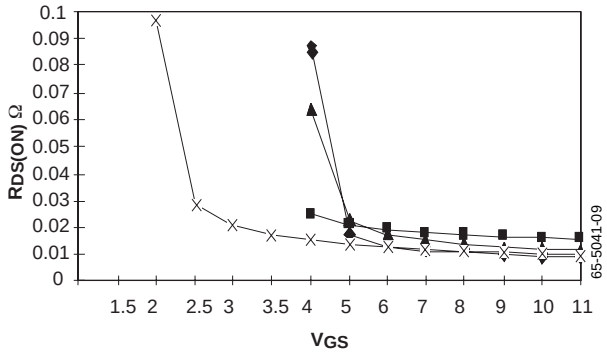


Figure 7. R(DS) vs. V_{GS} for Typical MOSFETs

Preliminary Information

Converter Efficiency

Losses due to parasitic resistance in the switches, coil, and sense resistor dominate at high load-current level. The major loss mechanisms under heavy loads, in usual order of importance, are:

- MOSFET I^2R Losses
- Inductor coil losses
- Sense resistor losses
- Gate-charge losses
- Diode-conduction losses
- Transition losses
- Input capacitor losses
- Losses due to the operating supply current of the IC.

Efficiency of the converter under heavy loads can be calculated as follows:

$$\text{Efficiency} = \frac{P_{OUT}}{p_{IN}} = \frac{I_{OUT} \times V_{OUT}}{I_{OUT} \times V_{OUT} + P_{LOSS}},$$

where $P_{LOSS} = PD_{MOSFET} + PD_{INDUCTOR} + PD_{RSENSE} + PD_{GATE} + PD_{DIODE} + PD_{TRAN} + PD_{CAP} + PD_{IC}$

Design Equations:

(1) $PD_{MOSFET} = I_{OUT}^2 \times (R_{DS(ON)} \times 1.5) \times \text{DutyCycle}$ where 1.5 is the temperature multiplier

where $\text{DutyCycle} = \frac{V_{OUT} + V_D}{V_{IN} + V_D - V_{SW}}$

(2) $PD_{INDUCTOR} = I_{OUT}^2 \times R_{INDUCTOR}$

(3) $PD_{RSENSE} = I_{OUT}^2 \times R_{SENSE}$

(4) $PD_{GATE} = q_{GATE} \times f \times 5V$, where q_{GATE} is the gate charge and f is the switching frequency

(5) $PD_{DIODE} = V_f \times I_{OUT}(1 - \text{Dutycycle})$

(6) $PD_{TRAN} = \frac{V_{IN}^2 \times C_{RSS} \times I_{LOAD} \times f}{I_{DRIVE}}$, where C_{RSS} is the reverse transfer capacitance of the MOSFET.

(7) $PD_{CAP} = I_{RMS}^2 \times ESR$

(8) $PD_{IC} = V_{CC} \times I_{CC}$

Example:

$\text{DutyCycle} = \frac{3.3 + 0.5}{5 + 0.5 - 0.1} = 0.70$

$PD_{MOSFET} = 10^2 \times (0.010 \times 1.5) \times 0.70 = 1.05W$

$PD_{INDUCTOR} = 10^2 \times 0.010 = 1W$

$PD_{RSENSE} = 10^2 \times 0.0065 = 0.65W$

$PD_{GATE} = CV \times f \times 5V = 1.75nf \times (9 - 1)V \times 300Khz \times 5V = 0.021W$

$PD_{DIODE} = 0.5 \times 10(1 - 0.70) = 1.5W$

$PD_{TRAN} = \frac{5^2 \times 400pf \times 10 \times 300khz}{0.7A} \sim 0.074W$

$PD_{CAP} = (7.5 - 2.5)^2 \times 0.015 = 0.37W$

$PD_{IC} = 0.2W$

$PD_{LOSS} = 1.05W + 1.0W + 0.65W + 0.021W + 1.50W + 0.074W + 0.37W + 0.2W = 4.865W$

$\therefore \text{Efficiency} = \frac{3.3 \times 10}{3.3 \times 10 + 4.865} \sim 87\%$

Selecting the Inductor

The inductor is one of the most critical components to be selected in the DC-DC converter application.. The critical parameters are inductance (L), maximum DC current (Io) and the coil resistance (R1). The inductor core material is a crucial factor in determining the amount of current the inductor will be able to withstand. As with all engineering designs, tradeoffs exist between various types of core materials. In general, Ferrites are popular due to their low cost, low EMI properties and high frequency (>500KHz) characteristics. Molypermalloy powder (MPP) materials exhibit good saturation characteristics, low EMI and low hysteresis losses; however, they tend to be expensive and more effectively utilized at operating frequencies below 400KHz. Another critical parameter is the DC winding resistance of the inductor. This value should typically be reduced as much as possible, as the power loss in the DC resistance will degrade the efficiency of the converter by the relationship: $P_{LOSS} = I_O^2$ x R1. The value of the inductor is a function of the oscillator duty cycle (T_{ON}) and the maximum inductor current (I_{PK}). I_{PK} can be calculated from the relationship:

$$I_{PK} = I_{MIN} + \left(\frac{V_{IN} - V_{SW} - V_D}{L}\right) T_{ON}$$

Where T_{ON} is the maximum duty cycle and V_D is the forward voltage of diode DS1.

Then the inductor value can be calculated using the relationship:

$$L = \left(\frac{V_{IN} - V_{SW} - V_O}{I_{PK} - I_{MIN}}\right) T_{ON}$$

Where V_{SW} (R_{DSON} x I_O) is the drain-to-source voltage of M1 when it is switched on.

Implementing Short Circuit Protection

Intel currently requires all power supply manufacturers to provide continuous protection against short circuit conditions that may damage the CPU. To address this requirement, Fairchild Semiconductor has implemented a current sense methodology to disable the output drive signal to the MOSFET(s) when an over current condition is detected. The voltage drop created by the output current flowing across a sense resistor is presented to one terminal of an internal comparator with hysterisis. The other comparator terminal has the threshold voltage, nominally of 120mV. Table 4 states the limits for the comparator threshold of the Switching Regulator.

Table 4. RC5041 Short Circuit Comparator Threshold Voltage

	Short Circuit Comparator $V_{threshold}$ (mV)
Typical	120
Minimum	100
Maximum	140

When designing the external current sense circuitry, pay careful attention to the output limitations during normal operation and during a fault condition. If the short circuit protection threshold current is set too low, the DC-DC converter may not be able to continuously deliver the maximum CPU load current. If the threshold level is too high, the output driver may not be disabled at a safe limit and the resulting power dissipation within the MOSFET(s) may rise to destructive levels.

The design equation used to set the short circuit threshold limit is as follows:

$$R_{SENSE} = \frac{V_{th}}{I_{SC}}, \text{ where: } I_{SC} = \text{Output short circuit current}$$

$$I_{SC} \geq I_{inductor} = I_{Load,\,max} + \frac{(I_{PK} - I_{min})}{2}$$

Where I_{pk} and I_{min} are peak ripple current and $I_{load,\,max}$ = maximum output load current.

The designer must also take into account the current ($I_{PK} - I_{min}$), or the ripple current flowing through the inductor under normal operation. Figure 8 illustrates the inductor current waveform for the RC5041 DC-DC converter at maximum load.

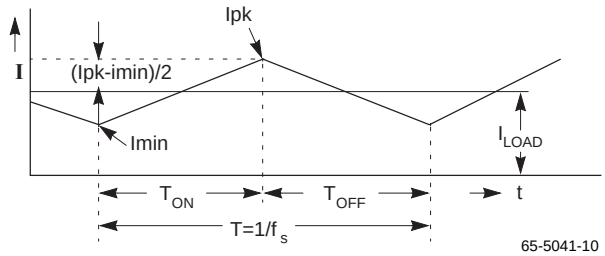


Figure 8. DC-DC Converter Inductor Current Waveform

The calculation of this ripple current is as follows:

$$\frac{(I_{pk} - I_{min})}{2} = \frac{(V_{IN} - V_{SW} - V_{OUT})}{L} \times \frac{(V_{OUT} + V_D)}{(V_{IN} - V_{SW} + V_D)} T$$

where:

- V_{in} = input voltage to Converter
- V_{SW} = voltage across Switcher (MOSFET) = I_{LOAD} x $R_{DS(ON)}$
- V_D = Forward Voltage of the Schottky diode
- T = the switching period of the converter = 1/fs, where f_S = switching frequency.

For an input voltage of 5V, an output voltage of 3.3V, an inductor value of 1.3µH and a switching frequency of 650KHz (using C_{EXT}=39pF), the inductor current can be calculated as follows:

Preliminary Information

Table 5. Comparison of Sense Resistors[1]

Description	Motherboard Trace Resistor	Discrete Iron Alloy resistor (IRC)	Discrete Metal Strip surface mount resistor (Dale)	Discrete MnCu Alloy wire resistor	Discrete CuNi Alloy wire resistor (Copel)
Tolerance Factor (TF)	±29%	±5% (±1% available)	±1%	±10%	±10%
Size (L x W x H)	2" x 0.2" x 0.001" (1 oz Cu trace)	0.45" x 0.065" x 0.200"	0.25" x 0.125" x 0.025"	0.200" x 0.04" x 0.160"	0.200" x 0.04" x 0.100"
Power capability	>50A/in	1 watt (3W and 5W available)	1 watt	1 watt	1 watt
Temperature Coefficient	+4,000 ppm	+30 ppm	±75 ppm	±30 ppm	±20 ppm
Cost @10,000 piece	Low included in motherboard	$0.31	$0.47	$0.09	$0.09

Notes:
1.Refer to Appendix A for Directory of component suppliers.

$$\frac{(I_{pk} - I_{min})}{2} = \frac{(5.0 - 14.5 \times 0.037 - 3.3)}{1.3 \times 10^{-6}} \times$$

$$\frac{(3.3 + 0.5)}{(5.0 - 14.5 \times 0.037 + 0.5)} \times \frac{1}{650 \times 10^{3}} = 1.048\text{A}$$

Therefore, the peak current, I_{PK}, through the inductor for a 14.5A load is found to be:

$$I_{SC} \geq I_{inductor} = I_{Load,\,max} + \frac{(I_{PK} - I_{min})}{2} = 14.5 + 1 = 15.5\text{A}$$

As a result, the short circuit detection threshold must be at least 15.5A

The next step is to determine the value of the sense resistor. Including sense resistor tolerance, the sense resistor value can be approximated as follows:

$$R_{SENSE} = \frac{V_{th,min}}{1 + I_{SC}} \times (1 - TF) = \frac{V_{th,min}}{1.0 + I_{Load,max} + I_R} \times (1 - TF)$$

Where TF = Tolerance Factor for the sense resistor.
I_R = Ripple Current = 1A

There are several different type of sense resistors. Table 7 describes tolerance, size, power capability, temperature coefficient and cost of various type of sense resistors:

Based on the Tolerance in Table 5,

- For Embedded PC Trace Resistor and for $I_{load,max}$ = 14.5A**:**

$$R_{SENSE} = \frac{V_{th,min}}{2.0\text{A} + I_{Load,\,max}} \times (1 - TF)$$

$$= \frac{100\text{mV}}{2.0\text{A} + 14.5\text{A}} \times (1 - 29\%) = 4.3\text{m}\Omega$$

- For discrete resistor and $I_{load,\,max}$ = 14.5A**:**

$$R_{SENSE} = \frac{V_{th,min}}{1.0\text{A} + I_{Load,\,max} + I_R} \times (1 - TF)$$

$$= \frac{100\text{mV}}{2.0\text{A} + 14.5\text{A}} \times (1 - 5\%) = 5.75\text{m}\Omega$$

For user convenience, Table 6 lists recommended value for sense resistor for various load current using embedded PC trace resistor or discrete resistor.

Table 6. R_{sense} for Various Load Current

$I_{Load,max}$ (A)	R_{SENSE} PC Trace Resistor (mΩ)	R_{SENSE} Discrete Resistor (mΩ)
10.00	5.9	7.9
11.20	5.4	7.2
12.40	4.9	6.6
13.90	4.5	6.0
14.00	4.4	5.9
14.50	4.3	5.7

RC5041 Short Circuit Current Characteristics

The RC5041 has a short circuit current characteristic that includes a hysteresis function that prevents the DC-DC converter from oscillating in the event of a short circuit. A typical V-I characteristic of the DC-DC converter output is presented in the Operating Conditions table. The converter performs with a normal load regulation characteristic until the voltage across the resistor reaches the internal short circuit threshold of 120mV. At this point, the internal comparator trips and sends a signal to the controller to turn off the gate drive to the power MOSFET. This causes a drastic reduction in the output voltage as the load regulation collapses into the short circuit mode of control. The output voltage will not return to the normal load characteristic until the output short circuit current is reduced to within the safe range for the DC-DC converter.

Schottky Diode Selection

The application circuit of Figure 1 shows a Schottky diode, DS1. DS1 is used as a flyback diode to provide a constant current path for the inductor when M1 is turned off. A vital selection criteria for DS1 is that it exhibits a very low forward voltage drop, as this parameter will directly impact the regulator efficiency as the output voltage is reduced. Table 7 presents several suitable Schottky diodes for this application. Note that the diode MBR2015CTL has a very low forward voltage drop. This diode is most ideal for applications where output voltages below 2.8V are required.

Table 7. Schottky Diode Selection Table

Manufacturer Model #	Conditions	Forward Voltage V_F
Philips	I_F = 20A; T_j = 25°C	< 0.84V
PBYR1035	I_F = 20A; T_j = 125°C	< 0.72V
Motorola	I_F = 20A; T_j = 25°C	< 0.84V
MBR2035CT	I_F = 20A; T_j = 125°C	< 0.72V
Motorola	I_F = 15A; T_j = 25°C	< 0.84V
MBR1545CT	I_F = 15A; T_j = 125°C	< 0.72V
Motorola	I_F = 20A; T_j = 25°C	< 0.58V
MBR2015CTL	I_F = 20A; T_j = 150°C	< 0.48V

Output Filter Capacitors

Optimal ripple performance and transient response are functions of the filter capacitors used. Since the 5V supply of a PC motherboard may be located several inches away from the DC-DC converter, input capacitance can play an important role in the load transient response of the RC5041. The higher the input capacitance, the more charge storage is available for improving the current transfer through the FET. Low “ESR” capacitors are best suited for this type of application and can influence the converter's efficiency if not chosen carefully. The input capacitor should be placed as close to the drain of the FET as possible to reduce the effect of ringing caused by long trace lengths.

The ESR rating of a capacitor is a difficult number to quantify. ESR or Equivalent Series Resistance, is defined as the resonant impedance of the capacitor. Since the capacitor is actually a complex impedance device having resistance, inductance and capacitance, it is quite natural for this device to have a resonant frequency. As a rule, the lower the ESR, the better suited the capacitor is for use in switching power supply applications. Many capacitor manufacturers do not supply ESR data. A useful estimate of the ESR can be obtained using the following equation:

$$ESR = \frac{DF}{2\pi fC}$$

Where DF is the dissipation factor of the capacitor, f is the operating frequency, and C is the capacitance in farads.

With this in mind, correct calculation of the output capacitance is crucial to the performance of the DC-DC converter. The output capacitor determines the overall loop stability, output voltage ripple and load transient response. The calculation is as follows:

$$C(\mu F) = \frac{I_O \times \Delta T}{\Delta V - I_O \times ESR}$$

Where ΔV is the maximum voltage deviation due load transient, ΔT is reaction time of the power source (Loop response time of the RC5041) and it is approximately 8μs), and I_O is the output load current.

For I_O = 10A, and ΔV = 75mV, the bulk capacitor required can be approximated as follows:

$$C(\mu F) = \frac{I_O \times \Delta T}{\Delta V - I_O \times ESR} = \frac{10A \times 8\mu s}{75mV - 10A \times 5m\Omega} = 3200\mu F$$

Input filter

We recommend that the design include an input inductor between the system +5V supply and the DC-DC converter input described below. This inductor will serve to isolate the +5V supply from noise occurring in the switching portion of the DC-DC converter and to also limit the inrush current into the input capacitors on power up. We recommend a value of around 2.5μH.

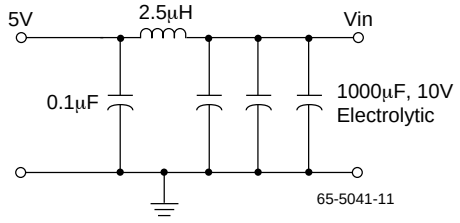


Figure 9. Input Filter

Preliminary Information

PCB Layout Guidelines and Considerations

PCB Layout Guidelines

- Placement of the MOSFETs relative to the RC5041 is critical. The MOSFETs (M1 & M2), should be placed such that the trace length of the HIDRV pin from the RC5041 to the FET gates is minimized. A long lead length on this pin will cause high amounts of ringing due to the inductance of the trace combined with the large gate capacitance of the FET. This noise will radiate all over the board, and because it is switching at such a high voltage and frequency, it will be very difficult to suppress.

  The drawing below depicts an example of good placement for the MOSFETs in relation to the RC5041 and also an example of problematic placement for the MOSFETs.

  In general, all of the noisy switching lines should be kept away from the quiet analog section of the RC5041. That is to say, traces that connect to pins 8 and 9 (HIDRV and VCCQP) should be kept far away from the traces that connect to pins 1 through 4, and pin 12.

- Place decoupling capacitors (.1µF) as close to the RC5041 pins as possible. Extra lead length on these will negate their ability to suppress noise.

- Each VCC and GND pin should have its own via down to the appropriate plane underneath. This will help give isolation between pins.

- Surround the CEXT timing capacitor with a ground trace as much as possible. Also be sure to keep a ground or power plane underneath the capacitor for further noise isolation. This will help to shield the oscillator pin 1 from the noise on the PCB. Place this capacitor as close to the RC5041 pin 1 as possible.

- Place MOSFETs, inductor and Schottky as close together as possible for the same reasons as #1 above. Place the input bulk capacitors as close to the drains of MOSFETs as possible. In addition, placement of a 0.1µF decoupling cap right on the drain of each MOSFET will help to suppress some of the high frequency switching noise on the input of the DC-DC converter.

- The traces that run from the RC5041 IFB (pin 3) and VFB (pin 4) pins should be run together next to each other and be Kelvin connected to the sense resistor. Running these lines together will help in rejecting some of the common noise that is presented to the RC5041 feedback input. Try as much as possible to run the noisy switching signals (HIDRV & VCCQP) on one layer; and use the inner layers for only power and ground. If the top layer is being used to route all of the noisy switching signals, use the bottom layer to route the analog sensing signals VFB and IFB.

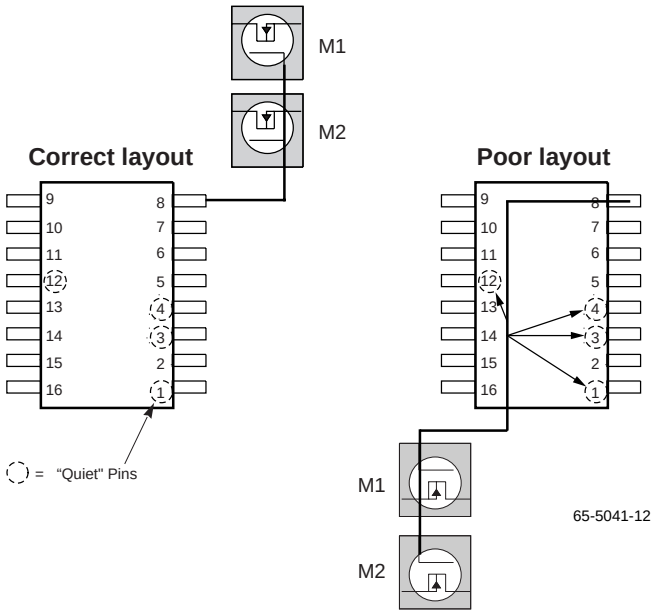


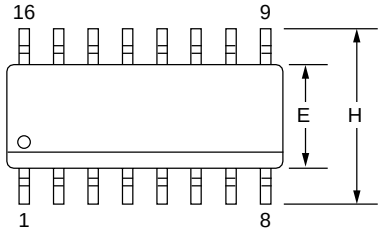
Figure 10. MOSFET Layout Guidelines

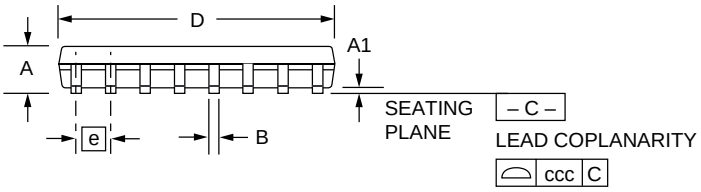
Mechanical Dimensions – 16 Lead SOIC

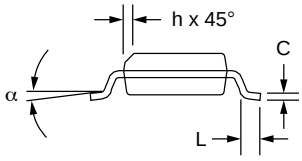
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.19	0.25	5
D	.386	.394	9.80	10.00	2
E	.150	.158	3.81	4.00	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.80	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	16		16		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Preliminary Information

Ordering Information

Product Number	Package
RC5041M	16 pin SOIC

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

5/20/98 0.0m 001
Stock#DS30005041

RC5042

Programmable DC-DC Converter

Features

- Programmable output from 2.1V to 3.5V using integrated 4-bit DAC
- 87% efficiency
- Oscillator frequency adjustable from 200KHz to 1MHz
- On-chip Power Good function
- Excellent transient response
- Over-Voltage Protection
- Short Circuit Protection
- Precision trimmed low TC voltage reference
- 16 pin SOIC package
- Meets Intel Pentium® Pro VRM specifications using minimum number of external components

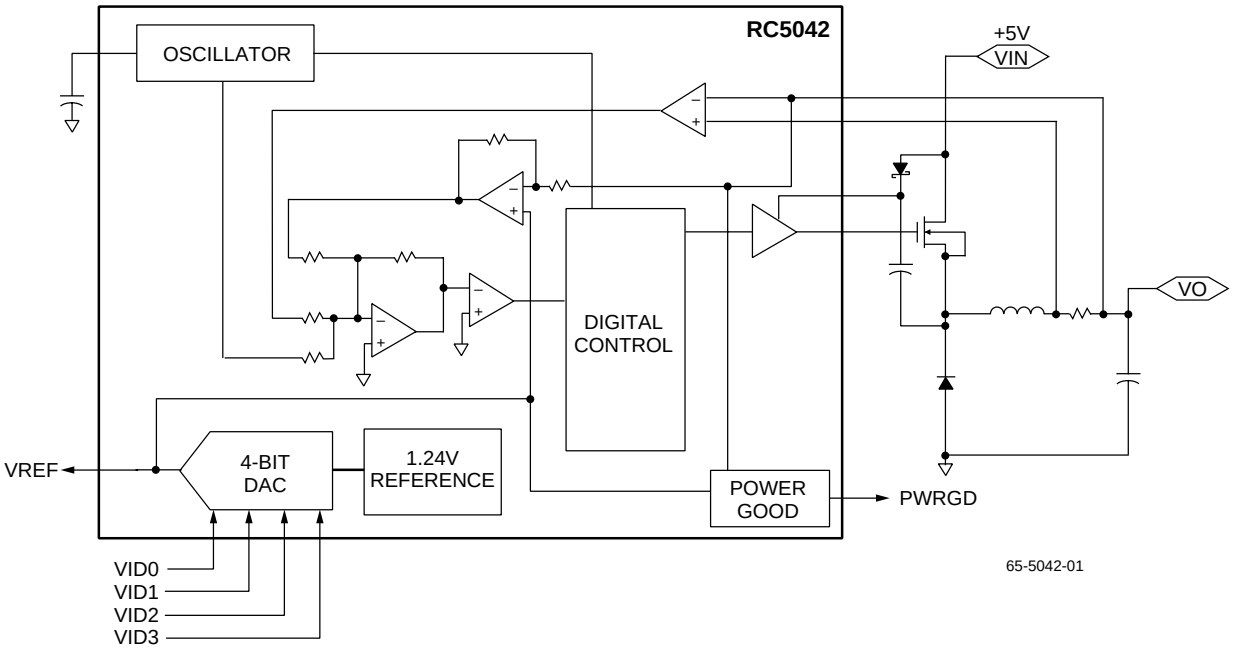
Applications

- Programmable power supply for Pentium Pro and Pentium-based CPU motherboards
- VRM module for Pentium Pro CPU
- Programmable power supply for high current microprocessors

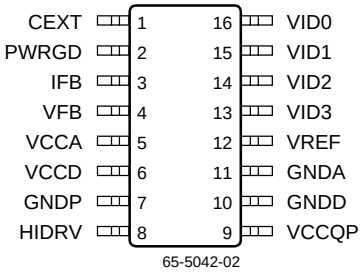
Description

The RC5042 is a non-synchronous DC-DC controller IC which provides an accurate, programmable output for Pentium Pro CPU applications. Using an integrated 4-bit DAC to accept a voltage identification (VID) code directly from the CPU, the RC5042 can generate precise output voltages between 2.1V and 3.5V in 100mV increments. Output load currents in excess of 12A can be delivered using minimal external circuitry. The RC5042 is designed to operate in a standard PWM control mode under heavy load conditions and in PFM control mode while supplying light loads for optimal efficiency. An on-board precision low TC voltage reference eliminates the requirement for external components in order to achieve tight voltage regulation. The Pentium Pro CPU is continuously protected by an integrated Power Good function, which sends an active-low interrupt signal to the CPU in the event that the output voltage is out of tolerance. The internal oscillator can be programmed to operate over a range of 200KHz to 1MHz to allow flexibility in choosing external components.

Block Diagram



Pin Assignments



65-5042-02

Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	CEXT	**Oscillator capacitor connection.** Connecting an external capacitor to this pin sets the internal oscillator frequency from 200 KHz to 1 MHz. Layout of this pin is critical to system performance. See Application Information for details.
2	PWRGD	**Power Good output flag.** Open collector output will be at logic HIGH under normal operation. Logic LOW indicates output voltage is not within ±10% of nominal.
3	IFB	**High side current feedback.** Pins short 4 and 5 are used as the inputs for the current feedback control loop and as the short circuit current sense points. Layout of these traces is critical to system performance. See Application Information for details.
4	VFB	**Voltage feedback.** Pin 5 is used as the input for the voltage feedback control loop and as the low side current feedback input. Layout of this trace is critical to system performance. See Application Information for details.
5	VCCA	**Analog V_{CC}.** Connect to system 5V supply and decouple to ground with 0.1μF ceramic capacitor.
6	VCCD	**Digital V_{CC}.** Connect to system 5V supply and decouple to ground with 4.7μF tantalum capacitor.
7	GNDP	**Power ground.** Return pin for high currents flowing in pins 8 and 9 (HIDRV and VCCQP). Connect to low impedance ground. See Application Information for details.
8	HIDRV	**FET driver output.** Connect this pin to the gate of the N-channel MOSFETs M1 and M2 in Figures 1 and 2. The trace from this pin to the MOSFET gates should be kept as short as possible (less than 0.5"). See Application Information for details.
9	VCCQP	**Power V_{CC} for FET Driver.** VCCQP must be connected to a voltage of at least VCCA + $V_{GS,ON}$ (M1). See Application Information for details.
10	GNDD	**Digital ground.** Return path for digital logic. This pin should be connected to system ground so that ground loops are avoided. See Application Information for details.
11	GNDA	**Analog ground.** Return path for low power analog circuitry. Connect to system ground so that ground loops are avoided. See Application Information for details.
12	VREF	**Reference voltage test point.** This pin provides access to the DAC output and should be decoupled to ground using a 0.1μF capacitor. No load should be connected to this pin.
13–16	VID3–VID0	**Voltage identification (VID) code inputs.** These open collector/TTL compatible inputs will program the output voltage over the ranges specified in Table 1. Internal 10KΩ pull-up resistors assure correct operation if pins are left unconnected.

Absolute Maximum Ratings[1]

Control Supply Voltages, VCCA and VCCD	13V
FET Supply Voltage, VCCQP	13V
Voltage Identification Code Inputs, VID3-VID0	13V
Junction Temperature, T_J	150˚C
Storage Temperature, T_S	-65 to 150˚C
Lead Soldering Temperature, 10 seconds	300˚C

Notes:

1. Functional operation under any of these conditions is not implied. Permanent damage may occur if the device is subjected to conditions outside these ratings.

Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Control Supply Voltages, VCCA and VCCD		4.5	5	7	V
Driver Supply Voltage, VCCQP		9	10	12	V
VID Code Input Voltage, Logic HIGH		2			V
VID Code Input Voltage, Logic LOW				0.8	V
PWRGD HIGH Threshold				+7	%VREF
PWRGD LOW Threshold		-7			%VREF
Ambient Temperature, T_A		0		70	°C

Electrical Specifications

(V_{CCA}, V_{CCD} = 5V, f_{osc} = 650 KHz, and T_A = +25°C using circuit in Figure 1, unless otherwise noted)
The • denotes specifications which apply over the full operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
Output Voltage	T_A = 0–70°C, See Table 1.	•	2.0		3.5	V
Output Current[1]				12.5	14.5	A
Setpoint Accuracy[2]	I_{LOAD} = 5.25A			1.0	1.5	%
Output Temperature Drift	T_A = 0–70°C	•		+100		ppm/°C
Load Regulation	I_{LOAD} = 0.5 to 12.5A	•		-0.5		%Vo
Line Regulation	V_{IN} = 4.75–5.25V, I_{LOAD} = 12.5A	•		+0.14		%Vo
Output Ripple/Noise, pk-pk	V_{OUT} = 2.1–3.5V, 20MHz BW	•		30		mV
Cumulative Accuracy[3]	T_A = 0–70°C	•		±3.3	±5.0	%
Efficiency	I_{LOAD} = 12.5A, V_{OUT} = 3.3V	•	80	85		%
Short Circuit Detect Threshold	Internal comparator offset	•	100	120	140	mV
Output Current Driver			0.5	1.0		A
Power Dissipation	No load			0.1	0.2	W
Thermal Impedance, θ_{JA}				150		°C/W
Response Time, Sleep to Full Load				10		µs
Oscillator Frequency Range[4]			0.2		1	MHz
Oscillator Frequency Accuracy	Excluding tolerance of C_{EXT}			10		%
Maximum Duty Cycle in PWM Mode			90	95		%
Minimum Duty Cycle in PFM Mode					100	ns

Electrical Specifications (continued)

(V_{CCA}, V_{CCD} = 5V, f_{osc} = 650 KHz, and T_A = +25°C using circuit in Figure 1, unless otherwise noted)
The • denotes specifications which apply over the full operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
Response Time to Short Circuit				15	30	ns
Soft Start Duration at Power-Up				10		μs
Load Transient, 0.5A to 12.5A step	Slew rate = 30A/μs			100		mV

Notes:

1. The maximum output current is limited only by the external components used and their thermal limitations. For loads greater than 12.5A, adequate thermal management is required to achieve optimal performance and reliability.
2. Setpoint Accuracy includes Output Ripple/Noise.
3. Cumulative Accuracy is determined by Setpoint Accuracy, Line and Load Regulation, Output Ripple/Noise, Transient Performance and Temperature Drift.
4. See Typical Operating Characteristics.

Table 1. Voltage Identification Codes[1]

Pentium Pro Processor Pins				VID Setpoint	Setpoint Accuracy[2] (mV)	Cumulative Accuracy[3] (mV)
VID3	VID2	VID1	VID0			
1	1	1	1	2.0	—	—
1	1	1	0	2.1	±31	±105
1	1	0	1	2.2	±33	±110
1	1	0	0	2.3	±34	±115
1	0	1	1	2.4	±36	±120
1	0	1	0	2.5	±37	±125
1	0	0	1	2.6	±39	±130
1	0	0	0	2.7	±40	±135
0	1	1	1	2.8	±42	±140
0	1	1	0	2.9	±43	±145
0	1	0	1	3.0	±45	±150
0	1	0	0	3.1	±46	±155
0	0	1	1	3.2	±48	±160
0	0	1	0	3.3	±49	±165
0	0	0	1	3.4	±51	±170
0	0	0	0	3.5	±60	±175

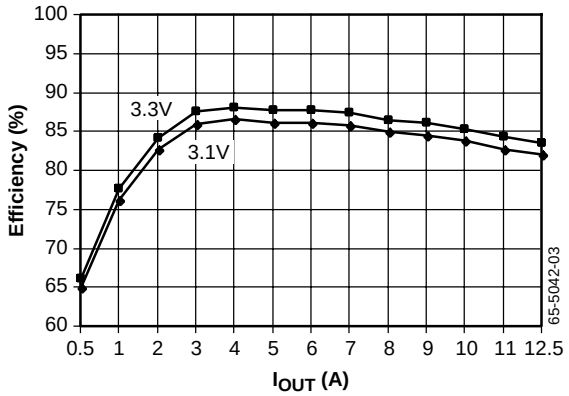
Notes:

1. 0 Indicates Processor pin is tied to V_{SS}. 1 = Open.
2. Setpoint Accuracy includes Output Ripple/Noise.
3. Cumulative Accuracy includes Setpoint Accuracy, Line & Load Regulation, Transient Effects and Temperature Drift.

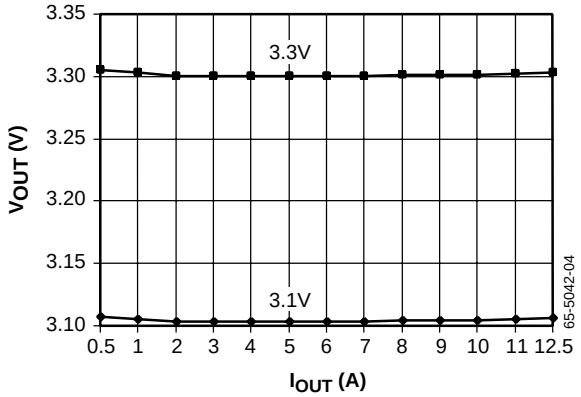
Typical Operating Characteristics

(VCCA, VCCD = 5V, f_{OSC} = 650 kHz and T_A = +25˚C using circuit in Figure 1, unless otherwise noted)

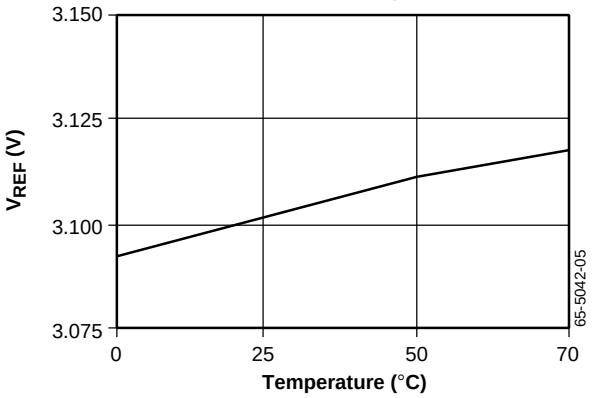
Efficiency vs. Output Current, 650 KHz



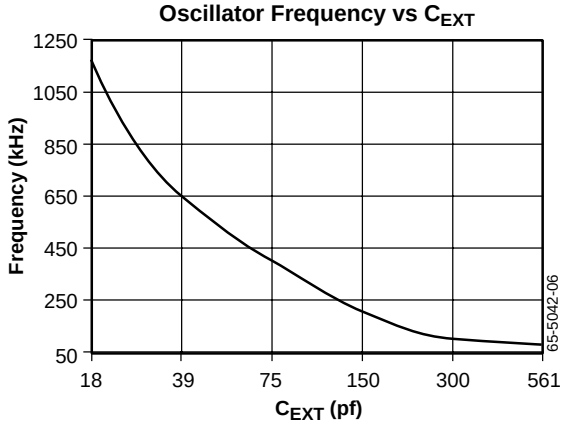
Load Regulation, 650 KHz



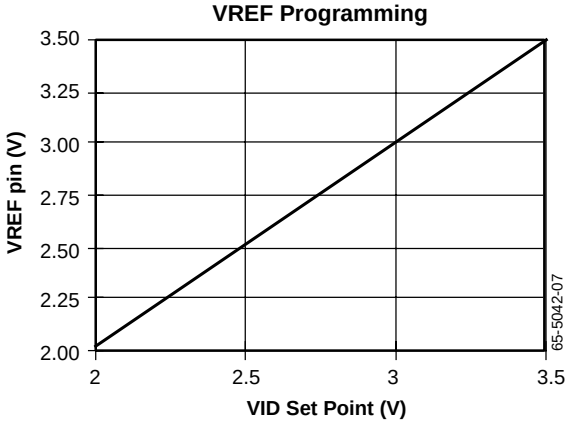
Reference Tempco



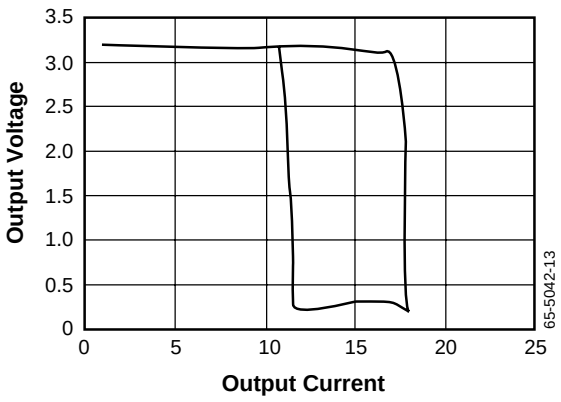
Oscillator Frequency vs C_{EXT}



VREF Programming

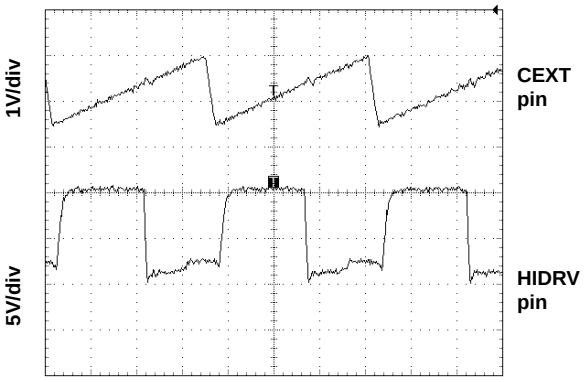


Output Voltage vs. Output Current, R_{SENSE} = 6mΩ



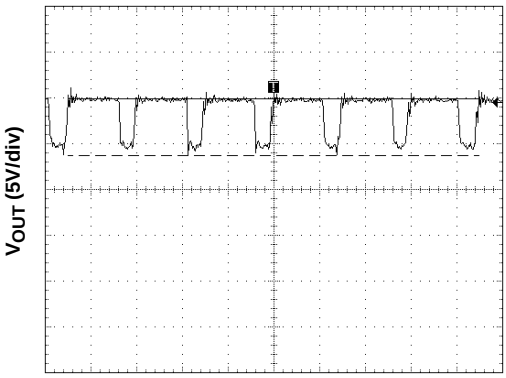
Typical Operating Characteristics (continued)

Switching Waveforms, 12.5A Load



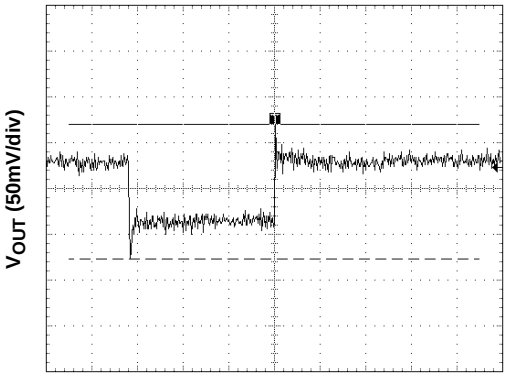
Time (500ns/division)

FET Driver Supply, VCCQP (I_{LOAD} = 12.5A using charge pump)



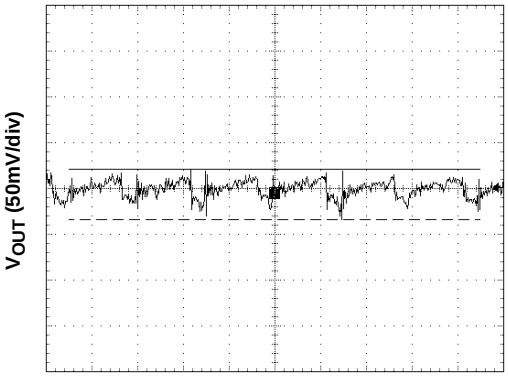
Time (1μs/division)

Transient Response, 0.5A to 12.5A Step



Time (200ns/division)

AC Ripple Response, 12.5A Load



Time (1μs/division)

65-5042-08

Test Circuits

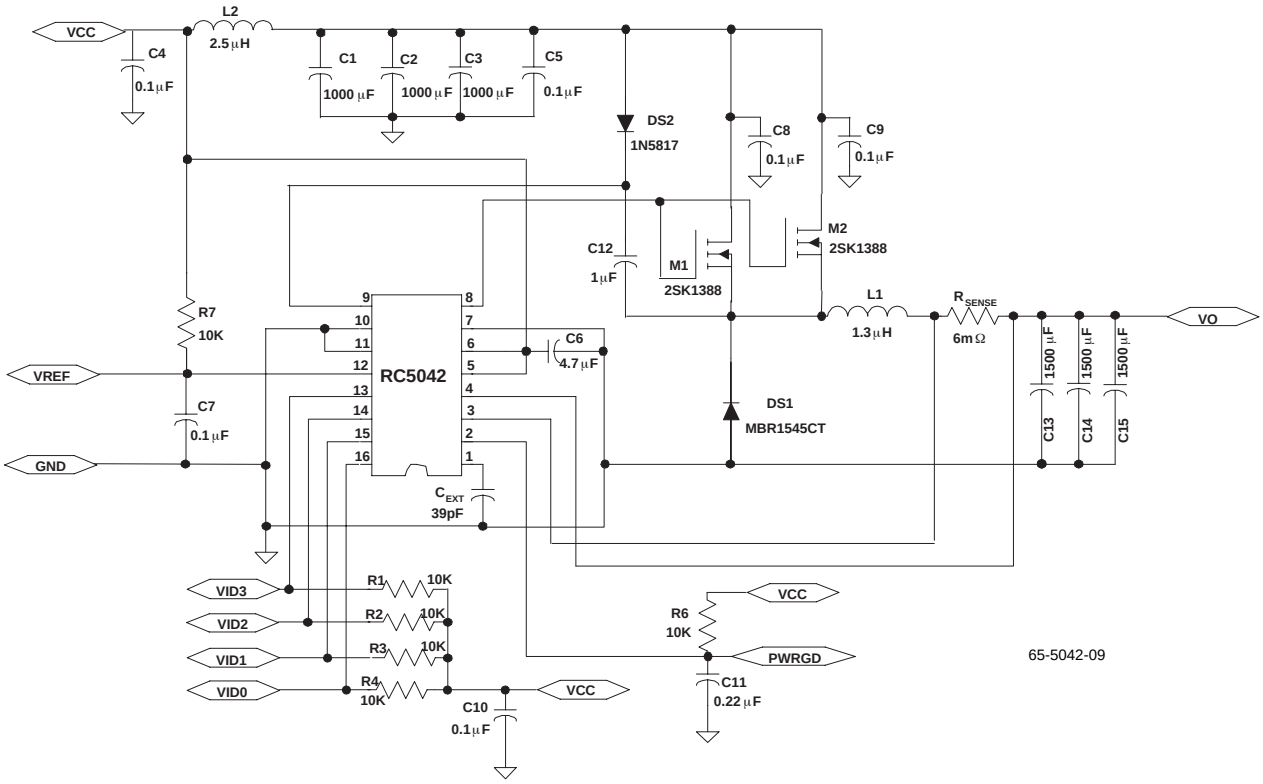


Figure 1. Standard Test or Application Schematic

Table 2. RC5042 Bill of Materials

Reference	Part Number	Description	Relevant Specification
C4, C5, C7–C10	Panasonic ECU-V1H104ZFX	0.1µF 50V capacitor	
C6	Panasonic ECSH1CY475R	4.7µF 16V capacitor	
C_{EXT}	Panasonic ECU-V1H121JCG	39pF capacitor	
C12	Panasonic ECSH1CY105R	1µF 16V capacitor	
C1, C2, C3	Sanyo 6MV1000GX	1000µF 6.3V electrolytic capacitor	
C11	Panasonic ECU-V1H224ZFX	0.22µF 50V capacitor	
C13, C14, C15	Sanyo 6MV1500GX	1500µF 6.3 electrolytic capacitor	ESR < 0.047 Ω
DS1	Motorola MBR1545CT	Schottky Diode	Vf < 0.72V @ If = 15A
DS2	General Instruments 1N5817	Schottky Diode	
L1	Skynet 320-8107	1.3µH inductor	
L2[1]	Skynet 320-6110	2.5µH inductor	
M1, M2	Fuji 2SK1388	N-Channel Logic Level Enhancement Mode MOSFET	$R_{DS(ON)}$ < 37mΩ V_{GS} < 4V, I_D > 20A
R_{SENSE}	Copel AWG #18	6 mΩ CuNi Alloy Wire Resistor	
R1–R4, R6, R7	Panasonic ERJ-6ENF10.0KV	10K 5% Resistors	

Note:

1. The inductor L2 is recommended to isolate the 5V input supply from current surges caused by MOSFET switching. L2 is not required for normal operation and may be omitted if desired.

Application Information

Simple Step-Down Converter

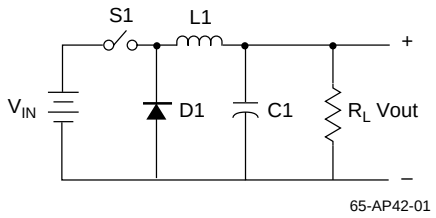


Figure 2. Simple Buck DC-DC Converter

Figure 2 illustrates a step-down DC-DC converter with no feedback control. The derivation of the basic step-down converter will serve as a basis for the design equations for the RC5042. Referring to Figure 1, the basic operation begins by closing the switch S1. When S1 is closed, the input voltage V_{IN} is impressed across inductor L1. The current flowing in this inductor is given by the following equation:

$$I_L = \frac{(V_{IN} - V_{OUT})T_{ON}}{L1}$$

Where T_{ON} is the duty cycle (the time when S1 is closed).

When S1 opens, the diode D1 will conduct the inductor current and the output current will be delivered to the load according to the equation:

$$I_L = \frac{V_{OUT}(T_S - T_{ON})}{L1}$$

Where T_S is the overall switching period, and (T_S – T_{ON}) is the time during which S1 is open.

By solving these two equations, we can arrive at the basic relationship for the output voltage of a step-down converter:

$$V_{OUT} = V_{IN}\left(\frac{T_{ON}}{T_S}\right)$$

In order to obtain a more accurate approximation for V_{OUT}, we must also include the forward voltage V_D across diode D1 and the switching loss, Vsw. After taking into account these factors, the new relationship becomes:

$$V_{OUT} = (V_{IN} + V_D - V_{SW})\frac{T_{ON}}{T_S} - V_D$$

Overview

The RC5042 is a programmable DC-DC controller IC. When designed around the appropriate external components, the RC5042 can be configured to deliver more than 14.5A of output current. During heavy loading conditions, the RC5042 functions as a current-mode PWM step-down regulator. Under light loads, the regulator functions in the PFM (pulse frequency modulation), or pulse skipping mode. The controller will sense the load level and switch between the two operating modes automatically, thus optimizing its efficiency under all loading conditions.

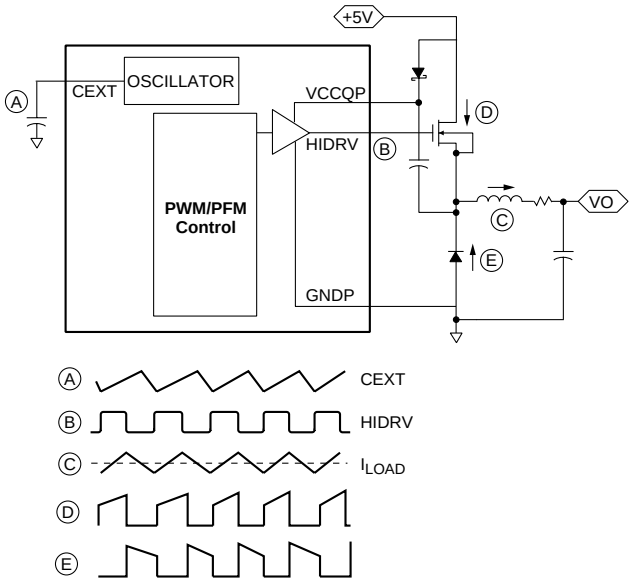


Figure 3. Typical Switching Waveforms

Main Control Loop

Refer to the Block Diagram on page 1. The control loop of the regulator contains two main sections, the analog control block and the digital control block. The analog block consists of signal conditioning amplifiers feeding into a set of comparators which provide the inputs to the digital block. The signal conditioning section accepts inputs from the IFB (current feedback) and VFB (voltage feedback) pins and sets up two controlling signal paths. The voltage control path amplifies the VFB signal and presents the output to one of the summing amplifier inputs. The current control path takes the difference between the IFB and VFB pins and presents the resulting signal to another input of the summing amplifier. These two signals are then summed together with the slope compensation input from the oscillator. This output is then presented to a comparator, which provides the main PWM control signal to the digital control block.

The additional comparators in the analog control section set the thresholds of where the RC5042 enters its pulse skipping mode during light loads as well as the point at which the maximum current comparator disables the output drive signals to the external power MOSFETs.

The digital control block is designed to take the comparator inputs along with the main clock signal from the oscillator and provide the appropriate pulses to the HIDRV output pin that controls the external power MOSFET. The digital section was designed utilizing high speed Schottky transistor logic, thus allowing the RC5042 to operate at clock speeds as high as 1MHz.

High Current Output Drivers

The RC5042 contains two identical high current output drivers which utilize high speed bipolar transistors arranged in a push-pull configuration. Each driver is capable of delivering 1A of current in less than 100ns. Each driver's power and ground are separated from the overall chip power and ground for additional switching noise immunity. The HIDRV driver has a power supply, VCCQP, which is boot-strapped from a flying capacitor as illustrated in Figure 2. Using this configuration, C12 is alternately charged from VCC via the Schottky diode DS2 and then boosted up when the FET is turned on. This scheme provides a VCCQP voltage equal to 2•VCC – VDS(DS2), or approximately 9.5V with VCC = 5V. This voltage is sufficient to provide the 9V gate drive to the external MOSFET required in order to achieve a low $R_{DS(ON)}$. Since the low side synchronous FET is referenced to ground (refer to Figure 3), there is no need to boost the gate drive voltage and its VCCP power pin can be tied to VCC. See Typical Operating Characteristics for typical full load VCCQP waveform.

Internal Voltage Reference

The reference included in the RC5042 is a 1.24V precision band-gap voltage reference. The internal resistors are precisely trimmed to provide a near zero temperature coefficient (TC). Added to the reference input is the resulting output from an integrated 4-bit DAC. The DAC is provided in accordance with the Pentium Pro specification guideline, which requires the DC-DC converter output to be directly programmable via a 4-bit voltage identification (VID) code. This code will scale the reference voltage from 2.0V (no CPU) to 3.5V in 100mV increments. For guaranteed stable operation under all loading conditions, a 10KΩ pull-up resistor and 0.1μF of decoupling capacitance should be connected to the VREF pin.

Power Good

The RC5042 Power Good function is designed in accordance with the Pentium Pro DC-DC converter specification and provides a constant voltage monitor on the VFB pin. The circuit compares the VFB signal to the VREF voltage and outputs an active-low interrupt signal to the CPU should the power supply voltage exceed ±7% of its nominal setpoint. The Power Good flag provides no other control function to the RC5042.

Upgrade Present (UP#)

Intel’s specifications state that the DC-DC converter must accept an open collector signal, used to indicate the presence of an upgrade processor. The typical state is high (standard CPU). When in the low or ground state (OverDrive processor present), the output voltage must be disabled unless the converter can supply the OverDrive processor’s specifications. When disabled, the PWRGD output must be in the low state. Since the RC5042 can supply the OverDrive processor specifications, the UP# signal is not required.

Over-Voltage Protection

The RC5042 provides a constant monitor of the output voltage for protection against overvoltage conditions. If the voltage at the VFB pin exceeds 20% of the selected program voltage, an overvoltage condition will be assumed, and the RC5042 will disable the output drive signal to the MOSFET(s).

Short Circuit Protection

A current sense methodology is implemented to disable the output drive signal to the MOSFET(s) when an over-current condition is detected. The voltage drop created by the output current flowing across a sense resistor is presented to an internal comparator. When voltage developed across the sense resistor exceeds the comparator threshold voltage, the RC5042 will disable the output drive signal to the MOSFET(s).

The DC-DC converter returns to normal operation after the fault has been removed, for either an overvoltage or a short circuit condition.

Oscillator

The RC5042 oscillator section is implemented using a fixed current capacitor charging configuration. An external capacitor (CEXT) is used to preset the oscillator frequency between 200KHz and 1MHz. This scheme allows maximum flexibility in setting the switching frequency as well as choosing external components.

In general, a lower operating frequency will increase the peak ripple current flowing in the output inductor, and thus require the use of a larger inductor value. Operation at lower frequencies also increases the amount of energy storage that must be provided by the bulk output capacitors during load transients due to the slower loop response of the controller.

As the operating frequency is increased, the user should note that the efficiency losses due to switching are relatively fixed per switching cycle. Therefore, as the switching frequency is increased, so is the contribution toward efficiency due to switching losses.

Careful analysis of the RC5042 DC-DC controller has resulted in an optimal operating frequency of 650KHz, which allows the use of smaller inductive and capacitive components while maximizing peak efficiency under all operating conditions.

Design Considerations and Component Selection

MOSFET Selection

This application requires N-channel *Logic Level* Enhancement Mode Field Effect Transistors. Desired characteristics are as follows:

- Low Static Drain-Source On-Resistance, $R_{DS(on)}$ < 37 mΩ (lower is better)
- Low gate drive voltage, V_{GS} < 4V
- Power package with low thermal resistance
- Drain current rating of 20A minimum
- Drain-Source voltage > 15V.

The on-resistance ($R_{DS(ON)}$) is the primary parameter for MOSFET selection. The on-resistance determines the power dissipation of the MOSFET and therefore significantly affects the efficiency of the DC-DC Converter. Table 5 presents a list of suitable MOSFETs for this application.

Table 5. MOSFET Selection Table

Manufacturer & Model #	Conditions[1]		$R_{DS,ON}$(mΩ) Typ.	$R_{DS,ON}$(mΩ) Max.	Package	Thermal Resistance
Fuji 2SK1388	V_{GS} = 4V, I_D = 17.5A	T_J = 25°C	25	37	TO-220	Φ_{JA} = 75
		T_J = 125°C	37	—		
Siliconix SI4410DY	V_{GS} = 4.5V, I_D = 5A	T_J = 25°C	16.5	20	SO-8 (SMD)	Φ_{JA} = 50
		T_J = 125°C	28	34		
National Semiconductor NDP706AL	V_{GS} = 5V, I_D = 40A	T_J = 25°C	13	15	TO-220	Φ_{JA} = 62.5 Φ_{JC} = 1.5
NDP706AEL		T_J = 125°C	20	24		
National Semiconductor NDP603AL	V_{GS} = 4.5V, I_D = 10A	T_J = 25°C	31	40	TO-220	Φ_{JA} = 62.5
		T_J = 125°C	42	54		Φ_{JC} = 2.5
National Semiconductor NDP606AL	V_{GS} = 5V, I_D = 24A	T_J = 25°C	22	25	TO-220	Φ_{JA} = 62.5
		T_J = 125°C	33	40		Φ_{JC} = 1.5
Motorola MTB75N03HDL	V_{GS} = 5V, I_D = 37.5A	T_J = 25°C	6	9	TO-263	Φ_{JA} = 62.5
		T_J = 125°C	9.3	14	(D_2 PAK)	Φ_{JC} = 1.0
Int. Rectifier IRLZ44	V_{GS} = 5V, I_D = 31A	T_J = 25°C	—	28	TO-220	Φ_{JA} = 62.5
		T_J = 125°C	—	46		Φ_{JC} = 1.0
Int. Rectifier IRL3103S	V_{GS} = 4.5V, I_D = 28A	T_J = 25°C	—	19	TO-220	Φ_{JA} = 62.5
		T_J = 125°C		31		Φ_{JC} = 1.0

Note:

1. $R_{DS(ON)}$ values at T_J=125°C for most devices were extrapolated from the typical operating curves supplied by the manufacturers and are approximations only. Only National Semiconductor offers maximum values at T_J = 125°C.

Two MOSFETs in Parallel

We recommend that two MOSFETs be used in parallel instead of one single MOSFET. Significant advantages are realized using two MOSFETs in parallel:

- **Significant reduction of power dissipation**.

  Maximum current of 14A with one MOSFET:

  $P_{MOSFET} = (I^2 R_{DS(ON)})(\text{Duty Cycle})$
  $= (14)^2(0.050*)(3.3+0.4)/(5+0.4-0.35) = 7.2\ W$

  With two MOSFETs in parallel:

  $P_{MOSFET} = (I^2 R_{DS(ON)})(\text{Duty Cycle})$
  $= (14/2)^2(0.037*)(3.3+0.4)/(5+0.4-0.35) = 1.3W/FET$

  *Note: $R_{DS(on)}$ increases with temperature. Assume $R_{DS(on)} = 0.025$ at 25°C. $R_{DS(on)}$ can easily increase to 0.050W at high temperature when using a single MOSFET. When using two MOSFETs in parallel, the temperature effects should not cause the $R_{DS(on)}$ to rise above the listed maximum value of 37mW.

- **Less heat sink required.** With power dissipation down to around one watt and with MOSFETs mounted flat on the motherboard, there will be considerably less heat sink required. The junction-to-case thermal resistance for the MOSFET package (TO-220) is typically at 2°C/W and the motherboard serves as an excellent heat sink.
- **Higher current capability.** With thermal management under control, this on-board DC-DC converter is able to deliver load currents up to 14.5A with no problem at all.

MOSFET Gate Bias

The MOSFET can be biased by one of two methods—Charge Pump or 12V Gate Bias.

Charge pump (or Bootstrap) method

Figure 4 employs a charge pump to provide gate bias. Capacitor CP is the charge pump deployed to boost the voltage of the RC5042 output driver. When the MOSFET switches off, the source of the MOSFET is at -0.6V. VCCQP is charged through the Schottky diode to 4.5V. Thus, the capacitor CP is charged to 5V. When the MOSFET turns on, the source of the MOSFET voltage is equal to 5V. The capacitor voltage follows, and hence provides a voltage at VCCQP equal to 10V. The Schottky is required to provide the charge path when the MOSFET is off. The Schottky reverses bias when the VCCQP goes to 10V. The charge pump capacitor, CP, needs to be a high Q and high frequency capacitor. A 1µF ceramic capacitor is recommended here.

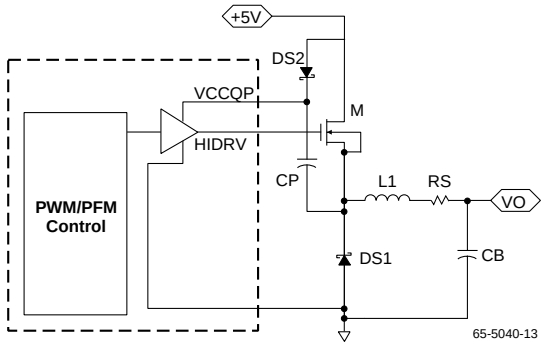


Figure 4. Charge Pump Configuration

Method 2. 12V Gate Bias

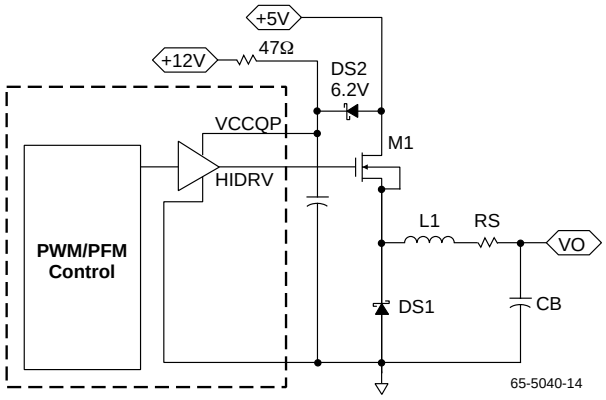


Figure 5. 12V Gate Bias Configuration

Figure 6 uses an external 12V source to bias VCCQP. A 47 Ω resistor is used to limit the transient current into the VCCQP pin. A 1µF capacitor filter is used to filter the VCCQP supply. This method provides a higher gate bias voltage to the MOSFET, and therefore reduces the $R_{SD(ON)}$ and resulting power loss within the MOSFET. Figure 7 illustrates how $R_{DS(ON)}$ decreases dramatically as V_{GS} increases. A 6.2V Zener (DS2) is used to clamp the voltage at V_{CCQP} to a maximum of 12V and ensure that the absolute maximum voltage of the IC will not be exceeded.

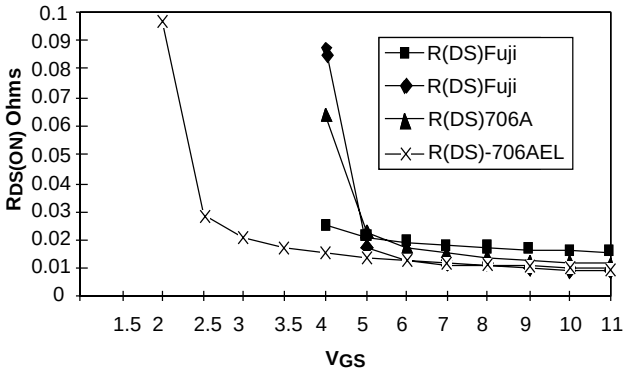


Figure 6. R(DS) vs. V_{GS} for Selected MOSFETs

Converter Efficiency

Losses due to parasitic resistance in the switches, coil, and sense resistor dominate at high load-current level. The major loss mechanisms under heavy loads, in usual order of importance, are:

- MOSFET I^2R Losses
- Inductor Coil Losses
- Sense Resistor Losses
- gate-charge losses
- diode-conduction losses
- transition losses
- Input Capacitor losses
- losses due to the operating supply current of the IC

Efficiency of the converter under heavy loads can be calculated as follows:

$$\text{Efficiency} = \frac{P_{OUT}}{p_{IN}} = \frac{I_{OUT} \times V_{OUT}}{I_{OUT} \times V_{OUT} + P_{LOSS}},$$

where $P_{LOSS} = PD_{MOSFET} + PD_{INDUCTOR} + PD_{RSENSE} + PD_{GATE} + PD_{DIODE} + PD_{TRAN} + PD_{CAP} + PD_{IC}$

Design Equations:

(1) $PD_{MOSFET} = I_{OUT}^2 \times R_{DS(ON)} \times \text{DutyCycle}$

where $\text{DutyCycle} = \frac{V_{OUT} + V_D}{V_{IN} + V_D - V_{SW}}$

(2) $PD_{INDUCTOR} = I_{OUT}^2 \times R_{INDUCTOR}$

(3) $PD_{RSENSE} = I_{OUT}^2 \times R_{SENSE}$

(4) $PD_{GATE} = q_{GATE} \times f \times 5V$, where q_{GATE} is the gate charge and f is the switching frequency

(5) $PD_{DIODE} = V_f \times I_{OUT}(1 - \text{Dutycycle})$

(6) $PD_{TRAN} = \frac{V_{IN}^2 \times C_{RSS} \times I_{LOAD} \times f}{I_{DRIVE}}$, where C_{RSS} is the reverse transfer capacitance of the high-side MOSFET.

(7) $PD_{CAP} = I_{RMS}^2 \times ESR$

(8) $PD_{IC} = V_{CC} \times I_{CC}$

Example:

$\text{DutyCycle} = \frac{3.3 + 0.5}{5 + 0.5 - 0.3} = 0.73$

$PD_{MOSFET} = 10^2 \times 0.030 \times 0.73 = 2.19W$

$PD_{INDUCTOR} = 10^2 \times 0.010 = 1W$

$PD_{RSENSE} = 10^2 \times 0.0065 = 0.65W$

$PD_{GATE} = CV \times f \times 5V = 1.75nf \times (9 - 1)V \times 650Khz \times 5V = 0.045W$

$PD_{DIODE} = 0.5 \times 10(1 - 0.73) = 1.35W$

$PD_{TRAN} = \frac{5^2 \times 400pf \times 10 \times 650khz}{0.7A} \sim 0.010W$

$PD_{CAP} = (7.5 - 2.5)^2 \times 0.015 = 0.37W$

$PD_{IC} = 0.2W$

PD_{LOSS} = 2.19W + 1.0W + 0.65W + 0.045W + 1.35W + 0.010W + 0.37W + 0.2W = 5.815W

$\therefore$ Efficiency = $\frac{3.3 \times 10}{3.3 \times 10 + 5.815} \sim 85\%$

Selecting the Inductor

The inductor is one of the most critical components to be selected in the DC-DC converter application.. The critical parameters are inductance (L), maximum DC current (Io) and the coil resistance (R1). The inductor core material is a crucial factor in determining the amount of current the inductor will be able to withstand. As with all engineering designs, tradeoffs exist between various types of core materials. In general, Ferrites are popular due to their low cost, low EMI properties and high frequency (>500KHz) characteristics. Molypermalloy powder (MPP) materials exhibit good saturation characteristics, low EMI and low hysteresis losses; however, they tend to be expensive and more effectively utilized at operating frequencies below 400KHz. Another critical parameter is the DC winding resistance of the inductor. This value should typically be reduced as much as possible, as the power loss in the DC resistance will degrade the efficiency of the converter by the relationship: $P_{LOSS} = I_O^2$ x R1. The value of the inductor is a function of the oscillator duty cycle (T_{ON}) and the maximum inductor current (I_{PK}). I_{PK} can be calculated from the relationship:

$$I_{PK} = I_{MIN} + \left(\frac{V_{IN} - V_{SW} - V_D}{L}\right) T_{ON}$$

Where T_{ON} is the maximum duty cycle and V_D is the forward voltage of diode DS1.

Then the inductor value can be calculated using the relationship:

$$L = \left(\frac{V_{IN} - V_{SW} - V_O}{I_{PK} - I_{MIN}}\right) T_{ON}$$

Where V_{SW} (R_{DSON} x I_O) is the drain-to-source voltage of M1 when it is switched on.

Implementing Short Circuit Protection

Intel currently requires all power supply manufacturers to provide continuous protection against short circuit conditions that may damage the CPU. To address this requirement, Fairchild Semiconductor has implemented a current sense methodology to disable the output drive signal to the MOSFET(s) when an over current condition is detected. The voltage drop created by the output current flowing across a sense resistor is presented to one terminal of an internal comparator with hysterisis. The other comparator terminal has the threshold voltage, nominally of 120mV. Table 6 states the limits for the comparator threshold of the Switching Regulator:

Table 6. RC5042 Short Circuit Comparator Threshold Voltage

	Short Circuit Comparator $V_{threshold}$ (mV)
Typical	120
Minimum	100
Maximum	140

When designing the external current sense circuitry, the designer must pay careful attention to the output limitations during normal operation and during a fault condition. If the short circuit protection threshold current is set too low, the DC-DC converter may not be able to continuously deliver the maximum CPU load current. If the threshold level is too high, the output driver may not be disabled at a safe limit and the resulting power dissipation within the MOSFET(s) may rise to destructive levels.

The design equation used to set the short circuit threshold limit is as follows:

$R_{SENSE} = \frac{V_{th}}{I_{SC}}$, where: I_{SC} = Output short circuit current

$$I_{SC} \geq I_{inductor} = I_{Load,\ max} + \frac{(I_{PK} - I_{min})}{2}$$

Where I_{pk} and I_{min} are peak ripple current and $I_{load,\ max}$ = maximum output load current.

The designer must also take into account the current ($I_{PK} - I_{min}$), or the ripple current flowing through the inductor under normal operation. Figure 7 illustrates the inductor current waveform for the RC5042/42 DC-DC converter at maximum load.

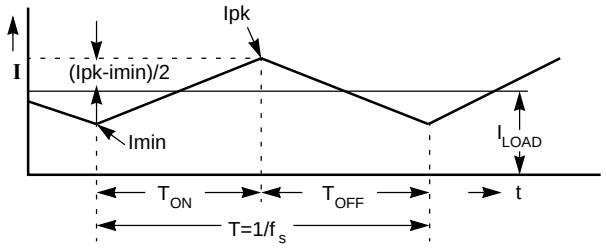


Figure 7. Typical DC-DC Converter Inductor Current Waveform

The calculation of this ripple current is as follows:

$$\frac{(I_{pk} - I_{min})}{2} = \frac{(V_{IN} - V_{SW} - V_{OUT})}{L} \times \frac{(V_{OUT} + V_D)}{(V_{IN} - V_{SW} + V_D)} T$$

where:
- V_{in} = input voltage to Converter
- V_{SW} = voltage across Switcher (MOSFET) = I_{LOAD} x $R_{DS(ON)}$
- V_D = Forward Voltage of the Schottky diode
- T = the switching period of the converter = 1/fs, where f_S = switching frequency.

For an input voltage of 5V, an output voltage of 3.3V, an inductor value of 1.3µH and a switching frequency of 650KHz (using C_{EXT}=39pF), the inductor current can be calculated as follows:

$$\frac{(I_{pk} - I_{min})}{2} = \frac{(5.0 - 14.5 \times 0.037 - 3.3)}{1.3 \times 10^{-6}} \times$$

$$\frac{(3.3 + 0.5)}{(5.0 - 14.5 \times 0.037 + 0.5)} \times \frac{1}{650 \times 10^{3}} = 1.048\text{A}$$

Therefore, the peak current, I_{PK}, through the inductor for a 14.5A load is found to be:

$$I_{SC} \geq I_{inductor} = I_{Load,\,max} + \frac{(I_{PK} - I_{min})}{2} = 14.5 + 1 = 15.5\text{A}$$

As a result, the short circuit detection threshold must be at least 15.5A.

The next step is to determine the value of the sense resistor. Including sense resistor tolerance, the sense resistor value can be approximated as follows:

$$R_{SENSE} = \frac{V_{th,min}}{I_{SC}} \times (1 - TF) = \frac{V_{th,min}}{1.0 + I_{Load,max}} \times (1 - TF)$$

Where TF = Tolerance Factor for the sense resistor.

There are several different type of sense resistors. Table 7 describes tolerance, size, power capability, temperature coefficient and cost of various type of sense resistors:

Table 7. Comparison of Sense Resistors[1]

Description	Motherboard Trace Resistor	Discrete Iron Alloy resistor (IRC)	Discrete Metal Strip surface mount resistor (Dale)	Discrete MnCu Alloy wire resistor	Discrete CuNi Alloy wire resistor (Copel)
Tolerance Factor (TF)	±29%	±5% (±1% available)	±1%	±10%	±10%
Size (L x W x H)	2" x 0.2" x 0.001" (1 oz Cu trace)	0.45" x 0.065" x 0.200"	0.25" x 0.125" x 0.025"	0.200" x 0.04" x 0.160"	0.200" x 0.04" x 0.100"
Power capability	>50A/in	1 watt (3W and 5W available)	1 watt	1 watt	1 watt
Temperature Coefficient	+4,000 ppm	+30 ppm	±75 ppm	±30 ppm	±20 ppm
Cost @10,000 piece	Low included in motherboard	$0.31	$0.47	$0.09	$0.09

Notes:
1. Refer to Appendix A for Directory of component suppliers

Based on the Tolerance in the above table,

For Embedded PC Trace Resistor and for $I_{load,max}$ = 14.5A**:**

$$R_{SENSE} = \frac{V_{th,min}}{1.0\text{A} + I_{Load,\,max}} \times (1 - TF)$$

$$= \frac{100\text{mV}}{1.0\text{A} + 14.5\text{A}} \times (1 - 29\%) = 4.6\text{m}\Omega$$

For discrete resistor and $I_{load,\,max}$ = 14.5A**:**

$$R_{SENSE} = \frac{V_{th,min}}{1.0\text{A} + I_{Load,\,max}} \times (1 - TF)$$

$$= \frac{100\text{mV}}{1.0\text{A} + 14.5\text{A}} \times (1 - 5\%) = 6.1\text{m}\Omega$$

For user convenience, Table 8 lists recommended value for sense resistor for various load current using embedded PC trace resistor or discrete resistor.

Table 8. R_{sense} for Various Load Current

$I_{Load,max}$ (A)	R_{SENSE} PC Trace Resistor (mΩ)	R_{SENSE} Discrete Resistor (mΩ)
10.00	6.5	8.6
11.20	5.8	7.8
12.40	5.3	7.1
13.90	4.8	6.4
14.00	4.7	6.3
14.50	4.6	6.1

RC5042 Short Circuit Current Characteristics

The RC5042 has a short circuit current characteristic that includes a hysteresis function that prevents the DC-DC converter from oscillating in the event of a short circuit. A typical V-I characteristic of the DC-DC converter output is presented in the Typical Operating Characteristics section, page 5. The converter performs with a normal load regulation characteristic until the voltage across the resistor reaches the internal short circuit threshold of 120mV. At this point, the internal comparator trips and sends a signal to the controller to turn off the gate drive to the power MOSFET. This causes a drastic reduction in the output voltage as the load regulation collapses into the short circuit mode of control. The output voltage will not return to the normal load characteristic until the output short circuit current is reduced to within the safe range for the DC-DC converter.

Schottky Diode Selection

The application circuit diagram of Figure 1 shows two Schottky diodes, DS1 and DS2. In synchronous mode, DS1 is used in parallel with M3 to prevent the lossy diode in the FET from turning on. DS2 serves a dual purpose. As configured, it allows the VCCQP supply pin of the RC5042 to be bootstrapped up to 9V using capacitor C12. When the lower MOSFET M3 is turned on, one side of capacitor C12 is connected to ground while the other side of the capacitor is being charged up to voltage VIN – VD through DS2. The voltage that is then applied to the gate of the MOSFET is VCCQP – VSAT, or typically around 9V. A vital selection criteria for DS1 and DS2 is that they exhibit a very low forward voltage drop, as this parameter can directly affect the regulator efficiency. In non-synchronous mode, DS1 is used as a flyback diode to provide a constant current path for the inductor when M1 is turned off. Table 9 lists several suitable Schottky diodes. Note that the MBR2015CTL has a very low forward voltage drop. This diode is most ideal for application where output voltage is required to be less than 2.8V.

Table 9. Schottky Diode Selection Table

Manufacturer Model #	Conditions	Forward Voltage V_F
Philips PBYR1035	I_F = 20A; T_j = 25°C I_F = 20A; T_j = 125°C	< 0.84V < 0.72V
Motorola MBR2035CT	I_F = 20A; T_j = 25°C I_F = 20A; T_j = 125°C	< 0.84V < 0.72V
Motorola MBR1545CT	I_F = 15A; T_j = 25°C I_F = 15A; T_j = 125°C	< 0.84V < 0.72V
Motorola MBR2015CTL	I_F = 20A; T_j = 25°C I_F = 20A; T_j = 150°C	< 0.58V < 0.48V

Output Filter Capacitors

Optimal ripple performance and transient response are functions of the filter capacitors used. Since the 5V supply of a PC motherboard may be located several inches away from the DC-DC converter, input capacitance can play an important role in the load transient response of the RC5042.

The higher the input capacitance, the more charge storage is available for improving the current transfer through the FET. Low “ESR” capacitors are best suited for this type of application and can influence the converter's efficiency if not chosen carefully. The input capacitor should be placed as close to the drain of the FET as possible to reduce the effect of ringing caused by long trace lengths.

The ESR rating of a capacitor is a difficult number to quantify. ESR or Equivalent Series Resistance, is defined as the resonant impedance of the capacitor. Since the capacitor is actually a complex impedance device having resistance, inductance and capacitance, it is quite natural for this device to have a resonant frequency. As a rule, the lower the ESR, the better suited the capacitor is for use in switching power supply applications. Many capacitor manufacturers do not supply ESR data. A useful estimate of the ESR can be obtained using the following equation:

$$ESR = \frac{DF}{2\pi fC}$$

Where:
- DF is the dissipation factor of the capacitor
- f is the operating frequency
- C is the capacitance in farads

With this in mind, correct calculation of the output capacitance is crucial to the performance of the DC-DC converter. The output capacitor determines the overall loop stability, output voltage ripple and load transient response. The calculation is as follows:

$$C(\mu F) = \frac{I_O \times \Delta T}{\Delta V - I_O \times ESR}$$

Where ΔV is the maximum voltage deviation due load transient

ΔT is reaction time of the power source (Loop response time of the RC5042) and it is approximately 8μs

I_O is the output load current

For I_O = 10A, and ΔV = 75mV, the bulk capacitor required can be approximated as follows:

$$C(\mu F) = \frac{I_O \times \Delta T}{\Delta V - I_O \times ESR} = \frac{10A \times 8\mu s}{75mV - 10A \times 5m\Omega} = 3200\mu F$$

Input filter

We recommend that the design include an input inductor between the system +5V supply and the DC-DC converter input described below. This inductor will serve to isolate the +5V supply from noise occurring in the switching portion of the DC-DC converter and to also limit the inrush current into the input capacitors on power up. We recommend a value of around 2.5μH.

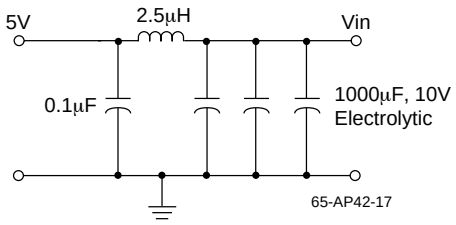


Figure 8. Input Filter

PCB Layout Guidelines and Considerations

PCB Layout Guidelines

1. Placement of the MOSFETs relative to the RC5042 is critical. The MOSFETs (M1 & M2), should be placed such that the trace length of the HIDRV pin from the RC5042 to the FET gates is minimized. A long lead length on this pin will cause high amounts of ringing due to the inductance of the trace combined with the large gate capacitance of the FET. This noise will radiate all over the board, and because it is switching at such a high voltage and frequency, it will be very difficult to suppress.

   The drawing below depicts an example of good placement for the MOSFETs in relation to the RC5042 and also an example of problematic placement for the MOSFETs.

   In general, all of the noisy switching lines should be kept away from the quiet analog section of the RC5042. That is to say, traces that connect to pins 8 and 9 (HIDRV and VCCQP) should be kept far away from the traces that connect to pins 1 through 4, and pin 12.

2. Place decoupling capacitors (.1µF) as close to the RC5042 pins as possible. Extra lead length on these will negate their ability to suppress noise.

3. Each VCC and GND pin should have its own via down to the appropriate plane underneath. This will help give isolation between pins.

4. Surround the CEXT timing capacitor with a ground trace as much as possible. Also be sure to keep a ground or power plane underneath the capacitor for further noise isolation. This will help to shield the oscillator pin 1 from the noise on the PCB. Place this capacitor as close to the RC5042 pin 1 as possible.

5. Place MOSFETs, inductor and Schottky as close together as possible for the same reasons as #1 above. Place the input bulk capacitors as close to the drains of MOSFETs as possible. In addition, placement of a 0.1µF decoupling cap right on the drain of each MOSFET will help to suppress some of the high frequency switching noise on the input of the DC-DC converter.

6. The traces that run from the RC5042 IFB (pin 3) and VFB (pin 4) pins should be run together next to each other and be Kelvin connected to the sense resistor. Running these lines together will help in rejecting some of the common noise that is presented to the RC5042 feed-

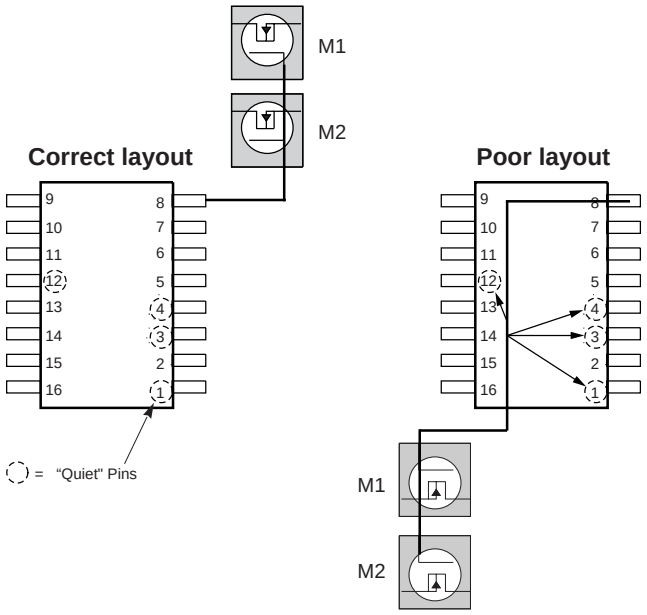
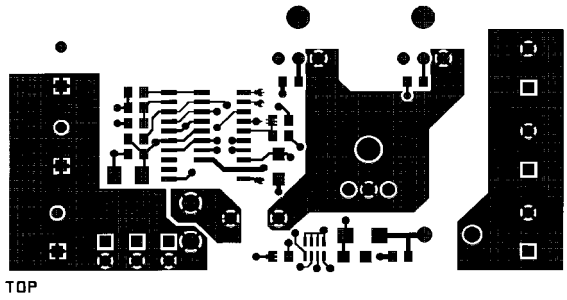


Figure 9. MOSFET Layout Guidelines

back input. Try as much as possible to run the noisy switching signals (HIDRV & VCCQP) on one layer; and use the inner layers for only power and ground. If the top layer is being used to route all of the noisy switching signals, use the bottom layer to route the analog sensing signals VFB and IFB.

Example of a Layout on a PC Motherboard and Gerber File

A reference design for motherboard implementation of the RC5042 along with Layout Gerber File and Silk Screen are presented here. The actual Gerber File can be obtained from a Fairchild Semiconductor local Sales Rep Office or from Fairchild Semiconductor Marketing Department at (415) 966-7819.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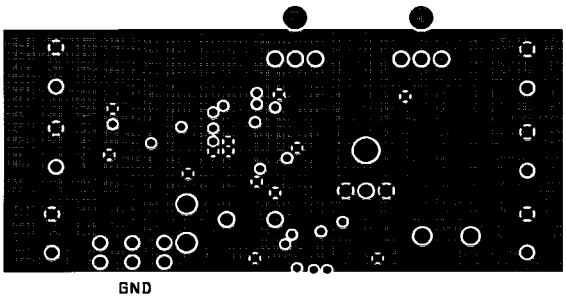
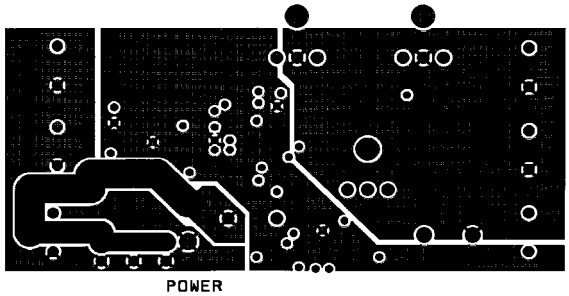
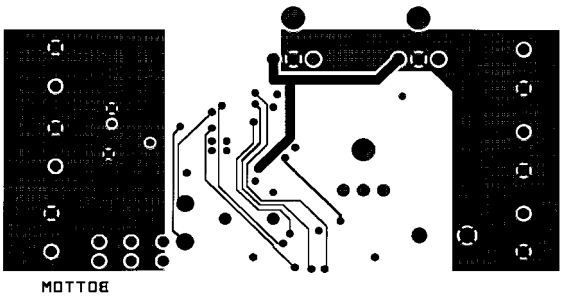
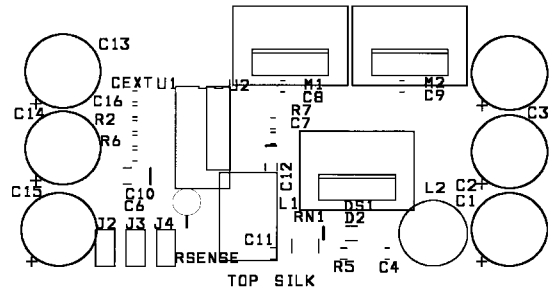
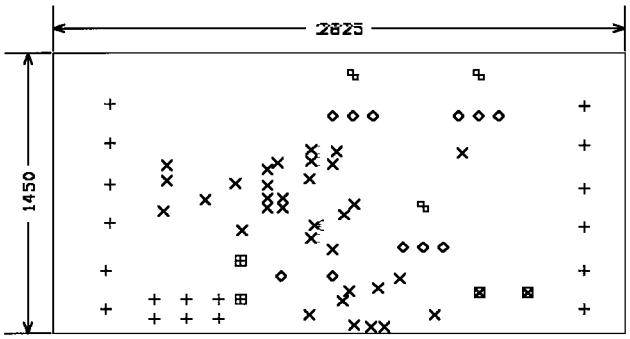

GND


POWER


MOTTOB





RC5042 Evaluation Board

Fairchild Semiconductor provides an evaluation board for the purpose of verifying the system level performance of the RC5042. The evaluation board serves as a guide as to what can be expected in performance with the supplied external components and PCB layout. Please call your Fairchild Semiconductor local Sales Rep Office or Fairchild Semiconductor Marketing Department at (650) 966-7819 for an evaluation board.

Additional Application Information

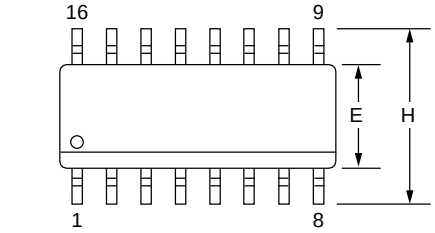
A comprehensive Application Note providing implementation guidelines for the RC5040 and RC5042 DC-DC Converters for Pentium® Pro processors (AP-42) is available from your local Fairchild Semiconductor Sales Rep or from Fairchild Semiconductor Marketing at 650-966-7819. Most application notes and data sheets can also be obtained by calling Fairchild Semiconductor's fax-on-demand system at 650-988-2123.

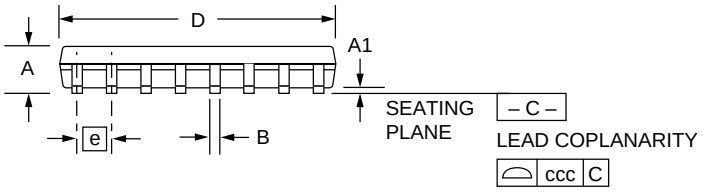
Mechanical Dimensions – 16 Lead SOIC

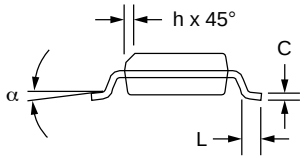
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.19	0.25	5
D	.386	.394	9.80	10.00	2
E	.150	.158	3.81	4.00	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.80	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	16		16		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Ordering Information

Product Number	Package
RC5042M	16 pin SOIC

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Stock#DS30005042

Embedded Secure Document

The file *http://www.fairchildsemi.com/ds/RC/RC5043.pdf* is a secure document that has been embedded in this document. Double click the pushpin to view RC5043.pdf.

RC5050

Programmable DC-DC Converter for Low Voltage Microprocessors

Features

- Programmable output from 1.3V to 3.5V
- 85% efficiency typical
- 1% output accuracy
- Oscillator frequency adjustable from 80KHz to 1MHz
- On-chip Power Good and Enable functions
- Over-Voltage Protection
- Foldback current limiting
- Precision trimmed low TC voltage reference
- 20 pin SOIC package
- Meets Intel Pentium® II specifications using minimum number of external components

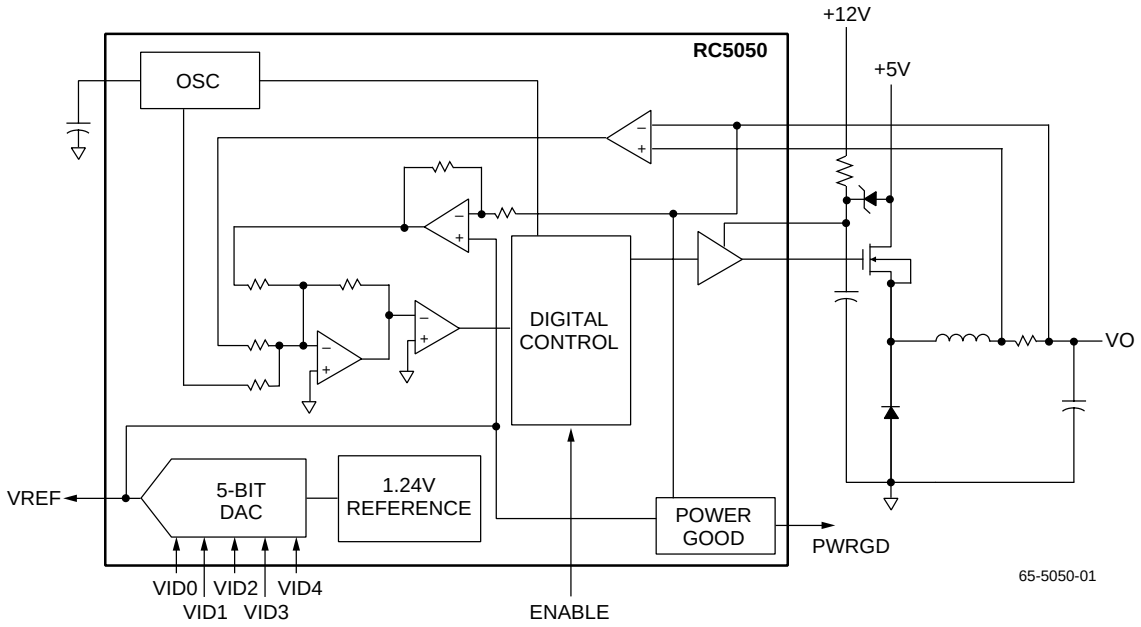
Applications

- Programmable power supply for Pentium II
- Voltage Regulator Module (VRM) for Pentium II processors
- Programmable step-down power supply

Description

The RC5050 is a DC-DC controller IC which provides an accurate, programmable output for all Pentium II CPU applications. The RC5050 uses a 5-bit D/A converter to program the output voltage from 1.3V to 3.5V. The RC5050 uses a high level of integration to deliver load currents in excess of 15A from a 5V source with minimal external circuitry. Non-synchronous operation allows a low cost solution for most CPU power supply applications. The internal oscillator can be programmed from 80KHz to 1MHz for additional flexibility in choosing external components. An on-board precision low TC reference achieves tight tolerance voltage regulation without expensive external components. The RC5050 also offers integrated functions including Power Good, Output Enable, over-voltage protection and current limiting.

Block Diagram



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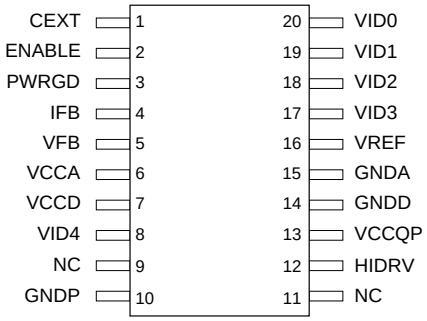
Pin Assignments



65-5050-02

Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	CEXT	**Oscillator Capacitor Connection**. Connecting an external capacitor to this pin sets the internal oscillator frequency. Layout of this pin is critical to system performance. See Application Information for details.
2	ENABLE	**Output Enable**. Open collector/TTL input. Logic LOW will disable output. A 10KΩ internal pull-up resistor assures correct operation if pin is left unconnected.
3	PWRGD	**Power Good Flag**. Open collector output will be at logic HIGH under normal operation. Logic LOW indicates output voltage is not within ±12% of nominal.
4	IFB	**High Side Current Feedback**. Pins 4 and 5 are used as the inputs for the current feedback control loop and as the short circuit current sense points. Layout of these traces is critical to system performance. See Application Information for details.
5	VFB	**Voltage Feedback**. Pin 5 is used as the input for the voltage feedback control loop and as the low side current feedback input. Layout of this trace is critical to system performance. See Application Information for details.
6	VCCA	**Analog Vcc**. Connect to system 5V supply and decouple to ground with 0.1μF ceramic capacitor.
7	VCCD	**Digital Vcc**. Connect to system 5V supply and decouple to ground with 4.7μF tantalum capacitor.
8	VID4	**VID4 Input**. A logic 1 on this open collector/TTL input will enable the VID3–VID0 inputs to set the output from 2.1V to 3.5V, and a logic 0 on this pin will set the output from 1.3V to 2.05V, as shown in Table 1. Pullup resistors are internal to the controller.
9, 11	NC	**No Internal Connection**. Connection of these pins to system ground will improve the thermal dissipation characteristics of the package.
10	GNDP	**Power Ground**. Return pin for high currents flowing in pins 12 and 13 (HIDRV and VCCQP). Connect to low impedance ground.
12	HIDRV	**FET Driver Output**. Connect this pin to the gates of N-channel MOSFETs M1 and M2 in Figure 1. The trace from this pin to the MOSFET gates should be < 0.5".
13	VCCQP	**Power Vcc**. This is the power supply for the FET driver. VCCQP must be connected to a voltage of at least VCCA + $V_{GS,ON}$ (M1). See Application Information for details.
14	GNDD	**Digital Ground**. Return path for digital logic. This pin should be connected to system ground to minimize ground loops.
15	GNDA	**Analog Ground**. Return path for low power analog circuitry. Connect to system ground to minimize ground loops.
16	VREF	**Reference Voltage Test Point**. This pin provides access to the DAC output and should be decoupled to ground using a 0.1μF capacitor. No load should be connected.
17–20	VID3–VID0	**Voltage Identification (VID) Code Inputs**. These open collector/TTL compatible inputs will program the output voltage over the ranges specified in Table 1. Pullup resistors are internal to the controller.

Absolute Maximum Ratings

Supply Voltages, V_{CCA}, V_{CCD}, V_{CCQP}	13V
Voltage Identification Code Inputs, VID4-VID0	13V
Junction Temperature, T_J	150°C
Storage Temperature	-65 to 150°C
Lead Soldering Temperature, 10 seconds	300°C

Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Voltages, V_{CCA} and V_{CCD}		4.5	5	7	V
Output Driver Supply, V_{CCQP}		8.5		12	V
Input Logic HIGH		2.0			V
Input Logic LOW				0.8	V
PWRGD Threshold	Logic HIGH Logic LOW	93 88		107 112	$\%V_O$ $\%V_O$
Ambient Operating Temperature		0		70	°C

Electrical Characteristics

(V_{CCA}, V_{CCD} = 5V, V_{OUT} = 2.8V, F_{osc} = 300 KHz, and T_A = +25°C using Figure 1, unless otherwise specified)
The • denotes specifications which apply over the full operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
Output Voltage	See Table 1	•	1.3		3.5	V
Output Current				13		A
Initial Voltage Setpoint	I_{LOAD} = 0.8A			±20		mV
Output Temperature Drift	T_A = 0 to 60°C	•		+10		mV
Load Regulation	I_{LOAD} = 0.8A to 13A	•		-25		mV
Line Regulation	V_{IN} = 4.75 to 5.25V	•		±2		mV
Output Ripple	20MHz BW, I_{LOAD} = 13A			±11		mV
Output Voltage Regulation Steady State[1] Transient[2]	 V_{OUT} = 2.8V, I_{LOAD} = 0.8 – 15A I_{LOAD} = 0.8 to 14.2A, 30A/µs	 • •	 2.74 2.67	 2.80 2.80	 2.90 2.93	 V V
Short Circuit Detect Threshold		•	100	120	140	mV
Efficiency	I_{LOAD} = 13A, V_{OUT} = 2.8V	•	80	85		%
Output Driver Rise and Fall Time	See Figure 2			50		ns
Turn-on Response Time	I_{LOAD} = 0 to 13A				10	ms
Oscillator Range			80	300	1000	KHz
Oscillator Frequency	C_{EXT} = 100 pF		270	300	330	KHz
Max Duty Cycle	PWM mode		90	95		%

Notes:

1. Steady State Voltage Regulation includes Initial Voltage Setpoint, DC load regulation, output ripple/noise and temperature drift.
2. These specifications assume a minimum of 20, 1µF ceramic capacitors are placed directly next to the CPU in order to provide adequate high-speed decoupling. For motherboard applications, the PCB layout must exhibit no more than 0.5mΩ parasitic resistance and 1nH parasitic inductance between the converter output and the CPU.

Table 1. Output Voltage Programming Codes

VID4	VID3	VID2	VID1	VID0	V_{OUT} to CPU
0	1	1	1	1	1.30V
0	1	1	1	0	1.35V
0	1	1	0	1	1.40V
0	1	1	0	0	1.45V
0	1	0	1	1	1.50V
0	1	0	1	0	1.55V
0	1	0	0	1	1.60V
0	1	0	0	0	1.65V
0	0	1	1	1	1.70V
0	0	1	1	0	1.75V
0	0	1	0	1	1.80V
0	0	1	0	0	1.85V
0	0	0	1	1	1.90V
0	0	0	1	0	1.95V
0	0	0	0	1	2.00V
0	0	0	0	0	2.05V
1	1	1	1	1	No CPU
1	1	1	1	0	2.1V
1	1	1	0	1	2.2V
1	1	1	0	0	2.3V
1	1	0	1	1	2.4V
1	1	0	1	0	2.5V
1	1	0	0	1	2.6V
1	1	0	0	0	2.7V
1	0	1	1	1	2.8V
1	0	1	1	0	2.9V
1	0	1	0	1	3.0V
1	0	1	0	0	3.1V
1	0	0	1	1	3.2V
1	0	0	1	0	3.3V
1	0	0	0	1	3.4V
1	0	0	0	0	3.5V

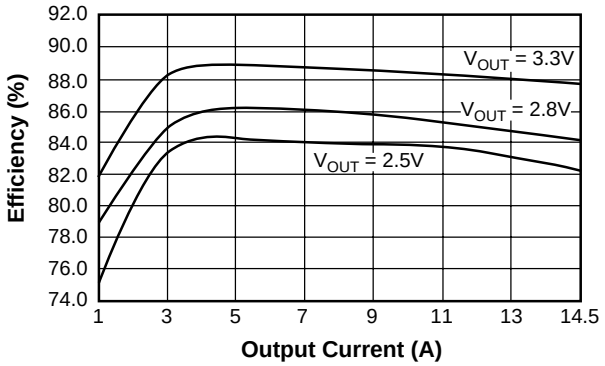
Note:

1. 0 = processor pin is tied to GND
   1 = processor pin is open.

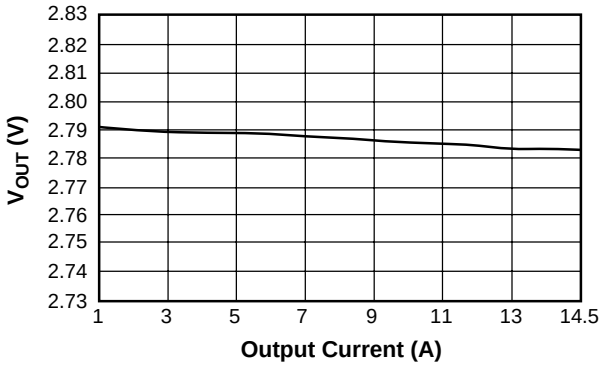
Typical Operating Characteristics

(VCCA, VCCD = 5V, fosc = 280 KHz, and T_A = +25°C using circuit in Figure 1, unless otherwise noted)

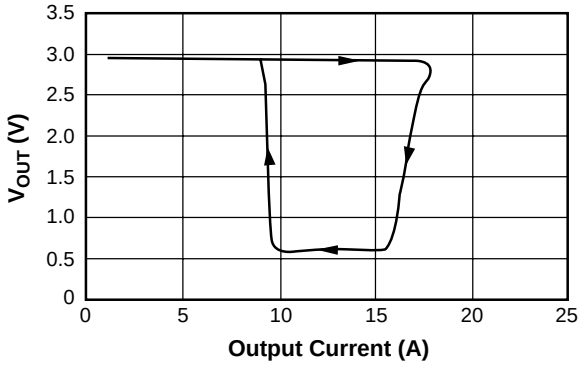
Efficiency vs. Output Current



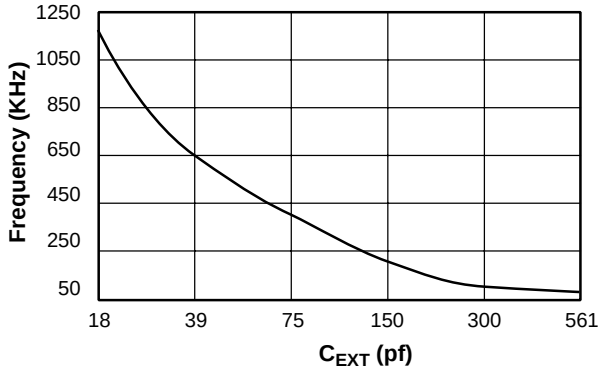
Load Regulation, V_{OUT} = 2.8 V



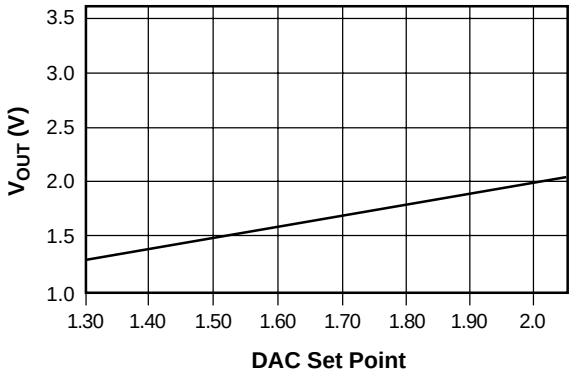
Output Voltage vs. Output Current, R_{SENSE} = 6mΩ



Oscillator Frequency vs. C_{EXT}



Output Programming, VID4 = 0



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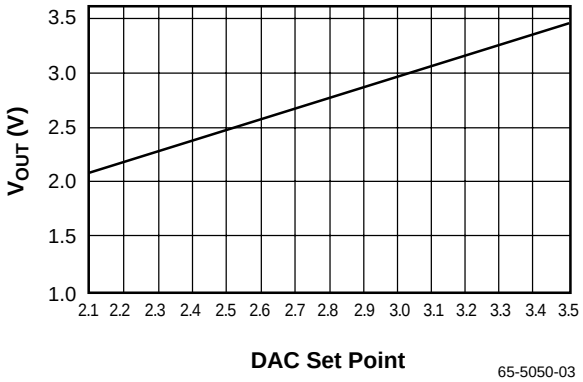

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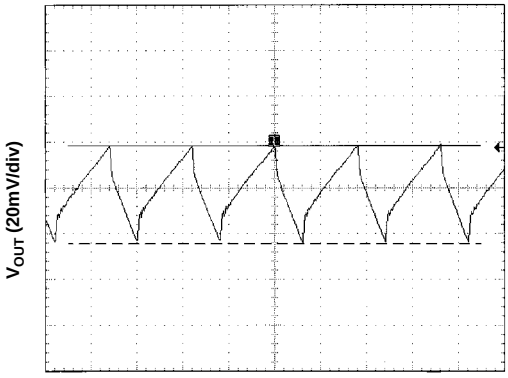
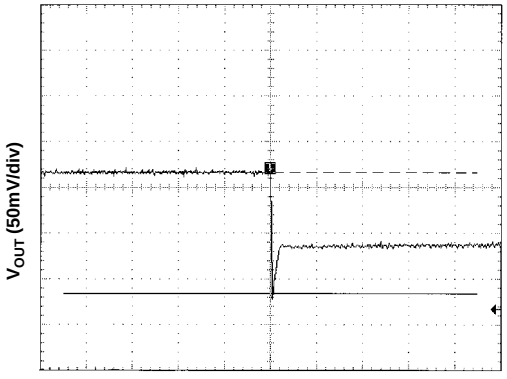
Typical Operating Characteristics (continued)

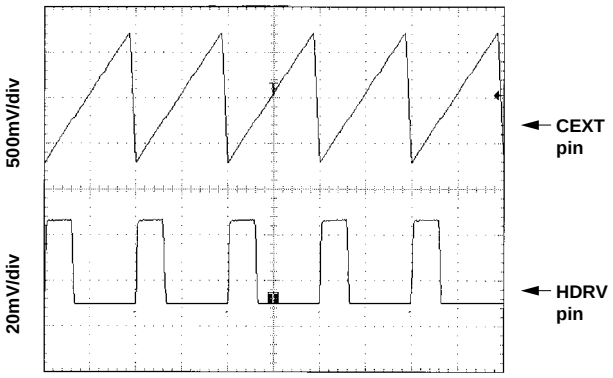
Output Ripple, 2.8V @ 13A



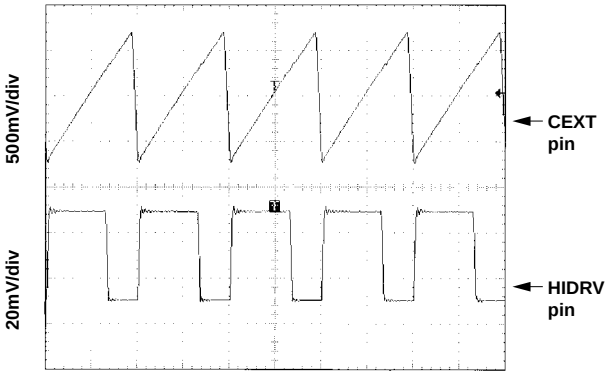
Transient Response, 0.5A to 13A



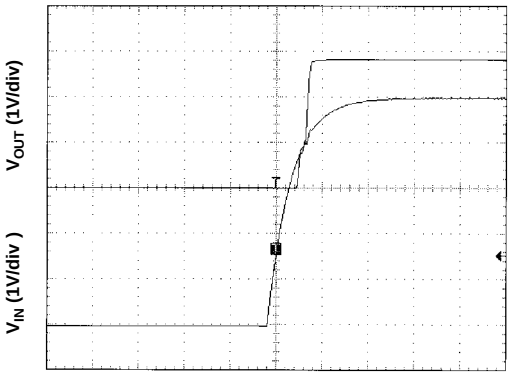
Switching Waveforms, 0.5A Load



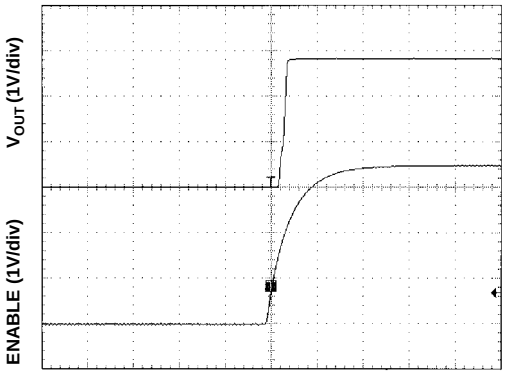
Switching Waveforms, 13A Load



Output Startup, System Power-up



Output Startup from Re-enable



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Test Circuit

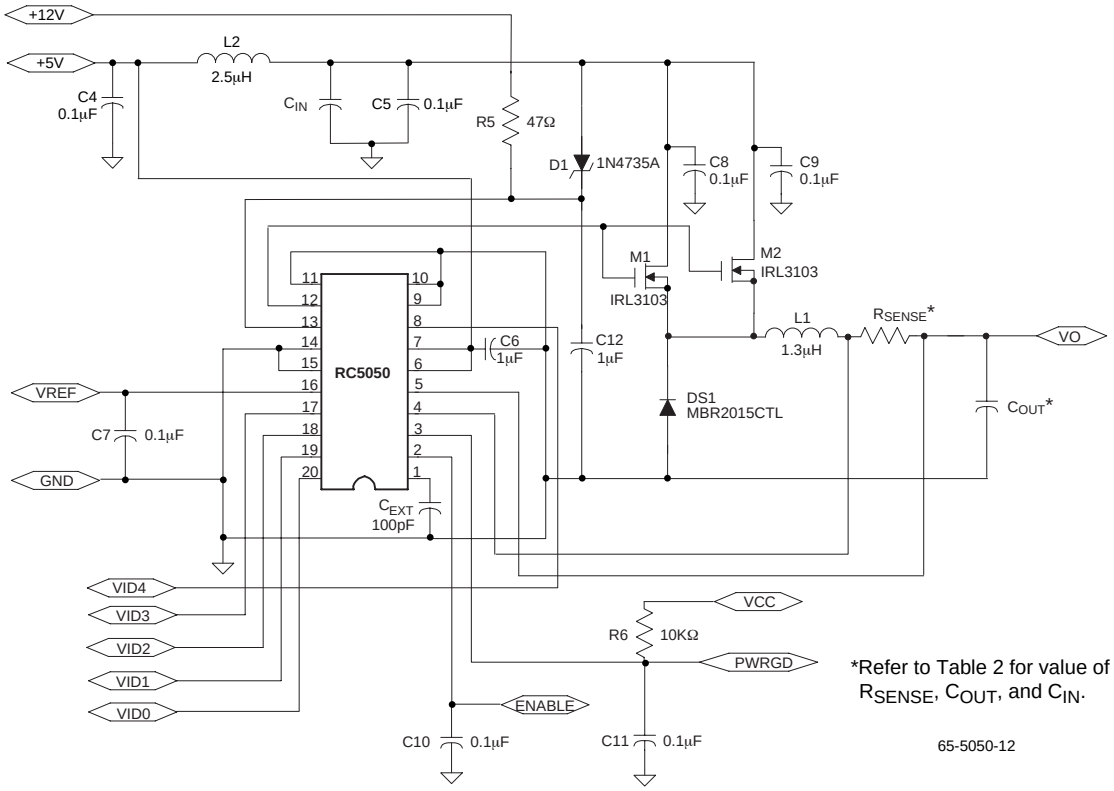


Figure 1. 15A Application Circuit for Pentium II Processor

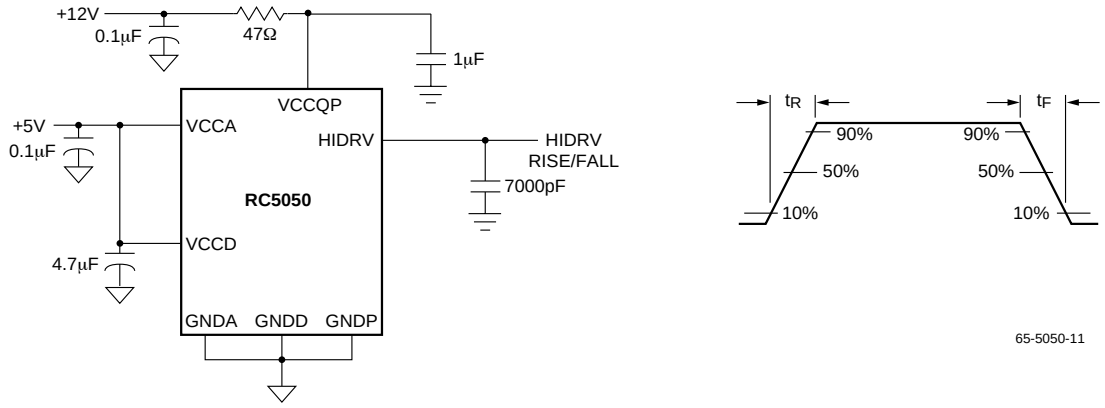


Figure 2. Output Driver Test Circuit

Table 2. Recommended Bulk Capacitors for CPU-based Applications

Application	Output Current	CIN	COUT	COUT Maximum ESR	RSENSE
Motorola PowerPC 603/604 Motherboard	7A	2 x 1500µF, 6V Sanyo 6MV1500CX	2 x 1500µF, 6V Sanyo 6MV1500SX	22mΩ	10.5mΩ
Intel Pentium II Klamath Motherboard	14.2	3 x 1200µF, 10V Sayno 10MV1200EG	5 x 1500µF, 6.3V Sanyo 6MV1500GX	9.0mΩ	5.5mΩ
Intel Pentium II Motherboard (All versions including next generation)	15A	3 x 1200µF, 10V Sayno 10MV1200EG	7 x 1500µF, 6.3V Sanyo 6MV1500GX	6.0mΩ	5.0mΩ

Table 3. RC5050 Application Bill of Materials for Intel Pentium II Processors

Reference	Manufacturer Part #	Description	Requirements/Comments
C4, C5, C7–C11	Panasonic ECU-V1H104ZFX	0.1μF 50V capacitor	
Cext	Panasonic ECU-V1H121JCG	100pF capacitor	
C12, C6	Panasonic ECSH1CY105R	1μF 16V capacitor	
C_{IN}	Sanyo 10MV1200EG	1200μF 10V electrolytic capacitor 10mm x 20mm	ESR < 62mΩ See Table 2
C_{OUT}	Sanyo 6MV1500GX	1500μF 6.3V electrolytic capacitor 10mm x 20mm	ESR < 44mΩ See Note 1 and Table 2
DS1	Motorola MBR2015CT	Schottky Diode	V_f < 0.52 at I_f = 10A
D1	1N4735A	6.2V Zener Diode, Motorola	
L1	Skynet 320-8107	1.3μH, 14A inductor DCR ~ 2.5mΩ	See Note 2
L2	Skynet 320-6110	2.5μH, 11A inductor DCR ~ 6mΩ	See Note 3
M1, M2	International Rectifier IRL3103	N-Channel Logic Level Enhancement Mode MOSFET	$R_{DS(ON)}$ < 19mΩ V_{GS} < 4.5V, I_D = 15A See Note 4
R_{SENSE}	Copel AWG#18	5.5mΩ CuNi Alloy Wire Resistor	
R5	Panasonic ERJ-6GEY050Y	47Ω 5% resistor	
R6	Panasonic ERJ-6ENF10.0KV	10KΩ 5% resistor	

Notes:

1. In order to meet the voltage transient requirements for the Intel Pentium II Motherboard application, the equivalent ESR of the output capacitors must not exceed 7.5mΩ. In order to satisfy the specified Output Voltage Regulation requirements for V_{OUT} = 1.8V at 15A for next generation processors, the output capacitors must exhibit no more than 6.0mΩ equivalent ESR for a motherboard application. The use of the capacitors recommended in Table 1 will address this and other voltage specifications without significant added cost, although it is left up to the user to specify the components used. Please refer to Application Bulletin 5 for additional considerations required to meet the Intel Pentium II voltage transient specifications.
2. To optimize a converter for 15A at 1.8V output, f_{SW} = 300 kHz, change the value of L1 to 1.24μH.
3. Inductor L2 is recommended to isolate the 5V input supply from current surges caused by MOSFET switching. L2 is not required for normal operation and may be omitted if desired.
4. For 15A designs using IR3103 MOSFETs, heat sinks with thermal resistance Θ_{SA} < 50°C/W should be used.

Application Information

Simple Step-Down Converter

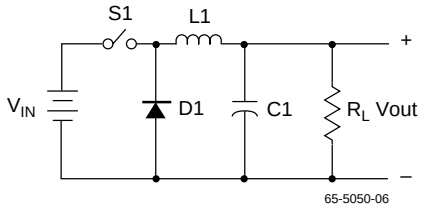


Figure 3. Simple Buck DC-DC Converter

Figure 3 illustrates a step-down DC-DC converter with no feedback control. The derivation of the basic step-down converter will serve as a basis for the design equations for the RC5050. Referring to Figure 3, the basic operation begins by closing the switch S1. When S1 is closed, the input voltage V_{IN} is impressed across inductor L1. The current flowing in this inductor is given by the following equation:

$$I_L = \frac{(V_{IN} - V_{OUT})T_{ON}}{L1}$$

where T_{ON} is the duty cycle (the time when S1 is closed).

When S1 opens, the diode D1 will conduct the inductor current and the output current will be delivered to the load according to the equation:

$$I_L = \frac{V_{OUT}(T_S - T_{ON})}{L1}$$

where T_S is the overall switching period and ($T_S - T_{ON}$) is the time during which S1 is open.

By solving these two equations, we can arrive at the basic relationship for the output voltage of a step-down converter:

$$V_{OUT} = V_{IN}\left(\frac{T_{ON}}{T_S}\right)$$

In order to obtain a more accurate approximation for V_{OUT}, we must also include the forward voltage V_D across diode D1 and the switching loss, Vsw. After taking into account these factors, the new relationship becomes:

$$V_{OUT} = (V_{IN} + V_D - V_{SW})\frac{T_{ON}}{T_S} - V_D$$

where V_{SW} = MOSFET switching loss
= $I_L \bullet R_{DS,ON}$

The RC5050 Controller

The RC5050 is a programmable DC-DC controller IC. When designed around the appropriate external components, The RC5050 can be configured to deliver more than 14.5A of output current. The RC5050 utilizes both current-mode and voltage-mode control to create an integrated step-down voltage regulator. During heavy loading conditions, the RC5050 functions as a PWM step down regulator. Under light loads, the controller goes into Pulse Frequency Modulation (PFM) or pulse-skipping mode. The controller will sense the load level and switch between the two modes automatically, thus optimizing its efficiency under all conditions.

Main Control Loop

For this discussion, refer to the Block Diagram on page 1 of the data sheet. The control loop of the regulator contains two main sections; the analog control block and the digital control block. The analog block consists of signal conditioning amplifiers feeding into a set of comparators which provide the inputs to the digital block. The signal conditioning section accepts inputs from the IFB (current feedback) and VFB (voltage feedback) pins and sets up two controlling signal paths. The voltage control path amplifies the VFB signal and presents the output to one of the summing amplifier inputs. The current control path takes the difference between the IFB and VFB pins and presents the resulting signal to another input of the summing amplifier. These two signals are then summed together with the slope compensation input from the oscillator. This output is then presented to a comparator, which provides the main PWM control signal to the digital control block.

The additional comparators in the analog control section set the point at which the max current comparator disables the output drive signals to the external power MOSFETs.

The digital control block is designed to take the comparator inputs along with the main clock signal from the oscillator and provide the appropriate pulses to the HIDRV output pin that controls the external power MOSFET(s). The digital section was designed utilizing high speed Schottky transistor logic, thus allowing the RC5050 to operate at clock speeds as high as 1MHz.

High Current Output Drivers

The RC5050 contains a high current output driver which utilizes high speed bipolar transistors arranged in a push-pull configuration. This driver is capable of delivering 1A of current in less than 100ns. The driver's power and ground are separated from the overall chip power and ground for additional switching noise immunity. The output driver power supply, VCCQP, is derived from an external 12V supply through a 47Ω series resistor. The resulting voltage is sufficient to provide the gate-source voltage to the external MOSFET required in order to achieve a low $R_{DS,ON}$.

Internal Voltage Reference

The reference included in the RC5050 is a precision bandgap voltage reference. The internal resistors are precisely trimmed to provide a near zero temperature coefficient (TC). Added to the reference output is the resulting output from an integrated 5-bit DAC. The DAC is provided in order to allow the DC-DC converter output to be directly programmable via a 5-bit digital input. When the VID4 pin is in the HIGH state, pins VID3–VID0 will scale the output voltage from 2V to 3.5V in 100mV increments. When the VID4 pin is pulled LOW, the output can be programmed from 1.3V to 2.05V in 50mV steps. For guaranteed stable operation under all operating conditions, a 0.1µF decoupling capacitor should be connected to the VREF pin. No load should be imposed upon this pin.

Power Good (PWRGD)

The RC5050 Power Good function is designed in accordance with the Pentium II DC-DC converter specifications and provides a constant voltage monitor on the VFB pin. The internal circuitry compares the VFB signal to the VREF voltage and outputs an active-low interrupt signal to the CPU should the power supply voltage exceed ±10% of its nominal setpoint. The Power Good flag provides no other control function to the RC5050.

Output Enable (ENABLE)

Intel specifications state that the DC-DC converter should accept an open collector signal for controlling the output voltage; a logic LOW on the ENABLE pin disables the output voltage. When disabled, the PWRGD output is in the low state.

Upgrade Present

Intel specifications state that the DC-DC converter should accept an open collector signal (UP#), used to indicate the presence of an upgrade processor. The typical state is high (standard processor). When in the low or ground state (OverDrive processor present), the output voltage must be disabled unless the converter can supply the OverDrive processor's power requirements. Because the RC5050 can supply the OverDrive processor requirements, the UP# signal is not required.

Over-Voltage Protection

The RC5050 provides a constant monitor of the output voltage for protection against over voltage conditions. If the voltage at the VFB pin exceeds 20% of the selected program voltage, an over-voltage condition will be assumed and the RC5050 will disable the output drive signal to the external MOSFET(s).

Short Circuit Protection

A current sense methodology is implemented to disable the output drive signal to the MOSFET(s) when an over-current condition is detected. The voltage drop created by the output current flowing across a sense resistor is presented to an internal comparator. When the voltage developed across the sense resistor exceeds the 120 mV comparator threshold voltage, the RC5050 will reduce the output duty cycle to protect the power devices.

The DC-DC converter will return to normal operation after the fault has been removed, for either an over voltage or a short circuit condition.

Oscillator

The RC5050 oscillator section is implemented using a fixed current capacitor charging configuration. An external capacitor (C_{EXT}) is used to preset the oscillator frequency between 80KHz and 1MHz. This scheme allows maximum flexibility in setting the switching frequency as well as in choosing external components.

In general, a lower operating frequency will increase the peak ripple current flowing in the output inductor and thus require the use of a larger inductor value. Operation at lower frequencies also increases the amount of energy storage that must be provided by the bulk output capacitors during load transients due to the slower loop response of the controller.

Additionally, the efficiency losses due to switching of the MOSFETs will increase as the operating frequency is increased. Therefore, efficiency will be optimized at lower operating frequencies.

Due to the trend of increasing load current at lower supply voltages, an operating frequency of 300 KHz has been chosen to optimize efficiency while maintaining excellent output regulation and transient performance.

Design Considerations and Component Selection

MOSFET Selection

This application requires the use of N-channel, Logic Level Enhancement Mode Field Effect Transistors. Desired characteristics are as follows:

- Low Static Drain-Source On-Resistance, $R_{DS,ON} < 37\ m\Omega$ (lower is better).
- Low gate drive voltage, $V_{GS} \leq 4.5V$.
- Power package with low Thermal Resistance.
- Drain current rating of 20A minimum.
- Drain-Source voltage > 15V

The on-resistance ($R_{DS,ON}$) is the primary parameter for MOSFET selection. The on-resistance determines the power dissipation of the MOSFET and therefore significantly affects the efficiency of the DC-DC Converter. Table 4 presents a list of suitable MOSFETs for this application.

Two MOSFETs in Parallel

At higher load currents, it is recommend that two MOSFETs be used in parallel instead of a single MOSFET. Significant advantages are realized using two MOSFETs in parallel:

- **Significant reduction of power dissipation**.

  Maximum current of 15A with one MOSFET:

  $$P_{MOSFET} = (I^2 R_{DS,ON})(\text{Duty Cycle})$$
  $$= (15)^2(0.050^*)(2.8+0.4)/(5+0.4-0.35)$$
  $$= 7.1\ W$$

  With two MOSFETs in parallel:

  $$P_{MOSFET} = (I^2 R_{DS,ON})(\text{Duty Cycle})$$
  $$= (15/2)^2(0.037^*)(2.8+0.4)/(5+0.4-0.35)$$
  $$= 1.3W/FET$$

  * **Note:** $R_{DS,ON}$ increases with temperature. Assume $R_{DS,ON} = 25m\Omega$ at 25°C. $R_{DS,ON}$ can easily increase to $50m\Omega$ at high temperature when using a single MOSFET. When using two MOSFETs in parallel, the temperature effects should not cause the $R_{DS,ON}$ to rise above the listed maximum value of $37m\Omega$.

- **No added heat sink required.** With power dissipation down to around one watt and with MOSFETs mounted flat on the motherboard, no external heat sink is required. The junction-to-case thermal resistance for the MOSFET package (TO-220) is typically at 2°C/W and the motherboard serves as an excellent heat sink.
- **Higher current capability.** With thermal management under control, this on-board DC-DC circuit is able to deliver load currents up to 15A with no performance or reliability concerns.

Table 4. MOSFET Selection Table

Manufacturer & Model #	Conditions[1]		$R_{DS,ON}$(mΩ) Typ.	$R_{DS,ON}$(mΩ) Max.	Package	Thermal Resistance
Fuji 2SK1388	V_{GS}=4V, I_D=17.5A	T_J =25°C	25	37	TO-220	Φ_{JA}=75
		T_J =125°C	37	—		
Siliconix SI4410DY	V_{GS}=4.5V, I_D=5A	T_J =25°C	16.5	20	SO-8 (SMD)	Φ_{JA}=50
		T_J =125°C	28	34		
National Semiconductor NDP706AL	V_{GS}=5V, I_D=40A	T_J =25°C	13	15	TO-220	Φ_{JA}=62.5 Φ_{JC}=1.5
NDP706AEL		T_J =125°C	20	24		
National Semiconductor	V_{GS}=4.5V, I_D=10A	T_J =25°C	31	40	TO-220	Φ_{JA}=62.5
NDP603AL		T_J =125°C	42	54		Φ_{JC}=2.5
National Semiconductor	V_{GS}=5V, I_D=24A	T_J =25°C	22	25	TO-220	Φ_{JA}=62.5
NDP606AL		T_J =125°C	33	40		Φ_{JC}=1.5
Motorola	V_{GS}=5V, I_D=37.5A	T_J =25°C	6	9	TO-263	Φ_{JA}=62.5
MTB75N03HDL		T_J =125°C	9.3	14	(D^2 PAK)	Φ_{JC}=1.0
Int. Rectifier	V_{GS}=5V, I_D=31A	T_J =25°C	—	28	TO-220	Φ_{JA}=62.5
IRLZ44		T_J =125°C	—	46		Φ_{JC}=1.0
Int. Rectifier	V_{GS}=4.5V, I_D=28A	T_J =25°C	—	19	TO-220	Φ_{JA}=62.5
IRL3103S		T_J =125°C		31		Φ_{JC}=1.0

Note:

1. $R_{DS,ON}$ values at Tj = 125°C for most devices were extrapolated from the typical operating curves supplied by the manufacturers and are approximations only.

MOSFET Gate Bias

Figure 4 illustrates how an external 12V supply is used to bias the output driver supply, VCCQP. A 47Ω resistor is used to limit the transient current into the VCCQP pin and a 1µF capacitor filter is used to filter the VCCQP supply. This method provides a sufficient gate-to-source bias voltage (V_{GS}) to the MOSFET, and therefore reduces the $R_{DS,ON}$ and the resulting power loss within the MOSFET. Figure 5 illustrates how the $R_{DS,ON}$ decreases dramatically as V_{GS} increases. A 6.2V Zener (D1) is used to clamp the voltage at VCCQP to a maximum of 12V, thus ensuring that the absolute maximum voltage limit of the IC will not be exceeded.

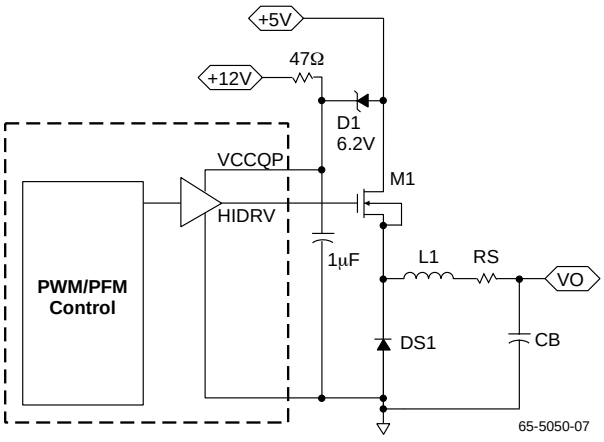


Figure 4. MOSFET Gate Bias Configuration

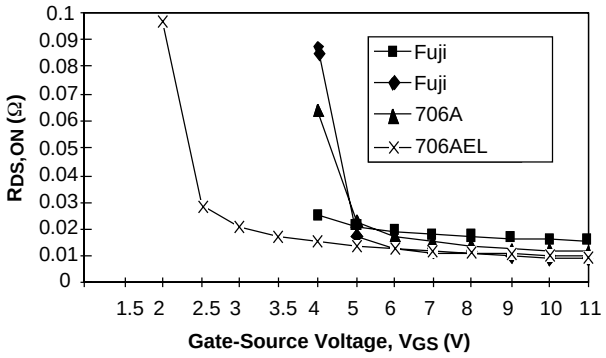


Figure 5. $R_{DS,ON}$ vs. V_{GS} for Selected MOSFETs

Converter Efficiency

Losses due to parasitic resistance in the switches, inductor coil and sense resistor dominate at high load current levels. The major loss mechanisms under heavy loads, in usual order of importance, are:

- MOSFET I^2R losses
- Inductor coil losses
- Sense resistor losses
- Gate-charge losses
- Diode-conduction losses
- Transition losses
- Input capacitor losses
- Losses due to the operating supply current of the IC.

The following sections provide details of these dominant loss components.

Selecting the Inductor

The inductor is one of the most critical components to be selected in the DC-DC converter application.. The critical parameters are inductance (L), maximum DC current (Io) and the DC coil resistance (R_l). The inductor core material is a crucial factor in determining the amount of current the inductor will be able to withstand. As with all engineering designs, tradeoffs exist between various types of core materials. In general, Ferrites are popular due to their low cost, low EMI properties and high frequency (>500KHz) characteristics. Molypermalloy powder (MPP) materials exhibit good saturation characteristics, low EMI and low hysteresis losses; however, they tend to be expensive and more effectively utilized at operating frequencies below 400KHz. Another critical parameter is the DC winding resistance of the inductor. This value should typically be reduced as much as possible, as the power loss in the DC resistance will degrade the efficiency of the converter by the relationship: $P_{LOSS} = I_O^2 \times R_l$.

Choosing the value of the inductor is a tradeoff between allowable ripple voltage and required transient response. The system designer can choose any value within the allowed range in order to maximize either ripple or transient performance. The first order equation (close approximation) for minimum inductance is:

$$L_{min} = \frac{(V_{OUT} - V_{IN})}{f} \times \frac{V_{OUT}}{V_{IN}} \times \frac{ESR}{V_r}$$

where:

- V_{IN} = Input Power Supply
- V_{OUT} = Output Voltage
- f = DC/DC converter switching frequency
- ESR = Equivalent series resistance of all output capacitors in parallel
- V_r = Peak to peak output ripple voltage budget.

The first order equation for maximum allowed inductance is:

$$L_{min} = 2Co \times \frac{(V_{IN} - V_{OUT})D_m V_{tb}}{I_{p^2}}$$

where:

- Co = The total output capacitance
- I_p = Peak to peak load transient current
- V_{tb} = The output voltage tolerance budget allocated to load transient
- D_m = Maximum duty cycle for the DC/DC converter (usually 95%).

Some margin should be maintained between L_{min} and L_{max}. Adding margin by increasing L_{max} almost always adds expense since all the variables are predetermined by system performance except for C_o, which must be increased to increase L_{max}. Adding margin by decreasing L_{min} can either be done by purchasing capacitors with lower ESR or by increasing the DC/DC converter switching frequency. The RC5050 is capable of running at high switching frequencies and provides significant cost savings for the newer CPU systems that typically run at high supply current.

Implementing Short Circuit Protection

Intel currently requires all power supply manufacturers to provide continuous protection against short circuit conditions that may damage the CPU. To address this requirement, Fairchild Semiconductor has implemented a current sense methodology to limit the power delivered to the load in the event of an overcurrent condition. The voltage drop created by the output current flowing across a sense resistor is presented to one terminal of an internal comparator with hysterisis. The other comparator terminal has a threshold voltage, nominally 120mV. Table 6 states the limits for the comparator threshold of the Switching Regulator.

Table 6. RC5050 Short Circuit Comparator Threshold Voltage

	Short Circuit Comparator $V_{threshold}$ (mV)
Typical	120
Minimum	100
Maximum	140

When designing the external current sense circuitry, the designer must pay careful attention to the output limitations during normal operation and during a fault condition. If the short circuit protection threshold current is set too low, the DC-DC converter may not be able to continuously deliver the maximum CPU load current. If the threshold level is too high, the output driver may not be disabled at a safe limit and the resulting power dissipation within the MOSFET(s) may rise to destructive levels.

The design equation used to set the short circuit threshold limit is as follows:

$$R_{SENSE} = \frac{V_{th}}{I_{SC}}, \text{ where: } I_{SC} = \text{Output short circuit current}$$

$$I_{SC} \geq I_{inductor} = I_{Load,\,max} + \frac{(I_{pk} - I_{min})}{2}$$

where I_{pk} and I_{min} are peak ripple current and $I_{load,\,max}$ = maximum output load current

The designer must also take into account the current ($I_{pk} - I_{min}$), or the ripple current flowing through the inductor under normal operation. Figure 6 illustrates the inductor current waveform for the RC5050 DC-DC converter at maximum load.

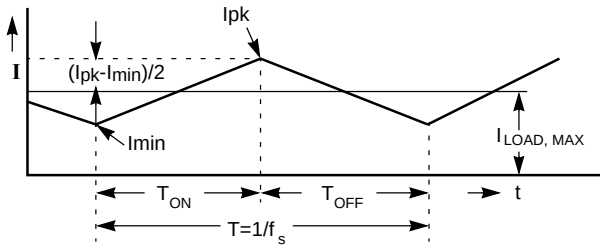


Figure 6. Typical DC-DC Converter Inductor Current Waveform

The calculation of this ripple current is as follows:

$$\frac{(I_{pk} - I_{min})}{2} = \frac{(V_{IN} - V_{SW} - V_{OUT})}{L} \times \frac{(V_{OUT} + V_D)}{(V_{IN} - V_{SW} + V_D)} \times T$$

where:

- V_{in} = input voltage to converter
- V_{SW} = voltage across the MOSFET
  = I_{LOAD} x $R_{DS,ON}$
- V_D = Forward Voltage of the Schottky diode
- T = the switching period of the converter = 1/fs,
  where f_S = switching frequency.

For an input voltage of 5V, an output voltage of 2.8V, an inductor value of 1.3µH and a switching frequency of 285KHz (using C_{EXT} = 100pF), the inductor current can be calculated as follows:

$$\frac{(I_{pk} - I_{min})}{2} = \frac{(5.0 - 14.5 \times 0.037 - 2.8)}{1.3 \times 10^{-6}} \times$$

$$\frac{(2.8 + 0.5)}{(5.0 - 14.5 \times 0.037 + 0.5)} \times \frac{1}{285 \times 10^{3}} \approx 3A$$

Therefore, for a continuous load current of 14.5A, the peak current through the inductor, I_{pk}, is found to be:

$$I_{SC} \geq I_{inductor} = I_{Load,\,max} + \frac{(I_{PK} - I_{min})}{2} = 14.5 + 3 = 17.5A$$

For continuous operation at 14.5A, the short circuit detection threshold must be at least 17.5A.

The next step is to determine the value of the sense resistor. Including tolerance, the sense resistor value can be approximated as follows:

$$R_{SENSE} = \frac{V_{th,min}}{I_{SC}} \times (1 - TF) = \frac{V_{th,min}}{3.0 + I_{Load,max}} \times (1 - TF)$$

where TF = Tolerance Factor for the sense resistor.

There are several different types of sense resistors. Table 7 describes tolerance, size, power capability, temperature coefficient and cost of various sense resistors.

Table 7. Comparison of Sense Resistors

Description	Motherboard Trace Resistor	Discrete Iron Alloy resistor (IRC)	Discrete Metal Strip surface mount resistor (Dale)	Discrete MnCu Alloy wire resistor	Discrete CuNi Alloy wire resistor (Copel)
Tolerance Factor (TF)	±29%	±5% (±1% available)	±1%	±10%	±10%
Size (L x W x H)	2" x 0.2" x 0.001" (1 oz Cu trace)	0.45" x 0.065" x 0.200"	0.25" x 0.125" x 0.025"	0.200" x 0.04" x 0.160"	0.200" x 0.04" x 0.100"
Power capability	>50A/in	1 watt (3W and 5W available)	1 watt	1 watt	1 watt
Temperature Coefficient	+4,000 ppm	+30 ppm	±75 ppm	±30 ppm	±20 ppm
Cost @10,000 piece	Low included in motherboard	$0.31	$0.47	$0.09	$0.09

Based on the Tolerance in the above table:

- For an embedded PC trace resistor and $I_{load,max}$ = 14.5A:

$$R_{SENSE} = \frac{V_{th,min}}{3.0A + I_{Load,\,max}} \times (1 - TF) =$$

$$\frac{100mV}{3.0A + 14.5A} \times (1 - 29\%) = 4.1m\Omega$$

- For a discrete resistor and $I_{load,\,max}$ = 14.5A:

$$R_{SENSE} = \frac{V_{th,min}}{3.0A + I_{Load,\,max}} \times (1 - TF) =$$

$$\frac{100mV}{3.0A + 14.5A} \times (1 - 5\%) = 5.4m\Omega$$

For user convenience, Table 8 lists the recommended values for sense resistor values at various load currents using an embedded PC trace resistor or discrete resistor.

Table 8. R_{sense} for Various Load Currents

$I_{Load,max}$ (A)	R_{SENSE} PC Trace Resistor (mΩ)	R_{SENSE} Discrete Resistor (mΩ)
10.0	5.5	7.3
11.2	5.0	6.7
12.4	4.6	6.2
13.9	4.2	5.6
14.0	4.2	5.6
14.5	4.1	5.4

RC5050 Short Circuit Current Characteristics

The RC5050 has a short circuit current characteristic that includes a foldback function with hysteresis that prevents the DC-DC converter from oscillating in the event of a short circuit. A typical V-I characteristic of the DC-DC converter output using a sense resistor value of 6mΩ is presented in the Typical Operating Characteristics section, page 5. The converter performs with a typical voltage regulation characteristic until the voltage across the resistor exceeds the internal short circuit comparator threshold of 120mV. At this point, the internal comparator trips and sends a signal to the controller to turn off the gate drive to the power MOSFET. This causes a drastic reduction in the output voltage as the load regulation collapses into the short circuit control mode. The output voltage will not return to the normal load characteristic until the output short circuit current is reduced to within the safe range for the DC-DC converter.

Schottky Diode Selection

The application circuit of Figure 1 shows a Schottky diode, DS1. DS1 is used as a flyback diode to provide a constant current path for the inductor when M1 is turned off. A vital selection criteria for DS1 is that it exhibits a very low forward voltage drop, as this parameter will directly impact the regulator efficiency as the output voltage is reduced. Table 9 presents several suitable Schottky diodes for this application. Note that the diode MBR2015CTL has a very low forward voltage drop. This diode is most ideal for applications where output voltages below 2.8V are required.

Table 9. Schottky Diode Selection Table

Manufacturer Model #	Conditions	Forward Voltage V_F
Philips	I_F = 20A; T_j=25°C	< 0.84V
PBYR1035	I_F = 20A; T_j=125°C	< 0.72V
Motorola	I_F = 20A; T_j=25°C	< 0.84V
MBR2035CT	I_F = 20A; T_j=125°C	< 0.72V
Motorola	I_F = 15A; T_j=25°C	< 0.84V
MBR1545CT	I_F = 15A; T_j=125°C	< 0.72V
Motorola	I_F = 20A; T_j=25°C	< 0.58V
MBR2015CTL	I_F = 20A; T_j=150°C	< 0.48V

Output Filter Capacitors

Optimal ripple performance and transient response are functions of the filter capacitors used. Since the 5V supply of a PC motherboard may be located several inches away from the DC-DC converter, input capacitance can play an important role in the load transient response of the RC5050. The higher the input capacitance, the more charge storage is available for improving the current transfer through the FET(s). Low "ESR" capacitors are best suited for this type of application and incorrect selection can influence the converter's overall performance. The input capacitor should be placed as close to the drain of the FET as possible to reduce the effect of ringing caused by long trace lengths.

The ESR rating of a capacitor is a difficult number to quantify. ESR or Equivalent Series Resistance, is defined as the resonant impedance of the capacitor. Since the capacitor is actually a complex impedance device having resistance, inductance and capacitance, it is quite natural for this device to have a resonant frequency. As a rule, the lower the ESR, the better suited the capacitor is for use in switching power supply applications. Many capacitor manufacturers do not supply ESR data. A useful estimate of the ESR can be obtained using the following equation:

$$ESR = \frac{DF}{2\pi fC}$$

where:
- DF is the dissipation factor of the capacitor
- f is the operating frequency
- C is the capacitance in farads.

With this in mind, correct calculation of the output capacitance is crucial to the performance of the DC-DC converter. The output capacitor determines the overall loop stability, output voltage ripple and load transient response. The calculation is as follows:

$$C(\mu F) = \frac{I_O \times \Delta T}{\Delta V - I_O \times ESR}$$

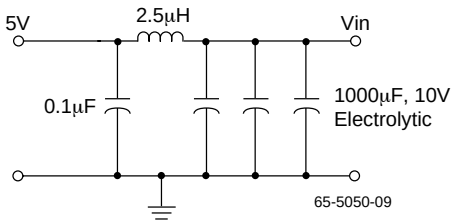
where:
- ΔV is the maximum voltage deviation due to load transients
- ΔT is the reaction time of the power source (Loop response time of the RC5050), approximately 2µs
- I_O is the output load current.

For I_O = 12.2A (0.8 to 13A) and ΔV = 100mV, the bulk capacitance required can be approximated as follows:

$$C(\mu F) = \frac{I_O \times \Delta T}{\Delta V - I_O \times ESR} = \frac{12.2 \times 2\mu s}{100mV - 12.2A \times 7.5m\Omega} = 3200\mu F$$

Input Filter

It is recommended that the design include an input inductor between the system +5V supply and the DC-DC converter input described below. This inductor will serve to isolate the +5V supply from noise occurring in the switching portion of the DC-DC converter and also to limit the inrush current into the input capacitors during power up. An inductor value of around 2.5µH is recommended, as illustrated below.



PCB Layout Guidelines and Considerations

PCB Layout Guidelines

1. Placement of the MOSFETs relative to the RC5050 is critical. The MOSFETs (M1 & M2), should be placed such that the trace length of the HIDRV pin from the RC5050 to the FET gates is minimized. A long lead length on this pin will cause high amounts of ringing due to the inductance of the trace combined with the large gate capacitance of the FET(s). This noise will radiate all over the board and will be very difficult to suppress, especially when the oscillator frequency is increased.

   Figure 7 depicts an example of proper placement of the MOSFETs in relation to the RC5050 as well as an example of incorrect placement of the MOSFETs.

   In general, all of the noisy switching lines should be kept away from the quiet analog section of the RC5050. That is to say, traces that connect to pins 12 and 13 (HIDRV and VCCQP) should be kept far away from the traces that connect to pins 1 through 5, and pin 16.

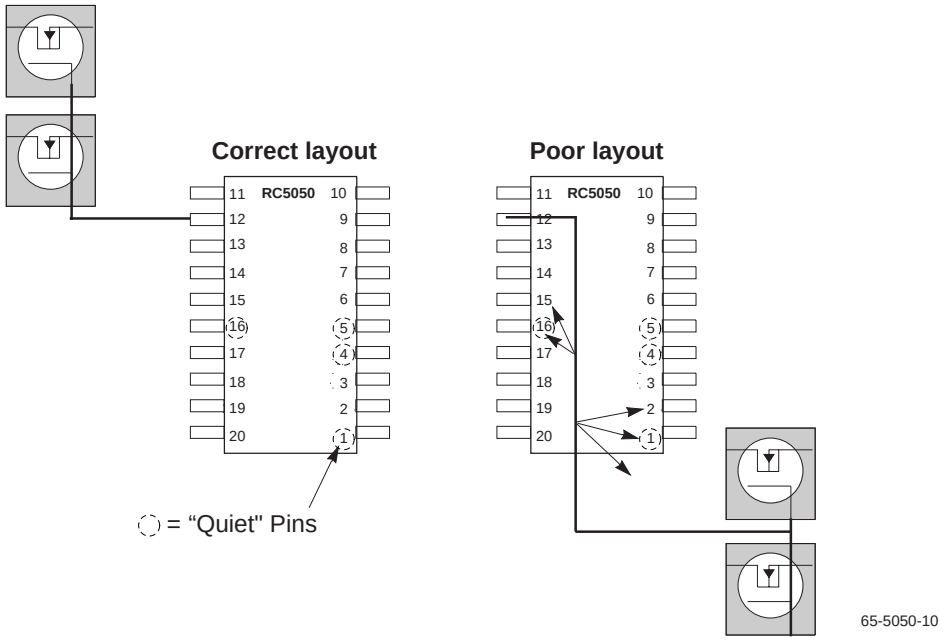


Figure 7. Examples of Good and Bad MOSFET Layout

2. Place decoupling capacitors (0.1µF) as close to the RC5050 pins as possible. Extra lead length on these capacitors will negate their ability to suppress noise.

3. Each VCC and GND pin should have its own via down to the appropriate plane underneath. This will help to add isolation between pins.

4. The CEXT timing capacitor should be surrounded with a ground trace if possible. The placement of a ground or power plane underneath the capacitor will also provide further noise isolation. This will help to shield the oscillator from the noise on the PCB. This capacitor should be placed as close to pin 1 as possible.

5. Group the MOSFETs, inductor and Schottky as close together as possible for the same reasons as #1 above. Also place the input bulk capacitors as close to the drains of MOSFETs as possible. In addition, placement of a 0.1µF decoupling cap right on the drain of each MOSFET will help to suppress some of the high frequency switching noise on the input of the DC-DC converter.

6. The traces that run from the RC5050 IFB (pin 4) and VFB (pin 5) pins should be run together next to each other and be Kelvin connected to the sense resistor. Running these lines together will help in rejecting some of the common noise that is presented to the RC5050 feedback input. Try as much as possible to run the noisy switching signals (HIDRV & VCCQP) on one layer and use the inner layers for power and ground only. If the top layer is being used to route all of the noisy switching signals, use the bottom layer to route the analog sensing signals VFB and IFB.

PC Board Layout Checklist

- **Bypass Capacitor near Vref pin.**
  This pin should be adequately bypassed with a 0.1µF capacitor.
- **Bypass Capacitors for VCC (5V).**
  A 0.1µF should be placed right next to the VCC pin of the controller.
- **Bypass Capacitors for Power MOSFET.**
  A 0.1µF cap should be placed at the drain connection of each power MOSFET.
- **5V Connection to the controller IC.**
  Each VCC pin on the IC should be connected to the 5V power plane through its own via.
- **Power MOSFET Gate Drive Trace.**
  - The gate drive trace should be routed on one layer only.
  - The controller IC and the power FET should be oriented in such a way as to minimize the trace length of the gate drive trace (< 1 inch).
  - The gate drive trace routing should stay away from the quiet analog section of the RC50XX controller IC. (i.e. keep away from Vref, IFB, VFB, and CEXT.)
- **Bulk Capacitance.**
  - The input bulk capacitance needs to be located less than 1" from the drain of the power MOSFET. We recommend the following guidelines for the amount of bulk input capacitance:
    - For an output load of <10A use 2 X 1500µF caps.
    - For an output load of >10A use 3 X 1500µF caps.
  - The output bulk capacitors should be located as close to the CPU socket as possible. We recommend the following guidelines for the amount of bulk output capacitance:
    - For Pentium Pro use 4 X 1500µF.
    - For P55C MMX Pentium/ AMD K6 use 2X 1500µF.
    - For Pentium II use 7 X 1500µF.

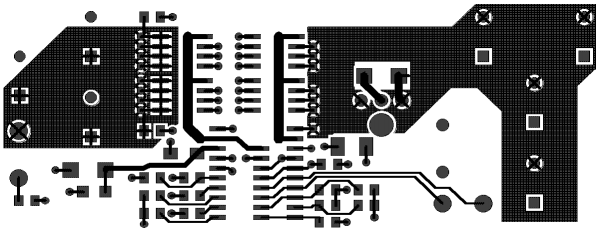
- **Inductor Location.**
  The inductor should be located near to the Source of the Power MOSFET. The ideal condition would be to use an internal power plane to connect the Source of the power MOSFET, the inductor, and the flyback schottky diode together.
- **Sense Resistor.**
  - The sense resistor should be located next to the inductor.
  - The two traces that run from the sense resistor to the RC50XX controller IC should be minimum width traces and be run parallel to each other. We recommend these sense resistor values:
    - For Pentium Pro use 0.006Ω.
    - For P55C MMX Pentium/ AMD K6 use 0.007Ω.
    - For Pentium II use 0.006Ω.
- **Ground Plane.**
  The RC50XX controller IC have a continuous ground plane running underneath the entire chip area. Each of the IC ground pins should have a separate via connection down into the ground plane.
- **Input Filter.**
  In many high current DC-DC converter designs, it is advisable to add an input inductor in order to create an input filter. An inductor on the order of 1-3uH is usually all that is required to perform the filter. When this component is added to the circuit, it is important that the RC50XX controller IC receive its VCC power from the system side of the input inductor and not the “dirty” side of the inductor. (ie the side that is connected to the power MOSFET drains)
- **To Minimize Electromagnetic Interference (EMI).**
  - Avoid long ground connections. Connect directly to the ground plane.
  - Use a star ground, where all grounds are connected to one point.
  - Use good quality inductors such as torrids or pot cores. Avoid rod inductors.
  - Route the high current carrying traces as power planes where possible.
  - Keep sensitive low-level signals away from the active switching components. Try to route them using the ground plane as a shield.

Example of a PC Motherboard Layout and Gerber File

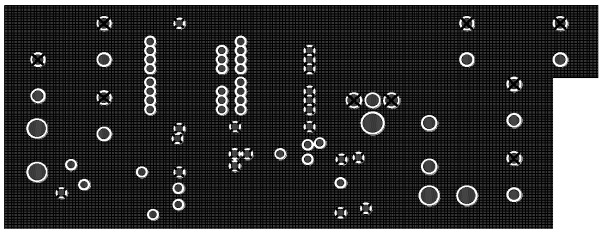
A reference design for motherboard implementation of the RC5050 along with the Layout Gerber File and Silk Screen are presented below. The actual PCAD Gerber File can be obtained from a Fairchild Semiconductor local Sales Office or from Marketing at 650-966-7734.

RC5050 Evaluation Board

Fairchild Semiconductor provides an evaluation board for the purpose of verifying the system level performance of the RC5050. The evaluation board serves as a guide as to what can be expected in performance with the supplied external components and PCB layout. Please call your local Sales Office or Fairchild Semiconductor Marketing department at 650-966-7734 for an evaluation board.



TOP



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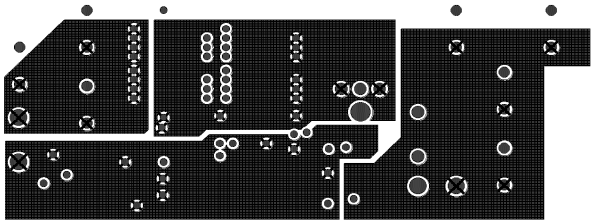
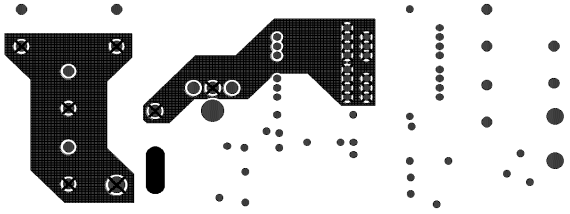
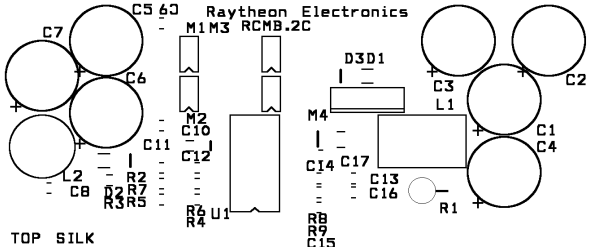


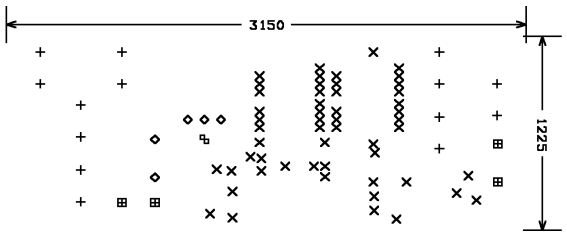
POWER



BOTTOM



TOP SILK

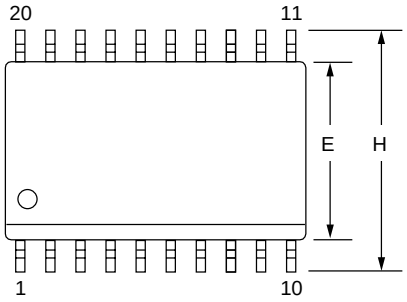


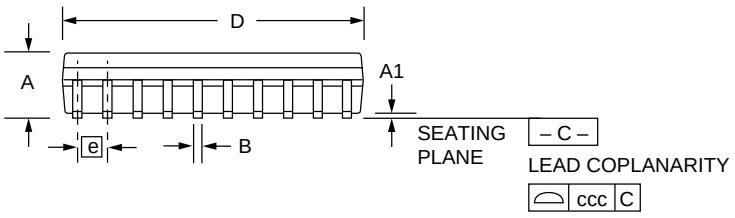
Mechanical Dimensions – 20 Lead SOIC

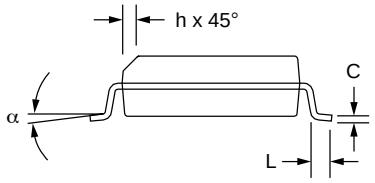
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.496	.512	12.60	13.00	2
E	.291	.299	7.40	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.029	0.25	0.75	
L	.016	.050	0.40	1.27	3
N	20		20		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Ordering Information

Product Number	Package
RC5050M	20 pin SOIC

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

5/20/98 0.0m 001
Stock#DS30005050

RC5051

Programmable Synchronous DC-DC Controller for Low Voltage Microprocessors

Features

- Programmable output from 1.3V to 3.5V using an integrated 5-bit DAC
- 85% efficiency typical
- Adjustable operation from 80KHz to 1MHz
- Integrated Power Good and Enable functions
- Overvoltage protection
- Overcurrent protection
- Drives N-channel MOSFETs
- 20 pin SOIC package
- Meets Intel Pentium II specifications using minimum number of external components

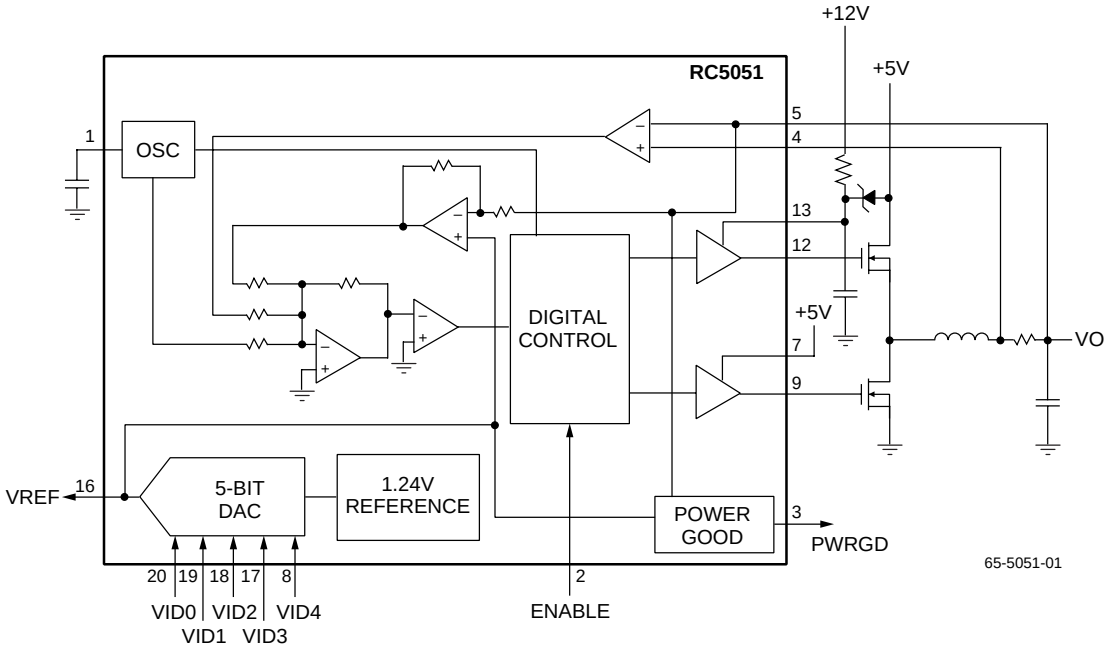
Applications

- Power supply for Pentium® II
- VRM for Pentium II processor
- Programmable step-down power supply

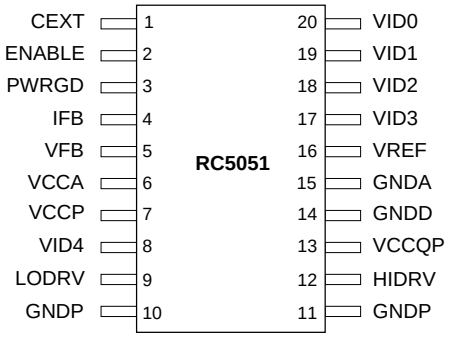
Description

The RC5051 is a synchronous mode DC-DC controller IC which provides an accurate, programmable output voltage for all Pentium II CPU applications. The RC5051 uses a 5-bit D/A converter to program the output voltage from 1.3V to 3.5V. The RC5051 uses a high level of integration to deliver load currents in excess of 19A from a 5V source with minimal external circuitry. Synchronous-mode operation offers optimum efficiency over the entire specified output voltage range, and the internal oscillator can be programmed from 80KHz to 1MHz for additional flexibility in choosing external components. An on-board precision low TC reference achieves tight tolerance voltage regulation without expensive external components. The RC5051 also offers integrated functions including Power Good, Output Enable, over-voltage protection and current limiting.

Block Diagram



Pin Assignments



65-5051-02

Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	CEXT	**Oscillator Capacitor Connection**. Connecting an external capacitor to this pin sets the internal oscillator frequency. Layout of this pin is critical to system performance. See Application Information for details.
2	ENABLE	**Output Enable**. A logic LOW on this pin will disable the output. An internal pull-up resistor allows for either open collector or TTL compatibility.
3	PWRGD	**Power Good Flag**. An open collector output that will be at logic LOW if the output voltage is not within ±12% of the nominal output voltage setpoint.
4	IFB	**High Side Current Feedback**. Pins 4 and 5 are used as the inputs for the current feedback control loop. Layout of these traces is critical to system performance. See Application Information for details.
5	VFB	**Voltage Feedback**. Pin 5 is used as the input for the voltage feedback control loop and as the low side current feedback input. See Application Information for details regarding correct layout.
6	VCCA	**Analog VCC**. Connect to system 5V supply and decouple with a 0.1μF ceramic capacitor.
7	VCCP	**Power VCC for low side FET driver**. Connect to system 5V supply and place a 1μF ceramic capacitor for decoupling and local charge storage.
8	VID4	**VID4 Input**. A logic 1 on this open collector/TTL input will enable the VID3–VID0 inputs to set the output from 2.1V to 3.5V, and a logic 0 will set the output from 1.3V to 2.05V, as shown in Table 1. Pullup resistors are internal to the controller.
9	LODRV	**Low Side FET Driver**. Connect this pin to the gate of an N-channel MOSFET for synchronous operation. The trace from this pin to the MOSFET gate should be < 0.5".
10, 11	GNDP	**Power Ground**. Return pin for high currents flowing in pins 7 and 13 (VCCP and VCCQP). Connect to a low impedance ground.
12	HIDRV	**High Side FET Driver**. Connect this pin to the gate of an N-channel MOSFET. The trace from this pin to the MOSFET gate should be < 0.5".
13	VCCQP	**Power VCC**. For high side FET driver. VCCQP must be connected to a voltage of at least VCCA + $V_{GS,ON}$ (MOSFET), and place a 1μF ceramic capacitor for decoupling and local charge storage. See Application Information for details
14	GNDD	**Digital Ground**. Return path for digital logic. Connect to a low impedance system ground plane to minimize ground loops.
15	GNDA	**Analog Ground**. Return path for low power analog circuitry. This pin should be connected to a low impedance system ground plane to minimize ground loops.
16	VREF	**Reference Voltage Test point**. This pin provides access to the DAC output and should be decoupled to ground using 0.1μF capacitor. No load should be connected.
17-20	VID0-VID3	**Voltage Identification Code Inputs**. These open collector/TTL compatible inputs will program the output voltage over the ranges specified in Table 1. Pull-up resistors are internal to the controller.

Absolute Maximum Ratings

Supply Voltages, VCCA, VCCP, VCCQP to GND	13V
Supply Voltage VCCQP, Charge Pump (V_{IN}+VCCA)	18V
Voltage Identification Code Inputs, VID4-VID0	13V
Junction Temperature, T_J	150°C
Storage Temperature	-65 to 150°C
Lead Soldering Temperature, 10 seconds	300°C

Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Voltage, VCCA, VCCP		4.75	5	5.25	V
Input Logic HIGH		2.0			V
Input Logic LOW				0.8	V
Ambient Operating Temp		0		70	°C
Output Driver Supply, VCCQP		8.5		12	V
PWRGD threshold	Logic High Logic Low	93 88		107 112	%V_{OUT} %V_{OUT}

Electrical Specifications

(V_{CCA} = 5V, V_{OUT} = 2.8V, f_{osc} = 300 KHz, and T_A = +25°C using circuit in Figure 1, unless otherwise noted)
The • denotes specifications which apply over the full operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
Output Voltage	See Table 1	•	1.3		3.5	V
Output Current				15		A
Initial Voltage Setpoint	I_{LOAD} = 0.8A, V_{OUT} = 2.8V V_{OUT} = 2.0V		2.797 2.000	2.825 2.020	2.853 2.040	V V
Output Temperature Drift	T_A = 0 to 70°C V_{OUT} = 2.8V V_{OUT} = 2.0V	• •		+16 +11		mV mV
Load Regulation	I_{LOAD} = 0.8A to 14.2A	•		-20		mV
Line Regulation	V_{IN} = 4.75V to 5.25V	•		±2		mV
Output Ripple	20MHz BW, I_{LOAD} = 14.2A			±13		mVpk
Total Output Variation Steady State[1]	V_{OUT} = 2.8V V_{OUT} = 2.0V	• •	2.740 1.940		2.900 2.060	V V
Total Output Variation Transient[2]	I_{LOAD} = 0.8 to 14.2A, V_{OUT} = 2.8V V_{OUT} = 2.0V	• •	2.670 1.900		2.930 2.100	V V
Short Circuit Detect Threshold		•	100	120	140	mV
Efficiency	I_{LOAD} = 14.2A, V_{OUT} = 2.8V	•		82		%
Output Driver Rise and Fall Time	See Figure 2			80		nsec
Output Driver Deadtime 1	See Figure 2			5		%/f_{OSC}
Output Driver Deadtime 2	See Figure 2			80		nsec
Turn-on Response Time	I_{LOAD} = 0A to 14.2A				10	msec
Oscillator Range			80		1000	KHz
Oscillator Frequency	C_{EXT} = 100 pF		270	300	330	KHz
Max Duty Cycle			90	95		%

Notes:

1. Steady Date Voltage Regulation includes Initial Voltage Setpoint, Load Regulation, Output Ripple and Output Temperature Drift and is measured at the converter's output capacitors.
2. As measured at the converter's output capacitors. For motherboard applications, the PCB layout should exhibit no more than 0.5mΩ trace resistance between the converter's output capacitors and the CPU.

Table 1. Output Voltage Programming Codes

VID4	VID3	VID2	VID1	VID0	V_{OUT} to CPU
0	1	1	1	1	1.30V
0	1	1	1	0	1.35V
0	1	1	0	1	1.40V
0	1	1	0	0	1.45V
0	1	0	1	1	1.50V
0	1	0	1	0	1.55V
0	1	0	0	1	1.60V
0	1	0	0	0	1.65V
0	0	1	1	1	1.70V
0	0	1	1	0	1.75V
0	0	1	0	1	1.80V
0	0	1	0	0	1.85V
0	0	0	1	1	1.90V
0	0	0	1	0	1.95V
0	0	0	0	1	2.00V
0	0	0	0	0	2.05V
1	1	1	1	1	No CPU
1	1	1	1	0	2.1V
1	1	1	0	1	2.2V
1	1	1	0	0	2.3V
1	1	0	1	1	2.4V
1	1	0	1	0	2.5V
1	1	0	0	1	2.6V
1	1	0	0	0	2.7V
1	0	1	1	1	2.8V
1	0	1	1	0	2.9V
1	0	1	0	1	3.0V
1	0	1	0	0	3.1V
1	0	0	1	1	3.2V
1	0	0	1	0	3.3V
1	0	0	0	1	3.4V
1	0	0	0	0	3.5V

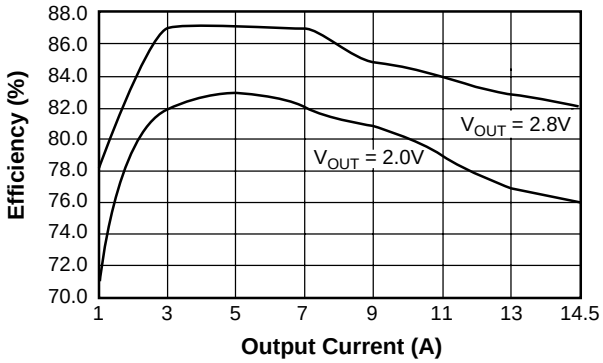
Note:

1. 0 = processor pin is tied to GND.
   1 = processor pin is open.

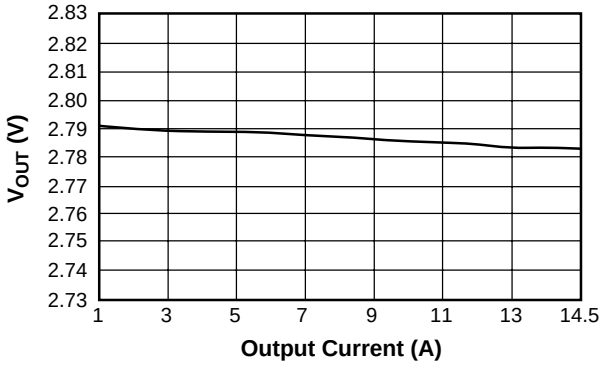
Typical Operating Characteristics

(VCCA, VCCD = 5V, f_{OSC} = 280 KHz, and T_A = +25°C using circuit in Figure 1, unless otherwise noted)

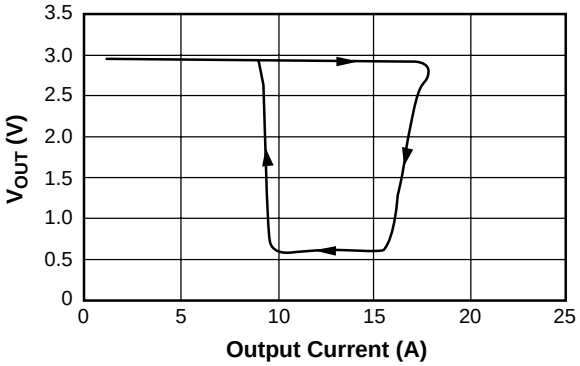
Efficiency vs. Output Current



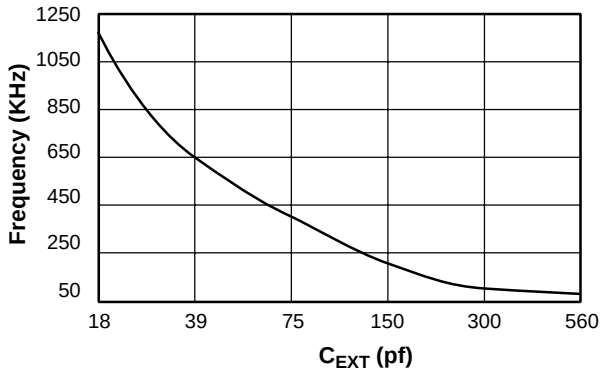
Load Regulation, V_{OUT} = 2.8 V



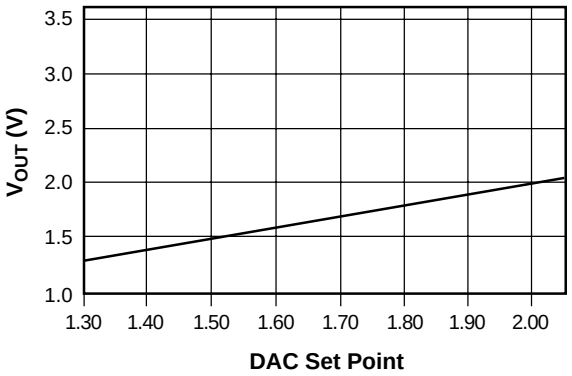
Output Voltage vs. Output Current, R_{SENSE} = 6mΩ



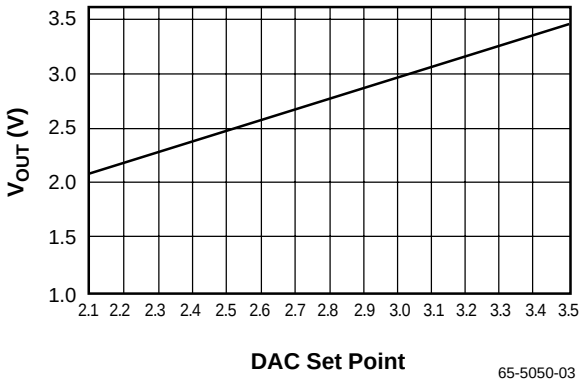
Oscillator Frequency vs. C_{EXT}



Output Programming, VID4 = 0



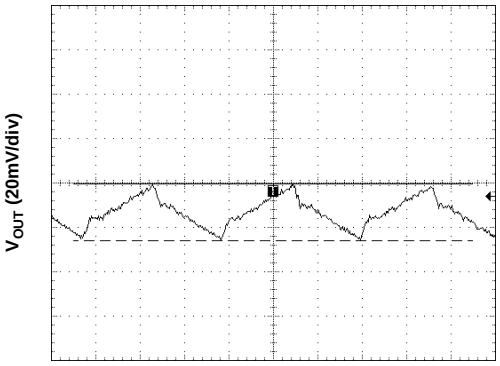
Output Programming, VID4 = 1



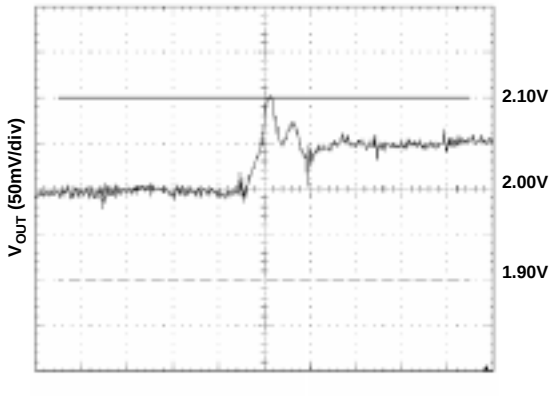
65-5050-03

Typical Operating Characteristics (continued)

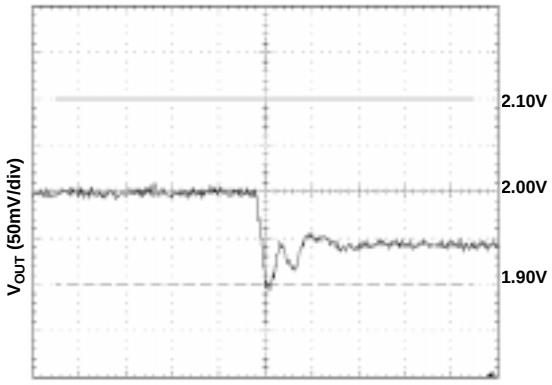
Output Ripple, 2.8V @ 14.2A



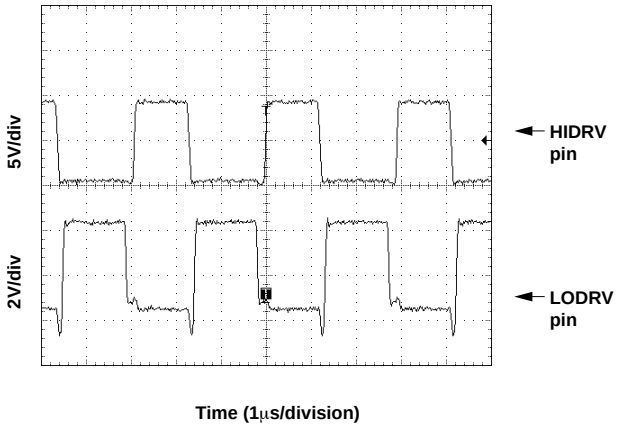
Transient Response, 14.2A to 0.8A



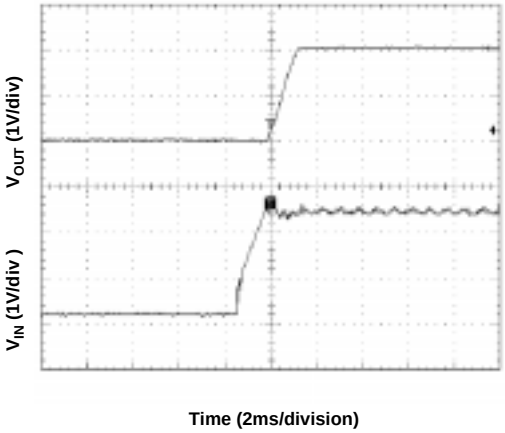
Transient Response, 0.8A to 14.2A



Switching Waveforms, 9A Load

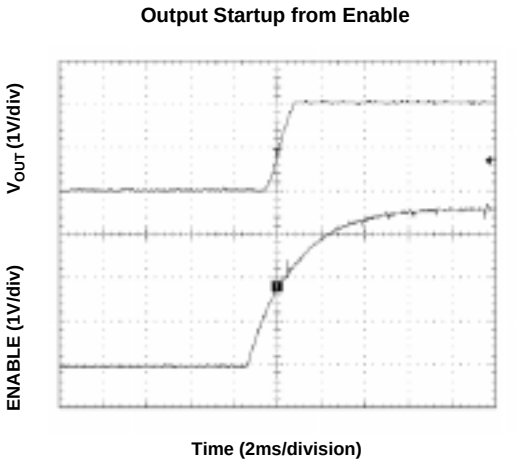


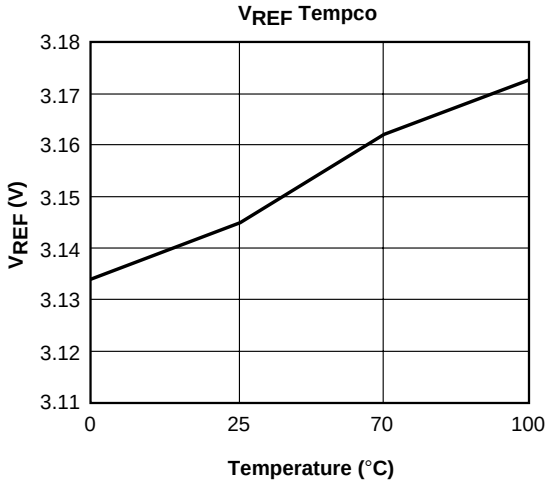
Output Startup, System Power-up



65-5051-12

Typical Operating Characteristics (continued)





Application Circuit

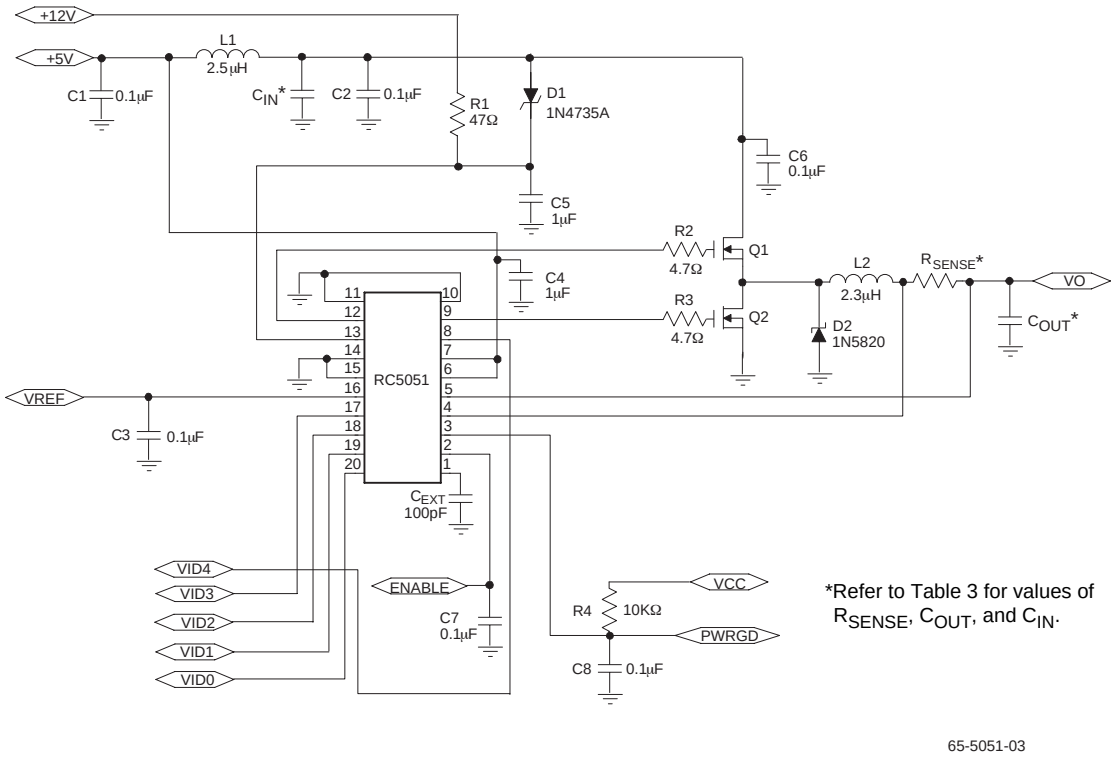


Figure 1. 15A Application Circuit for Pentium II Processors

Table 2. RC5051 Application Bill of Materials for Intel Pentium II Processors

Reference	Manufacturer Part #	Quantity	Description	Requirements/Comments
C1–3, C6–C8	Panasonic ECU-V1H104ZFX	6	100nF, 50V Capacitor	
C4–5	Panasonic ECU-V1C105ZFX	2	1μF, 16V Capacitor	
C_{ext}	Panasonic ECU-V1H101JCG	1	100pF Capacitor	5%, C0G
C_{IN}	Sanyo 10MV1200GX	*	1200μF, 10V Electrolytic	I_{RMS} = 2A
C_{OUT}	Sanyo 6MV1500GX	*	1500μF, 6.3V Electrolytic	ESR < 44mΩ
D1	Motorola 1N4735A	1	6.2V Zener Diode	
D2	Motorola 1N5820	1	3A Schottky Diode	
L1	Skynet 320-6110	1	2.5μH, 11A Inductor	DCR ~ 6mΩ See Note 1.
L2	Any	1	2.3μH, 15A inductor	DCR ~ 3mΩ
Q1–2	Fairchild FDP6030L or FDB6030L	2	N-Channel MOSFET (TO-220 or TO-263)	$R_{DS(ON)}$ = 20mΩ @ V_{GS} = 4.5V See Note 2
R1	Any	1	47Ω	
R2-3	Any	2	4.7Ω	
R4	Any	1	10KΩ	
R_{SENSE}	Fairchild RC10-XX*	1	CuNi Alloy Wire Resistor	
U1	Fairchild RC5051M	1	DC/DC Controller	

* See Table 3.

Notes:

1. Inductor L1 is recommended to isolate the 5V input supply from noise generated by the MOSFET switching, and to comply with Intel dl/dt requirements. L1 may be omitted if desired.
2. For 14.2A designs using the FDP6030L MOSFETs, heatsinks with thermal resistance Θ_{SA} < 20°C/W should be used. For details and a spreadsheet on MOSFET selections, refer to Applications Bulletin AB-8.

Table 3. Recommended Values for CPU-based Applications

Application	Output Current	C_{IN}	C_{OUT}*	C_{OUT} Maximum ESR*	R_{SENSE}
300MHz AMD K6 Motherboard	13A	3 x 1200μF, 10V Sanyo 10MV1200GX	2 x 1500μF, 6.3V Sanyo 6MV1500GX	6.1mΩ	5.8mΩ
300 MHz Intel Pentium Motherboard	14.2A	3 x 1200μF, 10V Sanyo 10MV1200GX	7 x 1500μF, 6.3V Sanyo 6MV1500GX	6.8mΩ	5.2mΩ
400MHz Intel Pentium II Motherboard	12.6A	3 x 1200μF, 10V Sanyo 10MV1200GX	7 x 1500μF, 6.3V Sanyo 6MV1500GX	6.3mΩ	5.8mΩ

* Output capacitance and ESR requirements depend critically on layout and processor type. Consult Application Bulletin AB-14 for details

Test Circuit

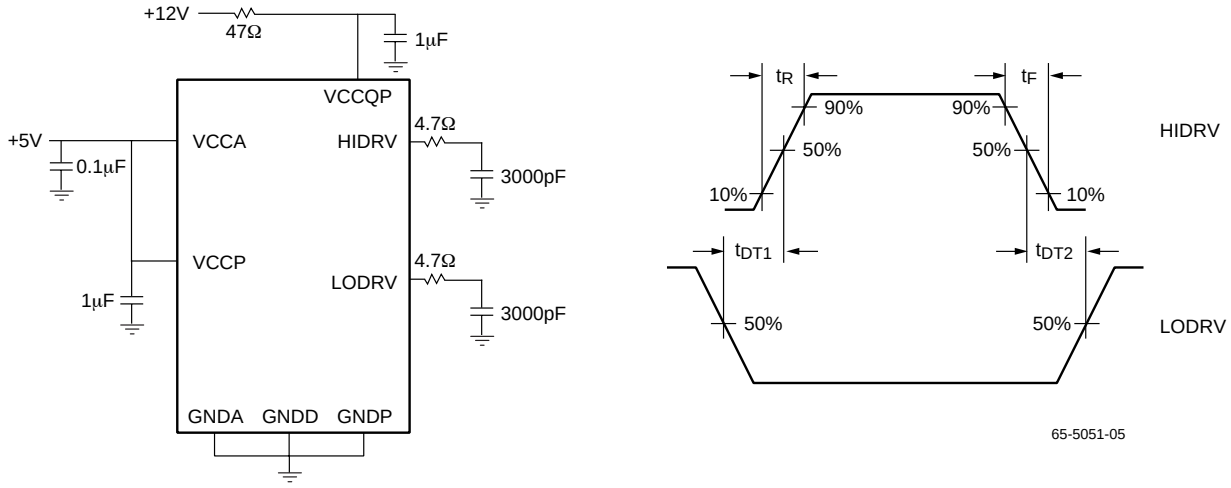


Figure 2. Output Drive Test Circuit and Timing Diagram

Application Information

The RC5051 Controller

The RC5051 is a programmable synchronous DC-DC controller IC. When designed around the appropriate external components, the RC5051 can be configured to deliver more than 19A of output current, as appropriate for the Klamath and Deschutes and other processors. The RC5051 functions as a fixed frequency PWM step down regulator.

Main Control Loop

Refer to the RC5051 Block Diagram on page 1. The RC5051 implements “summing mode control”, which is different from both classical voltage-mode and current-mode control. It provides superior performance to either by allowing a large converter bandwidth over a wide range of output loads.

The control loop of the regulator contains two main sections: the analog control block and the digital control block. The analog section consists of signal conditioning amplifiers feeding into a set of comparators which provide the inputs to the digital control block. The signal conditioning section accepts inputs from the IFB (current feedback) and VFB (voltage feedback) pins and sets up two controlling signal paths. The first, the voltage control path, amplifies the difference between the VFB signal the reference voltage from the DAC and presents the output to one of the summing amplifier inputs. The second, current control path, takes the difference between the IFB and VFB pins and presents the resulting signal to another input of the summing amplifier. These two signals are then summed together with the slope compensation input from the oscillator. This output is then presented to a comparator, which provides the main PWM control signal to the digital control block.

The digital control block takes the analog comparator inputs and the main clock signal from the oscillator to provide the appropriate pulses to the HIDRV and LODRV output pins. These two outputs control the external power MOSFETs. The digital block utilizes high speed Schottky transistor logic, allowing the RC5051 to operate at clock speeds as high as 1MHz.

There are additional comparators in the analog control section whose function is to set the point at which the RC5051 enters its pulse skipping mode during light loads, as well as the point at which the current limit comparator disables the output drive signals to the external power MOSFETs.

High Current Output Drivers

The RC5051 contains two identical high current output drivers that utilize high speed bipolar transistors in a push-pull configuration. The drivers’ power and ground are separated from the chip’s power and ground for switching noise immunity. The HIDRV driver has a power supply pin, VCCQP, which is supplied from an external 12V source through a series resistor or from a charge-pump circuit powered from 5V if 12V is not available. The LODRV driver has a power supply pin, VCCP, which can be supplied from either the 12V or 5V source. The resulting voltages are sufficient to provide the gate to source drive to the external MOSFETs required in order to achieve a low $R_{DS,ON}$.

Internal Voltage Reference

The reference included in the RC5051 is a precision bandgap voltage reference. Its internal resistors are precisely trimmed to provide a near zero temperature coefficient (TC). Based on the reference is the output from an integrated 5-bit DAC. The DAC monitors the 5 voltage identification pins, VID0–VID4. When the VID4 pin is at logic HIGH, the DAC scales the reference voltage from 2.0V to 3.5V in 100mV increments. When VID4 is pulled LOW, the DAC scales the reference from 1.30V to 2.05V in 50mV increments. All VID codes are available, including those below 1.80V. For guaranteed stable operation under all loading conditions, 0.1μF of decoupling capacitance should be connected to the VREF pin. No load should be connected to VREF.

Power Good (PWRGD)

The RC5051 Power Good function is designed in accordance with the Pentium II DC-DC converter specifications and provides a continuous voltage monitor on the VFB pin. The circuit compares the VFB signal to the VREF voltage and outputs an active-low interrupt signal to the CPU should the power supply voltage deviate more than ±12% of its nominal setpoint. The Power Good flag provides no other control function to the RC5051.

Output Enable (ENABLE)

The RC5051 will accept an open collector/TTL signal for controlling the output voltage. The low state disables the output voltage. When disabled, the PWRGD output is in the low state. If an enable is not required in the circuit, this pin may be left open.

Over-Voltage Protection

The RC5051 constantly monitors the output voltage for protection against over voltage conditions. If the voltage at the VFB pin exceeds 20% of the selected program voltage, an over-voltage condition is assumed and the RC5051 disables the output drive signal to the external MOSFETs. The DC-DC converter returns to normal operation after the fault has been removed.

Over-Current Protection

Current sense is implemented in the RC5051 to reduce the duty cycle of the output drive signal to the MOSFETs when an over-current condition is detected. The voltage drop created by the output current flowing across a sense resistor is presented to an internal comparator. When the voltage

developed across the sense resistor exceeds the 120mV comparator threshold voltage, the RC5051 reduces the output duty cycle to help protect the power devices. The DC-DC converter returns to normal operation after the fault has been removed.

Oscillator

The RC5051 oscillator section uses a fixed current capacitor charging configuration. An external capacitor (CEXT) is used to set the oscillator frequency between 80KHz and 1MHz. This scheme allows maximum flexibility in choosing external components.

In general, a higher operating frequency decreases the peak ripple current flowing in the output inductor, thus allowing the use of a smaller inductor value. In addition, operation at higher frequencies decreases the amount of energy storage that must be provided by the bulk output capacitors during load transients due to faster loop response of the controller.

Unfortunately, the efficiency losses due to switching of the MOSFETs increase as the operating frequency is increased. Thus, efficiency is optimized at lower frequencies. An operating frequency of 300KHz is a typical choice which optimizes efficiency and minimizes component size while maintaining excellent regulation and transient performance under all operating conditions.

Design Considerations and Component Selection

Additional information on design and component selection may be found in Fairchild Semiconductor's Application Note 53.

MOSFET Selection

This application requires N-channel Logic Level Enhancement Mode Field Effect Transistors. Desired characteristics are as follows:

- Low Static Drain-Source On-Resistance, $R_{DS,ON}$ < 20mΩ (lower is better)
- Low gate drive voltage, V_{GS} = 4.5V rated
- Power package with low Thermal Resistance
- Drain-Source voltage rating > 15V.

The on-resistance ($R_{DS,ON}$) is the primary parameter for MOSFET selection. The on-resistance determines the power dissipation within the MOSFET and therefore significantly affects the efficiency of the DC-DC Converter. For details and a spreadsheet on MOSFET selection, refer to Applications Bulletin AB-8

MOSFET Gate Bias

The high side MOSFET gate driver can be biased by one of two methods–Charge Pump or 12V Gate Bias. The charge pump method has the advantage of requiring only +5V as an input voltage to the converter, but the 12V method will realize increased efficiency by providing an increased V_{GS} to the high side MOSFETs.

Method 1. Charge Pump (Bootstrap)

Figure 3 shows the use of a charge pump to provide gate bias to the high side MOSFET when +12V is unavailable. Capacitor CP is the charge pump used to boost the voltage of the RC5051 output driver. When the MOSFET Q1 switches off, the source of the MOSFET is at approximately 0V because of the MOSFET Q2. (The Schottky D2 conducts for only a very short time, and is not relevent to this discussion.) CP is charged through the Schottky diode D1 to approximately 4.5V. When the MOSFET Q1 turns on, the voltage at the source of the MOSFET is equal to 5V. The capacitor voltage follows, and hence provides a voltage at VCCQP equal to almost 10V. The Schottky diode D1 is required to provide the charge path when the MOSFET is off, and reverses biases when VCCQP goes to 10V. The charge pump capacitor (CP) needs to be a high Q, high frequency capacitor. A 1μF ceramic capacitor is recommended here.

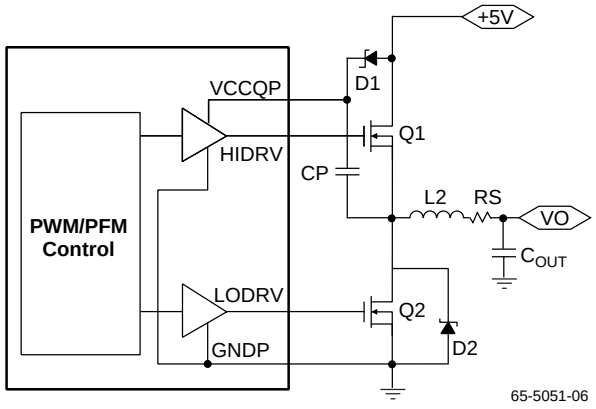


Figure 3. Charge Pump Configuration

Method 2. 12V Gate Bias

Figure 4 illustrates how a 12V source can be used to bias VCCQP. A 47Ω resistor is used to limit the transient current into the VCCQP pin and a 1μF capacitor is used to filter the VCCQP supply. This method provides a higher gate bias voltage (V_{GS}) to the high side MOSFET than the charge pump method, and therefore reduces the $R_{DS,ON}$ and the resulting power loss within the MOSFET. In designs where efficiency is a primary concern, the 12V gate bias method is recommended. A 6.2V Zener diode, D1, is used to clamp the voltage at VCCQP to a maximum of 12V and ensure that the absolute maximum voltage of the IC will not be exceeded.

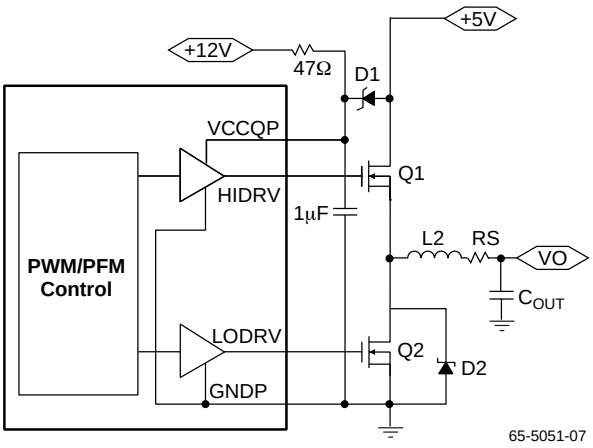


Figure 4. Gate Bias Configuration

Inductor Selection

Choosing the value of the inductor is a tradeoff between allowable ripple voltage and required transient response. The system designer can choose any value within the allowed minimum to maximum range in order to either minimize ripple or maximize transient performance. The first order equation (close approximation) for minimum inductance is:

$$L_{min} = \frac{(V_{in} - V_{out})}{f} \times \frac{V_{out}}{V_{in}} \times \frac{ESR}{V_{ripple}}$$

where:

V_{in} = Input Power Supply
V_{out} = Output Voltage
f = DC/DC converter switching frequency
ESR = Equivalent series resistance of all output capacitors in parallel
V_{ripple} = Maximum peak to peak output ripple voltage budget.

The first order equation for maximum allowed inductance is:

$$L_{max} = 2C_O \times \frac{(V_{in} - V_{out})D_m V_{tb}}{I_{PP}^2}$$

where:

C_o = The total output capacitance
I_{pp} = Maximum to minimum load transient current
V_{tb} = The output voltage tolerance budget allocated to load transient
D_m = Maximum duty cycle for the DC/DC converter (usually 95%).

Some margin should be maintained away from both L_{min} and L_{max}. Adding margin by increasing L almost always adds expense since all the variables are predetermined by system performance except for C_o, which must be increased to increase L. Adding margin by decreasing L can either be done by purchasing capacitors with lower ESR or by increasing the DC/DC converter switching frequency. The RC5051 is capable of running at high switching frequencies and provides significant cost savings for the newer CPU systems that typically run at high supply current.

RC5051 Short Circuit Current Characteristics

The RC5051 short circuit current characteristic includes a hysteresis function that prevents the DC-DC converter from oscillating in the event of a short circuit. Figure 5 shows the typical characteristic of the DC-DC converter circuit with a 6.8 mΩ sense resistor. The converter exhibits a normal load regulation characteristic until the voltage across the resistor exceeds the internal short circuit threshold of 120mV (= 17.5A * 6.8mΩ). At this point, the internal comparator trips and signals the controller to reduce the converter's duty cycle to approximately 20%. This causes a drastic reduction in the output voltage as the load regulation collapses into the short circuit control mode. With a 40mΩ output short, the voltage is reduced to 15A * 40mΩ = 600mV. The output voltage does not return to its nominal value until the output current is reduced to a value within the safe operating range for the DC-DC converter.

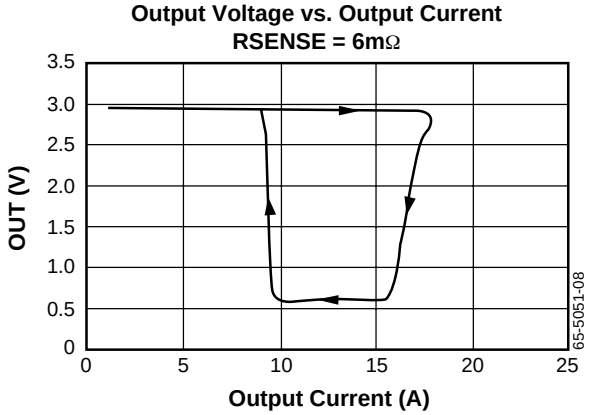


Figure 5. RC5051 Short Circuit Characteristic

Schottky Diode Selection

The application circuit of Figure 1 shows a Schottky diode, D2, which is used as a free-wheeling diode to assure that the body-diode in Q2 does not conduct when the upper MOSFET is turning off and the lower MOSFET is turning on. It is undesirable for this diode to conduct because its high forward voltage drop and long reverse recovery time degrades efficiency, and so the Schottky provides a shunt path for the current. Since this time duration is very short, the selection criterion for the diode is that the forward voltage of the Schottky at the output current should be less than the forward voltage of the MOSFET's body diode.

Output Filter Capacitors

The output bulk capacitors of a converter help determine its output ripple voltage and its transient response. It has already been seen in the section on selecting an inductor that the ESR helps set the minimum inductance, and the capacitance value helps set the maximum inductance. For most converters, however, the number of capacitors required is

determined by the transient response and the output ripple voltage, and these are determined by the ESR and not the capacitance value. That is, in order to achieve the necessary ESR to meet the transient and ripple requirements, the capacitance value required is already very large.

The most commonly used choice for output bulk capacitors is aluminum electrolytics, because of their low cost and low ESR. The only type of aluminum capacitor used should be those that have an ESR rated at 100kHz. Consult Application Bulletin AB-14 for detailed information on output capacitor selection.

The output capacitance should also include a number of small value ceramic capacitors placed as close as possible to the processor; 0.1µF and 0.01µF are recommended values.

Input Filter

The DC-DC converter design may include an input inductor between the system +5V supply and the converter input as shown in Figure 6. This inductor serves to isolate the +5V supply from the noise in the switching portion of the DC-DC converter, and to limit the inrush current into the input capacitors during power up. A value of 2.5µH is recommended.

It is necessary to have some low ESR aluminum electrolytic capacitors at the input to the converter. These capacitors deliver current when the high side MOSFET switches on. Figure 6 shows 3 x 1000µF, but the exact number required will vary with the speed and type of the processor. For the top speed Klamath and Deschutes, the capacitors should be rated to take 7A of ripple current. Capacitor ripple current rating is a function of temperature, and so the manufacturer should be contacted to find out the ripple current rating at the expected operational temperature. For details on the design of an input filter, refer to Applications Bulletin AB-15.

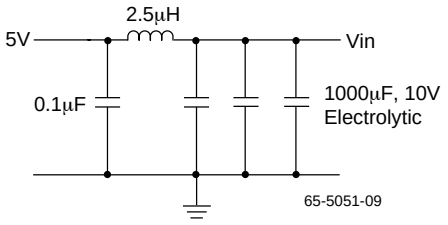


Figure 6. Input Filter

Droop Resistor

Figure 7 shows a converter using a “droop resistor”, R_D. The function of the droop resistor is to improve the transient response of the converter, potentially reducing the number of output capacitors required. In operation, the droop resistor causes the output voltage to be slightly lower at heavy load current than it otherwise would be. When the load transitions from heavy to light current, the output can swing up farther without exceeding limits, because it started from a lower voltage, thus reducing the capacitor requirements.

.

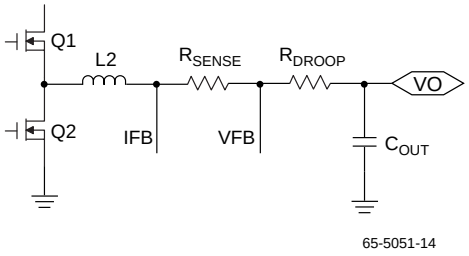


Figure 7. Use of a Droop Resistor

PCB Layout Guidelines

- Placement of the MOSFETs relative to the RC5051 is critical. Place the MOSFETs such that the trace length of the HIDRV and LODRV pins of the RC5051 to the FET gates is minimized. A long lead length on these pins will cause high amounts of ringing due to the inductance of the trace and the gate capacitance of the FET. This noise radiates throughout the board, and, because it is switching at such a high voltage and frequency, it is very difficult to suppress.
- In general, all of the noisy switching lines should be kept away from the quiet analog section of the RC5051. That is, traces that connect to pins 9, 12, and 13 (LODRV, HIDRV and VCCQP) should be kept far away from the traces that connect to pins 1 through 5, and pin 16.
- Place the 0.1µF decoupling capacitors as close to the RC5051 pins as possible. Extra lead length on these reduces their ability to suppress noise.
- Each VCC and GND pin should have its own via to the appropriate plane. This helps provide isolation between pins.
- Surround the CEXT timing capacitor with a ground trace. Be sure to place a ground or power plane underneath the capacitor for further noise isolation, in order to provide additional shielding to the oscillator (pin 1) from the noise on the PCB. In addition, place this capacitor as close to pin 1 as possible.
- Place the MOSFETs, inductor, and Schottky as close together as possible for the same reasons as in the first bullet above. Place the input bulk capacitors as close to the drains of the high side MOSFETs as possible. In addition, placement of a 0.1µF decoupling cap right on the drain of each high side MOSFET helps to suppress some of the high frequency switching noise on the input of the DC-DC converter.
- Place the output bulk capacitors as close to the CPU as possible to optimize their ability to supply instantaneous current to the load in the event of a current transient. Additional space between the output capacitors and the CPU will allow the parasitic resistance of the board traces to degrade the DC-DC converter’s performance under severe load transient conditions, causing higher voltage deviation. For more detailed information regarding capacitor placement, refer to Application Bulletin AB-5.

- The traces that run from the RC5051 IFB (pin 4) and VFB (pin 5) pins should be run together next to each other and Kelvin connected to the sense resistor. Running these lines together rejects some of the common mode noise that is presented to the RC5051 feedback input. Try, as much as possible, to run the noisy switching signals (HIDRV, LODRV & VCCQP) on one layer, but use the inner layers for power and ground only. If the top layer is being used to route all of the noisy switching signals, use the bottom layer to route the analog sensing sign VFB and IFB.
- A PC Board Layout Checklist is available from Fairchild Applications. Ask for Application Bulletin AB-11.

PC Motherboard Sample Layout and Gerber File

A reference design for motherboard implementation of the RC5051 along with the PCAD layout Gerber file and silk screen can be obtained from our marketing department at 650-968-9211 x 7833.

RC5051 Evaluation Board

Fairchild Semiconductor provides an evaluation board to verify the system level performance of the RC5051. It serves as a guide to performance expectations when using the supplied external components and PCB layout. Please call the marketing department at 650-968-9211 x 7833 for an evaluation board.

Additional Information

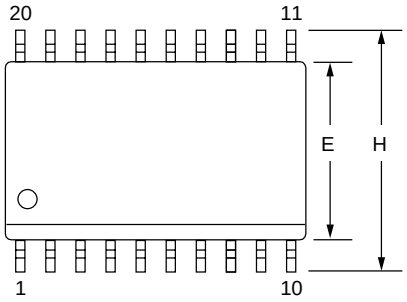
For additional information contact the Fairchild Semiconductor's Analog & Mixed Signal Products Group Marketing Department at 650-968-9211 x 7833.

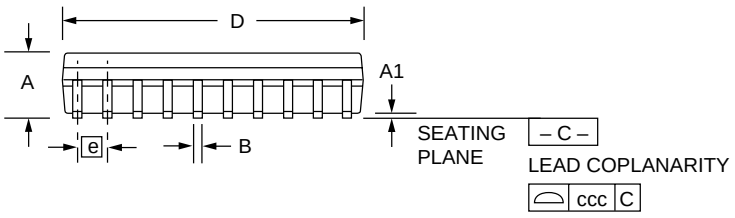
Mechanical Dimensions – 20 Lead SOIC

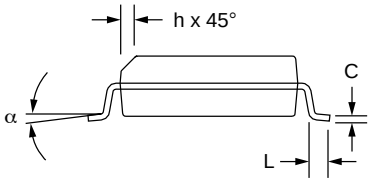
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.496	.512	12.60	13.00	2
E	.291	.299	7.40	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.029	0.25	0.75	
L	.016	.050	0.40	1.27	3
N	20		20		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Ordering Information

Product Number	Package
RC5051M	20 pin SOIC

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

6/4/98 0.0m 003
Stock#DS30005051

RC5052

High Performance Programmable Synchronous DC-DC Controller for Low Voltage Microprocessors

Features

- Programmable output from 1.3V to 3.5V using an integrated 5-bit DAC
- Remote sense
- Active Droop
- 85% efficiency typical at full load
- Integrated Power Good and Enable/Soft Start functions
- Drives N-channel MOSFETs
- Overcurrent protection using MOSFET sensing
- 20 pin SOIC package
- Meets Intel Pentium II specifications using minimum number of external components
- Adjustable deadtime, frequency
- Crowbar protection for overvoltage

Applications

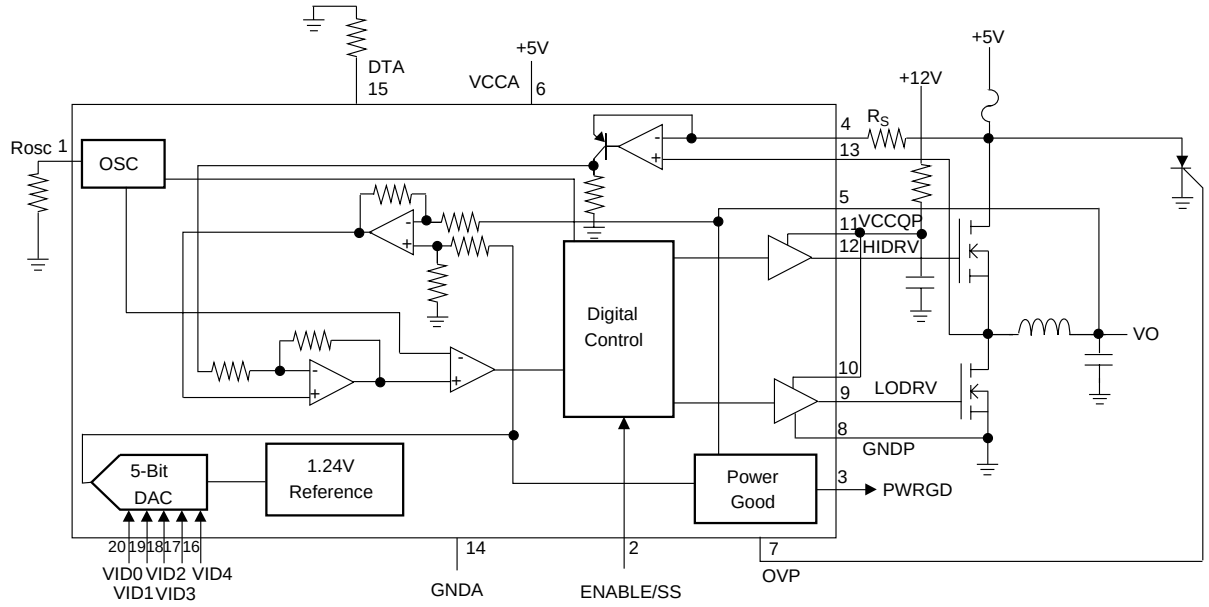
- Power supply for Pentium® II & III
- VRM for Pentium II & III processor
- Telecom line cards
- Routers, switches & hubs
- Programmable step-down power supply

Description

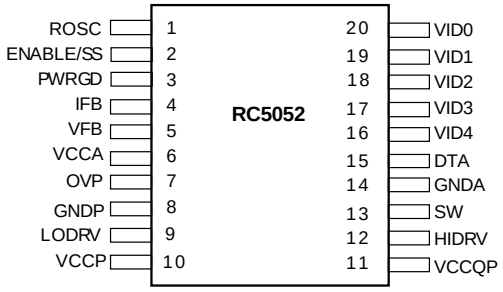
The RC5052 is a synchronous mode DC-DC controller IC which provides a highly accurate, programmable output voltage for all Pentium II & III CPU applications and other high-performance processors. The RC5052 features remote voltage sensing, adjustable current limit, and active droop for optimal converter transient response. The RC5052 uses a 5-bit D/A converter to program the output voltage from 1.3V to 3.5V. The RC5052 uses a high level of integration to deliver load currents in excess of 16A from a 5V source with minimal external circuitry. Synchronous-mode operation offers optimum efficiency over the entire specified output voltage range. An on-board precision low TC reference achieves tight tolerance voltage regulation without expensive external components, while active droop permits exact tailoring of voltage for the most demanding load transients. The RC5052 also offers integrated functions including Power Good, Output Enable/ Soft Start, current limiting, adjustable frequency, adjustable deadtime and overvoltage crowbar protection, and is available in a 20 pin SOIC package.

Preliminary Specification

Block Diagram



Pin Assignments



Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	ROSC	**Oscillator Resistor Connection.** Connect an external resistor to this pin to set the internal oscillator frequency. Layout of this pin is critical to system performance. See Application Information for details.
2	ENABLE/SS	**Output Enable/Soft Start.** A logic LOW on this pin will disable the output. An internal current source allows for open collector control. This pin also doubles as soft start.
3	PWRGD	**Power Good Flag.** An open collector output that will be logic LOW if the output voltage is not within ±12% of the nominal output voltage setpoint.
4	IFB	**Current Feedback.** Pin 4 is used in conjunction with pin 13, as the input for the current feedback control loop. Layout of these traces is critical to system performance. See Application Information for details.
5	VFB	**Voltage Feedback.** Pin 5 is used as the input for the voltage feedback control loop. See Application Information for details regarding correct layout.
6	VCCA	**Analog VCC.** Connect to system 5V supply and decouple with a 0.1µF ceramic capacitor.
7	OVP	**Over Voltage Protection.** This pin triggers the gate of an external SCR.
8	GNDP	**Power Ground.** Return pin for high currents flowing in pins 10 and 11. Connect to a low impedance ground.
9	LODRV	**Low Side FET Driver.** Connect this pin to the gate of an N-channel MOSFET for synchronous operation. The trace from this pin to the MOSFET gate should be <0.5".
10	VCCP	**Power VCC.** For low side FET driver. Connect to either system 12V supply or 5V supply, and decouple with a 4.7µF tantalum and a 0.1µF ceramic capacitor.
11	VCCQP	**High Side Power VCC.** For high side FET driver. Connect to system 12V supply, and decouple with a 4.7µF tantalum and a 0.1µF ceramic capacitor.
12	HIDRV	**High Side FET Driver.** Connect this pin to the gate of an N-channel MOSFET. The trace from this pin to the MOSFET gate should be <0.5".
13	SW	**High side driver source and low side driver drain switching node.** Together with IFB pin allows FET sensing for current.
14	GNDA	**Analog Ground.** Return path for low power analog circuitry. This pin should be connected to a low impedance system ground plane to minimize ground loops.
15	DTA	**Dead Time Adjust.** Connect an external resistor to this pin to set the dead time.
16–20	VID0-4	**Voltage Identification Code Inputs.** These open collector/TTL compatible inputs will program the output voltage over the ranges specified in Table 2. Pull-up resistors are internal to the controller.

Preliminary Specification

Absolute Maximum Ratings

Supply Voltages VCCA, VCCP, VCCQP to GND	13.5V
Supply Voltages (VCCQP, Charge Pump)	18V
Voltage Identification Code Inputs, VID0-VID4	VCCA
Junction Temperature, T_J	150°C
Storage Temperature	-65 to 150°C
Lead Soldering Temperature, 10 seconds	300°C
Power Dissipation, P_D	750mW
Thermal Resistance Junction-to-case, Θ_{JC}	105°C/W

Recommended Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Voltage VCCA		4.75	5	5.25	V
Input Logic HIGH		2.0			V
Input Logic LOW				0.8	V
Ambient Operating Temperature		0		70	°C
Output Driver Supply, VCCP & VCCQP		11.4	12	13.2	V

Preliminary Specification

Electrical Specifications (V_{CCA} = 5V, V_{CCP} = V_{CCQP} = 12V, V_{OUT} = 2.0V, and T_A = +25°C using circuit in Figure 1, unless otherwise noted.)

The • denotes specifications which apply over the full operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
Output Voltage	See Table 1	•	1.3		3.5	V
Output Current				18		A
Initial Voltage Setpoint	I_{LOAD} = 0.8A, V_{OUT} = 2.400V V_{OUT} = 2.000V V_{OUT} = 1.550V		2.397 2.000 1.550	2.424 2.020 1.565	2.454 2.040 1.580	V V V
Output Temperature Drift	T_A = 0 to 70°C, V_{OUT} = 2.000V V_{OUT} = 1.550V	• •		+8 +6		mV mV
Line Regulation	V_{CCA} = 4.75V to 5.25V, V_{OUT} = 2.000V	•		±2		mV
Internal Droop[3]	V_{OUT} at I_{LOAD} = 0.8A to I_{max}		-44	-40	-36	mV
Output Ripple	20MHz BW, I_{LOAD} = I_{max}			11		mVpk
Total Output Variation, Steady State[1]	V_{OUT} = 2.000V V_{OUT} = 1.550V[3]	• •	1.940 1.480		2.070 1.590	V
Total Output Variation, Transient[2]	I_{LOAD} = 0.8A to I_{max},V_{OUT} = 2.000V V_{OUT} = 1.550V[3]	• •	1.900 1.480		2.100 1.590	V
Short Circuit Detect Current		•	45		60	µA
Efficiency	I_{LOAD} = I_{max}, V_{OUT} = 2.0V			85		%
Output Driver Rise & Fall Time	See Figure 5 for t_R and t_F			50		nsec
Output Driver Deadtime	R_{OTA} = OPEN. See Figure 5 for t_{DT}			50		nsec
Oscillator Frequency	R_{OSC} = OPEN	•	255	300	345	kHz
Oscillator Range			80		1000	kHz
Duty Cycle			0		100	%
Dead Time Range			50		120	nsec
PWRGD Threshold	Logic HIGH Logic LOW	• •	93 88		107 112	%V_{out}
V_{CCA} UVLO		•	3.74	4	4.26	V
V_{CCP} UVLO		•	7.65	8.5	9.35	V
V_{CCA} Supply Current				19		mA
V_{CCP} Supply Current[4]				40		mA
Soft Start Current		•	5	10	17	µA
OVP Output Low Voltage	I = 1mA				200	mV
OVP Ouput High Current	V = 1.5V		30			mA
OVP Trigger Threshold			115	120	125	%V_{out}

Notes:

1. Steady State Voltage Regulation includes Initial Voltage Setpoint, Droop, Output Ripple and Output Temperature Drift and is measured at the converter's VFB sense point.
2. As measured at the converter's VFB sense point. For motherboard applications, the PCB layout should exhibit no more than 0.5mΩ trace resistance between the converter's output capacitors and the CPU. Remote sensing should be used for optimal performance.
3. Using the VFB pin for remote sensing of the converter's output at the load, the converter will be in compliance with Intel's VRM 8.4 specification of +50, -80mV. If Intel specifications on maximum plane resistance from the converter's output capacitors to the CPU are met, the specification of +40, -70mV at the capacitors will also be met.
4. Includes gate current.

Table 1. Output Voltage Programming Codes

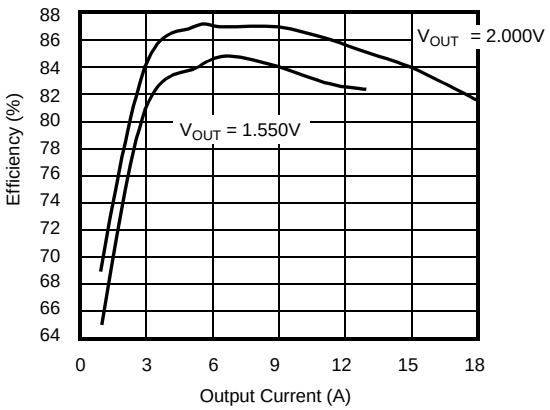
VID4	VID3	VID2	VID1	VID0	Nominal V_{OUT}
0	1	1	1	1	1.30V
0	1	1	1	0	1.35V
0	1	1	0	1	1.40V
0	1	1	0	0	1.45V
0	1	0	1	1	1.50V
0	1	0	1	0	1.55V
0	1	0	0	1	1.60V
0	1	0	0	0	1.65V
0	0	1	1	1	1.70V
0	0	1	1	0	1.75V
0	0	1	0	1	1.80V
0	0	1	0	0	1.85V
0	0	0	1	1	1.90V
0	0	0	1	0	1.95V
0	0	0	0	1	2.00V
0	0	0	0	0	2.05V
1	1	1	1	1	2.0V
1	1	1	1	0	2.1V
1	1	1	0	1	2.2V
1	1	1	0	0	2.3V
1	1	0	1	1	2.4V
1	1	0	1	0	2.5V
1	1	0	0	1	2.6V
1	1	0	0	0	2.7V
1	0	1	1	1	2.8V
1	0	1	1	0	2.9V
1	0	1	0	1	3.0V
1	0	1	0	0	3.1V
1	0	0	1	1	3.2V
1	0	0	1	0	3.3V
1	0	0	0	1	3.4V
1	0	0	0	0	3.5V

Note:

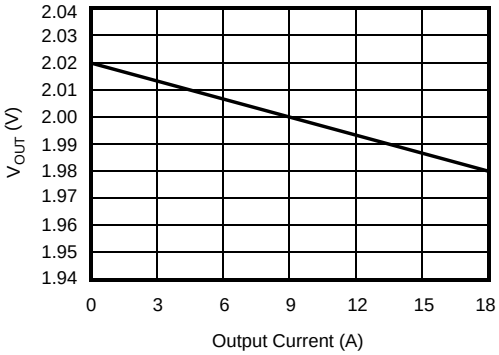
1. 0 = processor pin is tied to GND.
   1 = processor pin is open.

Typical Operating Characteristics (V_{CCA} = 5V, V_{CCP} = V_{CCQP} = 12V, and T_A = +25°C using circuit in Figure 1, unless otherwise noted.)

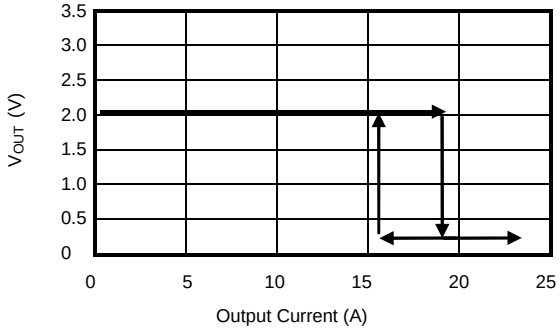
Efficiency vs. Output Current



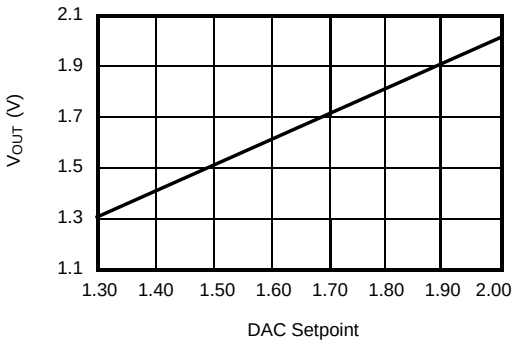
Droop, V_{OUT} = 2.0V



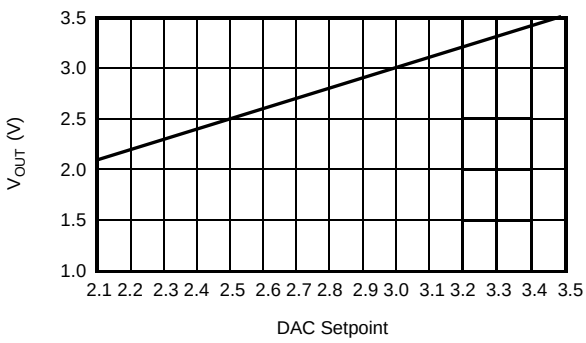
Output Voltage vs. Output Current



Output Programming, VID4 = 0



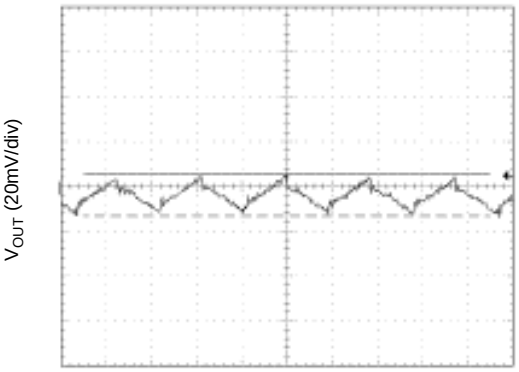
Output Programming, VID4 = 1



Preliminary Specification

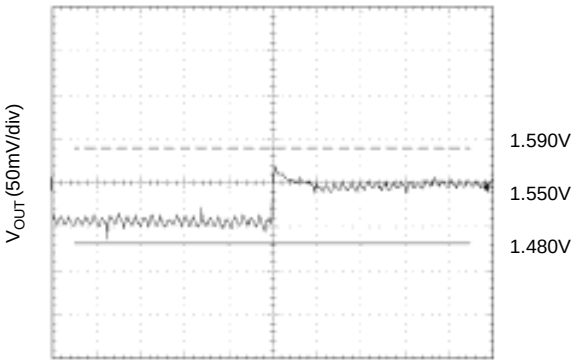
Typical Operating Characteristics (continued)

Output Ripple, 2.0V @ 18A



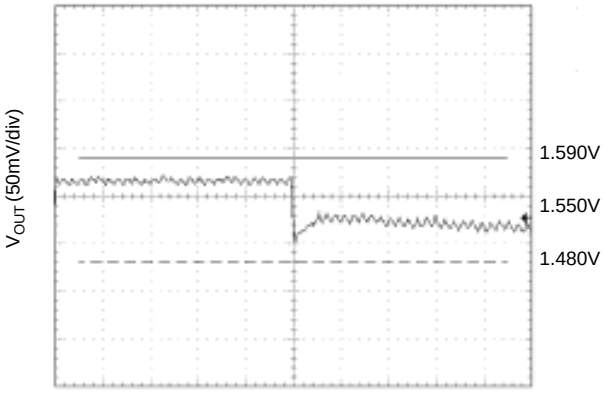
Time (1µs/division)

Transient Response, 12.5A to 0.5A



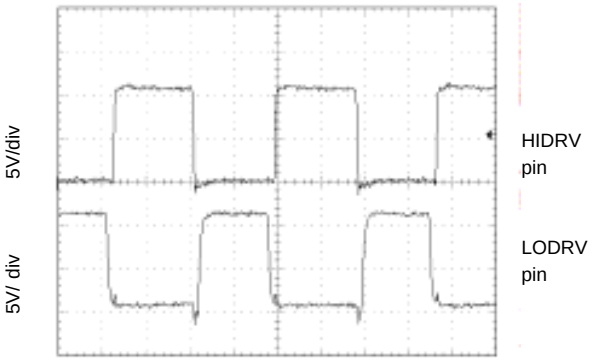
Time (20µs/division)

Transient Response, 0.5A to 12.5A



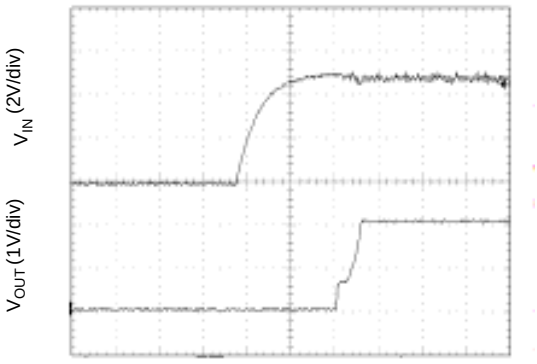
Time (20µs/division)

Switching Waveforms, 18A Load



Time (1µs/division)

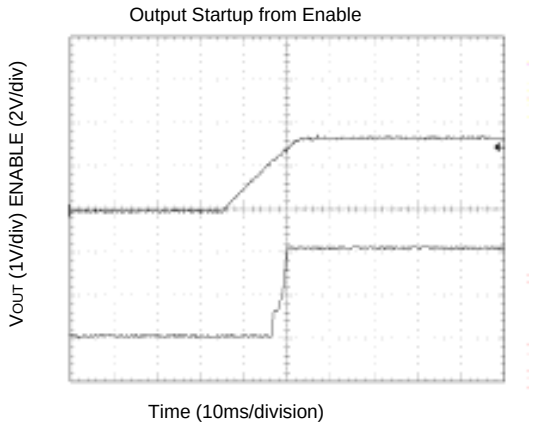
Output Startup, System Power-up

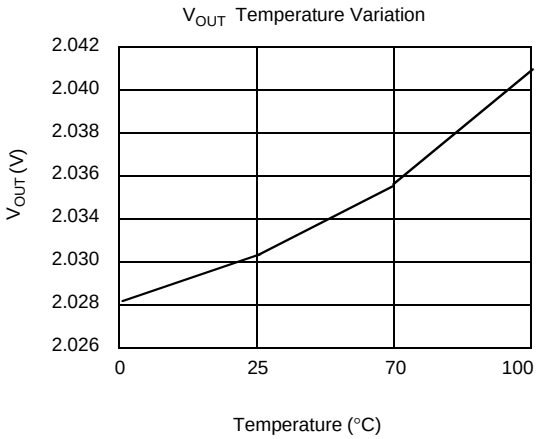


Time (10ms/division)

Preliminary Specification

Typical Operating Characteristics (continued)





Application Circuit

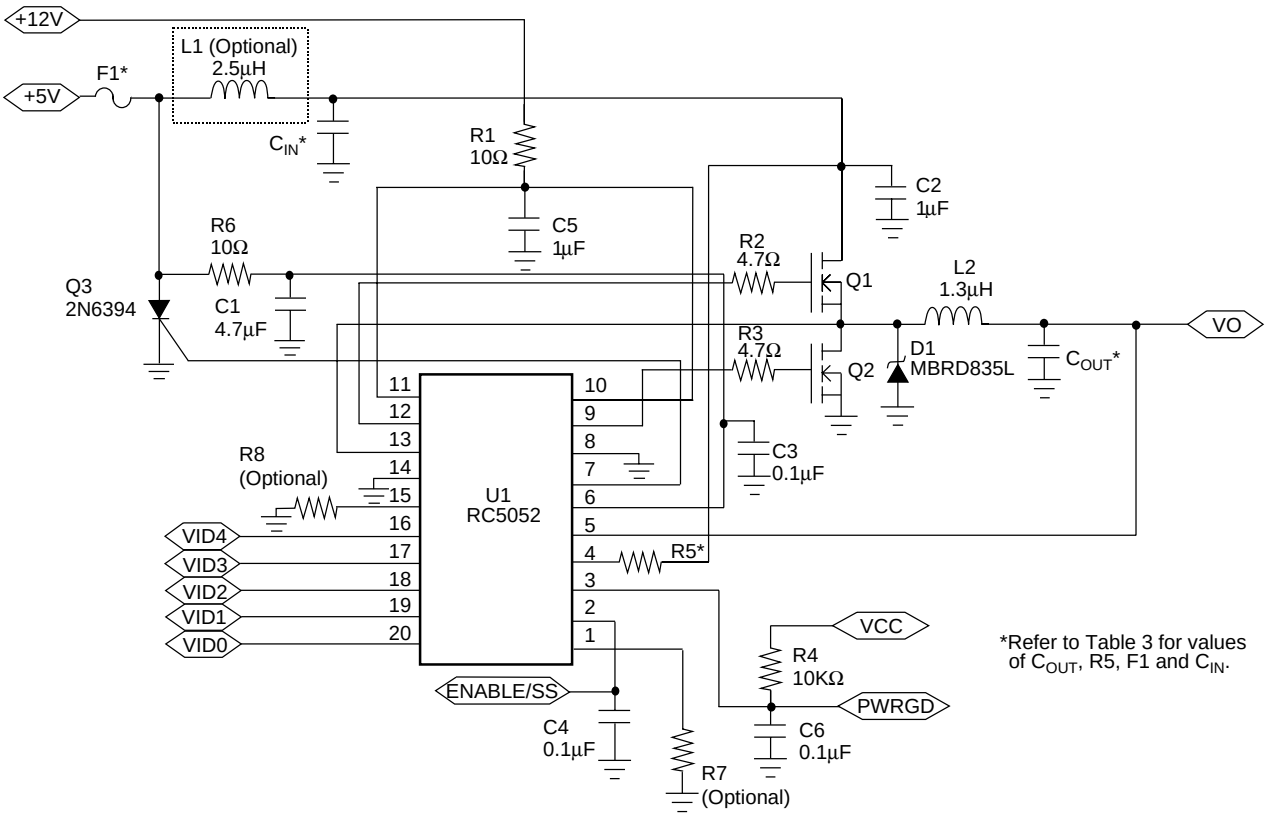


Figure 1. Application Circuit for Katmai, Mendocino, and Some Coppermine Processors
(*Worst Case Analyzed!* See Appendix for Details)

Preliminary Specification

Table 2. RC5052 Application Bill of Materials for Intel Pentium II Processors
(Components based on Worst Case Analysis—See Appendix for Details)

Reference	Manufacturer Part #	Quantity	Description	Requirements/Comments
C1	AVX TAJB475M010R5	1	4.7µF, 10V Capacitor	
C2, C5	Panasonic ECU-V1C105ZFX	2	1µF, 16V Capacitor	
C3-4,6	Panasonic ECU-V1H104ZFX	3	100nF, 50V Capacitor	
C_{IN}	Sanyo 10MV1200GX	*	1200µF, 10V Electrolytic	I_{RMS} = 2A
C_{OUT}	Sanyo 6MV1500GX	*	1500µF, 6.3V Electrolytic	ESR ≤44mΩ
D1	Motorola MBRD835L	1	8A Schottky Diode	
L1	Any	Optional	2.5µH, 10A Inductor	DCR ~ 6mΩ See Note 1.
L2	Any	1	1.3µH, 20A Inductor	DCR ~ 2mΩ
Q1	Fairchild FDP6030L or FDB6030L	1	N-Channel MOSFET (TO-220 or TO-263)	$R_{DS(ON)}$ = 20mΩ @ V_{GS} = 4.5V See Note 2.
Q2	Fairchild FDP7030BL or FDB7030BL	1	N-Channel MOSFET (TO-220 or TO-263)	$R_{DS(ON)}$ = 10mΩ @ V_{GS} = 4.5V See Note 2.
Q3	Motorola 2N6394	1	SCR	
R1, R6	Any	2	10Ω	
R2-3	Any	2	4.7Ω	
R4	Any	1	10KΩ	
R5	Any	1	*	
R7	Any	Optional		Sets frequency.
R8	Any	Optional		Sets deadtime.
F1	Littelfuse	1	*	
U1	Fairchild RC5052M	1	DC/DC Controller	

*See Table 3.

Notes:

1. Inductor L1 is recommended to isolate the 5V input supply from noise generated by the MOSFET switching, and to comply with Intel dI/dt requirements. L1 may be omitted if desired.
2. For designs using the TO-220 MOSFETs, heatsinks with thermal resistance Θ_{SA} < 20°C/W should be used. For designs using the TO-263 MOSFETs, adequate copper area should be used. For details and a spreadsheet on MOSFET selections, refer to Applications Bulletin AB-8.

Table 3. Recommended Values for CPU-based Applications

Processor	Chipset	C_{IN}	C_{OUT}*	R5 (KΩ)	F1 (A)
Coppermine	Whitney	3	4	8.45	5
Katmai	Camino	4	6	13.0	10
Mendocino	Whitney	4	5	11.3	10
Katmai	BX	5	6	11.8	10

* Output capacitance requirements depend critically on layout and processor type. Consult Application Bulletin AB-14 for details. See the Appendix to this datasheet for the method of calculation of these components. Pin 4 must be used to remote sense the voltage at the processor to achieve the specified performance.

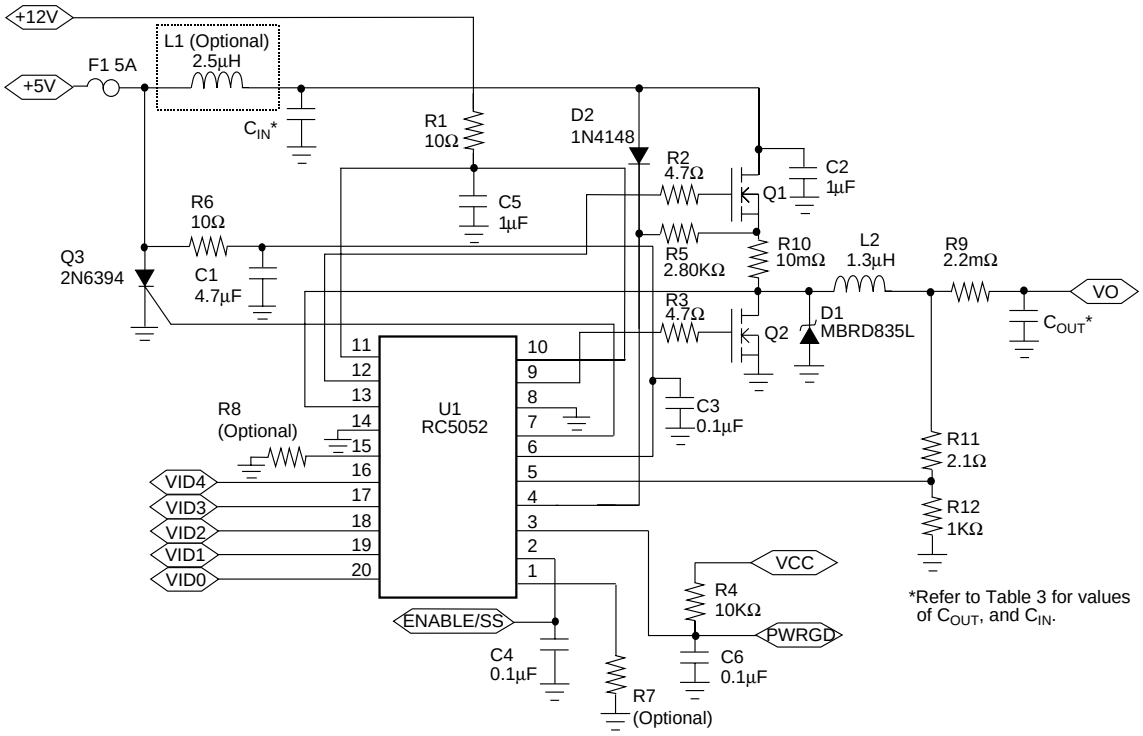


Figure 2. Application Circuit for Coppermine/Camino Processors
(*Worst Case Analyzed!* See Appendix for Details)

Table 4. RC5052 Application Bill of Materials for Coppermine/Camino Processors
(Components based on Worst Case Analysis—See Appendix for Details)

Reference	Manufacturer Part #	Quantity	Description	Requirements/Comments
C1	AVX TAJB475M010R5	1	4.7µF, 10V Capacitor	
C2, C5	Panasonic ECU-V1C105ZFX	2	1µF, 16V Capacitor	
C3-4,6	Panasonic ECU-V1H104ZFX	3	100nF, 50V Capacitor	
C_{IN}	Sanyo 10MV1200GX	3	1200µF, 10V Electrolytic	I_{RMS} = 2A
C_{OUT}	Sanyo 6MV1500GX	10	1500µF, 6.3V Electrolytic	ESR ≤ 44mΩ
D1	Motorola MBRD835L	1	8A Schottky Diode	
D2	Fairchild 1N4148	1	Signal Diode	
L1	Any	Optional	2.5µH, 10A Inductor	DCR ~ 6mΩ See Note 1.
L2	Any	1	1.3µH, 20A Inductor	DCR ~ 2mΩ
Q1	Fairchild FDP6030L or FDB6030L	1	N-Channel MOSFET (TO-220 or TO-263)	$R_{DS(ON)}$ = 20mΩ @ V_{GS} = 4.5V See Note 2.
Q2	Fairchild FDP7030BL or FDB7030BL	1	N-Channel MOSFET (TO-220 or TO-263)	$R_{DS(ON)}$ = 10mΩ @ V_{GS} = 4.5V See Note 2.
Q3	Motorola 2N6394	1	SCR	
R1, R6	Any	2	10Ω	
R2-3	Any	2	4.7Ω	
R4	Any	1	10KΩ	
R5	Any	1	2.80KΩ	
R7	Any	Optional		Sets frequency.
R8	Any	Optional		Sets deadtime.
R9	Any	1	2.2mΩ	PCB Trace Resistor
R10	Dale WSL-2512-.01Ω	1	10mΩ, 1W Resistor	
R11	Any	1	2.1Ω	
R12	Any	1	1KΩ	
F1	Littelfuse R251 005	1	5A Fast Fuse	
U1	Fairchild RC5052M	1	DC/DC Controller	

Notes:

1. Inductor L1 is recommended to isolate the 5V input supply from noise generated by the MOSFET switching, and to comply with Intel dI/dt requirements. L1 may be omitted if desired.
2. For designs using the TO-220 MOSFETs, heatsinks with thermal resistance Θ_{SA} < 20°C/W should be used. For designs using the TO-263 MOSFETs, adequate copper area should be used. For details and a spreadsheet on MOSFET selections, refer to Applications Bulletin AB-8.

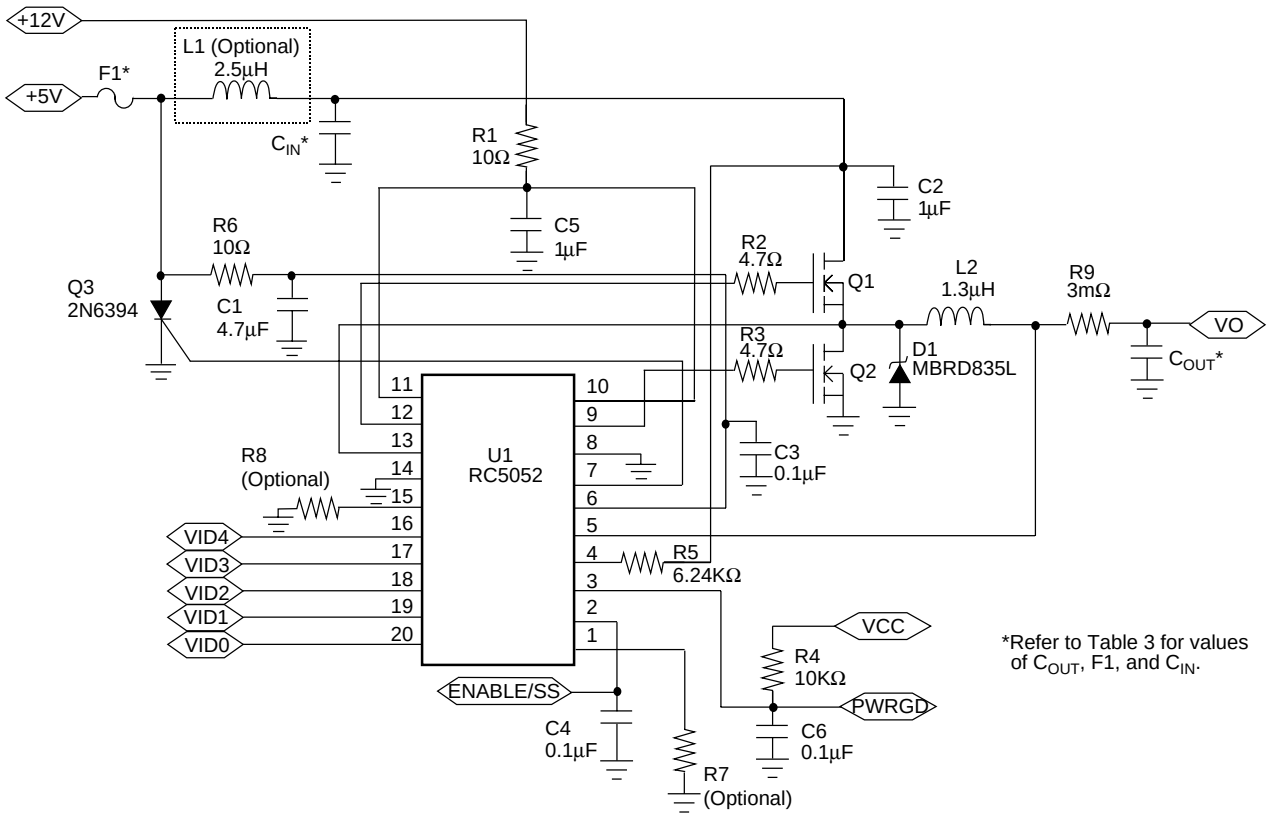


Figure 3. Application Circuit for Coppermine/Camino Processors
(*Typical Design*)

Table 5. RC5052 Application Bill of Materials for Coppermine/Camino Processors
(Typical Design)

Reference	Manufacturer Part #	Quantity	Description	Requirements/Comments
C1	AVX TAJB475M010R5	1	4.7µF, 10V Capacitor	
C2, C5	Panasonic ECU-V1C105ZFX	2	1µF, 16V Capacitor	
C3-4,6	Panasonic ECU-V1H104ZFX	3	100nF, 50V Capacitor	
C_{IN}	Sanyo 10MV1200GX	3	1200µF, 10V Electrolytic	I_{RMS} = 2A
C_{OUT}	Sanyo 6MV1500GX	8	1500µF, 6.3V Electrolytic	ESR ≤ 44mΩ
D1	Motorola MBRD835L	1	8A Schottky Diode	
L1	Any	Optional	2.5µH, 10A Inductor	DCR ~ 6mΩ See Note 1.
L2	Any	1	1.3µH, 20A Inductor	DCR ~ 2mΩ
Q1-2	Fairchild FDP6030L or FDB6030L	2	N-Channel MOSFET (TO-220 or TO-263)	$R_{DS(ON)}$ = 20mΩ @ VG_S = 4.5V See Note 2.
Q3	Motorola 2N6394	1	SCR	
R1, R6	Any	2	10Ω	
R2-3	Any	2	4.7Ω	
R4	Any	1	10KΩ	
R5	Any	1	6.24KΩ	
R7	Any	Optional		Sets frequency.
R8	Any	Optional		Sets deadtime.
R9	N/A	1	3.0mΩ	PCB Trace Resistor
F1	Littelfuse R251 005	1	5A Fast Fuse	
U1	Fairchild RC5052M	1	DC/DC Controller	

Notes:

1. Inductor L1 is recommended to isolate the 5V input supply from noise generated by the MOSFET switching, and to comply with Intel dI/dt requirements. L1 may be omitted if desired.
2. For designs using the TO-220 MOSFETs, heatsinks with thermal resistance Θ_{SA} < 20°C/W should be used. For designs using the TO-263 MOSFETs, adequate copper area should be used. For details and a spreadsheet on MOSFET selections, refer to Applications Bulletin AB-8.

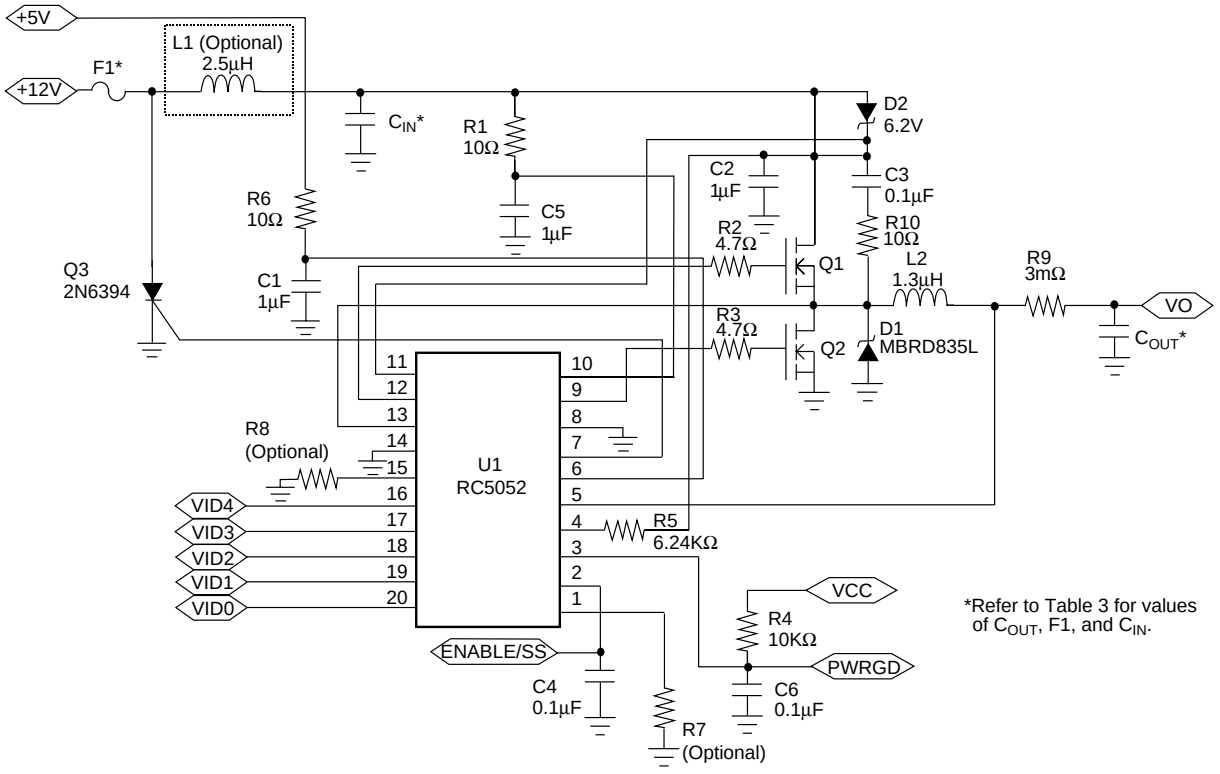


Figure 4. Application Circuit for Coppermine/Camino Processors
(*Typical Design*)

Table 6. RC5052 Application Bill of Materials for Coppermine/Camino Processors
(Typical Design)

Reference	Manufacturer Part #	Quantity	Description	Requirements/Comments
C1-2, C5	AVX TAJB475M010R5	3	1µF, 16V Capacitor	
C3-4,6	Panasonic ECU-V1H104ZFX	3	100nF, 50V Capacitor	
C_{IN}	Sanyo 10MV1200GX	3	1200µF, 10V Electrolytic	I_{RMS} = 2A
C_{OUT}	Sanyo 6MV1500GX	8	1500µF, 6.3V Electrolytic	ESR ≤ 44mΩ
D1	Motorola MDRDS835L	1	8A Schottky Diode	
D2	Fairchild MMSZ5233B	1	6.2V Zener	
L1	Any	Optional	2.5µH, 10A Inductor	DCR ~ 6mΩ See Note 1.
L2	Any	1	1.3µH, 20A Inductor	DCR ~ 2mΩ
Q1-2	Fairchild FDP6030L or FDB6030L	2	N-Channel MOSFET (TO-220 or TO-263)	$R_{DS(ON)}$ = 20mΩ @ VG_S = 4.5V See Note 2.
Q3	Motorola 2N6394	1	SCR	
R1, R6, R10	Any	3	10Ω	
R2-3	Any	2	4.7Ω	
R4	Any	1	10KΩ	
R5	Any	1	6.24KΩ	
R7	Any	Optional		Sets frequency.
R8	Any	Optional		Sets deadtime.
R9	N/A	1	3.0mΩ	PCB Trace Resistor
F1	Littelfuse R251 005	1	5A Fast Fuse	
U1	Fairchild RC5052M	1	DC/DC Controller	

Notes:

1. Inductor L1 is recommended to isolate the 5V input supply from noise generated by the MOSFET switching, and to comply with Intel dI/dt requirements. L1 may be omitted if desired.
2. For designs using the TO-220 MOSFETs, heatsinks with thermal resistance Θ_{SA} < 20°C/W should be used. For designs using the TO-263 MOSFETs, adequate copper area should be used. For details and a spreadsheet on MOSFET selections, refer to Applications Bulletin AB-8.

Test Parameters

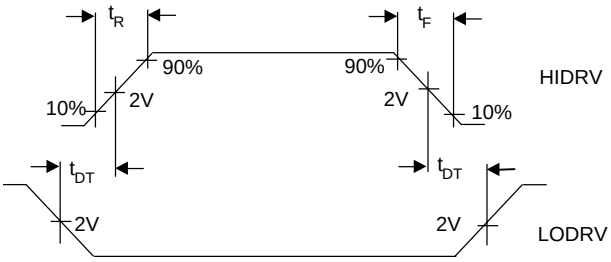


Figure 5. Output Drive Timing Diagram

Application Information

The RC5052 Controller

The RC5052 is a programmable synchronous DC-DC controller IC. When designed around the appropriate external components, the RC5052 can be configured to deliver more than 16A of output current, as appropriate for the Katmai and Coppermine and other processors. The RC5052 functions as a fixed frequency PWM step down regulator.

Main Control Loop

Refer to the RC5052 Block Diagram on page 1. The RC5052 implements "summing mode control", which is different from both classical voltage-mode and current-mode control. It provides superior performance to either by allowing a large converter bandwidth over a wide range of output loads.

The control loop of the regulator contains two main sections: the analog control block and the digital control block. The analog section consists of signal conditioning amplifiers feeding into a comparator which provides the input to the digital control block. The signal conditioning section accepts input from the IFB (current feedback) and VFB (voltage feedback) pins and sets up two controlling signal paths. The first, the voltage control path, amplifies the difference between the VFB signal and the reference voltage from the DAC and presents the output to one of the summing amplifier inputs. The second, current control path, takes the difference between the IFB and SW pins when the high-side MOSFET is on, reproducing the voltage across the MOSFET and thus the input current; it presents the resulting signal to another input of the summing amplifier. These two signals are then summed together. This output is then presented to a comparator looking at the oscillator ramp, which provides the main PWM control signal to the digital control block.

The digital control block takes the analog comparator input and the main clock signal from the oscillator to provide the appropriate pulses to the HIDRV and LODRV output pins. These two outputs control the external power MOSFETs.

There is an additional comparator in the analog control section whose function is to set the point at which the RC5052 current limit comparator disables the output drive signals to the external power MOSFETs.

High Current Output Drivers

The RC5052 contains two identical high current output drivers that utilize high speed bipolar transistors in a push-pull configuration. The drivers' power and ground are separated from the chip's power and ground for switching noise immunity. The high-side driver's power supply pin, VCCQP, is supplied from an external 12V source through a series resistor. The resulting voltage is sufficient to provide the gate to source drive to the external MOSFETs required in order to achieve a low $R_{DS,ON}$. The low-side driver's power supply pin, VCCP, is supplied from either 5V or from the same source as VCCQP. Choosing 12V will ensure lowest possible $R_{DS,ON}$; choosing 5V will result in lower gate current, which may be important when operating the RC5052 at high frequency and lower output power. The VCCQP pin may also be run as charge pump for +12V Main Power, as shown in Figure 4.

Internal Voltage Reference

The reference included in the RC5052 is a precision band-gap voltage reference. Its internal resistors are precisely trimmed to provide a near zero temperature coefficient (TC). Based on the reference is the output from an integrated 5-bit DAC. The DAC monitors the 5 voltage identification pins, VID0-4. When the VID4 pin is at logic HIGH, the DAC scales the reference voltage from 2.0V to 3.5V in 100mV increments. When VID4 is pulled LOW, the DAC scales the reference from 1.30V to 2.05V in 50mV increments. All VID codes are available, including those below 1.80V. The output voltage may be changed while the converter is on by changing the VID codes; however, it is necessary to do so in 1-bit steps, to avoid triggering the overvoltage protection.

Power Good (PWRGD)

The RC5052 Power Good function is designed in accordance with the Pentium II DC-DC converter specifications and provides a continuous voltage monitor on the VFB pin. The circuit compares the VFB signal to the VREF voltage and outputs an active-low interrupt signal to the CPU should the power supply voltage deviate more than ±12% of its nominal setpoint. The output is guaranteed open-collector high when the power supply voltage is within ±7% of its nominal setpoint. The Power Good flag provides no other control function to the RC5052.

Output Enable/Soft Start (ENABLE/SS)

The RC5052 will accept an open collector/TTL signal for controlling the output voltage. The low state disables the output voltage. When disabled, the PWRGD output is in the low state.

Even if an enable is not required in the circuit, this pin should have attached a capacitor (typically 100nF) to soft-start the switching.

Over-Voltage Protection

The RC5052 constantly monitors the output voltage for protection against over-voltage conditions. If the voltage at the VFB pin exceeds the selected program voltage, an over-voltage condition is assumed and the RC5052 disables the output drive signal to the external high-side MOSFET, and drives the OVP pin high. This is designed to drive the gate of an external SCR, which blows a fuse, disconnecting the short from the power bus.

Oscillator

The RC5052 oscillator free runs at 300 kHz, and may be adjusted from 80KHz to 1MHz as desired. Higher frequensies will permit smaller components, while decreasing efficiency. A typical operating frequency is 300KHz. The frequency may be adjusted upwith a resistor to ground on pin 1, according to the formula:

$$f = 300kHz^* \frac{40K\Omega}{R_{OSC}}$$

and may be adjusted down with aresistor to 5V on pin 1, according to the formula:

$$f = 300kHz^* \left(1- \frac{160K\Omega}{R_{OSC}}\right)$$

Dead Time

The RC5052 can control the deadtime, that is, the time between when the high-side MOSFET is turned off and the low-side MOSFET is turned on, and vice versa. Longer dead times are appropriate when using multiple MOSFETs in parallel, or when MOSFETs with larger gate capacitance are used. The dead time may be adjusted with a resistor to ground on pin 15, according to the formula:

$$T_{DT} = 100nsec^* \frac{R_{DTA}}{80K\Omega}$$

Design Considerations and Component Selection

Additional information on design and component selection may be found in Fairchild's Application Note 57.

MOSFET Selection

This application requires N-channel Logic Level Enhancement Mode Field Effect Transistors. Desired characteristics are as follows:

- Low Static Drain-Source On-Resistance, $R_{DS,ON} < 20m\Omega$ (lower is better)
- Low gate drive voltage, $V_{GS} = 4.5V$ rated
- Power package with low Thermal Resistance
- Drain-Source voltage rating > 15V.

The on-resistance (RDS,ON) is the primary parameter for MOSFET selection. The on-resistance determines the power dissipation within the MOSFET and therefore significantly affects the efficiency of the DC-DC Converter. For details and a spreadsheet on MOSFET selection, refer to Applications Bulletin AB-8.

Inductor Selection

Choosing the value of the inductor is a tradeoff between allowable ripple voltage and required transient response. The system designer can choose any value within the allowed minimum to maximum range in order to either minimize ripple or maximize transient performance. The first order equation (close approximation) for minimum inductance is:

$$L_{min} = \frac{(V_{in} - V_{out})}{f} \times \frac{V_{out}}{V_{in}} \times \frac{ESR}{V_{ripple}}$$

where:

V_{in} = Input Power Supply

V_{out} = Output Voltage

f = DC/DC converter switching frequency

ESR = Equivalent series resistance of all output capacitors in parallel

V_{ripple} = Maximum peak to peak output ripple voltage budget.

The first order equation for maximum allowed inductance is:

$$L_{max} = 2C_0 \frac{(V_{in} - V_{out})\, D_m\, V_{tb}}{I_{pp}^2}$$

where:

C_o = The total output capacitance

I_{pp} = Maximum to minimum load transient current

V_{tb} = The output voltage tolerance budget allocated to load transient

Preliminary Specification

D_m = Maximum duty cycle for the DC/DC converter (usually 95%).

Some margin should be maintained away from both L_{min} and L_{max}. Adding margin by increasing L almost always adds expense since all the variables are predetermined by system performance except for C_o, which must be increased to increase L. Adding margin by decreasing L can be done by purchasing capacitors with lower ESR. The RC5052 provides significant cost savings for the newer CPU systems that typically run at high supply current.

RC5052 Short Circuit Current Characteristics

The RC5052 short circuit current characteristic includes a hysteresis function that prevents the DC-DC converter from oscillating in the event of a short circuit. The short circuit limit is set with the R_S resistor, as given by the formula

$$R_S = \frac{I_{SC} \times *R_{DS,\,on}}{I_{Detect}}$$

with $I_{Detect} \approx 50\mu A$, I_{SC} the desired current limit, and $R_{DS,on}$ the high-side MOSFET's on resistance. Remember to make the R_S large enough to include the effects of initial tolerance and temperature variation on the MOSFET's $R_{DS,on}$. Alternately, use of a sense resistor in series with the source of the MOSFET, as shown in Figure 6, eliminates this source of inaccuracy in the current limit. Note one addition of one diode, which is necessary for proper operation of this circuit.

As an example, Figure 6 shows the typical characteristic of the DC-DC converter circuit with an FDB6030L high-side MOSFET (R_{DS} = 20mΩ maximum at 25°C * 1.25 at 75°C = 25mΩ) and a 8.2KΩ R_S.

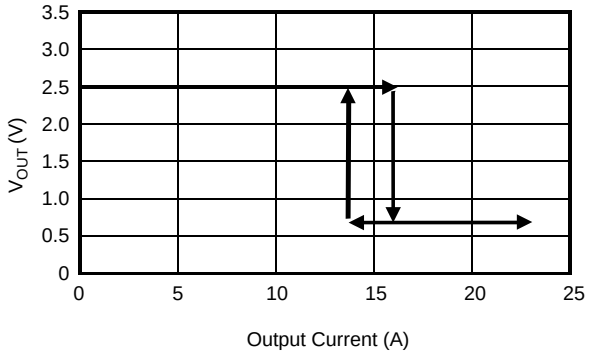


Figure 6. RC5052 Short Circuit Characteristic

The converter exhibits a normal load regulation characteristic until the voltage across the MOSFET exceeds the internal short circuit threshold of 50µA * 8.2KΩ = 410mV, which occurs at 410mV/25mΩ = 16.4A. (Note that this current limit level can be as high as 410mV/15mΩ = 27A, if the MOSFET has typical $R_{DS,on}$ rather than maximum, and is at 25°C. This is the reason for using the external sense resistor.) At this point, the internal comparator trips and signals the controller to reduce the converter's duty cycle to approximately 20%. This causes a drastic reduction in the output voltage as the load regulation collapses into the short circuit control mode. With a 40mΩ output short, the voltage is reduced to 16.4A * 40mΩ = 650mV. The output voltage does not return to its nominal value until the output current is reduced to a value within the safe operating range for the DC-DC converter.

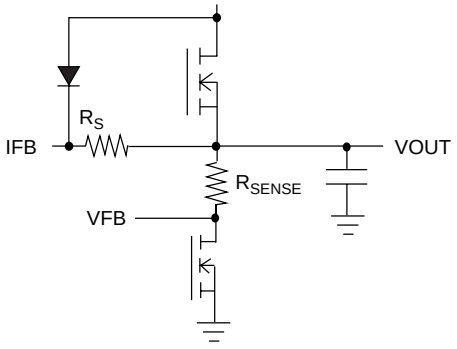


Figure 7. Precision Current Sensing

Schottky Diode Selection

The application circuit of Figure 1 shows a Schottky diode, D1, which is used as a free-wheeling diode to assure that the body-diode in Q2 does not conduct when the upper MOSFET is turning off and the lower MOSFET is turning on. It is undesirable for this diode to conduct because its high forward voltage drop and long reverse recovery time degrades efficiency, and so the Schottky provides a shunt path for the current. Since this time duration is very short, the selection criterion for the diode is that the forward voltage of the Schottky at the output current should be less than the forward voltage of the MOSFET's body diode.

Output Filter Capacitors

The output bulk capacitors of a converter help determine its output ripple voltage and its transient response. It has already been seen in the section on selecting an inductor that the ESR helps set the minimum inductance, and the capacitance value helps set the maximum inductance. For most converters, however, the number of capacitors required is determined by the transient response and the output ripple voltage, and these are determined by the ESR and not the capacitance value. That is, in order to achieve the necessary ESR to meet the transient and ripple requirements, the capacitance value required is already very large.

The most commonly used choice for output bulk capacitors is aluminum electrolytics, because of their low cost and low ESR. The only type of aluminum capacitor used should be those that have an ESR rated at 100kHz. Consult Application Bulletin AB-14 for detailed information on output capacitor selection.

The output capacitance should also include a number of small value ceramic capacitors placed as close as possible to the processor; 0.1µF and 0.01µF are recommended values.

Input Filter

The DC-DC converter design may include an input inductor between the system +5V supply and the converter input as shown in Figure 8. This inductor serves to isolate the +5V supply from the noise in the switching portion of the DC-DC converter, and to limit the inrush current into the input capacitors during power up. A value of 2.5µH is recommended.

It is necessary to have some low ESR aluminum electrolytic capacitors at the input to the converter. These capacitors deliver current when the high side MOSFET switches on. Figure 8 shows 3 x 1000µF, but the exact number required will vary with the speed and type of the processor. For the top speed Katmai and Coppermine, the capacitors should be rated to take 9A and 6A RMS of ripple current respectively. Capacitor ripple current rating is a function of temperature, and so the manufacturer should be contacted to find out the ripple current rating at the expected operational temperature. For details on the design of an input filter, refer to Applications Bulletin AB-15.

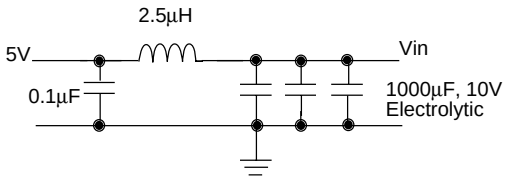


Figure 8. Input Filter

Active Droop

The RC5052 includes active droop: as the output current increases, the output voltage drops. This is done in order to allow maximum headroom for transient response of the converter. The current is sensed by measuring the voltage across the high-side MOSFET during its on time. Note that this makes the droop dependent on the temperature of the MOSFET. However, when the formula given for selecting R_S (current limit) is used, there is a maximum droop possible (-40mV), and when this value is reached, additional drop across the MOSFET will not cause any increase in droop—until current limit is reached.

Additional droop can be added to the active droop using a discrete resistor (typically a PCB trace) outside the control loop, as shown in Figure 1. This is typically only required for the most demanding applications, such as for the next generation Intel processor (tolerance = +40/-70mV), as shown in Figure 1.

PCB Layout Guidelines

- Placement of the MOSFETs relative to the RC5052 is critical. Place the MOSFETs such that the trace length of the HIDRV and LODRV pins of the RC5052 to the FET gates is minimized. A long lead length on these pins will cause high amounts of ringing due to the inductance of the trace and the gate capacitance of the FET. This noise radiates throughout the board, and, because it is switching at such a high voltage and frequency, it is very difficult to suppress.
- In general, all of the noisy switching lines should be kept away from the quiet analog section of the RC5052. That is, traces that connect to pins 9, 10, 11, 12 and 13 (LODRV, VCCP, VCCQP, HIDRV and SW) should be kept far away from the traces that connect to pins 4 through 6, and pin 14.
- Place the 0.1µF decoupling capacitors as close to the RC5052 pins as possible. Extra lead length on these reduces their ability to suppress noise.
- Each VCC and GND pin should have its own via to the appropriate plane. This helps provide isolation between pins.
- Place the MOSFETs, inductor, and Schottky as close together as possible for the same reasons as in the first bullet above. Place the input bulk capacitors as close to the drains of the high side MOSFETs as possible. In addition, placement of a 0.1µF decoupling cap right on the drain of each high side MOSFET helps to suppress some of the high frequency switching noise on the input of the DC-DC converter.
- Place the output bulk capacitors as close to the CPU as possible to optimize their ability to supply instantaneous current to the load in the event of a current transient. Additional space between the output capacitors and the CPU will allow the parasitic resistance of the board traces to degrade the DC-DC converter's performance under severe load transient conditions, causing higher voltage deviation. For more detailed information regarding capacitor placement, refer to Application Bulletin AB-5.
- A PC Board Layout Checklist is available from Fairchild Applications. Ask for Application Bulletin AB-11.

PC Motherboard Sample Layout and Gerber File

A reference design for motherboard implementation of the RC5052 along with the PCAD layout Gerber file and silk screen can be obtained from our marketing department at 650-968-9211 x7624.

RC5052 Evaluation Board

Fairchild provides an evaluation board to verify the system level performance of the RC5052. It serves as a guide to performance expectations when using the supplied external components and PCB layout. Please call the marketing department at 650-968-9211 x7624 for an evaluation board.

Additional Information

For additional information contact Fairchild Semiconductor's Analog & Mixed Signal Products Group Marketing Department at 650-968-9211 x7624.

Appendix

Worst-Case Formulae for the Calculation of C_{out}, R5, and C_{in} (Circuit of Figure 1 Only)

The following formulae design the RC5052 for worst-case operation, including initial tolerance and temperature dependence of all of the IC parameters (initial setpoint, reference tolerance and tempco, active droop tolerance, current sensor gain), the initial tolerance and temperature dependence of the MOSFET, and the ESR of the capacitors. The following information must be provided:

V_{T+}, the value of the positive transient voltage limit;

$|V_{T-}|$, the absolute value of the negative transient voltage limit;

I_O, the maximum output current;

V_{nom}, the nominal output voltage;

V_{in}, the input voltage (typically 5V);

ESR, the ESR of the output caps, per cap (44mΩ for the Sanyo parts shown in this datasheet);

R_D, the on-resistance of the MOSFET (20mΩ for the FDB6030);

ΔR_D, the tolerance of the current sensor (usually about 67% for MOSFET sensing, including temperature).

I_{rms}, the rms current rating of the input caps (2A for the Sanyo parts shown in this datasheet).

$$C_{in} = \frac{IO * \sqrt{\frac{V_{nom}}{V_{in}} - \left(\frac{V_{nom}}{V_{in}}\right)^2}}{I_{rms}}$$

$$R5 = \frac{I_O * R_D * (1 + \Delta R_D) * 1.10}{50 * 10^{-6}}$$

Number of capacitors needed for C_{out} = the greater of:

$$X = \frac{ESR * I_O}{|V_{T-}|}$$

or

$$Y = \frac{ESR * I_O}{V_{T+} - 0.004 * V_{nom} + \frac{14400 * I_O * R_D}{18 * R5 * 1.1}}$$

Example: Suppose that the transient limits are ±134mV, current I is 14.2A, and the nominal voltage is 2.000V, using MOSFET current sensing and the usual caps. We have V_{T+} = $|V_{T-}|$ = 0.134, I_O = 14.2, V_{nom} = 2.000, and ΔR_D = 0.67. We calculate:

$$C_{in} = \frac{14.2 * \sqrt{\frac{2.000}{5} - \left(\frac{2.000}{5}\right)^2}}{2} = 3.47 \Rightarrow 4 \text{ caps}$$

$$R5 = \frac{14.2 * 0.020 * (1 + 0.67) * 1.10}{50 * 10^{-6}} = 10.4K\Omega$$

$$X = \frac{0.044 * 14.2}{0.134} = 4.66$$

$$Y = \frac{0.044 * 14.2}{0.134 - 0.004 * 2.000 + \frac{14400 * 14.2 * 0.020}{18 * 10400 * 1.1}} = 4.28$$

Since X > Y, we choose X, and round up to find we need 5 capacitors for C_{OUT}.

A detailed explanation of this calculation, and the calculations used for Figure 2, may be found Applications Bulletin AB-XX.

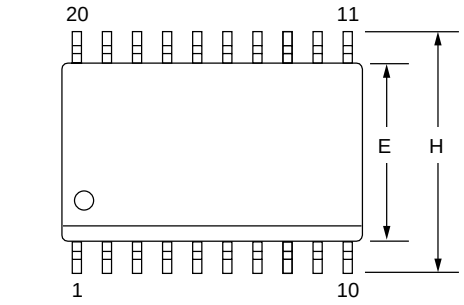
Mechanical Dimensions

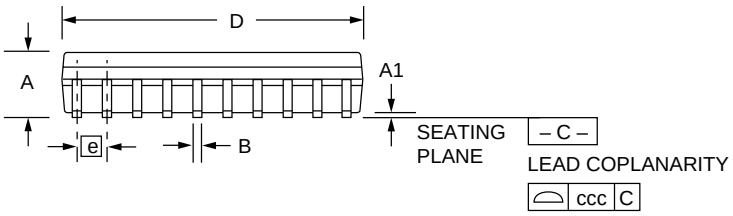
20 Lead SOIC

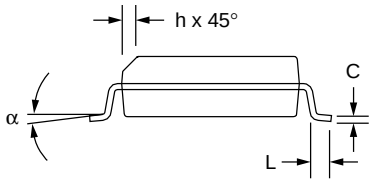
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.496	.512	12.60	13.00	2
E	.291	.299	7.40	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.029	0.25	0.75	
L	.016	.050	0.40	1.27	3
N	20		20		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Preliminary Specification

Ordering Information

Product Number	Package
RC5052M	20 pin SOIC

Preliminary Specification

RC5053

5-Bit Programmable Synchronous Switching Regulator Controller for Pentium® II Processor

Features

- 5-Bit Digitally Programmable 1.8V to 3.5V Fixed Output Voltage
- Provides All Features Required by the Intel Pentium II Processor VRM 8.2 DC/DC Converter Specification
- Flags for Power Good, Over-Temperature and Over-Voltage Fault
- Output Current Exceeds 14A from a 5V Supply
- Dual N-Channel MOSFET Synchronous Driver
- Initial Output Accuracy: ±1.5%
- Excellent Output Accuracy: ±2% Typ Over Line, Load and Temperature Variations
- High Efficiency: Over 95% Possible
- Adjustable Current Limit Without External Sense Resistors
- Fast Transient Response
- Available in SO-20 and SSOP-20 Packages

Applications

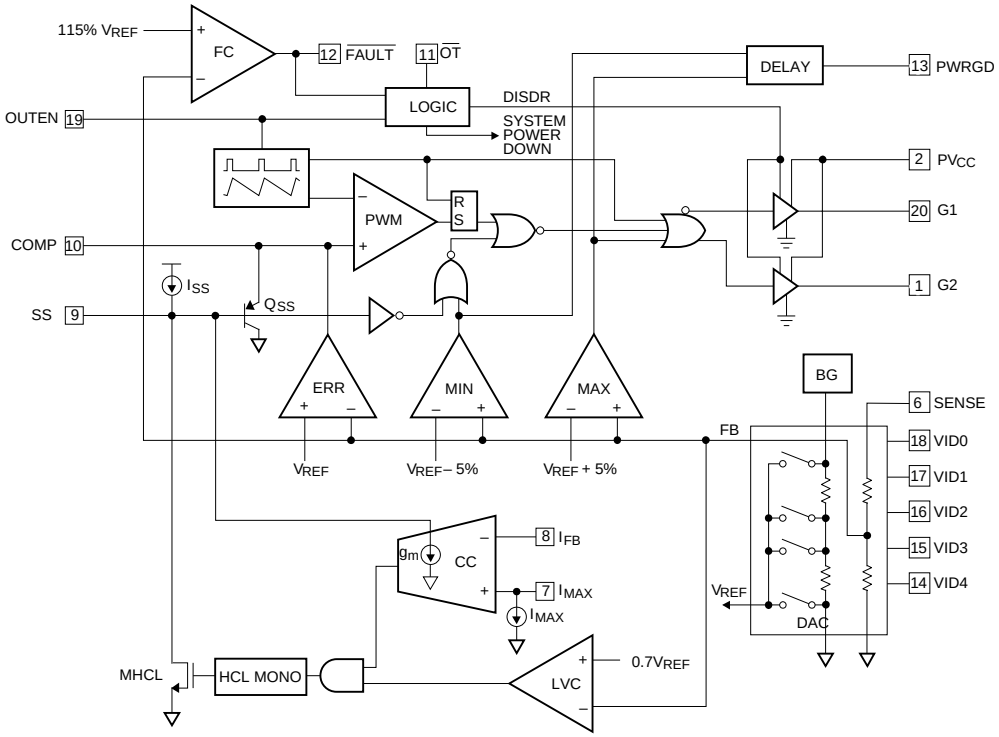
- Power Supply for Pentium II, SPARC, ALPHA and PA-RISC Microprocessors
- High Power 5V to 1.8V-3.5V Regulators

Descriptions

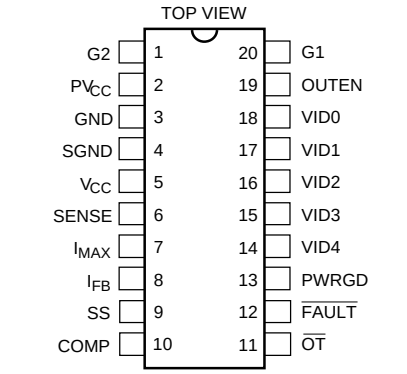
The RC5053 is a high power, high efficiency switching regulator controller optimized for 5V input to 1.8V-3.5V output applications. It features a digitally programmable output voltage, a precision internal reference and an internal feedback system that provides output accuracy of ±1.5% at room temperature and typically ±2% over-temperature, load current and line voltage shifts. The RC5053 uses a synchronous switching architecture with two external N-channel output devices, providing high efficiency and eliminating the need for a high power, high cost P-channel device. Additionally, it senses the output current across the on-resistance of the upper N-channel MOSFET, providing an adjustable current limit without an external low value sense resistor.

The RC5053 free-runs at 300kHz and can be synchronized to a faster external clock if desired. It includes all the inputs and outputs required to implement a power supply conforming to the Intel Pentium® II Processor VRM 8.2 DC/DC Converter Specification.

Block Diagram



Pin Assignment



G PACKAGE
20-LEAD PLASTIC SSOP

M PACKAGE
20-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 130°C/W(F)
T_{JMAX} = 125°C, θ_{JA} = 85.2°C/W(M)

Pin Definitions

Pin Number	Pin Name	Pin Description
1	G2	**Gate Drive for the Lower N-Channel MOSFET, Q2.** This output will swing from PV_{CC} to GND. It will always be low when G1 is high or when the output is disabled. To prevent undershoot during a soft start cycle, G2 is held low until G1 first goes high.
2	PV_{CC}	**Power Supply for G1 and G2.** PV_{CC} must be connected to a potential of at least V_{IN} + $V_{GS(ON)Q1}$. If V_{IN} = 5V, PV_{CC} can be generated using a simple charge pump connected to the switching node between Q1 and Q2 (see Figure 7), or it can be connected to an auxiliary 12V supply if one exists.
3	GND	**Power Ground.** GND should be connected to a low impedance ground plane in close proximity to the source of Q2.
4	SGND	**Signal Ground.** SGND is connected to the low power internal circuitry and should be connected to the negative terminal of the output capacitor where it returns to the ground plane. GND and SGND should be shorted right at the RC5053.
5	V_{CC}	**Power Supply.** Power for the internal low power circuitry. V_{CC} should be wired separately from the drain of Q1 if they share the same supply. A 10µF bypass capacitor is recommended from this pin to SGND.
6	SENSE	**Output Voltage Pin.** Connect to the positive terminal of the output capacitor. There is an internal 120k resistor connected from this pin to SGND. SENSE is a very sensitive pin; for optimum performance, connect an external 0.1µF capacitor from this pin to SGND. By connecting a small external resistor between the output capacitor and the SENSE pin, the initial output voltage can be raised slightly. Since the internal divider has a nominal impedance of 120kΩ, a 1200Ω series resistor will raise the nominal output voltage by 1%. If an external resistor is used, the value of the 0.1µF capacitor on the SENSE pin must be greatly reduced or loop phase margin will suffer. Set a time constant for the RC combination of approximately 0.1µs. So, for example, with a 1200Ω resistor, set C = 83pF. Use a standard 100pF capacitor.
7	I_{MAX}	**Current Limit Threshold.** Current limit is set by the voltage drop across an external resistor connected between the drain of Q1 and I_{MAX}. There is a 180µA internal pull-down at I_{MAX}.

Pin Definitions (continued)

Pin Number	Pin Name	Pin Description
8	I_{FB}	**Current Limit Sense Pin.** Connect to the switching node between the source of Q1 and the drain of Q2. If I_{FB} drops below I_{MAX} when G1 is on, the RC5053 will go into current limit. The current limit circuit can be disabled by floating I_{MAX} and shorting I_{FB} to V_{CC} through an external 10k resistor.
9	SS	**Soft Start.** Connect to an external capacitor to implement a soft start function. During moderate overload conditions, the soft start capacitor will be discharged slowly in order to reduce the duty cycle. In hard current limit, the soft start capacitor will be forced low immediately and the RC5053 will rerun a complete soft start cycle. C_{SS} must be selected such that during power-up the current through Q1 will not exceed the current limit value.
10	COMP	**External Compensation.** The COMP pin is connected directly to the output of the error amplifier and the input of the PWM comparator. An RC+ C network is used at this node to compensate the feedback loop to provide optimum transient response.
11	$\overline{OT}$	**Over-Temperature Fault.** $\overline{OT}$ is an open-drain output and will be pulled low if OUTEN is less than 2V.
12	$\overline{FAULT}$	**Overvoltage Fault.** $\overline{FAULT}$ is an open-drain output. If V_{OUT} reaches 15% above the nominal output voltage, $\overline{FAULT}$ will go low and G1 and G2 will be disabled. Once triggered, the RC5053 will remain in this state until the power supply is recycled or the OUTEN pin is toggled. If OUTEN = 0, $\overline{FAULT}$ floats or is pulled high by an external resistor.
13	PWRGD	**Power Good.** This is an open-drain signal to indicate validity of output voltage. A high indicates that the output has settled to within ±5% of the rated output for more than 1ms. PWRGD will go low if the output is out of regulation for more than 500µs. If OUTEN = 0, PWRGD pulls low.
18, 17, 16, 15, 14	VID0, VID1, VID2, VID3, VID4	**Digital Voltage Select.**TTL inputs used to set the regulated output voltage required by the processor (Table 3). There is an internal 20kΩ pull-up at each pin. When all five VIDn pins are high or floating, the chip will shut down.
19	OUTEN	**Output Enable.** TTL input which enables the output voltage.The external MOSFET temperature can be monitored with an external thermistor as shown in Figure 6. When the OUTEN input voltage drops below 2V, $\overline{OT}$ trips. As OUTEN drops below 1.7V, the drivers are internally disabled to prevent the MOSFETs from heating further. If OUTEN is less than 1.2V for longer than 30µs, the RC5053 will enter shutdown mode. The internal oscillator can be synchronized to a faster external clock by applying the external clocking signal to the OUTEN pin.
20	G1	**Gate Drive for the Upper N-Channel MOSFET, Q1.**This output will swing from PV_{CC} to GND. It will always be low when G2 is high or the output is disabled.

Absolute Maximum Ratings[1]

Parameter	Min.	Typ.	Max.
Supply Voltage			
V_{CC}			7V
PV_{CC}			13.5V
Input Voltage			
I_{FB} (Note 2)			PV_{CC} + 0.3V
I_{MAX}	-0.3V		13V
All Other Inputs	-0.3V		V_{CC} + 0.3V

Absolute Maximum Ratings[1] (continued)

Parameter	Min.	Typ.	Max.
Digital Output Voltage	-0.3V		7V
I_{FB} Input Current (Notes 2, 3)	-100mA		
Operating Temperature Range	0°C		70°C
Storage Temperature Range	-65°C		150°C
Lead Temperature (Soldering, 10 sec.)			300°C

Electrical Characteristics (V_{CC} = 5V, PV_{CC} = 12V, T_A = 25°C, unless otherwise noted.)[3]

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
V_{CC}	Supply Voltage		•	4.5		5.5	V
PV_{CC}	Supply Voltage for G1, G2		•			13.2	V
V_{OUT}	1.8V Initial Output Voltage	With Respect to Rated Output Voltage (Fig. 2)			±1.5%		mV
	2.8V Initial Output Voltage				±1.5%		mV
	3.5V Initial Output Voltage				±1.5%		mV
	1.8V Initial Output Voltage		•		±2%		mV
	2.8V Initial Output Voltage		•		±2%		mV
	3.5V Initial Output Voltage		•		±2%		mV
ΔV_{OUT}	Output Load Regulation	I_{OUT} = 0 to 14A (Fig. 2)			-5		mV
	Output Line Regulation	V_{CC} = 4.75V to 5.25V (Fig. 2)			±1		mV
V_{PWRGD}	Positive Power Good Trip Point	% Above Output Voltage (Fig. 2)	•		5	10	%
	Negative Power Good Trip Point	% Below Output Voltage (Fig. 2)	•	-10	-5		%
V_{FAULT}	$\overline{FAULT}$ Trip Point	% Above Output Voltage (Fig. 2)	•	10	15	20	%
I_{CC}	Operating Supply Current	OUTEN = V_{CC} = 5V[4] (Fig. 3)	•		2.0	3.0	mA
	Shutdown Supply Current	OUTEN = 0, VID0 to VID4 Floating (Fig. 3)	•		760	1500	µA
I_{PVCC}	Supply Current	PV_{CC} = 12V, OUTEN = V_{CC}[5] (Fig. 3)			26		mA
		PV_{CC} = 12V, OUTEN = 0, VID0 to VID4 Floating			430		µA
f_{OSC}	Internal Oscillator Frequency	(Fig. 4)	•	250	300	350	kHz
V_{SAWL}	V_{COMP} at Minimum Duty Cycle				1.8		V
V_{SAWH}	V_{COMP} at Maximum Duty Cycle				2.8		V
G_{ERR}	Error Amplifier Open-Loop DC Gain		•	40	53		dB
g_{mERR}	Error Amplifier Transconductance		•	0.7	1.3	1.9	mmho

Electrical Characteristics (V_{CC} = 5V, PV_{CC} = 12V, T_A = 25°C, unless otherwise noted.)[3] (continued)

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
BW_{ERR}	Error Amplifier -3dB Bandwidth	COMP = Open			400		kHz
I_{IMAX}	I_{MAX} Sink Current	$V_{IMAX} = V_{CC}$	•	150	180	220	µA
I_{SS}	Soft Start Source Current	V_{SS} = 0.4V, V_{IMAX} = 0V, $V_{IFB} = V_{CC}$	•	-13	-10	-7	µA
I_{SSIL}	Maximum Soft Start Sink Current Under Current Limit	$V_{SENSE} = V_{OUT}$, $V_{IMAX} = V_{CC}$, V_{IFB} = 0V[6, 7], $V_{SS} = V_{CC}$	•	30	60	150	µA
I_{SSHIL}	Soft Start Sink Current Under Hard Current Limit	V_{SENSE} = 0V, $V_{IMAX} = V_{CC}$, V_{IFB} = 0V, $V_{SS} = V_{CC}$	•	20	45		mA
t_{SSHIL}	Hard Current Limit Hold Time	V_{SENSE} = 0V, V_{IMAX} = 4V, $V_{IFB}\downarrow$ from 5V			500		µs
t_{PWRGD}	Power Good Response Time↑	$V_{SENSE}\uparrow$ from 0V to Rated V_{OUT}	•	0.5	1	2	ms
t_{PWRBAD}	Power Good Response Time↓	$V_{SENSE}\downarrow$ from Rated V_{OUT} to 0V	•	200	500	1000	µs
t_{FAULT}	$\overline{FAULT}$ Response Time	$V_{SENSE}\uparrow$ from Rated V_{OUT} to V_{CC}	•	200	500	1000	µs
t_{OT}	$\overline{OT}$ Response Time	OUTEN↓, VID0 to VID4 = 0 (Fig. 3)[8]	•	15	40	60	µs
V_{OT}	Over-Temperature Trip Point	OUTEN↓, VID0 to VID4 = 0 (Fig. 3)[8]	•	1.9	2	2.12	V
V_{OTDD}	Over-Temperature Driver Disable	OUTEN↓, VID0 to VID4 = 0 (Fig. 3)[8]	•	1.6	1.7	1.8	V
V_{SHDN}	Shutdown	OUTEN↓, VID0 to VID4 = 0 (Fig. 3)[8]	•	0.8	1.2	1.5	V
t_r, t_f	Driver Rise and Fall Time	(Figure 4)	•		90	150	ns
t_{NOL}	Driver Nonoverlap Time	(Figure 4)	•	30	100		ns
DC_{MAX}	Maximum G1 Duty Cycle	(Figure 4)	•	77	82	88	%
V_{IH}	VID0 to VID4 = 1 Input High Voltage		•	2			V
V_{IL}	VID0 to VID4 = 0 Input Low Voltage		•			0.8	V
R_{IN}	VID0 to VID4 = 0 Internal Pull-Up Resistance		•	10	20		kΩ
I_{SINK}	Digital Output Sink Current		•	10			mA

The • denotes specifications which apply over the full operating temperature range.

Notes:

1. Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.
2. When I_{FB} is taken below GND, it will be clamped by an internal diode. This pin can handle input currents greater than 100mA below GND without latchup. In the positive direction, it is not clamped to V_{CC} nor PV_{CC}.
3. All currents into device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.
4. The RC5053 goes into the shutdown mode if VID0 to VID4 are floating. Due to the internal pull-up resistors, there will be an additional 0.25mA/pin if any of the VID0 to VID4 pins are pulled low.
5. Supply current in normal operation is dominated by the current needed to charge and discharge the external FET gates. This will vary with the RC5053 operating frequency, supply voltage and the external FETs used.
6. The current limiting amplifier can sink but cannot source current. Under normal (not current limited) operation, the output current will be zero.
7. Under typical soft current limit, the net soft start discharge current will be 60µA (I_{SSIL}) + [-10µA(I_{SS})] = 50µA. The soft start sink-to-source current ratio is designed to be 6:1.
8. When VID0 to VID4 are all HIGH, the RC5053 will be forced to shut down internally. The OUTEN trip voltages are guaranteed by design for all other input codes.

Typical Application

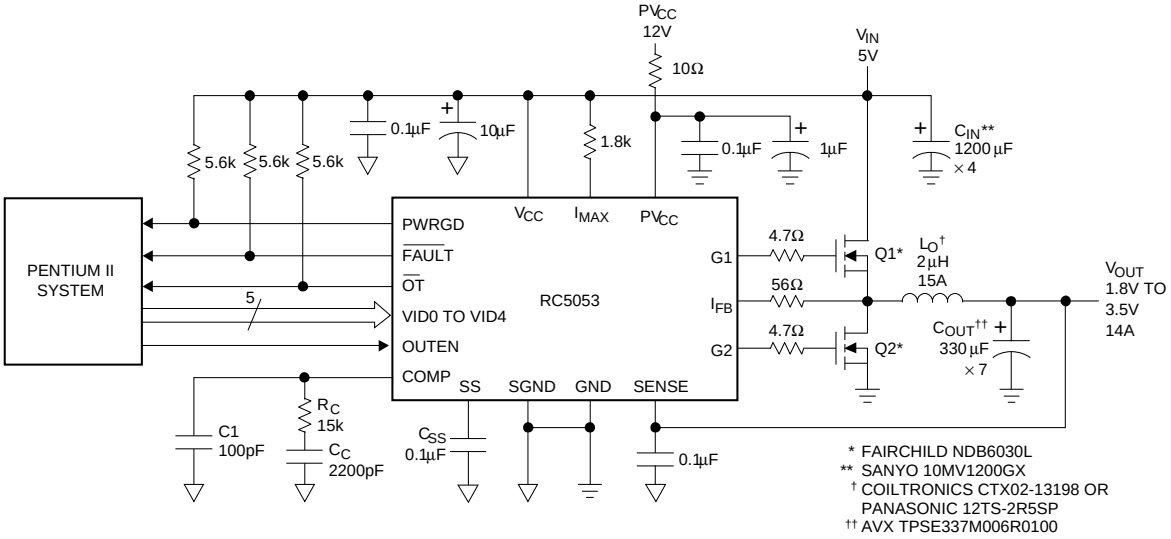


Figure 1. 5V to 1.8V-3.5V Supply Application

Test Circuits

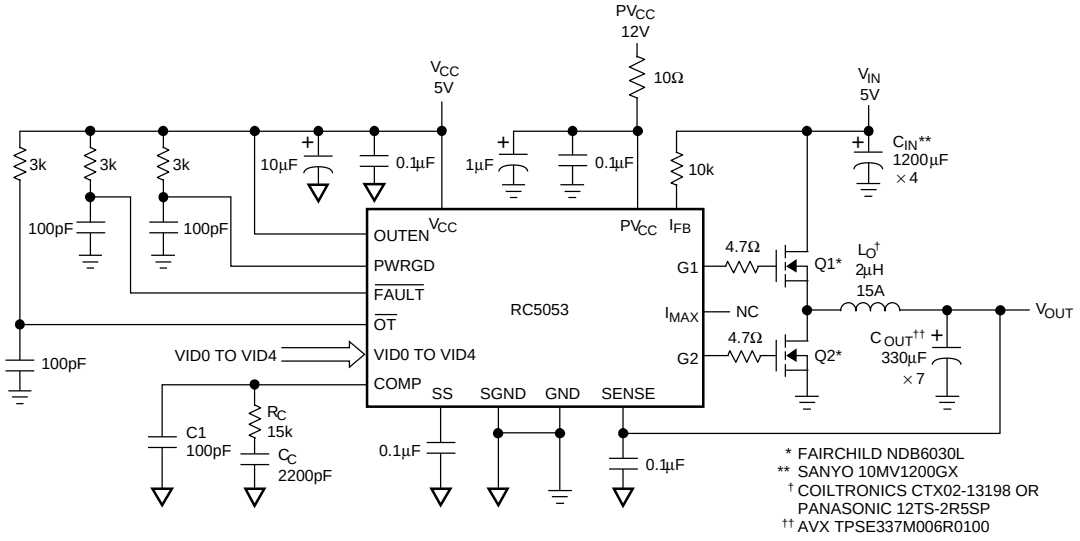


Figure 2

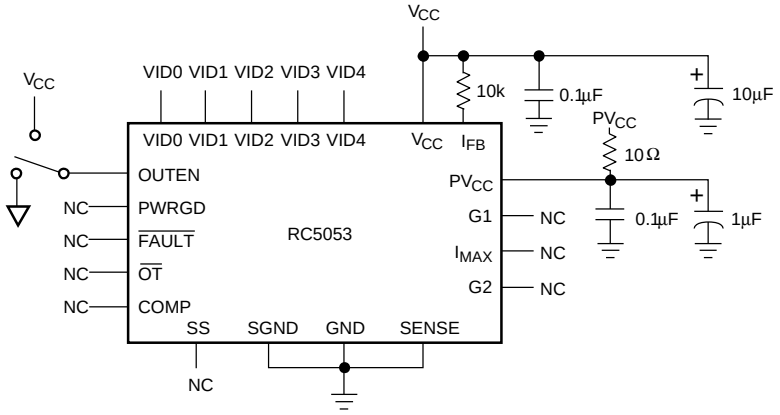


Figure 3

Test Circuits (continued)

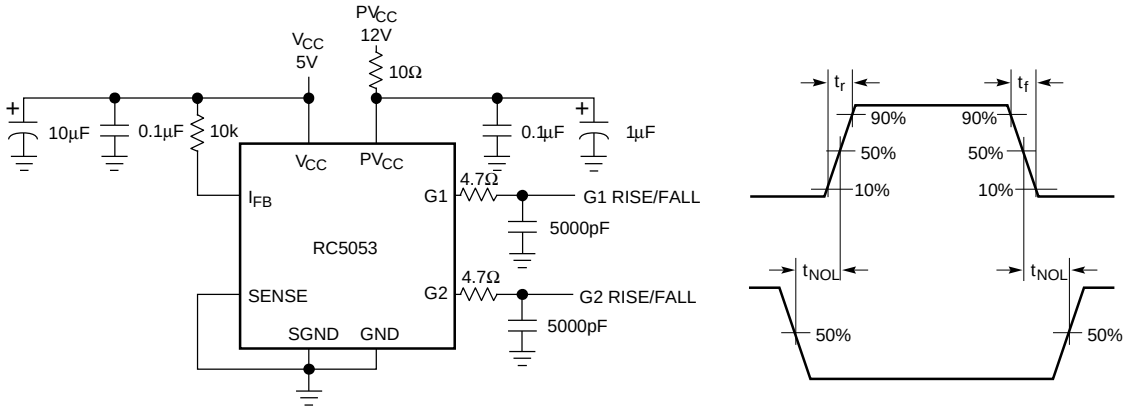


Figure 4

Function Tables

Table 1. $\overline{OT}$ Logic

OUTEN (V)	$\overline{OT}$[1]
< 2	0
> 2	1

Note:
1. With external pull-up resistor

Table 2. PWRGD and $\overline{FAULT}$ Logic

Input		Output[1]		
OUTEN	V_{SENSE}[2]	$\overline{OT}$	$\overline{FAULT}$	PWRGD
0	X	0	1	0
1	< 95%	1	1	0
1	> 95% < 105%	1	1	1
1	>105%	1	1	0
1	> 115%	1	0	0

Notes:
1. With external pull-up resistor
2. With respect to the output voltage selected in Table 3 as required by Intel Specification VRM 8.2
3. X = Don't care

Table 3. Rated Output Voltage

Input Pin					Rated Output Voltage (V)
V_{ID4}	V_{ID3}	V_{ID2}	V_{ID1}	V_{ID0}	
0	1	1	1	1	Disabled[1] (1.30)
0	1	1	1	0	Disabled[1] (1.35)
0	1	1	0	1	Disabled[1] (1.40)
0	1	1	0	0	Disabled[1] (1.45)
0	1	0	1	1	Disabled[1] (1.50)
0	1	0	1	0	Disabled[1] (1.55)
0	1	0	0	1	Disabled[1] (1.60)

Table 3. Rated Output Voltage (continued)

Input Pin					Rated Output Voltage (V)
V_{ID4}	V_{ID3}	V_{ID2}	V_{ID1}	V_{ID0}	
0	1	0	0	0	Disabled[1] (1.65)
0	0	1	1	1	Disabled[1] (1.70)
0	0	1	1	0	Disabled[1] (1.75)
0	0	1	0	1	1.80
0	0	1	0	0	1.85
0	0	0	1	1	1.90
0	0	0	1	0	1.95
0	0	0	0	1	2.00
0	0	0	0	0	2.05
1	1	1	1	1	SHDN
1	1	1	1	0	2.1
1	1	1	0	1	2.2
1	1	1	0	0	2.3
1	1	0	1	1	2.4
1	1	0	1	0	2.5
1	1	0	0	1	2.6
1	1	0	0	0	2.7
1	0	1	1	1	2.8
1	0	1	1	0	2.9
1	0	1	0	1	3.0
1	0	1	0	0	3.1
1	0	0	1	1	3.2
1	0	0	1	0	3.3
1	0	0	0	1	3.4
1	0	0	0	0	3.5

Notes:
1. These code selections are disabled in RC5053

Applications Information

Overview

The RC5053 is a voltage feedback, synchronous switching regulator controller (see Block Diagram) designed for use in high power, low voltage step-down (buck) converters. It is designed to satisfy the requirements of the Intel Pentium II power supply specification. It includes an on-chip DAC to control the output voltage, a PWM generator, a precision reference trimmed to ±1%, two high power MOSFET gate drivers and all the necessary feedback and control circuitry to form a complete switching regulator circuit.

The RC5053 includes a current limit sensing circuit that uses the upper external power MOSFET as a current sensing element, eliminating the need for an external sense resistor. Once the current comparator, CC, detects an overcurrent condition, the duty cycle is reduced by discharging the soft start capacitor through a voltage-controlled current source. Under severe overloads or output short circuit conditions, the chip will be repeatedly forced into soft start until the short is removed, preventing the external components from being damaged. Under output over-voltage conditions, the MOSFET drivers will be disabled permanently until the chip power supply is recycled or the OUTEN pin is toggled.

OUTEN can optionally be connected to an external negative temperature coefficient (NTC) thermistor placed near the external MOSFETs or the microprocessor. Three threshold levels are provided internally. When OUTEN drops to 2V, $\overline{OT}$ will trip, issuing a warning to the external CPU. If the temperature continues to rise and the OUTEN input drops to 1.7V, the G1 and G2 pins will be forced low. If OUTEN is pulled below 1.2V, the RC5053 will go into shutdown mode, cutting the supply current to a minimum. If thermal shutdown is not required, OUTEN can be connected to a conventional TTL enable signal. The free-running 300kHz PWM frequency can be synchronized to a faster external clock

connected to OUTEN. Adjusting the oscillator frequency can add flexibility in the external component selection. See the Clock Synchronization section.

Output regulation can be monitored with the PWRGD pin which in turn monitors the internal MIN and MAX comparators. If the output is ±5% beyond the selected value for more than 500µs, the PWRGD output will be pulled low. Once the output has settled within ±5% of the selected value for more than 1ms, PWRGD will return high.

Theory of Operation

Primary Feedback Loop

The regulator output voltage at the SENSE pin is divided down internally by a resistor divider with a total resistance of approximately 120kΩ. This divided down voltage is subtracted from a reference voltage supplied by the DAC output. The resulting error voltage is amplified by the error amplifier and the output is compared to the oscillator ramp waveform by the PWM comparator. This PWM signal controls the external MOSFETs through G1 and G2. The resulting chopped waveform is filtered by L_O and C_{OUT} closing the loop. Loop frequency compensation is achieved with an external RC + C network at the COMP pin, which is connected to the output node of the transconductance amplifier.

MIN, MAX Feedback Loops

Two additional comparators in the feedback loop provide high speed fault correction in situations where the ERR amplifier may not respond quickly enough. MIN compares the feedback signal FB to a voltage 60mV (5%) below the internal reference. If FB is lower than the threshold of this comparator, the MIN comparator overrides the ERR amplifier and forces the loop to full duty cycle which is set by the internal oscillator typically to 82%. Similarly, the MAX comparator forces the output to 0% duty cycle if FB is more than 5% above the internal reference. To prevent these two comparators from triggering due to noise, the MIN and MAX comparators' response times are deliberately controlled so that they take two or three microseconds to respond. These two comparators help prevent extreme output perturbations with fast output transients, while allowing the main feedback loop to be optimally compensated for stability.

Soft Start and Current Limit

The RC5053 includes a soft start circuit which is used for initial start-up and during current limit operation. The SS pin requires an external capacitor to SGND with the value determined by the required soft start time. An internal 10µA current source is included to charge the external SS capacitor. During start-up, the COMP pin is clamped to a diode drop above the voltage at the SS pin. This prevents the error amplifier, ERR, from forcing the loop to maximum duty cycle. The RC5053 will begin to operate at low duty cycle as the SS pin rises above about 1.2V ($V_{COMP} \approx 1.8V$). As SS continues to rise, Q_{SS} turns off and the error amplifier begins to regulate the output.The MIN comparator is disabled when soft start is active to prevent it from overriding the soft start function.

The RC5053 includes yet another feedback loop to control operation in current limit. Just before every falling edge of G1, the current comparator, CC, samples and holds the voltage drop measured across the external MOSFET, Q1, at the I_{FB} pin. CC compares the voltage at I_{FB} to the voltage at the I_{MAX} pin. As the peak current rises, the measured voltage across Q1 increases due to the drop across the $R_{DS(ON)}$ of Q1.When the voltage at I_{FB} drops below I_{MAX}, indicating that Q1's drain current has exceeded the maximum level, CC starts to pull current out of the external soft start capacitor, cutting the duty cycle and controlling the output current level. The CC comparator pulls current out of the SS pin in proportion to the voltage difference between I_{FB} and I_{MAX}. Under minor overload conditions, the SS pin will fall gradually, creating a time delay before current limit takes effect. Very short, mild overloads may not affect the output voltage at all. More significant overload conditions will allow the SS pin to reach a steady state, and the output will remain at a reduced voltage until the overload is removed. Serious overloads will generate a large overdrive at CC, allowing it to pull SS down quickly and preventing damage to the output components.

By using the $R_{DS(ON)}$ of Q1 to measure the output current, the current limiting circuit eliminates an expensive discrete sense resistor that would otherwise be required. This helps minimize the number of components in the high current path. Due to switching noise and variation of $R_{DS(ON)}$, the actual current limit trip point is not highly accurate. The current limiting circuitry is primarily meant to prevent damage to the power supply circuitry during fault conditions. The exact current level where the limiting circuit begins to take effect will vary from unit to unit as the $R_{DS(ON)}$ of Q1 varies.

For a given current limit level, the external resistor from I_{MAX} to V_{IN} can be determined by:

$$R_{IMAX} = \frac{(I_{LMAX})(R_{DS(ON)Q1})}{I_{IMAX}}$$

where,

$$I_{LMAX} = I_{LOAD} + \frac{I_{RIPPLE}}{2}$$

I_{LOAD} = Maximum load current;
I_{RIPPLE} = Inductor ripple current

$$= \frac{(V_{IN} - V_{OUT})(V_{OUT})}{(f_{OSC})(L_O)(V_{IN})}$$

f_{OSC} = RC5053 oscillator frequency = 300kHz
L_O = Inductor value
$R_{DS(ON)Q1}$ = Hot on-resistance of Q1 at I_{LMAX}
I_{IMAX} = Internal 180µA sink current at I_{MAX}

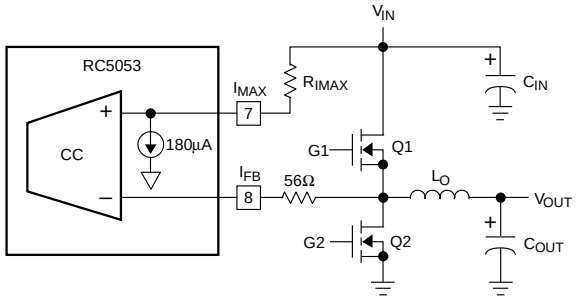


Figure 5. Current Limit Setting

OUTEN and Thermistor Input

The RC5053 includes a low power shutdown mode, controlled by the logic at the OUTEN pin. A high at OUTEN allows the part to operate normally. A low level at OUTEN stops all internal switching, pulls COMP and SS to ground internally and turns Q1 and Q2 off. $\overline{OT}$ and PWRGD are pulled low, and $\overline{FAULT}$ is left floating. In shutdown, the RC5053 quiescent current will drop to about 760µA. The remaining current is used to keep the thermistor sensing circuit at OUTEN alive. Note that the leakage current of the external MOSFETs may add to the total shutdown current consumed by the circuit, especially at elevated temperature.

OUTEN is designed with multiple thresholds to allow it to also be utilized for over-temperature protection. The power MOSFET operating temperature can be monitored with an external negative temperature coefficient (NTC) thermistor mounted next to the external MOSFET which is expected to run the hottest —often the high-side device, Q1. Electrically, the thermistor should form a voltage divider with another resistor, R1, connected to V_{CC}. Their midpoint should be connected to OUTEN (see Figure 6). As the temperature increases, the OUTEN pin voltage is reduced. Under normal operating conditions, the OUTEN pin should stay above 2V. All circuits will function normally, and the $\overline{OT}$ pin will remain in a high state. If the temperature gets abnormally high, the OUTEN pin voltage will eventually drop below 2V. $\overline{OT}$ will switch to a logic low, providing an over-temperature warning to the system. As OUTEN drops below 1.7V, the RC5053 disables both FET drivers. If OUTEN is less than 1.2V, the RC5053 will enter shutdown mode. To activate any of these three modes, the OUTEN voltage must drop below the respective threshold for longer than 30µs.

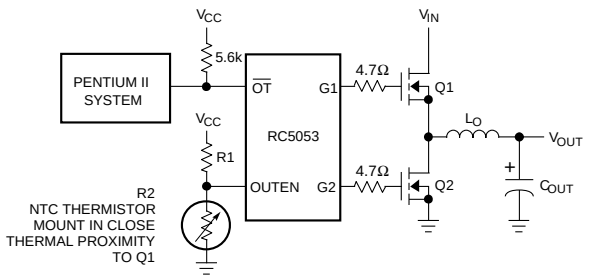


Figure 6. OUTEN Pin as a Thermistor Input

Clock Synchronization

The internal oscillator can be synchronized to an external clock by applying the external clocking signal to the OUTEN pin. The synchronizing range extends from the initial operating frequency up to 500kHz. If the external frequency is much higher than the natural free-running frequency, the peak-to-peak sawtooth amplitude within the RC5053 will decrease. Since the loop gain is inversely proportional to the amplitude of the sawtooth, the compensation network may need to be adjusted slightly. Note that the temperature sensing circuitry does not operate when external synchronization is used.

MOSFET Gate Drive

Power for the internal MOSFET drivers is supplied by PV_{CC}. This supply must be above the input supply voltage by at least one power MOSFET $V_{GS(ON)}$ for efficient operation. This higher voltage can be supplied with a separate supply, or it can be generated using a simple charge pump as shown in Figure 7. The 82% typical maximum duty cycle ensures sufficient off-time to refresh the charge pump during each cycle.

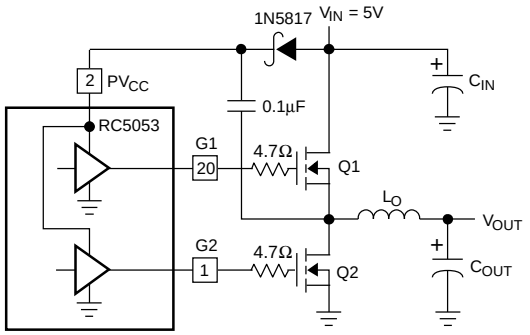


Figure 7. Doubling Charge Pump

Upon power-down, G1 and G2 will both be held low to prevent output voltage under shoot. On power-up or wake-up from thermal shutdown, the driver is designed such G2 will be held low until after G1 first goes high.

Power MOSFETs

Two N-channel power MOSFETs are required for most RC5053 circuits. They should be selected based primarily on gate threshold and on-resistance considerations. The required MOSFET threshold should be determined based on the available power supply voltages and/or the complexity of the gate driver charge pump scheme. In 5V input designs where a 12V supply is used to power PV_{CC}, standard MOSFETs with $R_{DS(ON)}$ specified at V_{GS} = 5V or 6V can be used with good results. However, logic level devices will improve efficiency. The current drawn from the 12V supply varies with the MOSFETs used and the RC5053 operating frequency, but is generally less than 50mA.

RC5053 designs that use a 5V V_{IN} voltage and a doubler charge pump to generate PV_{CC} will not provide enough drive voltage to fully enhance standard power MOSFETs. Under this condition, the effective MOSFET $R_{DS(ON)}$ may be quite high, raising the dissipation in the MOSFETs and reducing efficiency. Logic level MOSFETs are a better choice for 5V-only systems. They can be fully enhanced with the generated charge pump voltage and will operate at maximum efficiency. See the MOSFET Gate Drive section for more charge pump information.

Once the threshold voltage has been selected, $R_{DS(ON)}$ should be chosen based on input and output voltage, allowable power dissipation and maximum required output current. In a typical RC5053 buck converter circuit the average inductor current is equal to the output load current. This current is always flowing through either Q1 or Q2 with the power dissipation split up according to the duty cycle:

$$DC(Q1) = \frac{V_{OUT}}{V_{IN}}$$

$$DC(Q2) = 1 - \frac{V_{OUT}}{V_{IN}} = \frac{(V_{IN} - V_{OUT})}{V_{IN}}$$

The $R_{DS(ON)}$ required for a given conduction loss can now be calculated by rearranging the relation $P = I^2 R$.

$$R_{DS(ON)Q1} = \frac{P_{MAX(Q1)}}{[DC(Q1)](I_{MAX})^2} = \frac{(V_{IN})[P_{MAX(Q1)}]}{(V_{OUT})(I_{MAX})^2}$$

$$R_{DS(ON)Q2} = \frac{P_{MAX(Q2)}}{[DC(Q2)](I_{MAX})^2} = \frac{(V_{IN})[P_{MAX(Q2)}]}{(V_{IN} - V_{OUT})(I_{MAX})^2}$$

P_{MAX} should be calculated based primarily on required efficiency or allowable thermal dissipation. A typical high efficiency circuit designed for Pentium II with a 5V input and a 2.0V, 14.2A output might allow no more than 4% loss at full load for each MOSFET. Assuming roughly 90% efficiency at this current level, this gives a P_{MAX} value of:

[(2.0)(14.2A/0.9)(0.04)] = 1.26W per MOSFET
and a required $R_{DS(ON)}$ of:

$$R_{DS(ON)Q1} = \frac{(5V)(1.26W)}{(2.0V)(14.2A)^2} = 0.016\Omega$$

$$R_{DS(ON)Q2} = \frac{(5V)(1.26W)}{(5V - 2.0V)(14.2A)^2} = 0.010\Omega$$

Note also that while the required $R_{DS(ON)}$ values suggest large MOSFETs, the dissipation numbers are only 1.26W per device or less—large TO-220 packages and heat sinks are not necessarily required in high efficiency applications. Fairchild NDB6030L are small footprint surface mount devices with $R_{DS(ON)}$ values below 0.03Ω at 5V of gate drive that work well in RC5053 circuits. With lower output voltages, the $R_{DS(ON)}$ of Q2 may need to be significantly lower than that for Q1. These conditions can often be met by paralleling two MOSFETs for Q2 and using a single device for Q1. Note that using a higher P_{MAX} value in the $R_{DS(ON)}$ calculations will generally decrease MOSFET cost and circuit efficiency while increasing MOSFET heat sink requirements.

Inductor Selection

The inductor is often the largest component in the RC5053 design and should be chosen carefully. Inductor value and type should be chosen based on output slew rate requirements, output ripple requirements and expected peak current. Inductor value is primarily controlled by the required current slew rate. The maximum rate of rise of current in the inductor is set by its value, the input-to-output voltage differential and the maximum duty cycle of the RC5053. In a typical 5V input, 2.0V output application, the maximum current slew rate will be:

$$DC_{MAX}\frac{(V_{IN} - V_{OUT})}{L} = \frac{2.46}{L} \quad \frac{A}{\mu s}$$

where L is the inductor value in µH. With proper frequency compensation, the combination of the inductor and output capacitor will determine the transient recovery time. In general, a smaller value inductor will improve transient response at the expense of increased output ripple voltage and inductor core saturation rating. A 2µH inductor would have a 1.23A/µs rise time in this application, resulting in a 4.1µs delay in responding to a 5A load current step. During this 4.1µs, the difference between the inductor current and the output current must be made up by the output capacitor, causing a temporary voltage droop at the output. To minimize this effect, the inductor value should usually be in the 1µH to 5µH range for most typical 5V input RC5053 circuits. To optimize performance, different combinations of input and output voltages and expected loads may require different inductor values.

Once the required value is known, the inductor core type can be chosen based on peak current and efficiency requirements. Peak current in the inductor will be equal to the maximum output load current plus half of the peak-to- peak inductor ripple current. Ripple current is set by the inductor value, the input and output voltage and the operating frequency. The ripple current is approximately equal to:

$$I_{RIPPLE} = \frac{(V_{IN} - V_{OUT})(V_{OUT})}{(f_{OSC})(L_O)(V_{IN})}$$

f_{OSC} = RC5053 oscillator frequency = 300kHz
L_O = Inductor value

Solving this equation with our typical 5V to 2.0V application with a 2µH inductor, we get:

$$\frac{(3.0)(0.40)}{(300kHz)(2\mu H)} = 2A_{p\text{-}p}$$

Peak inductor current at 14.2A load:

$$14.2A + \frac{2A}{2} = 15.2A$$

The ripple current should generally be between 10% and 40% of the output current. The inductor must be able to withstand this peak current without saturating, and the copper resistance in the winding should be kept as low as possible to minimize resistive power loss. Note that in noncurrent limited circuits, the current in the inductor may rise above this maximum under short circuit or fault conditions; the inductor should be sized accordingly to withstand this additional current. Inductors with gradual saturation characteristics are often the best choice.

Input and Output Capacitors

A typical RC5053 design puts significant demands on both the input and the output capacitors. During constant load operation, a buck converter like the RC5053 draws square waves of current from the input supply at the switching frequency. The peak current value is equal to the output load current plus 1/2 peak-to-peak ripple current, and the minimum value is zero. Most of this current is supplied by the input bypass capacitor. The resulting RMS current flow in the input capacitor will heat it up, causing premature capacitor failure in extreme cases. Maximum RMS current occurs with 50% PWM duty cycle, giving an RMS current value equal to $I_{OUT}/2$. A low ESR input capacitor with an adequate ripple current rating must be used to ensure reliable operation.

Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours (three months) lifetime at rated temperature. Further derating of the input capacitor ripple current beyond the manufacturer's specification is recommended to extend the useful life of the circuit. Lower operating temperature will have the largest effect on capacitor longevity.

The output capacitor in a buck converter sees much less ripple current under steady-state conditions than the input capacitor. Peak-to-peak current is equal to that in the inductor, usually 10% to 40% of the total load current. Output capacitor duty places a premium not on power dissipation but on ESR. During an output load transient, the output capacitor must supply all of the additional load current demanded by the load until the RC5053 can adjust the inductor current to the new value. Output capacitor ESR results in a step in the output voltage equal to the ESR value multiplied by the change in load current. An 11A load step with a 0.05Ω ESR output capacitor will result in a 550mV output voltage shift; this is 27.5% of the output voltage for a 2.0V supply! Because of the strong relationship between output capacitor ESR and output load transient response, the output capacitor is usually chosen for ESR, not for capacitance value; a capacitor with suitable ESR will usually have a larger capacitance value than is needed for energy storage.

Electrolytic capacitors rated for use in switching power supplies with specified ripple current ratings and ESR can be used effectively in RC5053 applications. OS-CON electrolytic capacitors from SANYO and other manufacturers give excellent performance and have a very high performance/size ratio for electrolytic capacitors. Surface mount applications can use either electrolytic or dry tantalum capacitors. Tantalum capacitors must be surge tested and specified for use in switching power supplies. Low cost, generic tantalums are known to have very short lives followed by explosive deaths in switching power supply applications. AVX TPS series surface mount devices are popular surge tested tantalum capacitors that work well in RC5053 applications.

A common way to lower ESR and raise ripple current is to parallel several capacitors. A typical RC5053 application might exhibit 5A input ripple current. SANYO OS-CON part number 10SA220M (220µF/10V) capacitors feature 2.3A allowable ripple current at 85°C; three in parallel at the input (to withstand the input ripple current) will meet the above requirements. Similarly, AVX TPSE337M006R0100 (330µF/6V) have a rated maximum ESR of 0.1Ω; seven in parallel will lower the net output capacitor ESR to 0.014Ω. For low cost application, SANYO MV-GX series of capacitors can be used with acceptable performance.

Feedback Loop Compensation

The RC5053 voltage feedback loop is compensated at the COMP pin, attached to the output node of the internal gm error amplifier. The feedback loop can generally be compensated properly with an RC + C network from COMP to GND as shown in Figure 8a.

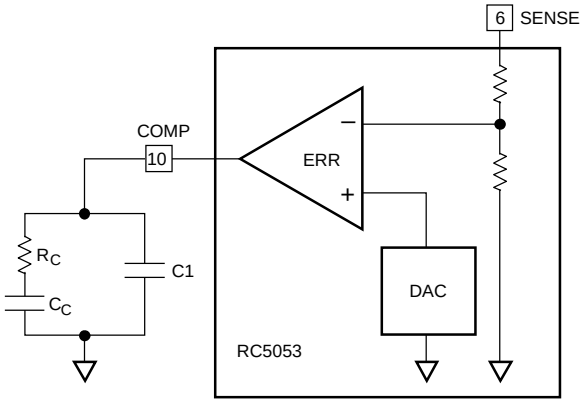


Figure 8a. Compensation Pin Hook-Up

Loop stability is affected by the values of the inductor, output capacitor, output capacitor ESR, error amplifier transconductance and error amplifier compensation network. The inductor and the output capacitor creates a double pole at the frequency:

$$f_{LC} = \frac{1}{2\pi\sqrt{(L_O)(C_{OUT})}}$$

The ESR of the output capacitor forms a zero at the frequency:

$$f_{ESR} = \frac{1}{2\pi(ESR)(C_{OUT})}$$

The compensation network at the error amplifier output is to provide enough phase margin at the 0dB crossover frequency for the overall closed-loop transfer function. The zero and pole from the compensation network are:

$$f_Z = \frac{1}{2\pi(R_C)(C_C)} \text{ and } f_P = \frac{1}{2\pi(R_C)(C1)} \text{ respectively.}$$

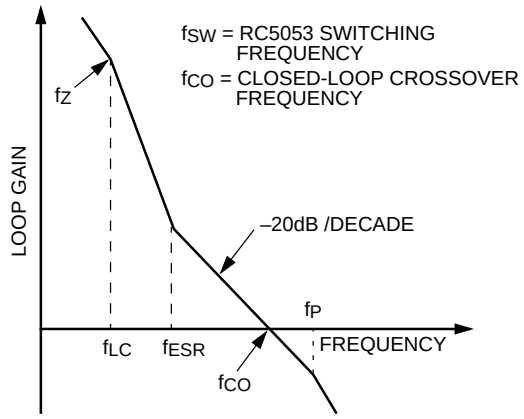


Figure 8b. Bode Plot of the RC5053 Overall Transfer Function

Figure 8b shows the Bode plot of the overall transfer function. The compensation value used in this design is based on the following criteria: $f_{SW} = 12f_{CO}$, $f_Z = f_{LC}$ and $f_P = 5f_{CO}$. At the closed-loop frequency f_{CO}, the attenuation due the LC filter and the input resistor divider is compensated by the gain of the PWM modulator and the gain of the error amplifier $(g_{mERR})(R_C)$.

Although a mathematical approach to frequency compensation can be used, the added complication of input and/or output filters, unknown capacitor ESR, and gross operating point changes with input voltage, load current variations, all suggest a more practical empirical method. This can be done by injecting a transient current at the load and using an RC network box to iterate toward the final compensation values, or by obtaining the optimum loop response using a network analyzer to find the actual loop poles and zeros.

Table 4. Suggested Compensation Network for 5V Input Application Using Multiple Paralleled 330µF AVX TPS Output Capacitors

L_O (µH)	C_O (µF)	R_C (kΩ)	C_C (pF)	C1 (pF)
1	990	3.6	10000	470
1	1980	6.8	4700	220
1	4950	22	2200	100
2.7	990	10	3300	150
2.7	1980	20	2200	68
2.7	4950	51	1000	47
5.6	990	20	2200	68
5.6	1980	39	1000	47
5.6	4950	100	470	33

Table 4 shows the suggested compensation components for 5V input applications based on the inductor and output capacitor values. The values were calculated using multiple paralleled 330µF AVX TPS series surface mount tantalum capacitors as the output capacitor. The optimum component values might deviate from the suggested values slightly because of board layout and operating condition differences.

An alternate output capacitor is the Sanyo MV-GX series. Using multiple parallel 1500µF Sanyo MV-GX capacitors for the output capacitor, Table 5 shows the suggested compensation component value for a 5V input application based on the inductor and output capacitor values.

Table 5. Suggested Compensation Network for 5V Input Application Using Multiple Paralleled 1500µF SANYO MV-GX Output Capacitors

L_O (µH)	C_O (µF)	R_C (kΩ)	C_C (pF)	C1 (pF)
1	4500	9.1	3300	150
1	6000	10	3300	100
1	9000	18	2200	68
2.7	4500	22	1500	47
2.7	6000	30	1000	47
2.7	9000	47	680	33
5.6	4500	47	680	33
5.6	6000	62	470	33
5.6	9000	91	330	22

VID0 to VID4, PWRGD and $\overline{\text{FAULT}}$

The digital inputs (VID0 to VID4) program the internal DAC which in turn controls the output voltage. These digital input controls are intended to be static and are not designed for high speed switching. Forcing V_{OUT} to step from a high to a low voltage by changing the VID_n pins quickly can cause $\overline{\text{FAULT}}$ to trip.

Figure 9 shows the relationship between the V_{OUT} voltage, PWRGD and $\overline{FAULT}$. To prevent PWRGD from interrupting the CPU unnecessarily, the RC5053 has a built-in t_{PWRBAD} delay to prevent noise at the SENSE pin from toggling PWRGD. The internal time delay is designed to take about 500µs for PWRGD to go low and 1ms for it to recover. Once PWRGD goes low, the internal circuitry watches for the output voltage to exceed 115% of the rated voltage. If this happens, $\overline{FAULT}$ will be triggered. Once $\overline{FAULT}$ is triggered, G1 and G2 will be forced low immediately and the RC5053 will remain in this state until V_{CC} power supply is recycled or OUTEN is toggled.

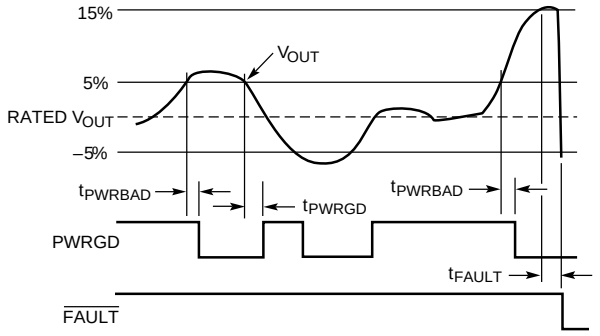


Figure 9. PWRGD and $\overline{FAULT}$

Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the RC5053. These items are also illustrated graphically in the layout diagram of Figure 10. The thicker lines show the high current paths. Note that at 10A current levels or above, current density in the PC board itself is a serious concern. Traces carrying high current should be as wide as possible. For example, a PCB fabricated with 2oz copper requires a minimum trace width of 0.15" to carry 10A.

1. In general, layout should begin with the location of the power devices. Be sure to orient the power circuitry so that a clean power flow path is achieved. Conductor widths should be maximized and lengths minimized. After you are satisfied with the power path, the control circuitry should be laid out. It is much easier to find routes for the relatively small traces in the control circuits than it is to find circuitous routes for high current paths.

2. The GND and SGND pins should be shorted right at the RC5053. This helps to minimize internal ground disturbances in the RC5053 and prevents differences in ground potential from disrupting internal circuit operation. This connection should then tie into the ground plane at a single point, preferably at a fairly quiet point

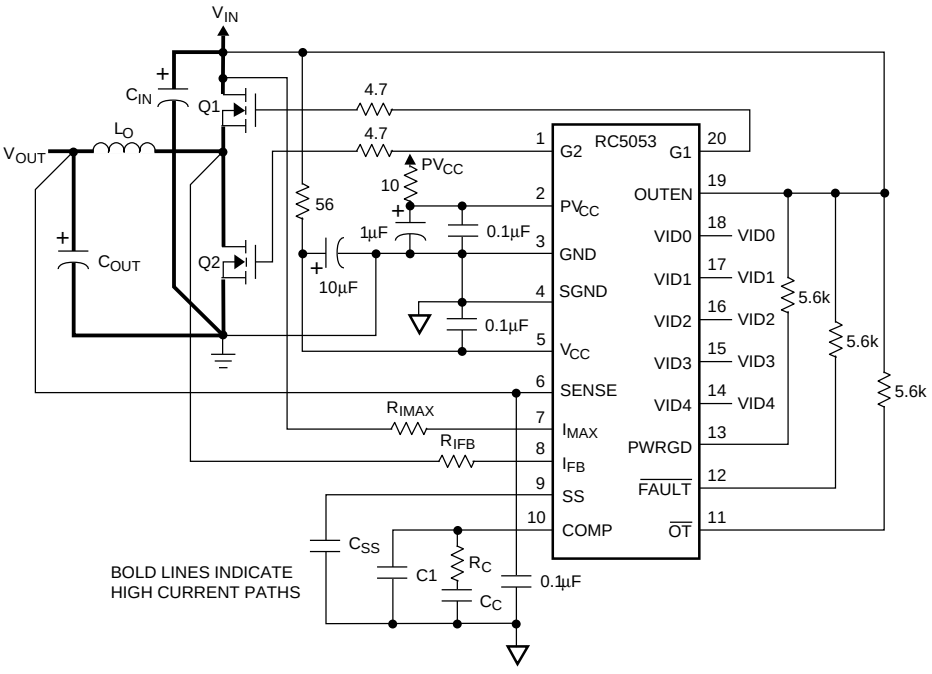


Figure 10. RC5053 Layout Diagram

in the circuit such as close to the output capacitors. This is not always practical, however, due to physical constraints. Another reasonably good point to make this connection is between the output capacitors and the source connection of the lowside FET Q2. Do not tie this single point ground in the trace run between the low side FET source and the input capacitor ground, as this area of the ground plane will be very noisy.

3. The small signal resistors and capacitors for frequency compensation and soft start should be located very close to their respective pins and the ground ends connected to the signal ground pin through a separate trace. Do not connect these parts to the ground plane!

4. The V_{CC} and PV_{CC} decoupling capacitors should be as close to the RC5053 as possible. The 10µF bypass capacitors for V_{CC} and a 1µF bypass capacitor for PV_{CC} will help provide optimum regulation performance.

5. The (+) plate of C_{IN} should be connected as close as possible to the drain of the upper MOSFET. An additional 1µF ceramic capacitor between V_{IN} and power ground is recommended.

6. The SENSE pin is very sensitive to pickup from the switching node. Care should be taken to isolate SENSE from possible capacitive coupling to the inductor switching signal. A 0.1µF is required between the SENSE pin and the SGND pin next to the RC5053.

7. OUTEN is a high impedance input and should be externally pulled up to a logic HIGH for normal operation.

8. Kelvin sense I_{MAX} and I_{FB} at Q1 drain and source pins.

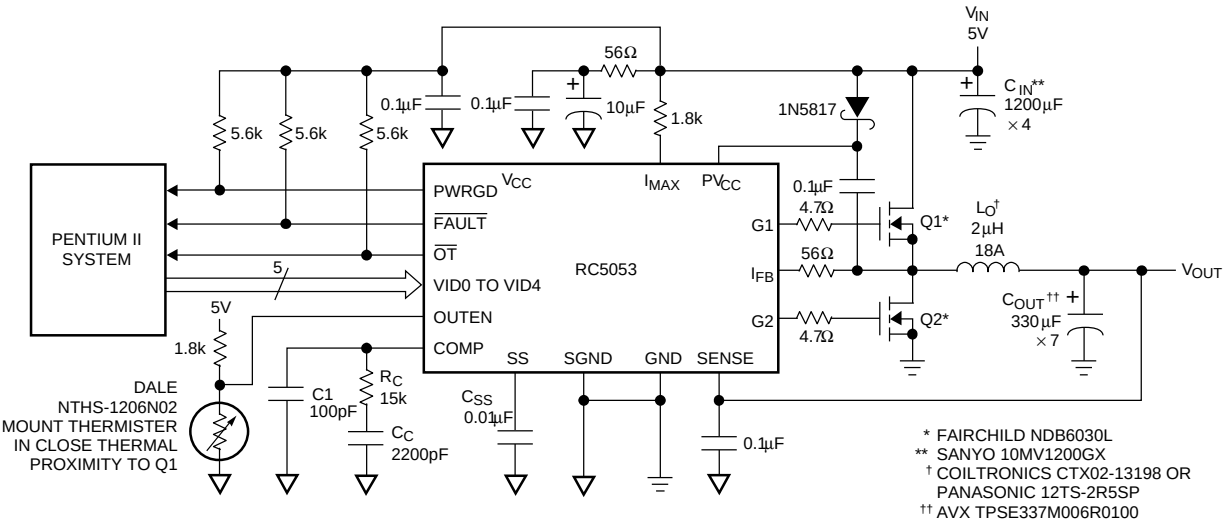


Figure 11. Single Supply RC5053 5V to 1.8V-3.5V Application with Thermal Monitor

Notes:

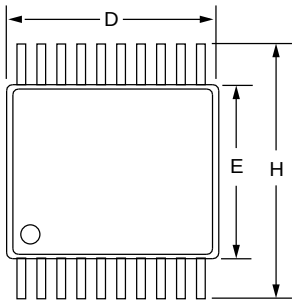
Notes:

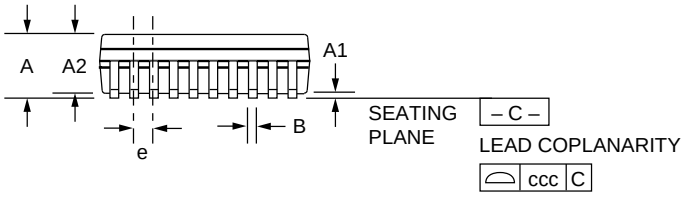
Mechanical Dimensions (20 Lead SSOP)

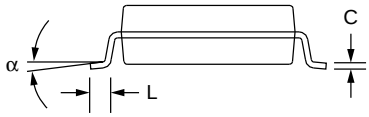
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.079	—	2.00	
A1	.002	—	0.05	—	
A2	.065	.073	1.65	1.85	
b	.009	.015	0.22	0.38	5
c	.004	.010	0.09	0.25	5
D	.272	.295	6.90	7.50	2, 4
E	.291	.323	7.40	8.20	
E1	.197	.220	5.00	5.60	2
e	.026 BSC		0.65 BSC		
L	.022	.037	0.55	0.95	3
N	20		20		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "b" and "c" dimensions include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.





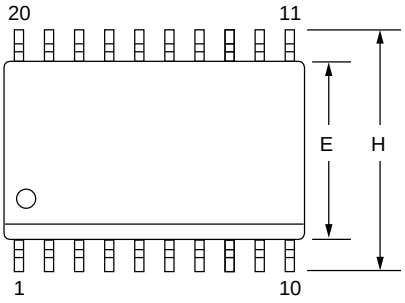


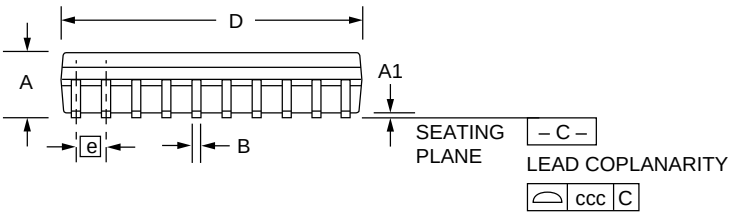
Mechanical Dimensions (20 Lead SOIC)

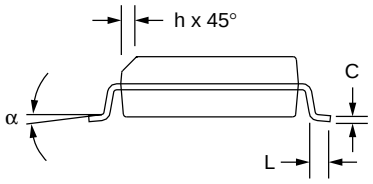
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.496	.512	12.60	13.00	2
E	.291	.299	7.40	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.029	0.25	0.75	
L	.016	.050	0.40	1.27	3
N	20		20		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Ordering Information

Product Number	Package
RC5053M	SOIC
RC5053G	SSOP

RC5054A

Programmable Synchronous DC-DC Converter Controller for Low Voltage Microprocessors

Features

- Drives Two N-Channel MOSFETs
- Operates from +5V or +12V V_{CC} Bias
- Operates from +5V Power Input
- Simple Single-Loop Control Design
  - Voltage-Mode PWM Control
- Fast Transient Response
  - High-Bandwidth Error Amplifier
  - Full 0% to 100% Duty Ratio
- Excellent Output Voltage Regulation
  - ±1% Over Line Voltage and Temperature
- TTL Compatible 5 Bit Digital-to-Analog Output Voltage Selection
  - Wide Range - 1.3V_{DC} to 3.5V_{DC}
  - 0.1V Binary Steps from 2.1V_{DC} to 3.5V_{DC}
  - 0.05V Binary Steps from 1.3V_{DC} to 2.1V_{DC}
- Power-Good Output Voltage Monitor
- Over-Voltage and Over-Current Fault Monitors
  - Does Not Require Extra Current Sensing Element,
  - Uses MOSFET's $R_{DS(ON)}$
- Small Converter Size
  - Constant Frequency Operation
  - 200kHz Free-Running Oscillator Programmable from 50kHz to 1MHz

Applications

- Power Supply for Pentium®, Pentium Pro, PowerPC™ and Alpha™ Microprocessors
- High-Power 5V to 3.xV DC-DC Regulators
- Low-Voltage Distributed Power Supplies

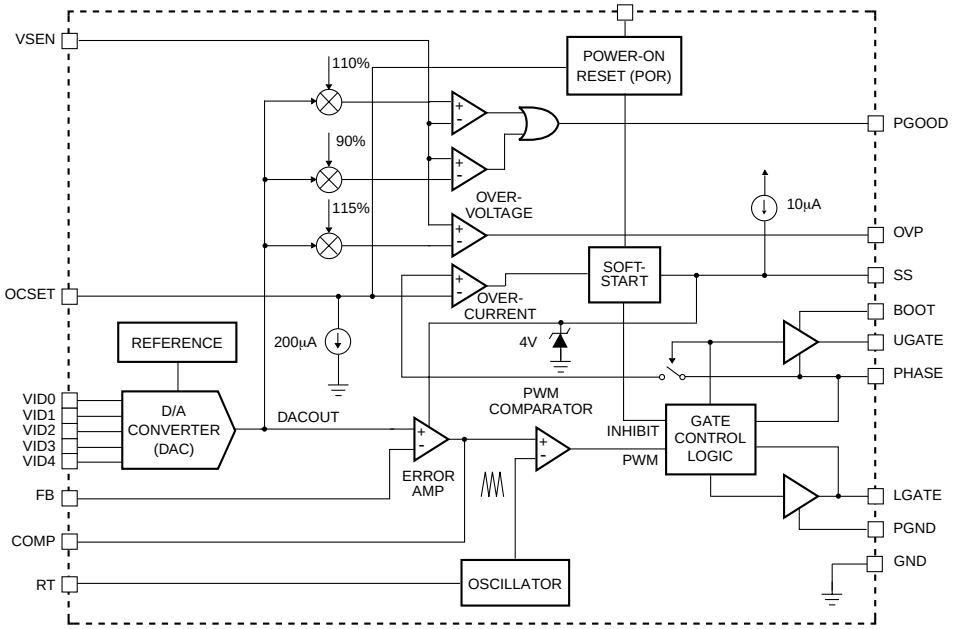
Description

The RC5054A provides complete control and protection for a DC-DC converter optimized for high-performance microprocessor applications. It is designed to drive two N-Channel MOSFETs in a synchronous-rectified buck topology. The RC5054A integrates all of the control, output adjustment, monitoring and protection functions into a single package.

The output voltage of the converter is easily adjusted and precisely regulated. The RC5054A includes a 5-input digital-to-analog converter (DAC) that adjusts the output voltage from 2.1V_{DC} to 3.5V_{DC} in 0.1V increments and from 1.3V_{DC} to 2.1V_{DC} in 0.05V steps. The precision reference and voltage-mode regulator hold the selected output voltage to within ±1% over temperature and line voltage variations.

Preliminary Information

Block Diagram



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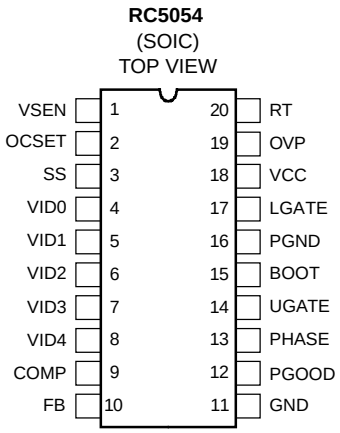
Pentium is a registered trademark of Intel Corporation.
PowerPC™ is a trademark of IBM Corporation.

Rev. 0.9.3

The RC5054A provides simple, single feedback loop, voltage-mode control with fast transient response. It includes a 200KHz free-running triangle-wave oscillator that is adjustable from 50KHz to 1MHz. The error amplifier features a 15MHz gain-bandwidth product and 6V/μs slew rate which enables high converter bandwidth for fast transient performance. The resulting PWM duty ratio ranges from 0% to 100%.

The RC5054A monitors the output voltage with a window comparator that tracks the DAC output and issues a Power Good signal when the output is within ±10%. The RC5054A protects against over-current conditions by inhibiting PWM operation. Built-in over-voltage protection triggers an external SCR to crowbar the input supply. The RC5054A monitors the current by using the $R_{DS(ON)}$ of the upper MOSFET which eliminates the need for a current sensing resistor.

Pin Assignments



Pin Definitions

Pin Number	Pin Names	Pin Function Description
1	VSEN	This pin is connected to the converters output voltage. The PGOOD and OVP comparator circuits use this signal to report output voltage status and for overvoltage protection.
2	OCSET	Connect a resistor (R_{OCSET}) from this pin to the drain of the upper MOSFET. R_{OCSET}, an internal 200μA current source (I_{OCS}), and the upper MOSFET on-resistance ($R_{DS(ON)}$) set the converter over-current (OC) trip point according to the following equation: $I_{PEAK} = \frac{I_{OCS} \bullet R_{OCSET}}{R_{DS(ON)}}$ An over-current trip cycles the soft-start function.
3	SS	Connect a capacitor from this pin to ground. This capacitor, along with an internal 10μA current source, sets the soft-start interval of the converter.
4-8	VID0-VID4	VID0-4 are the input pins to the 5-bit DAC. The states of these five pins program the internal voltage reference (DACOUT). The level of DACOUT sets the converter output voltage. It also sets the PGOOD and OVP thresholds. Table 1 specifies DACOUT for the 32 combinations of DAC inputs.
9	COMP	COMP and FB are the available external pins of the error amplifier. The FB pin is the inverting input of the error amplifier and the COMP pin is the error amplifier output. These pins are used to compensate the voltage-control feedback loop of the converter.
10	FB	
11	GND	Signal ground for the IC. All voltage levels are measured with respect to this pin.
12	PGOOD	PGOOD is an open collector output used to indicate the status of the converter output voltage. This pin is pulled low when the converter output is not within ±10% of the DACOUT reference voltage.
13	PHASE	Connect the PHASE pin to the upper MOSFET source. This pin is used to monitor the voltage drop across the MOSFET for over-current protection. This pin also provides the return path for the upper gate drive.
14	UGATE	Connect UGATE to the upper MOSFET gate. This pin provides the gate drive for the upper MOSFET.
15	BOOT	This pin provides bias voltage to the upper MOSFET driver. A bootstrap circuit may be used to create a BOOT voltage suitable to drive a standard N-Channel MOSFET.
16	PGND	This is the power ground connection. Tie the lower MOSFET source to this pin.

Preliminary Information

Pin Definitions (continued)

Pin Number	Pin Names	Pin Function Description
17	LGATE	Connect LGATE to the lower MOSFET gate. This pin provides the gate drive for the lower MOSFET.
18	VCC	Provide a 12V bias supply for the chip to this pin.
19	OVP	The OVP pin can be used to drive an external SCR in the event of an overvoltage condition.
20	RT	This pin provides oscillator switching frequency adjustment. By placing a resistor (R_T) from this pin to GND, the nominal 200KHz switching frequency is increased according to the following equation: $F_S = 200kHz + \frac{5.6E3[KHz \times Kohm]}{R_T[Kohm]}$ (R_T to GND) Conversely, connecting a pull-up resistor (RT) from this pin to VCC reduces the switching frequency according to the following equation: $F_S = 200kHz - \frac{30.0E3[KHz \times Kohm]}{R_T[Kohm]}$ (R_T to 12V)

Absolute Maximum Ratings

	Min.	Max.
Power Input Voltage, V_{IN}		6V
Supply Voltage, V_{CC}		+13.5V
Boot Voltage, V_{BOOT} - V_{PHASE}		+13.5V
V_{CC} or I/O Voltage	GND -0.3V	V_{CC} + 0.3V
ESD Classification		Class 2

Operating Conditions

	Min.	Max.
Supply Voltage, V_{CC}	+12V -10%	+12V +10%
Ambient Temperature Range	0°C	70°C
Junction Temperature Range	0°C	125°C

Thermal Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance[1] θJA SOIC Package SOIC Package	 With 3in^2 of Copper		 110 86		 °C/W °C/W
Maximum Junction Temperature	Plastic Package			150	°C
Maximum Storage Temperature Range		-65		150	°C
Maximum Lead Temperature	Soldering 10s			300	°C

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Preliminary Information

Electrical Specifications

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
VCC Supply Current						
I_{CC}	Nominal Supply	UGATE and LGATE Open	–	22	–	mA
	Power-On Reset					
	Rising VCC Threshold	V_{OCSET} = 4.5V	–	–	10.4	V
	Falling VCC Threshold	V_{OCSET} = 4.5V	8.8	–	–	V
	Rising V_{OCSET} Threshold		–	1.26	–	V
Oscillator						
	Free Running Frequency	RT = OPEN	185	200	215	KHz
	Total Variation	6KΩ < RT to GND < 200KΩ	-15	–	+15	%
ΔV_{OSC}	Ramp Amplitude	RT = Open	–	1.9	–	V_{P-P}
Reference and DAC						
	DACOUT Voltage Accuracy		-1.0	–	+1.0	%
Error Amplifier						
	DC Gain		–	88	–	dB
GBW	Gain-Bandwidth Product		–	15	–	MHz
SR	Slew Rate	COMP = 10pF	–	6	–	V/μs
Gate Drivers						
I_{UGATE}	Upper Gate Source	V_{BOOT} - V_{PHASE} = 12V	350	500	–	mA
I_{UGATE}	Upper Gate Sink	V_{UGATE} - V_{PHASE} = 1V	–	100	–	mA
I_{LGATE}	Lower Gate Source	V_{CC} = 12V, V_{LGATE} = 6V	300	450	–	mA
I_{LGATE}	Lower Gate Sink	V_{UGATE} - V_{PHASE} = 1V	–	100	–	mA
Protection						
	Over-Voltage Trip (V_{SEN}/DACOUT)		–	115	120	%
I_{OCSET}	OCSET Current Source	V_{OCSET} = 4.5V_{DC}	170	200	230	μA
I_{OVP}	OVP Sourcing Current	V_{SEN} = 5.5V, V_{OVP} = 0V	60	–	–	mA
I_{SS}	Soft Start Current		–	10	–	μA
Power Good						
	Upper Threshold (V_{SEN}/DACOUT)	VSEN Rising	106	–	111	%
	Lower Threshold (V_{SEN}/DACOUT)	VSEN Falling	89	–	94	%
	Hysteresis (V_{SEN}/DACOUT)	Upper and Lower Threshold	–	2	–	%
V_{PGOOD}	PGOOD Voltage Low	I_{PGOOD} = -5mA	–	0.5	–	V

Functional Description

Initialization

The RC5054A automatically initializes upon receipt of power. Special sequencing of the input supplies is not necessary. The Power-On Reset (POR) function continually monitors the input supply voltages. The POR monitors the bias volt-age at the V_{CC} pin and the input voltage (V_{IN}) on the OCSET pin. The level on OCSET is equal to V_{IN} less a fixed voltage drop (see over-current protection). The POR function initiates soft start operation after both input supply voltages exceed their POR thresholds. For operation with a single +12V power source, V_{IN} and V_{CC} are equivalent and the +12V power source must exceed the rising V_{CC} threshold before POR initiates operation.

Soft Start

The POR function initiates the soft start sequence. An internal 10μA current source charges an external capacitor (C_{SS}) on the SS pin to 4V. Soft start clamps the error amplifier output (COMP pin) and reference input (+ terminal of error amp) to the SS pin voltage. Figure 1 shows the soft start interval with C_{SS} = 0.1μF. Initially the clamp on the error amplifier (COMP pin) controls the converter's output voltage. At t_1 in Figure 1, the SS voltage reaches the valley of the oscillator's triangle wave. The oscillator's triangular

waveform is compared to the ramping error amplifier voltage. This generates PHASE pulses of increasing width that charge the output capacitor(s). This interval of increasing pulse width continues to t_2. With sufficient output voltage, the clamp on the reference input controls the output voltage. This is the interval between t_2 and t_3 in Figure 1. At t_3 the SS voltage exceeds the DACOUT voltage and the output voltage is in regulation. This method provides a rapid and controlled output voltage rise. The PGOOD signal toggles 'high' when the output voltage (VSEN pin) is within ±5% of DACOUT. The 2% hysteresis built into the power good comparators prevents PGOOD oscillation due to nominal output voltage ripple.

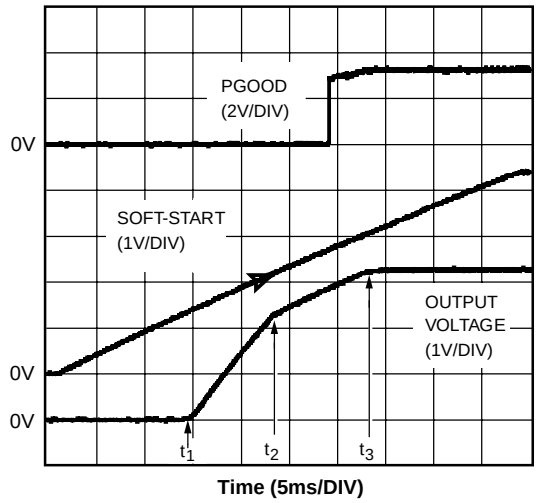


Figure 1. Soft Start Interval

Over-Current Protection

The over-current function protects the converter from a shorted output by using the upper MOSFET's on-resistance, $R_{DS(ON)}$ to monitor the current. This method enhances the converter's efficiency and reduces cost by eliminating a current sensing resistor. The over-current function cycles the soft-start function in a hiccup mode to provide fault protection. A resistor (R_{OCSET}) programs the over-current trip level. An internal 200µA current sink develops a voltage across R_{OCSET} that is referenced to V_{IN}. When the voltage across the upper MOSFET (also referenced to V_{IN}) exceeds the voltage across R_{OCSET} , the over-current function initiates a soft-start sequence. The soft-start function discharges C_{SS} with a 10µA current sink and inhibits PWM operation. The soft-start function recharges C_{SS}, and PWM operation resumes with the error amplifier clamped to the SS voltage. Should an overload occur while recharging C_{SS}, the soft start function inhibits PWM operation while fully charging C_{SS} to 4V to complete its cycle. Figure 2 shows this operation with an overload condition. Note that the inductor current increases to over 15A during the CSS charging interval and causes an over-current trip. The converter dissipates very little power with this method. The measured input power for the conditions of Figure 2 is 2.5W.

The over-current function will trip at a peak inductor current (I_{PEAK}) determined by:

$$I_{PEAK} = \frac{I_{OCSET} \bullet R_{OCSET}}{R_{DS(ON)}}$$

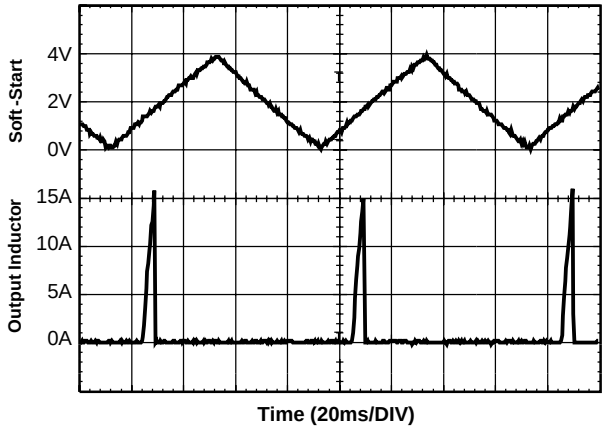


Figure 2. Over-Current Operation

where I_{OCSET} is the internal OCSET current source (200µA typical). The OC trip point varies mainly due to the MOSFET's $R_{DS(ON)}$ variations. To avoid over-current tripping in the normal operating load range, find the R_{OCSET} resistor from the equation above with:

- The maximum $R_{DS(ON)}$ at the highest junction temperature.
- The minimum I_{OCSET} from the specification table.
- Determine I_{PEAK} for $I_{PEAK} > I_{OUT(MAX)} + (\Delta I)/2$, where ΔI is the output inductor ripple current.

For an equation for the ripple current see the section under component guidelines titled 'Output Inductor Selection.'

A small ceramic capacitor should be placed in parallel with R_{OCSET} to smooth the voltage across R_{OCSET} in the presence of switching noise on the input voltage.

Output Voltage Program

The output voltage of a RC5054A converter is programmed to discrete levels between 1.3V_{DC} and 3.5V_{DC} . The voltage identification (VID) pins program an internal voltage reference (DACOUT) with a 5-bit digital-to-analog converter (DAC). The level of DACOUT also sets the PGOOD and OVP thresholds. Table 1 specifies the DACOUT voltage for the 32 combinations of open or short connections on the VID pins. The output voltage should not be adjusted while the converter is delivering power. Remove input power before changing the output voltage. Adjusting the output voltage during operation could toggle the PGOOD signal and exercise the overvoltage protection.

Grounding any combination of the VID pins increases the DACOUT voltage.

Preliminary Information

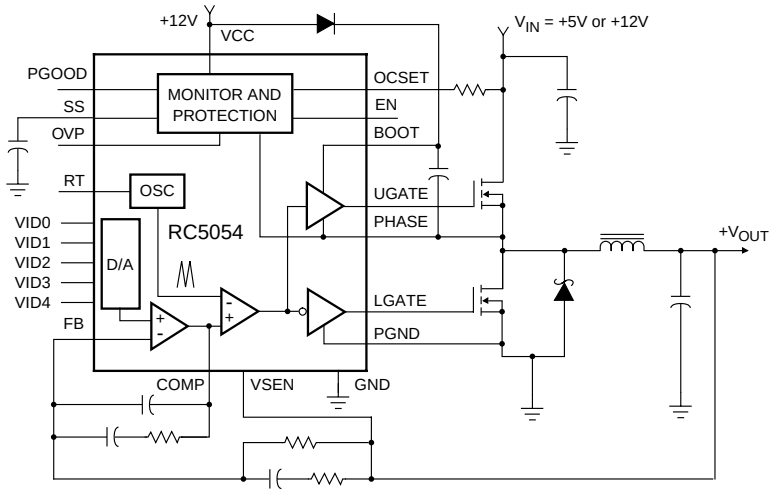
Table 1. Output Voltage Table

PIN NAME					NOMINAL OUTPUT VOLTAGE	PIN NAME					NOMINAL OUTPUT VOLTAGE
VID4	VID3	VID2	VID1	VID0		VID4	VID3	VID2	VID1	VID0	
0	1	1	1	1	1.30	1	1	1	1	1	SHDN
0	1	1	1	0	1.35	1	1	1	1	0	2.1
0	1	1	0	1	1.40	1	1	1	0	1	2.2
0	1	1	0	0	1.45	1	1	1	0	0	2.3
0	1	0	1	1	1.50	1	1	0	1	1	2.4
0	1	0	1	0	1.55	1	1	0	1	0	2.5
0	1	0	0	1	1.60	1	1	0	0	1	2.6
0	1	0	0	0	1.65	1	1	0	0	0	2.7
0	0	1	1	1	1.70	1	0	1	1	1	2.8
0	0	1	1	0	1.75	1	0	1	1	0	2.9
0	0	1	0	1	1.80	1	0	1	0	1	3.0
0	0	1	0	0	1.85	1	0	1	0	0	3.1
0	0	0	1	1	1.90	1	0	0	1	1	3.2
0	0	0	1	0	1.95	1	0	0	1	0	3.3
0	0	0	0	1	2.00	1	0	0	0	1	3.4
0	0	0	0	0	2.05	1	0	0	0	0	3.5

Note:

1. 0 = connected to GND or V_{SS}, 1 = OPEN

Typical Application



Applications Discussion

Layout Considerations

As in any high frequency switching converter, layout is very important. Switching current from one power device to another can generate voltage transients across the impedances of the interconnecting bond wires and circuit traces. These interconnecting impedances should be minimized by using wide, short printed circuit traces. The critical components should be located as close together as possible, using ground plane construction or single point grounding.

Figure 3 shows the critical power components of the converter. To minimize the voltage overshoot the interconnecting wires indicated by heavy lines should be part of ground or power plane in a printed circuit board. The components

shown in Figure 3 should be located as close together as possible. Please note that the capacitors C_{IN} and C_O each represent numerous physical capacitors. Locate the RC5054A within 3 inches of the MOSFETs, Q1 and Q2. The circuit traces for the MOSFETs' gate and source connections from the RC5054A must be sized to handle up to 1A peak current.

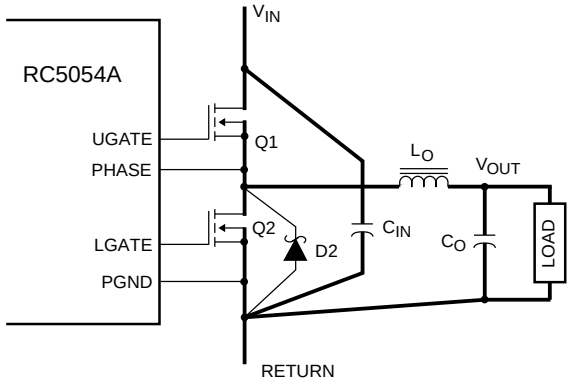


Figure 3. Printed Circuit Board Power and Ground Planes or Islands

Figure 4 shows the circuit traces that require additional layout consideration. Use single point and ground plane construction for the circuits shown. Minimize any leakage current paths on the SS PIN and locate the capacitor, C_{SS} close to the SS pin because the internal current source is only 10µA. Provide local V_{CC} decoupling between V_{CC} and GND pins. Locate the capacitor, C_{BOOT} as close as practical to the BOOT and PHASE pins.

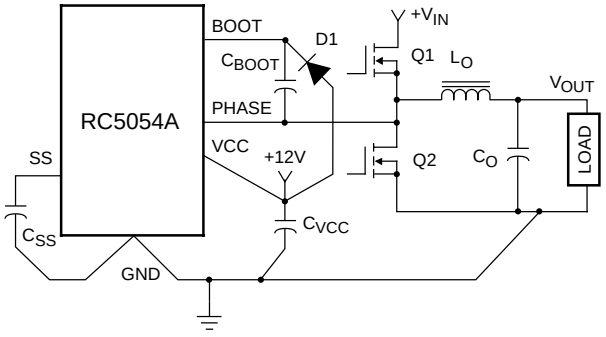


Figure 4. Printed Circuit Board Small Signal Layout Guidelines

Feedback Compensation

Figure 5 highlights the voltage-mode control loop for a synchronous-rectified buck converter. The output voltage (V_{OUT}) is regulated to the Reference voltage level. The error amplifier (Error Amp) output ($V_{E/A}$) is compared with the oscillator (OSC) triangular wave to provide a pulse-width modulated (PWM) wave with an amplitude of V_{IN} at the PHASE node. The PWM wave is smoothed by the output filter (L_O and C_O).

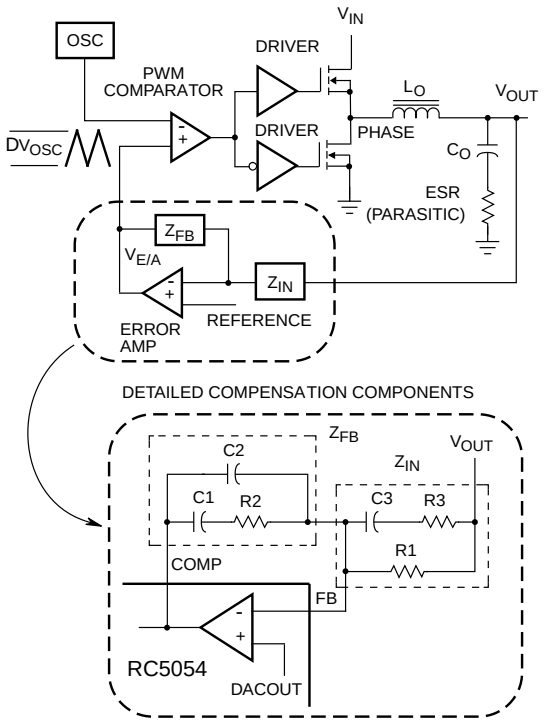


Figure 5. Voltage-Mode Buck Converter Compensation Design

The modulator transfer function is the small-signal transfer function of $V_{OUT}/V_{E/A}$. This function is dominated by a DC Gain and the output filter (L_O and C_O), with a double pole break freaquency at F_{LC} and a zero at F_{ESR}. The DC Gain of the modulator is simply the input voltage (V_{IN}) divided by the peak-to-peak oscillator voltage ΔV_{OSC}.

Modulator Break Frequency Equations

$$F_{LC} = \frac{1}{2\pi \bullet \sqrt{L_O \bullet C_O}} \qquad F_{ESR} = \frac{1}{2\pi \bullet ESR \bullet C_O}$$

The compensation network consists of the error amplifier (internal to the RC5054A) and the impedance networks Z_{IN} and Z_{FB}. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency (f_{0dB}) and adequate phase margin. Phase margin is the difference between the closed loop phase at f_{0dB} and 180 degrees. The equations below relate the compensation network's poles, zeros and gain to the components (R1, R2, R3, C1, C2, and C3) in Figure 5. Use these guidelines for locating the poles and zeros of the compensation network:

1. Pick Gain (R2/R1) for desired converter bandwidth
2. Place 1^{ST} Zero Below Filter's Double Pole (~75% F_{LC})
3. Place 2^{ND} Zero at Filter's Double Pole

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4. Place 1ST Pole at the ESR Zero
5. Place 2ND Pole at Half the Switching Frequency
6. Check Gain against Error Amplifier's Open-Loop Gain
7. Estimate Phase Margin - Repeat if Necessary

Compensation Break Frequency Equations

$$F_{Z1} = \frac{1}{2\pi \bullet R2 \bullet C1} \qquad F_{P1} = \frac{1}{2\pi \bullet R2 \bullet \left(\frac{C1 \bullet C2}{C1 + C2}\right)}$$

$$F_{Z2} = \frac{1}{2\pi \bullet (R1 + R3) \bullet C3} \qquad F_{P2} = \frac{1}{2\pi \bullet R3 \bullet C3}$$

Figure 6 shows an asymptotic plot of the DC-DC converter's gain vs. frequency. The actual Modulator Gain has a high gain peak due to the high Q factor of the output filter and is not shown in Figure 6. Using the above guidelines should give a Compensation Gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at F_{P2} with the capabilities of the error amplifier. The Closed Loop Gain is constructed on the log-log graph of Figure 6 by adding the Modulator Gain (in dB) to the Compensation Gain (in dB). This is equivalent to multiplying the modulator transfer function to the compensation transfer function and plotting the gain.

The compensation gain uses external impedance networks Z_{FB} and Z_{IN} to provide a stable, high bandwidth (BW) overall loop. A stable control loop has a gain crossing with -20dB/decade slope and a phase margin greater than 45 degrees. Include worst case component variations when determining phase margin.

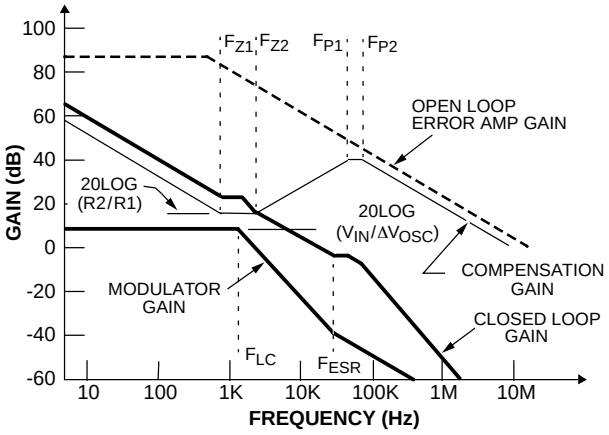


Figure 6. Asymptotic Bode Plot of Converter Gain

Component Selection Guidelines

Output Capacitor Selection

An output capacitor is required to filter the output and supply the load transient current. The filtering requirements are a function of the switching frequency and the ripple current. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout.

Modern microprocessors produce transient load rates above 1A/ns. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (effective series resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements. For example, Intel recommends that the high frequency decoupling for the Pentium Pro be composed of at least forty (40) 1µF ceramic capacitors in the 1206 surface-mount package.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the equivalent series inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

Output Inductor Selection

The output inductor is selected to meet the output voltage ripple requirements and minimize the converter's response time to the load transient. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current. The ripple voltage and current are approximated by the following equations:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{FS \times L} \bullet \frac{V_{OUT}}{V_{IN}} \qquad \Delta V_{OUT} = \Delta I \times ESR$$

Increasing the value of inductance reduces the ripple current and voltage. However, the large inductance values reduce the converter's response time to a load transient.

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the RC5054A will provide either 0% or 100% duty cycle in response to a load transient. The response time is the time

required to slew the inductor current from an initial current value to the transient current level. During this interval the difference between the inductor current and the transient current level must be supplied by the output capacitor. Minimizing the response time can minimize the output capacitance required.

The response time to a transient is different for the application of load and the removal of load. The following equations give the approximate response time interval for application and removal of a transient load:

$$t_{RISE} = \frac{L \times I_{TRAN}}{V_{IN} - V_{OUT}} \qquad t_{FALL} = \frac{L \times I_{TRAN}}{V_{OUT}}$$

where: I_{TRAN} is the transient load current step, t_{RISE} is the response time to the application of load, and t_{FALL} is the response time to the removal of load. With a +5V input source, the worst case response time can be either at the application or removal of load and dependent upon the DACOUT setting. Be sure to check both of these equations at the minimum and maximum output levels for the worst case response time.

Input Capacitor Selection

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time Q1 turns on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of Q1 and the source of Q2.

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current rating requirement for the input capacitor of a buck regulator is approximately 1/2 the DC load current.

For a through hole design, several electrolytic capacitors (Panasonic HFQ series or Nichicon PL series or Sanyo MVGX or equivalent) may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up. The TPS series available from AVX, and the 593D series from Sprague are both surge current tested.

MOSFET Selection/Considerations

The RC5054A requires 2 N-Channel power MOSFETs. These should be selected based upon $R_{DS(ON)}$, gate supply requirements, and thermal management requirements.

In high-current applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components; conduction loss and switching loss. The conduction losses are the largest component of power dissipation for both the upper and the lower MOSFETs. These losses are distributed between the two MOSFETs according to duty factor (see the equations below). Only the upper MOSFET has switching losses, since the Schottky rectifier clamps the switching node before the synchronous rectifier turns on. These equations assume linear voltage-current transitions and do not adequately model power loss due the reverse-recovery of the lower MOSFET's body diode. The gate-charge losses are dissipated by the RC5054A and don't heat the MOSFETs. However, large gate-charge increases the switching interval,
t_{SW} which increases the upper MOSFET switching losses. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

$$P_{LOWER} = I_O^2 \times R_{DS(ON)} \times (1 - D)$$

$$P_{UPPER} = I_O^2 \times R_{DS(ON)} \times D + \frac{1}{2} Io \times V_{IN} \times t_{SW} \times F_S$$

Where: D is the duty cycle = V_{OUT}/V_{IN},
t_{SW} is the switching interval, and
F_S is the switching frequency

Standard-gate MOSFETs are normally recommended for use with the RC5054A. However, logic-level gate MOSFETs can be used under special circumstances. The input voltage, upper gate drive level, and the MOSFET's absolute gate-to-source voltage rating determine whether logic-level MOSFETs are appropriate.

Figure 7 shows the upper gate drive (BOOT pin) supplied by a bootstrap circuit from V_{CC}. The boot capacitor, C_{BOOT} develops a floating supply voltage referenced to the PHASE pin. This supply is refreshed each cycle to a voltage of V_{CC} less the boot diode drop (V_D) when the lower MOSFET, Q2 turns on. Logic-level MOSFETs can only be used if the MOSFET's absolute gate-to-source voltage rating exceeds the maximum voltage applied to V_{CC}.

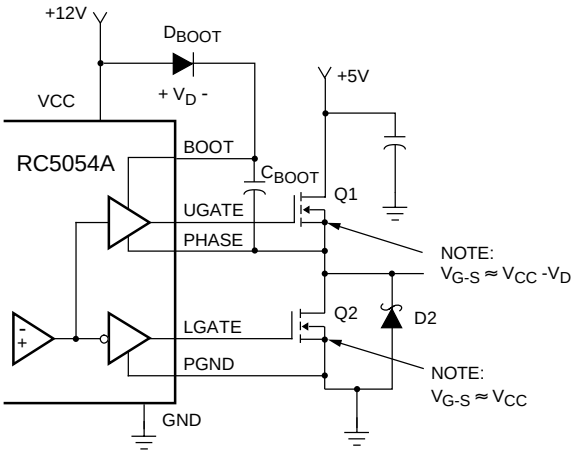


Figure 7. Upper Gate Drive - Bootstrap Option

Figure 8 shows a similar circuit for 12 Volt power input applications with two major differences. D_{Boot} has been replaced with a 5.1 Volt Zener diode and a small resistor (5Ω-10Ω) is inserted in series with C_{Boot}. This circuit will deliver the necessary drive voltage for Q1 while maintaining a safe operating voltage on pin 15 (Boot).

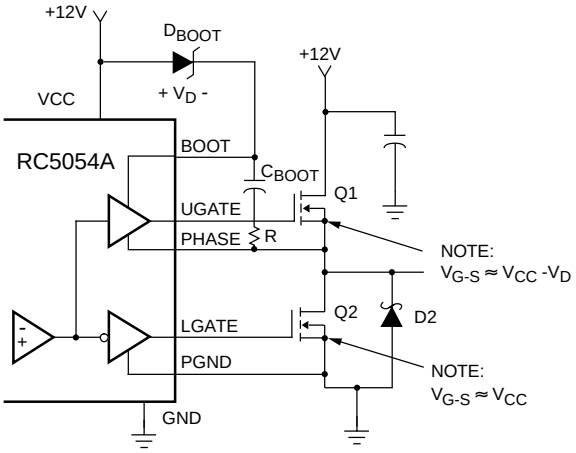


Figure 8. Upper Gate Drive - Bootstrap Option-Server Application

Figure 9 shows the upper gate drive supplied by a direct connection to V_{CC}. This option should only be used in converter systems where the main input voltage is $+5V_{DC}$ or less. The peak upper gate-to-source voltage is approximately V_{CC} less the input supply. For +5V main power and +12VDC for the bias, the gate-to-source voltage of Q1 is 7V. A logic-level MOSFET is a good choice for Q1 and a logic-level MOSFET can be used for Q2 if its absolute gate-to-source voltage rating exceeds the maximum voltage applied to V_{CC}.

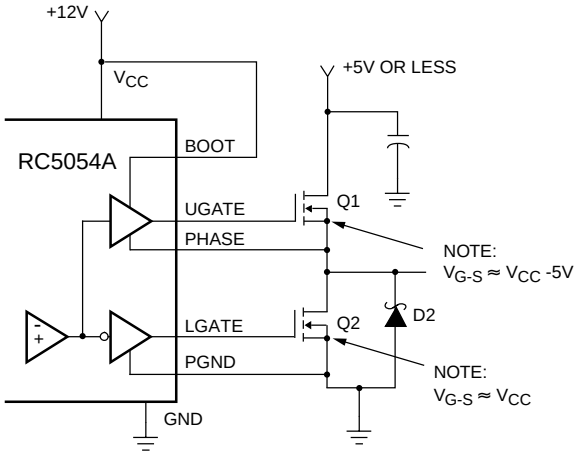


Figure 9. Upper Gate Drive - Direct V_{CC} Drive Option

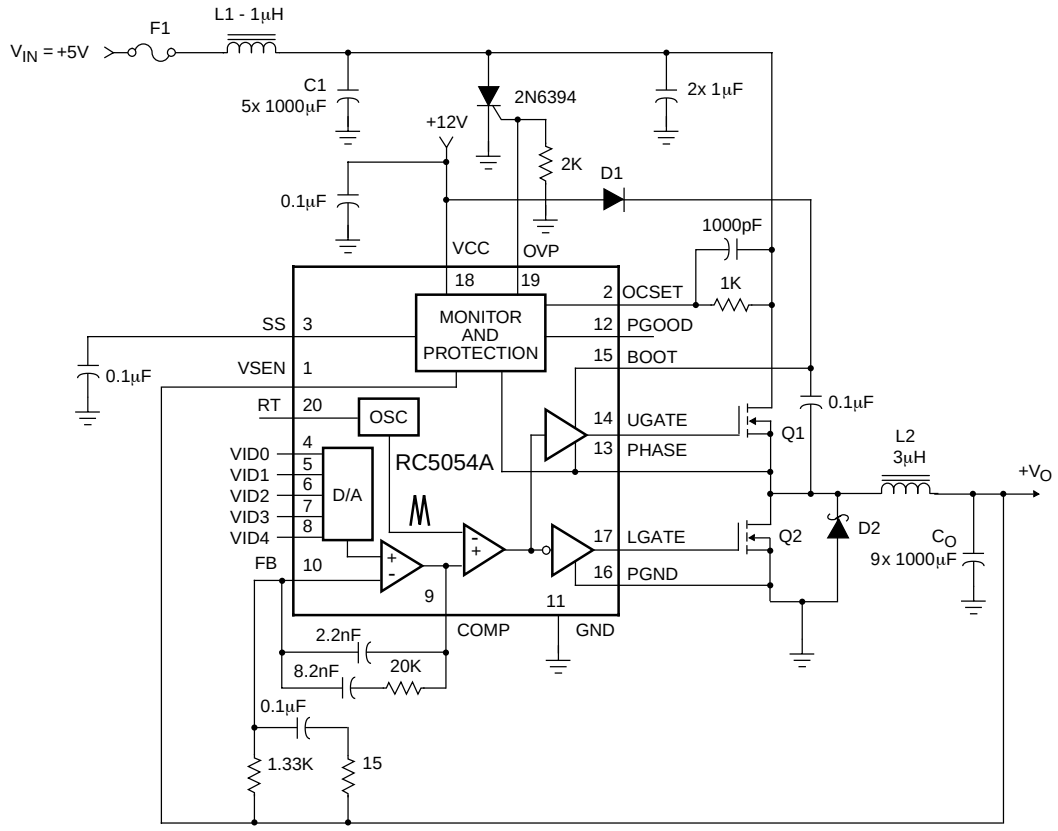
Schottky Selection

Rectifier D2 is a clamp that catches the negative inductor swing during the dead time between turning off the lower MOSFET and turning on the upper MOSFET. The diode must be a Schottky type to prevent the lossy parasitic MOSFET body diode from conducting. It is acceptable to omit the diode and let the body diode of the lower MOSFET clamp the negative inductor swing, but efficiency will drop one or two percent as a result. The diode's rated reverse breakdown voltage must be greater than the maximum input voltage.

Preliminary Information

RC5054A DC-DC Converter Application Circuit

Figure 10 shows an application circuit of a DC-DC Converter for an Intel Pentium Pro microprocessor.



Component Selection Notes;

C_0 - 9 Each 1000μF 6.3W VDC, Sanyo MV-GX or Equivalent
C1 - 5 Each 1000μF 25W VDC, Sanyo MV-GX or Equivalent
L2 - Core: Micrometals T50-52B; Each Winding: 10 Turns of 16AWG
L1 - Core: Micrometals T50-52; Winding: 5 Turns of 18AWG
D1 - 1N4148 or Equivalent
D2 - 3A, 40V Schottky, Motorola MBR340 or Equivalent
Q1, Q2 - Fairchild FDB6030L

Figure 10. Pentium Pro DC-DC Converter

Preliminary Information

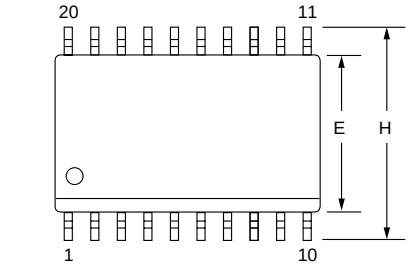
Notes:

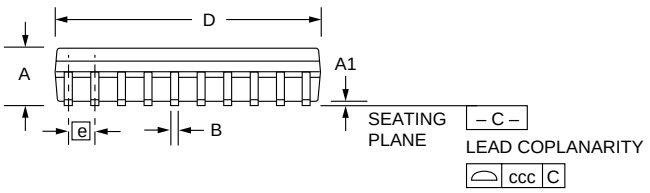
Mechanical Dimensions (20 Lead SOIC)

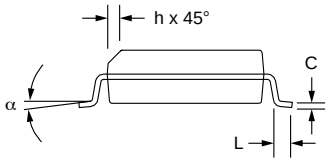
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.496	.512	12.60	13.00	2
E	.291	.299	7.40	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.029	0.25	0.75	
L	.016	.050	0.40	1.27	3
N	20		20		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Preliminary Information

Ordering Information

Part Number	Temperature Range (°C)	Package
RC5054ACB	0 to 70	20 Ld SOIC

Preliminary Information

RC5054A

Programmable Synchronous DC-DC Converter Controller for Low Voltage Microprocessors

Features

- Drives Two N-Channel MOSFETs
- Operates from +5V Power Input
- Simple Single-Loop Control Design
  - Voltage-Mode PWM Control
- Fast Transient Response
  - High-Bandwidth Error Amplifier
  - Full 0% to 100% Duty Ratio
- Excellent Output Voltage Regulation
- TTL Compatible 5 Bit Digital-to-Analog Output Voltage Selection
  - Wide Range - 1.3V_{DC} to 3.5V_{DC}
  - 0.1V Binary Steps from 2.1V_{DC} to 3.5V_{DC}
  - 0.05V Binary Steps from 1.3V_{DC} to 2.1V_{DC}
- Power-Good Output Voltage Monitor
- Over-Voltage and Over-Current Fault Monitors
  - Does Not Require Extra Current Sensing Element, Uses MOSFET's $R_{DS(ON)}$
- Small Converter Size
  - Constant Frequency Operation
  - 200kHz Free-Running Oscillator Programmable from 50kHz to 1MHz

Applications

- Power Supply for Pentium®, Pentium Pro, PowerPC™ and Alpha™ Microprocessors
- High-Power 5V to 3.xV DC-DC Regulators
- Low-Voltage Distributed Power Supplies

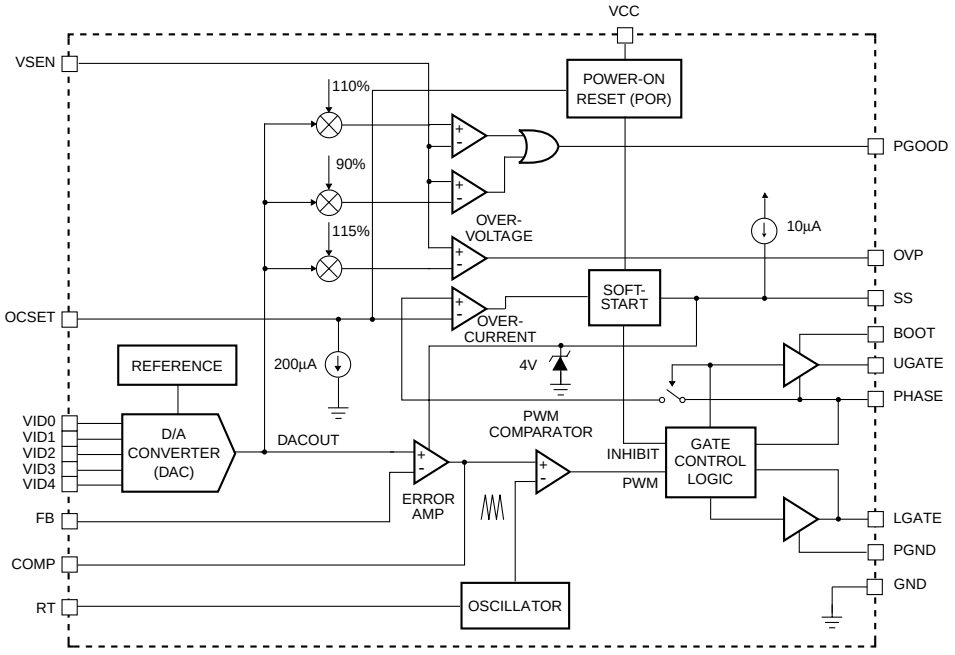
Description

The RC5054A provides complete control and protection for a DC-DC converter optimized for high-performance microprocessor applications. It is designed to drive two N-Channel MOSFETs in a synchronous-rectified buck topology. The RC5054A integrates all of the control, output adjustment, monitoring and protection functions into a single package.

The output voltage of the converter is easily adjusted and precisely regulated. The RC5054A includes a 5-input digital-to-analog converter (DAC) that adjusts the output voltage from 2.1V_{DC} to 3.5V_{DC} in 0.1V increments and from 1.3V_{DC} to 2.1V_{DC} in 0.05V steps.

The RC5054A provides simple, single feedback loop, volt-

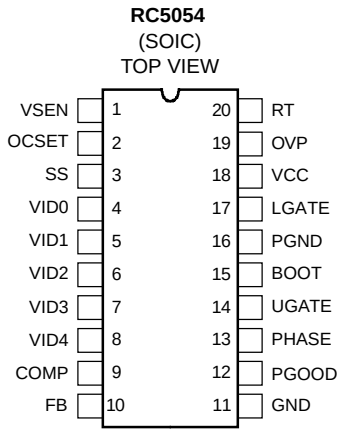
Block Diagram



age-mode control with fast transient response. It includes a 200KHz free-running triangle-wave oscillator that is adjustable from 50KHz to 1MHz. The error amplifier features a 15MHz gain-bandwidth product and 6V/µs slew rate which enables high converter bandwidth for fast transient performance. The resulting PWM duty ratio ranges from 0% to 100%.

The RC5054A monitors the output voltage with a window comparator that tracks the DAC output and issues a Power Good signal when the output is within ±10%. The RC5054A protects against over-current conditions by inhibiting PWM operation. Built-in over-voltage protection triggers an external SCR to crowbar the input supply. The RC5054A monitors the current by using the $R_{DS(ON)}$ of the upper MOSFET which eliminates the need for a current sensing resistor.

Pin Assignments



Pin Definitions

Pin Number	Pin Names	Pin Function Description
1	VSEN	This pin is connected to the converter's output voltage. The PGOOD and OVP comparator circuits use this signal to report output voltage status and for overvoltage protection.
2	OCSET	Connect a resistor (R_{OCSET}) from this pin to the drain of the upper MOSFET. R_{OCSET}, an internal 200µA current source (I_{OCS}), and the upper MOSFET on-resistance ($R_{DS(ON)}$) set the converter over-current (OC) trip point according to the following equation: $I_{PEAK} = \frac{I_{OCS} \bullet R_{OCSET}}{R_{DS(ON)}}$ An over-current trip cycles the soft-start function.
3	SS	Connect a capacitor from this pin to ground. This capacitor, along with an internal 10µA current source, sets the soft-start interval of the converter.
4-8	VID0-VID4	VID0-4 are the input pins to the 5-bit DAC. The states of these five pins program the internal voltage reference (DACOUT). The level of DACOUT sets the converter output voltage. It also sets the PGOOD and OVP thresholds. Table 1 specifies DACOUT for the 32 combinations of DAC inputs.
9	COMP	COMP and FB are the available external pins of the error amplifier. The FB pin is the inverting input of the error amplifier and the COMP pin is the error amplifier output. These pins are used to compensate the voltage-control feedback loop of the converter.
10	FB	
11	GND	Signal ground for the IC. All voltage levels are measured with respect to this pin.
12	PGOOD	PGOOD is an open collector output used to indicate the status of the converter output voltage. This pin is pulled low when the converter output is not within ±10% of the DACOUT reference voltage.
13	PHASE	Connect the PHASE pin to the upper MOSFET source. This pin is used to monitor the voltage drop across the MOSFET for over-current protection. This pin also provides the return path for the upper gate drive.
14	UGATE	Connect UGATE to the upper MOSFET gate. This pin provides the gate drive for the upper MOSFET.
15	BOOT	This pin provides bias voltage to the upper MOSFET driver. A bootstrap circuit may be used to create a BOOT voltage suitable to drive a standard N-Channel MOSFET.
16	PGND	This is the power ground connection. Tie the lower MOSFET source to this pin.

Pin Definitions (continued)

Pin Number	Pin Names	Pin Function Description
17	LGATE	Connect LGATE to the lower MOSFET gate. This pin provides the gate drive for the lower MOSFET.
18	VCC	Provide a 12V bias supply for the chip to this pin.
19	OVP	The OVP pin can be used to drive an external SCR in the event of an overvoltage condition.
20	RT	This pin provides oscillator switching frequency adjustment. By placing a resistor (R_T) from this pin to GND, the nominal 200KHz switching frequency is increased according to the following equation: $F_S = 200kHz + \frac{3.5 \times 10^6 [KHz \times Kohm]}{R_T[Kohm]}$ (R_T to GND) Conversely, connecting a pull-up resistor (RT) from this pin to VCC reduces the switching frequency according to the following equation: $F_S = 200kHz - \frac{3 \times 10^5 [KHz \times Kohm]}{R_T[Kohm]}$ (R_T to 12V)

Absolute Maximum Ratings

	Min.	Max.
Power Input Voltage, V_{IN}		6V
Supply Voltage, V_{CC}		+13.5V
Boot Voltage, V_{BOOT} - V_{PHASE}		+13.5V
V_{CC} or I/O Voltage	GND -0.3V	V_{CC} + 0.3V
ESD Classification		Class 2

Recommended Operating Conditions

	Min.	Max.
Supply Voltage, V_{CC}	+12V -10%	+12V +10%
Ambient Temperature Range	0°C	70°C
Junction Temperature Range	0°C	125°C

Thermal Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance[1] θ_{JA}					
SOIC Package			110		°C/W
SOIC Package	With 3in^2 of Copper		86		°C/W
Maximum Junction Temperature	Plastic Package			150	°C
Maximum Storage Temperature Range		-65		150	°C
Maximum Lead Temperature	Soldering 10s			300	°C

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications (Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
VCC Supply Current						
I_{CC}	Nominal Supply	UGATE and LGATE Open	–	22	–	mA
	Power-On Reset					
	Rising VCC Threshold	V_{OCSET} = 4.5V	–	–	10.4	V
	Falling VCC Threshold	V_{OCSET} = 4.5V	8.8	–	–	V
	Rising V_{OCSET} Threshold		–	1.26	–	V
Oscillator						
	Free Running Frequency	RT = OPEN	185	200	215	KHz
ΔV_{OSC}	Ramp Amplitude	RT = Open	–	1.9	–	V_{P-P}
Reference and DAC						
	Initial Voltage Setpoint	I_{LOAD} = 0.8A, V_{OUT} = 2.000V V_{OUT} = 1.550V	1.980 1.534	2.000 1.550	2.020 1.566	V V
Error Amplifier						
	DC Gain		–	88	–	dB
GBW	Gain-Bandwidth Product		–	15	–	MHz
SR	Slew Rate	COMP = 10pF	–	6	–	V/µs
Gate Drivers						
I_{UGATE}	Upper Gate Source	V_{BOOT} - V_{PHASE} = 12V	350	500	–	mA
I_{UGATE}	Upper Gate Sink	V_{UGATE} - V_{PHASE} = 1V	–	100	–	mA
I_{LGATE}	Lower Gate Source	V_{CC} = 12V, V_{LGATE} = 6V	300	450	–	mA
I_{LGATE}	Lower Gate Sink	V_{UGATE} - V_{PHASE} = 1V	–	100	–	mA
Protection						
	Over-Voltage Trip (V_{SEN}/DACOUT)		–	115	120	%
I_{OCSET}	OCSET Current Source	V_{OCSET} = 4.5V_{DC}	170	200	230	µA
I_{OVP}	OVP Sourcing Current	V_{SEN} = 5.5V, V_{OVP} = 0V	60	–	–	mA
I_{SS}	Soft Start Current		–	10	–	µA
Power Good						
	Upper Threshold (V_{SEN}/DACOUT)	VSEN Rising	106	–	111	%
	Lower Threshold (V_{SEN}/DACOUT)	VSEN Falling	89	–	94	%
	Hysteresis (V_{SEN}/DACOUT)	Upper and Lower Threshold	–	2	–	%
V_{PGOOD}	PGOOD Voltage Low	I_{PGOOD} = -5mA	–	0.5	–	V

Functional Description

Initialization

The RC5054A automatically initializes upon receipt of power. Special sequencing of the input supplies is not necessary. The Power-On Reset (POR) function continually monitors the input supply voltages. The POR monitors the bias volt-age at the V_{CC} pin and the input voltage (V_{IN}) on the OCSET pin. The level on OCSET is equal to V_{IN} less a fixed voltage drop (see over-current protection). The POR function initiates soft start operation after both input supply voltages exceed their POR thresholds. For operation with a single +12V power source, V_{IN} and V_{CC} are equivalent and the +12V power source must exceed the rising V_{CC} threshold before POR initiates operation.

Soft Start

The POR function initiates the soft start sequence. An internal 10µA current source charges an external capacitor (C_{SS}) on the SS pin to 4V. Soft start clamps the error amplifier output (COMP pin) and reference input (+ terminal of error amp) to the SS pin voltage. Figure 1 shows the soft start interval with C_{SS} = 0.1µF. Initially the clamp on the error amplifier (COMP pin) controls the converter's output voltage. At t_1 in Figure 1, the SS voltage reaches the valley of the oscillator's triangle wave. The oscillator's triangular waveform is compared to the ramping error amplifier voltage. This generates PHASE pulses of increasing width that charge the output capacitor(s). This interval of increasing pulse width continues to t_2. With sufficient output voltage, the clamp on the reference input controls the output voltage. This is the interval between t_2 and t_3 in Figure 1. At t_3 the SS voltage exceeds the DACOUT voltage and the output voltage is in regulation. This method provides a rapid and controlled output voltage rise. The PGOOD signal toggles 'high' when the output voltage (VSEN pin) is within ±5% of DACOUT. The 2% hysteresis built into the power good comparators prevents PGOOD oscillation due to nominal output voltage ripple.

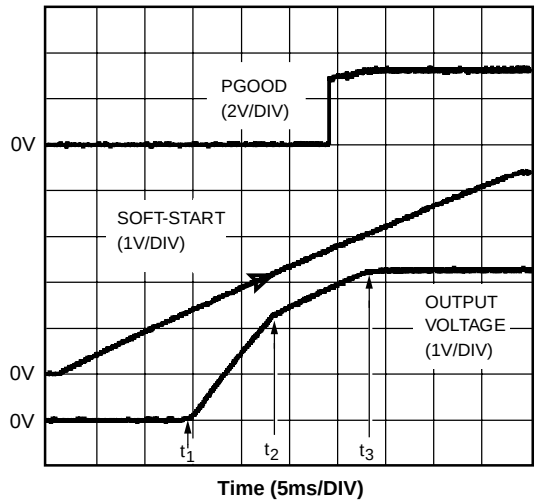


Figure 1. Soft Start Interval

Over-Current Protection

The over-current function protects the converter from a shorted output by using the upper MOSFET's on-resistance, $R_{DS(ON)}$ to monitor the current. This method enhances the converter's efficiency and reduces cost by eliminating a current sensing resistor. The over-current function cycles the soft-start function in a hiccup mode to provide fault protection. A resistor (R_{OCSET}) programs the over-current trip level. An internal 200µA current sink develops a voltage across R_{OCSET} that is referenced to V_{IN}. When the voltage across the upper MOSFET (also referenced to V_{IN}) exceeds the voltage across R_{OCSET} , the over-current function initiates a soft-start sequence. The soft-start function discharges C_{SS} with a 10µA current sink and inhibits PWM operation. The soft-start function recharges C_{SS}, and PWM operation resumes with the error amplifier clamped to the SS voltage. Should an overload occur while recharging C_{SS}, the soft start function inhibits PWM operation while fully charging C_{SS} to 4V to complete its cycle. Figure 2 shows this operation with an overload condition. Note that the inductor current increases to over 15A during the CSS charging interval and causes an over-current trip. The converter dissipates very little power with this method. The measured input power for the conditions of Figure 2 is 2.5W.

The over-current function will trip at a peak inductor current (I_{PEAK}) determined by:

$$I_{PEAK} = \frac{I_{OCSET} \bullet R_{OCSET}}{R_{DS(ON)}}$$

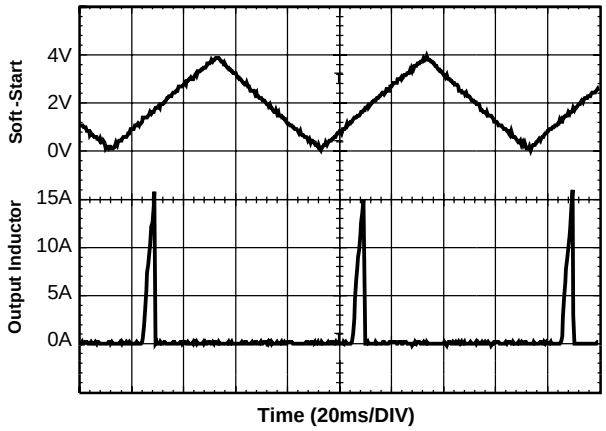


Figure 2. Over-Current Operation

where I_{OCSET} is the internal OCSET current source (200µA typical). The OC trip point varies mainly due to the MOSFET's $R_{DS(ON)}$ variations. To avoid over-current tripping in the normal operating load range, find the R_{OCSET} resistor from the equation above with:

- The maximum $R_{DS(ON)}$ at the highest junction temperature.
- The minimum I_{OCSET} from the specification table.
- Determine I_{PEAK} for $I_{PEAK} > I_{OUT(MAX)} + (\Delta I)/2$, where ΔI is the output inductor ripple current.

For an equation for the ripple current see the section under component guidelines titled 'Output Inductor Selection.'

A small ceramic capacitor should be placed in parallel with R_{OCSET} to smooth the voltage across R_{OCSET} in the presence of switching noise on the input voltage.

Output Voltage Program

The output voltage of a RC5054A converter is programmed to discrete levels between $1.3V_{DC}$ and $3.5V_{DC}$. The voltage identification (VID) pins program an internal voltage reference (DACOUT) with a 5-bit digital-to-analog converter (DAC). The level of DACOUT also sets the PGOOD and OVP thresholds. Table 1 specifies the DACOUT voltage for the 32 combinations of open or short connections on the VID pins. The output voltage should not be adjusted while the converter is delivering power. Remove input power before changing the output voltage. Adjusting the output voltage during operation could toggle the PGOOD signal and exercise the overvoltage protection.

Grounding any combination of the VID pins increases the DACOUT voltage.

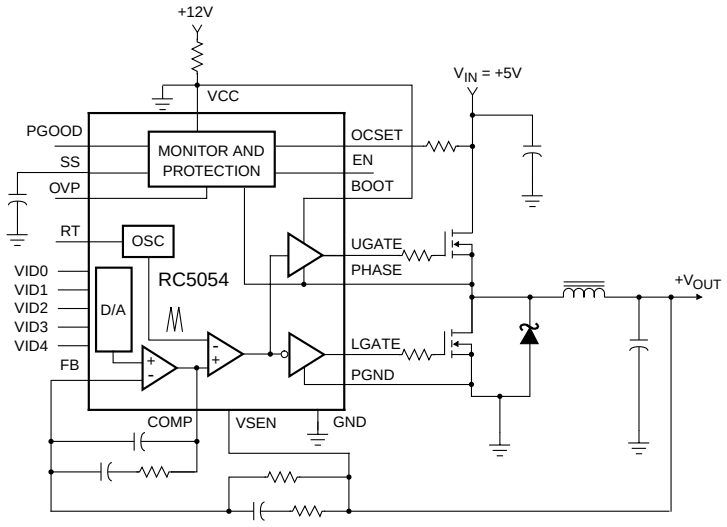
Table 1. Output Voltage Table

PIN NAME					NOMINAL OUTPUT VOLTAGE	PIN NAME					NOMINAL OUTPUT VOLTAGE
VID4	VID3	VID2	VID1	VID0		VID4	VID3	VID2	VID1	VID0	
0	1	1	1	1	1.30	1	1	1	1	1	SHDN
0	1	1	1	0	1.35	1	1	1	1	0	2.1
0	1	1	0	1	1.40	1	1	1	0	1	2.2
0	1	1	0	0	1.45	1	1	1	0	0	2.3
0	1	0	1	1	1.50	1	1	0	1	1	2.4
0	1	0	1	0	1.55	1	1	0	1	0	2.5
0	1	0	0	1	1.60	1	1	0	0	1	2.6
0	1	0	0	0	1.65	1	1	0	0	0	2.7
0	0	1	1	1	1.70	1	0	1	1	1	2.8
0	0	1	1	0	1.75	1	0	1	1	0	2.9
0	0	1	0	1	1.80	1	0	1	0	1	3.0
0	0	1	0	0	1.85	1	0	1	0	0	3.1
0	0	0	1	1	1.90	1	0	0	1	1	3.2
0	0	0	1	0	1.95	1	0	0	1	0	3.3
0	0	0	0	1	2.00	1	0	0	0	1	3.4
0	0	0	0	0	2.05	1	0	0	0	0	3.5

Note:

1. 0 = connected to GND or V_{SS}, 1 = OPEN

Typical Application



Applications Discussion

Layout Considerations

As in any high frequency switching converter, layout is very important. Switching current from one power device to another can generate voltage transients across the impedances of the interconnecting bond wires and circuit traces. These interconnecting impedances should be minimized by using wide, short printed circuit traces. The critical components should be located as close together as possible, using ground plane construction or single point grounding.

Figure 3 shows the critical power components of the converter. To minimize the voltage overshoot the interconnecting wires indicated by heavy lines should be part of ground or power plane in a printed circuit board The components shown in Figure 3 should be located as close together as possible. Please note that the capacitors C_{IN} and C_O each represent numerous physical capacitors. Locate the RC5054A within 3 inches of the MOSFETs, Q1 and Q2. The circuit traces for the MOSFETs' gate and source connections from the RC5054A must be sized to handle up to 1A peak current.

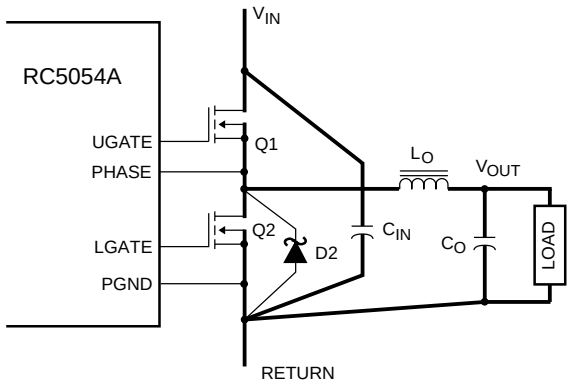


Figure 3. Printed Circuit Board Power and Ground Planes or Islands

Figure 4 shows the circuit traces that require additional layout consideration. Use single point and ground plane construction for the circuits shown. Minimize any leakage current paths on the SS PIN and locate the capacitor, C_{SS} close to the SS pin because the internal current source is only 10µA. Provide local V_{CC} decoupling between V_{CC} and GND pins. Locate the capacitor, C_{BOOT} as close as practical to the BOOT and PHASE pins.

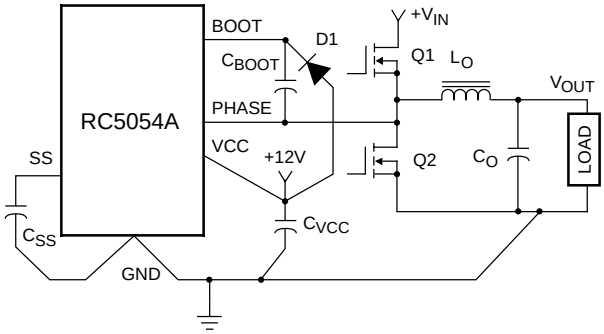


Figure 4. Printed Circuit Board Small Signal Layout Guidelines

Feedback Compensation

Figure 5 highlights the voltage-mode control loop for a synchronous-rectified buck converter. The output voltage (V_{OUT}) is regulated to the Reference voltage level. The error amplifier (Error Amp) output ($V_{E/A}$) is compared with the oscillator (OSC) triangular wave to provide a pulse-width modulated (PWM) wave with an amplitude of V_{IN} at the PHASE node. The PWM wave is smoothed by the output filter (L_O and C_O).

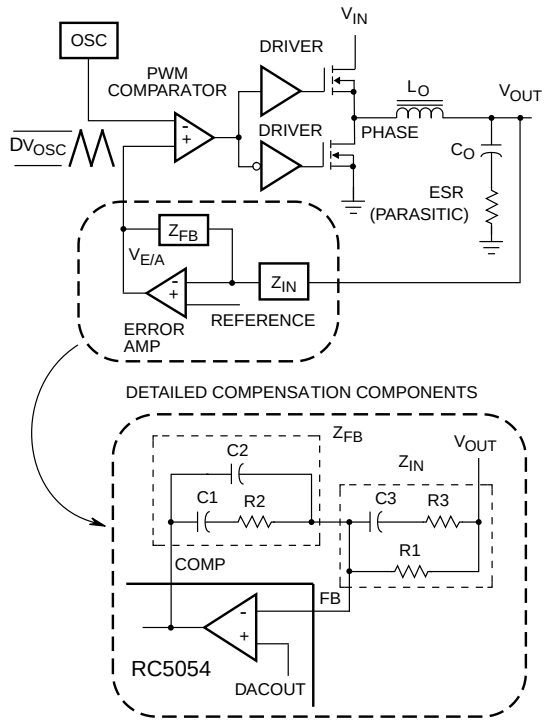


Figure 5. Voltage-Mode Buck Converter Compensation Design

The modulator transfer function is the small-signal transfer function of $V_{OUT}/V_{E/A}$. This function is dominated by a DC Gain and the output filter (L_O and C_O), with a double pole break freaquency at F_{LC} and a zero at F_{ESR}. The DC Gain of the modulator is simply the input voltage (V_{IN}) divided by the peak-to-peak oscillator voltage ΔV_{OSC}.

Modulator Break Frequency Equations

$$F_{LC} = \frac{1}{2\pi \bullet \sqrt{L_O \bullet C_O}} \qquad F_{ESR} = \frac{1}{2\pi \bullet ESR \bullet C_O}$$

The compensation network consists of the error amplifier (internal to the RC5054A) and the impedance networks Z_{IN} and Z_{FB}. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency (f_{0dB}) and adequate phase margin. Phase margin is the difference between the closed loop phase at f_{0dB} and 180 degrees. The equations below relate the compensation network's poles, zeros and gain to the components (R1, R2, R3, C1, C2, and C3) in Figure 5. Use these guidelines for locating the poles and zeros of the compensation network:

1. Pick Gain (R2/R1) for desired converter bandwidth
2. Place 1ST Zero Below Filter's Double Pole (~75% F_{LC})
3. Place 2ND Zero at Filter's Double Pole
4. Place 1ST Pole at the ESR Zero
5. Place 2ND Pole at Half the Switching Frequency
6. Check Gain against Error Amplifier's Open-Loop Gain
7. Estimate Phase Margin - Repeat if Necessary

Compensation Break Frequency Equations

$$F_{Z1} = \frac{1}{2\pi \bullet R2 \bullet C1} \qquad F_{P1} = \frac{1}{2\pi \bullet R2 \bullet \left(\frac{C1 \bullet C2}{C1 + C2}\right)}$$

$$F_{Z2} = \frac{1}{2\pi \bullet (R1 + R3) \bullet C3} \qquad F_{P2} = \frac{1}{2\pi \bullet R3 \bullet C3}$$

Figure 6 shows an asymptotic plot of the DC-DC converter's gain vs. frequency. The actual Modulator Gain has a high gain peak due to the high Q factor of the output filter and is not shown in Figure 6. Using the above guidelines should give a Compensation Gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at F_{P2} with the capabilities of the error amplifier. The Closed Loop Gain is constructed on the log-log graph of Figure 6 by adding the Modulator Gain (in dB) to the Compensation Gain (in dB). This is equivalent to multiplying the modulator transfer function to the compensation transfer function and plotting the gain.

The compensation gain uses external impedance networks Z_{FB} and Z_{IN} to provide a stable, high bandwidth (BW) overall loop. A stable control loop has a gain crossing with -20dB/decade slope and a phase margin greater than 45 degrees. Include worst case component variations when determining phase margin.

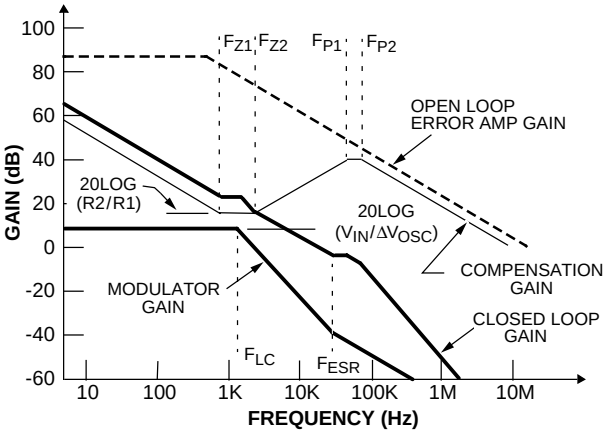


Figure 6. Asymptotic Bode Plot of Converter Gain

Component Selection Guidelines

Output Capacitor Selection

An output capacitor is required to filter the output and supply the load transient current. The filtering requirements are a function of the switching frequency and the ripple current. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout.

Modern microprocessors produce transient load rates above 1A/ns. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (effective series resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements. For example, Intel recommends that the high frequency decoupling for the Pentium Pro be composed of at least forty (40) 1µF ceramic capacitors in the 1206 surface-mount package.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the equivalent series inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

Output Inductor Selection

The output inductor is selected to meet the output voltage ripple requirements and minimize the converter's response time to the load transient. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current. The ripple voltage and current are approximated by the following equations:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{FS \times L} \bullet \frac{V_{OUT}}{V_{IN}} \qquad \Delta V_{OUT} = \Delta I \times ESR$$

Increasing the value of inductance reduces the ripple current and voltage. However, the large inductance values reduce the converter's response time to a load transient.

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the RC5054A will provide either 0% or 100% duty cycle in response to a load transient. The response time is the time required to slew the inductor current from an initial current value to the transient current level. During this interval the difference between the inductor current and the transient current level must be supplied by the output capacitor. Minimizing the response time can minimize the output capacitance required.

The response time to a transient is different for the application of load and the removal of load. The following equations give the approximate response time interval for application and removal of a transient load:

$$t_{RISE} = \frac{L \times I_{TRAN}}{V_{IN} - V_{OUT}} \qquad t_{FALL} = \frac{L \times I_{TRAN}}{V_{OUT}}$$

where: I_{TRAN} is the transient load current step, t_{RISE} is the response time to the application of load, and t_{FALL} is the response time to the removal of load. With a +5V input source, the worst case response time can be either at the application or removal of load and dependent upon the DACOUT setting. Be sure to check both of these equations at the minimum and maximum output levels for the worst case response time.

Input Capacitor Selection

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time Q1 turns on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of Q1 and the source of Q2.

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current rating requirement for the input capacitor of a buck regulator is approximately 1/2 the DC load current.

For a through hole design, several electrolytic capacitors (Panasonic HFQ series or Nichicon PL series or Sanyo MVGX or equivalent) may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up. The TPS series available from AVX, and the 593D series from Sprague are both surge current tested.

MOSFET Selection/Considerations

The RC5054A requires 2 N-Channel power MOSFETs. These should be selected based upon $R_{DS(ON)}$, gate supply requirements, and thermal management requirements.

In high-current applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components; conduction loss and switching loss. The conduction losses are the largest component of power dissipation for both the upper and the lower MOSFETs. These losses are distributed between the two MOSFETs according to duty factor (see the equations below). Only the upper MOSFET has switching losses, since the Schottky rectifier clamps the switching node before the synchronous rectifier turns on. These equations assume linear voltage-current transitions and do not adequately model power loss due the reverse-recovery of the lower MOSFET's body diode. The gate-charge losses are dissipated by the RC5054A and don't heat the MOSFETs. However, large gate-charge increases the switching interval, t_{SW}, which increases the upper MOSFET switching losses. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

$$P_{LOWER} = I_O^2 \times R_{DS(ON)} \times (1 - D)$$

$$P_{UPPER} = I_O^2 \times R_{DS(ON)} \times D + \frac{1}{3} Io \times V_{IN} \times t_{SW} \times F_S$$

Where: D is the duty cycle = V_{OUT}/V_{IN},
t_{SW} is the switching interval, and
F_S is the switching frequency

Standard-gate MOSFETs are normally recommended for use with the RC5054A. However, logic-level gate MOSFETs can be used under special circumstances. The input voltage, upper gate drive level, and the MOSFET's absolute gate-to-source voltage rating determine whether logic-level MOSFETs are appropriate.

Figure 7 shows the upper gate drive (BOOT pin) supplied by a bootstrap circuit from V_{CC}. The boot capacitor, C_{BOOT} develops a floating supply voltage referenced to the PHASE pin. This supply is refreshed each cycle to a voltage of V_{CC} less the boot diode drop (V_D) when the lower MOSFET, Q2 turns on. Logic-level MOSFETs can only be used if the MOSFET's absolute gate-to-source voltage rating exceeds the maximum voltage applied to V_{CC}.

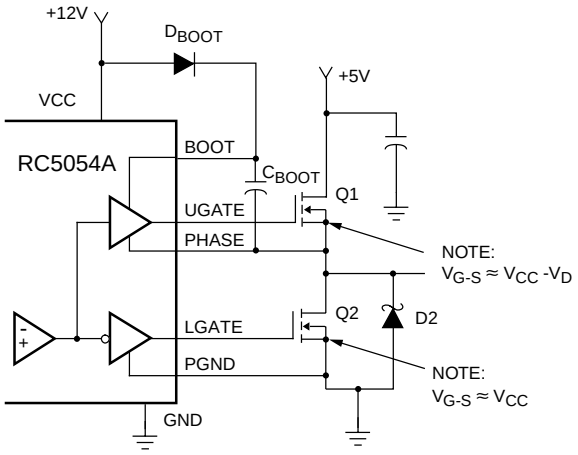


Figure 7. Upper Gate Drive - Bootstrap Option

Figure 8 shows the upper gate drive supplied by a direct connection to V_{CC}. This option should only be used in converter systems where the main input voltage is $+5V_{DC}$ or less. The peak upper gate-to-source voltage is approximately V_{CC} less the input supply. For +5V main power and +12VDC for the bias, the gate-to-source voltage of Q1 is 7V. A logic-level MOSFET is a good choice for Q1 and a logic-level MOSFET can be used for Q2 if its absolute gate-to-source voltage rating exceeds the maximum voltage applied to V_{CC}.

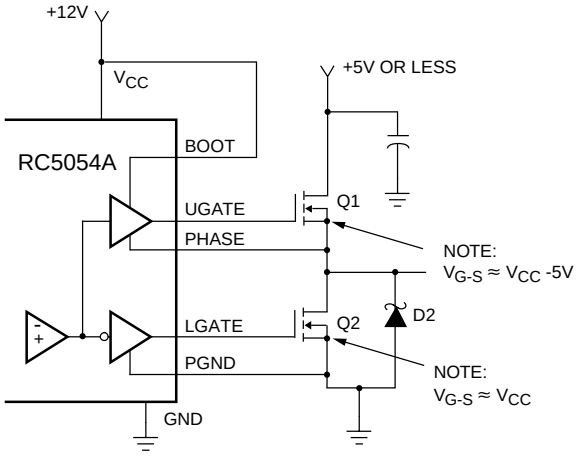


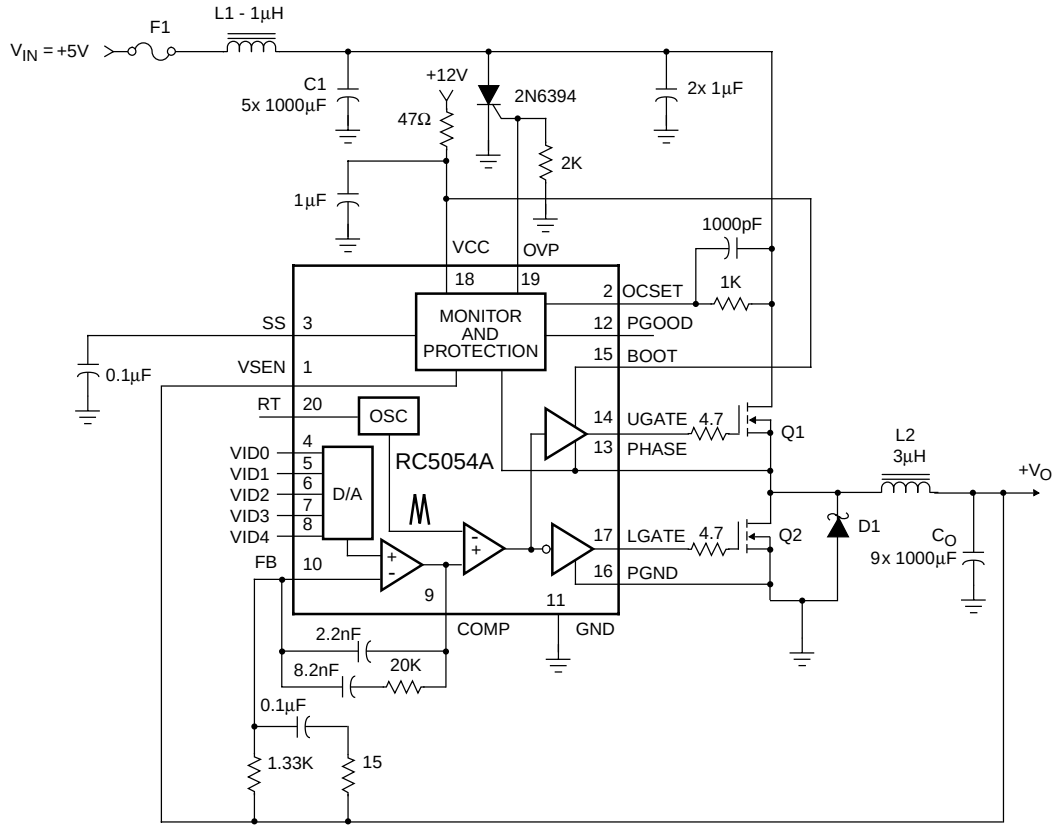
Figure 8. Upper Gate Drive - Direct V_{CC} Drive Option

Schottky Selection

Rectifier D2 is a clamp that catches the negative inductor swing during the dead time between turning off the lower MOSFET and turning on the upper MOSFET. The diode must be a Schottky type to prevent the lossy parasitic MOSFET body diode from conducting. It is acceptable to omit the diode and let the body diode of the lower MOSFET clamp the negative inductor swing, but efficiency will drop one or two percent as a result. The diode's rated reverse breakdown voltage must be greater than the maximum input voltage.

RC5054A DC-DC Converter Application Circuit

Figure 10 shows an application circuit of a DC-DC Converter for an Intel Pentium Pro microprocessor.



Component Selection Notes;

C_0 - 9 Each 1000µF 6.3W VDC, Sanyo MV-GX or Equivalent
C1 - 5 Each 1000µF 25W VDC, Sanyo MV-GX or Equivalent
L2 - Core: Micrometals T50-52B; Each Winding: 10 Turns of 16AWG
L1 - Core: Micrometals T50-52; Winding: 5 Turns of 18AWG
D1 - 3A, 40V Schottky, Motorola MBR340 or Equivalent
Q1, Q2 - Fairchild FDB6030L

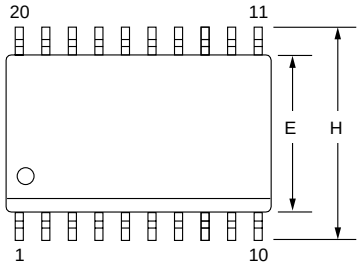
Figure 9. Pentium Pro DC-DC Converter

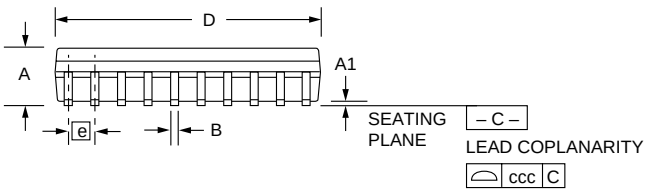
Mechanical Dimensions (20 Lead SOIC)

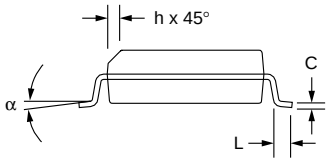
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.496	.512	12.60	13.00	2
E	.291	.299	7.40	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.029	0.25	0.75	
L	.016	.050	0.40	1.27	3
N	20		20		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Ordering Information

Part Number	Temperature Range (°C)	Package
RC5054AM	0 to 70	20 Ld SOIC

RC5055

Programmable Synchronous DC-DC Converter Controller for Low Voltage Microprocessors, Vtt and Clock Linear Regulator

Features

- Current Sensing is achieved using MOSFET $R_{DS(ON)}$
- Programmable output from 1.3V to 3.5V using an integrated 5-bit DAC
- 85% efficiency typical at full load
- Adjustable operation from 100KHz to 1MHz
- Integrated Power Good and Enable/Soft Start functions
- Overvoltage protection pin controls external SCR
- Short circuit protection with current limiting
- Drives N-channel MOSFETs
- 24 pin SSOP and SOIC package
- Meets Intel Pentium II specifications using minimum number of external components
- On board Linear regulator for GTL termination
- On board fixed linear regulator for Clock power supply
- TTL Compatible inputs

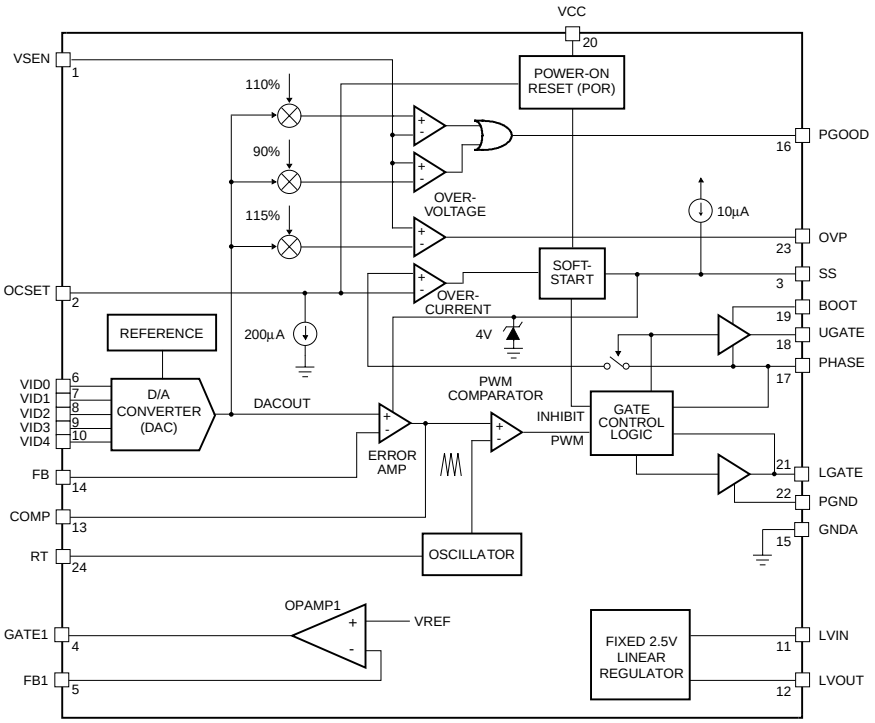
Applications

- Power supply for Pentium® II
- VRM for Pentium II processor
- Programmable step-down power supply

Description

The RC5055 is a triple combo combining a synchronous DC-DC controller with a fixed 2.5V output linear regulator and an adjustable linear regulator. The synchronous mode DC-DC controller provides an accurate, programmable output voltage for all Pentium II CPU applications. It uses a 5-bit D/A converter to program the output voltage from 1.3V to 3.5V and uses a high level of integration to deliver load currents in excess of 17A from a 5V source with minimal external circuitry. Synchronous-mode operation offers optimum efficiency over the entire specified output voltage range, and the internal oscillator can be programmed from 100KHz to 1MHz for additional flexibility in choosing external components. An on-board precision low TC reference achieves tight tolerance voltage regulation without expensive external components. The RC5055 also offers integrated functions including Power Good, Output Enable/Soft Start, over-voltage protection and current limiting.

Block Diagram



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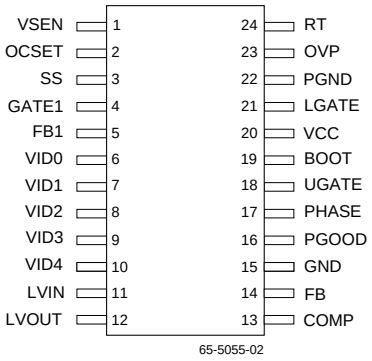
Pin Assignments



Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	VSEN	This pin is connected to the converter's output voltage. The PGOOD and OVP comparator circuits use this signal to report output voltage status and for overvoltage protection.
2	OCSET	Connect a resistor (ROCSET) from this pin to the drain of the upper MOSFET. An internal 200µA current source (Iocs) and the upper MOSFET $R_{DS(ON)}$ set the converter peak over-current trip point: $$I_{PEAK} = \frac{I_{OCS} \bullet R_{OCSET}}{R_{DS(ON)}}$$
3	SS	Soft Start. A capacitor from this point to ground together with an internal 10µA will cause the output duty cycle to increase slowly
4	GATE1	Linear Regulator Error Amplifier Output.
5	FB1	Linear Regulator Error Amplifier Inverting Input. When FB1 and GATE1 are tied together the Output Voltage = Vref
6-10	VID0-4	DAC inputs. Used to adjust the output voltage to the voltage required by the processor.
11	LVIN	Input for fixed linear regulator
12	LVOUT	2.5V fixed output from fixed linear regulator
13	COMP	PWM Loop Error Amplifier output.
14	FB	PWM Loop Voltage Feedback. Inverting input of Error Amplifier.
15	GND	Analog Ground.
16	PGOOD	Power good. This pin is pulled low when any of the regulator's output is not within the spec.
17	PHASE	Connect the PHASE pin to the upper MOSFET source. This pin is used to monitor the voltage drop across the MOSFET for over-current protection. This pin also provides the return path for the upper gate drive.
18	UGATE	Upper MOSFET gate driver
19	BOOT	Upper MOSFET bootstrap.
20	VCC	12V bias supply.
21	LGATE	Low MOSFET gate driver.
22	PGND	Power ground.
23	OVP	Over-voltage Protection. This pin drives an external SCR.
24	RT	Oscillator switching frequency adjust according to the following equations: $$F_S = 200kHz + \frac{3.5 \times 10^6 [KHz \times Kohm]}{R_T[Kohm]} \quad (R_T \text{ to GND})$$ $$F_S = 200kHz - \frac{3 \times 10^5 [KHz \times Kohm]}{R_T[Kohm]} \quad (R_T \text{ to 12V})$$

Absolute Maximum Ratings

Parameter	Min.	Max.
Power Input Voltage, Vin		6V
Supply Voltage Vcc		13.5V
Boot Voltage, V_{BOOT}-V_{PHASE}		13.5V
I/O Voltages	GND-0.3V	Vin+0.3V
ESD Classification		Class 2

Operating Conditions

Parameter	Min.	Max.
Supply Voltage	+12V -10%	+12+10%
Ambient Temperature	0°C	70°C
Junction Temperature	0°C	125°C

Thermal Information

Parameter	Conditions	Min.	Typ.	Max.
Thermal Resistance, Θ_{JA}	SOIC SSOP		80 89	°C/W
Maximum Junction Temperature				150°C
Storage Temperature		-65°C		150°C
Maximum Lead Temperature	Soldering 10 Seconds			300°C

Electrical Specifications

(V_{CC}=12V, F_{OSC}=200KHz and T_A=25°C using circuit in figure 1, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
PWM Section						
VCC Supply Current						
Nominal Supply	I_{CC}	UGATE and LGATE Open	–	24	35	mA
Power-On Reset						
Rising VCC Threshold		V_{OCSET} = 4.5V	–	–	10.4	V
Falling VCC Threshold		V_{OCSET} = 4.5V	8.8	–	–	V
Rising V_{OCSET} Threshold			–	1.26	–	V
Oscillator						
Free Running Frequency	F_S	RT = OPEN	185	200	215	kHz
Ramp Amplitude	ΔV_{OSC}	RT = OPEN	–	1.9	–	V_{P-P}
Reference and DAC						
Input Voltage Setpoint		I_{LOAD} = 0.8A, V_{OUT}=2.000V VOUT=1.550V	1.980 1.534	2.000 1.550	2.020 1.566	V V
Error Amplifier						
DC Gain	A_{DC}		–	88	–	dB
Gain-Bandwidth Product	GBW		–	15	–	MHz
Slew Rate	SR	COMP = 10pF	–	6	–	V/µs

Electrical Specifications (continued)

(V_{CC}=12V, F_{OSC}=200KHz and T_A=25°C using circuit in figure 1, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Gate Driver						
Upper Gate Source Current	I_{UGATE}	V_{BOOT} - V_{PHASE} = 12V		1	–	A
Lower Gate Source Current	I_{LGATE}	V_{CC} = 12V, V_{LGATE} = 6V		1	–	A
Protection						
Over-Voltage Trip (V_{SEN}/DACOUT)			–	115	120	%
OCSET Current Source	I_{OCSET}	V_{OCSET} = 4.5V_{DC}	170	200	230	µA
OVP Sourcing Current	I_{OVP}	V_{SEN} = 5.5V; V_{OVP} = 0V	60	–	–	mA
Soft Start Current	I_{SS}		–	10	–	µA
Power Good						
Upper Threshold (V_{SEN} /DACOUT)		V_{SEN} Rising	106	–	111	%
Lower Threshold (V_{SEN} /DACOUT)		V_{SEN} Falling	89	–	94	%
Hysteresis (V_{SEN} /DACOUT)		Upper and Lower Threshold	–	2	–	%
PGOOD Voltage Low	V_{PGOOD}	I_{PGOOD} = -5mA	–	0.5	–	V
Adjustable Linear Regulator						
Output Voltage		Set by external resistors	1.3			V
Output Voltage Precision		I_{LOAD} = 50 mAto 5.4A V_{CC} = 12V ± 10% T_A = 0 to 70°C	-2		+2	%
Under Voltage Level		Power good trigger point		60		%
Controller Output Current	GATE 1		20			mA
Output Transient Tolerance		50mA to 4.4 Amp Set by ESR of output caps	-135		135	mV
Bias Current	FB 1			1		µA
Feedback Voltage	FB 1			1.265		V
Fixed Linear Regulator						
Output Voltage	V_{OUT}	$I_{LOAD} \leq$ 100mA V_{CC} = 12V ± 10% V_{IN} = 5V	2.375	2.5	2.625	V
Under Voltage Level		Power good trigger point		60		%
Output Current	I_{OUT}	V_{CC} = 12V ± 10% V_{IN} = 5V	100			mA
Over Current Trip Point		V_{CC} = 12V ± 10% V_{IN} = 5V		150		mA
I_{SC} Foldback		V_{OUT} = 0		25		mA
Input Voltage	V_{IN}	V_{CC} = 12V ± 10%	4.75	5	5.25	V

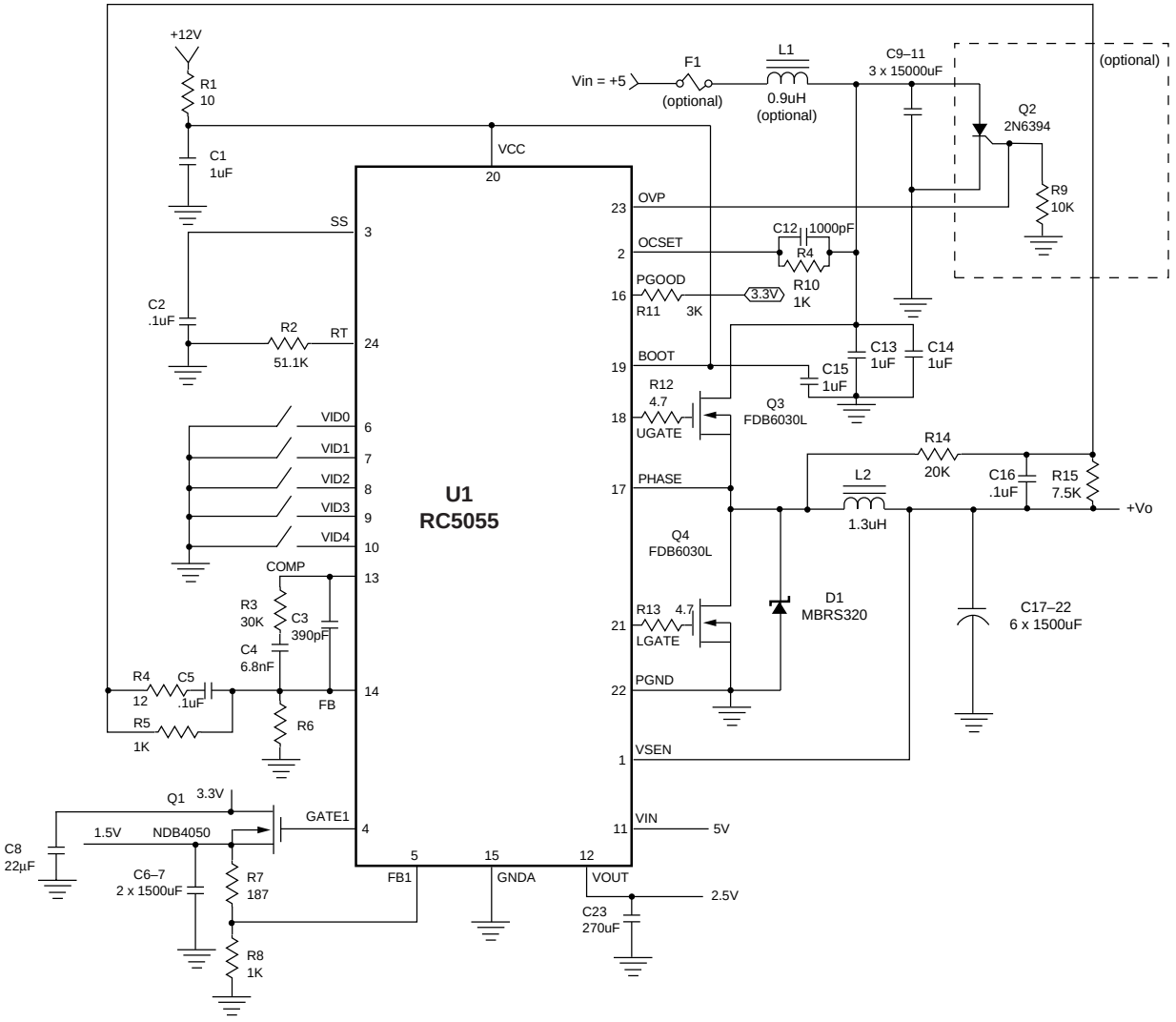


Figure 1. Deschutes 400MHz DC-DC Converter

Table 1. Deschutes 400MHz DC-DC Converter Bill of Materials

Item	Manufacturer Part #	Quantity	Description	Requirements/Comments
C1, C13–15	Any	4	1µF, 16V Capacitor	
C2, C5, C16	Any	3	100nF, 50V Capacitor	
C3	Any	1	390pF, 50V Capacitor	
C4	Any	1	6.8nF, 50V Capacitor	
C6–7, C17–22	Sanyo 6MV1500GX	8	1500µF, 6.3V Electrolytic	ESR ≤ 44MΩ
C8		1	22µF, 16V Capacitor	
C9–11	Sanyo 10MV1200GX	3	1200µF, 10V Electrolytic	I_{RMS} = 2A
C12	Any	1	1nF, 50V Capacitor	
C23	Sanyo 6MV270GX	1	270µF, 6.3V Electrolytic	
D1	Fairchild MBRS320L	1	3A, 20V Schottky Diode	
L1	Any	Optional	0.9µH inductor	See Note 1.
L2	Any	1	1.3µH inductor1.3µH	See Note 2.
Q1	Fairchild NDB4050	1	N-Channel MOSFET	
Q2	Motoraola 2N6394	1	SCR	
Q3–4	Fairchild FDB6030L	2	N-Channel MOSFET	$R_{DS(ON)}$ =20mΩ @ V_{GS} = 4.5V
R1	Any	1	10Ω	
R2	Any	1	51.1KΩ	
R3	Any	1	30.1KΩ	
R4	Any	1	12Ω	
R5, R8, R10	Any	3	1KΩ	
R6	Any	1		Used to adjust output voltage offset.
R7	Any	1	187Ω	
R9	Any	1	10KΩ	
R11	Any	1	3.01KΩ	
R12–13	Any	2	4.7Ω	
R14	Any	1	20KΩ	
R15	Any	1	7.5KΩ	
F1	Littelfuse	1	12A, 32V fast-acting fuse	
U1	Fairchild RC5055M	1	DC/DC Controller	

Notes:

1. 12 turns of 16AWG wire on mocrometals T60-2 core.
2. 9 turns of 16AWG wire on Micrometals T50-8/90 core.

Applications

Increasing the Clock Current

The RC5055 can produce as much as 100mA of current at 2.5V for powering the motherboard's clock chips. If additional current capability is required, an external PNP transistor may be used to enhance the current to 600mA or more, as shown in Figure 2. This circuit also provides a measure of current limit by letting the first 100mA of current be sourced through the 6.8Ω resistor, so that if too much collector, and thus base, current is demanded, the RC5055 cuts off the drive to the base.

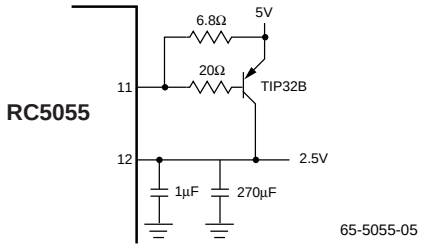


Figure 2. Boosting the Clock Current

Table 2. Output Voltage Table

PIN NAME					NOMINAL OUTPUT VOLTAGE	PIN NAME					NOMINAL OUTPUT VOLTAGE
VID4	VID3	VID2	VID1	VID0		VID4	VID3	VID2	VID1	VID0	
0	1	1	1	1	1.30	1	1	1	1	1	2.0
0	1	1	1	0	1.35	1	1	1	1	0	2.1
0	1	1	0	1	1.40	1	1	1	0	1	2.2
0	1	1	0	0	1.45	1	1	1	0	0	2.3
0	1	0	1	1	1.50	1	1	0	1	1	2.4
0	1	0	1	0	1.55	1	1	0	1	0	2.5
0	1	0	0	1	1.60	1	1	0	0	1	2.6
0	1	0	0	0	1.65	1	1	0	0	0	2.7
0	0	1	1	1	1.70	1	0	1	1	1	2.8
0	0	1	1	0	1.75	1	0	1	1	0	2.9
0	0	1	0	1	1.80	1	0	1	0	1	3.0
0	0	1	0	0	1.85	1	0	1	0	0	3.1
0	0	0	1	1	1.90	1	0	0	1	1	3.2
0	0	0	1	0	1.95	1	0	0	1	0	3.3
0	0	0	0	1	2.00	1	0	0	0	1	3.4
0	0	0	0	0	2.05	1	0	0	0	0	3.5

Note:

1. 0 = connected to GND or V_{SS}, 1 = OPEN

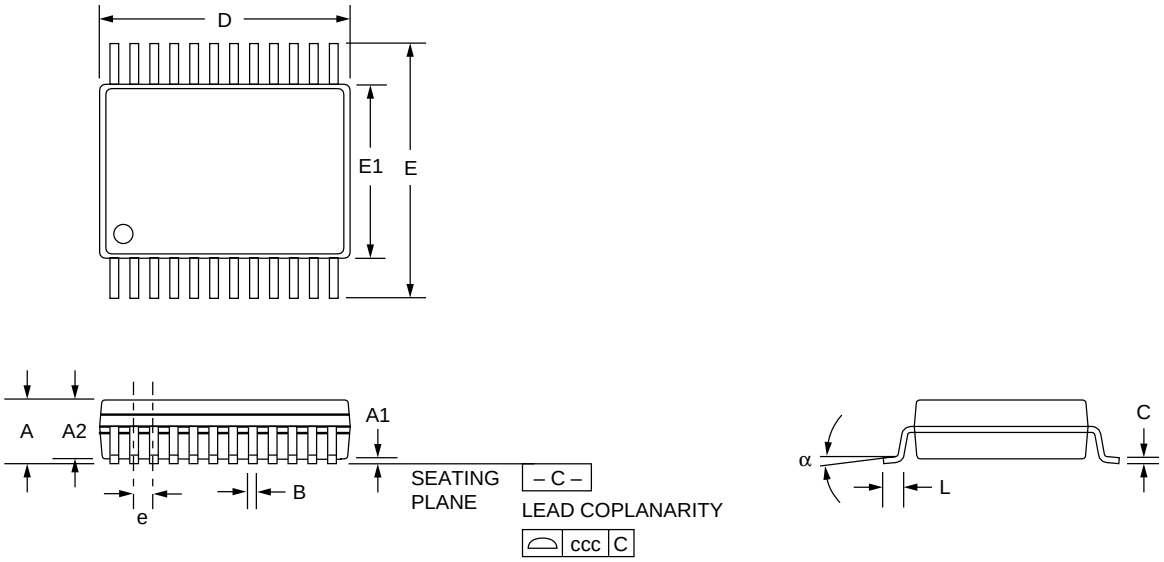
Package Dimensions

24-pin SSOP package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.078	—	2.00	
A1	.002	—	0.05	—	
A2	.065	.073	1.65	1.85	
b	.010	.015	0.22	0.38	5
c	.0035	.010	0.09	0.25	5
D	.311	.335	7.90	8.50	2, 4
E	.291	.323	7.40	8.20	
E1	.197	.220	5.00	5.60	2
e	.026 BSC		0.65 BSC		
L	.022	.037	0.55	0.95	3
N	24		24		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .006 inch (0.15mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "b" and "c" dimensions include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.

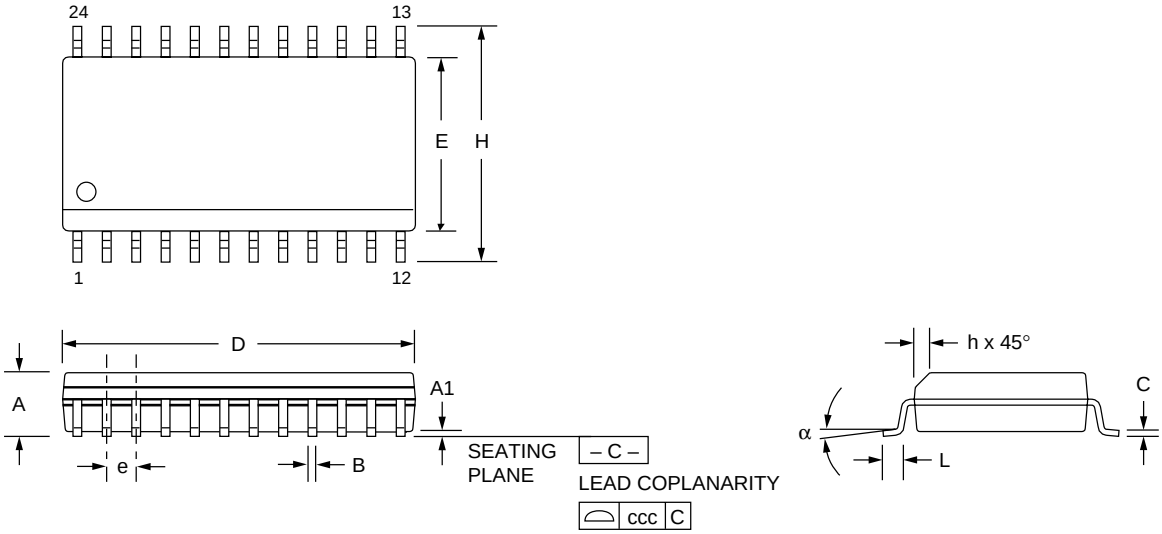


24-pin .300 mil SOIC package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.599	.614	15.20	15.60	2
E	.290	.299	7.36	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.020	0.25	0.51	
L	.016	.050	0.40	1.27	3
N	24		24		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.



Notes

Ordering Information

Product Number	Package
RC5055G	24 pin SSOP
RC5055M	24 pin SOIC

RC5056

Programmable Synchronous DC-DC Converter Controller for Low Voltage Microprocessors and Vtt Linear Regulator

Features

- Current Sensing is achieved using MOSFET $R_{DS(ON)}$
- Programmable output from 1.3V to 3.5V using an integrated 5-bit DAC
- 85% efficiency typical at full load
- Adjustable operation from 50KHz to 1MHz
- Integrated Power Good and Enable/Soft Start functions
- Overvoltage protection pin controls external SCR
- Short circuit protection with current limiting
- Drives N-channel MOSFETs
- 20 pin SSOP and SOIC package
- Meets Intel Pentium II specifications using minimum number of external components
- On board LDO for GTL termination
- On board LDO for Clock power supply
- TTL Compatible inputs

Applications

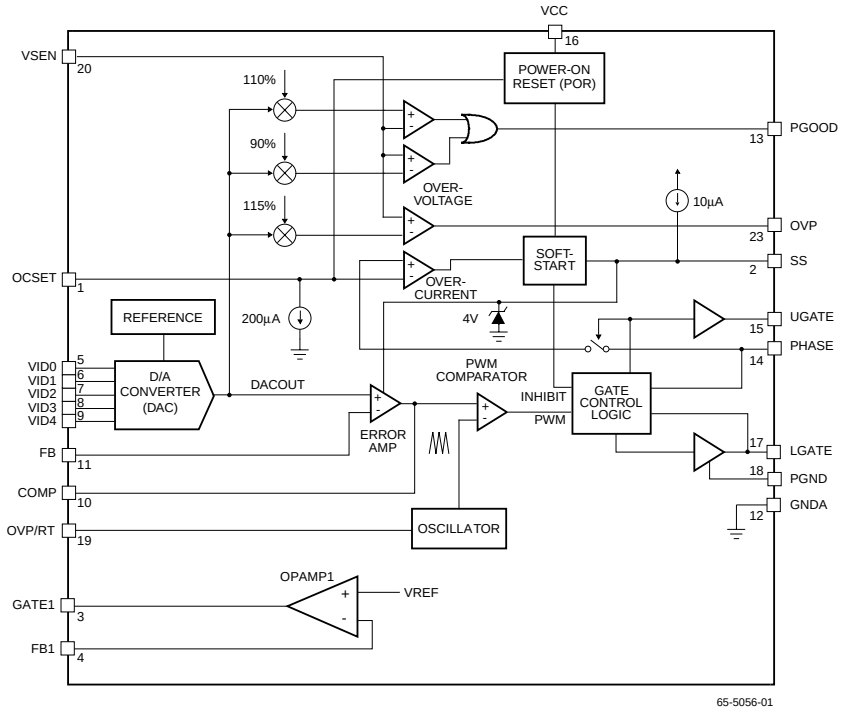
- Power supply for Pentium® II
- VRM for Pentium II processor
- Programmable step-down power supply

Description

The RC5056 is a synchronous mode DC-DC controller IC which provides an accurate, programmable output voltage for all Pentium II CPU applications. The RC5056 uses a 5-bit D/A converter to program the output voltage from 1.3V to 3.5V. The RC5056 uses a high level of integration to deliver load currents in excess of 17A from a 5V source with minimal external circuitry. Synchronous-mode operation offers optimum efficiency over the entire specified output voltage range, and the internal oscillator can be programmed from 50KHz to 1MHz for additional flexibility in choosing external components. An on-board precision low TC reference achieves tight tolerance voltage regulation without expensive external components. The RC5056 also offers integrated functions including Power Good, Output Enable/ Soft Start, over-voltage protection and current limiting. The linear regulator is also specified at 1% precision.

Preliminary Information

Block Diagram



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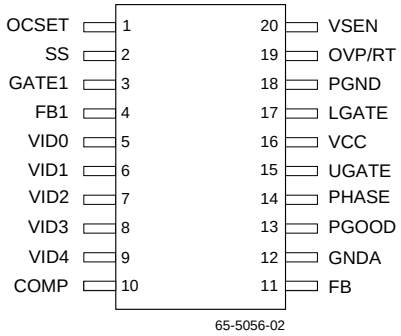
Rev. 0.9.0

Pin Assignments



Pin Definitions

Pin Number	Pin Name	Pin Function Description
20	VSEN	This pin is connected to the converter's output voltage. The PGOOD and OVP comparator circuits use this signal to report output voltage status and for overvoltage protection.
1	OCSET	Connect a resistor (ROCSET) from this pin to the drain of the upper MOSFET. An internal 200µA current source (Iocs) and the upper MOSFET $R_{DS(ON)}$ set the converter peak over-current trip point: $$I_{PEAK} = \frac{I_{OCS} \bullet R_{OCSET}}{R_{DS(ON)}}$$
2	SS	Soft Start. A capacitor from this point to ground together with an internal 10µA will cause the output duty cycle to increase slowly
3	GATE1	First LDO Error Amplifier Output.
4	FB1	First LDO Error Amplifier Inverting Input. When FB1 and GATE1 are tied together the Output Voltage = Vref
5-9	VID0-4	DAC inputs. Used to adjust the output voltage to the voltage required by the processor.
10	COMP	PWM Loop Error Amplifier output.
11	FB	PWM Loop Voltage Feedback. Inverting input of Error Amplifier.
12	GND	Signal Ground.
13	PGOOD	Power good. This pin is pulled low when the converter output is not within 10% of the Dacout reference voltage.
14	PHASE	Connect the PHASE to the upper MOSFET source.
15	UGATE	Upper MOSFET gate driver
16	VCC	12V bias supply.
17	LGATE	Low MOSFET gate driver.
18	PGND	Power ground.
19	OVP/RT	Over-voltage Protection. This pin drives an external SCR. $$F_S = 200kHz + \frac{5 \times 10^6 [KHz \times Kohm]}{R_T[Kohm]} \quad (R_T \text{ to GND})$$ $$F_S = 200kHz - \frac{4 \times 10^7 [KHz \times Kohm]}{R_T[Kohm]} \quad (R_T \text{ to 12V})$$

Preliminary Information

Absolute Maximum Ratings

Parameter	Min.	Max.
Power Input Voltage, Vin		6V
Supply Voltage Vcc		13.5V
Boot Voltage, V_{BOOT}-V_{PHASE}		13.5V
I/O Voltages	GND-0.3V	Vcc+0.3V
ESD Classification		Class 2

Operating Conditions

Parameter	Min.	Max.
Supply Voltage	+12V -10%	+12+10%
Ambient Temperature	0°C	70°C
Junction Temperature	0°C	125°C

Thermal Information

Parameter	Conditions	Min.	Typ.	Max.
Thermal Resistance SOIC 24 pin package	With TBD in^2 of Copper			
Maximum Junction Temperature	Plastic Package			150°C
Storage Temperature		-65°C		150°C
Maximum Lead Temperature	Soldering 10 Seconds			300°C

Electrical Specifications

(V_{CC}=12V, F_{OSC}=200KHz and T_A=25°C using circuit in figure 1, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
PWM Section						
VCC Supply Current						
Nominal Supply	I_{CC}	UGATE and LGATE Open	–	22	–	mA
Power-On Reset						
Rising VCC Threshold		V_{OCSET} = 4.5V	–	–	10.4	V
Falling VCC Threshold		V_{OCSET} = 4.5V	8.8	–	–	V
Rising V_{OCSET} Threshold			–	1.26	–	V
Oscillator						
Free Running Frequency	F_S	RT = OPEN	185	200	215	kHz
Total Variation		6kΩ < RT to GND < 200kΩ	-15	–	+15	%
Ramp Amplitude	ΔV_{OSC}	RT = OPEN	–	1.9	–	V_{P-P}
Reference and DAC						
DACOUT Voltage Accuracy			-1.0	–	+1.0	%
Error Amplifier						
DC Gain	A_{DC}		–	88	–	dB
Gain-Bandwidth Product	GBW		–	15	–	MHz
Slew Rate	SR	COMP = 10pF	–	6	–	V/µs

Preliminary Information

Electrical Specifications (continued)

(V_{CC}=12V, F_{OSC}=200KHz and T_A=25°C using circuit in figure 1, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Gate Driver						
Upper Gate Source Current	I_{UGATE}	V_{BOOT} - V_{PHASE} = 12V	350	500	–	mA
Upper Gate Sink Current	I_{UGATE}	V_{UGATE} - V_{PHASE} = 1V	–	100	–	mA
Lower Gate Source Current	I_{LGATE}	V_{CC} = 12V, V_{LGATE} = 6V	350	450	–	mA
Lower Gate Sink Current	I_{LGATE}	V_{UGATE} - V_{PHASE} = 1V	–	100	–	mA
Protection						
Over-Voltage Trip (V_{SEN}/DACOUT)			–	115	120	%
OCSET Current Source	I_{OCSET}	V_{OCSET} = 4.5V_{DC}	170	200	230	µA
OVP Sourcing Current	I_{OVP}	V_{SEN} = 5.5V; V_{OVP} = 0V	60	–	–	mA
Soft Start Current	I_{SS}		–	10	–	µA
Power Good						
Upper Threshold (V_{SEN} /DACOUT)		V_{SEN} Rising	106	–	111	%
Lower Threshold (V_{SEN} /DACOUT)		V_{SEN} Falling	89	–	94	%
Hysteresis (V_{SEN} /DACOUT)		Upper and Lower Threshold	–	2	–	%
PGOOD Voltage Low	V_{PGOOD}	I_{PGOOD} = -5mA	–	0.5	–	V
Adjustable Linear Regulator						
Output Voltage		Set by external resistors	1.3			V
Output Voltage Precision		I_{LOAD} = 50 mAto 5.4A V_{CC} = 12V ± 10% T_A = 0 to 70°C R_1 = TBD R_2 = TBD	-2		+2	%
Controller Output Current	GATE 1		20			mA
Output Transient Tolerance		50mA to 4.4 Amp Set by ESR of output caps	-135		135	mV
Bias Current	FB 1			1		µA
Feedback Voltage	FB 1			1265		mV

Preliminary Information

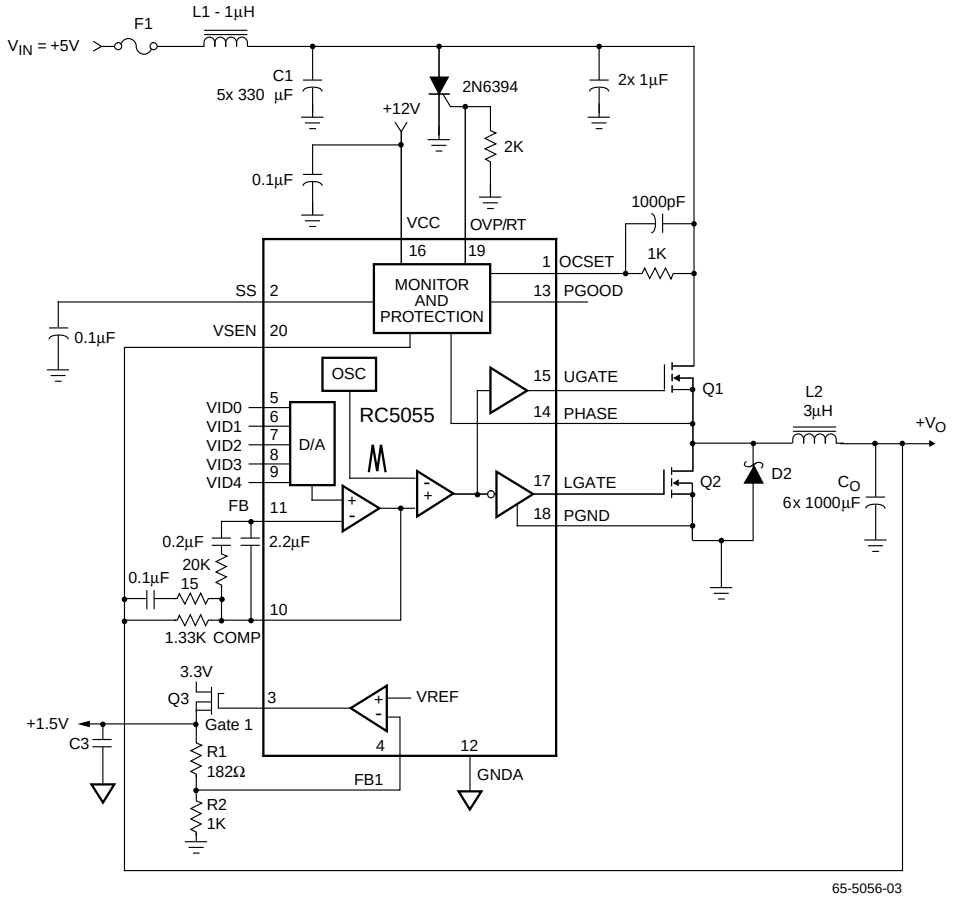


Figure 1. Pentium II DC-DC Converter

Table 1. Bill of Materials for Figure 1

Item	Quantity	Manufacturer	Part Number	Description
C0	6	Sanyo	MV-GX	1000µF 6.3 WVDC
C1	5	Sanyo	MV-GX	330µF 25 WVDC
C3	2	Sanyo	10MV1200GX	1200µF 10 WVDC
R1	1	Generic		182Ω 1%
R2	2	Generic		1K 1%
L1	1	Micrometals	Core: T50-52	5 Turns of 18 AWG Copper Wire
L2	1	Micrometals	Core: T50-52B	5 Turns of 16 AWG Copper Wire
D1	1	Generic	1N4148	Diode
D2	1	Motorola	MBR340	Schottky Diode
Q1, Q2	2	Fairchild Semiconductor	NDB7030L	Power MOSFET
Q3	1	Fairchild Semiconductor	NDB4050	MOSFET $R_{DS(ON)}$ = 1Ω

Preliminary Information

The output voltage of a RC5056 converter is programmed to discrete levels between 1.3VDC and 3.5VDC . The voltage identification (VID) pins program an internal voltage reference (DACOUT) with a 5-bit digital-to-analog converter (DAC). The level of DACOUT also sets the PGOOD and OVP thresholds. Table 2 specifies the DACOUT voltage for the 32 combinations of open or short connections on the VID pins. The output voltage should not be adjusted while the converter is delivering power. Remove input power before changing the output voltage. Adjusting the output voltage during operation could toggle the PGOOD signal and exercise the overvoltage protection. The DAC function is a precision non-inverting summation amplifier shown in Figure 2. The resistor values shown are only approximations of the actual precision values used. Grounding any combination of the VID pins increases the DACOUT voltage. The 'open' circuit voltage on the VID pins is the band gap reference voltage, 1.26V.

Table 2. Output Voltage Table

PIN NAME					NOMINAL OUTPUT VOLTAGE	PIN NAME					NOMINAL OUTPUT VOLTAGE
VID4	VID3	VID2	VID1	VID0		VID4	VID3	VID2	VID1	VID0	
0	1	1	1	1	1.30	1	1	1	1	1	2.0
0	1	1	1	0	1.35	1	1	1	1	0	2.1
0	1	1	0	1	1.40	1	1	1	0	1	2.2
0	1	1	0	0	1.45	1	1	1	0	0	2.3
0	1	0	1	1	1.50	1	1	0	1	1	2.4
0	1	0	1	0	1.55	1	1	0	1	0	2.5
0	1	0	0	1	1.60	1	1	0	0	1	2.6
0	1	0	0	0	1.65	1	1	0	0	0	2.7
0	0	1	1	1	1.70	1	0	1	1	1	2.8
0	0	1	1	0	1.75	1	0	1	1	0	2.9
0	0	1	0	1	1.80	1	0	1	0	1	3.0
0	0	1	0	0	1.85	1	0	1	0	0	3.1
0	0	0	1	1	1.90	1	0	0	1	1	3.2
0	0	0	1	0	1.95	1	0	0	1	0	3.3
0	0	0	0	1	2.00	1	0	0	0	1	3.4
0	0	0	0	0	2.05	1	0	0	0	0	3.5

Note:

1. 0 = connected to GND or V_{SS}, 1 = OPEN

Absolute Maximum Ratings

Power Input Voltage, Vin	6V
Supply Voltage Vcc	13.5V
Vcc or I/O Voltage	Vcc+0.3V
ESD Classification	Class 2

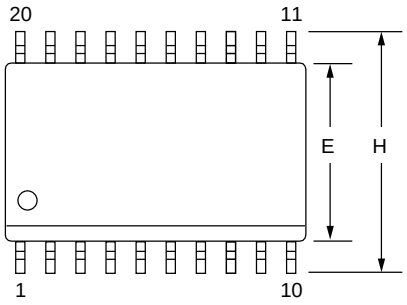
Package Dimensions

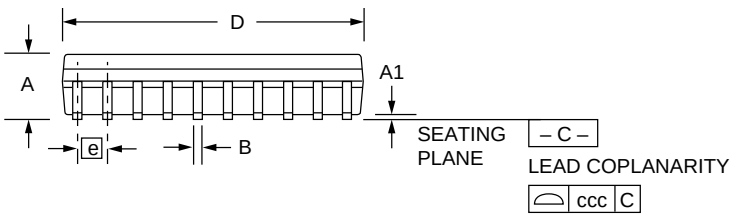
20-pin SOIC package

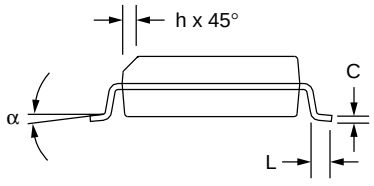
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.496	.512	12.60	13.00	2
E	.291	.299	7.40	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.029	0.25	0.75	
L	.016	.050	0.40	1.27	3
N	20		20		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Preliminary Information

Ordering Information

Product Number	Package
RC5056M	20 pin SOIC

Preliminary Information

RC5057

High Performance Programmable Synchronous DC-DC Controller for Low Voltage Microprocessors

Features

- Programmable output from 1.3V to 3.5V using an integrated 5-bit DAC
- Remote sense
- Active Droop
- 85% efficiency typical at full load
- Integrated Power Good and Enable/Soft Start functions
- Drives N-channel MOSFETs
- Overcurrent protection using MOSFET sensing
- 16 pin SOIC package
- Meets Intel Pentium II specifications using minimum number of external components

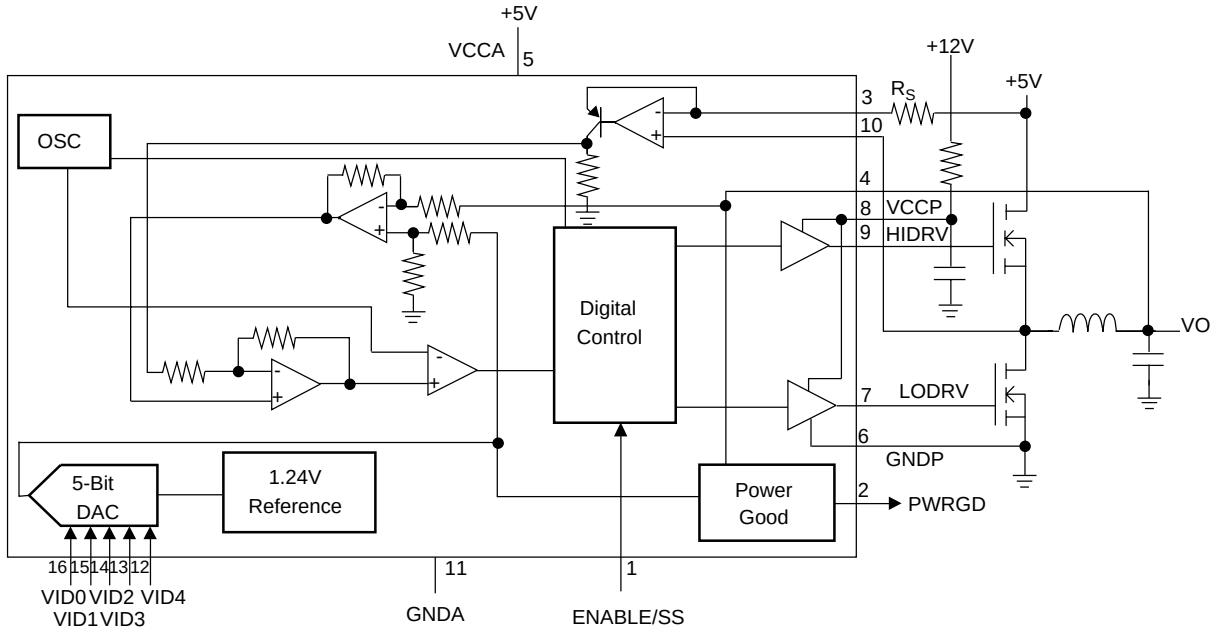
Applications

- Power supply for Pentium® II & III
- VRM for Pentium II & III processor
- Telecom line cards
- Routers, switches & hubs
- Programmable step-down power supply

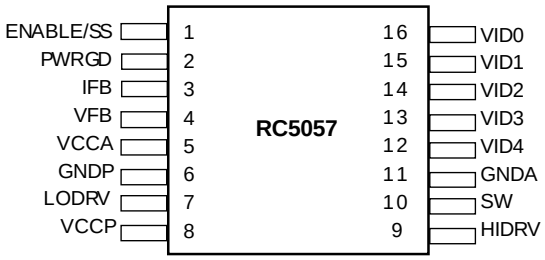
Description

The RC5057 is a synchronous mode DC-DC controller IC which provides a highly accurate, programmable output voltage for all Pentium II & III CPU applications and other high-performance processors. The RC5057 features remote voltage sensing, adjustable current limit, and active droop for optimal converter transient response. The RC5057 uses a 5-bit D/A converter to program the output voltage from 1.3V to 3.5V. The RC5057 uses a high level of integration to deliver load currents in excess of 16A from a 5V source with minimal external circuitry. Synchronous-mode operation offers optimum efficiency over the entire specified output voltage range. An on-board precision low TC reference achieves tight tolerance voltage regulation without expensive external components, while active droop permits exact tailoring of voltage for the most demanding load transients. The RC5057 also offers integrated functions including Power Good, Output Enable/Soft Start and current limiting, and is available in a 16 pin SOIC package.

Block Diagram



Pin Assignments



Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	ENABLE/SS	**Output Enable/Softstart.** A logic LOW on this pin will disable the output. An internal current source allows for open collector control. This pin also doubles as soft start.
2	PWRGD	**Power Good Flag.** An open collector output that will be logic LOW if the output voltage is not within ±12% of the nominal output voltage setpoint.
3	IFB	**Current Feedback.** Pin 3 is used in conjunction with pin 10, as the input for the current feedback control loop. Layout of these traces is critical to system performance. See Application Information for details.
4	VFB	**Voltage Feedback.** Pin 4 is used as the input for the voltage feedback control loop. See Application Information for details regarding correct layout.
5	VCCA	**Analog VCC.** Connect to system 5V supply and decouple with a 0.1µF ceramic capacitor.
6	GNDP	**Power Ground.** Return pin for high currents flowing in pin 8 (VCCP). Connect to a low impedance ground.
7	LODRV	**Low Side FET Driver.** Connect this pin to the gate of an N-channel MOSFET for synchronous operation. The trace from this pin to the MOSFET gate should be <0.5".
8	VCCP	**Power VCC.** For both high side and low side FET drivers. Connect to system 12V supply, and decouple with a 4.7µF tantalum and a 0.1µF ceramic capacitor.
9	HIDRV	**High Side FET Driver.** Connect this pin to the gate of an N-channel MOSFET. The trace from this pin to the MOSFET gate should be <0.5".
10	SW	**High side driver source and low side driver drain switching node.** Together with IFB pin allows FET sensing for current.
11	GNDA	**Analog Ground.** Return path for low power analog circuitry. This pin should be connected to a low impedance system ground plane to minimize ground loops.
12–16	VID0-4	**Voltage Identification Code Inputs.** These open collector/TTL compatible inputs will program the output voltage over the ranges specified in Table 2. Pull-up resistors are internal to the controller.

Absolute Maximum Ratings

Supply Voltages VCCA, VCCP to GND	13.5V
Supply Voltages (VCCP, Charge Pump)	18V
Voltage Identification Code Inputs, VID0-VID4	VCCA
Junction Temperature, T_J	150°C
Storage Temperature	-65 to 150°C
Lead Soldering Temperature, 10 seconds	300°C
Power Dissipation, P_D	750mW
Thermal Resistance Junction-to-case, Θ_{JC}	105°C/W

Recommended Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Voltage VCCA		4.75	5	5.25	V
Input Logic HIGH		2.0			V
Input Logic LOW				0.8	V
Ambient Operating Temperature		0		70	°C
Output Driver Supply, VCCP		11.4	12	13.2	V

Electrical Specifications (V_{CCA} = 5V, V_{CCP} = 12V, V_{OUT} = 2.0V, and T_A = +25°C using circuit in Figure 1, unless otherwise noted.)

The • denotes specifications which apply over the full operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
Output Voltage	See Table 1	•	1.3		3.5	V
Output Current				18		A
Initial Voltage Setpoint	I_{LOAD} = 0.8A, V_{OUT} = 2.400V V_{OUT} = 2.000V V_{OUT} = 1.550V		2.394 2.000 1.550	2.424 2.020 1.565	2.454 2.040 1.580	V V V
Output Temperature Drift	T_A = 0 to 70°C, V_{OUT} = 2.000V V_{OUT} = 1.550V	• •		+8 +6		mV mV
Line Regulation	V_{CCA} = 4.75V to 5.25V, V_{OUT} = 2.000V	•		±2		mV
Internal Droop[3]	V_{OUT} at I_{LOAD} = 0.8A to I_{max}		-44	-40	-36	mV
Output Ripple	20MHz BW, I_{LOAD} = I_{max}			11		mVpk
Total Output Variation, Steady State[1]	V_{OUT} = 2.000V V_{OUT} = 1.550V[3]	• •	1.940 1.480		2.070 1.590	V
Total Output Variation, Transient[2]	I_{LOAD} = 0.8A to I_{max},V_{OUT} = 2.000V V_{OUT} = 1.550V[3]	• •	1.900 1.480		2.100 1.590	V
Short Circuit Detect Current		•	45		60	µA
Efficiency	I_{LOAD} = I_{max}, V_{OUT} = 2.0V			85		%
Output Driver Rise & Fall Time	See Figure 4 for t_R and t_F			50		nsec
Output Driver Deadtime	See Figure 7 for t_{DT}			50		nsec
Oscillator Frequency		•	255	300	345	kHz
Duty Cycle			0		100	%
PWRGD Threshold	Logic HIGH Logic LOW	• •	93 88		107 112	$\%V_{out}$
V_{CCA} UVLO		•	3.74	4	4.26	V
V_{CCP} UVLO		•	7.65	8.5	9.35	V
V_{CCA} Supply Current				19		mA
V_{CCP} Supply Current[4]				40		mA
Soft Start Current		•	5	10	17	µA

Notes:

1. Steady State Voltage Regulation includes Initial Voltage Setpoint, Droop, Output Ripple and Output Temperature Drift and is measured at the converter's VFB sense point.
2. As measured at the converter's VFB sense point. For motherboard applications, the PCB layout should exhibit no more than 0.5mΩ trace resistance between the converter's output capacitors and the CPU. Remote sensing should be used for optimal performance.
3. Using the VFB pin for remote sensing of the converter's output at the load, the converter will be in compliance with Intel's VRM 8.4 specification of +50, -80mV. If Intel specifications on maximum plane resistance from the converter's output capacitors to the CPU are met, the specification of +40, -70mV at the capacitors will also be met.
4. Includes gate current.

Table 1. Output Voltage Programming Codes

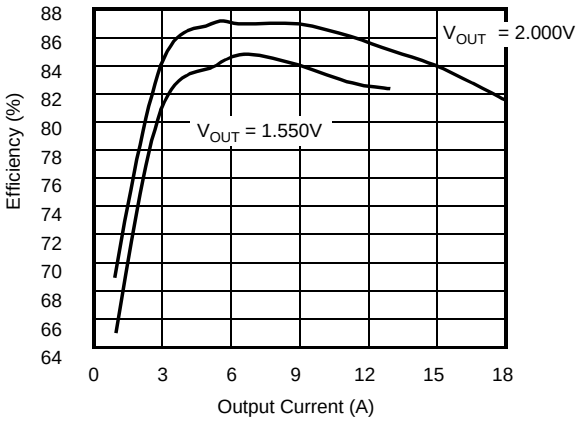
VID4	VID3	VID2	VID1	VID0	Nominal V_{OUT}
0	1	1	1	1	1.30V
0	1	1	1	0	1.35V
0	1	1	0	1	1.40V
0	1	1	0	0	1.45V
0	1	0	1	1	1.50V
0	1	0	1	0	1.55V
0	1	0	0	1	1.60V
0	1	0	0	0	1.65V
0	0	1	1	1	1.70V
0	0	1	1	0	1.75V
0	0	1	0	1	1.80V
0	0	1	0	0	1.85V
0	0	0	1	1	1.90V
0	0	0	1	0	1.95V
0	0	0	0	1	2.00V
0	0	0	0	0	2.05V
1	1	1	1	1	2.0V
1	1	1	1	0	2.1V
1	1	1	0	1	2.2V
1	1	1	0	0	2.3V
1	1	0	1	1	2.4V
1	1	0	1	0	2.5V
1	1	0	0	1	2.6V
1	1	0	0	0	2.7V
1	0	1	1	1	2.8V
1	0	1	1	0	2.9V
1	0	1	0	1	3.0V
1	0	1	0	0	3.1V
1	0	0	1	1	3.2V
1	0	0	1	0	3.3V
1	0	0	0	1	3.4V
1	0	0	0	0	3.5V

Note:

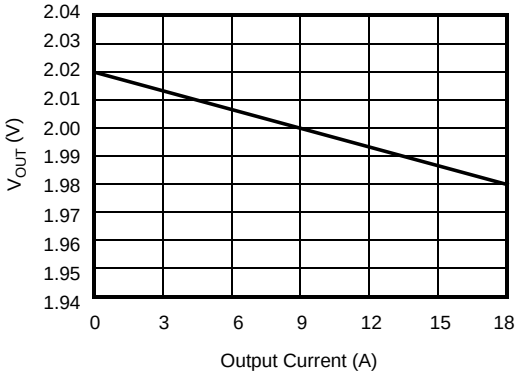
1. 0 = processor pin is tied to GND.
   1 = processor pin is open.

Typical Operating Characteristics (V_{CCA} = 5V, V_{CCP} = 12V, and T_A = +25°C using circuit in Figure 1, unless otherwise noted.)

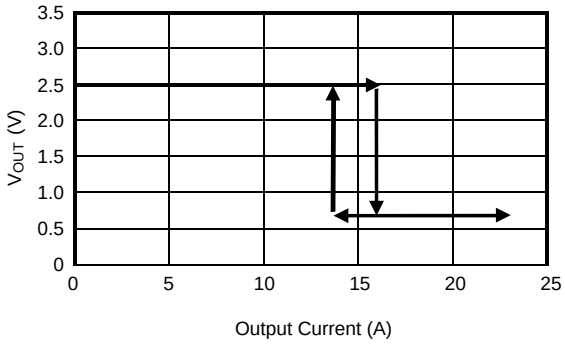
Efficiency vs. Output Current



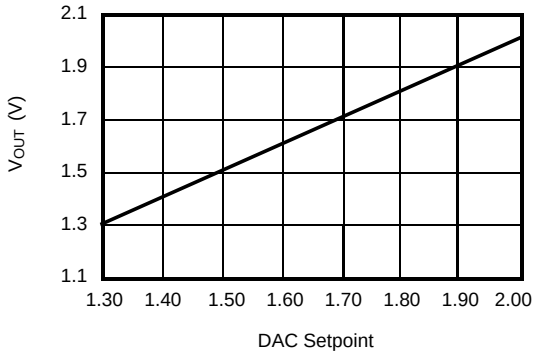
Droop, V_{OUT} = 2.0V



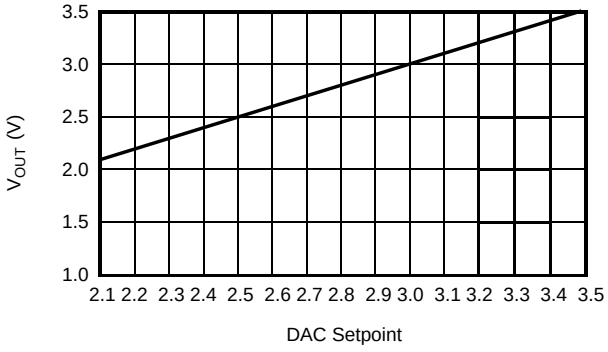
Output Voltage vs. Output Current



Output Programming, VID4 = 0

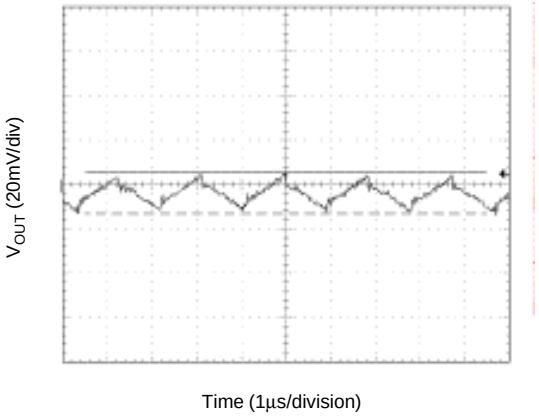


Output Programming, VID4 = 1

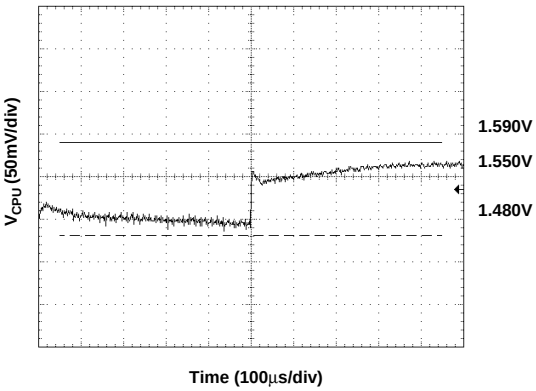


Typical Operating Characteristics (continued)

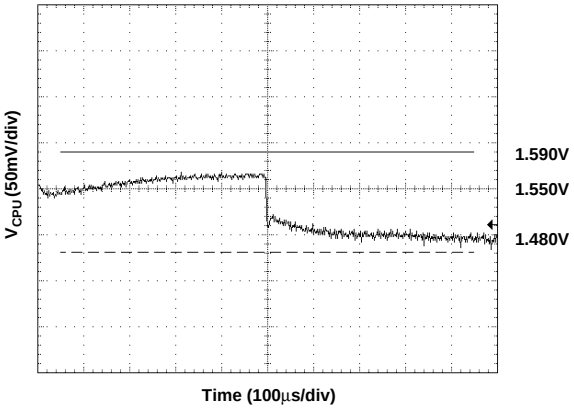
Output Ripple, 2.0V @ 18A



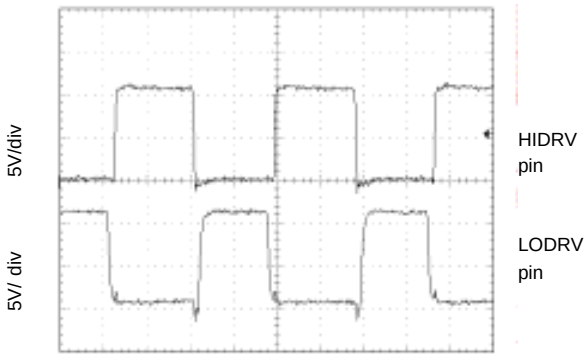
Transient Response, 12.5A to 0.5A



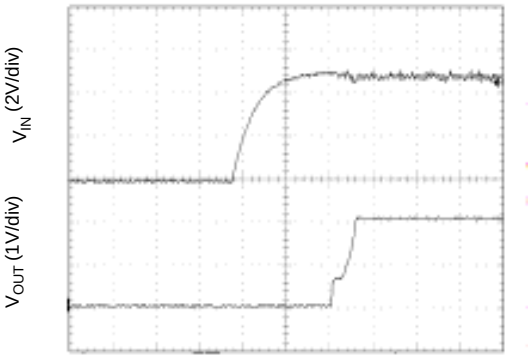
Transient Response, 0.5A to 12.5A



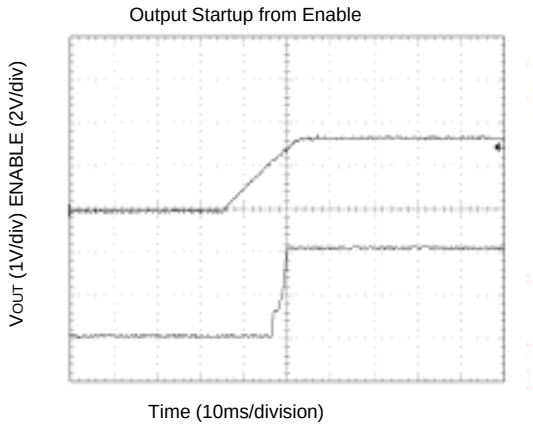
Switching Waveforms, 18A Load

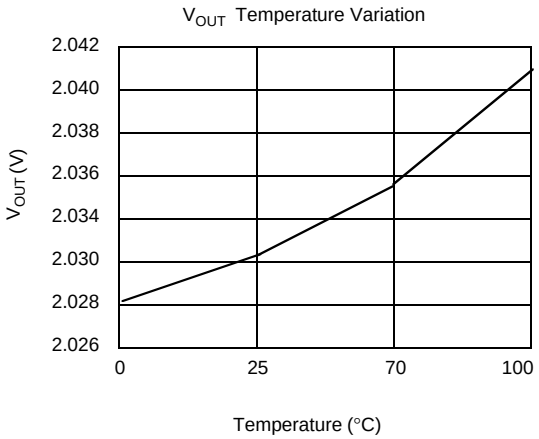


Output Startup, System Power-up



Typical Operating Characteristics (continued)





Application Circuit

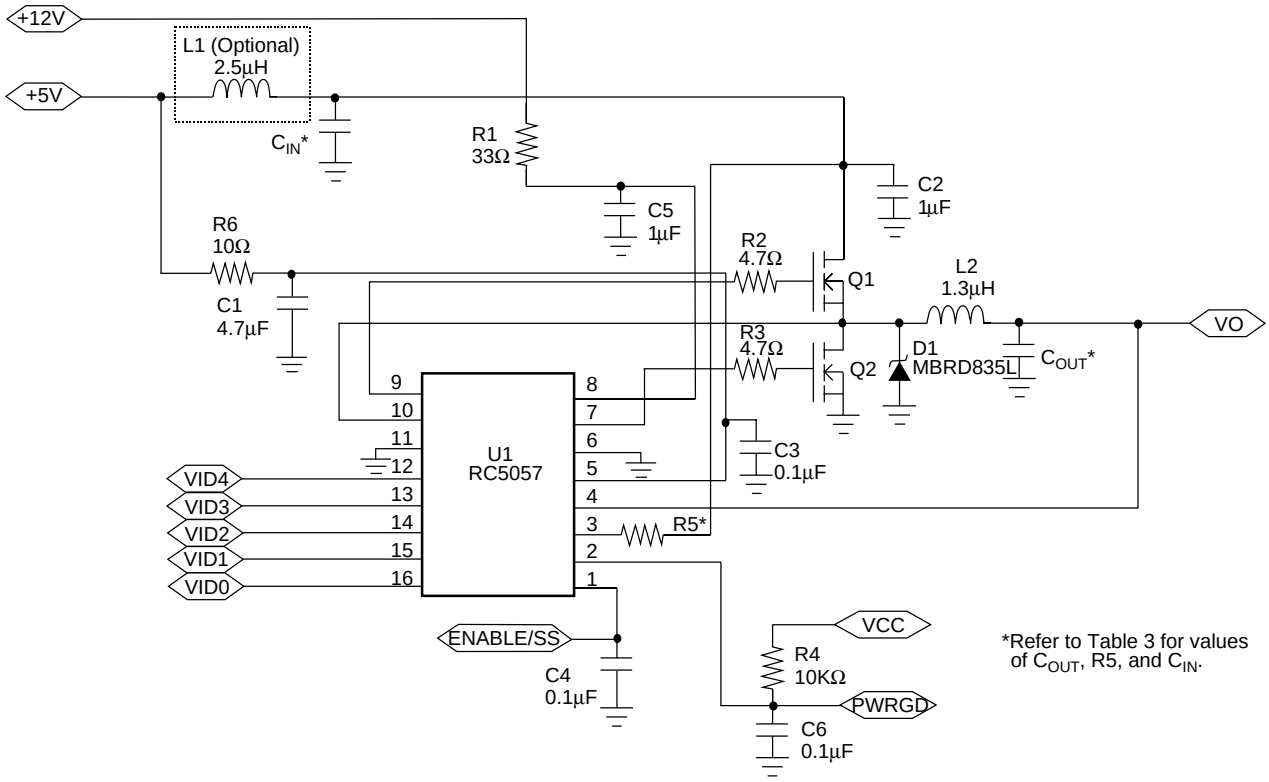


Figure 1. Application Circuit for Katmai, Mendocino, and Some Coppermine Processors
(*Worst Case Analyzed!* See Appendix for Details)

Table 2. RC5057 Application Bill of Materials for Intel Pentium II & III Processors
(Components based on Worst Case Analysis—See Appendix for Details)

Reference	Manufacturer Part #	Quantity	Description	Requirements/Comments
C1	AVX TAJB475M010R5	1	4.7µF, 10V Capacitor	
C2, C5	Panasonic ECU-V1C105ZFX	2	1µF, 16V Capacitor	
C3-4,6	Panasonic ECU-V1H104ZFX	3	100nF, 50V Capacitor	
C_{IN}	Sanyo 10MV1200GX	*	1200µF, 10V Electrolytic	I_{RMS} = 2A
C_{OUT}	Sanyo 6MV1500GX	*	1500µF, 6.3V Electrolytic	ESR ≤44mΩ
D1	Motorola MBRD835L	1	8A Schottky Diode	
L1	Any	Optional	2.5µH, 10A Inductor	DCR ~ 6mΩ See Note 1.
L2	Any	1	1.3µH, 20A Inductor	DCR ~ 2mΩ
Q1	Fairchild FDP6030L or FDB6030L	1	N-Channel MOSFET (TO-220 or TO-263)	$R_{DS(ON)}$ = 20mΩ @ V_{GS} = 4.5V See Note 2.
Q2	Fairchild FDP7030BL or FDB7030BL	1	N-Channel MOSFET (TO-220 or TO-263)	$R_{DS(ON)}$ = 10mΩ @ V_{GS} = 4.5V See Note 2.
R1	Any	1	33Ω	
R2-3	Any	2	4.7Ω	
R4	Any	1	10KΩ	
R5	Any	1	*	
R6	Any	1	10Ω	
U1	Fairchild RC5057M	1	DC/DC Controller	

*See Table 3.

Notes:

1. Inductor L1 is recommended to isolate the 5V input supply from noise generated by the MOSFET switching, and to comply with Intel dI/dt requirements. L1 may be omitted if desired.
2. For designs using the TO-220 MOSFETs, heatsinks with thermal resistance Θ_{SA} < 20°C/W should be used. For designs using the TO-263 MOSFETs, adequate copper area should be used. For details and a spreadsheet on MOSFET selections, refer to Applications Bulletin AB-8.

Table 3. Recommended Values for CPU-based Applications

Processor	Chipset	C_{IN}	C_{OUT}*	R5 (KΩ)
Coppermine	Whitney	3	4	8.45
Katmai	Camino	4	6	13.0
Mendocino	Whitney	4	5	11.3
Katmai	BX	5	6	11.8

*Output capacitance requirements depend critically on layout and processor type. Consult Application Bulletin AB-14 for details. See the Appendix to this datasheet for the method of calculation of these components. Pin 4 must be used to remote sense the voltage at the processor to achieve the specified performance.

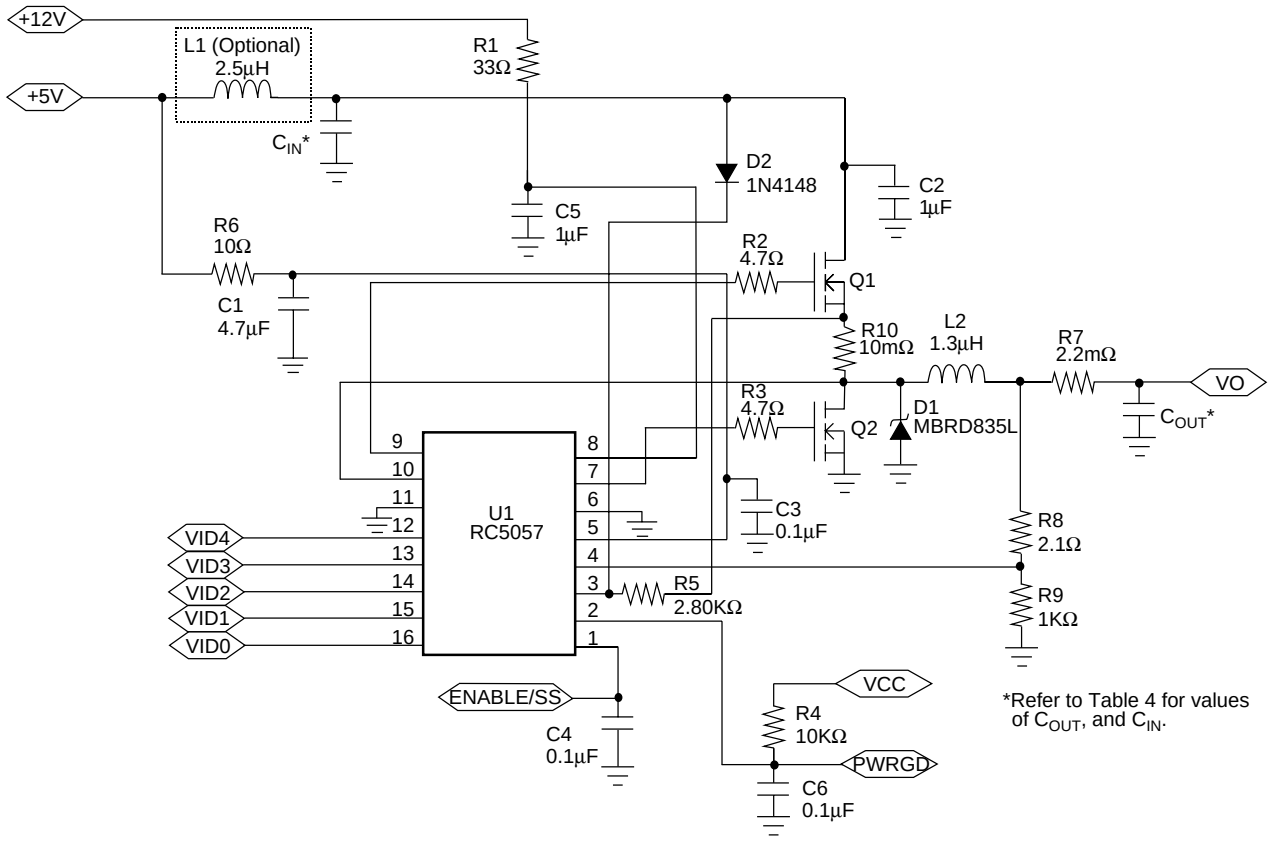


Figure 2. Application Circuit for Coppermine/Camino Processors
(*Worst Case Analyzed!* See Appendix for Details)

Table 4. RC5057 Application Bill of Materials for Coppermine/Camino Processors
(Components based on Worst Case Analysis—See Appendix for Details)

Reference	Manufacturer Part #	Quantity	Description	Requirements/Comments
C1	AVX TAJB475M010R5	1	4.7µF, 10V Capacitor	
C2, C5	Panasonic ECU-V1C105ZFX	2	1µF, 16V Capacitor	
C3-4,6	Panasonic ECU-V1H104ZFX	3	100nF, 50V Capacitor	
C_{IN}	Sanyo 10MV1200GX	3	1200µF, 10V Electrolytic	I_{RMS} = 2A
C_{OUT}	Sanyo 6MV1500GX	10	1500µF, 6.3V Electrolytic	ESR ≤ 44mΩ
D1	Motorola MBRD835L	1	8A Schottky Diode	
D2	Fairchild 1N4148	1	Signal Diode	
L1	Any	Optional	2.5µH, 10A Inductor	DCR ~ 6mΩ See Note 1.
L2	Any	1	1.3µH, 20A Inductor	DCR ~ 2mΩ
Q1	Fairchild FDP6030L or FDB6030L	1	N-Channel MOSFET (TO-220 or TO-263)	$R_{DS(ON)}$ = 20mΩ @ V_{GS} = 4.5V See Note 2.
Q2	Fairchild FDP7030BL or FDB7030BL	1	N-Channel MOSFET (TO-220 or TO-263)	$R_{DS(ON)}$ = 10mΩ @ V_{GS} = 4.5V See Note 2.
R1	Any	1	33Ω	
R2-3	Any	2	4.7Ω	
R4	Any	1	10KΩ	
R5	Any	1	2.80KΩ	
R6	Any	1	10Ω	
R7	N/A	1	1.8mΩ	PCB Trace Resistor
R8	Any	1	2.1Ω	
R9	Any	1	1KΩ	
R10	Dale WSL-2512-.01Ω	1	10mΩ, 1W Resistor	
U1	Fairchild RC5057M	1	DC/DC Controller	

Notes:

1. Inductor L1 is recommended to isolate the 5V input supply from noise generated by the MOSFET switching, and to comply with Intel dI/dt requirements. L1 may be omitted if desired.
2. For designs using the TO-220 MOSFETs, heatsinks with thermal resistance Θ_{SA} < 20°C/W should be used. For designs using the TO-263 MOSFETs, adequate copper area should be used. For details and a spreadsheet on MOSFET selections, refer to Applications Bulletin AB-8.

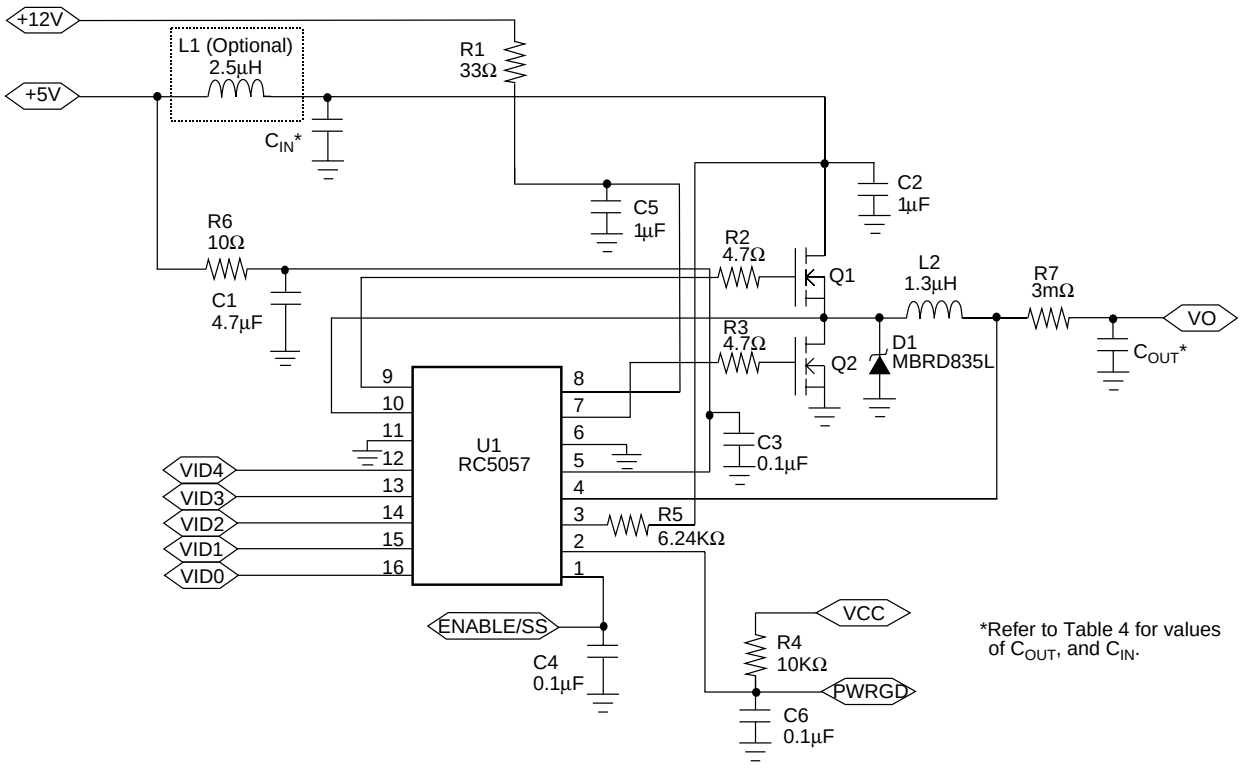


Figure 3. Application Circuit for Coppermine/Camino Processors
(*Typical Design*)

Table 5. RC5057 Application Bill of Materials for Coppermine/Camino Processors
(Typical Design)

Reference	Manufacturer Part #	Quantity	Description	Requirements/Comments
C1	AVX TAJB475M010R5	1	4.7µF, 10V Capacitor	
C2, C5	Panasonic ECU-V1C105ZFX	2	1µF, 16V Capacitor	
C3-4,6	Panasonic ECU-V1H104ZFX	3	100nF, 50V Capacitor	
C_{IN}	Sanyo 10MV1200GX	3	1200µF, 10V Electrolytic	I_{RMS} = 2A
C_{OUT}	Sanyo 6MV1500GX	8	1500µF, 6.3V Electrolytic	ESR ≤ 44mΩ
D1	Motorola MBRD835L	1	3A Schottky Diode	
L1	Any	Optional	2.5µH, 10A Inductor	DCR ~ 6mΩ See Note 1.
L2	Any	1	1.3µH, 20A Inductor	DCR ~ 2mΩ
Q1-2	Fairchild FDP6030L or FDB6030L	2	N-Channel MOSFET (TO-220 or TO-263)	$R_{DS(ON)}$ = 20mΩ @ VG_S = 4.5V See Note 2.
R1	Any	1	33Ω	
R2-3	Any	2	4.7Ω	
R4	Any	1	10KΩ	
R5	Any	1	6.24KΩ	
R6	Any	1	10Ω	
R7	N/A	1	3.0mΩ	PCB Trace Resistor
U1	Fairchild RC5057M	1	DC/DC Controller	

Notes:
1. Inductor L1 is recommended to isolate the 5V input supply from noise generated by the MOSFET switching, and to comply with Intel dI/dt requirements. L1 may be omitted if desired.
2. For designs using the TO-220 MOSFETs, heatsinks with thermal resistance Θ_{SA} < 20°C/W should be used. For designs using the TO-263 MOSFETs, adequate copper area should be used. For details and a spreadsheet on MOSFET selections, refer to Applications Bulletin AB-8.

Test Parameters

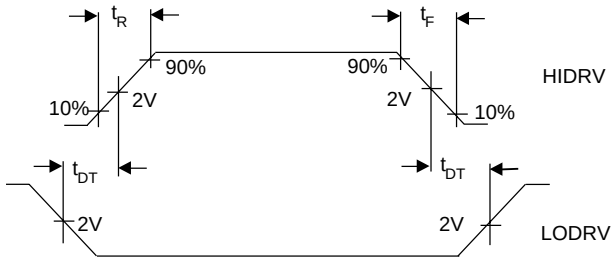


Figure 4. Output Drive Timing Diagram

Application Information

The RC5057 Controller

The RC5057 is a programmable synchronous DC-DC controller IC. When designed around the appropriate external components, the RC5057 can be configured to deliver more than 16A of output current, as appropriate for the Katmai and Coppermine and other processors. The RC5057 functions as a fixed frequency PWM step down regulator.

Main Control Loop

Refer to the RC5057 Block Diagram on page 1. The RC5057 implements “summing mode control”, which is different from both classical voltage-mode and current-mode control. It provides superior performance to either by allowing a large converter bandwidth over a wide range of output loads.

The control loop of the regulator contains two main sections: the analog control block and the digital control block. The analog section consists of signal conditioning amplifiers feeding into a comparator which provides the input to the digital control block. The signal conditioning section accepts input from the IFB (current feedback) and VFB (voltage feedback) pins and sets up two controlling signal paths. The first, the voltage control path, amplifies the difference between the VFB signal and the reference voltage from the DAC and presents the output to one of the summing amplifier inputs. The second, current control path, takes the difference between the IFB and SW pins when the high-side MOSFET is on, reproducing the voltage across the MOSFET and thus the input current; it presents the resulting signal to another input of the summing amplifier. These two signals are then summed together. This output is then presented to a comparator looking at the oscillator ramp, which provides the main PWM control signal to the digital control block.

The digital control block takes the analog comparator input and the main clock signal from the oscillator to provide the appropriate pulses to the HIDRV and LODRV output pins. These two outputs control the external power MOSFETs.

There is an additional comparator in the analog control section whose function is to set the point at which the RC5057 current limit comparator disables the output drive signals to the external power MOSFETs.

High Current Output Drivers

The RC5057 contains two identical high current output drivers that utilize high speed bipolar transistors in a push-pull configuration. The drivers’ power and ground are separated from the chip’s power and ground for switching noise immunity. The power supply pin, VCCP, is supplied from an external 12V source through a series resistor. The resulting voltage is sufficient to provide the gate to source drive to the external MOSFETs required in order to achieve a low $R_{DS,ON}$.

Internal Voltage Reference

The reference included in the RC5057 is a precision band-gap voltage reference. Its internal resistors are precisely trimmed to provide a near zero temperature coefficient (TC). Based on the reference is the output from an integrated 5-bit DAC. The DAC monitors the 5 voltage identification pins, VID0-4. When the VID4 pin is at logic HIGH, the DAC scales the reference voltage from 2.0V to 3.5V in 100mV increments. When VID4 is pulled LOW, the DAC scales the reference from 1.30V to 2.05V in 50mV increments. All VID codes are available, including those below 1.80V.

Power Good (PWRGD)

The RC5057 Power Good function is designed in accordance with the Pentium II & III DC-DC converter specifications and provides a continuous voltage monitor on the VFB pin. The circuit compares the VFB signal to the VREF voltage and outputs an active-low interrupt signal to the CPU should the power supply voltage deviate more than ±12% of its nominal setpoint. The output is guaranteed open-collector high when the power supply voltage is within ±7% of its nominal setpoint. The Power Good flag provides no other control function to the RC5057.

Output Enable/Soft Start (ENABLE/SS)

The RC5057 will accept an open collector/TTL signal for controlling the output voltage. The low state disables the output voltage. When disabled, the PWRGD output is in the low state.

Even if an enable is not required in the circuit, this pin should have attached a capacitor (typically 100nF) to softstart the switching.

Over-Voltage Protection

The RC5057 constantly monitors the output voltage for protection against over-voltage conditions. If the voltage at the VFB pin exceeds the selected program voltage, an over-voltage condition is assumed and the RC5057 disables the output drive signal to the external high-side MOSFET. The DC-DC converter returns to normal operation after the fault has been removed. If it is desired to have an active over-voltage protection circuit, the RC5052, which includes all the features of the RC5057, may be chosen instead of the RC5057.

Oscillator

The RC5057 oscillator section uses a fixed frequency of operation of 300KHz. If it is desired to adjust this frequency for reasons of efficiency or component size, the RC5052, which includes all of the features of the RC5057, may be chosen instead of the RC5057.

Design Considerations and Component Selection

Additional information on design and component selection may be found in Fairchild’s Application Note 57.

MOSFET Selection

This application requires N-channel Logic Level Enhancement Mode Field Effect Transistors. Desired characteristics are as follows:

- Low Static Drain-Source On-Resistance, $R_{DS,ON} < 20m\Omega$ (lower is better)
- Low gate drive voltage, $V_{GS} = 4.5V$ rated
- Power package with low Thermal Resistance
- Drain-Source voltage rating > 15V.

The on-resistance (RDS,ON) is the primary parameter for MOSFET selection. The on-resistance determines the power dissipation within the MOSFET and therefore significantly affects the efficiency of the DC-DC Converter. For details and a spreadsheet on MOSFET selection, refer to Applications Bulletin AB-8.

Inductor Selection

Choosing the value of the inductor is a tradeoff between allowable ripple voltage and required transient response. The system designer can choose any value within the allowed minimum to maximum range in order to either minimize ripple or maximize transient performance. The first order equation (close approximation) for minimum inductance is:

$$L_{min} = \frac{(V_{in} - V_{out})}{f} \times \frac{V_{out}}{V_{in}} \times \frac{ESR}{V_{ripple}}$$

where:

V_{in} = Input Power Supply

V_{out} = Output Voltage

f = DC/DC converter switching frequency

ESR = Equivalent series resistance of all output capacitors in parallel

V_{ripple} = Maximum peak to peak output ripple voltage budget.

The first order equation for maximum allowed inductance is:

$$L_{max} = 2C_0 \frac{(V_{in} - V_{out})\, D_m\, V_{tb}}{I_{pp}^2}$$

where:

C_o = The total output capacitance

I_{pp} = Maximum to minimum load transient current

V_{tb} = The output voltage tolerance budget allocated to load transient

D_m = Maximum duty cycle for the DC/DC converter (usually 95%).

Some margin should be maintained away from both Lmin and L_{max}. Adding margin by increasing L almost always adds expense since all the variables are predetermined by system performance except for C_o, which must be increased to increase L. Adding margin by decreasing L can be done by purchasing capacitors with lower ESR. The RC5057 provides significant cost savings for the newer CPU systems that typically run at high supply current.

RC5057 Short Circuit Current Characteristics

The RC5057 protects against output short circuit by turning off both the high-side and low-side MOSFETs and resetting softstart. The short circuit limit is set with the R_S resistor, as given by the formula

$$R_S = \frac{I_{SC} \times R_{DS,\,on}}{I_{Detect}}$$

with $I_{Detect} \approx 50\mu A$, I_{SC} the desired current limit, and $R_{DS,on}$ the high-side MOSFET's on resistance. Remember to make the R_S large enough to include the effects of initial tolerance and temperature variation on the MOSFET's $R_{DS,on}$. However, the value of R_S should be less than $10K\Omega$. If a greater value is necessary, a lower $R_{DS,on}$ MOSFET should be used instead. Alternately, use of a sense resistor in series with the source of the MOSFET, as shown in Figure 6, eliminates this source of inaccuracy in the current limit. Note the addition of the diode, which is necessary for proper operation of this circuit.

As an example, Figure 5 shows the typical characteristic of the DC-DC converter circuit with an FDB6030L high-side MOSFET ($R_{DS} = 20m\Omega$ maximum at 25°C * 1.25 at 75°C = $25m\Omega$) and a $8.2K\Omega$ R_S.

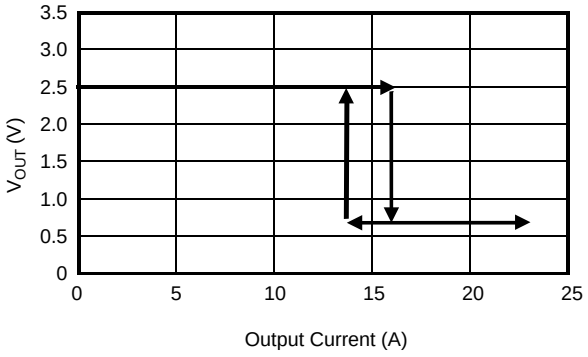


Figure 5. RC5057 Short Circuit Characteristic

The converter exhibits a normal load regulation characteristic until the voltage across the MOSFET exceeds the internal short circuit threshold of $50\mu A * 8.2K\Omega = 410mV$, which occurs at $410mV/25m\Omega = 16.4A$. (Note that this current limit level can be as high as $410mV/15m\Omega = 27A$, if the MOSFET

has typical $R_{DS,on}$ rather than maximum, and is at 25°C. This is the reason for using the external sense resistor.) At this point, the internal comparator trips and signals the controller to discharge the softstart capacitor. This causes a drastic reduction in the output voltage as the load regulation collapses into the short circuit control mode. With a 40mΩ output short, the voltage is reduced to 16.4A * 40mΩ = 650mV. The output voltage does not return to its nominal value until the output current is reduced to a value within the safe operating range for the DC-DC converter.

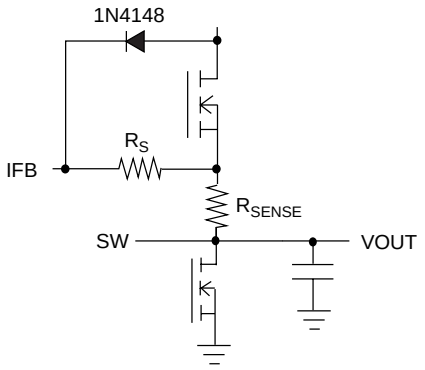


Figure 6. Precision Current Sensing

Schottky Diode Selection

The application circuit of Figure 1 shows a Schottky diode, D1, which is used as a free-wheeling diode to assure that the body-diode in Q2 does not conduct when the upper MOSFET is turning off and the lower MOSFET is turning on. It is undesirable for this diode to conduct because its high forward voltage drop and long reverse recovery time degrades efficiency, and so the Schottky provides a shunt path for the current. Since this time duration is very short, the selection criterion for the diode is that the forward voltage of the Schottky at the output current should be less than the forward voltage of the MOSFET's body diode.

Output Filter Capacitors

The output bulk capacitors of a converter help determine its output ripple voltage and its transient response. It has already been seen in the section on selecting an inductor that the ESR helps set the minimum inductance, and the capacitance value helps set the maximum inductance. For most converters, however, the number of capacitors required is determined by the transient response and the output ripple voltage, and these are determined by the ESR and not the capacitance value. That is, in order to achieve the necessary ESR to meet the transient and ripple requirements, the capacitance value required is already very large.

The most commonly used choice for output bulk capacitors is aluminum electrolytics, because of their low cost and low ESR. The only type of aluminum capacitor used should be those that have an ESR rated at 100kHz. Consult Application Bulletin AB-14 for detailed information on output capacitor selection.

The output capacitance should also include a number of small value ceramic capacitors placed as close as possible to the processor; 0.1µF and 0.01µF are recommended values.

Input Filter

The DC-DC converter design may include an input inductor between the system +5V supply and the converter input as shown in Figure 7. This inductor serves to isolate the +5V supply from the noise in the switching portion of the DC-DC converter, and to limit the inrush current into the input capacitors during power up. A value of 2.5µH is recommended.

It is necessary to have some low ESR aluminum electrolytic capacitors at the input to the converter. These capacitors deliver current when the high side MOSFET switches on. Figure 7 shows 3 x 1000µF, but the exact number required will vary with the speed and type of the processor. For the top speed Katmai and Coppermine, the capacitors should be rated to take 9A and 6A RMS of ripple current respectively. Capacitor ripple current rating is a function of temperature, and so the manufacturer should be contacted to find out the ripple current rating at the expected operational temperature. For details on the design of an input filter, refer to Applications Bulletin AB-15.

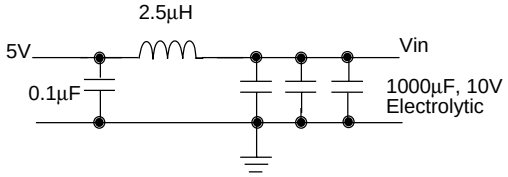


Figure 7. Input Filter

Active Droop

The RC5057 includes active droop: as the output current increases, the output voltage drops. This is done in order to allow maximum headroom for transient response of the converter. The current is sensed by measuring the voltage across the high-side MOSFET during its on time. Note that this makes the droop dependent on the temperature of the MOSFET. However, when the formula given for selecting R_S (current limit) is used, there is a maximum droop possible (-40mV), and when this value is reached, additional drop across the MOSFET will not cause any increase in droop—until current limit is reached.

Additional droop can be added to the active droop using a discrete resistor (typically a PCB trace) outside the control loop, as shown in Figure 2. This is typically only required for the most demanding applications, such as for the next generation Intel processor (tolerance = +40/-70mV), as shown in Figure 2.

PCB Layout Guidelines

- Placement of the MOSFETs relative to the RC5057 is critical. Place the MOSFETs such that the trace length of the HIDRV and LODRV pins of the RC5057 to the FET gates is minimized. A long lead length on these pins will cause high amounts of ringing due to the inductance of the trace and the gate capacitance of the FET. This noise radiates throughout the board, and, because it is switching at such a high voltage and frequency, it is very difficult to suppress.
- In general, all of the noisy switching lines should be kept away from the quiet analog section of the RC5057. That is, traces that connect to pins 7, 9, 10, and 8 (LODRV, HIDRV, SW and VCCP) should be kept far away from the traces that connect to pins 3 through 5, and pin 11.
- Place the 0.1µF decoupling capacitors as close to the RC5057 pins as possible. Extra lead length on these reduces their ability to suppress noise.
- Each VCC and GND pin should have its own via to the appropriate plane. This helps provide isolation between pins.
- Place the MOSFETs, inductor, and Schottky as close together as possible for the same reasons as in the first bullet above. Place the input bulk capacitors as close to the drains of the high side MOSFETs as possible. In addition, placement of a 0.1µF decoupling cap right on the drain of each high side MOSFET helps to suppress some of the high frequency switching noise on the input of the DC-DC converter.
- Place the output bulk capacitors as close to the CPU as possible to optimize their ability to supply instantaneous current to the load in the event of a current transient. Additional space between the output capacitors and the CPU will allow the parasitic resistance of the board traces to degrade the DC-DC converter's performance under severe load transient conditions, causing higher voltage deviation. For more detailed information regarding capacitor placement, refer to Application Bulletin AB-5.
- A PC Board Layout Checklist is available from Fairchild Applications. Ask for Application Bulletin AB-11.

PC Motherboard Sample Layout and Gerber File

A reference design for motherboard implementation of the RC5057 along with the PCAD layout Gerber file and silk screen can be obtained from our marketing department at 650-966-7624.

RC5057 Evaluation Board

Fairchild provides an evaluation board to verify the system level performance of the RC5057. It serves as a guide to performance expectations when using the supplied external components and PCB layout. Please call the marketing department at 650-966-7624 for an evaluation board.

Additional Information

For additional information contact Fairchild Semiconductor's Analog & Mixed Signal Products Group Marketing Department at 650-966-7624.

Appendix

Worst-Case Formulae for the Calculation of C_{out}, R5, and C_{in} (Circuit of Figure 1 Only)

The following formulae design the RC5057 for worst-case operation, including initial tolerance and temperature dependence of all of the IC parameters (initial setpoint, reference tolerance and tempco, active droop tolerance, current sensor gain), the initial tolerance and temperature dependence of the MOSFET, and the ESR of the capacitors. The following information must be provided:

V_{T+}, the value of the positive transient voltage limit;

$|V_{T-}|$, the absolute value of the negative transient voltage limit;

I_O, the maximum output current;

V_{nom}, the nominal output voltage;

V_{in}, the input voltage (typically 5V);

ESR, the ESR of the output caps, per cap (44mΩ for the Sanyo parts shown in this datasheet);

R_D, the on-resistance of the MOSFET (20mΩ for the FDB6030);

ΔR_D, the tolerance of the current sensor (usually about 67% for MOSFET sensing, including temperature).

I_{rms}, the rms current rating of the input caps (2A for the Sanyo parts shown in this datasheet).

$$C_{in} = \frac{IO * \sqrt{\frac{V_{nom}}{V_{in}} - \left(\frac{V_{nom}}{V_{in}}\right)^2}}{I_{rms}}$$

$$R5 = \frac{I_O * R_D * (1 + \Delta R_D) * 1.10}{50 * 10^{-6}}$$

Number of capacitors needed for C_{out} = the greater of:

$$X = \frac{ESR * I_O}{\left| V_{T-} \right|}$$

or

$$Y = \frac{ESR * I_O}{V_{T+} - 0.004 * V_{nom} + \frac{14400 * I_O * R_D}{18 * R5 * 1.1}}$$

Example: Suppose that the transient limits are ±134mV, current I is 14.2A, and the nominal voltage is 2.000V, using MOSFET current sensing and the usual caps. We have $V_{T+} = |V_{T-}| = 0.134$, $I_O = 14.2$, $V_{nom} = 2.000$, and $\Delta R_D = 0.67$. We calculate:

$$C_{in} = \frac{14.2 * \sqrt{\frac{2.000}{5} - \left(\frac{2.000}{5}\right)^2}}{2} = 3.47 \Rightarrow 4 \text{ caps}$$

$$R5 = \frac{14.2 * 0.020 * (1 + 0.67) * 1.10}{50 * 10^{-6}} = 10.4K\Omega$$

$$X = \frac{0.044 * 14.2}{0.134} = 4.66$$

$$Y = \frac{0.044 * 14.2}{0.134 - 0.004 * 2.000 + \frac{14400 * 14.2 * 0.020}{18 * 10400 * 1.1}} = 4.28$$

Since X > Y, we choose X, and round up to find we need 5 capacitors for C_{OUT}.

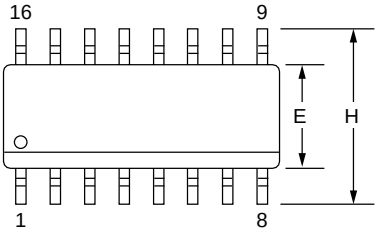
Mechanical Dimensions

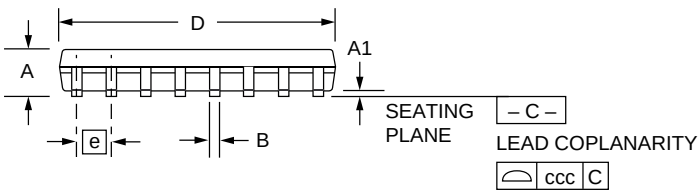
16 Lead SOIC

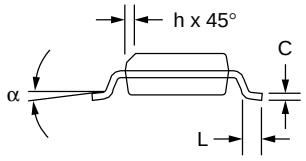
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.19	0.25	5
D	.386	.394	9.80	10.00	2
E	.150	.158	3.81	4.00	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.80	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	16		16		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Ordering Information

Product Number	Package
RC5057M	16 pin SOIC

RC5058

High Performance Programmable Synchronous DC-DC Controller for Multi-Voltage Platforms

Preliminary Specification

Features

- Programmable output for Vcore from 1.3V to 3.5V using an integrated 5-bit DAC
- Controls adjustable linears for Vagp (selectable 1.5V/3.3V), Vclock (2.5V), and Vtt (1.5V) or Vnorthbridge (1.8V)
- Meets VRM specification with as few as 5 capacitors
- Meets 1.550V +40/-70mV over initial tolerance, temperature and transients
- Remote sense
- Programmable Active Droop™ (Voltage Positioning)
- Drives N-Channel MOSFETs
- Overcurrent protection using MOSFET sensing
- 85% efficiency typical at full load
- Integrated Power Good and Enable/Soft Start functions
- 24 pin SOIC package

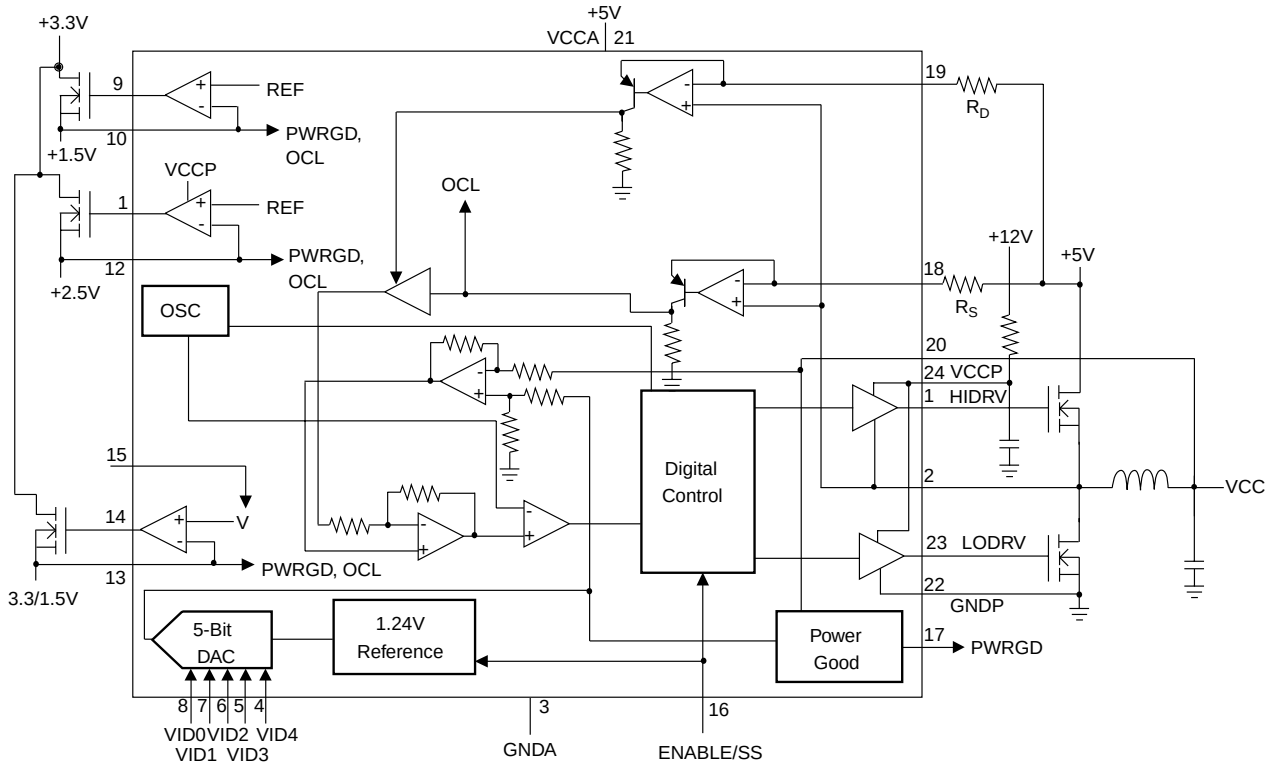
Applications

- Power supply for Pentium® III Camino Platform
- Power supply for Pentium III Whitney Platform
- VRM for Pentium III processor
- Programmable multi-output power supply

Description

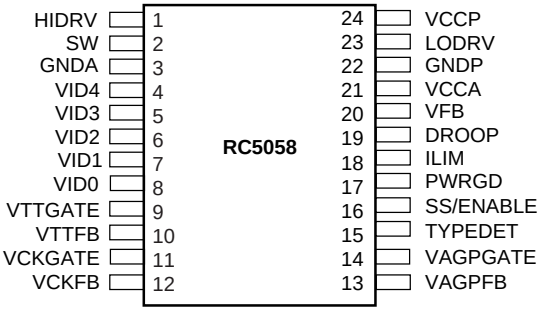
The RC5058 is a synchronous mode DC-DC controller IC which provides a highly accurate, programmable set of output voltages for multi-voltage platforms such as the Intel Camino, and provides a complete solution for the Intel Whitney and other high-performance processors. The RC5058 features remote voltage sensing, independently adjustable current limit, and a proprietary Programmable Active Droop™ for optimal converter transient response. The RC5058 uses a 5-bit D/A converter to program the output voltage from 1.3V to 3.5V. The RC5058 uses a high level of integration to deliver load currents in excess

Block Diagram



of 16A from a 5V source with minimal external circuitry. Synchronous-mode operation offers optimum efficiency over the entire specified output voltage range. An on-board precision low TC reference achieves tight tolerance voltage regulation without expensive external components, while Programmable Active Droop™ permits exact tailoring of voltage for the most demanding load transients. The RC5058 includes linear regulator controllers for Vtt termination (1.5V), Vclock (2.5V), and Vnorthbridge (1.8V) or Vagp (selectable 1.5V/3.3V), each adjustable with an external divider. The RC5058 also offers integrated functions including Power Good, Output Enable/Soft Start and current limiting, and is available in a 24 pin SOIC package.

Pin Assignments



Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	HIDRV	**High Side FET Driver.** Connect this pin through a resistor to the gate of an N-channel MOSFET. The trace from this pin to the MOSFET gate should be <0.5".
2	SW	**High side Driver Source and Low side Driver Drain Switching Node.** Together with DROOP and ILIM pins allows FET sensing for Vcc current.
3	GNDA	**Analog Ground.** Return path for low power analog circuitry. This pin should be connected to a low impedance system ground plane to minimize ground loops.
4-8	VID0-4	**Voltage Identification Code Inputs.** These open collector/TTL compatible inputs will program the output voltage over the ranges specified in Table 2. Pull-up resistors are internal to the controller.
9	VTTGATE	**Gate Driver for VTT Transistor.** For 1.5V output.
10	VTTFB	**Voltage Feedback for VTT.**
11	VCKGATE	**Gate Driver for VCK Transistor.** For 2.5V output.
12	VCKFB	**Voltage Feedback for VCK.**
13	VAGPFB	**Voltage Feedback for VAGP.**
14	VAGPGATE	**Gate Driver for VAGP Transistor.** For 3.3/1.5V output.
15	TYPEDET	**Type Detect.** Sets 3.3V or 1.5V for AGP.
16	ENABLE/SS	**Output Enable.** A logic LOW on this pin will disable all outputs. An internal current source allows for open collector control. This pin also doubles as soft start for all outputs.
17	PWRGD	**Power Good Flag.** An open collector output that will be logic LOW if any output voltage is not within ±12% of the nominal output voltage setpoint.
18	ILIM	**Vcc Current Feedback.** Pin 18 is used in conjunction with pin 2 as the input for the Vcc current feedback control loop. Layout of these traces is critical to system performance. See Application Information for details.
19	DROOP	**Droop set.** Use this pin to set magnitude of active droop.
20	VFB	**Vcc Voltage Feedback.** Pin 20 is used as the input for the Vcc voltage feedback control loop. See Application Information for details regarding correct layout.
21	VCCA	**Analog VCC.** Connect to system 5V supply and decouple with a 0.1µF ceramic capacitor.
22	GNDP	**Power Ground.** Return pin for high currents flowing in pin 24 (VCCP).
23	LODRV	**Vcc Low Side FET Driver.** Connect this pin through a resistor to the gate of an N-channel MOSFET for synchronous operation. The trace from this pin to the MOSFET gate should be <0.5".
24	VCCP	**Power VCC.** For all FET drivers. Connect to system 12V supply through a 33Ω, and decouple with a 1µF ceramic capacitor.

Preliminary Specification

Absolute Maximum Ratings

Supply Voltages VCCA, VCCP to GND	13.5V
Voltage Identification Code Inputs, VID0-VID4	VCCA
All Other Pins	13.5V
Junction Temperature, T_J	150°C
Storage Temperature	-65 to 150°C
Lead Soldering Temperature, 10 seconds	300°C
Thermal Resistance Junction-to-ambient, Θ_{JA}[1]	75°C/W

Note:

1. Component mounted on demo board in free air.

Recommended Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Voltage VCCA		4.75	5	5.25	V
Input Logic HIGH		2.0			V
Input Logic LOW				0.8	V
Ambient Operating Temperature		0		70	°C
Output Driver Supply, VCCP		10.8	12	13.2	V

Electrical Specifications

(V_{CCA} = 5V, V_{CCP} = 12V, V_{OUT} = 2.0V, and T_A = +25°C using circuit in Figure 1 unless otherwise noted.)
The • denotes specifications which apply over the full operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
VCC Regulator						
Output Voltage	See Table 1	•	1.3		3.5	V
Output Current				18		A
Initial Voltage Setpoint	I_{LOAD} = 0.8A, V_{OUT} = 2.400V V_{OUT} = 2.000V V_{OUT} = 1.550V		2.397 2.000 1.550	2.424 2.020 1.565	2.454 2.040 1.580	V V V
Output Temperature Drift	T_A = 0 to 70°C, V_{OUT} = 2.000V V_{OUT} = 1.550V	• •		+8 +6		mV mV
Line Regulation	V_{IN} = 4.75V to 5.25V	•		-4		mV/V
Internal Droop Impedance	I_{LOAD} = 0.8A to 12.5A		13.0	14.4	15.8	KΩ
Maximum Droop				60		mV
Output Ripple	20MHz BW, I_{LOAD} = 18A			11		mVpk
Total Output Variation, Steady State[1]	V_{OUT} = 2.000V V_{OUT} = 1.550V[3]	• •	1.940 1.480		2.070 1.590	V
Total Output Variation, Transient[2]	I_{LOAD} = 0.8A to 18A, V_{OUT} = 2.000V V_{OUT} = 1.550V[3]	• •	1.900 1.480		2.100 1.590	V
Short Circuit Detect Current		•	45	50	60	µA
Efficiency	I_{LOAD} = 18A, V_{OUT} = 2.0V			85		%
Output Driver Rise & Fall Time	See Figure 3			50		nsec
Output Driver Deadtime	See Figure 3			50		nsec
Duty Cycle			0		100	%

Preliminary Specification

Electrical Specifications (Continued)

(V_{CCA} = 5V, V_{CCP} = 12V, V_{OUT} = 2.0V, and T_A = +25°C using circuit in Figure 1 unless otherwise noted.)
The • denotes specifications which apply over the full operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
5V UVLO		•	3.74	4	4.26	V
12V UVLO		•	7.65	8.5	9.35	V
Soft Start Current		•	5	10	17	µA
VTT Linear Regulator						
Output Voltage	$I_{LOAD} \leq 2A$	•	1.425	1.5	1.575	V
Under Voltage Trip Level	Over Current			80		$\%V_O$
VCLK Linear Regulator						
Output Voltage	$I_{LOAD} \leq 2A$	•	2.375	2.5	2.625	V
Under Voltage Trip Level	Over Current			80		$\%V_O$
VAGP Linear Regulator						
Output Voltage	$I_{LOAD} \leq 2A$, TYPEDET=0V	•	1.425	1.5	1.575	V
Output Voltage	$I_{LOAD} \leq 2A$, TYPEDET=OPEN	•	3.135	3.3	3.465	V
Under Voltage Trip Level	Over Current			80		$\%V_O$
Common Functions						
Oscillator Frequency		•	255	310	345	kHz
PWRGD Threshold	Logic HIGH, All Outputs Logic LOW, Any Output	• •	93 88		107 112	$\%V_{OUT}$
Linear Regulator Under Voltage Delay Time	Over Current			30		µsec

Notes:

1. Steady State Voltage Regulation includes Initial Voltage Setpoint, Droop, Output Ripple and Output Temperature Drift and is measured at the converter's VFB sense point.
2. As measured at the converter's VFB sense point. For motherboard applications, the PCB layout should exhibit no more than 0.5mΩ trace resistance between the converter's output capacitors and the CPU. Remote sensing should be used for optimal performance.
3. Using the VFB pin for remote sensing of the converter's output at the load, the converter will be in compliance with Intel's VRM 8.4 specification of +50, –80mV. If Intel specifications on maximum plane resistance from the converter's output capacitors to the CPU are met, the specification of +40, –70mV at the capacitors will also be met.

Table 1. Output Voltage Programming Codes

VID4	VID3	VID2	VID1	VID0	Nominal V_{OUT}
0	1	1	1	1	1.30V
0	1	1	1	0	1.35V
0	1	1	0	1	1.40V
0	1	1	0	0	1.45V
0	1	0	1	1	1.50V
0	1	0	1	0	1.55V
0	1	0	0	1	1.60V
0	1	0	0	0	1.65V
0	0	1	1	1	1.70V
0	0	1	1	0	1.75V
0	0	1	0	1	1.80V
0	0	1	0	0	1.85V
0	0	0	1	1	1.90V
0	0	0	1	0	1.95V
0	0	0	0	1	2.00V
0	0	0	0	0	2.05V
1	1	1	1	1	2.0V
1	1	1	1	0	2.1V
1	1	1	0	1	2.2V
1	1	1	0	0	2.3V
1	1	0	1	1	2.4V
1	1	0	1	0	2.5V
1	1	0	0	1	2.6V
1	1	0	0	0	2.7V
1	0	1	1	1	2.8V
1	0	1	1	0	2.9V
1	0	1	0	1	3.0V
1	0	1	0	0	3.1V
1	0	0	1	1	3.2V
1	0	0	1	0	3.3V
1	0	0	0	1	3.4V
1	0	0	0	0	3.5V

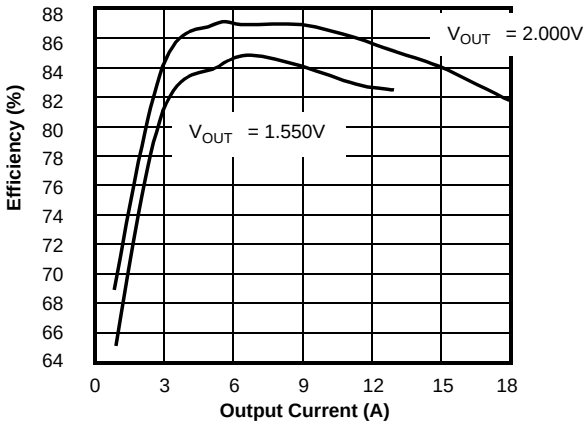
Note:

1. 0 = processor pin is tied to GND.
   1 = processor pin is open.

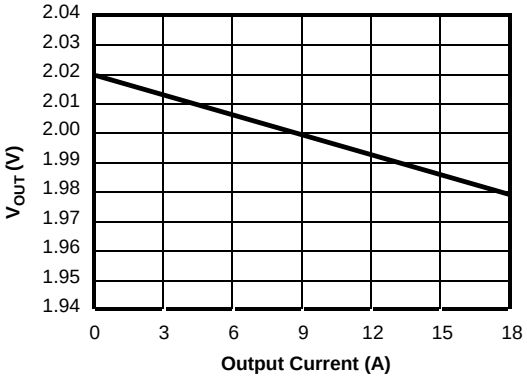
Typical Operating Characteristics

(V_{CCA} = 5V, V_{CCP} = 12V, and T_A = +25°C using circuits in Figure 1, unless otherwise noted.)

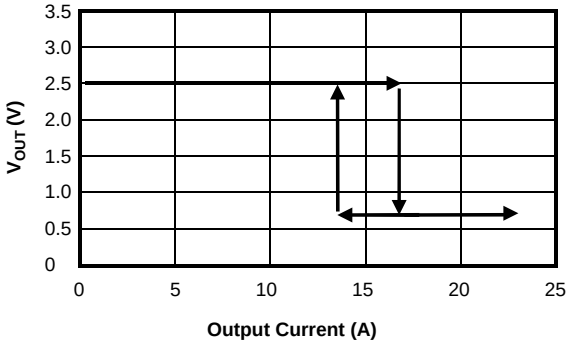
V_{CPU} Efficiency vs. Output Current



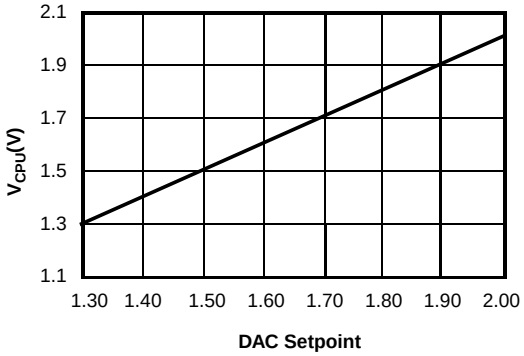
Droop, V_{CPU} = 2.0V, R_D = 8K Ω



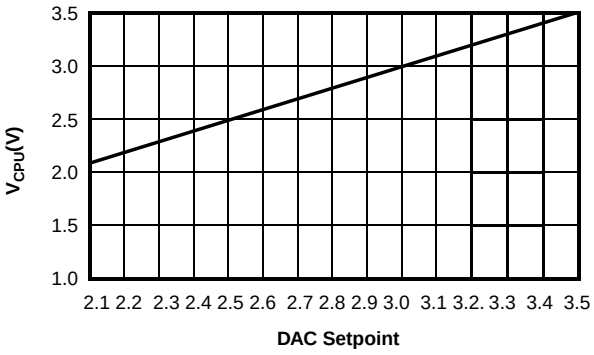
CPU Output Voltage vs. Output Current



Output Programming, VID4 = 0



Output Programming, VID4 = 1



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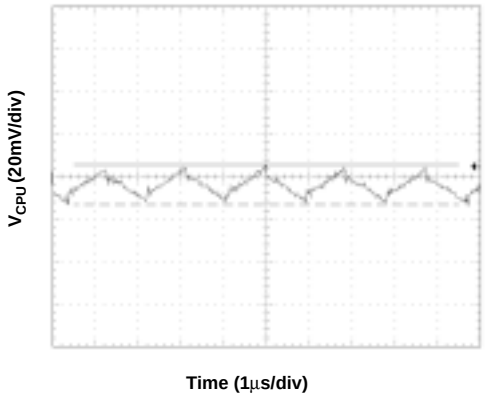
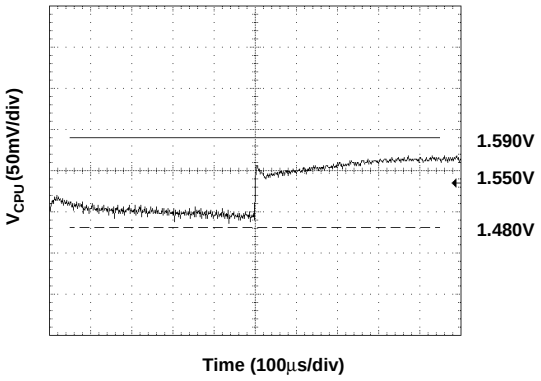
Typical Operating Characteristics (continued)

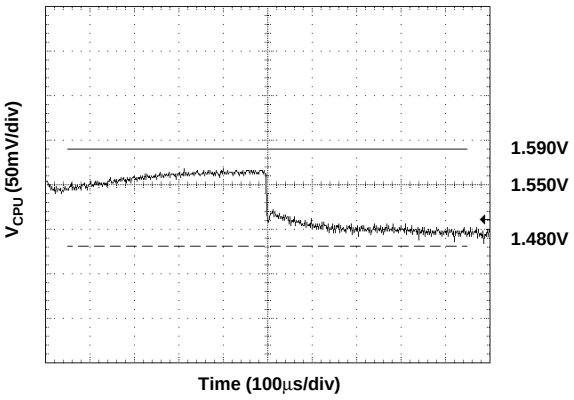
Output Ripple, 2.0V @ 18A



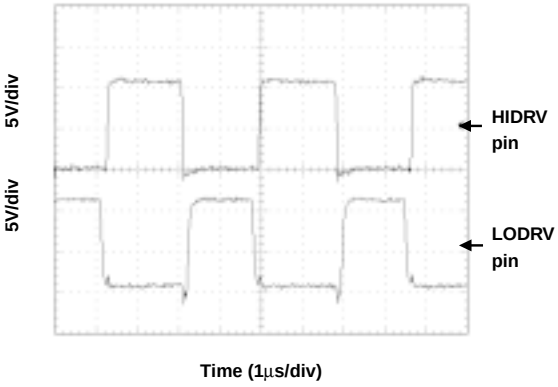
Transient Response, 12.5A to 0.5A



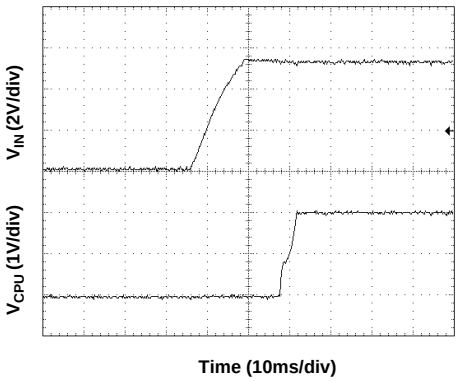
Transient Response, 0.5A to 12.5A



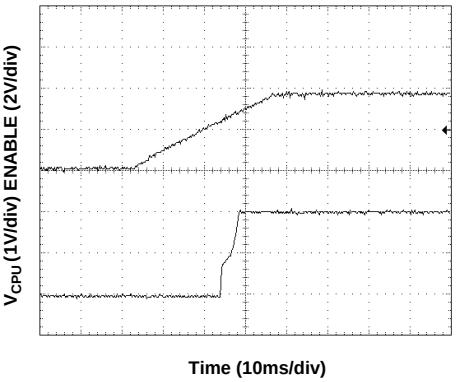
Switching Waveforms, 18A Load



Output Startup, System Power-up

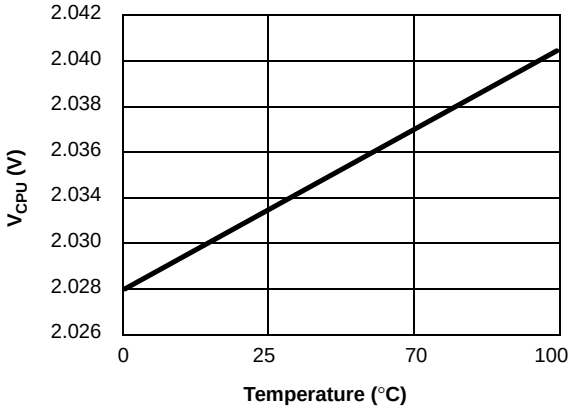


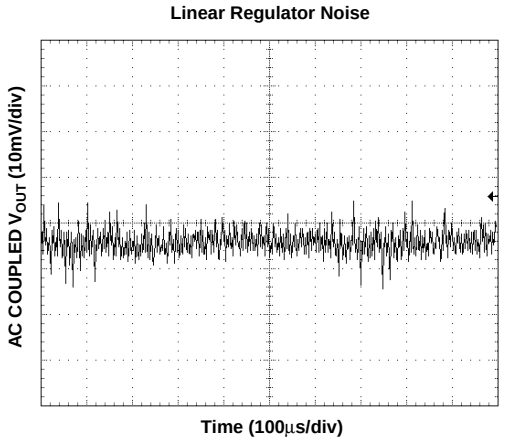
Output Startup from Enable



Preliminary Specification

Typical Operating Characteristics (continued)





Application Circuit

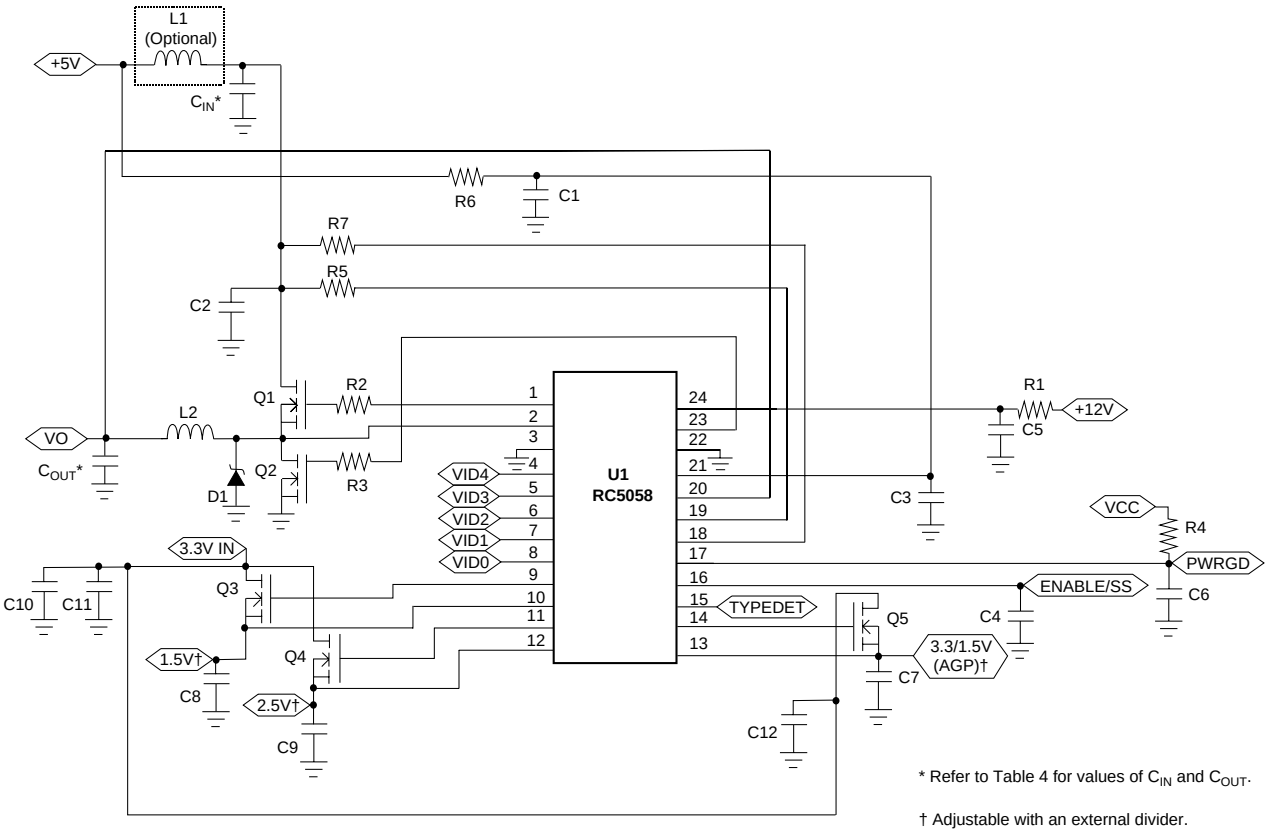


Figure 1. Application Circuit for Katmai/Camino/BX/ZX Motherboards
(Worst Case Analyzed! See Appendix for Details*)*

Preliminary Specification

Table 2. RC5058 Application Bill of Materials for Intel Katmai/Camino/BX/ZX Motherboards

(Components based on Worst Case Analysis—See Appendix for Details)

Reference	Manufacturer Part #	Quantity	Description	Requirements/Comments
C1	AVX TAJB475M010R5	1	4.7µF, 10V Capacitor	
C2, C5	Panasonic ECU-V1C105ZFX	2	1µF, 16V Capacitor	
C3-4,C6	Panasonic ECU-V1H104ZFX	3	100nF, 50V Capacitor	
C7-9	Sanyo 6MV1000FA	3	1000µF, 6.3V Electrolytic	
C10-12	Any	3	22µF, 6.3V Capacitor	Low ESR
C_{IN}	Sanyo 10MV1200GX	*	1200µF, 10V Electrolytic	I_{RMS} = 2A
C_{OUT}	Sanyo 6MV1500GX	*	1500µF, 6.3V Electrolytic	ESR ≤ 44mΩ
D1	Motorola MBRD835L	1	8A Schottky Diode	
L1	Any	Optional	2.5µH, 8A Inductor	DCR ~ 10mΩ See Note 1.
L2	Any	1	1.3µH, 20A Inductor	DCR ~ 2mΩ
Q1	Fairchild FDB6030L	1	N-Channel MOSFET	$R_{DS(ON)}$ = 20mΩ @ V_{GS} = 4.5V See Note 2.
Q2	Fairchild FDB7030BL	1	N-Channel MOSFET	$R_{DS(ON)}$ = 10mΩ @ V_{GS} = 4.5V See Note 2.
Q3-5	Fairchild FDB4030L	3	N-Channel MOSFET	
R1	Any	1	33Ω	
R2-3	Any	2	4.7Ω	
R4	Any	1	10KΩ	
R5	Any	1	*	
R6	Any	1	10Ω	
R7	Any	1	*	
U1	Fairchild RC5058M	1	DC/DC Controller	

Notes:

1. Inductor L1 is recommended to isolate the 5V input supply from noise generated by the MOSFET switching, and to comply with Intel dI/dt requirements. L1 may be omitted if desired.
2. For 17.4A designs using the TO-220 MOSFETs, heatsinks with thermal resistance Θ_{SA} < 20°C/Ω should be used. For designs using the TO-263 MOSFETs, adequate copper area should be used. For details and a spreadsheet on MOSFET selections, refer to Applications Bulletins AB-8 and AB-15.

*Refer to table 4 for values.

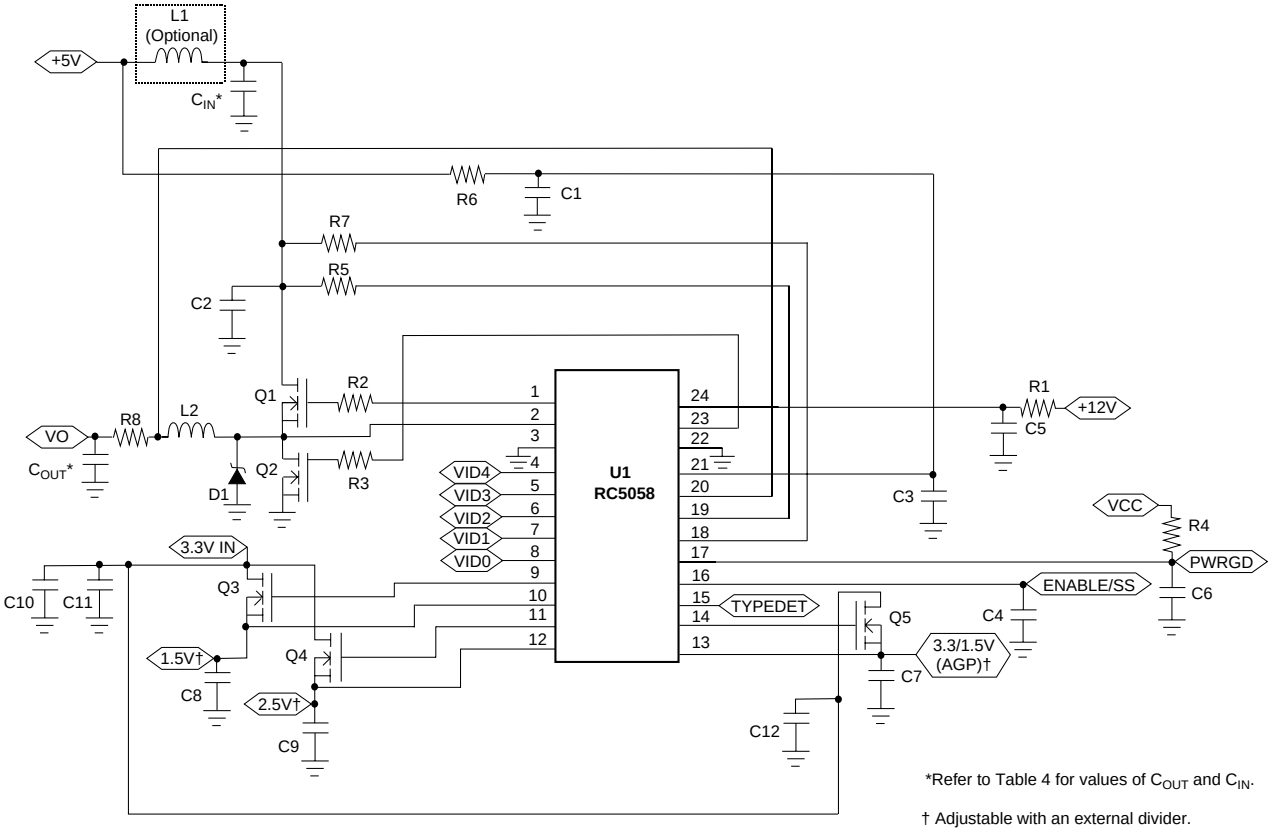


Figure 2. Application Circuit for Coppermine/Camino Motherboards
(Typical Design)

Table 3. RC5058 Application Bill of Materials for Intel Coppermine/Camino Motherboards
(Typical Design)

Reference	Manufacturer Part #	Quantity	Description	Requirements/Comments
C1	AVX TAJB475M010R5	1	4.7µF, 10V Capacitor	
C2, C5	Panasonic ECU-V1C105ZFX	2	1µF, 16V Capacitor	
C3-4,C6	Panasonic ECU-V1H104ZFX	3	100nF, 50V Capacitor	
C7-9	Sanyo 6MV1000FA	3	1000µF, 6.3V Electrolytic	
C10-12	Any	3	22µF, 6.3V Capacitor	Low ESR
C_{IN}	Sanyo 10MV1200GX	3	1200µF, 10V Electrolytic	I_{RMS} = 2A
C_{OUT}	Sanyo 6MV1500GX	12	1500µF, 6.3V Electrolytic	ESR ≤ 44mΩ
D1	Motorola MBRD835L	1	8A Schottky Diode	
L1	Any	Optional	2.5µH, 5A Inductor	DCR ~ 10mΩ See Note 1.
L2	Any	1	1.3µH, 15A Inductor	DCR ~ 3mΩ
Q1	Fairchild FDB6030L	1	N-Channel MOSFET	$R_{DS(ON)}$ = 20mΩ @ V_{GS} = 4.5V See Note 2.
Q2	Fairchild FDB7030BL	1	N-Channel MOSFET	$R_{DS(ON)}$ = 10mΩ @ V_{GS} = 4.5V See Note 2.
Q3-5	Fairchild FDB4030L	3	N-Channel MOSFET	
R1	Any	1	33Ω	
R2-3	Any	2	4.7Ω	
R4	Any	1	10KΩ	
R5, R7	Any	2	6.24KΩ	
R6	Any	1	10Ω	
R8	N/A	1	3.0mΩ	PCB Trace Resistor
U1	Fairchild RC5058M	1	DC/DC Controller	

Notes:

1. Inductor L1 is recommended to isolate the 5V input supply from noise generated by the MOSFET switching, and to comply with Intel dI/dt requirements. L1 may be omitted if desired.
2. For 12.5A designs using the TO-220 MOSFETs, heatsinks with thermal resistance Θ_{SA} < 20°C/Ω should be used. For designs using the TO-263 MOSFETs, adequate copper area should be used. For details and a spreadsheet on MOSFET selections, refer to Applications Bulletins AB-8 and AB-15.

Application Circuit Summary

Table 4 summarizes the worst-case design schematics presented in this section. The basic choices are: A) The processor, B) the chipset used, and C) the use or not of a sense resistor. Depending on board layout and component selection, it may be possible to use fewer output capacitors than shown here. For configurations not shown in this datasheet, consult the Appendix for selection of component values.

Table 4. Recommended Values for CPU-based Applications

Processor	Chipset	C_{IN}	C_{OUT}*	R5, R7 (KΩ)
Coppermine	Whitney	3	4	8.45
Katmai	Camino	4	6	13.0
Mendocino	Whitney	4	5	11.3
Katmai	BX	5	6	11.8

*Output capacitance requirements depend critically on layout and processor type. Consult Application Bulletin AB-14 for details. See the Appendix to this datasheet for the method of calculation of these components. Pin 4 must be used to remote sense the voltage at the processor to achieve the specified performance.

Test Parameters

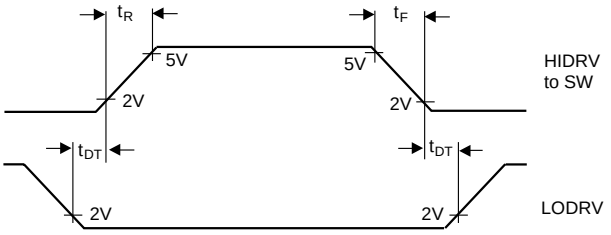


Figure 3. Ouput Drive Timing Diagram

Application Information

The RC5058 Controller

The RC5058 is a programmable synchronous DC-DC controller IC. When designed around the appropriate external components, the RC5058 can be configured to deliver more than 16A of output current, as appropriate for the Katmai and Coppermine and other processors. The RC5058 functions as a fixed frequency PWM step down regulator.

Main Control Loop

Refer to the RC5058 Block Diagram on page 1. The RC5058 implements “summing mode control”, which is different from both classical voltage-mode and current-mode control. It provides superior performance to either by allowing a large converter bandwidth over a wide range of output loads.

The control loop of the regulator contains two main sections: the analog control block and the digital control block. The analog section consists of signal conditioning amplifiers feeding into a comparator which provides the input to the digital control block. The signal conditioning section accepts input from the DROOP (current feedback) and VFB (voltage feedback) pins and sets up two controlling signal paths. The first, the voltage control path, amplifies the difference between the VFB signal and the reference voltage from the DAC and presents the output to one of the summing amplifier inputs. The second, current control path, takes the difference between the DROOP and SW pins when the high-side MOSFET is on, reproducing the voltage across the MOSFET and thus the input current; it presents the resulting signal to another input of the summing amplifier. These two signals are then summed together. This output is then presented to a comparator looking at the oscillator ramp, which provides the main PWM control signal to the digital control block.

The digital control block takes the analog comparator input and the main clock signal from the oscillator to provide the appropriate pulses to the HIDRV and LODRV output pins. These two outputs control the external power MOSFETs.

There is an additional comparator in the analog control section whose function is to set the point at which the RC5058 current limit comparator disables the output drive signals to the external power MOSFETs.

High Current Output Drivers

The RC5058 contains two identical high current output drivers that utilize high speed bipolar transistors in a push-pull configuration. The drivers’ power and ground are separated from the chip’s power and ground for switching noise immunity. The power supply pin, VCCP, is supplied from an external 12V source through a series 33Ω resistor. The resulting voltage is sufficient to provide the gate to source drive to the external MOSFETs required in order to achieve a low $R_{DS,ON}$.

Internal Voltage Reference

The reference included in the RC5058 is a precision band-gap voltage reference. Its internal resistors are precisely trimmed to provide a near zero temperature coefficient (TC). Based on the reference is the output from an integrated 5-bit DAC. The DAC monitors the 5 voltage identification pins, VID0-4. When the VID4 pin is at logic HIGH, the DAC scales the reference voltage from 2.0V to 3.5V in 100mV increments. When VID4

is pulled LOW, the DAC scales the reference from 1.30V to 2.05V in 50mV increments. All VID codes are available, including those below 1.80V.

Power Good (PWRGD)

The RC5058 Power Good function is designed in accordance with the Pentium II DC-DC converter specifications and provides a continuous voltage monitor on the VFB pin. The circuit compares the VFB signal to the VREF voltage and outputs an active-low interrupt signal to the CPU should the power supply voltage deviate more than ±12% of its nominal setpoint. The Power Good flag provides no other control function to the RC5058.

Output Enable/Soft Start (ENABLE/SS)

The RC5058 will accept an open collector/TTL signal for controlling the output voltage. The low state disables the output voltage. When disabled, the PWRGD output is in the low state.

Even if an enable is not required in the circuit, this pin should have attached a capacitor (typically 100nF) to softstart the switching.

Over-Voltage Protection

The RC5058 constantly monitors the output voltage for protection against over-voltage conditions. If the voltage at the VFB pin exceeds the selected program voltage, an over-voltage condition is assumed and the RC5058 disables the output drive signal to the external high-side MOSFET. The DC-DC converter returns to normal operation after the output voltage returns to normal levels.

Oscillator

The RC5058 oscillator section uses a fixed frequency of operation of 300KHz.

Design Considerations and Component Selection

Additional information on design and component selection may be found in Fairchild's Application Note 57.

MOSFET Selection

This application requires N-channel Logic Level Enhancement Mode Field Effect Transistors. Desired characteristics are as follows:

- Low Static Drain-Source On-Resistance, $R_{DS,ON} < 20m\Omega$ (lower is better)
- Low gate drive voltage, $V_{GS} = 4.5V$ rated
- Power package with low Thermal Resistance
- Drain-Source voltage rating > 15V.

The on-resistance ($R_{DS,ON}$) is the primary parameter for MOSFET selection. The on-resistance determines the power dissipation within the MOSFET and therefore significantly affects the efficiency of the DC-DC Converter. For details and a spreadsheet on MOSFET selection, refer to Applications Bulletin AB-8.

Inductor Selection

Choosing the value of the inductor is a tradeoff between allowable ripple voltage and required transient response. The system designer can choose any value within the allowed minimum to maximum range in order to either minimize ripple or maximize transient performance. The first order equation (close approximation) for minimum inductance is:

$$L_{min} = \frac{(V_{in} - V_{out})}{f} \times \frac{V_{out}}{V_{in}} \times \frac{ESR}{V_{ripple}}$$

where:
V_{in} = Input Power Supply
V_{out} = Output Voltage
f = DC/DC converter switching frequency
ESR = Equivalent series resistance of all output capacitors in parallel
V_{ripple} = Maximum peak to peak output ripple voltage budget.

The first order equation for maximum allowed inductance is:

$$L_{max} = 2C_O \frac{(V_{in} - V_{out})\, D_m\, V_{tb}}{I_{pp}^2}$$

where:
C_o = The total output capacitance
I_{pp} = Maximum to minimum load transient current
V_{tb} = The output voltage tolerance budget allocated to load transient
D_m = Maximum duty cycle for the DC/DC converter (usually 95%).

Some margin should be maintained away from both L_{min} and L_{max}. Adding margin by increasing L almost always adds expense since all the variables are predetermined by system performance except for C_O, which must be increased to increase L. Adding margin by decreasing L can be done by purchasing capacitors with lower ESR. The RC5058 provides significant cost savings for the newer CPU systems that typically run at high supply current.

RC5058 Short Circuit Current Characteristics

The RC5058 protects against output short circuit on the core supply by turning off both the high-side and low-side MOSFETs and resetting softstart. The short circuit limit is set with the R_S resistor, as given by the formula

$$R_S = \frac{I_{SC} * R_{DS,\,on}}{I_{Detect}}$$

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with $I_{Detect} \approx 50\mu A$, I_{SC} is the desired current limit, and $R_{DS,on}$ the high-side MOSFET's on resistance. Remember to make the R_S large enough to include the effects of initial tolerance and temperature variation on the MOSFET's $R_{DS,on}$. Alternately, use of a sense resistor in series with the source of the MOSFET eliminates this source of inaccuracy in the current limit. The value of R_S should be less than 10KΩ. If a greater value is necessary, a lower $R_{DS,on}$ MOSFET should be used instead.

As an example, Figure 4 shows the typical characteristic of the DC-DC converter circuit with an FDB6030L high-side MOSFET (R_{DS} = 20mΩ maximum at 25°C * 1.25 at 75°C = 25mΩ) and a 8.2KΩ R_S.

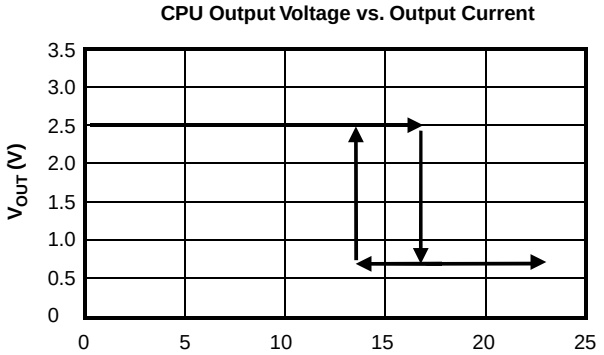


Figure 4. RC5058 Short Circuit Characteristic

The converter exhibits a normal load regulation characteristic until the voltage across the MOSFET exceeds the internal short circuit threshold of 50µA * 8.2KΩ = 410mV, which occurs at 410mV/25mΩ = 16.4A. (Note that this current limit level can be as high as 410mV/15mΩ = 27A, if the MOSFET has typical $R_{DS,on}$ rather than maximum, and is at 25°C).

At this point, the internal comparator trips and signals the controller to discharge softstart. This causes a drastic reduction in the output voltage as the load regulation collapses into the short circuit control mode. With a 40mΩ output short, the voltage is reduced to 16.4A * 40mΩ = 650mV. The output voltage does not return to its nominal value until the output current is reduced to a value within the safe operating ranges for the DC-DC converter.

If any of the linear regulator outputs are loaded heavily enough that their output voltage drops below 80% of nominal for >30µsec, all RC5058 outputs, including the switcher, are shut off and remain off until power is recycled.

Schottky Diode Selection

The application circuit of Figure 1 shows a Schottky diode, D1, which is used as a free-wheeling diode to assure that the body-diode in Q2 does not conduct when the upper MOSFET is turning off and the lower MOSFET is turning on. It is undesirable for this diode to conduct because its high forward voltage drop and long reverse recovery time degrades efficiency, and so the Schottky provides a shunt path for the current. Since this time duration is very short, the selection criterion for the diode is that the forward voltage of the Schottky at the output current should be less than the forward voltage of the MOSFET's body diode.

Output Filter Capacitors

The output bulk capacitors of a converter help determine its output ripple voltage and its transient response. It has already been seen in the section on selecting an inductor that the ESR helps set the minimum inductance, and the capacitance value helps set the maximum inductance. For most converters, however, the number of capacitors required is determined by the transient response and the output ripple voltage, and these are determined by the ESR and not the capacitance value. That is, in order to achieve the necessary ESR to meet the transient and ripple requirements, the capacitance value required is already very large.

The most commonly used choice for output bulk capacitors is aluminum electrolytics, because of their low cost and low ESR. The only type of aluminum capacitor used should be those that have an ESR rated at 100kHz. Consult Application Bulletin AB-14 for detailed information on output capacitor selection.

The output capacitance should also include a number of small value ceramic capacitors placed as close as possible to the processor; 0.1µF and 0.01µF are recommended values.

Input Filter

The DC-DC converter design may include an input inductor between the system +5V supply and the converter input as shown in Figure 5. This inductor serves to isolate the +5V supply from the noise in the switching portion of the DC-DC converter, and to limit the inrush current into the input capacitors during power up. A value of 2.5µH is recommended.

It is necessary to have some low ESR aluminum electrolytic capacitors at the input to the converter. These capacitors deliver current when the high side MOSFET switches on. Figure 5 shows 3 x 1000µF, but the exact number required will vary with the speed and type of the processor. For the top speed Katmai and Coppermine, the capacitors should be rated to take 9A and 6A of ripple current respectively. Capacitor ripple current rating is a function of temperature, and so the manufacturer should be contacted to find out the ripple current rating at the expected operational temperature. For details on the design of an input filter, refer to Applications Bulletin AB-15.

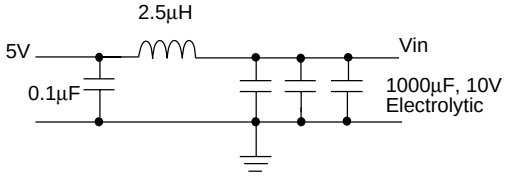


Figure 5. Input Filter

Programmable Active Droop™

The RC5058 includes Programmable Active Droop™: as the output current increases, the output voltage drops, and the amount of this drop is user adjustable. This is done in order to allow maximum headroom for transient response of the converter. The current is typically sensed by measuring the voltage across the $R_{DS,on}$ of the high-side MOSFET during its on time, as shown in Figure 1.

To program the amount of droop, use the formula

$$R_D \simeq \frac{14.4K\Omega * I_{max} * R_{sense}}{V_{Droop} * 18}$$

where I_{max} is the current at which the droop occurs, and R_{sense} is the resistance of the current sensor, either the source resistor or the high-side MOSFET's on-resistance. For example, to get 30mV of droop with a maximum output current of 12.5A and a 10mΩ sense resistor, use R_D = 14.4KΩ * 12.5A * 10mΩ/(30mV * 18) = 3.33KΩ. Further details on use of the Programmable Active Droop™ may be found in Applications Bulletin AB-24.

Remote Sense

The RC5058 offers remote sense of the output voltage to minimize the output capacitor requirements of the converter. It is highly recommended that the remote sense pin, Pin 20, be tied directly to the processor power pins, so that the effects of power plane impedance are eliminated. Further details on use of the remote sense feature of the RC5058 may be found in Applications Bulletin AB-24.

Adjusting the Linear Regulators' Output Voltages

Any or all of the linear regulators' outputs may be adjusted high to compensate for voltage drop along traces, as shown in Figure 6.

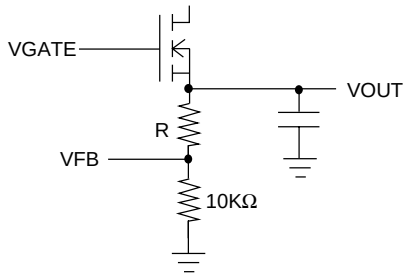


Figure 6. Adjusting the Output Voltage of the Linear Regulator

The resistor value should be chosen as

$$R = 10K\Omega * \left(\frac{V_{out}}{V_{nom}} - 1\right)$$

For example, to get the V_{TT} voltage to be 1.55V instead of 1.50V, use R = 10KΩ * [(1.55/1.50) – 1] = 333Ω.

Using the RC5058 for Vnorthbridge = 1.8V

In some motherboards, Intel requires that the AGP power can not be greater than 2.2V while the chipset voltage (Vnorthbridge = 1.8V) is less than 1.0V. The RC5058 can accomplish this by using the VTT regulator to generate Vnorthbridge. Use the circuit in Figure 6 with R = 2KΩ. Since the linear regulators on the RC5058 all rise proportionally to one another, when Vnorthbridge = 1.0V, Vagp = 1.8V, meeting the Intel requirement.

PCB Layout Guidelines

- Placement of the MOSFETs relative to the RC5058 is critical. Place the MOSFETs such that the trace length of the HIDRV and LODRV pins of the RC5058 to the FET gates is minimized. A long lead length on these pins will cause high amounts of ringing due to the inductance of the trace and the gate capacitance of the FET. This noise radiates throughout the board, and, because it is switching at such a high voltage and frequency, it is very difficult to suppress.
- In general, all of the noisy switching lines should be kept away from the quiet analog section of the RC5058. That is, traces that connect to pins 1, 2, 23, and 24 (HIDRV, SW, LODRV and VCCP) should be kept far away from the traces that connect to pins 3, 20 and 21.
- Place the 0.1µF decoupling capacitors as close to the RC5058 pins as possible. Extra lead length on these reduces their ability to suppress noise.
- Each VCC and GND pin should have its own via to the appropriate plane. This helps provide isolation between pins.
- Place the MOSFETs, inductor, and Schottky as close together as possible for the same reasons as in the first bullet above. Place the input bulk capacitors as close to the drains of the high side MOSFETs as possible. In addition, placement of a 0.1µF decoupling cap right on the drain of each high side MOSFET helps to suppress some of the high frequency switching noise on the input of the DC-DC converter.
- Place the output bulk capacitors as close to the CPU as possible to optimize their ability to supply instantaneous current to the load in the event of a current transient. Additional space between the output capacitors and the CPU will allow the parasitic resistance of the board traces to degrade the DC-DC converter's performance under severe load transient conditions, causing higher voltage deviation. For more detailed information regarding capacitor placement, refer to Application Bulletin AB-5.
- A PC Board Layout Checklist is available from Fairchild Applications. Ask for Application Bulletin AB-11.

PC Motherboard Sample Layout and Gerber File

A reference design for motherboard implementation of the RC5058 along with the PCAD layout Gerber file and silk screen can be obtained from our marketing department at 650-966-7624.

RC5058 Evaluation Board

Fairchild provides an evaluation board to verify the system level performance of the RC5058. It serves as a guide to performance expectations when using the supplied external components and PCB layout. Please call the marketing department at 650-966-7624 for an evaluation board.

Additional Information

For additional information contact Fairchild Semiconductor's Analog & Mixed Signal Products Group Marketing Department at 650-966-7624.

Appendix

Worst-Case Formulae for the Calculation of Cin, Cout , R5, R7 and Roffset (Circuits similar to Figure 1 only)

The following formulae design the RC5058 for worst-case operation, including initial tolerance and temperature dependence of all of the IC parameters (initial setpoint, reference tolerance and tempco, internal droop impedance, current sensor gain), the initial tolerance and temperature dependence of the MOSFET, and the ESR of the capacitors. The following information must be provided:

V_{S+}, the value of the positive static voltage limit;

$|V_{S-}|$, the absolute value of the negative static voltage limit;

V_{T+}, the value of the positive transient voltage limit;

$|V_{T-}|$, the absolute value of the negative transient voltage limit;

I_O, the maximum output current;

V_{nom}, the nominal output voltage;

V_{in}, the input voltage (typically 5V);

I_{rms}, the ripple current rating of the input capacitors, per cap (2A for the Sanyo parts shown in this datasheet);

R_D, the resistance of the current sensor (usually the MOSFET);

ΔR_D, the tolerance of the current sensor (usually about 67% for MOSFET sensing, including temperature); and

ESR, the ESR of the output capacitors, per cap (44mΩ for the Sanyo parts shown in this datasheet).

$$C_{in} = \frac{IO * \sqrt{\frac{V_{nom}}{V_{in}} - \left(\frac{V_{nom}}{V_{in}}\right)^2}}{I_{rms}}$$

$$R_{offset} = \frac{V_{S+} - .024 * V_{nom}}{1.01 * V_{nom}} * 1K\Omega$$

$$R7 = \frac{I_O * R_D * (1 + \Delta R_D)}{45 * 10^{-6}}$$

$$R5 = \frac{14400 * I_O * R_D * (1 + \Delta R_D) * 1.1}{18 * (V_{S+} + |V_{S-}| - .024 * V_{nom})}$$

Number of capacitors needed for C_{out} = the greater of:

$$X = \frac{ESR * I_O}{|V_{T-}| + V_{S+} - .024 * V_{nom}}$$

or

$$Y = \frac{ESR * I_O}{V_{T+} - V_{S+} + \frac{14400 * I_O * R_D}{18 * R5 * 1.1}}$$

Example: Suppose that the static limits are +89mV/-79mV, transient limits are ±134mV, current I is 14.2A, and the nominal voltage is 2.000V, using MOSFET current sensing. We have V_{S+} = 0.089, $|V_{S-}|$ = 0.079, V_{T+} = $|V_{T-}|$ = 0.134, I_O = 14.2, V_{nom} = 2.000, and ΔR_D = 1.67. We calculate:

$$C_{in} = \frac{14.2 * \sqrt{\frac{2.000}{5} - \left(\frac{2.000}{5}\right)^2}}{2} = 3.47 \Rightarrow 4 \text{ caps}$$

$$R_{offset} = \frac{0.089 - .024 * 2.000}{1.01 * 2.000} * 1000 = 20.3\Omega$$

$$R7 = \frac{14.2 * 0.020 * (1 + 0.67)}{45 * 10^{-6}} = 10.5K\Omega$$

$$R5 = \frac{14400 * 14.2 * 0.020 * (1 + 0.67) * 1.1}{18 * (0.089 + 0.079 - .024 * 2.000)} = 3.48K\Omega$$

$$X = \frac{0.044 * 14.2}{0.134 + 0.089 - .024 * 2.00} = 3.57$$

$$Y = \frac{0.044 * 14.2}{0.134 - 0.089 + \frac{14400 * 14.2 * 0.020}{18 * 3640 * 1.1}} = 6.14$$

Since Y > X, we choose Y, and round up to find we need 7 capacitors for C_{OUT}.

A detailed explanation of this calculation may be found in Applications Bulletin AB-24.

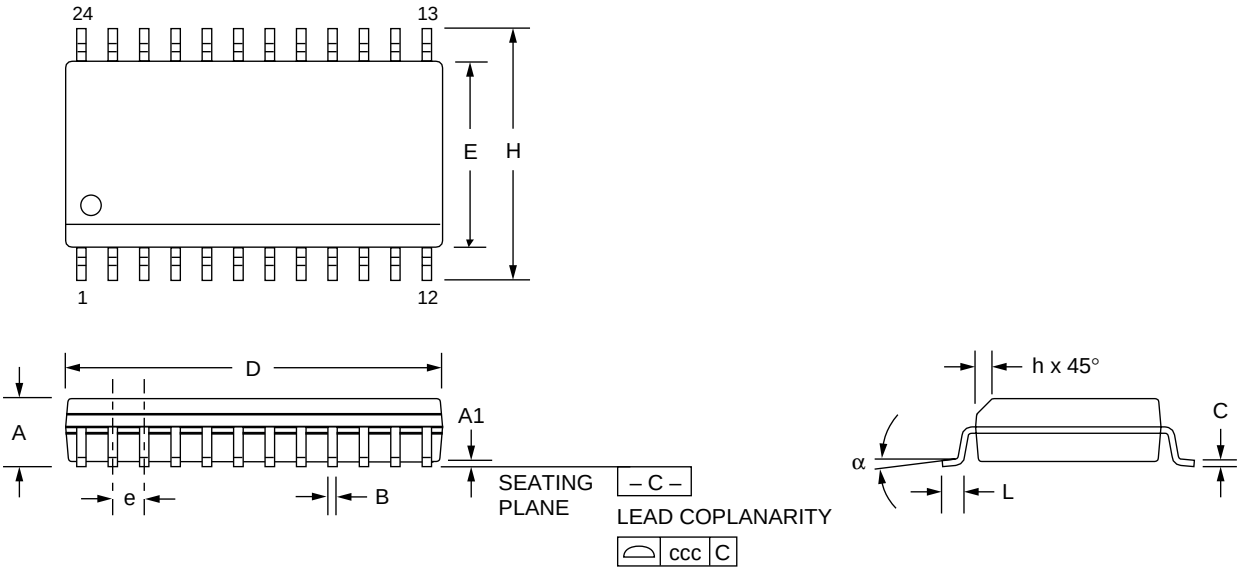
Mechanical Dimensions

24 Lead SOIC

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.599	.614	15.20	15.60	2
E	.290	.299	7.36	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.020	0.25	0.51	
L	.016	.050	0.40	1.27	3
N	24		24		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.



Ordering Information

Product Number	Package
RC5058M	24 pin SOIC

Preliminary Specification

RC5060

ACPI Switch Controller

Features

- Implements ACPI control with PWROK, SLP_S3# and SLP_S5#
- Switch and linear regulator controller for 3.3V Dual (PCI)
- Linear regulator controller and linear regulator for 2.5V Dual (RAMBUS)
- Two switch controller for 5V Dual (USB)
- Switch controller and linear regulator for 3.3V SDRAM
- Provides SDRAM and RAMBUS power simutaneously
- Adaptive Break-before-Make
- Integrated Power Good
- Drives all N-Channel MOSFETs plus NPN
- Latched overcurrent protection for outputs, functional during startup too
- Power-up softstarts for the linear regulators
- UVLO guarantees correct operation for all conditions
- 20 pin SOIC package

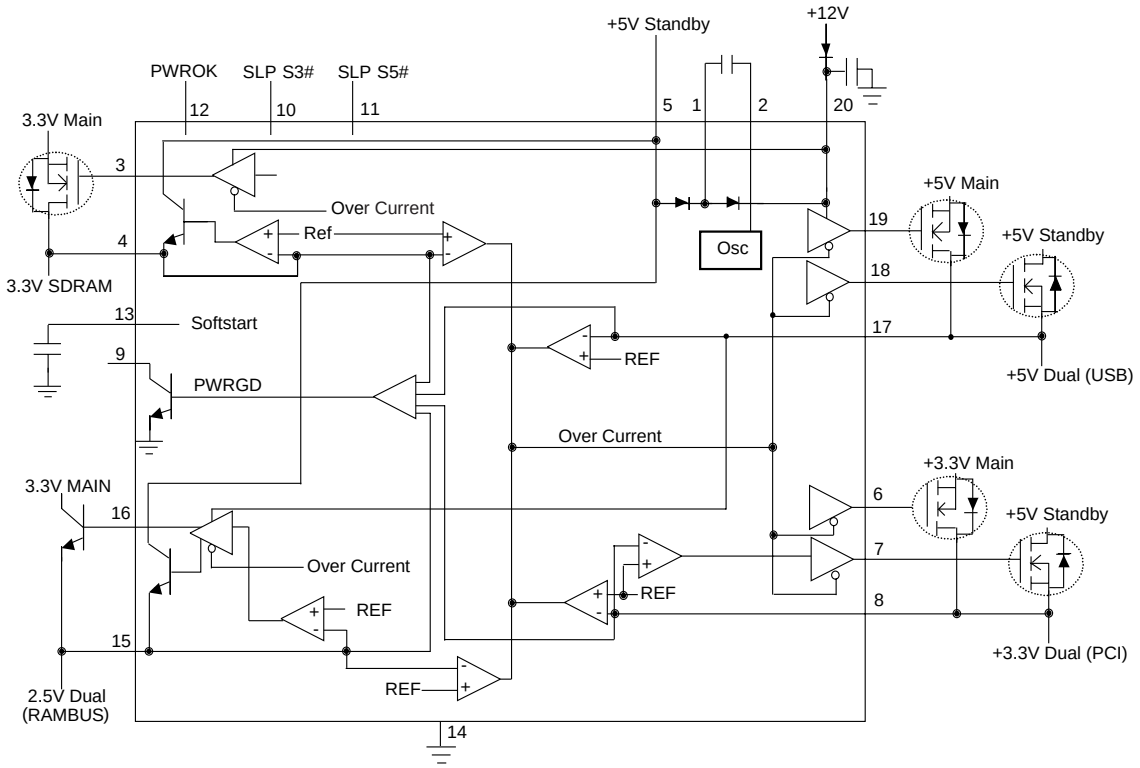
Applications

- Camino Platform ACPI Controller
- Whitney Platform ACPI Controller

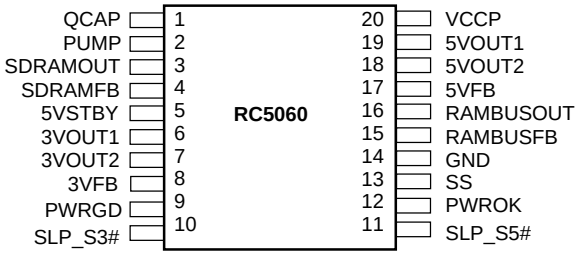
Description

The RC5060 is an ACPI Switch Controller for the Camino and Whitney Platforms. It is controlled by PWROK, SLP_S3# and SLP_S5#, and provides 3.3V Dual for PCI, 3.3V for SDRAM, 2.5V Dual for RAMBUS, and 5V Dual voltages. An on-board precision low TC reference achieves tight tolerance voltage regulation without expensive external components. The RC5060 also offers integrated Power Good and Current Limiting that protects each output, and softstart for the linear regulators. The RC5060 is available in a 20 pin SOIC.

Block Diagram



Pin Assignments



Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	QCAP	**Charge pump cap.** Attach flying capacitor between this pin and PUMP to generate high voltage from standby power.
2	PUMP	**Charge pump switcher.**
3	SDRAMOUT	**3.3V SDRAM gate control.** Attach this pin to a transistor powering 3.3V SDRAM from the 3.3V main supply.
4	SDRAMFB	**3.3V SDRAM voltage feedback.** Pin 4 is used as the input for the voltage feedback control loop for 3.3V SDRAM, and also sources 3.3V SDRAM in standby.
5	5VSTBY	**5V Standby.** Apply +5V standby on this pin to run the circuit in standby mode.
6	3VOUT1	**3.3V main gate control.** Attach this pin to a transistor powering 3.3V dual from the 3.3V main supply.
7	3VOUT2	**3.3V standby gate control.** Attach this pin to a transistor powering 3.3V dual from the 5V standby supply.
8	3VFB	**3.3V voltage Feedback.** Pin 8 is used as the input for the voltage feedback control loop for 3.3V dual.
9	PWRGD	**Power Good.** Open collector output is high when all outputs are valid.
10	SLP_S3#	**SLP_S3#.** Control signal governing the Soft Off state S3. Internal current source pulls this line high if left open.
11	SLP_S5#	**SLP_S5#.** Control signal governing the Soft Off state S5. Internal current source pulls this line high if left open.
12	PWROK	**PWROK.** Control signal for switches. Internal current source pulls this line high if left open.
13	SS	**Softstart.** Attach a capacitor to this pin to determine the softstart rate.
14	GND	**Ground.** Connect this pin to ground.
15	RAMBUSFB	**2.5V feedback.** Pin 15 is used as the input for the voltage feedback control loop for 2.5V dual (RAMBUS), and also sources 2.5V dual in standby.
16	RAMBUSOUT	**2.5V base drive control.** Attach this pin to an NPN transistor powering 2.5V dual (RAMBUS) from the 3.3V main supply.
17	5VFB	**5V Voltage Feedback.** Pin 17 is used to sense undervoltage to protect the 5V dual from overcurrent.
18	5VOUT2	**5V standby gate control.** Attach this pin to a transistor powering 5V dual from the 5V standby supply.
19	5VOUT1	**5V main gate control.** Attach this pin to a transistor powering 5V dual from the 5V main supply.
20	VCCP	**Main Power.** Apply +12V through a diode on this pin to run the circuit in normal mode. Bypass with a 0.1µF capacitor. When 12V is not present, this pin produces voltage doubled 5V standby.

Absolute Maximum Ratings

All Pins	13.5V
Junction Temperature, T_J	150°C
Storage Temperature	-65 to 150°C
Lead Soldering Temperature, 10 seconds	300°C
Thermal Resistance Junction to Ambient Θ_{JA}	85°C/W
Thermal Resistance Junction-to-case, Θ_{JC}	24°C/W

Recommended Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
+3.3VMAIN		3.135	3.3	3.465	V
+5VMAIN		4.75	5	5.25	V
+5VSTBY		4.75	5	5.25	V
+12V		11.4	12	12.6	V
Ambient Operating Temperature		0		70	°C

Preliminary Specification

Preliminary Specification

Electrical Specifications

($V_{+5VSTBY}$ = $V_{+5VMAIN}$ =5V, $V_{+3.3V}$ = 3.3V, V_{+12V} = 12V and T_A = +25°C using circuit in Figure 3, unless otherwise noted.)
The • denotes specifications which apply over the full operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
+5V DUAL						
V_{Out1}, On		•	10			V
V_{Out1}, Off		•			200	mV
$V_{GS, Out2}$	Standby	•	2.7			V
V_{Out2}, Off		•			200	mV
Maximum Drive Current, Each		•	10			mA
Overcurrent Limit: Undervoltage				80		$\%V_{out}$
Overcurrent Delay Time				30		µsec
Output Driver Overlap Time	See Figure 2	•	1		5	µsec
+3.3V DUAL						
V_{Out1}, On		•	10			V
V_{Out1}, Off		•			200	mV
Total Output Voltage Variation[1]	3VOUT2 On	•	3.135	3.3	3.465	V
Maximum Drive Current		•	100			mA
Minimum Load Current	3VOUT2 On	•			50	mA
Overcurrent Limit: Undervoltage				80		%Vout
Overcurrent Delay Time				30		µsec
Output Driver Deadtime	See Figure 2: Main → Standby	•	2		6	µsec
	: Standby → Main	•	200		1000	nsec
+2.5V DUAL						
I_B, On	RAMBUSOUT On	•	200			mA
I_{Out}	RAMBUSOUT Off	•	144			mA
Total Output Voltage Variation[1]		•	2.375	2.5	2.625	V
Overcurrent Limit				80		%Vout
Overcurrent Delay Time				30		µsec
Output Driver Overlap Time	See Figure 2	•	1		5	µsec
+3.3V SDRAM						
V_{out}, On		•	10			V
V_{out}, Off		•			200	mV
I_{Out}	SDRAMOUT Off	•	100			mA
Overcurrent Limit				80		%Vout
Total Output Voltage Variation[1]	SDRAMFB On	•	3.135	3.3	3.465	V
Overcurrent Delay Time				30		µsec
Output Driver Dead Time		•	200		1500	nsec
Common Functions						
PWRGD Threshold				80		%Vout
PWRGD Delay Time				30		µsec
PWRGD Sink Current		•	1			mA
Charge Pump Frequency				200		KHz
+5VSTBY UVLO				4.5		V
+5VSTBY UVLO Hysteresis				0.5		V

Electrical Specifications (continued)

($V_{+5VSTBY}$ = $V_{+5VMAIN}$ =5V, $V_{+3.3V}$ = 3.3V, V_{+12V} = 12V and T_A = +25°C using circuit in Figure 3, unless otherwise noted.)
The • denotes specifications which apply over the full operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
+12V UVLO				7.5		V
+12V UVLO Hysteresis				1		V
+5VSTBY Current	MAIN Power Present			10	25	mA
+12V Current				2.5	10	mA
Input Logic HIGH		•	2.0			V
Input Logic LOW		•			0.8	V
Softstart Current				10		µA
Control Line Input Current	SLP_S5#, SLP_S3#, PWROK	•			10	µA
Over Temperature Shutdown				150		°C

Note:
1. Voltage Regulation includes Initial Voltage Setpoint and Output Temperature Drift.

Table 1. Static Power Descriptors

PWROK	SLP_S3#	SLP_S5#	Main	5 & 3.3V Duals	2.5V Dual/3.3V SDRAM	State
0	0	0	OFF	ON	OFF	S5
0	0	1	OFF	ON	ON	S3
1	0	0	OFF	ON	OFF	S0 → S5
1	0	1	OFF	ON	ON, Powered from STBY	S0 → S3
1	1	1	ON	ON	ON, Powered from MAIN	S0

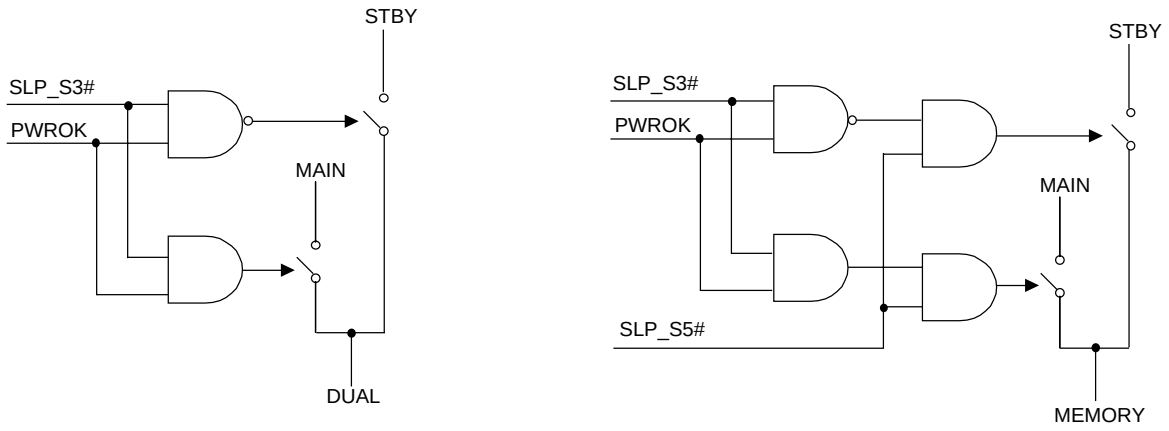


Figure 1. Control Logic for Dual Voltages and Memory Voltages

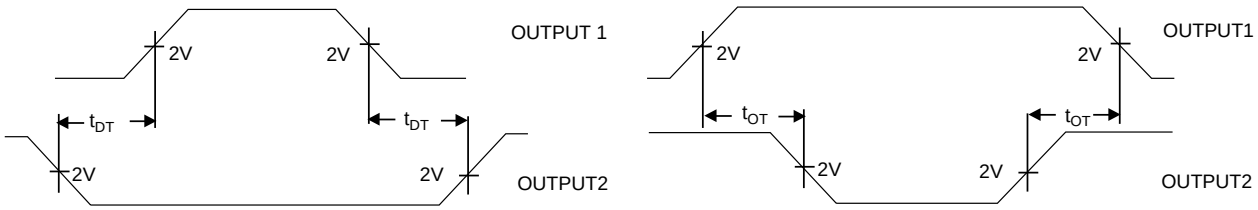


Figure 2. Deadtime and Overlap Time Measurements

Application Circuits

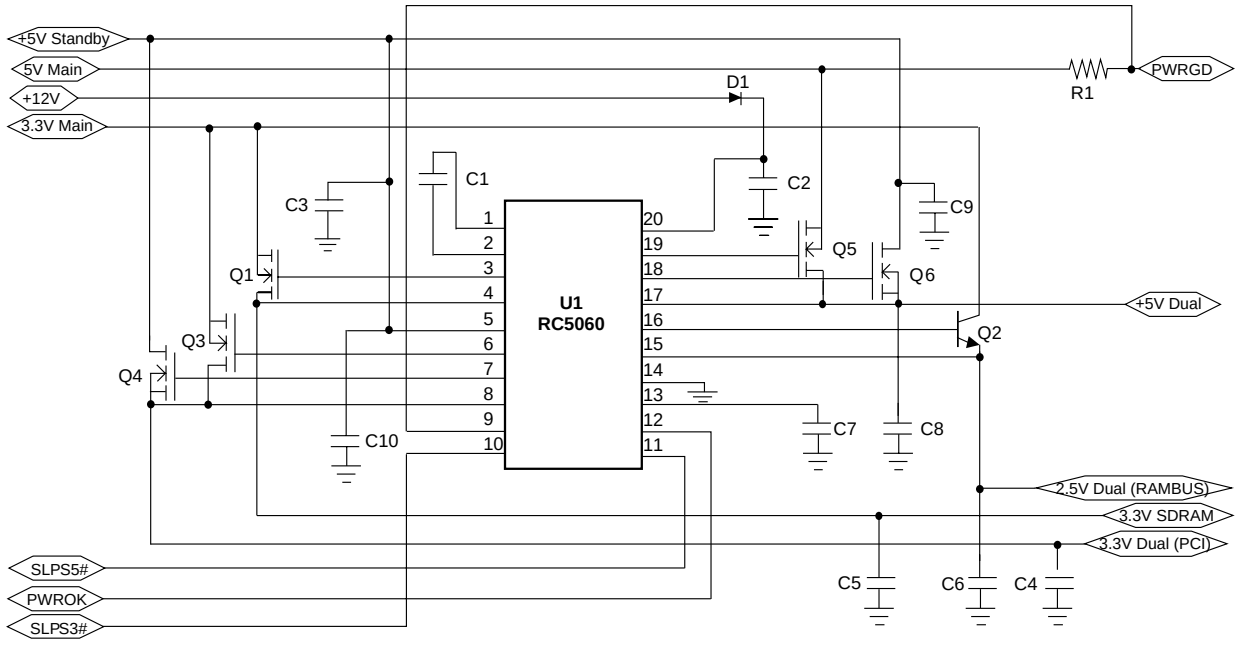


Figure 3. Camino ACPI Selector

Table 2. RC5060 Application Bill of Materials for Camino

Reference	Manufacturer, Part #	Quantity	Description	Comments
C1-3, C8	Various	4	100nF, 25V	Ceramic
C4–6, C9	Various	4	220µF, 6V	Tantalum, ESR ~ 0.1Ω
C7	Various	1	10nF, 50V	Ceramic
C10	Various	1	47µF, 10V	Tantalum
R1	Various	1	10KΩ Resistor	
D1	Fairchild MBR0520L	1	20V, 1/2A Schottky	
Q1, Q3	Fairchild FDS4410DY	2	N-channel MOSFET	$R_{ds,on}$ = 20mΩ @ V_{gs} = 4.5V
Q2	Fairchild TIP41A	1	NPN	V_{CE} ~0.4V @ I_C = 2A, I_B = 100mA
Q4	Fairchild NDS9956A	1	N-channel MOSFET	$R_{ds,on}$ = 110mΩ @ V_{gs} = 4.5V
Q5-6	Fairchild NDH833N	2	N-channel MOSFET	$R_{ds,on}$ = 25mΩ @ V_{gs} = 2.7V
U1	Fairchild RC5060	1	ACPI Switch Controller	

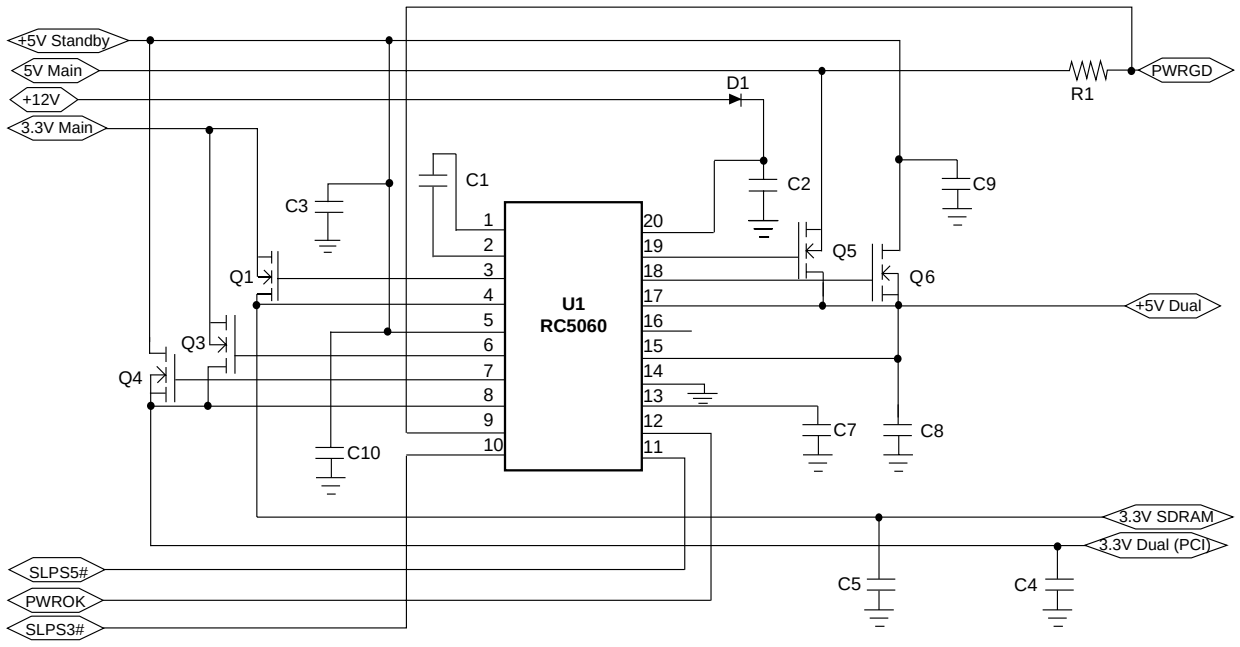


Figure 4. Whitney ACPI Selector

Table 3. RC5060 Application Bill of Materials for Whitney

Reference	Manufacturer, Part #	Quantity	Description	Comments
C1-3, C8	Various	4	100nF, 25V	Ceramic
C4-5, C9	Various	3	220µF, 6V	Tantalum, ESR ~ 0.1Ω
C7	Various	1	10nF, 50V	Ceramic
C10	Various	1	47µF, 10V	Tantalum
R1	Various	1	10KΩ Resistor	
D1	Fairchild MBR0520L	1	20V, 1/2A Schottky	
Q1, Q3	Fairchild FDS4410DY	2	N-channel MOSFET	$R_{ds,on}$ = 20mΩ @ V_{gs} = 4.5V
Q4	Fairchild NDS9956A	1	N-channel MOSFET	$R_{ds,on}$ = 110mΩ @ V_{gs} = 4.5V
Q5-6	Fairchild NDH833N	2	N-channel MOSFET	$R_{ds,on}$ = 25mΩ @ V_{gs} = 2.7V
U1	Fairchild RC5060	1	ACPI Switch Controller	

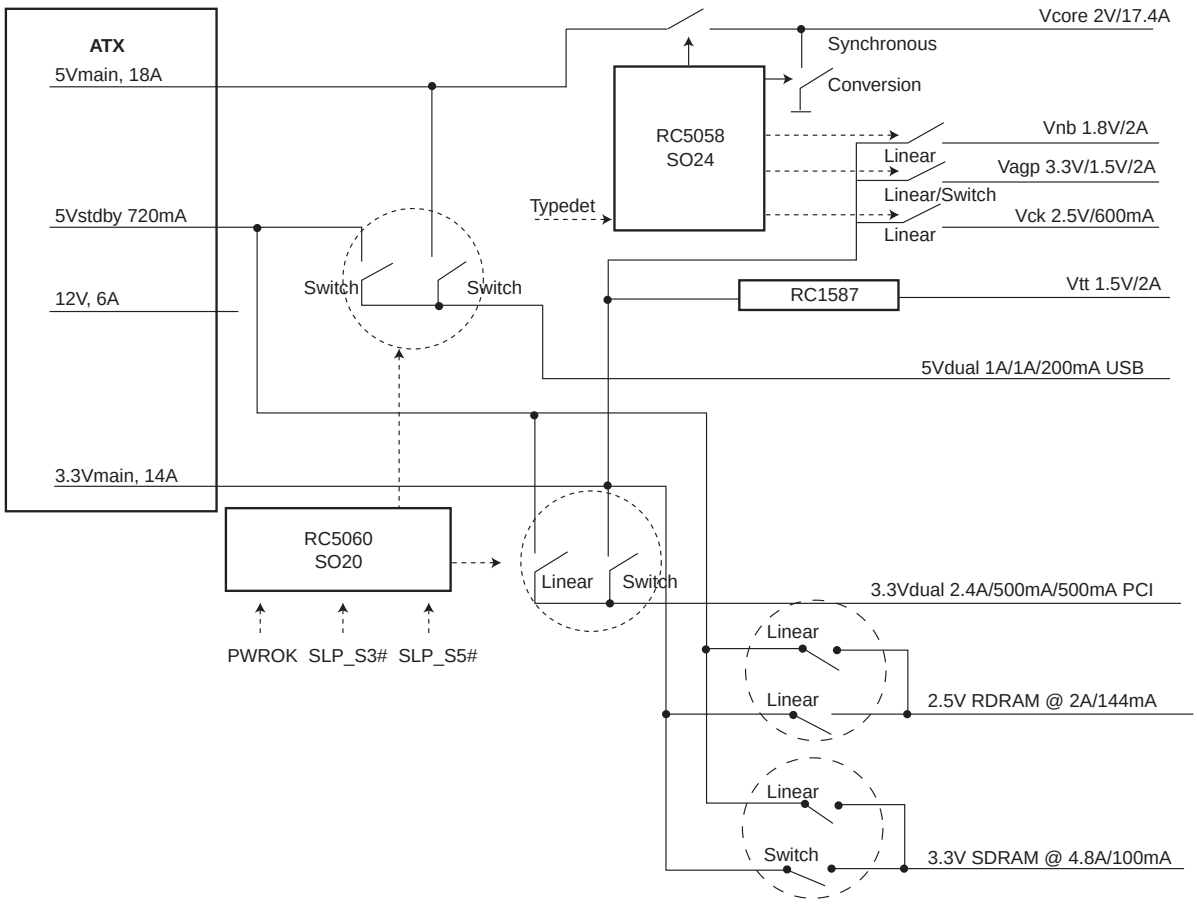


Figure 5. Camino System Architectural Block Diagram (Power Paths Only)

Application Information

The RC5060 Controller

The RC5060 is a fully compliant ACPI controller IC. Used with an ATX power supply, it generates a 5V Dual voltage, a 3.3V Dual for PCI, and power for both SDRAM and RAMBUS, and has a large array of additional protection functions integrated in. Used in conjunction with Fairchild's RC5058, it provides the complete set of control and power functions necessary to implement a Camino or Whitney motherboard.

Overview of ACPI

The Advanced Configuration and Power Interface, or ACPI, is a system for controlling the use of power in a computer. It enables the computer manufacturer and the computer user to determine the computer's power usage dynamically. For example, when the computer has been unused for a certain time, the monitor and peripherals could be turned off, and their states saved to memory. After a longer period, the processor could be turned off, and the memory saved to disk. A peripheral could then re-awaken the entire system on the occurrence of an event, such as the arrival of a FAX on a modem.

As shown in Figure 5, the available power inputs to the computer system from the ATX power supply are +5V main, +12V main, +3.3V main, and +5V standby. "Main" means that these power outputs are available under full-power operation of the system, but can be turned off in some of the power-saving modes. "Standby" means that this power output is always present.

The most general ACPI system requires four dual outputs: 5V dual, 3.3V dual, 3.3V SDRAM, and 2.5V RAMBUS (or 2.5V dual). "Dual" means that the power can be (but is not necessarily) present whether the main power supplies are present or not. To ensure the presence of these outputs, while not overloading the standby power, they have dual inputs, from both main power and standby. The presence or absence of the dual outputs is determined by the control signals to the RC5060.

ACPI States

As shown in Table 1, there are three ACPI states that are of primary concern to the system designer, designated S0, S3 and S5. S0 is the full-power state, the state of the computer when it is being actively used. The other two states are sleep states, reflecting differing levels of power-down.

S3 is a state in which the processor is powered down, but its last state is being preserved in IC memory, which is kept on. Since memory is fast, the computer can quickly come back up to full operation. However, this state continues to draw moderate power, due to the memory being kept

S5 is a state in which memory is off, and the last state of the processor has been written to the hard disk. Since the disk is slow, the computer takes longer to come back to full operation. However, since memory is off, this state draws minimal power.

It is anticipated that only the following state transitions will occur: S0 → S3, S0 → S5, S3 → S5, S5 → S0, and S3 → S0; the transition S5 → S3 will not occur, as going from save-to-disk to save-to-memory will not be activated by any mechanism.

5V Dual Output

The RC5060 controls four separate dual outputs, the first of which is the 5V dual. This output is intended to run subsystems such as the USB ports. A typical application that would require the use of 5V dual rather than +5V main for a USB port would be the use of a USB mouse: if the system needs to be able to awaken from sleep when the mouse is moved, then the mouse must be powered from dual, because main power is off.

5V dual is generated by two MOSFET switches, one from +5V main, the other from +5V standby, as shown in Figures 3 or 4. When main power is present, the first switch is on and the second off, and the opposite when main power is absent. Note carefully the polarity of the MOSFET Q5 that delivers power from the +5V main to the 5V dual: opposite to the connection of Q6, the source is connected to the +5V main input, and the drain is connected to the 5V dual output. This connection must be done this way because of Q5's body diode. When +5V main is not present, 5V dual is still on, and if Q5 were connected with the same polarity as Q6, the dual voltage would conduct through the body diode of Q5, attempting to power up the entire +5V main line. It is to avoid this overload that Q5 must be connected as shown.

The state of the switches is controlled by the SLP_ S3# and PWROK lines, as shown in Figure 1. When both SLP_ S3# and PWROK are asserted, the main switch is on, and the standby switch is off. If either line is de-asserted, the main switch is off and the standby switch is on.

Note that Q5 and Q6 should be low-gate-voltage type MOSFETs, with guaranteed operation at 2.7V V_{gs}, in order to ensure full enhancement in worst case. In a typical system, it is anticipated that full-power current will be about 1A maximum, and standby current will be about 200mA maximum.

3.3V Dual Output

The 3.3V dual output is intended to power subsystems such as the computer's PCI slots. A typical application that would require the use of 3.3V dual rather than +3.3V main for a PCI slot would be the use of a modem: if the system needs to be able to awaken from sleep when the modem receives incoming data, then that slot must be powered from dual, because main power is off. Other slots not requiring dual power can be configured using the control signals.

3.3V dual is generated by two MOSFETs, one from +3.3V main, the other from +5V standby, as shown in Figures 3 or 4. When main power is present, the MOSFET Q3 is turned on as a switch, so that input and output are connected together. When main power is absent, the MOSFET Q4 is controlled by the RC5060 as a linear regulator, generating a regulated 3.3V from +5V standby. As with the 5V dual, the MOSFET Q3 must be connected as shown in the figures, to avoid back-feed.

The state of the MOSFETs is controlled by the SLP_S3# and PWROK lines, as shown in Figure 1. When both SLP_S3# and PWROK are asserted, the main switch is on, and the linear regulator is off. If either line is de-asserted, the main switch is off and the linear regulator is on.

Q3 and Q4 as shown in Tables 2 or 3 have different $R_{DS,on}$ ratings. In a typical system, it is anticipated that full-power current will be about 2.4A maximum, and standby current will be about 500mA maximum. The difference in maximum currents means that Q4 can be a less expensive device than Q3.

3.3V SDRAM Output

3.3V SDRAM output is intended to provide power to SDRAM memory. Most systems will use this power. Those systems using RAMBUS may also use the SDRAM power, possibly piped to the same slots, to ensure backward compatibility or even mixed operation of SDRAM with RAMBUS.

3.3V SDRAM is generated by one external MOSFET switch from +3.3V main, and one linear regulator internal to the RC5060 from +5V standby, as shown in Figures 3 or 4, and in the block diagram on the front page. When main power is present, the MOSFET Ql is turned on as a switch, so that input and output are connected together. When main power is absent, the internal linear regulator is on, generating a regulated 3.3V from +5V standby. As with the other duals, the MOSFET Ql must be connected as shown in the figures, to avoid back-feed.

The state of the external MOSFET and the internal linear regulator is controlled by the SLP_S3# and PWROK lines, and additionally the SLP_S5# line, as shown in Figure 1. When SLP_S5# is de-asserted, both the external MOSFET and the internal linear regulator are off, and there is no output voltage on the 3.3V SDRAM line.

If the SLP_S5# line is asserted, the 3.3V SDRAM output is on. In this condition, if either the SLP_S3# or the PWROK line, or both, are de-asserted, the linear regulator is on and the MOSFET is off. Only in the case if both the SLP_S3# and the PWROK lines are asserted, the MOSFET is on and the linear regulator is off.

In a typical system, it is anticipated that standby current will be about 100mA maximum. Full power current will be as high as 4.8A maximum, so that Ql must have a low $R_{DS,on}$ in order to prevent excessive voltage drop across it.

2.5V Dual Output

The 2.5V dual output is intended to provide power to RAMBUS memory. Only high-end systems will use this power. Those systems using RAMBUS may also use the SDRAM power, possibly piped to the same slots, to ensure backward compatibility or even mixed operation of SDRAM with RAMBUS.

2.5V dual is generated by one external NPN bipolar acting as a linear regulator from +3.3V main, and one linear regulator internal to the RC5060 from +5V standby, as shown in Figure 3, and in the block diagram on the front page. When main power is present, the NPN Q2 linear regulates, and when main power is absent, the internal linear regulator is on. Q2 cannot be substituted with a MOSFET. If used in one direction, the MOSFET's body diode would permit backfeed; if used in the other direction, it would short-circuit the linear regulator action.

2.5V dual output is controlled in the same way and by the same lines as the 3.3V SDRAM output. In a typical system, it is anticipated that standby current will be a maximum of 144mA, and full-power current may be as high as 2A. This places some significant constraints on the selection of Q2. Since its input may be as low as (3.3V - 5%) = 3.135V, there is only 3.135V -2.5V = 635mV of V_{CE} headroom for its operation as a linear regulator. For this reason the RC5060 can provide up to 200mA of steady-state base current. The TIP41 device shown has a sufficiently low $V_{CE,\ sat}$ to guarantee worst-case regulation even at 2A I_E with this base current.

RC5060 ACPI Control Lines

As already discussed, the RC5060 outputs are controlled by the three ACPI control lines, SLP_S3#, SLP_S5# and PWROK, as summarized in Table 1. System designers must in particular be careful to ensure that their system is designed with SLP_S5#, not SLP_S5#; if SLP_S5 is used, it must be inverted before being used with the RC5060.

The control lines have internal pull-ups of approximately 10µA, and so can be controlled by open collector drivers if desired. In a noisy system, it may be desirable to filter these lines, which can be done with a 1KΩ resistor and a small capacitor.

RC5060 Dynamic Operation

The RC5060 is designed to minimize the output capacitance required to hold up the various output lines during transitions between different states. Thus in particular, the 5V dual and 2.5V dual outputs have guaranteed minimum overlap times, the time (as shown in Figure 2) during a state transition during which both main and standby are connected to the output. This overlap time guarantees that a power source is always connected to the output, so that there will be no dip in the output voltage during state transitions. There is also a maximum overlap time, to ensure that the standby power doesn't have to source main power very long, thus minimizing thermal stress on the standby device.

The 3.3V dual and 3.3V SDRAM are different than the other outputs, because they are powered by both a linear regulator and a switch. If the linear regulator were to turn on while the switch is on (or vice versa) the linear regulator would supply power to the main line through the switch. For this reason, the linear regulator must be off before the switch is on, and vice versa. Thus, these two outputs have guaranteed minimum deadtime when both linear regulator and switch are off. During this time, the output capacitors must hold up the load, and so there is also a specified maximum deadtime, allowing a maximum necessary capacitance to be selected, see below.

Stability

As with all linear regulators, the RC5060's linear regulators require a minimum load. With the exception of the 3.3V dual output, however, all of these minimum loads are internal to the RC5060. The 3.3V dual output requires a minimum load of 50mA; if a situation may occur in which the load is less than 50mA, additional steps may be necessary to ensure stability.

Furthermore, depending on location, it may be necessary to bypass the drain (or collector) of the linear regulator with a low ESR capacitor for stability. As a rule of thumb, if the pass element is more than 1" from its power source, it should have a bypass.

Softstart

Pin 13 of the RC5060 functions as a softstart. When power is first applied to the chip, a constant current is applied from the pin into an external capacitor, linearly ramping up the voltage. This ramp in turn controls the internal reference of the RC5060. providing a softstart for the linear regulators. The actual state of the RC5060 on power up will be determined by the state of its control lines.

The switches in the system must be either on or off, and so softstart has no effect on their characteristics: if the appropriate control signals are asserted, they will turn on at once.

The softstart is effective only during power on. During a transition between states, such as from S5 → S0, the linear regulators are not softstarted.

It is important to note that the softstart pin is not an enable; pulling it low will not necessarily turn off all outputs.

Charge Pump

In main power operation, the RC5060 is run from the +12V main supply. This supply also provides voltage to the various MOSFET gates. However, during standby, this supply is off. To provide power to the chip and the appropriate gates, the RC5060 incorporates a free-running charge pump. As shown in Figures 3 and 4, and in the block diagram on the front page, a capacitor attached between pins 1 and 2 of the RC5060 acts as a charge pump with internal diodes. The charge pump output is internally diode or'red with the 12V input. The 12V input must have a series diode to prevent back-feeding the charge pump to the + 12V main when in standby. The 12V input line needs a bypass capacitor for high-frequency noise rejection.

Overcurrent

The RC5060 does not directly detect current through the eight devices that power its outputs. Instead, it monitors the four output voltages. In the event of a hard short, the voltage drops below 80% of nominal, and all outputs are latched off, and remain off until 5V standby power is recycled. The overcurrent latch off is delayed by 30µsec to prevent nuisance trips.

During softstart, the overcurrent voltage monitors are kept proportional to the reference, to avoid tripping overcurrent during startup. The monitors are kept active during softstart, to avoid turning on into a short.

In the S5 state, when the memory outputs are off, the voltage monitors on the memory lines are disabled, to prevent tripping the overcurrent. When turning these lines back on from the S5 state, the delay prevents overcurrent from tripping.

If the 2.5V dual is not used, its feedback line, pin 15, must be connected to 5V dual as shown in Figure 4, to prevent an overcurrent trip.

UVLO

If the +5V standby is below approximately 4.5V, the RC5060 will leave off or turn off all outputs. Similar comments apply to the +12V main at 7.5V. The +5V standby UVLO has approximately 0.5V hysteresis, the +12V main UVLO 1V.

Power Good

The Power Good is an open collector that pulls low if any of the outputs are less than 80% of nominal.

Over Temperature

The RC5060 is capable of sourcing substantial current, 200mA minimum to the RAMBUS transistor's base during S0, 144mA to the RAMBUS line during S3, and 100mA to SDRAM during S3. As a result, there can be heavy power dissipation in the IC. While the RC5060 is designed to accept this power dissipation, any overloading of outputs can cause excessive heating. If the RC5060 die temperature exceeds about 150°, all outputs are shut off. Outputs remain off until the die temperature returns to its safe area.

Transistor Selection

External transistor selection depends on usage, differing for the linear regulators and the switches.

The MOSFET switches, Ql, Q3, Q5 and Q6 should be sized based on regulation requirements and power dissipation. Since the ATX outputs are ±5%, the outputs driven from them must be wider. As an example, if we want to hold 3.3V SDRAM to -10%, we can drop only 5% = 165mV across Q1. At 4.8A, this means Ql must have a maximum $R_{DS,on}$ of 165mV/4.8A = 34mΩ, including tolerance and self-heating effects. We thus choose a Fairchild FDS4410Y, which has 20mΩ maximum $R_{DS,\ on}$ at 4.5V V_{GS} at 25°C. We can estimate power dissipation as $(4.8A)^2 * 20m\Omega = 460mW$, which should be acceptable for this package. Similar calculations apply to the other MOSFET switches.

Q4 is a MOSFET functioning as a linear regulator. Since it delivers only 500mA, it is easy to select a MOSFET, it need only have $R_{DS,on}$ less than (5V–5%–3.3V)/500mA = 2.9Ω. We select the Fairchild NDS9956A which has maximum $R_{DS,\ on}$ of 110mΩ at 4.5V V_{GS} at 25°C. Power dissipation will be a maximum of $(0.5A)^2 * 110m\Omega = 27mW$.

Q2 is an NPN bipolar functioning as a linear regulator. As already discussed, it must have a $V_{CE,sat}$ lower than 635mV at I_E = 2A and I_B = 200mA. Its power dissipation can be as high as (3.3V + 5%–2.5V) * 2A = l.9W.

Output Capacitor Selection

Output capacitor selection depends on whether the line has overlap time or not.

For both the 5V dual and the 2.5V dual, there is guaranteed overlap time between when one source is turned on and the other source turned off. For these outputs, the output capacitor is not needed to hold up the supply, but only for noise filtering and to respond to transient loading.

The 3.3V dual and 3.3V SDRAM outputs have deadtime between when one source is turned off and the other source turned on. During the time when both are off, the output current must be supplied by the output capacitor. Mitigating this, it must be realized that the system will be designed in such a way that the current has gone to its sleep value before the transition occurs. For example, the 3.3V dual has a sleep current of 500mA maximum. Maximum deadtime is 6µsec, and so charge depletion is 500mA * 6µsec = 3µC. Suppose that we have a total of 8% drop due to the source tolerance and the MOSFET drop, and we are trying to hold 10% regulation. The remaining 2% = 66mV implies a minimum capacitance of 3µC/66mV = 45µF.

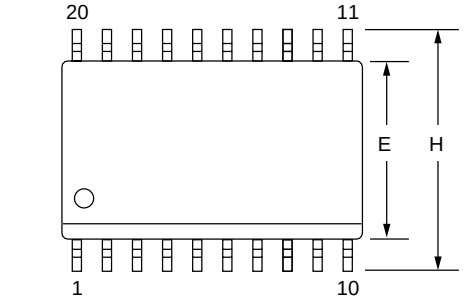
Mechanical Dimensions

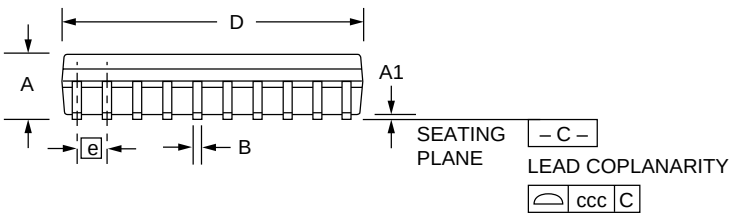
20 Lead SOIC

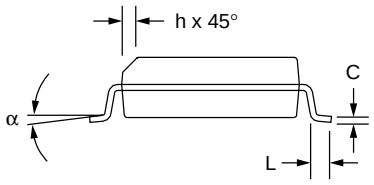
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.496	.512	12.60	13.00	2
E	.291	.299	7.40	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.029	0.25	0.75	
L	.016	.050	0.40	1.27	3
N	20		20		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Preliminary Specification

Ordering Information

Product Number	Package
RC5060M	20 pin SOIC

Preliminary Specification

RC5061

High Performance Programmable Synchronous DC-DC Controller for Multi-Voltage Platforms

Features

- Programmable output for Vcore from 1.3V to 3.5V using an integrated 5-bit DAC
- Controls adjustable linears for Vtt (1.5V), and Vclock (2.5V)
- Meets VRM specification with as few as 5 capacitors
- Meets 1.550V +40/-70mV over initial tolerance, temperature and transients
- Remote sense
- Active Droop (Voltage Positioning)
- Drives N-Channel MOSFETs
- Overcurrent protection using MOSFET sensing
- 85% efficiency typical at full load
- Integrated Power Good and Enable/Soft Start functions
- 20 pin SOIC package

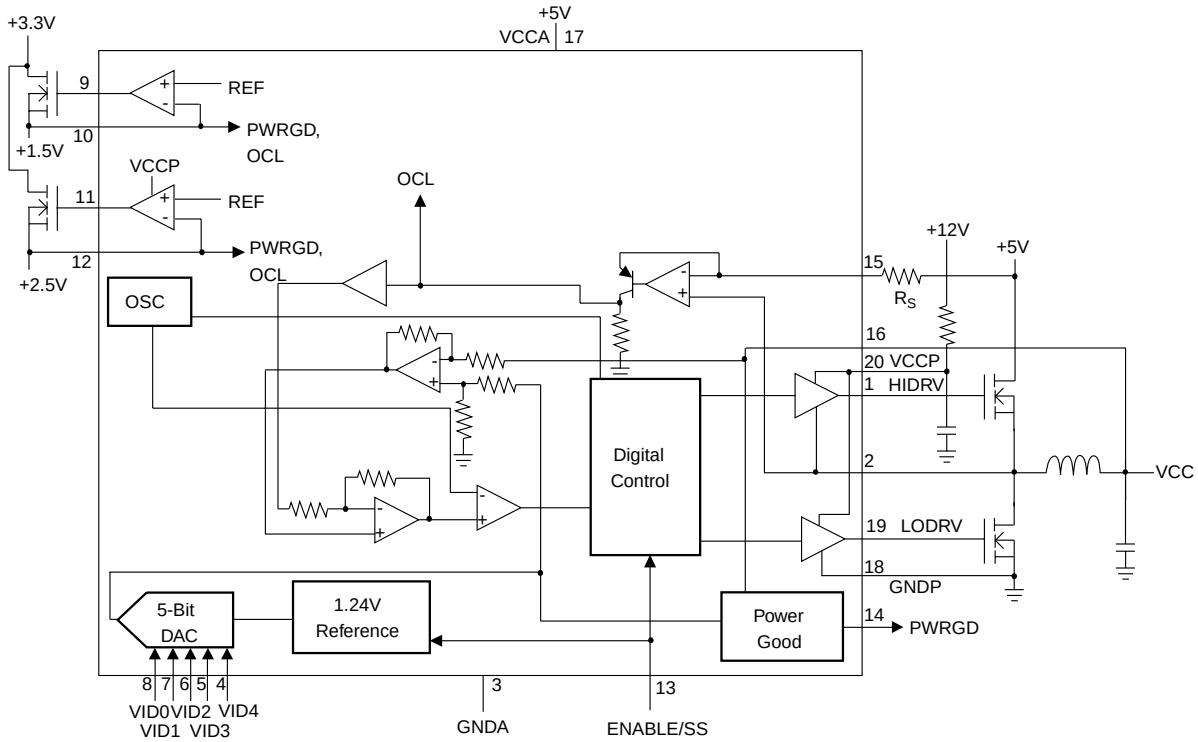
Applications

- Power supply for Pentium® III Camino Platform
- Power supply for Pentium III Whitney Platform
- VRM for Pentium III processor
- Programmable multi-output power supply

Description

The RC5061 is a synchronous mode DC-DC controller IC which provides a highly accurate, programmable set of output voltages for multi-voltage platforms such as the Intel Camino, and provides a complete solution for the Intel Whitney and other high-performance processors. The RC5061 features remote voltage sensing, independently adjustable current limit, and Active Droop for optimal converter transient response. The RC5061 uses a 5-bit D/A converter to program the output voltage from 1.3V to 3.5V. The RC5061 uses a high level of integration to deliver load currents in excess of 16A from a 5V

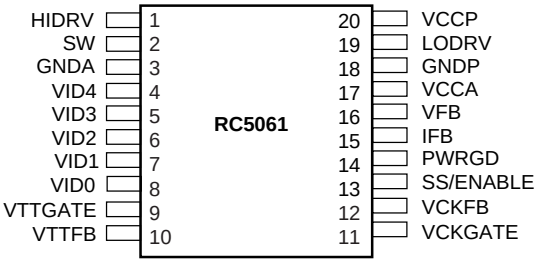
Block Diagram



Preliminary Specification

source with minimal external circuitry. Synchronous-mode operation offers optimum efficiency over the entire specified output voltage range. An on-board precision low TC reference achieves tight tolerance voltage regulation without expensive external components, while Active Droop permits exact tailoring of voltage for the most demanding load transients. The RC5061 includes linear regulator controllers for Vtt termination (1.5V), and Vclock (2.5V), each adjustable with an external divider. The RC5061 also offers integrated functions including Power Good, Output Enable/Soft Start and current limiting, and is available in a 20 pin SOIC package.

Pin Assignments



Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	HIDRV	**High Side FET Driver.** Connect this pin through a resistor to the gate of an N-channel MOSFET. The trace from this pin to the MOSFET gate should be <0.5".
2	SW	**High side Driver Source and Low side Driver Drain Switching Node.** Together with DROOP and ILIM pins allows FET sensing for Vcc current.
3	GNDA	**Analog Ground.** Return path for low power analog circuitry. This pin should be connected to a low impedance system ground plane to minimize ground loops.
4-8	VID0-4	**Voltage Identification Code Inputs.** These open collector/TTL compatible inputs will program the output voltage over the ranges specified in Table 2. Pull-up resistors are internal to the controller.
9	VTTGATE	**Gate Driver for VTT Transistor.** For 1.5V output.
10	VTTFB	**Voltage Feedback for VTT.**
11	VCKGATE	**Gate Driver for VCK Transistor.** For 2.5V output.
12	VCKFB	**Voltage Feedback for VCK.**
13	ENABLE/SS	**Output Enable.** A logic LOW on this pin will disable all outputs. An internal current source allows for open collector control. This pin also doubles as soft start for all outputs.
14	PWRGD	**Power Good Flag.** An open collector output that will be logic LOW if any output voltage is not within ±12% of the nominal output voltage setpoint.
15	IFB	**Vcc Current Feedback.** Pin 15 is used in conjunction with pin 2 as the input for the Vcc current feedback control loop. Layout of these traces is critical to system performance. See Application Information for details.
16	VFB	**Vcc Voltage Feedback.** Pin 16 is used as the input for the Vcc voltage feedback control loop. See Application Information for details regarding correct layout.
17	VCCA	**Analog VCC.** Connect to system 5V supply and decouple with a 0.1µF ceramic capacitor.
18	GNDP	**Power Ground.** Return pin for high currents flowing in pin 20 (VCCP).
19	LODRV	**Vcc Low Side FET Driver.** Connect this pin through a resistor to the gate of an N-channel MOSFET for synchronous operation. The trace from this pin to the MOSFET gate should be <0.5".
20	VCCP	**Power VCC.** For all FET drivers. Connect to system 12V supply through a 33Ω, and decouple with a 1µF ceramic capacitor.

Preliminary Specification

Absolute Maximum Ratings

Supply Voltages VCCA, VCCP to GND	13.5V
Voltage Identification Code Inputs, VID0-VID4	VCCA
All Other Pins	13.5V
Junction Temperature, T_J	150°C
Storage Temperature	-65 to 150°C
Lead Soldering Temperature, 10 seconds	300°C
Thermal Resistance Junction-to-ambient, Θ_{JA}[1]	75°C/W

Note:

1. Component mounted on demo board in free air.

Recommended Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Voltage VCCA		4.75	5	5.25	V
Input Logic HIGH		2.0			V
Input Logic LOW				0.8	V
Ambient Operating Temperature		0		70	°C
Output Driver Supply, VCCP		10.8	12	13.2	V

Electrical Specifications

(V_{CCA} = 5V, V_{CCP} = 12V, V_{OUT} = 2.0V, and T_A = +25°C using circuit in Figure 1 unless otherwise noted.)
The • denotes specifications which apply over the full operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
VCC Regulator						
Output Voltage	See Table 1	•	1.3		3.5	V
Output Current				18		A
Initial Voltage Setpoint	I_{LOAD} = 0.8A, V_{OUT} = 2.400V V_{OUT} = 2.000V V_{OUT} = 1.550V		2.397 2.000 1.550	2.424 2.020 1.565	2.454 2.040 1.580	V V V
Output Temperature Drift	T_A = 0 to 70°C, V_{OUT} = 2.000V V_{OUT} = 1.550V	• •		+8 +6		mV mV
Line Regulation	V_{IN} = 4.75V to 5.25V	•		-4		mV/V
Internal Droop Impedance	I_{LOAD} = 0.8A to 12.5A		13.0	14.4	15.8	KΩ
Maximum Droop				60		mV
Output Ripple	20MHz BW, I_{LOAD} = 18A			11		mVpk
Total Output Variation, Steady State[1]	V_{OUT} = 2.000V V_{OUT} = 1.550V[3]	• •	1.940 1.480		2.070 1.590	V
Total Output Variation, Transient[2]	I_{LOAD} = 0.8A to 18A, V_{OUT} = 2.000V V_{OUT} = 1.550V[3]	• •	1.900 1.480		2.100 1.590	V
Short Circuit Detect Current		•	45	50	60	µA
Efficiency	I_{LOAD} = 18A, V_{OUT} = 2.0V			85		%
Output Driver Rise & Fall Time	See Figure 3			50		nsec
Output Driver Deadtime	See Figure 3			50		nsec
Duty Cycle			0		100	%

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Electrical Specifications (Continued)

(V_{CCA} = 5V, V_{CCP} = 12V, V_{OUT} = 2.0V, and T_A = +25°C using circuit in Figure 1 unless otherwise noted.)
The • denotes specifications which apply over the full operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
5V UVLO		•	3.74	4	4.26	V
12V UVLO		•	7.65	8.5	9.35	V
Soft Start Current		•	5	10	17	µA
VTT Linear Regulator						
Output Voltage	$I_{LOAD} \leq 2A$	•	1.425	1.5	1.575	V
Under Voltage Trip Level	Over Current			80		$\%V_O$
VCLK Linear Regulator						
Output Voltage	$I_{LOAD} \leq 2A$	•	2.375	2.5	2.625	V
Under Voltage Trip Level	Over Current			80		$\%V_O$
Common Functions						
Oscillator Frequency		•	255	310	345	kHz
PWRGD Threshold	Logic HIGH, All Outputs Logic LOW, Any Output	• •	93 88		107 112	$\%V_{OUT}$
Linear Regulator Under Voltage Delay Time	Over Current			30		µsec

Notes:

1. Steady State Voltage Regulation includes Initial Voltage Setpoint, Droop, Output Ripple and Output Temperature Drift and is measured at the converter's VFB sense point.
2. As measured at the converter's VFB sense point. For motherboard applications, the PCB layout should exhibit no more than 0.5mΩ trace resistance between the converter's output capacitors and the CPU. Remote sensing should be used for optimal performance.
3. Using the VFB pin for remote sensing of the converter's output at the load, the converter will be in compliance with Intel's VRM 8.4 specification of +50, –80mV. If Intel specifications on maximum plane resistance from the converter's output capacitors to the CPU are met, the specification of +40, –70mV at the capacitors will also be met.

Table 1. Output Voltage Programming Codes

VID4	VID3	VID2	VID1	VID0	Nominal V_{OUT}
0	1	1	1	1	1.30V
0	1	1	1	0	1.35V
0	1	1	0	1	1.40V
0	1	1	0	0	1.45V
0	1	0	1	1	1.50V
0	1	0	1	0	1.55V
0	1	0	0	1	1.60V
0	1	0	0	0	1.65V
0	0	1	1	1	1.70V
0	0	1	1	0	1.75V
0	0	1	0	1	1.80V
0	0	1	0	0	1.85V
0	0	0	1	1	1.90V
0	0	0	1	0	1.95V
0	0	0	0	1	2.00V
0	0	0	0	0	2.05V
1	1	1	1	1	2.0V
1	1	1	1	0	2.1V
1	1	1	0	1	2.2V
1	1	1	0	0	2.3V
1	1	0	1	1	2.4V
1	1	0	1	0	2.5V
1	1	0	0	1	2.6V
1	1	0	0	0	2.7V
1	0	1	1	1	2.8V
1	0	1	1	0	2.9V
1	0	1	0	1	3.0V
1	0	1	0	0	3.1V
1	0	0	1	1	3.2V
1	0	0	1	0	3.3V
1	0	0	0	1	3.4V
1	0	0	0	0	3.5V

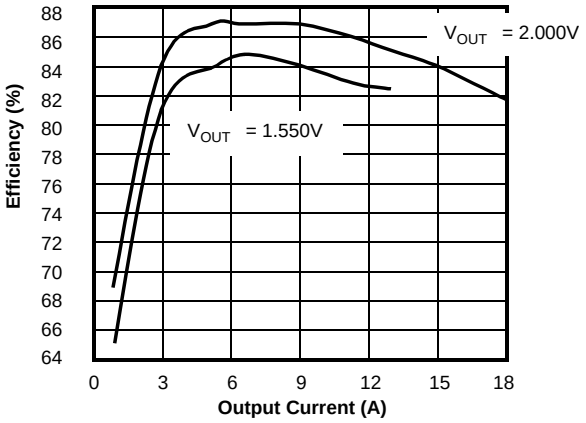
Note:

1. 0 = processor pin is tied to GND.
   1 = processor pin is open.

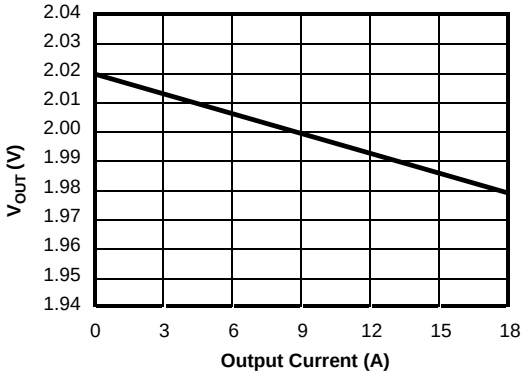
Typical Operating Characteristics

(V_{CCA} = 5V, V_{CCP} = 12V, and T_A = +25°C using circuits in Figure 1, unless otherwise noted.)

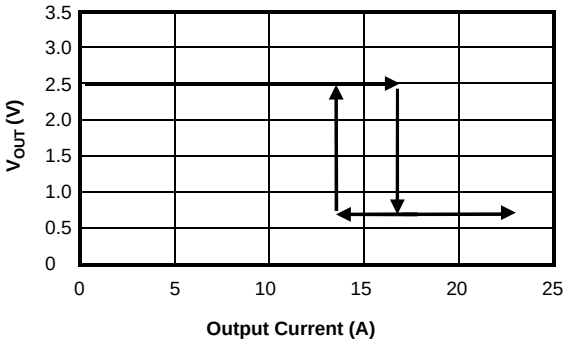
V_{CPU} Efficiency vs. Output Current



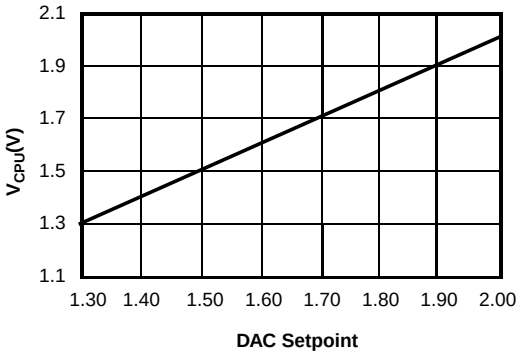
Droop, V_{CPU} = 2.0V, R_D = 8K Ω



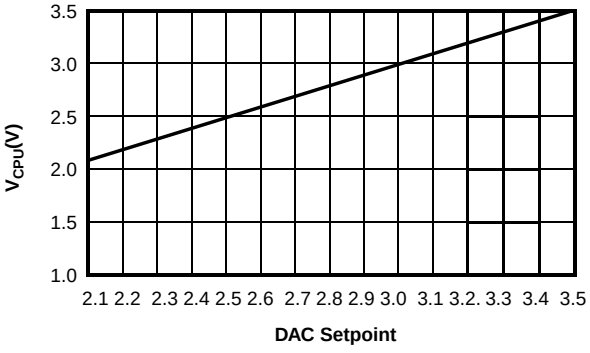
CPU Output Voltage vs. Output Current



Output Programming, VID4 = 0



Output Programming, VID4 = 1



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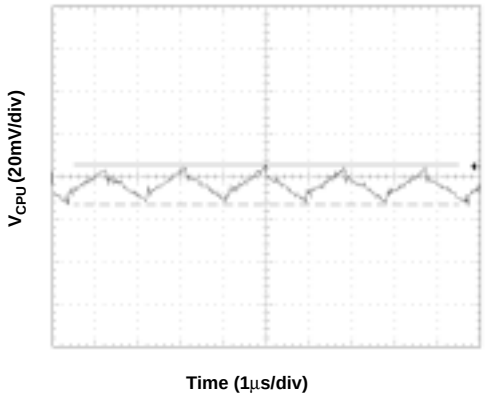
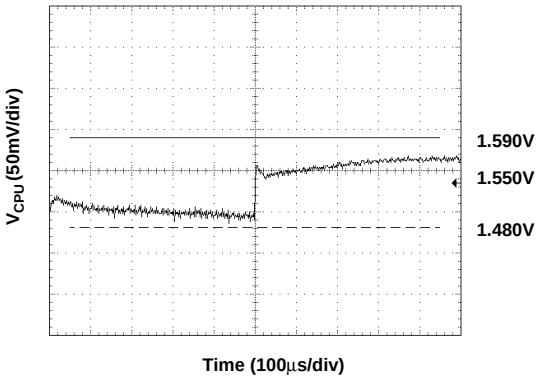
Typical Operating Characteristics (continued)

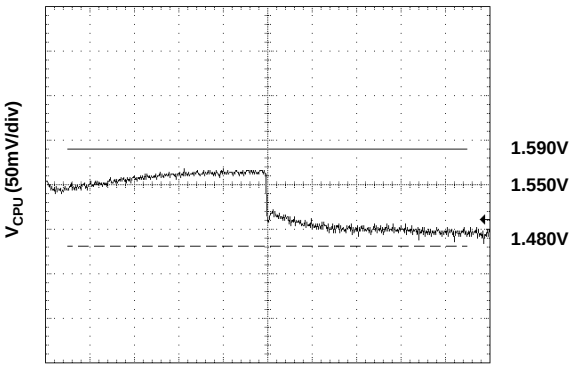
Output Ripple, 2.0V @ 18A



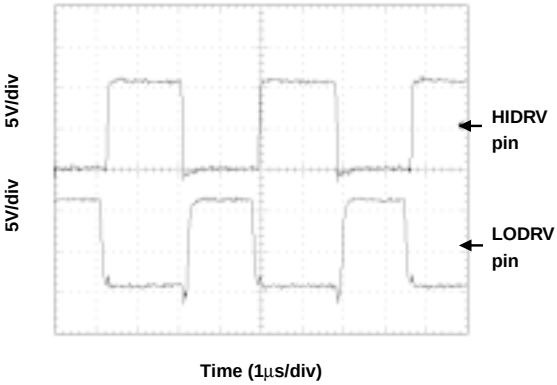
Transient Response, 12.5A to 0.5A



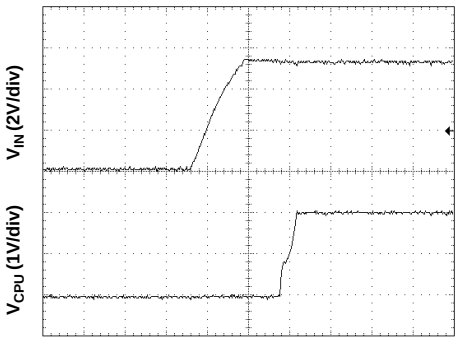
Transient Response, 0.5A to 12.5A



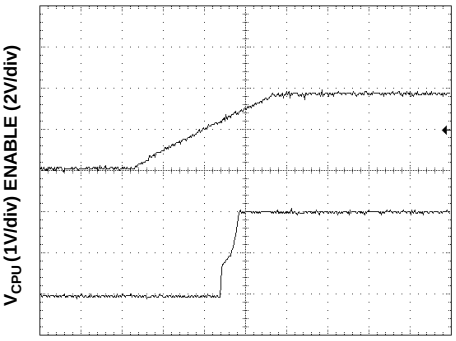
Switching Waveforms, 18A Load



Output Startup, System Power-up

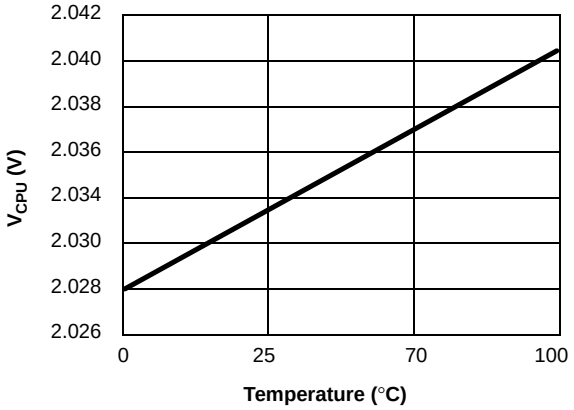


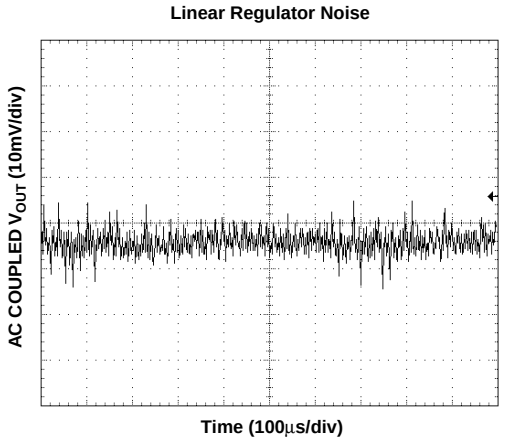
Output Startup from Enable



Preliminary Specification

Typical Operating Characteristics (continued)





Application Circuit

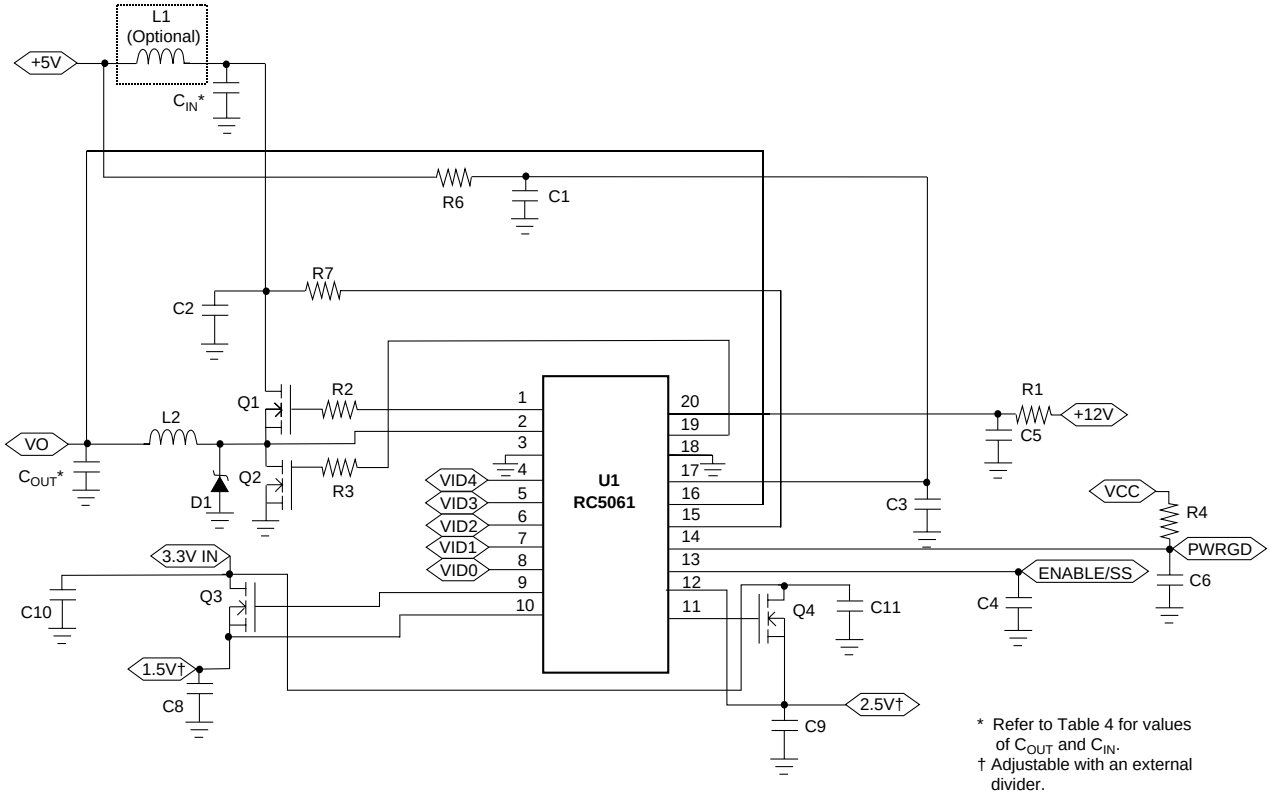


Figure 1. Application Circuit for Katmai/Camino/BX/ZX Motherboards
(Worst Case Analyzed! See Appendix for Details*)*

Preliminary Specification

Table 2. RC5061 Application Bill of Materials for Intel Katmai/Camino/BX/ZX Motherboards

(Components based on Worst Case Analysis—See Appendix for Details)

Reference	Manufacturer Part #	Quantity	Description	Requirements/Comments
C1	AVX TAJB475M010R5	1	4.7µF, 10V Capacitor	
C2, C5	Panasonic ECU-V1C105ZFX	2	1µF, 16V Capacitor	
C3-4,C6	Panasonic ECU-V1H104ZFX	3	100nF, 50V Capacitor	
C8-9	Sanyo 6MV1000FA	2	1000µF, 6.3V Electrolytic	
C10-11	Any	2	22µF, 6.3V Capacitor	Low ESR
C_{IN}	Sanyo 10MV1200GX	*	1200µF, 10V Electrolytic	I_{RMS} = 2A
C_{OUT}	Sanyo 6MV1500GX	*	1500µF, 6.3V Electrolytic	ESR ≤ 44mΩ
D1	Motorola MBRD835L	1	8A Schottky Diode	
L1	Any	Optional	2.5µH, 8A Inductor	DCR ~ 10mΩ See Note 1.
L2	Any	1	1.3µH, 20A Inductor	DCR ~ 2mΩ
Q1	Fairchild FDB6030L	1	N-Channel MOSFET	$R_{DS(ON)}$ = 20mΩ @ V_{GS} = 4.5V See Note 2.
Q2	Fairchild FDB7030BL	1	N-Channel MOSFET	$R_{DS(ON)}$ = 10mΩ @ V_{GS} = 4.5V See Note 2.
Q3-4	Fairchild FDB4030L	2	N-Channel MOSFET	
R1	Any	1	33Ω	
R2-3	Any	2	4.7Ω	
R4	Any	1	10KΩ	
R6	Any	1	10Ω	
R7	Any	1	*	
U1	Fairchild RC5061M	1	DC/DC Controller	

Notes:

1. Inductor L1 is recommended to isolate the 5V input supply from noise generated by the MOSFET switching, and to comply with Intel dI/dt requirements. L1 may be omitted if desired.
2. For 17.4A designs using the TO-220 MOSFETs, heatsinks with thermal resistance Θ_{SA} < 20°C/Ω should be used. For designs using the TO-263 MOSFETs, adequate copper area should be used. For details and a spreadsheet on MOSFET selections, refer to Applications Bulletins AB-8 and AB-15.

*Refer to table 4 for values.

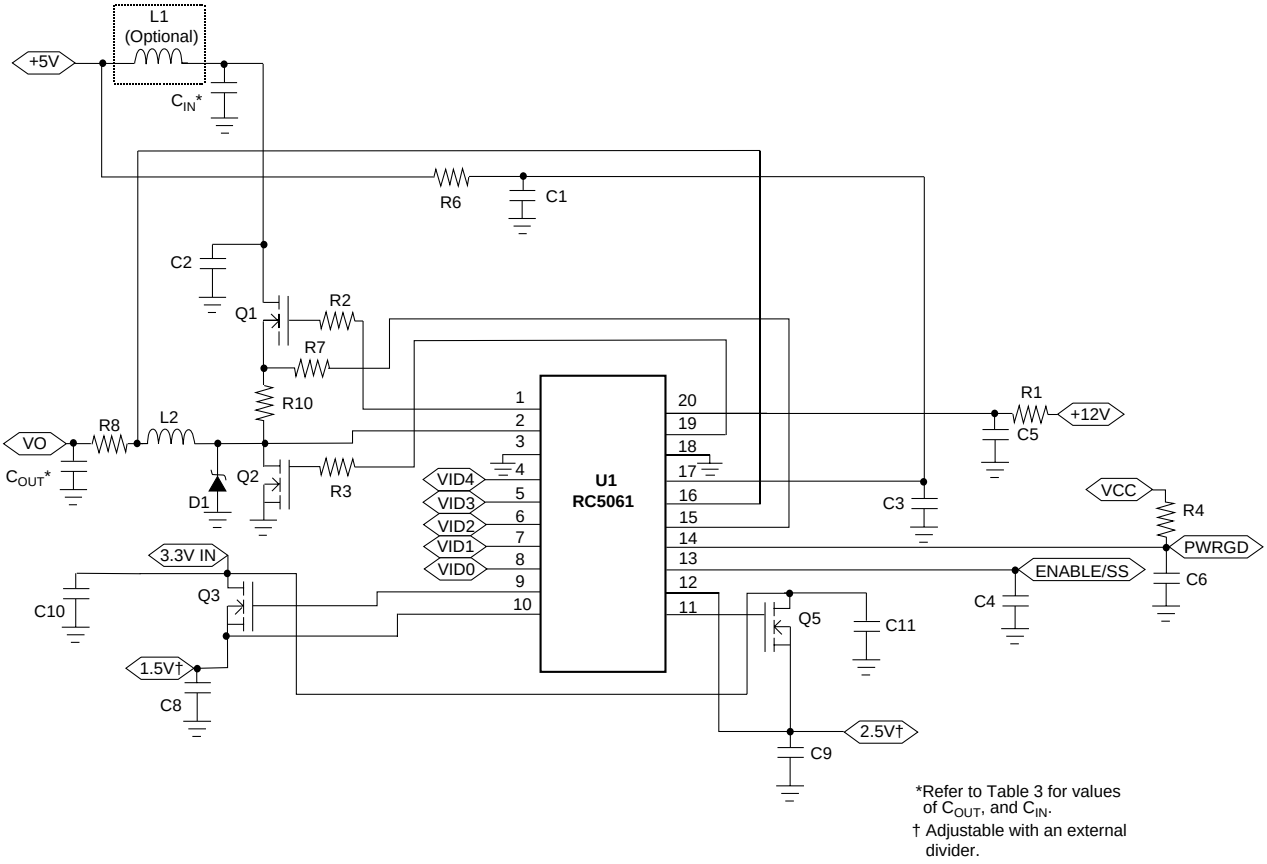


Figure 2. Application Circuit for Coppermine/Camino Motherboards
(Typical Design)

Table 3. RC5061 Application Bill of Materials for Intel Coppermine/Camino Motherboards
(Typical Design)

Reference	Manufacturer Part #	Quantity	Description	Requirements/Comments
C1	AVX TAJB475M010R5	1	4.7µF, 10V Capacitor	
C2, C5	Panasonic ECU-V1C105ZFX	2	1µF, 16V Capacitor	
C3-4,C6	Panasonic ECU-V1H104ZFX	3	100nF, 50V Capacitor	
C8-9	Sanyo 6MV1000FA	2	1000µF, 6.3V Electrolytic	
C10-11	Any	2	22µF, 6.3V Capacitor	Low ESR
C_{IN}	Sanyo 10MV1200GX	3	1200µF, 10V Electrolytic	I_{RMS} = 2A
C_{OUT}	Sanyo 6MV1500GX	12	1500µF, 6.3V Electrolytic	ESR ≤ 44mΩ
D1	Motorola MBRD835L	1	8A Schottky Diode	
L1	Any	Optional	2.5µH, 5A Inductor	DCR ~ 10mΩ See Note 1.
L2	Any	1	1.3µH, 15A Inductor	DCR ~ 3mΩ
Q1	Fairchild FDB6030L	1	N-Channel MOSFET	$R_{DS(ON)}$ = 20mΩ @ V_{GS} = 4.5V See Note 2.
Q2	Fairchild FDB7030BL	1	N-Channel MOSFET	$R_{DS(ON)}$ = 10mΩ @ V_{GS} = 4.5V See Note 2.
Q3-4	Fairchild FDB4030L	2	N-Channel MOSFET	
R1	Any	1	33Ω	
R2-3	Any	2	4.7Ω	
R4	Any	1	10KΩ	
R6	Any	1	10Ω	
R7	Any	1	6.24KΩ	
R8	N/A	1	30mΩ	PCB Trace Resistor
U1	Fairchild RC5061M	1	DC/DC Controller	

Notes:

1. Inductor L1 is recommended to isolate the 5V input supply from noise generated by the MOSFET switching, and to comply with Intel dI/dt requirements. L1 may be omitted if desired.
2. For 12.5A designs using the TO-220 MOSFETs, heatsinks with thermal resistance Θ_{SA} < 20°C/Ω should be used. For designs using the TO-263 MOSFETs, adequate copper area should be used. For details and a spreadsheet on MOSFET selections, refer to Applications Bulletins AB-8 and AB-15.

Application Circuit Summary

Table 4 summarizes the worst-case design schematics presented in this section. The basic choices are: A) The processor, B) the chipset used, and C) the use or not of a sense resistor. Depending on board layout and component selection, it may be possible to use fewer output capacitors than shown here. For configurations not shown in this datasheet, consult the Appendix for selection of component values.

Table 4. Recommended Values for CPU-based Applications

Processor	Chipset	C_{IN}	C_{OUT}*	R5, R7 (KΩ)
Coppermine	Whitney	3	4	8.45
Katmai	Camino	4	6	13.0
Mendocino	Whitney	4	5	11.3
Katmai	BX	5	6	11.8

*Output capacitance requirements depend critically on layout and processor type. Consult Application Bulletin AB-14 for details. See the Appendix to this datasheet for the method of calculation of these components. Pin 4 must be used to remote sense the voltage at the processor to achieve the specified performance.

Test Parameters

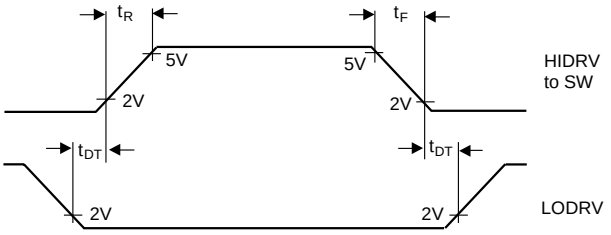


Figure 3. Ouput Drive Timing Diagram

Application Information

The RC5061 Controller

The RC5061 is a programmable synchronous DC-DC controller IC. When designed around the appropriate external components, the RC5061 can be configured to deliver more than 16A of output current, as appropriate for the Katmai and Coppermine and other processors. The RC5061 functions as a fixed frequency PWM step down regulator.

Main Control Loop

Refer to the RC5061 Block Diagram on page 1. The RC5061 implements “summing mode control”, which is different from both classical voltage-mode and current-mode control. It provides superior performance to either by allowing a large converter bandwidth over a wide range of output loads.

The control loop of the regulator contains two main sections: the analog control block and the digital control block. The analog section consists of signal conditioning amplifiers feeding into a comparator which provides the input to the digital control block. The signal conditioning section accepts input from the DROOP (current feedback) and VFB (voltage feedback) pins and sets up two controlling signal paths. The first, the voltage control path, amplifies the difference between the VFB signal and the reference voltage from the DAC and presents the output to one of the summing amplifier inputs. The second, current control path, takes the difference between the DROOP and SW pins when the high-side MOSFET is on, reproducing the voltage across the MOSFET and thus the input current; it presents the resulting signal to another input of the summing amplifier. These two signals are then summed together. This output is then presented to a comparator looking at the oscillator ramp, which provides the main PWM control signal to the digital control block.

The digital control block takes the analog comparator input and the main clock signal from the oscillator to provide the appropriate pulses to the HIDRV and LODRV output pins. These two outputs control the external power MOSFETs.

There is an additional comparator in the analog control section whose function is to set the point at which the RC5061 current limit comparator disables the output drive signals to the external power MOSFETs.

High Current Output Drivers

The RC5061 contains two identical high current output drivers that utilize high speed bipolar transistors in a push-pull configuration. The drivers’ power and ground are separated from the chip’s power and ground for switching noise immunity. The power supply pin, VCCP, is supplied from an external 12V source through a series 33Ω resistor. The resulting voltage is sufficient to provide the gate to source drive to the external MOSFETs required in order to achieve a low $R_{DS,ON}$.

Internal Voltage Reference

The reference included in the RC5061 is a precision band-gap voltage reference. Its internal resistors are precisely trimmed to provide a near zero temperature coefficient (TC). Based on the reference is the output from an integrated 5-bit DAC. The DAC monitors the 5 voltage identification pins, VID0-4. When the VID4 pin is at logic HIGH, the DAC scales the reference voltage from 2.0V to 3.5V in 100mV increments. When VID4

is pulled LOW, the DAC scales the reference from 1.30V to 2.05V in 50mV increments. All VID codes are available, including those below 1.80V.

Power Good (PWRGD)

The RC5061 Power Good function is designed in accordance with the Pentium III DC-DC converter specifications and provides a continuous voltage monitor on the VFB pin. The circuit compares the VFB signal to the VREF voltage and outputs an active-low interrupt signal to the CPU should the power supply voltage deviate more than ±12% of its nominal setpoint. The Power Good flag provides no other control function to the RC5061.

Output Enable/Soft Start (ENABLE/SS)

The RC5061 will accept an open collector/TTL signal for controlling the output voltage. The low state disables the output voltage. When disabled, the PWRGD output is in the low state.

Even if an enable is not required in the circuit, this pin should have attached a capacitor (typically 100nF) to softstart the switching.

Over-Voltage Protection

The RC5061 constantly monitors the output voltage for protection against over-voltage conditions. If the voltage at the VFB pin exceeds the selected program voltage, an over-voltage condition is assumed and the RC5061 disables the output drive signal to the external high-side MOSFET. The DC-DC converter returns to normal operation after the output voltage returns to normal levels.

Oscillator

The RC5061 oscillator section uses a fixed frequency of operation of 300KHz.

Design Considerations and Component Selection

Additional information on design and component selection may be found in Fairchild's Application Note 57.

MOSFET Selection

This application requires N-channel Logic Level Enhancement Mode Field Effect Transistors. Desired characteristics are as follows:

- Low Static Drain-Source On-Resistance, $R_{DS,ON} < 20m\Omega$ (lower is better)
- Low gate drive voltage, $V_{GS} = 4.5V$ rated
- Power package with low Thermal Resistance
- Drain-Source voltage rating > 15V.

The on-resistance ($R_{DS,ON}$) is the primary parameter for MOSFET selection. The on-resistance determines the power dissipation within the MOSFET and therefore significantly affects the efficiency of the DC-DC Converter. For details and a spreadsheet on MOSFET selection, refer to Applications Bulletin AB-8.

Inductor Selection

Choosing the value of the inductor is a tradeoff between allowable ripple voltage and required transient response. The system designer can choose any value within the allowed minimum to maximum range in order to either minimize ripple or maximize transient performance. The first order equation (close approximation) for minimum inductance is:

$$L_{min} = \frac{(V_{in} - V_{out})}{f} \times \frac{V_{out}}{V_{in}} \times \frac{ESR}{V_{ripple}}$$

where:
V_{in} = Input Power Supply
V_{out} = Output Voltage
f = DC/DC converter switching frequency
ESR = Equivalent series resistance of all output capacitors in parallel
V_{ripple} = Maximum peak to peak output ripple voltage budget.

The first order equation for maximum allowed inductance is:

$$L_{max} = 2C_O \frac{(V_{in} - V_{out})\, D_m\, V_{tb}}{I_{pp}^2}$$

where:
C_o = The total output capacitance
I_{pp} = Maximum to minimum load transient current
V_{tb} = The output voltage tolerance budget allocated to load transient
D_m = Maximum duty cycle for the DC/DC converter (usually 95%).

Some margin should be maintained away from both L_{min} and L_{max}. Adding margin by increasing L almost always adds expense since all the variables are predetermined by system performance except for C_O, which must be increased to increase L. Adding margin by decreasing L can be done by purchasing capacitors with lower ESR. The RC5061 provides significant cost savings for the newer CPU systems that typically run at high supply current.

RC5061 Short Circuit Current Characteristics

The RC5061 protects against output short circuit on the core supply by turning off both the high-side and low-side MOSFETs and resetting softstart. The short circuit limit is set with the R_S resistor, as given by the formula

$$R_S = \frac{I_{SC} * R_{DS,\,on}}{I_{Detect}}$$

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with $I_{Detect} \approx 50\mu A$, I_{SC} is the desired current limit, and $R_{DS,on}$ the high-side MOSFET's on resistance. Remember to make the R_S large enough to include the effects of initial tolerance and temperature variation on the MOSFET's $R_{DS,on}$. Alternately, use of a sense resistor in series with the source of the MOSFET eliminates this source of inaccuracy in the current limit. The value of R_S should be less than 10KΩ. If a greater value is necessary, a lower $R_{DS,on}$ MOSFET should be used instead.

As an example, Figure 4 shows the typical characteristic of the DC-DC converter circuit with an FDB6030L high-side MOSFET (R_{DS} = 20mΩ maximum at 25°C * 1.25 at 75°C = 25mΩ) and a 8.2KΩ R_S.

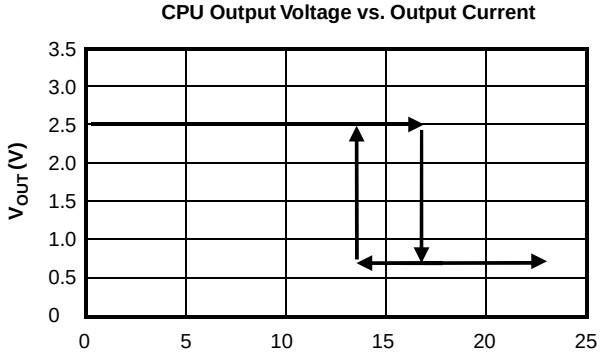


Figure 4. RC5061 Short Circuit Characteristic

The converter exhibits a normal load regulation characteristic until the voltage across the MOSFET exceeds the internal short circuit threshold of 50µA * 8.2KΩ = 410mV, which occurs at 410mV/25mΩ = 16.4A. (Note that this current limit level can be as high as 410mV/15mΩ = 27A, if the MOSFET has typical $R_{DS,on}$ rather than maximum, and is at 25°C).

At this point, the internal comparator trips and signals the controller to discharge softstart. This causes a drastic reduction in the output voltage as the load regulation collapses into the short circuit control mode. With a 40mΩ output short, the voltage is reduced to 16.4A * 40mΩ = 650mV. The output voltage does not return to its nominal value until the output current is reduced to a value within the safe operating ranges for the DC-DC converter.

If any of the linear regulator outputs are loaded heavily enough that their output voltage drops below 80% of nominal for > 30µsec, all RC5061 outputs, including the switcher, are shut off and remain off until power is recycled.

Schottky Diode Selection

The application circuit of Figure 1 shows a Schottky diode, D1, which is used as a free-wheeling diode to assure that the body-diode in Q2 does not conduct when the upper MOSFET is turning off and the lower MOSFET is turning on. It is undesirable for this diode to conduct because its high forward voltage drop and long reverse recovery time degrades efficiency, and so the Schottky provides a shunt path for the current. Since this time duration is very short, the selection criterion for the diode is that the forward voltage of the Schottky at the output current should be less than the forward voltage of the MOSFET's body diode.

Output Filter Capacitors

The output bulk capacitors of a converter help determine its output ripple voltage and its transient response. It has already been seen in the section on selecting an inductor that the ESR helps set the minimum inductance, and the capacitance value helps set the maximum inductance. For most converters, however, the number of capacitors required is determined by the transient response and the output ripple voltage, and these are determined by the ESR and not the capacitance value. That is, in order to achieve the necessary ESR to meet the transient and ripple requirements, the capacitance value required is already very large.

The most commonly used choice for output bulk capacitors is aluminum electrolytics, because of their low cost and low ESR. The only type of aluminum capacitor used should be those that have an ESR rated at 100kHz. Consult Application Bulletin AB-14 for detailed information on output capacitor selection.

The output capacitance should also include a number of small value ceramic capacitors placed as close as possible to the processor; 0.1µF and 0.01µF are recommended values.

Input Filter

The DC-DC converter design may include an input inductor between the system +5V supply and the converter input as shown in Figure 5. This inductor serves to isolate the +5V supply from the noise in the switching portion of the DC-DC converter, and to limit the inrush current into the input capacitors during power up. A value of 2.5µH is recommended.

It is necessary to have some low ESR aluminum electrolytic capacitors at the input to the converter. These capacitors deliver current when the high side MOSFET switches on. Figure 5 shows 3 x 1000µF, but the exact number required will vary with the speed and type of the processor. For the top speed Katmai and Coppermine, the capacitors should be rated to take 9A and 6A of ripple current respectively. Capacitor ripple current rating is a function of temperature, and so the manufacturer should be contacted to find out the ripple current rating at the expected operational temperature. For details on the design of an input filter, refer to Applications Bulletin AB-15.

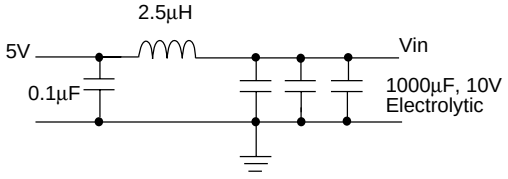


Figure 5. Input Filter

Active Droop

The RC5061 includes active droop; as the ouptut current increases, the output voltage drops. This is done in order to allow maximum headroom for transient response of the converter. The current is sensed by measuring the voltage across the high-side MOSFET during its on time. Note that this makes the droop dependent on the temperature of the MOSFET. However, when the formula given for selecting R_S (current limit) is used, there is a maximum droop possible (-40mV), and when this value is reached, additional drop across the MOSFET will not cause any increase in droop—until current limit is reached.

Additional droop can be added to the active droop using a discrete resistor (typically a PCB trace) outside the control loop, as shown in Figure 2. This is typically only required for the most demanding applications, such as for the next generation Intel processor (tolerance = +40/-70mV), as shown in Figure 2.

Remote Sense

The RC5061 offers remote sense of the output voltage to minimize the output capacitor requirements of the converter. It is highly recommended that the remote sense pin, Pin 16, be tied directly to the processor power pins, so that the effects of power plane impedance are eliminated. Further details on use of the remote sense feature of the RC5061 may be found in Applications Bulletin AB-24.

Adjusting the Linear Regulators' Output Voltages

Any or all of the linear regulators' outputs may be adjusted high to compensate for voltage drop along traces, as shown in Figure 6.

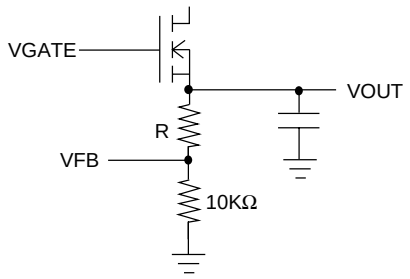


Figure 6. Adjusting the Output Voltage of the Linear Regulator

The resistor value should be chosen as

$$R = 10K\Omega * \left(\frac{V_{out}}{V_{nom}} - 1 \right)$$

For example, to get the V_{TT} voltage to be 1.55V instead of 1.50V, use R = 10KΩ * [(1.55/1.50) – 1] = 333Ω.

PCB Layout Guidelines

- Placement of the MOSFETs relative to the RC5061 is critical. Place the MOSFETs such that the trace length of the HIDRV and LODRV pins of the RC5061 to the FET gates is minimized. A long lead length on these pins will cause high amounts of ringing due to the inductance of the trace and the gate capacitance of the FET. This noise radiates throughout the board, and, because it is switching at such a high voltage and frequency, it is very difficult to suppress.
- In general, all of the noisy switching lines should be kept away from the quiet analog section of the RC5061. That is, traces that connect to pins 1, 2, 19, and 20 (HIDRV, SW, LODRV and VCCP) should be kept far away from the traces that connect to pins 3, 16 and 17.
- Place the 0.1µF decoupling capacitors as close to the RC5061 pins as possible. Extra lead length on these reduces their ability to suppress noise.
- Each VCC and GND pin should have its own via to the appropriate plane. This helps provide isolation between pins.
- Place the MOSFETs, inductor, and Schottky as close together as possible for the same reasons as in the first bullet above. Place the input bulk capacitors as close to the drains of the high side MOSFETs as possible. In addition, placement of a 0.1µF decoupling cap right on the drain of each high side MOSFET helps to suppress some of the high frequency switching noise on the input of the DC-DC converter.
- Place the output bulk capacitors as close to the CPU as possible to optimize their ability to supply instantaneous current to the load in the event of a current transient. Additional space between the output capacitors and the CPU will allow the parasitic resistance of the board traces to degrade the DC-DC converter's performance under severe load transient conditions, causing higher voltage deviation. For more detailed information regarding capacitor placement, refer to Application Bulletin AB-5.
- A PC Board Layout Checklist is available from Fairchild Applications. Ask for Application Bulletin AB-11.

PC Motherboard Sample Layout and Gerber File

A reference design for motherboard implementation of the RC5061 along with the PCAD layout Gerber file and silk screen can be obtained from our marketing department at 650-966-7624.

RC5061 Evaluation Board

Fairchild provides an evaluation board to verify the system level performance of the RC5061. It serves as a guide to performance expectations when using the supplied external components and PCB layout. Please call the marketing department at 650-966-7624 for an evaluation board.

Additional Information

For additional information contact Fairchild Semiconductor's Analog & Mixed Signal Products Group Marketing Department at 650-966-7624.

Appendix

Worst-Case Formulae for the Calculation of Cout, R5, and Cin (Circuit of Figure 1 only)

The following formulae design the RC5061 for worst-case operation, including initial tolerance and temperature dependence of all of the IC parameters (initial setpoint, reference tolerance and tempco, active droop tolerance, current sensor gain), the initial tolerance and temperature dependence of the MOSFET, and the ESR of the capacitors. The following information must be provided:

V_{T+}, the value of the positive transient voltage limit;

$|V_{T-}|$, the absolute value of the negative transient voltage limit;

I_O, the maximum output current;

V_{nom}, the nominal output voltage;

V_{in}, the input voltage (typically 5V);

ESR, the ESR of the ouput caps, per cap (44mΩ for the Sanyo parts shown in this datsheet);

R_D, the on-resistance of the MOSFET (20mΩ for the FDB6030);

ΔR_D, the tolerance of the current sensor (usually about 67% for MOSFET sensing, including temperature).

I_{rms}, the rms current rating of the input caps (2A for the sanyo parts shown in this datasheet.)

$$C_{in} = \frac{IO * \sqrt{\frac{V_{nom}}{V_{in}} - \left(\frac{V_{nom}}{V_{in}}\right)^2}}{I_{rms}}$$

$$R5 = \frac{I_O * R_D * (1 + \Delta R_D) * 1.10}{50 * 10^{-6}}$$

Number of capacitors needed fo C_{out} = the greater of:

$$X = \frac{ESR * I_O}{|V_{T-}|}$$

or

$$Y = \frac{ESR * I_O}{V_{T+} - 0.004 * V_{nom} + \frac{14400 * I_O * R_D}{18 * R5 * 1.1}}$$

Example: Suppose that the transient limits are ±134mV, current I is 14.2A, and the nominal voltage is 2.000V, using MOSFET current sensing and the usual caps. We have V_{T+} = $|V_{T-}|$ = 0.134, I_O = 14.2, V_{nom} = 2.000, and ΔR_D = 0.67. We calculate:

$$C_{in} = \frac{14.2 * \sqrt{\frac{2.000}{5} - \left(\frac{2.000}{5}\right)^2}}{2} = 3.47 \Rightarrow 4 \text{ caps}$$

$$R5 = \frac{14.2 * 0.020 * (1 + 0.67) * 1.0}{50 * 10^{-6}} = 10.4K\Omega$$

$$X = \frac{0.044 * 14.2}{0.134} = 4.66$$

$$Y = \frac{0.044 * 14.2}{0.134 - 0.004 * 2.000 + \frac{14400 * 14.2 * 0.020}{18 * 10400 * 1.1}} = 4.28$$

Since X > Y, we choose X, and round up to find we need 5 capacitors for C_{OUT}.

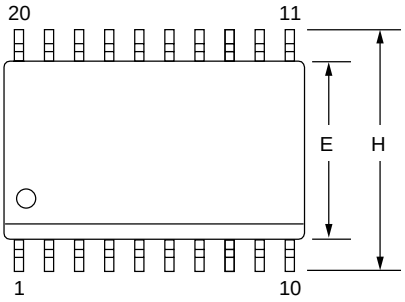
Mechanical Dimension

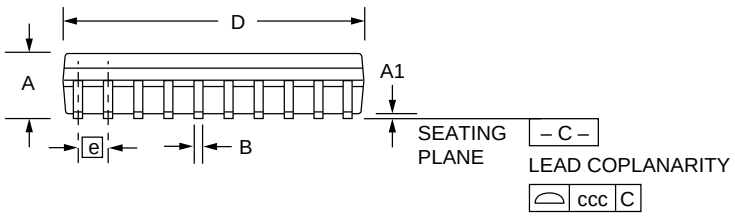
20-Lead SOIC

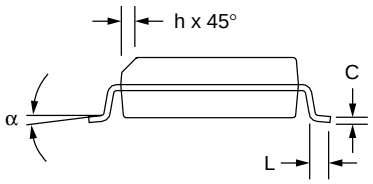
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.496	.512	12.60	13.00	2
E	.291	.299	7.40	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.029	0.25	0.75	
L	.016	.050	0.40	1.27	3
N	20		20		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Preliminary Specification

Ordering Information

Product Number	Package
RC5061M	20 pin SOIC

Preliminary Specification

RC5102

Dual Adjustable Voltage Regulators

Features

- 0.5% Setpoint Accuracy
- Both outputs adjustable from 1.5V to 3.6V
- 100mA output drivers for high current loads
- Short circuit protection
- Fast transient response
- Low Icc current < 1mA
- Factory trimmed low TC voltage reference
- Drives N-Channel MOSFET, NPN or Darlington Pair
- 8 Lead SOIC

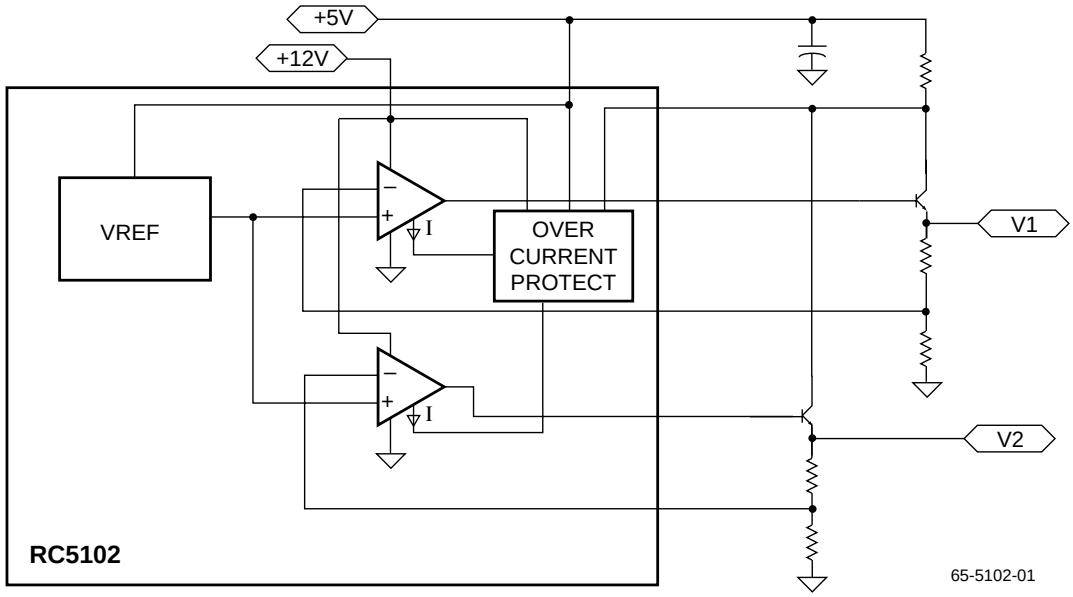
Applications

- 3.3V, 2.8V dual power supply for Pentium® P55 Processor
- Switchable single/dual power supply for Pentium P54C/P55C flexible motherboard implementation
- 1.5V regulator for Pentium Pro GTL+ Bus
- Adjustable dual output power supply for high current loads

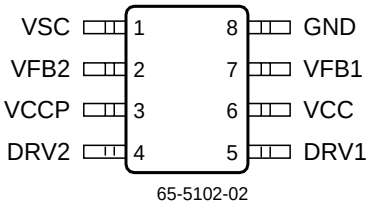
Description

The RC5102, in combination with low Rds,on n-channel MOSFETs, provides a precision low-dropout dual voltage regulator for Pentium, Cyrix® and Power PC® CPUs. By using the 12V supply available within the motherboard of the PC, the RC5102 achieves the high Vgs drive voltage to minimize the Rds, on of the MOSFET for low dropout applications. Earlier designs involving p-channel MOSFETs or pnp transistors are either too costly or provide inadequate drop-out voltages at the high current required. Using the RC5102, a linear conversion from 5V to 2.8V is achieved at load currents in excess of 7A, depending upon the pass element. The RC5102 incorporates a 50MHz operational amplifier in the control path, thus optimizing transient performance due to instantaneous load changes.. Wafer-level trimming is used to adjust the precision of the reference to a nominal accuracy of ±0.5%. Improved line regulation is achieved through the use of a bootstrapped architecture within the bandgap reference. Overcurrent protection is available through the use of an external sense resistor.

Block Diagram



Pin Assignments



65-5102-02

Pin Description

Pin Name	Pin Number	Pin Function Description
VSC	1	Over Current Protection Input
VFB2	2	Regulator 2 Voltage Feedback
VCCP	3	Output driver VCC; 12V nominal
DRV2	4	Regulator 2 Driver Output
DRV1	5	Regulator 1 Driver Output
VCC	6	Analog VCC; 5V nominal
VFB1	7	Regulator 1 Voltage Feedback
GND	8	Ground

Preliminary Information

Absolute Maximum Ratings[1]

Parameter		Conditions	Min.	Typ.	Max.	Unit
VCCP	Driver Supply Voltage				13	V
VCC	Analog Supply Voltage				13	V
T_S	Storage Temperature		-65		150	°C
	Soldering Temperature	10 Seconds			300	°C

Note:

1. Functional operation under any of these condition is not implied. Performance is guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

(VCC = 5V, VCCP = +12V, T_A = 25°C unless otherwise noted)

Parameter		Conditions	Min.	Typ.	Max.	Unit
VCC	Analog Supply Voltage		4.75	5	10	V
VCCP	Driver Supply Voltage	Minimum VCC + 3V	8	12	13	V
T_A	Ambient Temperature		0		70	°C

DC Electrical Characteristics

(VCC = 5V, VCCP = +12V, T_A = 25°C unless otherwise noted)

Parameter		Conditions	Min.	Typ.	Max.	Unit
Vo	Output Voltage	T_A = 0–70°C	1.5		3.6	V
Io	Output Drive Current	Each output		100		mA
Vref Acc	Setpoint Accuracy	I_L = 1mA, Vout = 1.5V		0.5	1.2	%
VTC	Output Voltage TC	0 to 70 °C		-230		µV/°C
LDR	Load Regulation	0.5A to 7A		0.25		%Vo
LIR1	5V Line Regulation	VCC = 5V ± 5%, I_L = 3.5A		12		mV/V
LIR2	12V Line Regulation	VCCP = 12V ± 10%, I_L = 3.5A		19		mV/V
Vr	Output Noise	0.1 to 20KHz		30		µV
Vsc	Short Circuit trip	Rsense = 0.01Ω		100		mV
Pd	Power Dissipation	No Load		68		mW

AC Electrical Characteristics

(VCC = 5V, VCCP = +12V, T_A = 25°C unless otherwise noted)

Parameter		Conditions	Min.	Typ.	Max.	Unit
Tr	Response Time	I_L = 0.5A to 5.5A		5		µs
PSRR	Power Supply Rejection Ratio			65		dB

Application Schematics

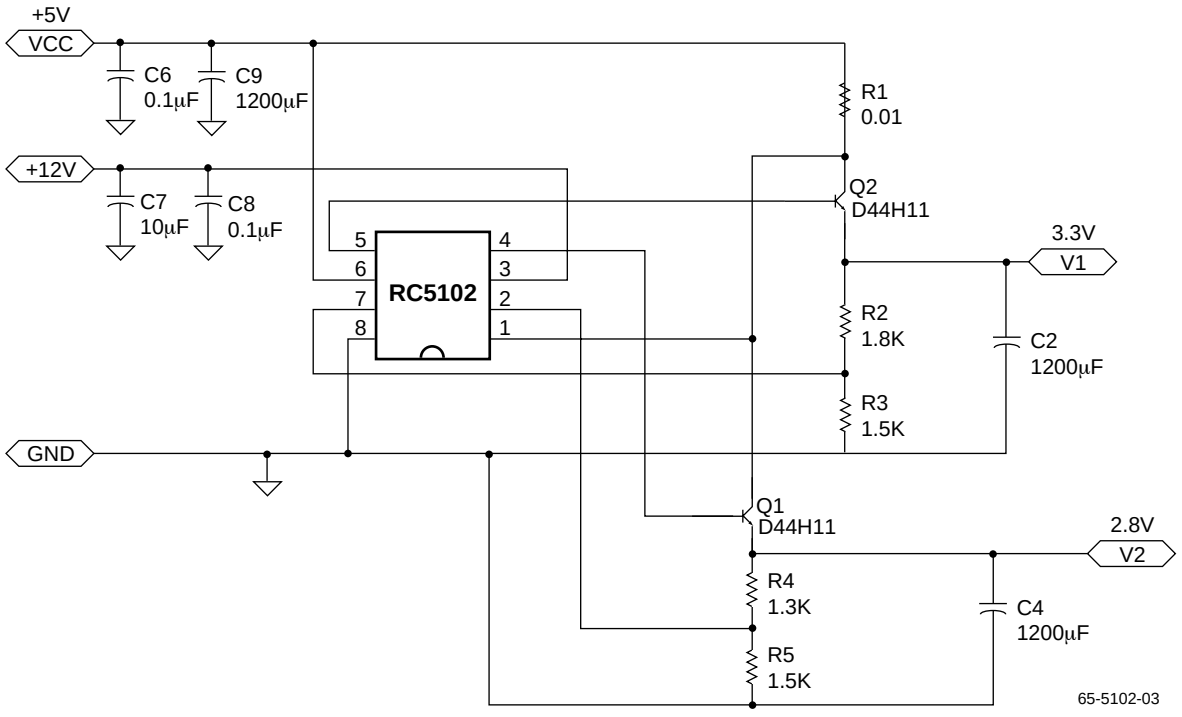


Figure 1. RC5102 Dual Output, 4A Application Schematic

Preliminary Information

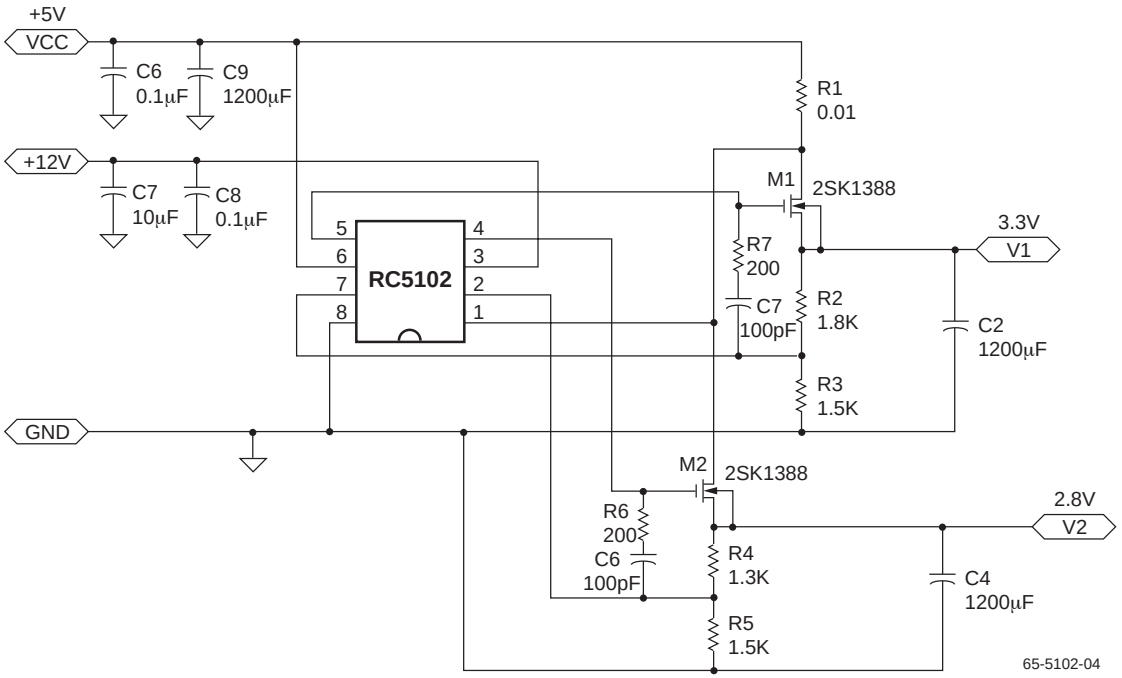


Figure 2. RC5102 Dual Output, 5A Application Schematic

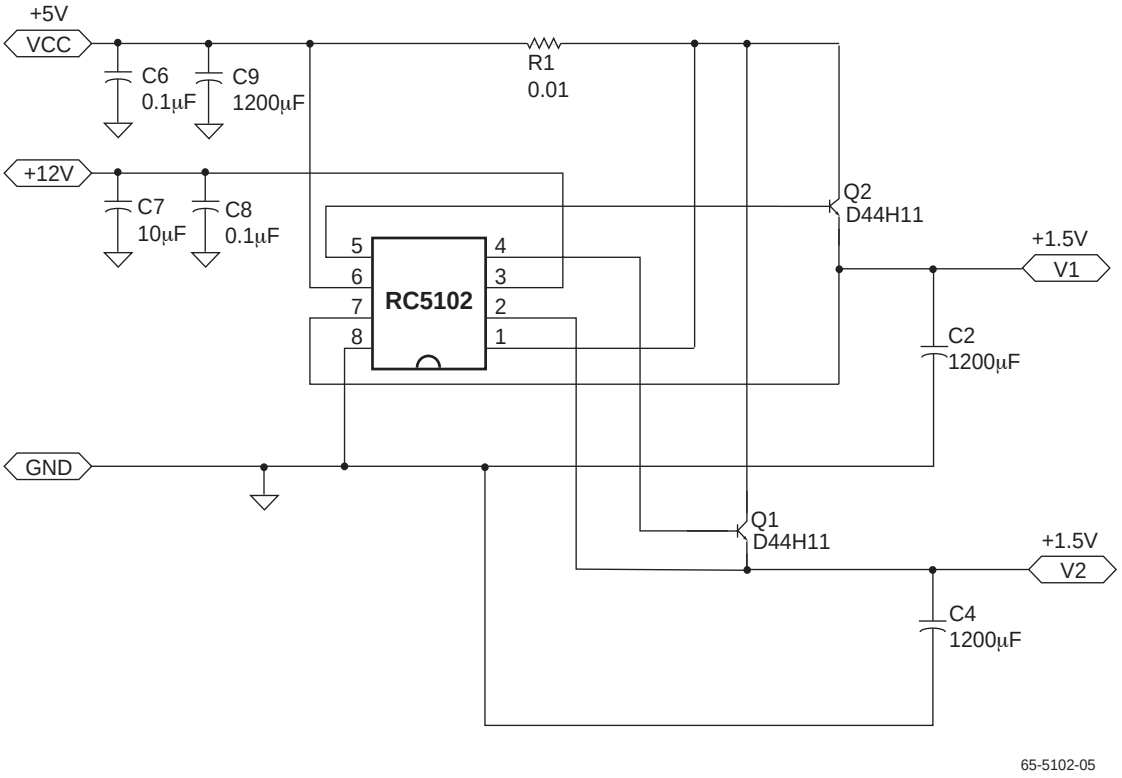


Figure 3. RC5102 Application Schematic for Pentium Pro GTL+ Bus Termination

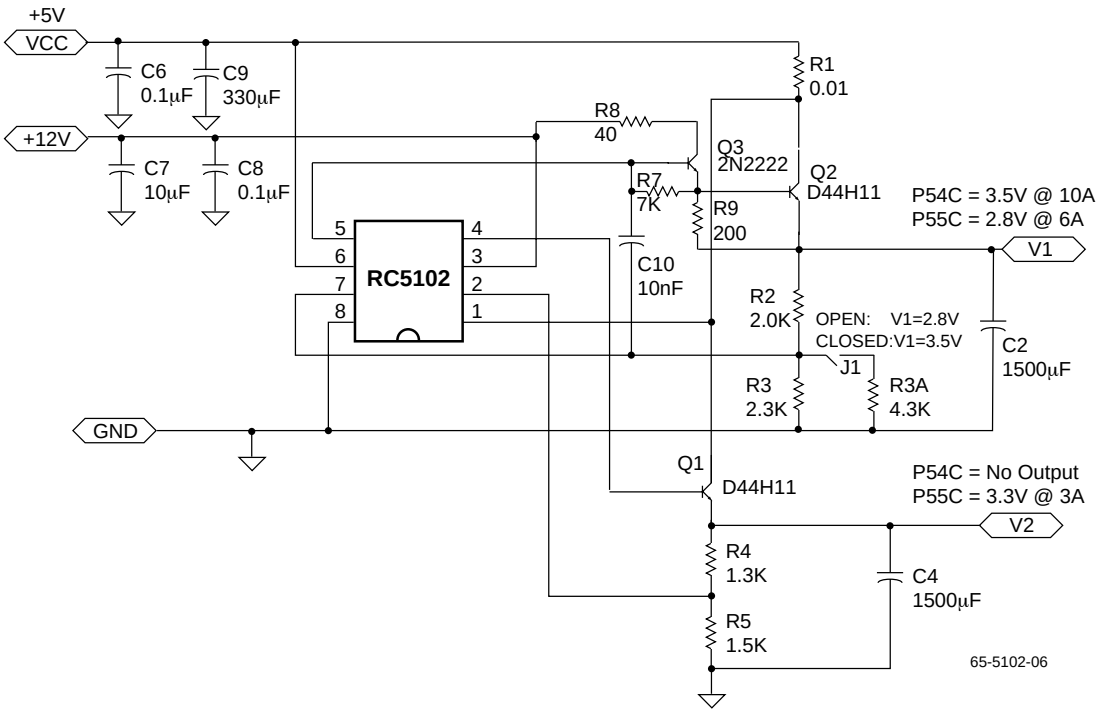


Figure 4. RC5102 Application Schematic for Pentium P54/P55C

Table 2. Components for P54C/P55C Application Circuit

Quantity	Reference	Part	Description
1	C9	330 μF	AVX Electrolytic
1	C7	1 μF	Chip Cap
2	C6, C8	0.1 μF	Chip Ceramic
2	Q1, Q2	D44H11	Power NPN Transistor
1	Q3	2N2222	General Purpose NPN Transistor
1	R1	0.01	1% Resistor
2	R5, R2	200	1% Resistor
1	R3	1.8 K	1% Resistor
1	R4	1.5 K	1% Resistor
1	R7	1.5 K	0.1% Resistor
1	R6	1.3 K	1% Resistor
1	R8	2.786 K	1% Resistor
1	R11	2 K	1% Resistor
1	R12	300 K	5% Resistor
1	R13	100 K	5% Resistor
1	R14	20 K	5% Resistor
2	C2, C4	1500 μF	Sanyo Electrolytic

Applications Information

Theory of Operation

The RC5102 is a dual output, low dropout voltage regulator controller intended for use in applications that require dual voltages at moderate to high output currents. Using external power transistors and precision trim resistors, a dual adjustable voltage regulator can be implemented. The choice of the component(s) will depend heavily upon the type of application. For load currents of up to 5A per output, the use of low-cost power NPN transistors is sufficient, as illustrated in figure 1. For applications requiring load currents greater than 5A, either an NPN darlington pair or an N-channel MOSFET is recommended due to the increased power throughput. Because the gate/base drive voltage is derived from the 12V input supply, the overall dropout voltage will depend only on the load current and either the Vce,sat of the NPN transistor or the Ron of the MOSFET. Therefore, very low dropout voltages can be achieved when the load currents are sufficiently low and a low Ron MOSFET or a low Vce,sat transistor is used.

In applications using N-channel MOSFETs, the external R-C network should be implemented as illustrated in figure 2. Failure to include this circuitry can result in an unstable gate drive signal. The actual component values may vary depending upon the individual application.

Minimum Load

The RC5102 regulator controller is specified over a finite load range. If the output current becomes too small, leakage currents will dominate and the output voltage(s) may drift out of regulation. Maintaining a minimum of 1mA load current on each output will assure that the load current will dominate any leakage currents over the operating temperature range.

Adjustable Output Voltage Design

The RC5102 allows each of the two outputs to be adjusted between the 1.5V reference voltage and 3.6V using two external precision resistors. In order to maintain the 1% output voltage accuracy, a minimum of 100uA should be fed back to the VFB1 and VFB2 pin to correctly bias the internal op-amp. For most applications, the sum value of the two resistors should not exceed approximately 35KΩ. For figures 1 and 2, the resistor values can be calculated using the following equations:

$$V_1 = V_{REF} \times \left(\frac{R2 + R3}{R3}\right)$$

$$V_2 = V_{REF} \times \left(\frac{R4 + R5}{R5}\right)$$

Output Capacitors

For stability and output noise reduction, the use of output capacitors is required. The required amount of load capacitance will depend upon the actual load current; higher loads will require larger capacitors. Regardless, an absolute minimum of 1uF is required to maintain stability under all load conditions. It is not necessary to use expensive low ESR type capacitors here; standard aluminum electrolytics are generally sufficient and can actually provide increased stability over extremely low ESR type devices. If possible, solid tantalum capacitors should be used in applications where transient response is critical.

Current Sense resistor

Over current protection is implemented using an external current sense resistor between the 5V input and the VSC pin that feeds the collector/drain of the pass transistors. This resistor will need to carry currents in excess of the sum of the two loads in order to perform correctly. The RC5102 will begin to limit the output current to the load(s) by turning off the output driver when the voltage across the sense resistor exceeds the nominal 100mV threshold. When this happens, the output voltage will temporarily go out of regulation. As the voltage across the resistor increases, the switch will continue to turn off until the current limit value is reached. At this point, the RC5102 will continuously deliver the limit current at a reduced output voltage level. To insure that load transient conditions do not momentarily cause deregulation of the output voltage, a 20% margin in the limit voltage is recommended. Thus the current sense resistor should be determined by the relationship:

R = 100mV/Ipeak ,

Where Ipeak = Imax • 1.2

Since the value of the sense resistor is generally in the 10mΩ region, care should be taken in the layout of the PCB. Trace resistance can contribute significant errors. The traces to the VCC and VSC pins of the RC5102 should be Kelvin connected to the outside pads of the sense resistor.

Dual Power Supply Application

Some CPU power applications such as the Intel Pentium® P55C will require separate voltages for the CPU core and I/O circuitry. The circuit illustrated in figure 2 addresses this requirement using a minimum of external components. In this configuration, both linear regulator outputs can be easily programmed between 1.5V and 3.6V to meet a variety of dual voltage requirements. For loads of 4A or lower, the power dissipation of the external MOSFET should not pose any thermal design problems if it is chosen wisely. For loads greater than 10W, an appropriate heatsink must be chosen to assure the pass transistor remains within its Safe Operating Area for the desired output current level.

Auto Switching Single/Dual Power Supply for a Flexible Motherboard Design

A detailed analysis of the new Pentium-class processors reveals the requirement for an open-ended motherboard power supply design that can accomodate different CPUs in a single system. As an example, consider the Intel® P54C and P55C Pentium® processors. Although these two processors may occupy the same CPU socket, distinct differences exist in their power supply requirements. The present generation P54C uses a single supply for both the processor core and the I/O. For the higher performance devices, the supply voltage required is 3.5V ±100mV (VRE s-specification). For the lower performance models, a 3.3V ±5% supply is acceptable. For improved compatibility, Intel has now re-specified its 3.3V standard CPUs for operation at the new 3.5V VRE level. The P55C multimedia upgrade processor, due to be released in the latter part of 1996, requires separate voltages for the core and I/O circuitry. The nominal core voltage is currently 2.8V ±100mV, while the I/O supply remains at a nominal 3.3V. It is therefore desirable to implement a power supply design that will automatically detect the CPU model present and program each output voltage accordingly. The circuit in figure 4 directly addresses this requirement. The basic theory of this design is to provide an automatic switch between a single and a dual linear power supply depending upon which CPU occupies the socket.

To ease the task of identifying the CPU, the P55C processor includes a single-bit identification pin *VCC2DET*, at location AL1, to distinguish itself from the standard Pentium® P54C processor. This pin is always bonded to ground on the P55C CPU, while it is an internal no connect on the P54C. Therefore, the user can easily identify which processor occupies the CPU socket by direct monitoring of this pin. The circuit in figure 4 uses the CPU identification pin to select either a single or a dual output as well as select the appropriate output voltage for the CPU core power island.

Because the I/O circuitry can always operate from a nominal 3.5V supply, output 1 is set at a fixed 3.5V output. The CPU core supply is thus switched between 2.8V and 3.5V using an external FET and the appropriate resistor values. Using this circuit configuration, both output s can source up to 5A. These current ranges will easily accomodate the standard Pentium® P54C and the P55C as well as other Pentium® compatible processors. For selected processors, the load currents required by each output will force the use of a MOSFET or Darlington pair as the pass elements. Using these higher-powered devices, the RC5102 can source up to 10A given the appropriate thermal requirements are also met. Please consult Fairchild Semiconductor Applications for additional details regarding CPU applications.

Current Sharing Option

If the RC5102 is to be used in an application that must address several CPUs, additional load current capability may be required from one of the outputs. For example, consider the Cyrix® 6x86 microprocessor. Although its specifications are very similar to those of the Intel Pentium® P54, it requires as much as 10A under worst-case conditions. To remedy this situation without adding additional costly pass elements, the RC5102 can be configured to allow both outputs to share the load current. In order to achieve acceptable performance, the layout of the output traces must be carefully routed. If the traces from the emitter of the pass transistors to the point where the two outputs are joined together, both outputs will share the load current equally. If the series impedances of each trace are different however, one output will tend to provide more than 50% of the load current while the other output will not be heavily burdened.

Using this option, low cost NPN transistors may be used instead of MOSFETs to deliver up to 10A loads. Again, the overall power limitation will depend heavily upon the level of thermal management for the pass elements. Please consult Fairchild Semiconductor Applications for additional details on this and other possible configurations using the RC5102.

Notes:

Notes:

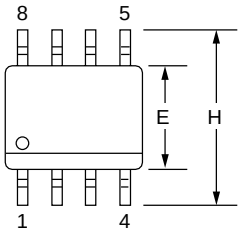
Notes:

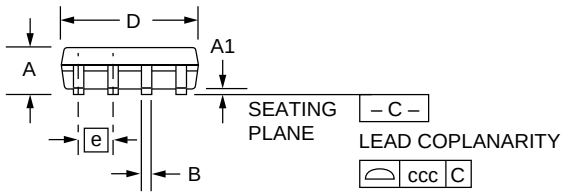
Mechanical Dimensions – 8 Lead SOIC

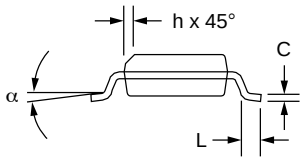
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.20	0.25	5
D	.189	.197	4.80	5.00	2
E	.150	.158	3.81	4.01	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	8		8		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Preliminary Information

Ordering Information

Product Number	Package
RC5102M	8 pin SOIC

Preliminary Information

RC5201

Chemistry Independent Intelligent Battery Charger

Advanced Information

Features

- Chemistry independent charging
- SMBus™ 2-wire serial interface controlled
- Single and dual battery systems
- 8 bit output voltage DAC
- 8 bit current DAC
- 4 bit power DAC
- 6A max charging current
- 19V max battery voltage
- 24V max input voltage
- 6V min input voltage
- 3.3V, ±1% over temperature “keep alive” precision reference
- 5V keep-alive regulator controller onboard
- 100% maximum duty-cycle
- Synchronous rectification
- Voltage mode control
- System soft start protects during adapter hot plug-ins
- System current limit protection
- Output overvoltage crowbar protection
- Undervoltage (UVLO) shutdown
- Charger output soft start implemented digitally
- Input Isolation P-FET open with un-powered adapter
- Battery backfeed prevented
- Available in SSOP 24 package and TSSOP24
- Optimized response for each control loop (current, voltage and power)
- 90% efficiency for minimum heat dissipation
- Power down driven by SMBus or by adapter not available
- Controlled drive of discrete FETs minimizes switching power dissipation
- Logic signal ACAV indicates presence of AC adapter (adjustable threshold)
- Average current control
- Remote sense input
- Voltage feed forward

Applications

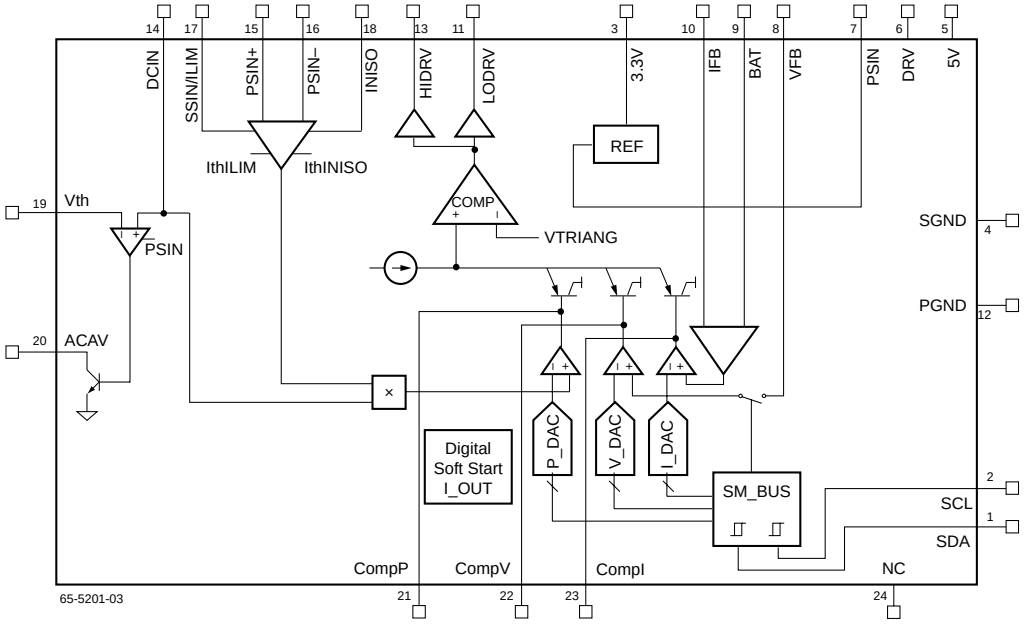
- Notebooks’ fast chargers
- PDAs
- Hand-held portable instruments

Description

The RC5201 is a smart battery charger IC controller for Li+ and Ni based battery chemistries. The charger (slave) together with the host controller and smart battery constitutes a smart battery system that communicates via the SMBus protocol, a two wire serial communication system.

An innovative power control loop allows operation from line power and battery charging (with residual power) without exceeding the max input power programmed according to the AC adapter power rating.

Block Diagram



SMBus is a trademark of Intel Corporation

RC5230

System Electronics Regulator for Mobile PC's

Features

- Synchronous rectification
- High precision
- High efficiency
- Input and output voltage feedback
- 6V to 20V input voltage range
- ±10% current limit precision
- TSSOP24
- 5V, 5V-Always, 12V and 3.3V outputs
- UVLO
- OVP

Applications

- Notebook and PDA PC's
- Hand-held portable instruments

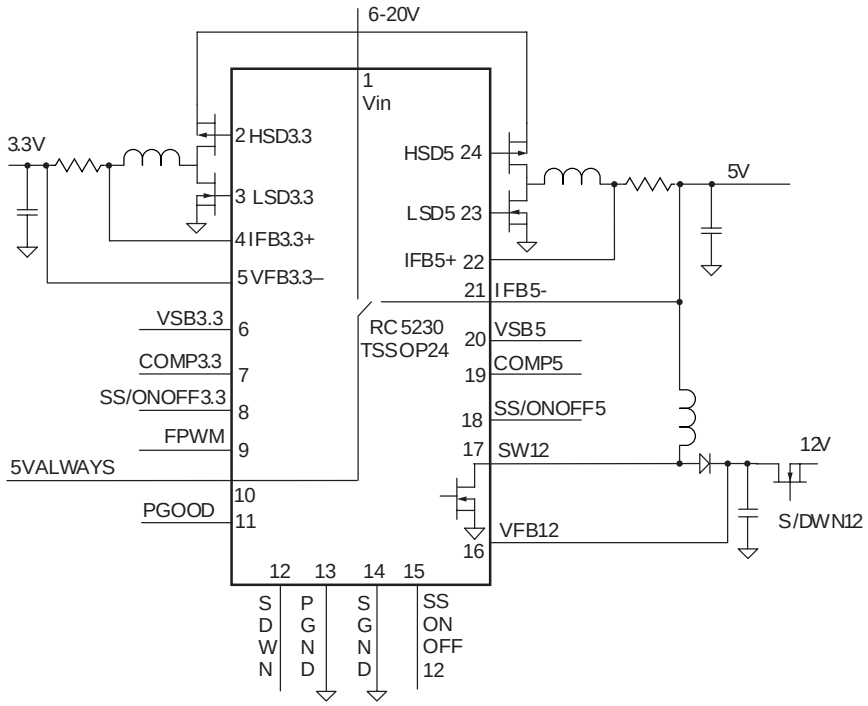
Description

The RC5230 is a high efficiency and high precision DC/DC controller for notebooks. Double voltage mode-input and output voltage feedback- allows for fast loop response over a wide range of input and output variations.

This scheme also allows for minimum power dissipation as a small value for the sense resistor is selected to set current (as opposed to having to sense current over the entire current range as required in other schemes). The tightly controller current limit threshold allows for a tight design of magnetics and discrete transistors for minimum cost and space at maximum performance.

Target Specifications

Block Diagram



RC5231

CPU Voltage Regulator for Mobile PC's

Features

- **S**ynchronous rectification
- High precision
- High efficiency
- Voltage mode
- 6V to 20V input voltage range
- ±10% current limit precision
- TSSOP20
- 1.7V CPU and 1.8V CACHE
- UVLO
- OVP

Applications

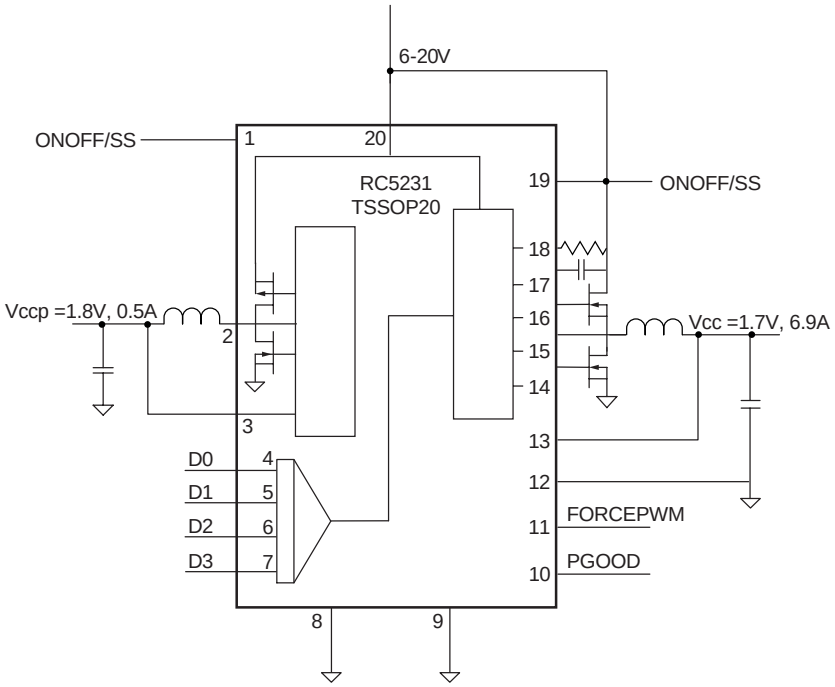
- Notebook and PDA PC's
- Hand-held portable instruments

Description

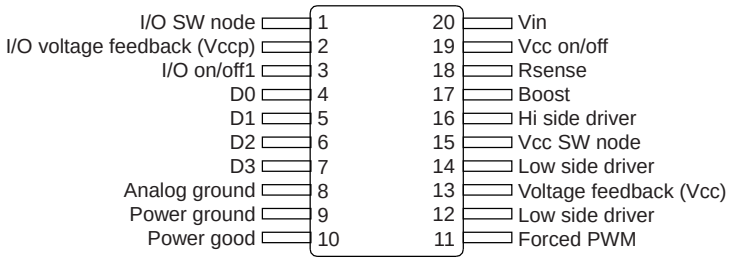
The RC5231 is a high efficiency and high precision DC/DC controller for notebooks. The tightly controller current limit threshold allows for a tight design of magnetics and discrete transistors for minimum cost and space at maximum performance.

Preliminary Information

Block Diagram



Pin Assignments



Preliminary Information

Pin Description

Pin Number	Pin Name
1	I/O SW node
2	I/O voltage feedback (Vccp)
3	I/O on/off1
4	D0
5	D1
6	D2
7	D3
8	Analog ground
9	Power ground
10	Power good
11	Forced PWM
12	Low side driver
13	Voltage feedback (Vcc)
14	Low side driver
15	Vcc SW node
16	Hi side driver
17	Boost
18	Rsense
19	Vcc on/off
20	Vin

Absolute Maximum Ratings (Beyond which the device may be damaged)[1]

Parameter	Conditions	Min.	Typ.	Max.	Units
Vs	Input Supply Voltage			30	V
Ambient Temperature, Ta		0		70	Deg. C

Note: 1. Functional Operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

Operating Conditions (DCIN = 19VV, Ta = 0-70°C unless otherwise specified)

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply and Regulator					
Vs Input Supply Voltage		6		20	V
Input Quiescent Current	Operation Sleep			2 1	mA µA
5V regulator accuracy	0 to 70 Deg. C	- 2		+2	%

Note: 1. Functional Operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

Applications

Figure 1 below shows the system block diagram.

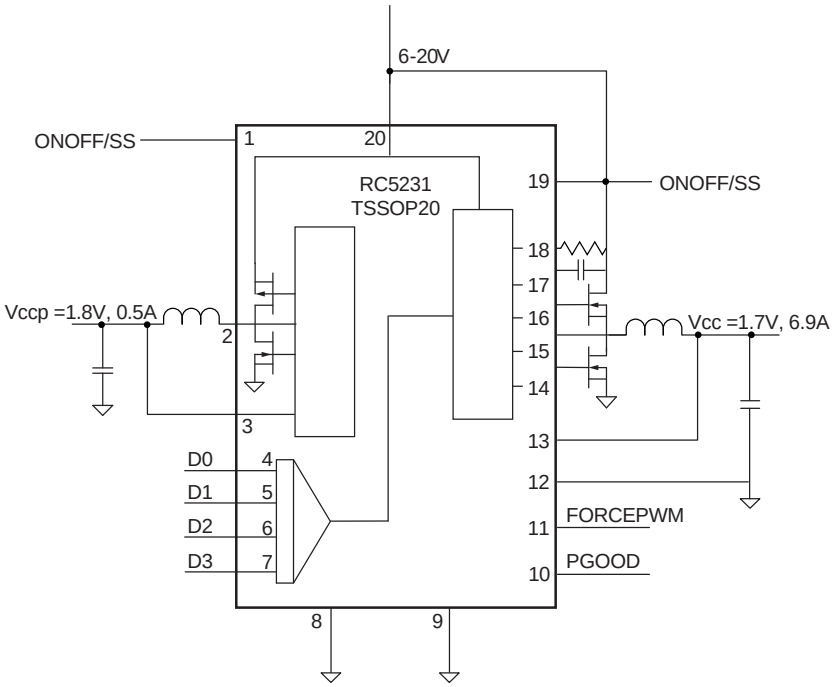


Figure 1

Preliminary Information

Notes:

Notes:

Notes:

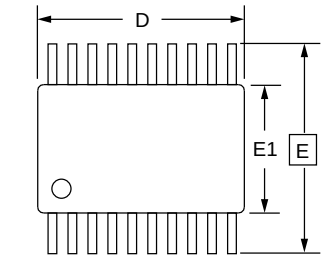
Mechanical Dimensions

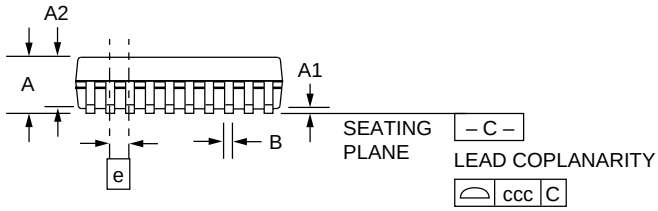
20 Lead TSSOP

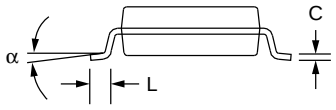
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.047	—	1.20	
A1	.002	.006	0.05	0.15	
A2	.031	.041	0.80	1.05	
B	.007	.012	0.19	0.30	5
C	.004	.008	0.09	0.20	5
D	.250	.257	6.40	6.60	2, 4
E	.240	.264	6.10	6.70	
E1	.168	.176	4.30	4.50	
e	.026 BSC		0.65 BSC		
L	.018	.029	0.45	0.75	3
N	20		20		6
α	0°	10°	0°	10°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "B" & "C" dimensions include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Preliminary Information

Preliminary Information

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

1/20/99 0.0m 002
Stock#DS30005231

RC5501

4 Watt Stereo Sound Driver

Features

- Up to 4W/channel
- Drives 8Ω and 4Ω non-powered speakers
- NO-POP during power-up/power-down and mute
- Internal thermal limiting circuitry
- Total Harmonic Distortion < 0.1%

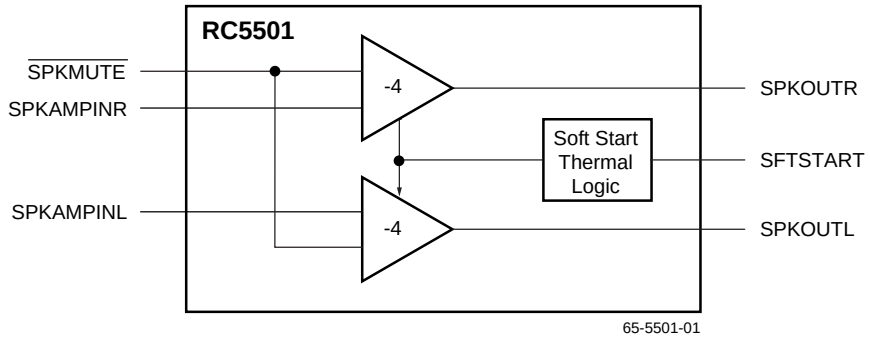
Applications

- Multimedia PC motherboards and add-in sound cards
- Companion chip to sigma-delta sound codecs
- Sound Channel back-end in set-top boxes

Description

The RC5501 is a stereo power amplifier used for directly powering speaker and headphone sets.

Block Diagram



65-5501-01

Preliminary Information

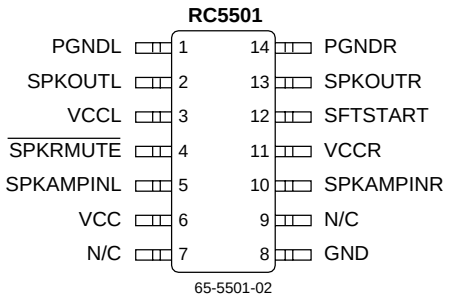
Functional Description

The RC5501 stereo sound driver is an audio device that can be used on PC motherboards and add-in sound cards. It consists of stereo output drivers for headphone or speakers with a mute feature and circuitry that eliminates popping at power on, power off, mute enable, and mute disable.

The output drivers can deliver up to 2 Watts peak and 4 Watts peak into 8Ω and 4Ω speakers, respectively, from a 12V source. The drivers use class AB amplifiers and maintain a low bias current. To help prevent turn-on speaker pop, a delay is provided to these output drivers to allow settling before speaker activation. The time constant is user-defined through an external capacitor (C_{DELAY}) on the SFTSTART pin.

The thermal limiting circuitry activates if the chip temperature typically exceeds 150°C.

Pin Assignments



Pin Definitions

Pin Name	Pin Number	Pin Function Description
PGNDL	1	Left speaker ground.
SPKOUTL	2	Left speaker output.
VCCL	3	Left speaker 12V power supply.
$\overline{\text{SPKRMUTE}}$	4	Speaker mute.
SPKAMPINL	5	Left channel power amp input.
VCC	6	12V power supply input.
N/C	7, 9	No connection.
GND	8	Ground.
SPKAMPINR	10	Right channel power amp input.
VCCR	11	Right speaker 12V power supply.
SFTSTART	12	Soft start timing capacitor.
SPKOUTR	13	Right speaker output.
PGNDR	14	Right speaker ground.

Preliminary Information

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min	Typ	Max	Units
V_{CC} V_{CCR} V_{CCL}	Power supply voltage			13.2	V

Note:

1. Functional operation under any of these conditions is NOT implied. Performance is guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter		Conditions	Min	Typ	Max	Units
V_{CC} V_{CCL} V_{CCR}	Power Supply		11.2	12	12.8	V
V_{IH}	Input Voltage Logic High		2			V
V_{IL}	Input Voltage Logic Low				0.8	V
	Ambient Temperature		0		70	˚C
T_C	Maximum Operation Die Temperature	Overthermal Protection		150		˚C
I_{total}	Power Supply Current	No load		19	25	mA
ESD	ESD Threshold	Human Body Model	2000			V

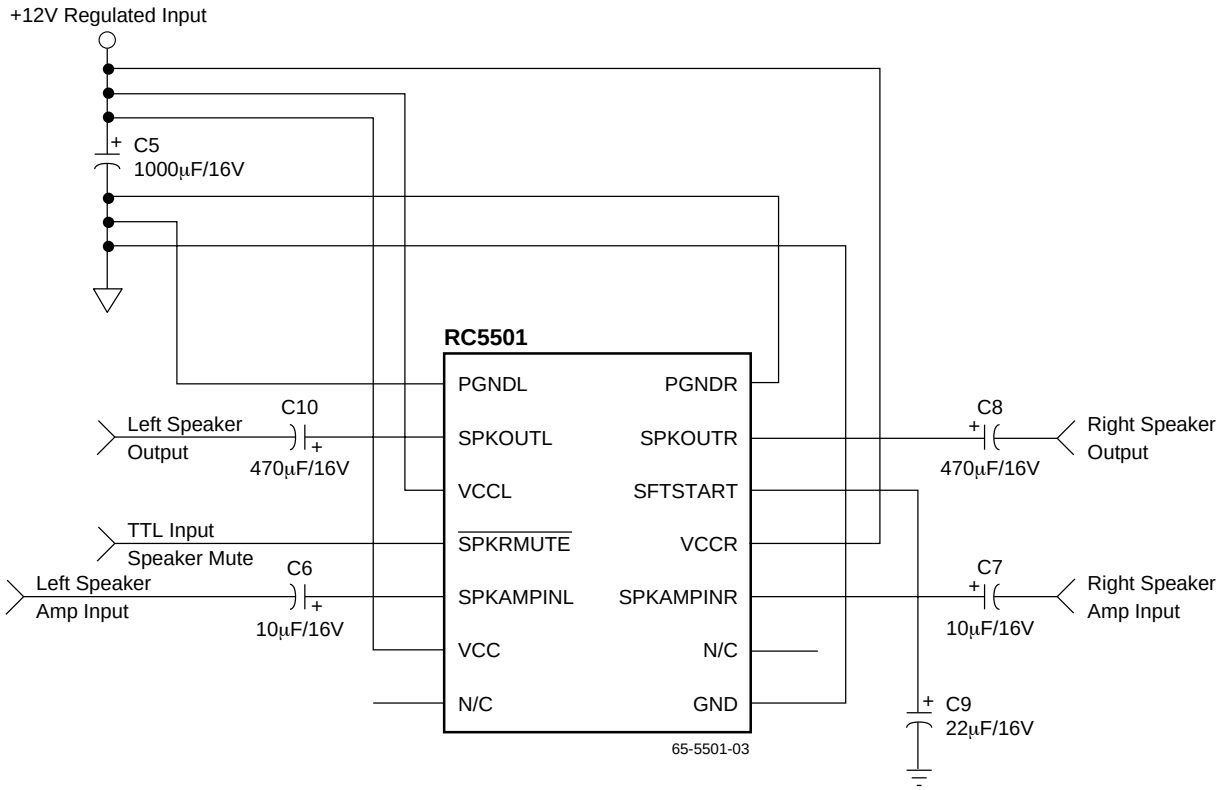
Electrical Characteristics

$V_{CC} = V_{CCL} = V_{CCR} = 12V \pm 6\%$, unless otherwise specified.

Parameter		Conditions	Min	Typ	Max	Units
Speaker Driver		f = 1KHz, RL = 8Ω unless otherwise specified				
Zin	Input Impedance		100			KΩ
Av	Voltage Gain	Vin = 0.5 Vrms	-3.80	-4.0	-4.20	V/V
L&R Av	Left and Right Gain Matching	Vout = $4V_{P-P}$		0.5		%
Vo	Output Voltage	RL = 4Ω or 8Ω, VCC = 12V		±4		V
SNR	Signal to Noise Ratio	Input Referenced		85		dB
Po	Power Output Per Channel Peak	RL = 4Ω, VCC = 12V (See Figure 1)		4		W
CS	Channel Separation L/R Input Referenced	Vin = 0.5 Vrms	66			dB
THD	Total Harmonic Distortion	fo = 1KHz, Po = 50mW		0.1		%
Noise		20Hz to 20kHz, A-Weighted		4		μVrms
PSRR	Power Supply Rejection Ratio Input Referenced	f = 100Hz, ΔVcc = 1.6Vp-p	70	80		dB
Soft Start						
Delay	Anti-Pop Ramp-Up and Ramp-Down time	No Pop condition C_{DELAY} = 22μF on SFTSTART		2		sec

Preliminary Information

Applications Discussion



Notes:

1. 4 watt power represents the peak of the audio level and cannot be sustained without correct package thermal considerations. The average audio signal can be sustained by the RC5501 without extra thermal considerations.
2. To improve the thermal resistance of the PDIP package, a heat sink can be used.

Figure 1. 4 Ohm Speaker, 4 Watt Application or 8 Ohm Speaker, 2 Watt application

Preliminary Information

Notes:

Notes:

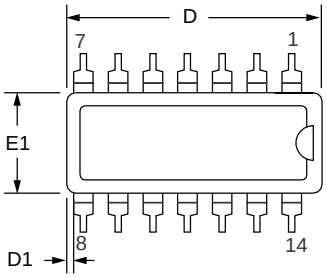
Mechanical Dimensions

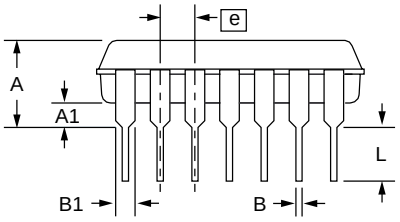
14 Lead Plastic DIP Package

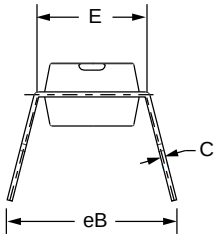
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	.725	.795	18.42	20.19	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.200	2.92	5.08	
N	14		14		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are shown for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.







Preliminary Information

Ordering Information

Product Number	Package
RC5501N	14 PDIP

Preliminary Information

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

5/20/98 0.0m 001
Stock#DS30005501

RC5502

Dual High Power Audio Amplifier

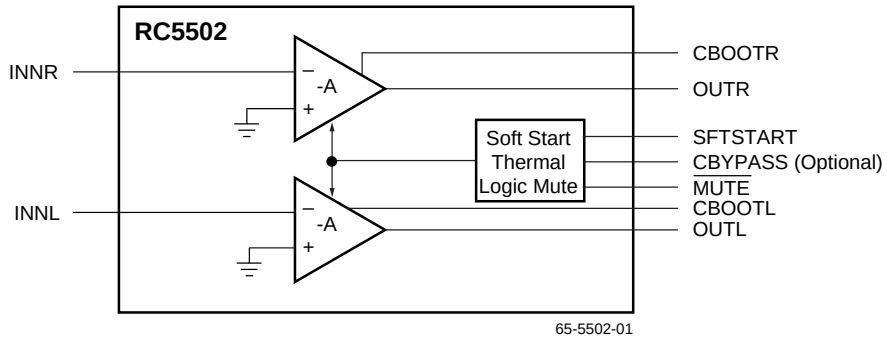
Features

- 3W/channel into an 8 ohm speaker with V_{CC}=12V
- No pop during power-up and power-down
- Speaker mute control pin
- Internal thermal limiting circuitry
- User definable gain
- Self-centering output bias voltage
- Total Harmonic Distortion < 0.1%

Description:

The RC5502 is a stereo audio amplifier for use in directly driving non-powered speakers. The RC5502 amplifier can provide up to 3 watts of peak power into an 8 ohm speaker load from a 12 volt supply. The gain of the RC5502 is user defined by the selection of the appropriate feedback resistors. The RC5502 has internal circuitry for the prevention of "popping" with power-up/power-down and internal thermal limiting circuitry.

Block Diagram



Preliminary Information

Functional Description:

The RC5502 stereo sound amplifier is an audio device that can be used on PC motherboards and add-in sound cards. It consists of stereo output amplifiers which can drive 4 and 8 ohm speakers without popping during power-up/power-down, a mute control pin for disabling the power amplifiers and internal thermal limiting circuitry.

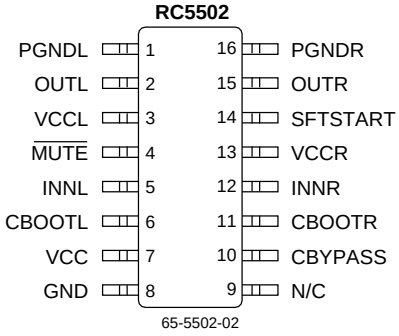
The power amplifiers can deliver 3 watts per channel of peak power to an 8 ohm speaker with a 12 volt power supply. This is accomplished by using an external boot strap capacitor to raise the internal base voltage of the output transistor. In this application, the output voltage can swing ±5 volts into an 8 ohm speaker load with only a 12 volt supply. The user defines the amplifier gain so the output power level can be optimized based on the input signal level.

To prevent turn-on speaker pop, a time delay is provided to the power amplifiers during power-up to allow the output voltage to settle before the amplifiers are activated. This time constant is user defined through an external capacitor on the SFTSTART pin.

The positive (+) input signals for both amplifiers are internally biased at approximately 6.2 volts and this sets the “AC ground” reference level for the amplifiers. This reference signal is connected to pin 10. This signal is internally generated, however, an external bypass capacitor can be connected to this pin to improve the L/R channel cross talk.

The internal thermal limiting circuitry activates if the chip temperature typically exceeds 150°C.

Pin Assignments



Pin Definitions

Pin Name	Pin Number	Pin Function Description
PGNDL	1	Left Amplifier ground.
OUTL	2	Left Amplifier output.
VCCL	3	Left Amplifier 12V power supply.
$\overline{\text{MUTE}}$	4	Amplifier mute. (L=Disable, H=Enable)
INNL	5	Left Amplifier IN.
CBOOTL	6	Left Amplifier VBoot Capacitor.
VCC	7	12V power supply.
GND	8	Ground.
NC	9	No Connection.
CBYPASS	10	Bypass Capacitor. (optional)
CBOOTR	11	Right Amplifier VBoot Capacitor.
INNR	12	Right Amplifier IN.
VCCR	13	Right Amplifier 12V Power Supply
SFTSTART	14	Soft Start Timing Capacitor
OUTR	15	Right Amplifier Output.
PGNDR	16	Right speaker ground.

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min	Typ	Max	Units
V_{CC} V_{CCR} V_{CCL}	Power supply voltage			13.2	V

Note:

1. Functional operation under any of these conditions is NOT implied. Performance is guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter		Conditions	Min	Typ	Max	Units
V_{CC} V_{CCL} V_{CCR}	Power Supply		11.2	12	12.8	V
V_{IH}	Input Voltage Logic High		2			V
V_{IL}	Input Voltage Logic Low				0.8	V
	Ambient Temperature		0		70	˚C
T_C	Maximum Operation Die Temperature	Overthermal Protection		150		˚C
I_{total}	Power Supply Current	No load		19	25	mA
ESD	ESD Threshold	Human Body Model	2000			V

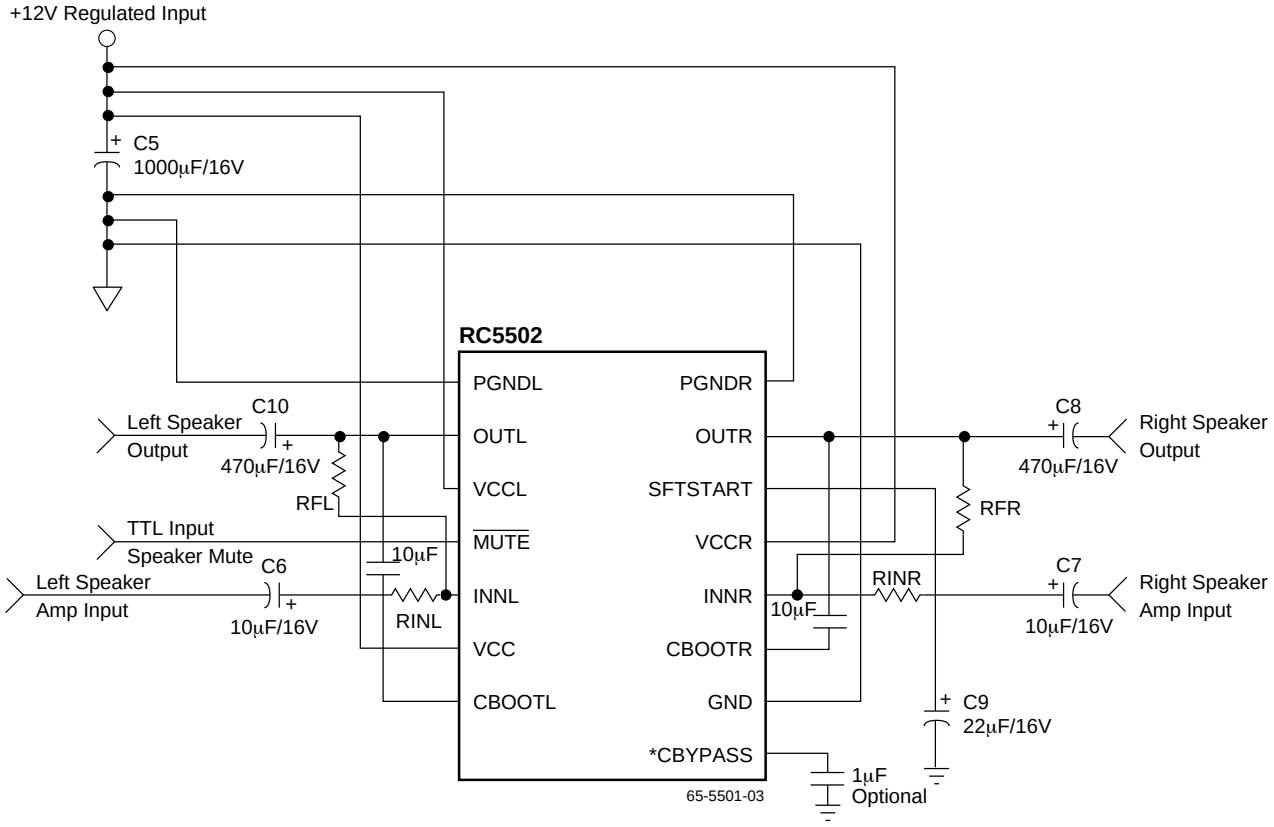
Electrical Characteristics

$V_{CC} = V_{CCL} = V_{CCR} = 12V \pm 6\%$, unless otherwise specified.

Parameter		Conditions	Min	Typ	Max	Units
		f = 1KHz, RL = 8Ω unless otherwise specified				
Zin	Input Impedance		100			KΩ
Vo	Output Voltage	RL = 8Ω, VCC = 12V		±5		V
SNR	Signal to Noise Ratio	Input Referenced		85		dB
Po	Power Output Per Channel Peak	RL = 8Ω, VCC = 12V (See Figure 1)		3		W
CS	Channel Separation L/R Input Referenced	Vin = 0.5 Vrms	66			dB
THD	Total Harmonic Distortion	fo = 1KHz, Po = 50mW		0.1		%
Noise		20Hz to 20kHz, A-Weighted		4		μVrms
PSRR	Power Supply Rejection Ratio Input Referenced	f = 100Hz, ΔVcc = 1.6Vp-p	70	80		dB
Soft Start						
Delay	Anti-Pop Ramp-Up and Ramp-Down time	No Pop condition C_{DELAY} = 22μF on SFTSTART		2		sec

Preliminary Information

Applications Discussion



Notes:
The gain for each amplifier is user defined and is calculated as follows: A = –Rf/Rin with typical values for Rf = 100K.
*Cbypass is optional. An external 1μF bypass capacitor will typically improve the L/R channel cross talk by 20dB.

Figure 1

Preliminary Information

Notes:

Notes:

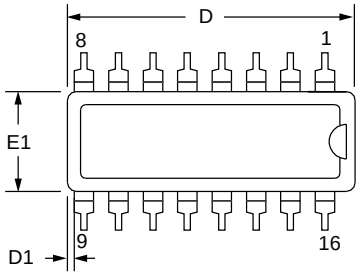
Mechanical Dimensions

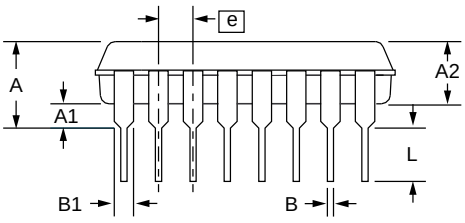
16 Lead Plastic DIP Package

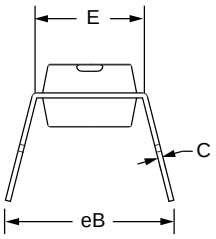
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	.745	.840	18.92	21.33	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.160	2.92	4.06	
N	16		16		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are shown for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.







Preliminary Information

Ordering Information

Product Number	Package
RC5502N	16 PDIP

Preliminary Information

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonable expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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RC5512

RAPPER™ Family – 4 Watt Stereo Sound Driver

Features

- Up to 4W/channel
- Drives 8Ω and 4Ω non-powered speakers
- NO-POP: during power-up/power-down and mute control
- Individual control pins to select mute and on/off for headphone, speaker, microphone, and regulator block
- Provides regulated 5V supply for sound codec, etc.
- Line output signal-to-noise ratio of 85dB
- Sleep mode supply current typically 10μA
- Microphone multiplexing
- Total harmonic distortion <0.1%
- Microphone amplifier with AGC 40dB dynamic range
- Internal Thermal Limiting Circuitry

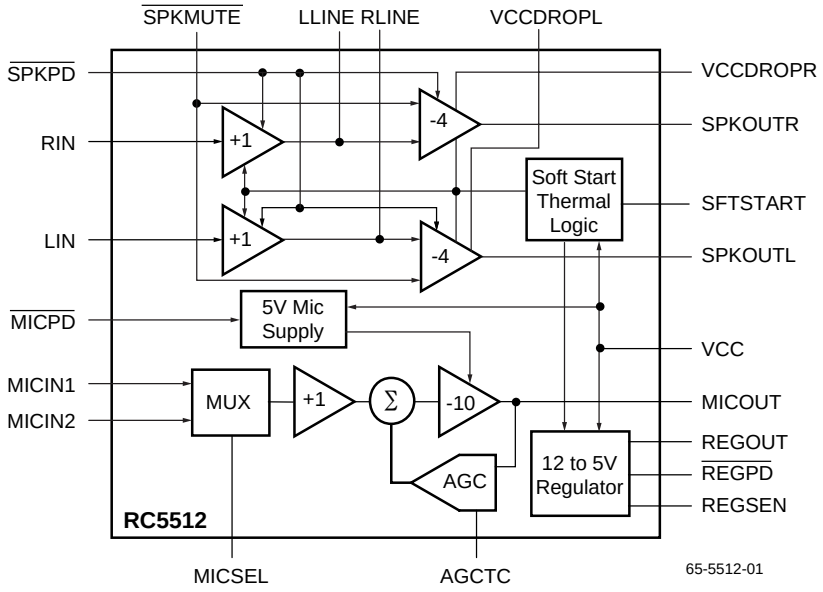
Applications

- Multimedia PC motherboards and add-in sound cards
- Portable multimedia personal computers
- Companion chip to Sigma-Delta Sound Codecs
- Sound Channel back-end in Set-top boxes

Description

The RC5512 can be used for driving key functions that are needed in all multimedia PCs and sound cards. These functions include directly powering speakers and headphone sets, providing a microphone pre-amplifier with AGC, and having a 12V to 5V regulator that can isolate the noise from the sound channel. Each function can be controlled individually, thus providing power saving features.

Block Diagram



Functional Description

The Rapper Stereo Sound Driver is an audio device that can be used on PC motherboards and add-in sound cards. It consists of stereo output drivers for headphone or speakers, a low noise microphone amplifier with AGC, and a regulator to provide a clean 5V supply. The RC5512 has two microphone inputs which are user selectable. Each section can be individually put into a shut-down mode and muted by pulling the appropriate pin low.

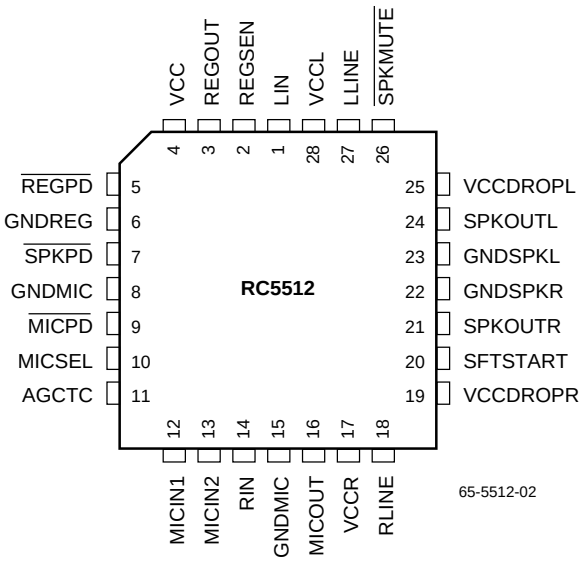
The output drivers can deliver up to 2 watts peak and 4 watts peak into 8Ω and 4Ω speakers, respectively, from a 12V source. The drivers use class AB amplifiers and maintain a low bias current. The power-down function is designed to save power and to turn on/off the driver without generating *popping* signals. To prevent popping signals, when the circuit is activated, a delay is provided to these output drivers. These drivers become active only after their outputs have settled. The time constant is user-defined through an external capacitor (C_{DELAY}) on the SFTSTART pin.

The microphone amplifier feeds into an AGC with a dynamic range of 40dB. An external capacitor is used to provide attack and decay features. Attack and decay times can be varied linearly by varying an external capacitor (C_{AD}) on the AGCTC pin. The attack and decay time ratio has been set for pleasant audio quality.

The 12 V to 5V voltage regulator can provide up to 20mA of current without external components. It can provide a noise-free regulated voltage supply to the other devices that complete the sound channel. Use of an external transistor can boost the regulator output to 150mA or higher with the appropriate thermal precautions. The line regulation of 50dB improves the cross talk and the power supply rejection ratio of all other audio blocks that are supplied by the 5V source.

The thermal limiting circuitry activates if the chip temperature typically exceeds 150°C.

Pin Assignments



Pin Definitions

Pin Name	Pin Number	Description
LIN	1	Left Channel Input.
REGSEN	2	Regulator Sense Point.
REGOUT	3	Regulator 5V Output.
VCC	4	12V Power Supply Input.
$\overline{\text{REGPD}}$	5	Regulator Power-Down.
GNDREG	6	Regulator Ground.
$\overline{\text{SPKPD}}$	7	Speaker and Line Driver Power-Down.
GNDMIC	8, 15	Microphone Ground.
$\overline{\text{MICPD}}$	9	Microphone Power-Down.
MICSEL	10	Microphone Output Select. LOW selects MICIN1, HIGH selects MICIN2.
AGCTC	11	Attack and Decay Capacitor Pin.
MICIN1	12	Microphone Input 1.
MICIN2	13	Microphone Input 2.
RIN	14	Right Channel Input.
MICOUT	16	Microphone Output.
VCCR	17	Right Speaker Supply.
RLINE	18	Right Line Driver Output.
VCCDROPR	19	Right Speaker Power Drop Supply.
SFTSTART	20	Soft Start Timing Capacitor.
SPKOUTR	21	Right Speaker Output.
GNDSPKR	22	Right Speaker Ground.
GNDSPKL	23	Left Speaker Ground.
SPKOUTL	24	Left Speaker Output.
VCCDROPL	25	Left Speaker Power Drop Supply.
$\overline{\text{SPKMUTE}}$	26	Speaker Mute.
LLINE	27	Left Line Driver Output.
VCCL	28	Left Speaker Supply.

Absolute Maximum Ratings[1]

(beyond which the device may be damaged)

Parameter		Min.	Typ.	Max.	Units
VCC	Power supply voltage			13.2	V

Note:

1. Functional operation under any of these conditions is NOT implied. Performance is guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter		Conditions	Min.	Typ.	Max.	Units
VCC VCCR VCCL	Power Supply		11.2	12	12.8	V
VCCDROPR VCCDROPL	Right and Left Power Drop Supplies	RDROP = 2Ω (See Figure 1)	11.2	12	12.8	V
V_{IH}	Input Voltage Logic High		2			V
V_{IL}	Input Voltage Logic Low				0.8	V
	Ambient Temperature		0		70	˚C
T_C	Maximum Operation Die Temperature	Overthermal Protection		150		˚C
I_{total}	Power Supply Current	No load		19	25	mA
I_{SD}	Shut-Down Current	$\overline{SPKPD}$, $\overline{MICPD}$, $\overline{REGPD} \le 0.4V$		10	75	μA
ESD	ESD Threshold	Human Body Model	2000			V

Electrical Characteristics

VCC = 12V ± 6%, unless otherwise specified.

Parameter		Conditions	Min.	Typ.	Max.	Units
Line Driver		f = 1KHz,RL = 600Ω unless otherwise specified				
Zin	Input Impedance			10		KΩ
Av	Voltage Gain	V_{IN} = 0.5 Vrms	0.95	1.0	1.05	V/V
L&R Av	Left and Right Gain Matching	V_{OUT} = 4V_{P-P}		0.3		%
Vo	Output Voltage	RL = 600Ω		±4		V
THD	Total Harmonic Distortion	V_{OUT} = 4V_{P-P}		0.01		%
PSRR	Power Supply Rejection Ratio	f = 100Hz, ΔVcc = 0.85Vrms	80	86		dB
SNR	Signal-to-Noise Ratio	V_{IN} = 2.8Vrms		85		dB
Speaker Driver		f = 1KHz, RL = 8Ω unless otherwise specified				
Ispk	Speaker Driver and Line Driver Supply Current	V_{IN} = 0V		9		mA
Zin	Input Impedance		100			KΩ
Av	Voltage Gain	V_{IN} = 0.5 Vrms	-3.8	-4.0	-4.2	V/V
L&R Av	Left and Right Gain Matching	V_{OUT} = 4V_{P-P}		0.5		%
Vo	Output Voltage	RL = 4 Ω or 8Ω, VCC = 12V		±4		V_{pK}

Electrical Characteristics (continued)

VCC = 12V ± 6%, unless otherwise specified.

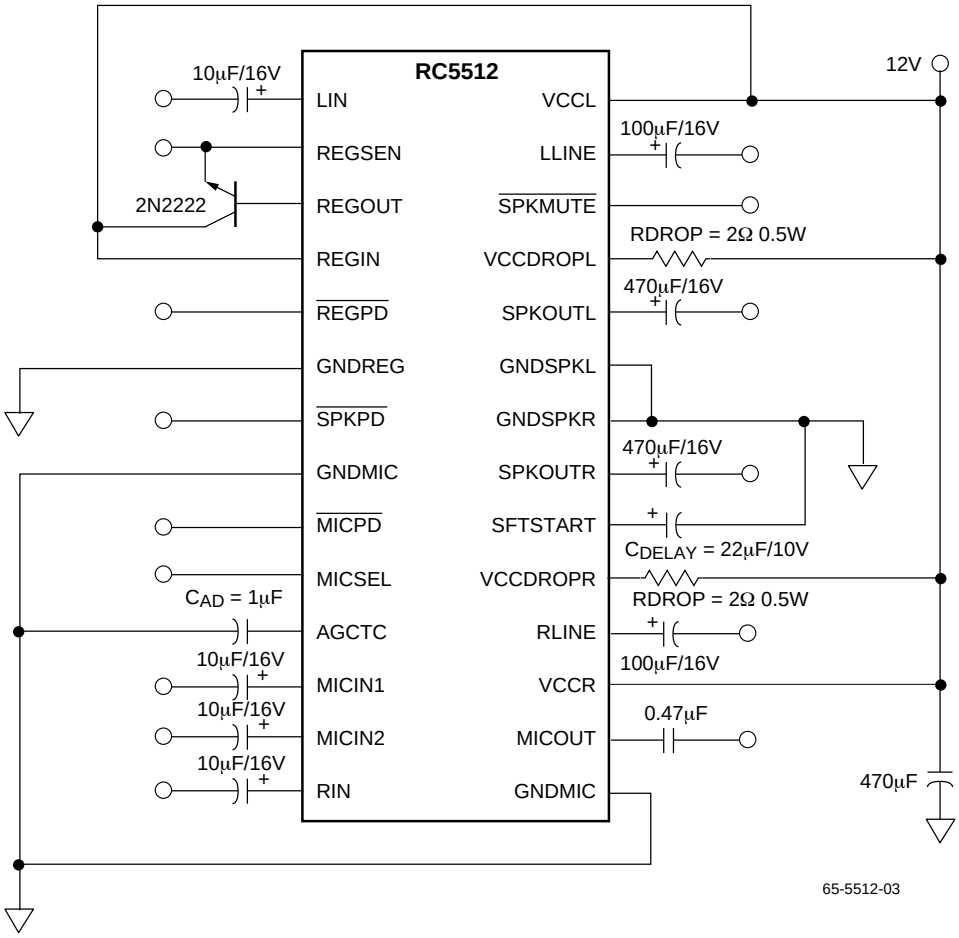
Parameter		Conditions	Min.	Typ.	Max.	Units
SNR	Signal-to-Noise Ratio	V_{IN} = 2.8Vrms		85		dB
Po	Power Output Per Channel Peak	RL = 4Ω, VCC = 12V		4		W
CS	Channel Separation L/R Input Referenced	V_{IN} = 0.5 Vrms	66			dB
XTALK	Cross Talk L/R to Mic Input Referenced	V_{IN} = 0.5 Vrms	90			dB
XTALK	Cross Talk L/R to Reg Input Referenced	V_{IN} = 0.5 Vrms	75			dB
THD	Total Harmonic Distortion	fo = 1KHz, Po = 50mW		0.1		%
Noise		20Hz - 20KHz, A-Weighted		4		μVrms
PSRR	Power Supply Rejection Ratio Input Referenced	f = 100Hz, ΔVCC = 1.6Vp-p	70	80		dB
Microphone Amplifier		f = 1KHz,RL = 10KΩ unless otherwise specified				
Imicamp	Microphone Amp Supply Current	V_{IN} = 0V, max gain		4		mA
Zin1	First Amp Input Impedance			4.5		KΩ
Av1	First Amp Gain			1		V/V
Av2	Second Amp Gain			-10		V/V
AGC	AGC Dynamic Range			40		dB
THD	Total Harmonic Distortion	Vin = 5mV_{P-P}, AGC off		0.1		%
Noise		20Hz - 20KHz, A-Weighted		8		μVrms
XTALK	XTALK from other blocks at MICOUT	V_{IN} = 1Vrms at 1KHz	70			dB
PSRR	Input Referenced	f = 100Hz, ΔVCC = 1.6Vp-p	70			dB
Voltage Regulator						
Ireg	Voltage Regulator Supply Current			1.5		mA
Vreg	Regulator Voltage		4.75	5	5.25	V
Tc	Tempco			0.5		mV/˚C
	Line Regulation			3		mV/V
	Load Regulation			2		mV/mA
Io	Output Current	Source		20		mA
		Source With External 2N2222		150		mA
		Sink		100		μA
Soft Start						
Delay	Anti-Pop Ramp-Up and Ramp-Down time	No Pop condition C_{DELAY} = 22μF on SFTSTART		2		sec

Power-Down Function Table

L = $V_{IL} \leq 0.8V$, H = $V_{IH} \geq 2.0V$, X = Don't Care

$\overline{\text{SPKPD}}$	$\overline{\text{MICPD}}$	$\overline{\text{REGPD}}$	$\overline{\text{SPKMUTE}}$	Function
L	L	L	X	Chip Disabled
H	H	H	H	All Sections Enabled
H	L	L	L	Line Driver Enabled, Regulator and Microphone Disabled, Speaker Muted
L	H	H	X	Line Driver and Speaker Disabled, Regulator and Microphone Enabled
H	L	H	H	Microphone Only Disabled
H	H	L	H	Regulator Only Disabled

Applications Discussion



Notes:

1. 4 Watt power represents the peak of the audio level and cannot be sustained without correct package thermal considerations. The average audio signal can be sustained by the RC5512 without extra thermal considerations.
2. To improve the thermal resistance of the PLCC 28 package, a heat sink can be used. One possible vendor is: AAVID, P/N CLC12059501.

Figure 1. Rapper™ RC5512, 4 Ohm Speaker, 4 Watt Application with External Pass Transistor for Voltage Regulator.

Portable PC Application

Figure 2 shows an application of the RC5512 for portable PCs when a high current, regulated 12 volts is not available. Because the portable PC's battery voltage can exceed the VCC maximum specification of the RC5512, a low drop out linear regulator with power down has been included. The linear regualtor provides 12 volts of regulation even if the battery voltage exceeds 20 volts. In addition, the low drop out regulator allows good sound quality even when the battery voltage drops to 9 volts. The low power down current bias of the regulator minimizes the battery current drain when the RC5512 is in a sleep mode.

Alternatively, if a regulated 12 volt supply is available with a minimum current output of 300mA and sufficient by-pass capacitance, no additional regulation is required.

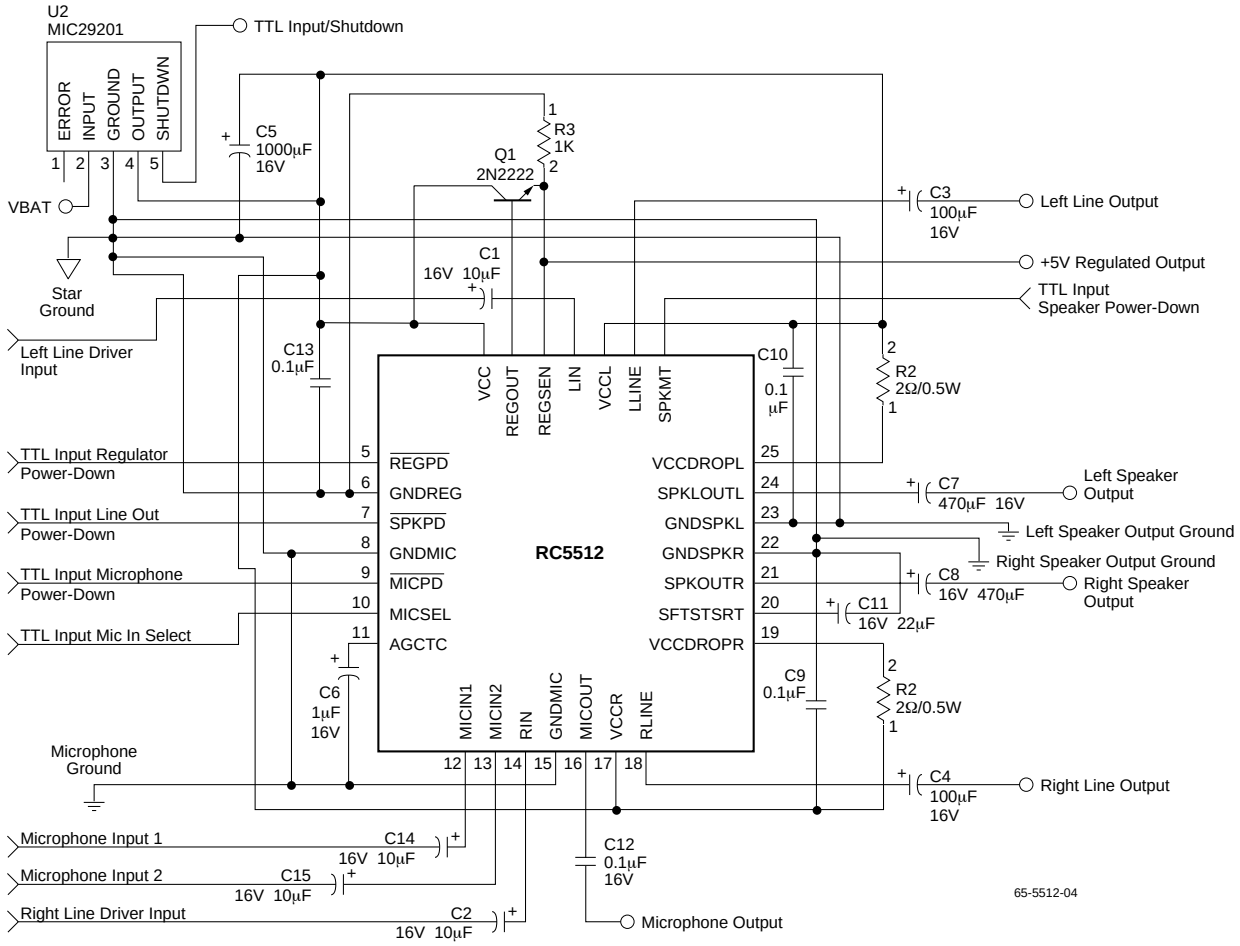


Figure 2. RC5512 Portable PC Application.

Notes:

Notes:

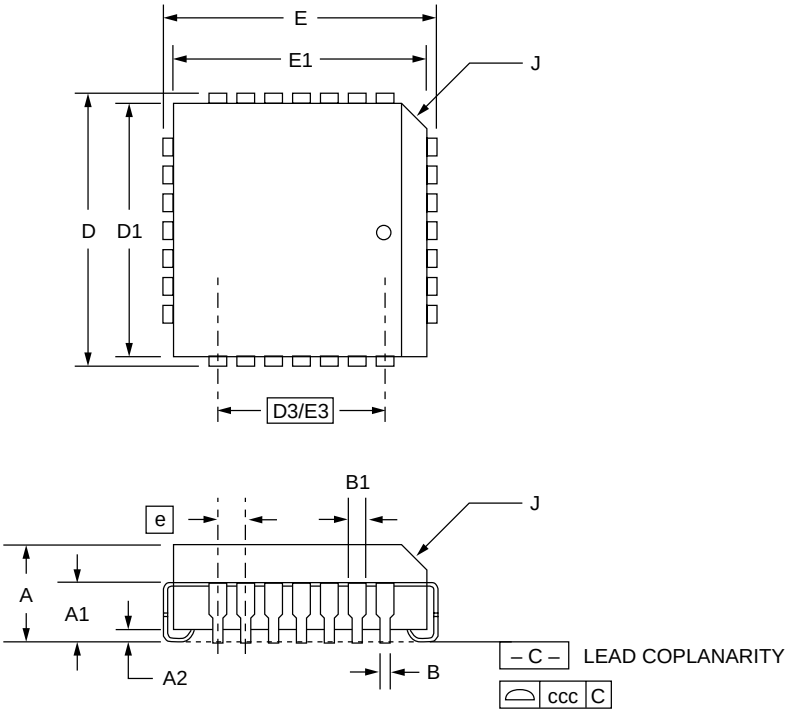
Notes:

Mechanical Dimensions – 28 Lead PLCC Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.180	4.19	4.57	
A1	.090	.120	2.29	3.05	
A2	.020	—	.51	—	
B	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D/E	.485	.495	12.32	12.57	
D1/E1	.450	.456	11.43	11.58	3
D3/E3	.300 BSC		7.62 BSC		
e	.050 BSC		1.27 BSC		
J	.042	.048	1.07	1.22	2
ND/NE	7		7		
N	28		28		
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982
2. Corner and edge chamfer (J) = 45°
3. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is .101" (.25mm)



Ordering Information

Product Number	Package
RC5512V	28 PLCC

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Stock#DS30005512

RC5513

RAPPER™ Family – 4 Watt Stereo Sound Driver

Features

- Up to 4W/channel
- Drives 8Ω and 4Ω non-powered speakers
- NO-POP during power-up/power-down and mute
- Provides regulated 5V supply for sound codec, etc.
- Line Output signal to noise ratio of 85 dB
- Microphone amplifier and AGC dynamic range of 40dB
- Microphone multiplexing
- Internal thermal limiting circuitry
- 24 Lead SOIC package
- Total Harmonic Distortion < 0.1%

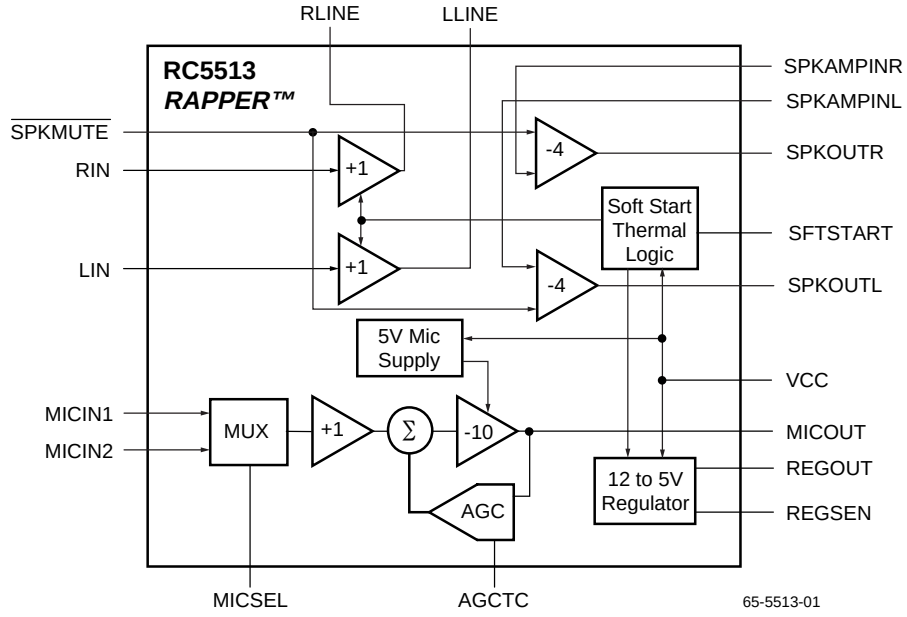
Applications

- Multimedia PC motherboards and add-in sound cards
- Companion chip to Sigma-Delta Sound Codecs
- Sound Channel back-end in Set-top boxes

Description

The Rapper is a stereo sound driver used for driving key functions that are needed in all multimedia PCs and sound cards. These functions include directly powering speakers and headphone sets, providing a microphone pre-amplifier with AGC, and having a 12V to 5V regulator that can isolate the noise from the sound channel.

Block Diagram



Functional Description

The Rapper Stereo Sound Driver is an audio device that can be used on PC motherboards and add-in sound cards. It consists of stereo output drivers for headphone or speakers, a low noise microphone amplifier with AGC, and a regulator to provide a clean 5V supply.

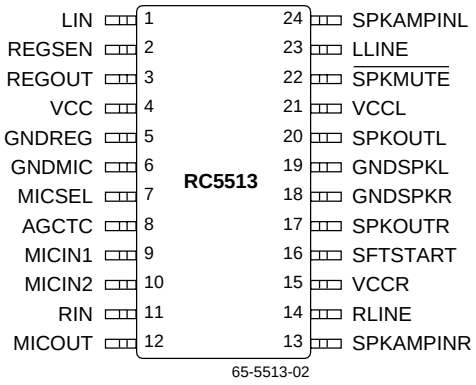
The output drivers can deliver up to 2 Watts peak and 4 Watts peak into 8Ω and 4Ω speakers, respectively, from a 12V source. The drivers use class AB amplifiers and maintain a low bias current. To help prevent popping signals a delay is provided to these output drivers to allow settling. The time constant is user-defined through an external capacitor (C_{DELAY}) on the SFTSTART pin.

The microphone amplifier feeds into an AGC with a dynamic range of 40dB. An external capacitor is used to provide attack and decay features. Attack and decay times can be varied linearly by varying an external capacitor (C_{AD}) on the AGCTC pin. The attack and decay time ratio has been set for pleasant audio quality.

The 12 V to 5V voltage regulator can provide up to 20mA of current without external components. It can provide a clean regulated voltage supply to the other devices that complete the sound channel. Use of an external transistor can boost the regulator output to 150mA or higher with the appropriate thermal precautions. The line regulation of 50dB improves the cross talk and the power supply rejection ratio of all other audio blocks that are supplied by the 5V source.

The thermal limiting circuitry activates if the chip temperature typically exceeds 150°C.

Pin Assignments



65-5513-02

Pin Definitions

Pin Name	Pin Number	Pin Function Description
LIN	1	Left Channel Input
REGSEN	2	Regulator Sense Point
REGOUT	3	Regulator 5V Output
VCC	4	12V Power Supply Input
GNDREG	5	Regulator Ground
GNDMIC	6	Microphone Ground
MICSEL	7	MICOUT Select. LOW selects MICIN1, HIGH selects MICIN2
AGCTC	8	Attack and Decay Capacitor Pin
MICIN1	9	Microphone Input 1
MICIN2	10	Microphone Input 2
RIN	11	Right Channel Input
MICOUT	12	Microphone Output
SPKAMPINR	13	Right Channel Power Amplifier Input
RLINE	14	Right Line Driver Output
VCCR	15	Right Speaker Supply
SFTSTART	16	Soft Start Timing Capacitor
SPKOUTR	17	Right Speaker Output
GNDSPKR	18	Right Speaker Ground
GNDSPKL	19	Left Speaker Ground
SPKOUTL	20	Left Speaker Output
VCCL	21	Left Speaker Supply
$\overline{\text{SPKMUTE}}$	22	Speaker Mute
LLINE	23	Left Line Driver Output
SPKAMPINL	24	Left Channel Power Amplifier Input

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min	Typ	Max	Units
VCC	Power supply voltage			13.2	V

Note:

1. Functional operation under any of these conditions is NOT implied. Performance is guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter		Conditions	Min	Typ	Max	Units
VCC VCCR VCCL	Power Supply		11.2	12	12.8	V
V_{IH}	Input Voltage Logic High		2			V
V_{IL}	Input Voltage Logic Low				0.8	V
	Ambient Temperature		0		70	˚C
T_C	Maximum Operation Die Temperature	Overthermal Protection		150		˚C
I_{total}	Power Supply Current	No load		19	25	mA
ESD	ESD Threshold	Human Body Model	2000			V

Electrical Characteristics

V_{CC} = 12V ± 6%, unless otherwise specified.

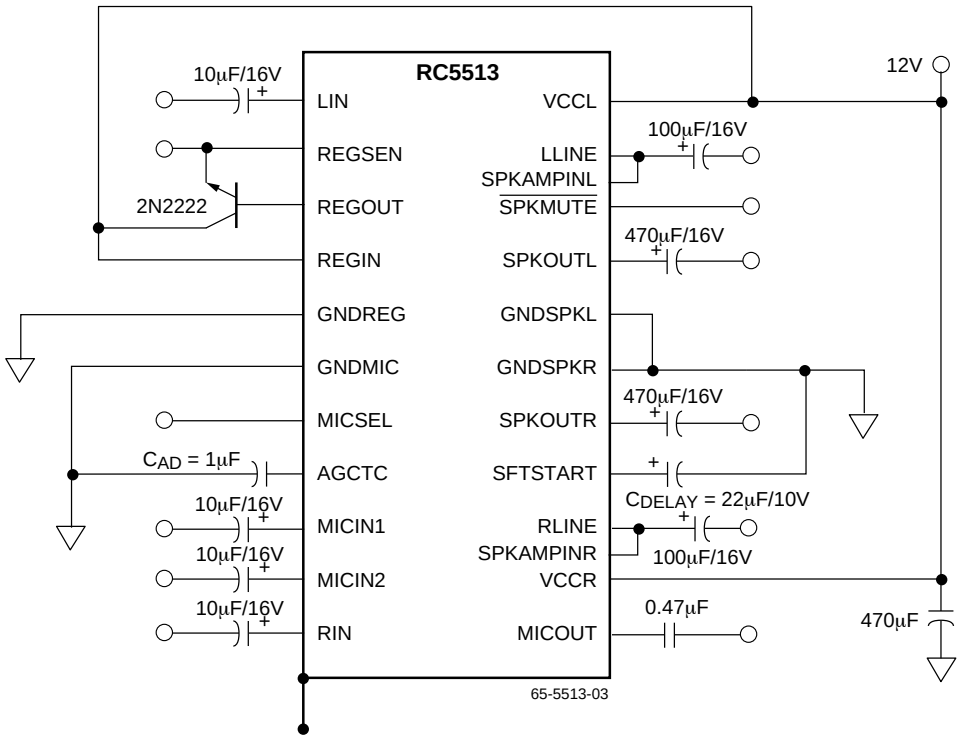
Parameter		Conditions	Min	Typ	Max	Units
Line Driver		f = 1KHz,RL = 600Ω unlees otherwise specified				
Zin	Input Impedance			10		KΩ
Av	Voltage Gain	Vin = 1 Vrms	0.95	1.0	1.05	V/V
L&R Av	Left and Right Gain Matching	Vout = $4V_{P-P}$		0.3		%
Vo	Output Voltage	RL = 600Ω		±4		V
THD	Total Harmonic Distortion	Vout = $4V_{P-P}$		0.01		%
PSRR	Power Supply Rejection Ratio	f = 100Hz, ΔVcc = 0.85Vrms	80	86		dB
SNR	Signal to Noise Ratio	Vin = 2.8V rms		85		dB
Speaker Driver		f = 1KHz, RL = 8Ω unless otherwise specified				
Ispk	Speaker Driver Supply Current	Vin = 0V		5		mA
Zin	Input Impedance		100			KΩ
Av	Voltage Gain	Vin = 0.5 Vrms	3.80	-4.0	-4.20	V/V
L&R Av	Left and Right Gain Matching	Vout = $4V_{P-P}$		0.5		%
Vo	Output Voltage	RL = 4Ω or 8Ω, VCC = 12V		±4		V
SNR	Signal to Noise Ratio	Input Referenced		85		dB

Electrical Characteristics (continued)

V_{CC} = 12V ± 6%, unless otherwise specified.

Parameter		Conditions	Min	Typ	Max	Units
Po	Power Output Per Channel Peak	RL = 4Ω, VCC = 12V (See Figure 1)		4		W
CS	Channel Separation L/R Input Referenced	Vin = 0.5 Vrms	66			dB
XTALK	Cross Talk L/R to Mic Input Referenced	Vin = 1 mVrms	90			dB
XTALK	Cross Talk L/R to Reg Input Referenced	Vin = 0.5 Vrms	75			dB
THD	Total Harmonic Distortion	fo = 1KHz, Po = 50mW		0.1		%
Noise		20Hz to 20kHz, A-Weighted		4		μVrms
PSRR	Power Supply Rejection Ratio Input Referenced	f = 100Hz, ΔVcc = 1.6Vp-p	70	80		dB
Microphone Amplifier		f = 1KHz,RL = 10KΩ unless otherwise specified				
Imicamp	Microphone Amp Supply Current	Vin = 0V, max gain		4		mA
Zin1	First Amp Input Impedance			4.5		KΩ
Av1	First Amp Gain			1		V/V
Av2	Second Amp Gain			-10		V/V
AGC	AGC Dynamic Range			40		dB
THD	Total Harmonic Distortion	Vin = 5mVP-P, AGC off		0.1		%
Noise		20Hz to 20kHz, A-Weighted		8		μVrms
XTALK	XTALK from other blocks at MICOUT	Vin = 1Vrms at 1KHz	70			dB
PSRR	Input Referenced	f = 100Hz, ΔVcc = 1.6Vp-p	70			dB
Voltage Regulator						
Ireg	Voltage Regulator Supply Current			1.5		mA
Vreg	Regulator Voltage		4.75	5	5.25	V
Tc	Tempco			0.5		mV/°C
	Line Regulation			3		mV/V
	Load Regulation			2		mV/mA
Io	Output Current	Source		20		mA
		Source With External 2N2222		150		mA
		Sink		100		μA
Soft Start						
Delay	Anti-Pop Ramp-Up and Ramp-Down time	No Pop condition C_{DELAY} = 22μF on SFTSTART		2		sec

Applications Discussion



Notes:

1. 4 watt power represents the peak of the audio level and cannot be sustained without correct package thermal considerations. The average audio signal can be sustained by the RC5513 without extra thermal considerations.
2. To improve the thermal resistance of the SOIC package a heat sink can be used.

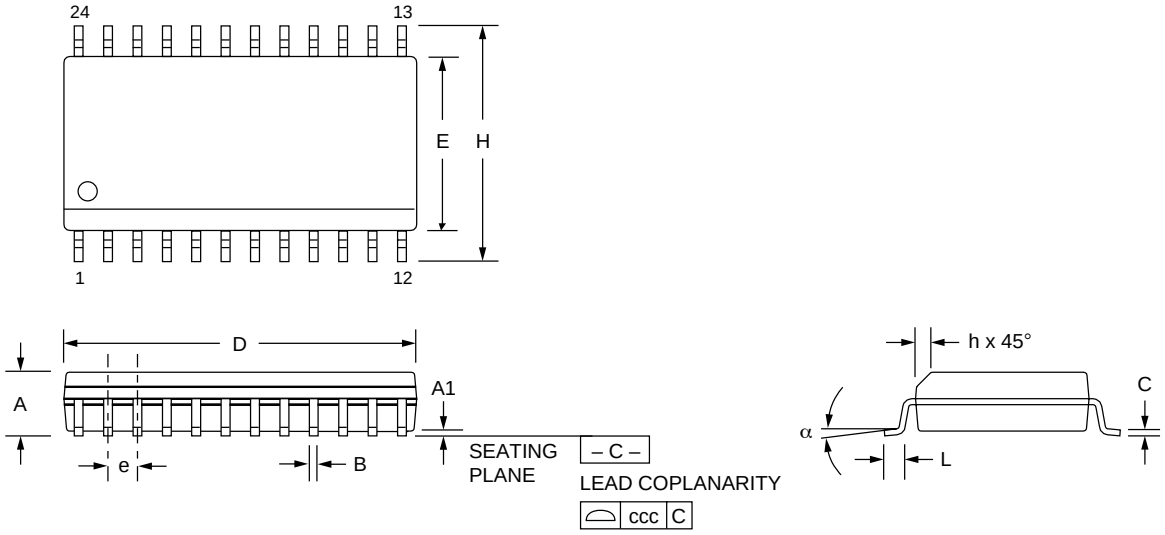
Figure 1. Rapper™ RC5513, 4 Ohm Speaker, 4 Watt Application with External Pass Transistor for Voltage Regulator

Mechanical Dimensions – 24 Lead SOIC Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.599	.614	15.20	15.60	2
E	.290	.299	7.36	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.020	0.25	0.51	
L	.016	.050	0.40	1.27	3
N	24		24		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.



Ordering Information

Product Number	Package
RC5513M	24 SOIC

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

5/20/98 0.0m 001
Stock#DS30005513

RC5532/RC5532A

High Performance Dual Low Noise Operational Amplifier

Features

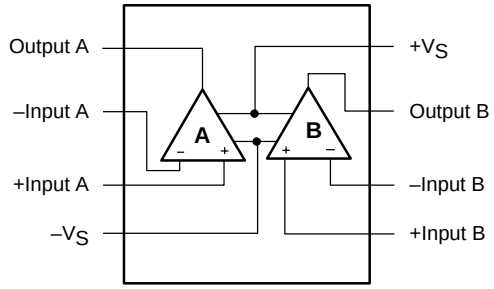
- Small signal bandwidth – 10 MHz
- Output drive capability – 600Ω, 10 VRMS
- Input noise voltage – 5 nV/$\sqrt{\text{Hz}}$
- DC voltage gain – 50,000
- AC voltage gain – 2200 at 10 KHz
- Power bandwidth – 140 KHz
- Slew rate – 8 V/μS
- Large supply voltage range – ±3V to ±20V

Description

The RC5532 is a high performance, dual low noise operational amplifier. Compared to standard dual operational amplifiers, such as the RC747, it shows better noise performance, improved output drive capability, and considerably higher small-signal and power bandwidths.

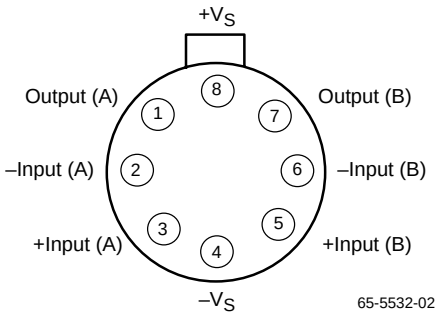
This makes the device especially suitable for application in high quality and professional audio equipment, instrumentation, control circuits, and telephone channel amplifiers. The op amp is internally compensated for gains equal to one. If very low noise is of prime importance, it is recommended that the RC5532A version be used which has guaranteed noise specifications.

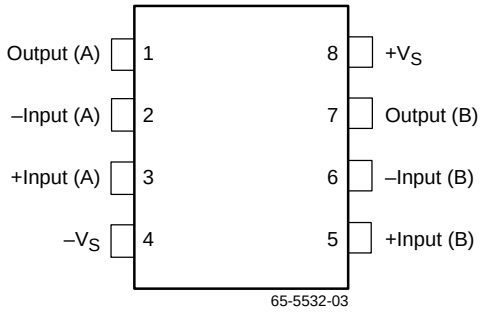
Block Diagram



65-5532-01

Pin Assignments





Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min.	Typ.	Max.	Units
Supply Voltage				±22	V
Input Voltage				±V_S	V
Differential Input Voltage				0.5	V
P_D T_A < 50°C	PDIP			468	mW
	CerDIP			833	
	SOIC			658	
Junction Temperature	PDIP			125	°C
	CerDIP, TO-99			175	
Storage Temperature		-65		150	°C
Operating Temperature	RM5532/A	-55		125	°C
	RC5532/A	0		70	
Lead Soldering Temperature (10 sec)				300	°C

Notes:

1. Functional operation under any of these conditions is NOT implied.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit to ground on one amplifier only.

Operating Conditions

Parameter			Min.	Typ.	Max.	Units
θ_{JC}	Thermal resistance	CerDIP		45		°C/W
		TO-99		50		
θ_{JA}	Thermal resistance	PDIP		160		°C/W
		CerDIP		150		
		TO-99		190		
For T_A > 50°C Derate at		PDIP		6.25		mW/°C
		CerDIP		8.33		
		TO-99		5.26		

DC Electrical Characteristics

(V_S = ±15V and T_A = +25˚C unless otherwise noted)

Parameters	Test Conditions	RM5532/5532A			RC5532/5532A			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage			0.5	2.0		0.5	4.0	mV
	Over Temperature			3.0			5.0	mV
Input Offset Current				100		10	150	nA
	Over Temperature			200			200	nA
Input Bias Current			200	400		200	800	nA
	Over Temperature			700			1000	nA
Supply Current			6.0	11		6.0	16	mA
	Over Temperature			13			22	mA
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio		80	100		70	100		dB
Power Supply Rejection Ratio		86	100		80	100		dB
Large Signal Voltage Gain	$R_L \geq 2$ KΩ, V_{OUT} = ±10V	50			25	100		V/mV
	Over Temperature	25			15	50		
	$R_L \geq 600\Omega$, V_{OUT} = ±10V	40			15	50		
	Over Temperature	20			10			
Output Voltage Swing	$R_L \geq 600\Omega$	±12	±13		±12	±13		V
	R_L = 600Ω, V_S = ±18V	±15	±16		±15	±16		
	$R_L \geq 2k\Omega$	±12	±13					
Input Resistance (Diff. Mode)			300			300		KΩ
Short Circuit Current			38			38		mA

Notes:

1. Diodes protect the inputs against over-voltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum input current should be limited to ±10mA.
2. Over Temperature: RM = 55 °C ≤ T_A ≤ 125°C; RC = 0°C ≤ T_A ≤70°C

Electrical Characteristics

(V_S = ±15V and T_A = +25°C)

Parameters	Test Conditions	RC/RM5532			RC/RM5532A			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Noise Voltage Density	F_O = 30 Hz		8.0			8.0	12	nV/$\sqrt{Hz}$
	F_O = 1 kHz		5.0			5.0	6.0	
Input Noise Current Density	F_O = 30 Hz		2.7			2.7		pA/$\sqrt{Hz}$
	F_O = 1 kHz		0.7			0.7		
Channel Separation	F = 1 kHz, R_S = 5 kΩ		110			110		dB

AC Electrical Characteristics

(V_S = ±15V and T_A = +25°C)

Parameters	Test Conditions	Min.	Typ.	Max.	Units
Output Resistance	A_V = 30 dB Closed Loop, F = 10 kHz, R_L = 600Ω		0.3		Ω
Overshoot	Unity Gain, V_{IN} = 100 mV_{p-p} C_L = 100 pF, R_L = 600Ω		10		%
Gain	F = 10 KHz		2.2		V/mV
Gain Bandwidth Product	C_L = 100 pF, R_L = 600Ω		10		MHz
Slew Rate			8.0		V/μS
Power Bandwidth	V_{OUT} = ±10V		140		KHz
	V_{OUT} = ±14V, R_L = 600Ω, V_S = ±18V		100		KHz

Test Circuits

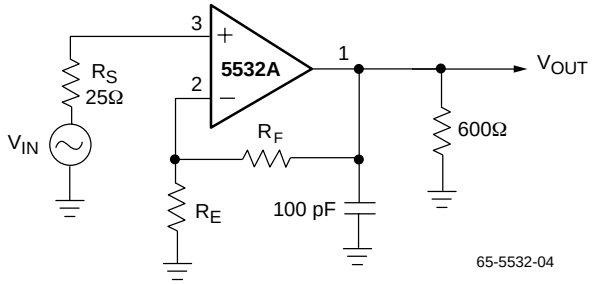


Figure 1. Closed Loop Frequency Response

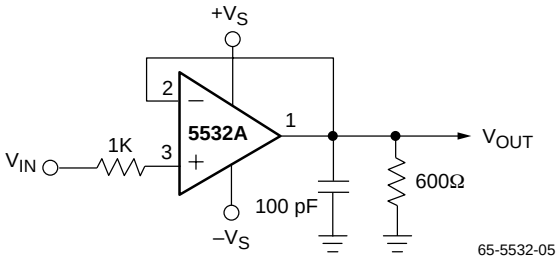


Figure 2. Follower, Transient Response

Typical Performance Characteristics

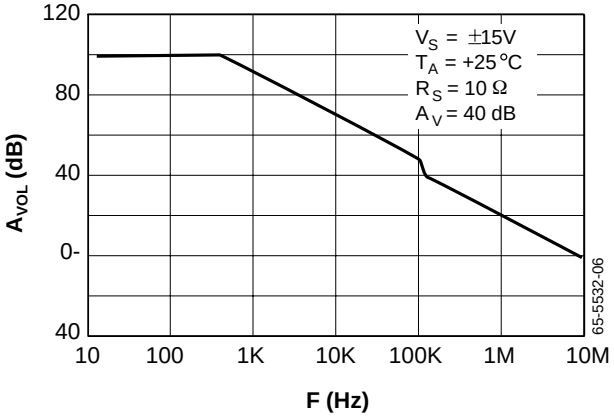


Figure 3. Open Loop Gain vs. Frequency

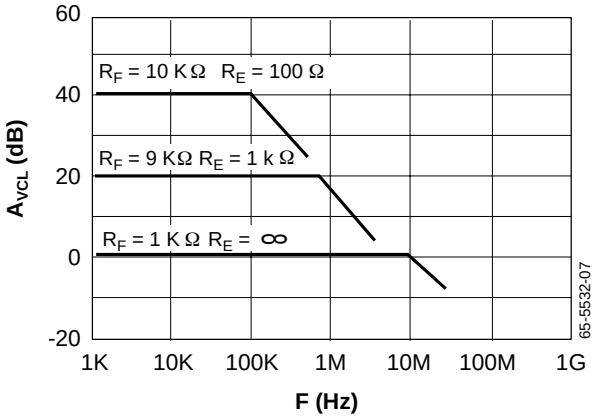


Figure 4. Closed Loop Gain vs. Frequency

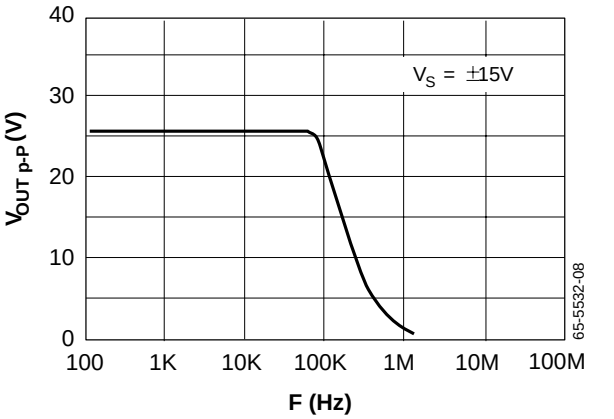


Figure 5. Output Voltage Swing vs. Frequency

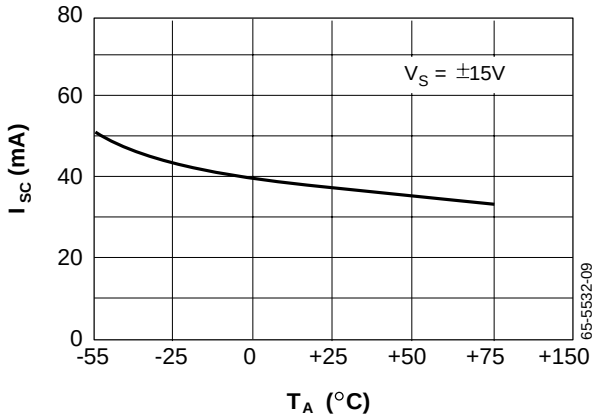


Figure 6. Short Circuit Current vs. Temperature

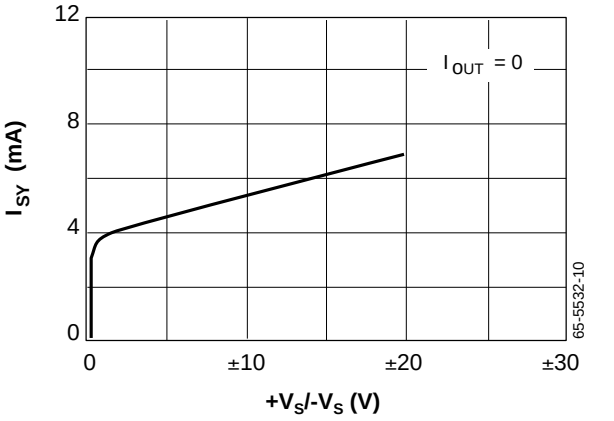


Figure 7. Supply Current vs. Supply Voltage

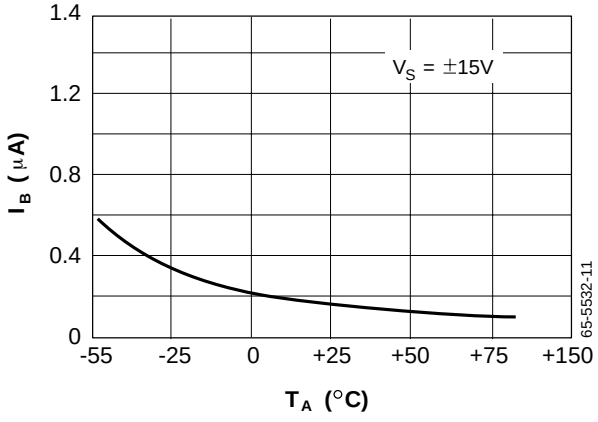


Figure 8. Input Bias Current vs. Temperature

Typical Performance Characteristics (continued)

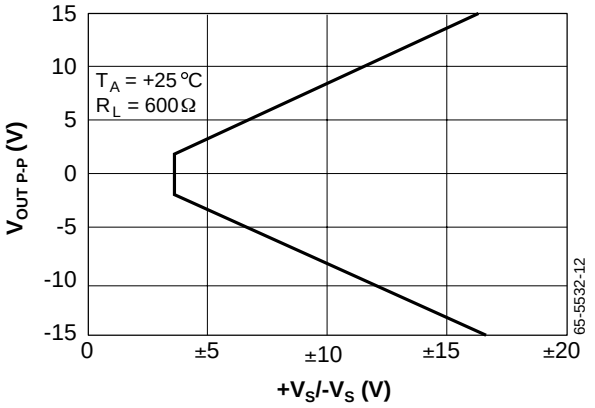


Figure 9. Output Voltage Swing vs. Supply Voltage

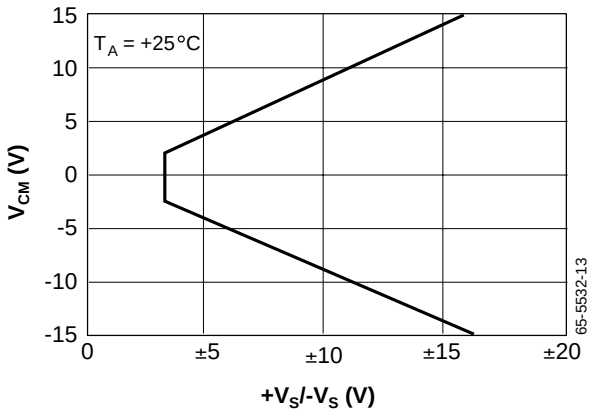


Figure 10. Common Mode Input Range vs. Supply Voltage

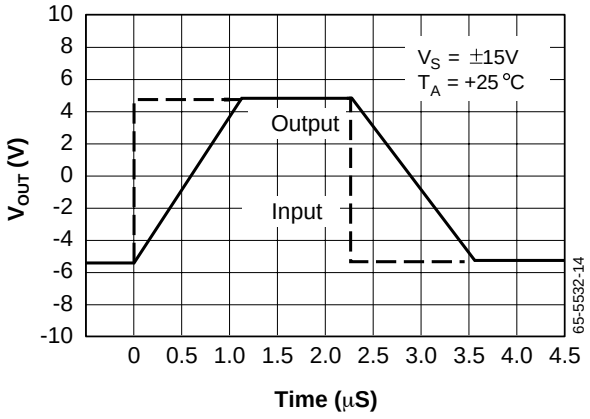


Figure 11. Follower Large Signal Pulse Response

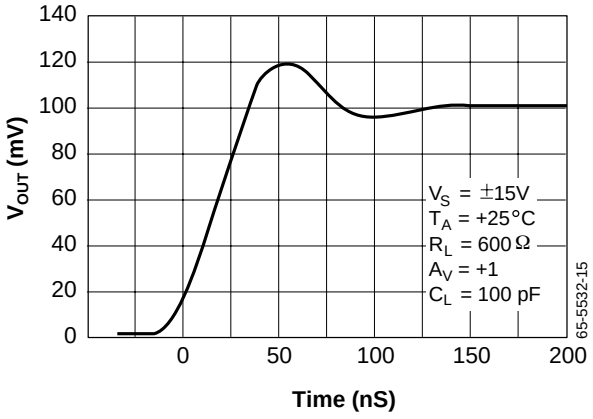


Figure 12. Transient Response Output Voltage vs. Time

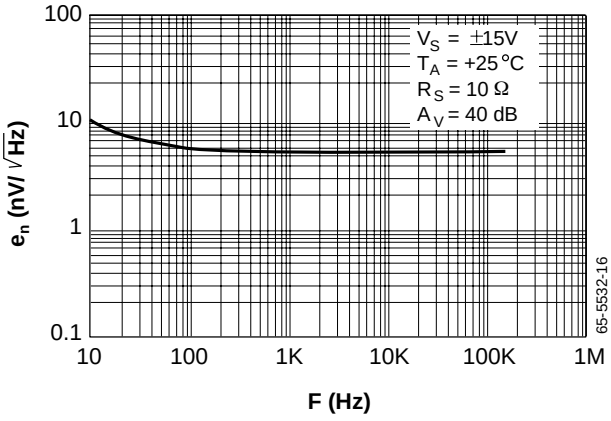


Figure 13. Input Noise Density vs. Frequency

Notes:

Notes:

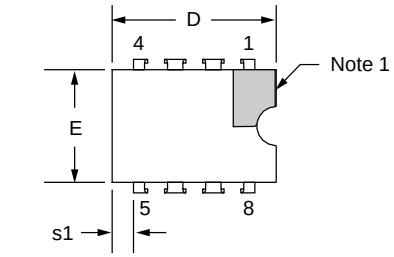
Mechanical Dimensions

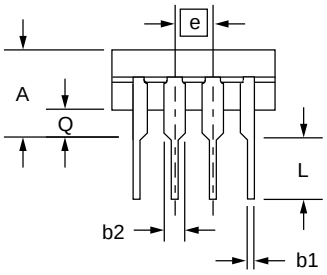
8-Lead Ceramic DIP Package

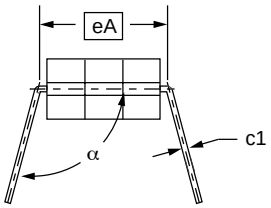
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2, 8
c1	.008	.015	.20	.38	8
D	—	.405	—	10.29	4
E	.220	.310	5.59	7.87	4
e	.100 BSC		2.54 BSC		5, 9
eA	.300 BSC		7.62 BSC		7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 4, 5 and 8 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 8.
6. Applies to all four corners (leads number 1, 4, 5, and 8).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Six spaces.







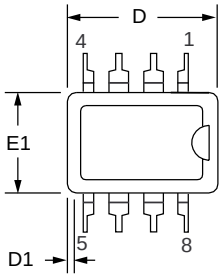
Mechanical Dimensions (continued)

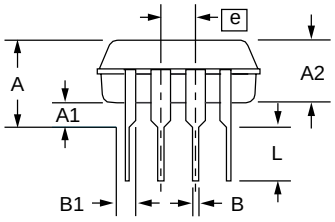
8-Lead Plastic DIP Package

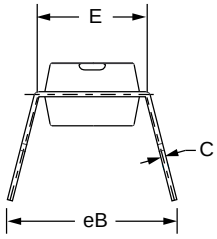
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	.348	.430	8.84	10.92	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.160	2.92	4.06	
N	8°		8°		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.

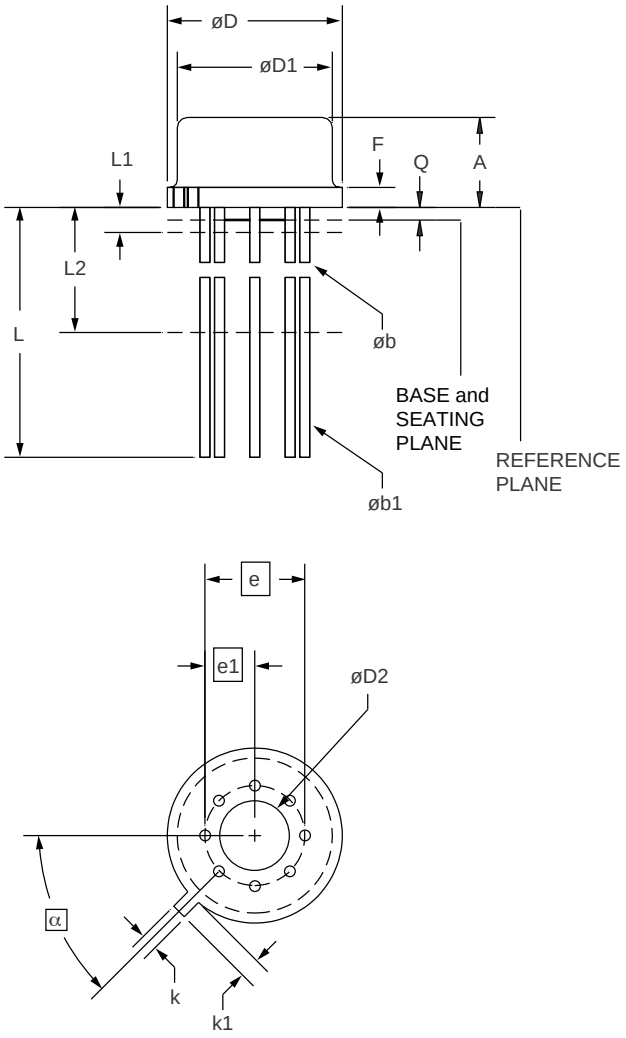






Mechanical Dimensions (continued)

8-Lead Metal Can IC Header Package



Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.185	4.19	4.70	
øb	.016	.019	.41	.48	1, 5
øb1	.016	.021	.41	.53	1, 5
øD	.335	.375	8.51	9.52	
øD1	.305	.335	7.75	8.51	
øD2	.110	.160	2.79	4.06	
e	.200 BSC		5.08 BSC		
e1	.100 BSC		2.54 BSC		
F	—	.040	—	1.02	
k	.027	.034	.69	.86	
k1	.027	.045	.69	1.14	2
L	.500	.750	12.70	19.05	1
L1	—	.050	—	1.27	1
L2	.250	—	6.35	—	1
Q	.010	.045	.25	1.14	
α	45° BSC		45° BSC		

Notes:

1. (All leads) øb applies between L1 & L2. øb1 applies between L2 & .500 (12.70mm) from the reference plane. Diameter is uncontrolled in L1 & beyond .500 (12.70mm) from the reference plane.
2. Measured from the maximum diameter of the product.
3. Leads having a maximum diameter .019 (.48mm) measured in gauging plane, .054 (1.37mm) +.001 (.03mm) –.000 (.00mm) below the reference plane of the product shall be within .007 (.18mm) of their true position relative to a maximum width tab.
4. The product may be measured by direct methods or by gauge.
5. All leads – increase maximum limit by .003 (.08mm) when lead finish is applied.

Ordering Information

Product Number	Temperature Range	Screening	Package
RC5532D/RC5532AD	0°C to +70°C	Commercial	8 Pin Ceramic DIP
RC5532N/RC5532AN	0°C to +70°C	Commercial	8 Pin Plastic DIP
RM5532D/RM5532AD	-55°C to +125°C	Commercial	8 Pin Ceramic DIP
RM5532D/883B	-55°C to +125°C	Military	8 Pin Ceramic DIP
RM5532AD/883B	-55°C to +125°C	Military	8 Pin Ceramic DIP
RM5532T/RM5532AT	-55°C to +125°C	Commercial	8 Pin TO-99 Metal Can
RM5532T/883B	-55°C to +125°C	Military	8 Pin TO-99 Metal Can
RM5532AT/883B	-55°C to +125°C	Military	8 Pin TO-99 Metal Can

Note:

1. /883B suffix denotes MIL-STD-883, Par. 1.2.1 compliant device.

5/20/98 0.0m 001
Stock#DS30005532

RC5534/RC5534A

High Performance Low Noise Operational Amplifier

Features

- Small signal bandwidth – 10 MHz
- Output drive capability – 600Ω, 10 V_{RMS} at V_S = ±18V
- Input noise voltage – 4 nV/√Hz
- DC voltage gain – 100,000
- AC voltage gain – 6000 at 10 kHz
- Power bandwidth – 200 kHz
- Slew rate – 13 V/μS
- Large supply voltage range – ±3V to ±20V

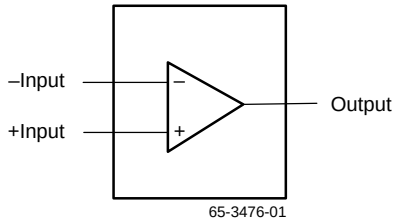
Description

The RC5534 is a high performance, low noise operational amplifier. This amplifier features popular pin-out, superior noise performance, and high output drive capability.

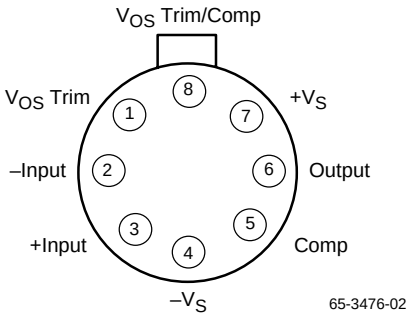
This amplifier also features guaranteed noise performance with substantially higher gain-bandwidth product, power bandwidth, and slew rate which far exceeds that of the 741 type amplifiers. The RC5534 is internally compensated for a gain of three or higher and may be externally compensated for optimizing specific performance requirements of various applications such as unity-gain voltage followers, drivers for capacitive loads or fast settling.

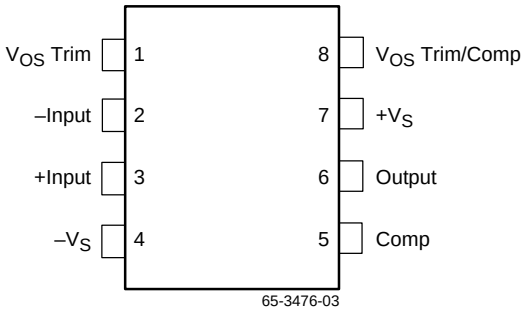
The specially designed low noise input transistors allow the RC5534 to be used in very low noise signal processing applications such as audio preamplifiers and servo error amplifiers.

Block Diagram



Pin Assignments





Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min	Typ	Max	Units
Supply Voltage				±22	V
Input Voltage				$\pm V_S$	V
Differential Input Voltage				0.5	V
$P_D T_A$ < 50°C	PDIP			468	mW
	CerDIP			833	
	SOIC			658	
Junction Temperature	PDIP			125	°C
	CerDIP, TO-99			175	
Storage Temperature		-65		150	°C
Operating Temperature	RM5534/A	-55		125	°C
	RC5534/A	0		70	
Lead Soldering Temperature (60 sec)				300	°C
Output Short Circuit Duration[2]		Indefinite			

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Short circuit may be to ground only. Rating applies to +125°C case temperature or +175°C junction temperature.

Operating Conditions

Parameter			Min	Typ	Max	Units
θ_{JC}	Thermal resistance	CerDIP		45		°C/W
		TO-99		50		
θ_{JA}	Thermal resistance	PDIP		160		°C/W
		CerDIP		150		
		TO-99		190		
For T_A > 50°C Derate at		PDIP		6.25		mW/°C
		CerDIP		8.33		
		TO-99		5.26		

Operating Conditions

(RM = -55°C ≤ T_A ≤ +125°C; RC = 0°C ≤ T_A ≤ + 70°C, V_S = ±15V)

Parameter	Test Conditions	RM5534/A			RC5534/A			Units
Input Offset Voltage	R_S ≤ 1 kΩ			3.0			5.0	mV
Input Offset Current				500			400	nA
Input Bias Current				1500			2000	nA
Large Signal Voltage Gain	R_L ≥ 600Ω, V_{OUT} = ±10V	25			15			V/mV
Output Voltage Swing	R_L ≥ 600Ω	±10			±10			V
Supply Current	V_S = ±15V, R_L = ∞			9.0			14	mA

DC Electrical Characteristics

(V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	RM5534/A			RC5534/A			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \le 1k\Omega$		0.5	2.0		0.5	4.0	mV
Input Offset Current			10	200		20	300	nA
Input Bias Current			400	800		500	1500	nA
Input Resistance (Diff. Mode)			100			100		kΩ
Large Signal Voltage Gain	$R_L \ge 600\Omega$, V_{OUT} = ±10V	50	100		25	100		V/mV
Output Voltage Swing	$R_L \ge 600\Omega$	±12	±13		±12	±13		V
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \le 1k\Omega$	80	100		70	100		dB
Power Supply Rejection Ratio	$R_S \le 1k\Omega$	86	100		86	100		dB
Supply Current	$R_L = \infty$		4.0	6.5		4.0	8.0	mA
Transient Response Rise Time	V_{IN} = 50 mV, R_L = 600Ω, C_L = 100 pF, C_C = 22 pF		35			35		nS
Overshoot			17			17		%
Slew Rate	C_C = 0		13			13		V/μS
Gain Bandwidth Product	C_C = 22 pF, C_L = 100 pF		10			10		MHz
Power Bandwidth	$V_{OUT} = 20V_{p-p}$, C_C = 0		200			200		kHz
Input Noise Voltage	F = 20 Hz to 20 kHz		1.0			1.0		μV_{RMS}
Input Noise Current	F = 20 Hz to 20 kHz		25			25		pA_{RMS}
Channel Separation	F = 1 kHz, R_S = 5 kΩ		110			110		dB

AC Electrical Characteristics

(V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	RC/RM5534A			RC/RM5534			Units
Input Noise Voltage Density	F_O = 30 Hz		5.5	7.0		7.0		nV/$\sqrt{Hz}$
	F_O = 1 kHz		3.5	4.5		4.0		
Input Noise Current Density	F_O = 30 Hz		1.5			2.5		pA/$\sqrt{Hz}$
	F_O = 1 kHz		0.4			0.6		
Broadband Noise Figure	F = 10 Hz - 20 kHz, RS = 5 kΩ		0.9					dB

Typical Performance Characteristics

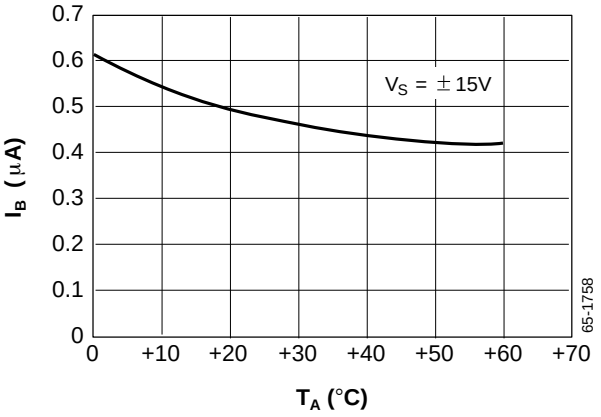


Figure 1. Input Bias Current vs. Temperature

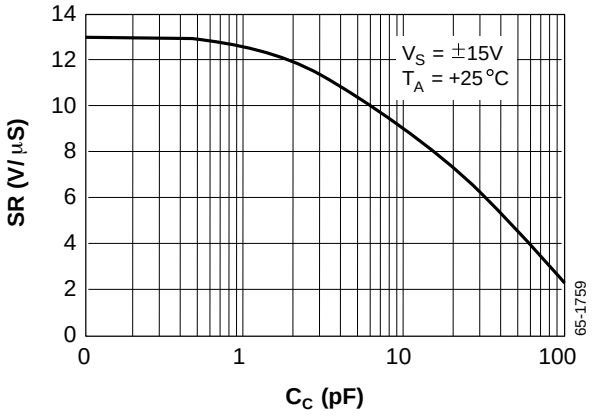


Figure 2. Slew Rate vs. Compensation Capacitor

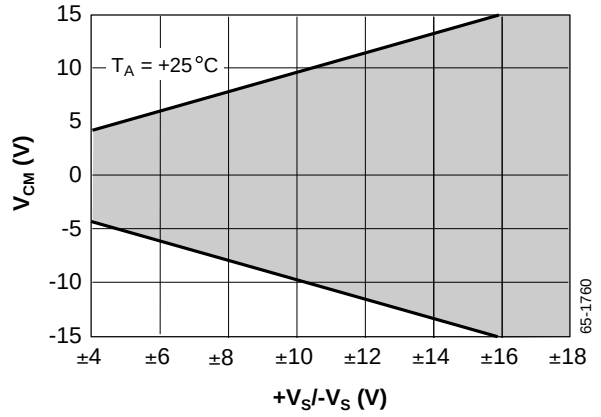


Figure 3. Common Mode Input Range vs. Supply Voltage

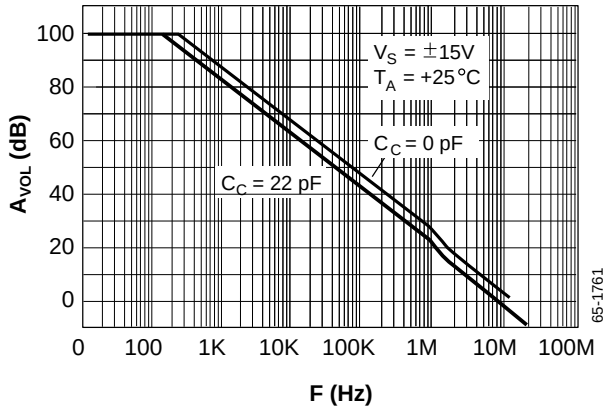


Figure 4. Open Loop Gain vs. Frequency

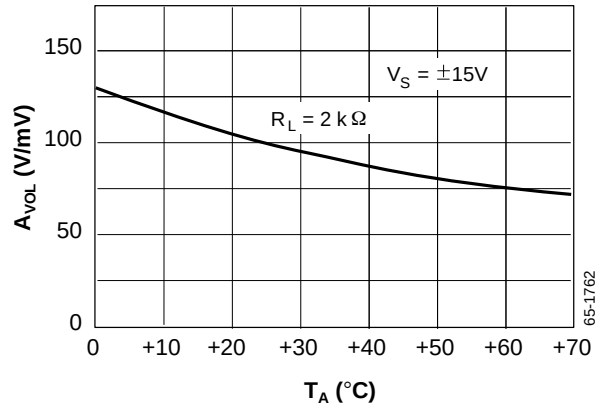


Figure 5. Open Loop Gain vs. Temperature

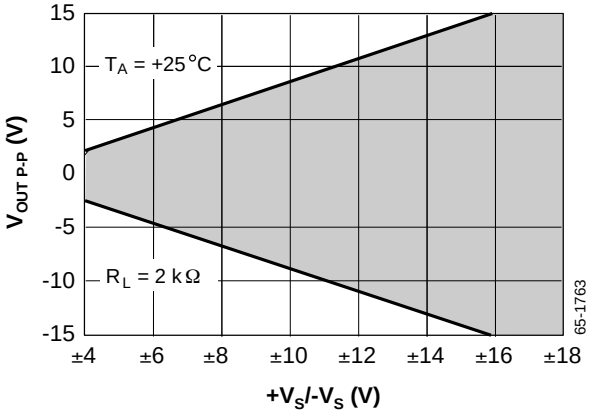


Figure 6. Output Voltage Swing vs. Supply Voltage

Typical Performance Characteristics (continued)

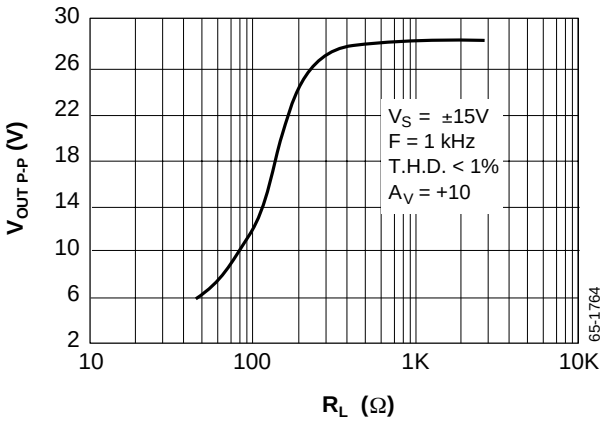


Figure 7. Output Voltage Swing vs. Load Resistance

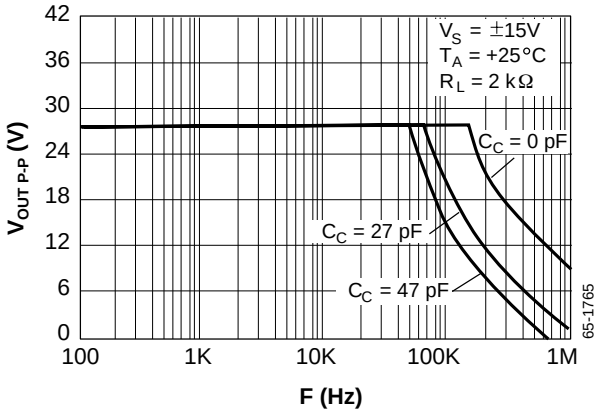


Figure 8. Output Voltage Swing vs. Frequency

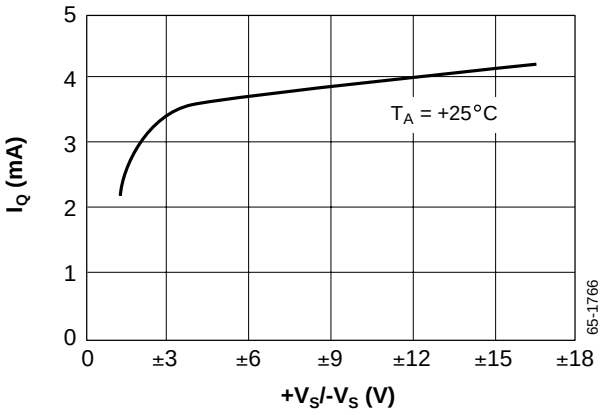


Figure 9. Quiescent Current vs. Supply Voltage

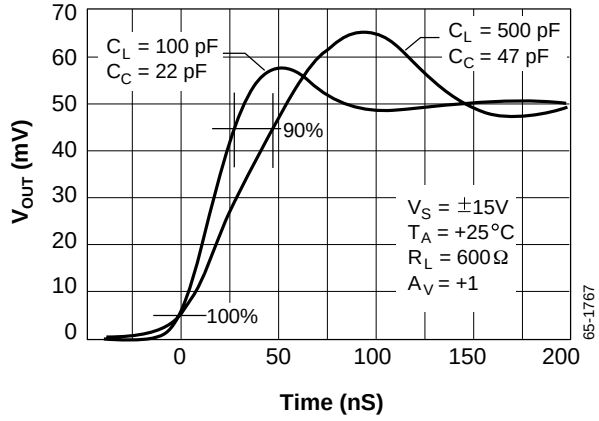


Figure 10. Transient Response Output Voltage vs. Time

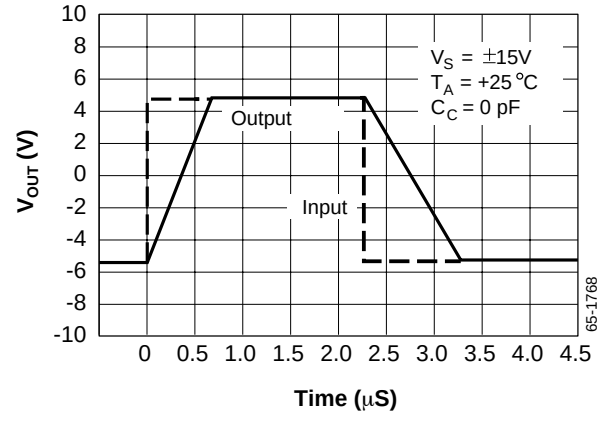


Figure 11. Follower Large Signal Pulse Response Output Voltage vs. Time

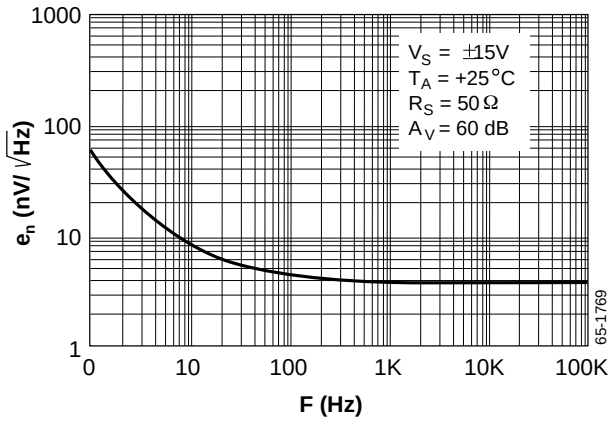


Figure 12. Input Noise Density vs. Frequency

Typical Performance Characteristics (continued)

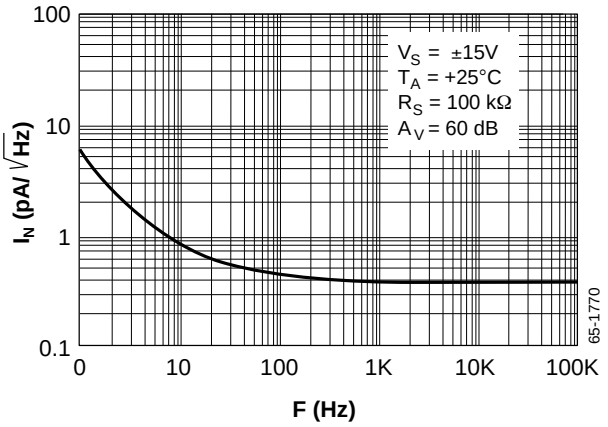


Figure 13. Input Noise Current Density vs. Frequency

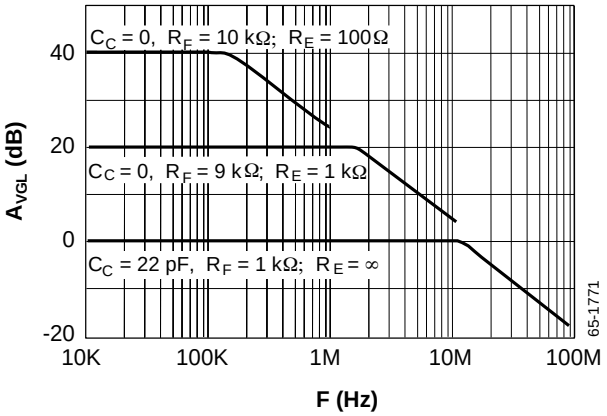


Figure 14. Closed Loop Gain vs. Frequency

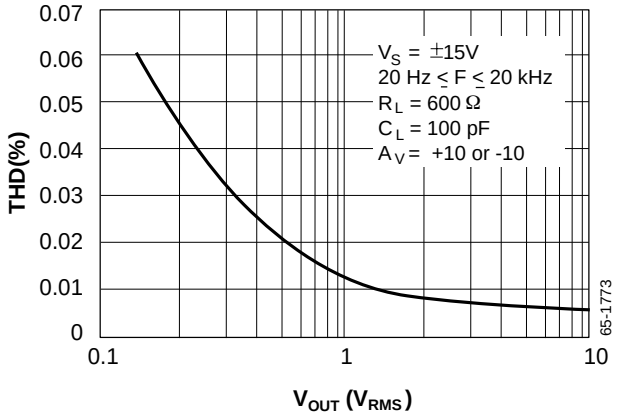


Figure 15. Total Harmonic Distortion vs. Output Voltage

Typical Test Circuits

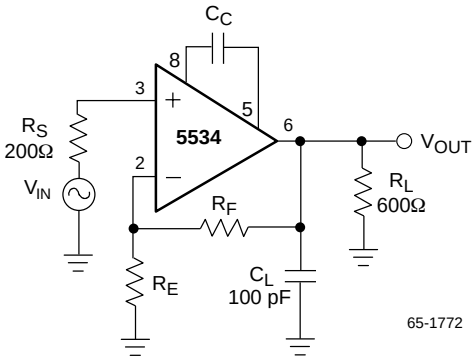


Figure 16. Closed Loop Frequency Response Test Circuit

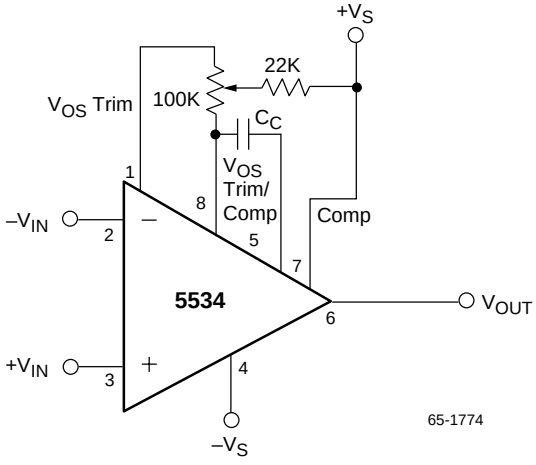
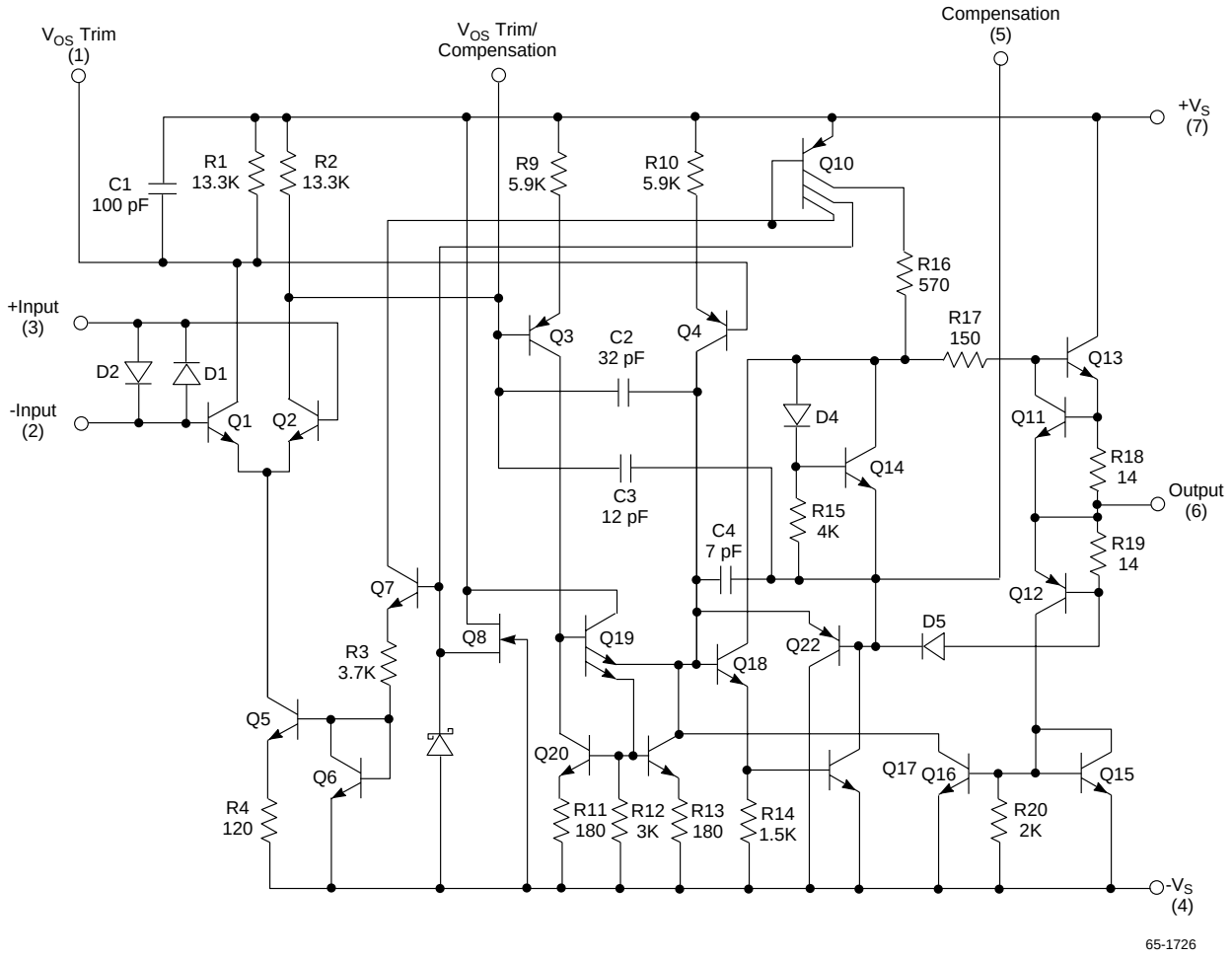


Figure 17. Offset Voltage Trim Circuit

Simplified Schematic Diagram



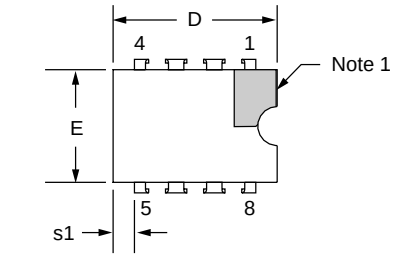
Mechanical Dimensions

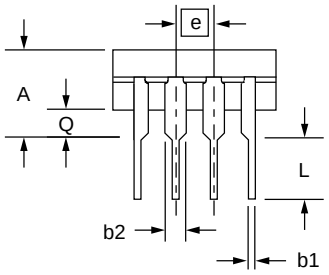
8-Lead Ceramic DIP Package

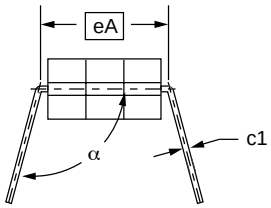
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2, 8
c1	.008	.015	.20	.38	8
D	—	.405	—	10.29	4
E	.220	.310	5.59	7.87	4
e	.100 BSC		2.54 BSC		5, 9
eA	.300 BSC		7.62 BSC		7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 4, 5 and 8 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 8.
6. Applies to all four corners (leads number 1, 4, 5, and 8).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Six spaces.







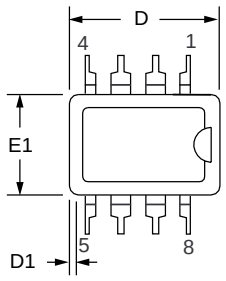
Mechanical Dimensions (continued)

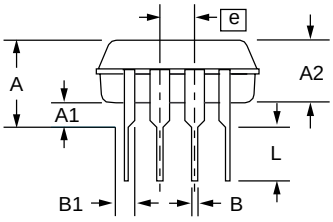
8-Lead Plastic DIP Package

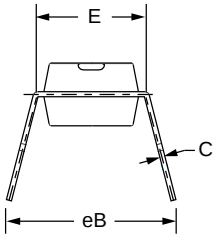
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	.348	.430	8.84	10.92	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.160	2.92	4.06	
N	8°		8°		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.

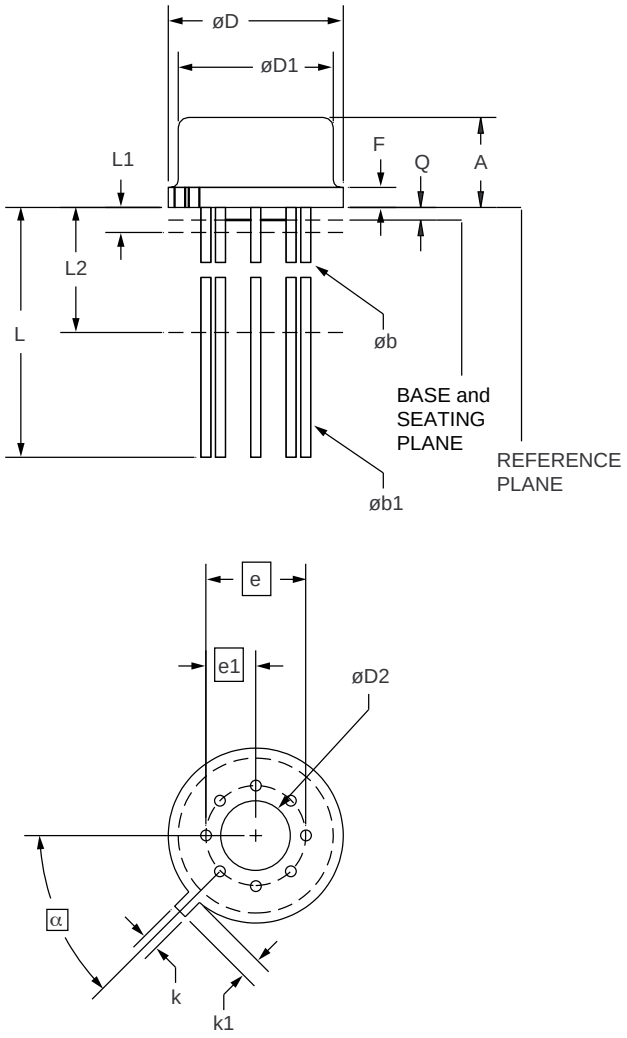






Mechanical Dimensions (continued)

8-Lead Metal Can IC Header Package



Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.185	4.19	4.70	
øb	.016	.019	.41	.48	1, 5
øb1	.016	.021	.41	.53	1, 5
øD	.335	.375	8.51	9.52	
øD1	.305	.335	7.75	8.51	
øD2	.110	.160	2.79	4.06	
e	.200 BSC		5.08 BSC		
e1	.100 BSC		2.54 BSC		
F	—	.040	—	1.02	
k	.027	.034	.69	.86	
k1	.027	.045	.69	1.14	2
L	.500	.750	12.70	19.05	1
L1	—	.050	—	1.27	1
L2	.250	—	6.35	—	1
Q	.010	.045	.25	1.14	
α	45° BSC		45° BSC		

Notes:

1. (All leads) øb applies between L1 & L2. øb1 applies between L2 & .500 (12.70mm) from the reference plane. Diameter is uncontrolled in L1 & beyond .500 (12.70mm) from the reference plane.
2. Measured from the maximum diameter of the product.
3. Leads having a maximum diameter .019 (.48mm) measured in gauging plane, .054 (1.37mm) +.001 (.03mm) –.000 (.00mm) below the reference plane of the product shall be within .007 (.18mm) of their true position relative to a maximum width tab.
4. The product may be measured by direct methods or by gauge.
5. All leads – increase maximum limit by .003 (.08mm) when lead finish is applied.

Ordering Information

Product Number	Temperature Range	Screening	Package
RC5534D/RC5534AD	0°C to +70°C	Commercial	8 Pin Ceramic DIP
RC5534N/RC5534AN	0°C to +70°C	Commercial	8 Pin Plastic DIP
RM5534D/RM5534AD	-55°C to +125°C	Commercial	8 Pin Ceramic DIP
RM5534D/883	-55°C to +125°C	Military	8 Pin Plastic DIP
RM5534AD/883	-55°C to +125°C	Military	8 Pin Plastic DIP
RM5534T/RM5534AT	-55°C to +125°C	Commercial	8 Pin TO-99 Metal Can
RM5534T/883	-55°C to +125°C	Military	8 Pin TO-99 Metal Can
RM5534AT/883	-55°C to +125°C	Military	8 Pin TO-99 Metal Can

Note: /883 denotes MIL-STD-883, Par. 1.2.1 compliant device.

5/20/98 0.0m 001
Stock#DS30005534

Embedded Secure Document

The file *http://www.fairchildsemi.com/ds/RC/RC5601.pdf* is a secure document that has been embedded in this document. Double click the pushpin to view RC5601.pdf.

RC5X01

CPU Core PWM Controller

Features

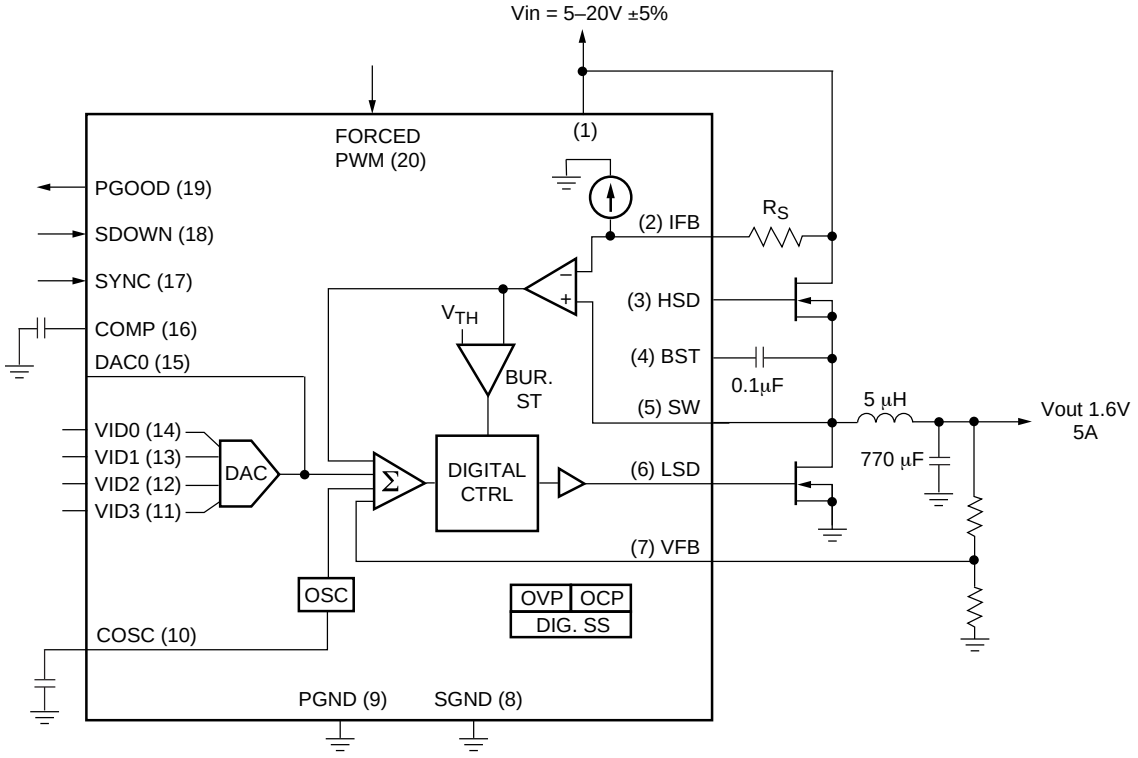
- Maximum efficiency at 5 V - 12V and 3A - 5A
- ±120mV Regulation
- T = 5µsec Ton = 350nsec with 7% minimum DC
- RDSON = 10 mΩ
- 20 Lead TSSPOP Package

Applications

- Notebook PCs
- MMOs

Target Specification

Block Diagram



10/29/97 Rev. 0.0.0

RC5X02

Multi PWM Regulator controller

Features

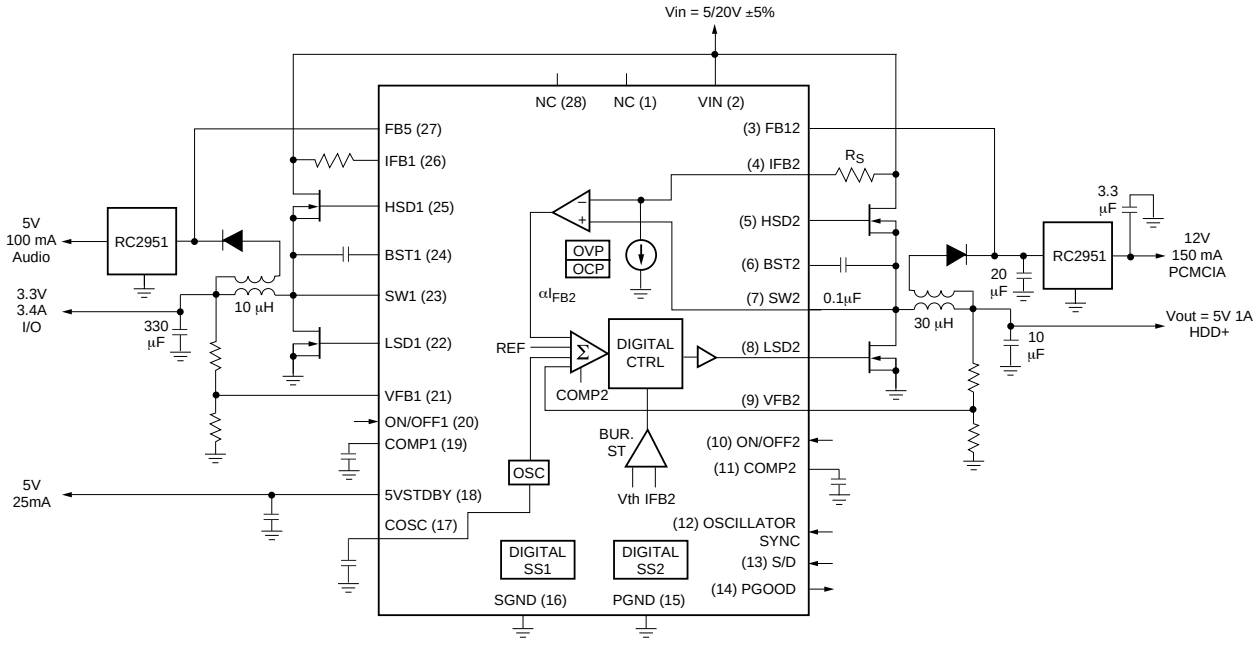
- Efficiency > 80% at 7.8V - 12V
- 28 Lead TSSOP Package

Applications

- Notebook PCs
- PDAs

Target Specification

Block Diagram



10/29/97 Rev. 0.0.0

RC6100

Horizontal Genlock

Features

- High speed tracking sync separator easily follows hum or average picture level (APL) fluctuations
- Glitch remover for operation in high impulse noise environment
- On chip phase-locked loop
- Locks and follows VCR sync
- Compatible with NTSC and PAL systems
- Choice of eight output frequencies
- Field ID output
- Internal VCO

Applications

- Digital video signal processing
- Digital television receivers and VCRs
- Video conferencing equipment
- Multimedia computers

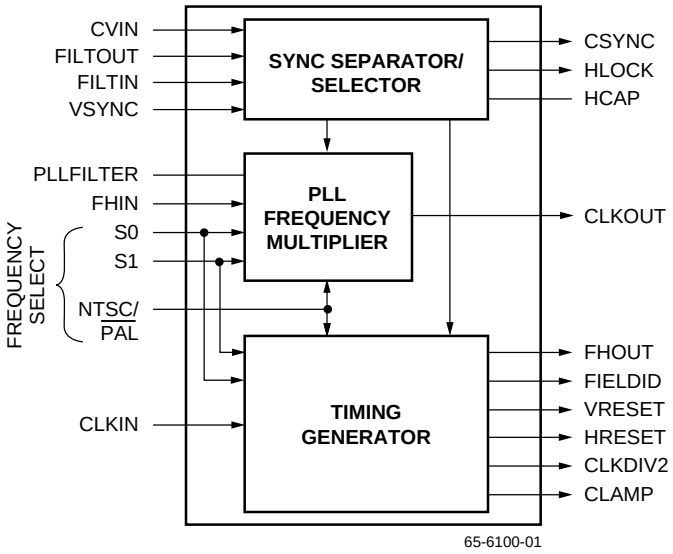
Description

The RC6100 contains a phase-locked loop (PLL) in a frequency multiplier configuration to generate a high-frequency clock as required for video A/D converter and digital video signal processing.

The device accepts composite video, composite sync or component sync signals as input. The output signals generated are: clamp gate, composite sync, horizontal sync, vertical sync, field ID, lock detector output, oscillator output (Clock), and Clock/2.

The NTSC output frequency choices are: 27.0, 25.175, 14.318, 13.5, 12.588, 12.273, 7.159, and 6.137 MHz. The PAL frequencies generated are: 27.0, 17.734, 15.0, 14.75, 13.5, 8.867, 7.5, and 7.375 MHz.

Logic Symbol



Block Diagram

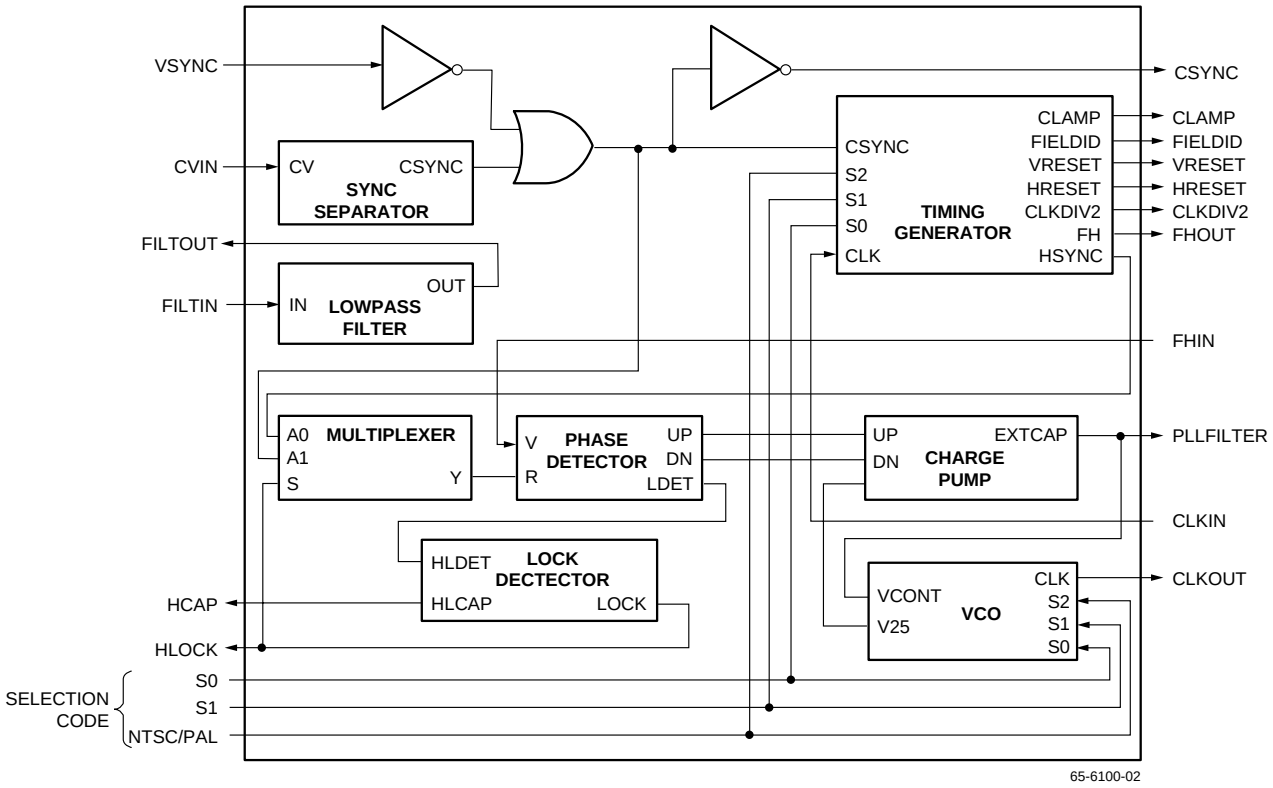


Figure 1.

Functional Description

The RC6100 block diagram is shown in Figure 1. Baseband composite video may be applied to either the FILTIN or CVIN input, depending upon whether the lowpass filter circuit function is desired. Use of the lowpass filter is desirable whenever the input video signal contains impulse noise or glitches that can cause jitter on the sync and clock output signals. Signals that require lowpass filtering should be input at FILTIN and the lowpass filter output (FILTOUT) should be connected to the CVIN input. However, video signals that do not require noise filtering should be input directly at CVIN to optimize performance. The FILTIN and CVIN inputs can also receive composite sync or horizontal sync signals at CMOS or TTL levels.

The input VSYNC is intended for those applications in which the horizontal and vertical sync signals have already been separated. In this mode, horizontal sync should be applied to CVIN and vertical sync applied to VSYNC. These two signals will be combined to form CSYNC and used by the timing generator to form HRESET, VRESET, and the other timing control signals. The VSYNC input is active low and is held at logic high via an internal bias network. If VSYNC is left open, there is no effect on signal processing.

The sync separator extracts a composite sync signal from the composite video, or creates composite sync from separate horizontal and vertical sync inputs. This signal is available at the CSYNC output. Composite sync is also used to control the timing generator, which is the workhorse function of the RC6100.

The timing generator contains programmable dividers for generating and controlling the pixel clock. The selection of pixel clock frequencies is controlled via logic inputs NTSC/PAL, S0, and S1. Table 1 shows the states of these inputs and the corresponding clock frequencies. The timing generator also provides the following output signals: CLAMP, VRESET, FIELDID, HRESET, FHOUT, and CLKDIV2. The CLAMP output is an active-low rectangular pulse of about 4 μs duration, the origination of which is timed by the rising-edge of CSYNC; the pulse is active during the horizontal back-porch interval, as shown in Figure 2. The CLAMP output is also active during the vertical blanking interval. The VRESET output is a short vertical sync signal that is logic low for the duration of the scan line that follows the first serration pulse of the vertical interval, as shown in Figure 3. HRESET is a horizontal sync signal that is set to logic low for one period of the pixel clock (CLKOUT); it is also phase coherent with the pixel clock. FHOUT is a clock signal at the horizontal frequency. It is normally connected to FHIN and used as the VCO (feedback) input to the loop phase comparator. The timing of HRESET relative to FHOUT is shown in Figure 4. (Note: the drawing exaggerates delays t1 and t2.) The FIELDID output goes to logic low immediately after the

VRESET pulse for RS170 Field 1 (the odd field) and toggles to logic high at the same time in the next field (see Figure 3). CLOCKDIV2 is the half-frequency pixel clock output; it is a 50-percent duty-cycle waveform. The Selection Codes of Table 1 (NTSC/PAL, S0, and S1) are input to the RC6100 to select the desired clock frequency to be output. The divisors shown in Table 1 indicate on-half the number of pixel clocks in each horizontal line. The pixel clock generator circuit (Figure 5) is formed by the Phase Detector, Charge Pump, external Loop Filter, and the VCO. The loop filter requires only a simple RC lag-lead network. When the PLL is locked, the VCO provides a pixel clock that is equal to $2*N*f_H$, (two times the horizontal scan frequency where N is the frequency divisor value). CLKOUT is normally connected to CLKIN, the clock input of the timing generator function. Note that a half-frequency pixel clock (CLKDIV2) is also generated. Both pixel clock outputs are 50-percent duty-cycle waveforms.

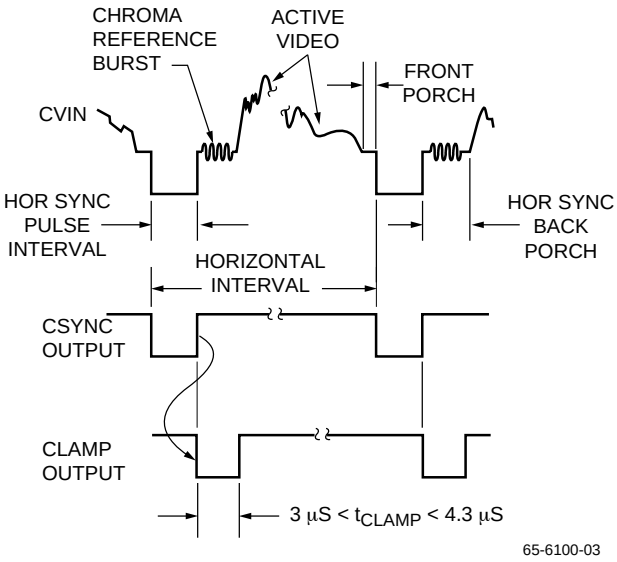
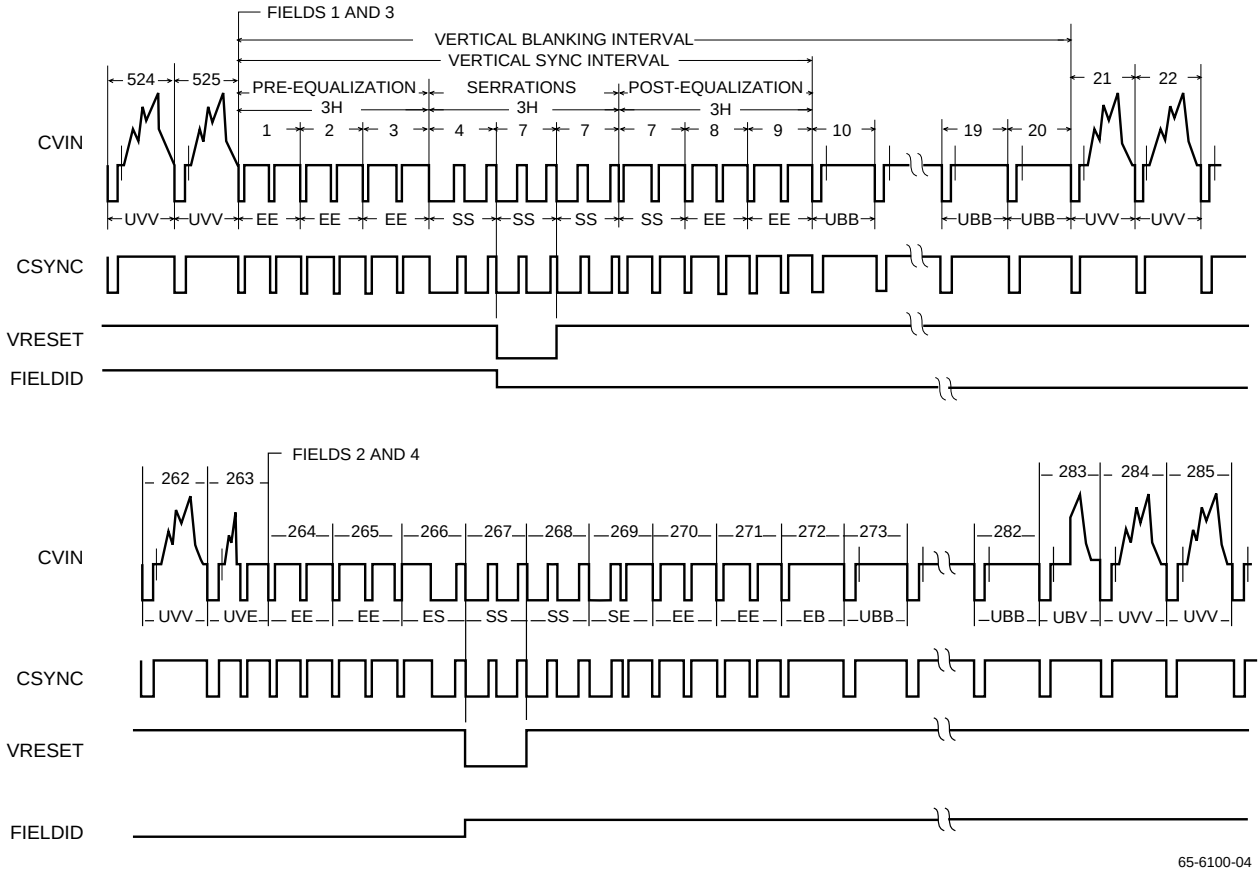


Figure 2. CLAMP Output Timing



Definitions:

UVV: active video
UVE: half-line video, half-line equalization pulse
EE: equalization pulse
EB: equalization broad pulse
SS: vertical sync pulse with serrations
ES: half-line equalization pulse, half-line vertical sync pulse
SE: half-line vertical sync pulse, half-line equalization pulse
UBV: half-line black, half-line video
UBB: black burst

Figure 3. VRESET Output TIming

Table 1. Clock Frequency Selection

Selection Codes			Frequencies (MHz) and Divisors (N)			
NTSC/ PAL	S1	S0	System	Clock Out	Clock/2 Out	Divide by N
1	0	0	NTSC (CCIR601)	27.0	13.5	858
1	0	1	NTSC (VGA)	25.175	12.588	800
1	1	0	NTSC (4fSC/Studio)	14.318	7.159	455
1	1	1	NTSC (Sq. Pixel)	12.273	6.137	390
0	0	0	PAL (CCIR601)	27.0	13.5	864
0	0	1	PAL (4fSC/Studio)	17.734	8.867	567.5
0	1	0	PAL	15.0	7.5	480
0	1	1	PAL (Sq. Pixel)	14.75	7.375	472

The timing performance of the phase lock is controlled by an external RC filter, the CSYNC signal, and internally-generated horizontal sync signals. When the PLL is not locked, CSYNC is selected as the reference input to the phase detector. CSYNC is derived directly from the composite video input, which contains the required horizontal edge information, and is not dependent upon the loop being locked. When the loop is locked, an internally generated horizontal sync signal from the timing generator is used for this reference input. CSYNC is only used as the loop reference input in the unlocked condition, because it contains serration pulses that would contribute undesirable jitter to the VCO output.

The lock-detect output signal (HLOCK) indicates when the phase reference and VCO inputs of the phase detector are locked. The response time of the lock detector is controlled by an external capacitor (C3) and, when lock is established, the HLOCK output goes low and the MUX makes the appropriate reference signal choice. The value of C3 was chosen to provide a lock-indication response time that is approximately 15 horizontal lines in duration, and an unlock-indication response time of approximately three horizontal lines in duration. Increasing the value of C3 would result in increasing both the lock and unlock response times.

The PLL consists of the phase detector, charge pump, loop filter, VCO, and divide-by-N counter. The phase detector is essentially a control loop summing junction. The charge pump, loop filter, and VCO are in the forward path, and the divide-by-N counter forms the feedback path. Stabilizing this control system consists of choosing the proper component values for the loop filter, such that sufficient phase margin exists at the unity-gain crossover frequency. The filter is a lag-lead network formed by the charge pump, C1, R1, and C2. Increasing the value of C1 moves the pole of the lag network (low pass) closer to the origin (lower frequency). This

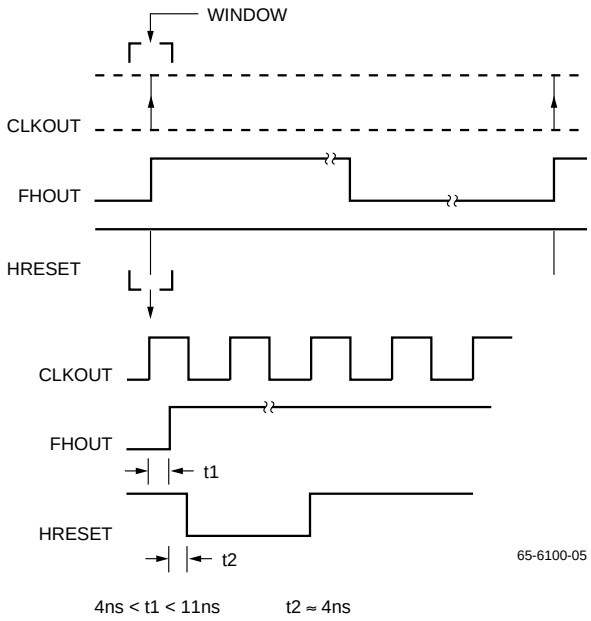


Figure 4. HRESET Output Timing

will reduce the loop bandwidth, which generally tends to reduce VCO jitter, but at a cost of settling (response) time and (in the extreme) stability. Table 2 shows values for R1, C1, and C2 for all input setings.

Increasing the value of either R1 or C2 moves the zero of the lead network (high pass) lower in frequency, which tends to increase loop gain at higher frequencies and can also result in poorer noise performance. The location of the zero is generally determined empirically to adjust the loop transfer function for adequate phase margin for a given desired bandwidth. The RC6100 loop settling time is approximately 400 μs, and lock detection requires about one millisecond.

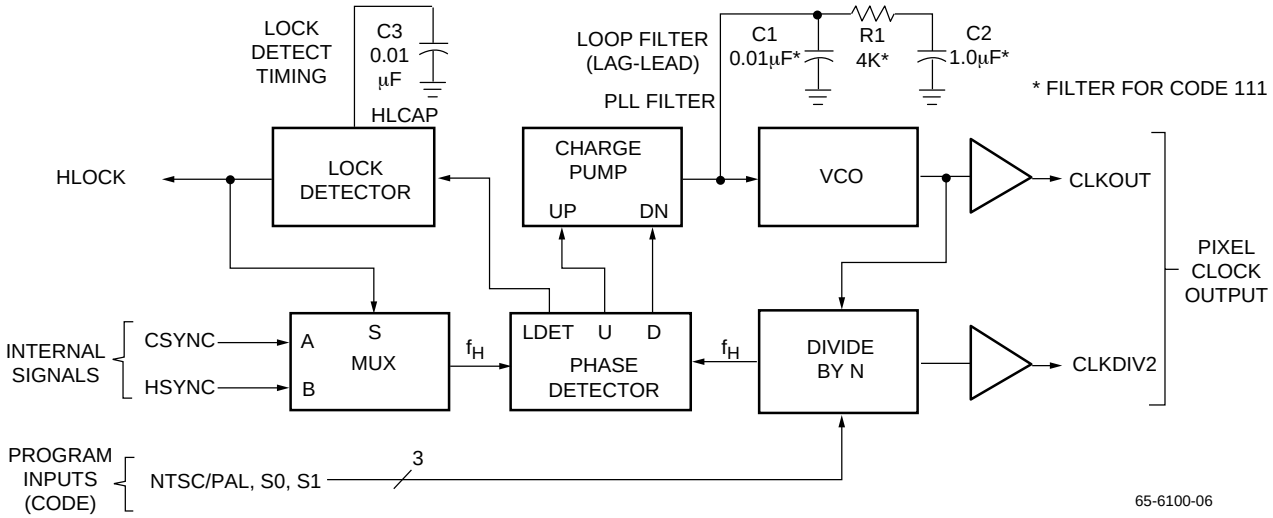


Figure 5. Pixel Clock Generator

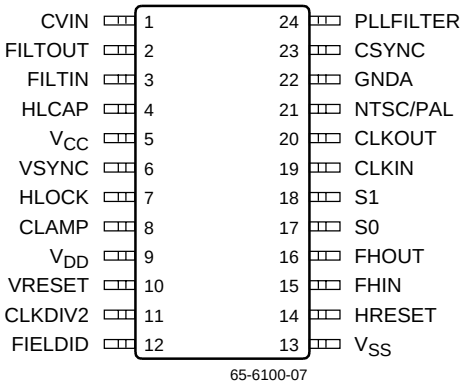
Table 2. PLL Filter Components

code	fin	fosc	Dividers		KVC0	KCP	R1	C2(K/20)	C1
			N	M					
100	15734	27.00E+06	1.00	858	2.66E+07	3.82E–05	4.17E+03	9.69E–07	9.69E–09
101	15734	25.18E+06	1.00	800	2.66E+07	3.82E–05	3.89E+03	1.04E–06	1.04E–08
110	15734	14.32E+06	2.00	455	2.51E+07	3.82E–05	4.68E+03	8.64E–07	8.64E–09
111	15734	12.27E+06	2.00	390	2.51E+07	3.82E–05	4.01E+03	1.01E–06	1.01E–08
000	15625	27.00E+06	1.00	864	2.66E+07	3.82E–05	4.17E+03	9.76E–07	9.76E–09
001	15625	17.73E+06	2.00	567.5	3.48E+07	3.82E–05	4.19E+03	9.72E–07	9.72E–09
010	15625	15.00E+06	2.00	480	2.48E+07	3.82E–05	4.97E+03	8.19E–07	8.19E–09
011	15625	14.75E	2.00	472	2.48E+07	3.82E–05	4.89E+03	8.33E–07	8.33E–09

Note:

1. Table values are ideal; actual values may vary by ±20% due to process variations.
2. Code: <NTSC/$\overline{\text{PAL}}$> <S1> <S0>

Pin Assignments



Pin Descriptions

Pin Name	Pin Number	Description
CVIN	1	This input accepts composite video.
FILTOUT	2	Output of low pass video input filter.
FILTIN	3	This input accepts either composite video, composite sync or horizontal sync signals. The input can be analog (1 Vpp) or TTL/CMOS logic levels.
HLCAP	4	Horizontal lock-detect timing capacitor.
V_{CC}	5	+5V power supply for analog circuits.
VSYNC	6	This input accepts vertical sync pulses for use when video input signals do not contain vertical sync components. This input is active low but remains high in normal operation. The input is TTL or CMOS compatible.
HLOCK	7	The locked-loop output indicates that the oscillator is phase-locked to the incoming horizontal sync. Sensitivity and delay time constant are set by an external capacitor. This output is CMOS or TTL compatible.
CLAMP	8	Clamp gate pulse output. This signal is approximately 4 μs in duration and is timed from the trailing edge of composite sync signal. The clamp gate is used by the video ADC and other video processing circuitry for DC restoration. This output is CMOS or TTL compatible.
V_{DD}	9	+5V power supply for digital circuits.
VRESET	10	Vertical sync signal output. This output is low during the line following the first serration pulse in the vertical sync interval. VRESET is CMOS or TTL compatible.
CLKDIV2	11	CLKOUT divided-by-two output frequency.
FIELDID	12	The field ID output signal is low following the VRESET pulse of RS170 field 1. This output is CMOS or TTL compatible.
V_{SS}	13	Digital ground.
HRESET	14	Horizontal reset signal is decoded from a programmable counter. This signal is coherent with the clock output and is one clock cycle in duration. This output is CMOS or TTL compatible.
FHIN	15	Horizontal frequency signal input; normally driven by FHOUT.
FHOUT	16	Horizontal frequency signal output.
S0, S1	17, 18	Frequency select inputs. They select one of four possible clock frequencies by providing the appropriate divide-by-N for the frequency-multiplying PLL. Table 1 shows the binary, frequency select codes. These inputs are TTL or CMOS compatible.
CLKIN	19	Clock input for internal timing functions; normally driven by CLKOUT.
CLKOUT	20	Buffered VCO output signal.
NTSC/PAL	21	This pin is used to select between NTSC or PAL frequencies of operation. A logic one selects the NTSC frequencies. See Table 1. These inputs are TTL or CMOS compatible.
GNDA	22	Analog ground.
CSYNC	23	Composite sync signal output. This signal is the sync separated from the video input, and is CMOS or TTL compatible.
PLLFILTER	24	PLL loop-compensation filter input.

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Min.	Typ.	Max.	Units
Power Supply Voltage (V_{CC})			7	V
Input Voltage	V_{CC} + 0.3V ≥ V_{IN} ≥ GND – 0.3V			
Operating Temperature	0		70	°C
Storage Temperature	-40		125	°C
Junction Temperature			150	°C
Lead Soldering Temperature (10 sec)			300	°C

Note:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter		Min.	Typ.	Max.	Units
θ_{JA}	SO-24 thermal resistance		75		°C/W
V_{CC}	Supply voltage	4.75	5.0	5.25	V
I_{CC}	Supply current		30	40	mA

DC Electrical Characteristics

V_{CC} = 5V, T_A = 0 to 70°C, unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Units
Logic Interface					
V_{IH}	Logic input high voltage	4			V
V_{IL}	Logic input low voltage			0.8	V
V_{OH}	Logic output high voltage	4			V
V_{OL}	Logic output low voltage			0.4	V
I_{IN}	Logic input current (V_{CC} ≥ VIN ≥ GND)			±30	μA
Analog Interface					
V_{IN}	Composite video signal (AC coupled)		1.0	2.0	V_{p-p}
I_{IN}	Input current (V_{IN} = V_{CC}–1V)			±700	μA
HLOCK	Lo @ 10mA		0.5	1.5	V
HLOCK	HI	3.5			V

AC Electrical Characteristics

V_{CC} = 5V, T_A = 0 to 70°C, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{CS}	Composite sync amplitude	Maintains lock with horizontal rate jitter T_{HJ} of <10 ns	150		600	mV_{p-p}
V_{IN}	Impulse noise immunity	CVIN = 1 V_{p-p} + glitch; Glitch < 50 ns, Neg polarity, Voltage relative to blanking; Test for proper CSYNC output	0.3			V
f_{CLOCK}	Clock range		12.273		27.0	MHz
$\Delta HFOUT/\Delta V_{CC}$	VCO power supply rejection rate HFOUT = 27 MHz	4.5V < V_{CCA} < 5.5V			3.5	%/V
HFPULL	PLL Lock/Hold in Range	CVIN horizontal frequency	±500			Hz
	code 100	= 15734 Hz nominal		750		Hz
$t_{PD\ (VCS)}$	Video in to CSYNC delay			750		ns
$t_{PD\ (VHS)}$	Video in to HRESET delay			750		ns
$t_{PD\ (HCG)}$	H sync to CLAMPgate delay			300		ns
t_{DHS}	Duration of HRESET reset	fclk = 27 MHz	69	74	89	ns
t_{DCG}	Duration of CLAMPgate		3.0		4.5	µs
fclk jitter	DC=2.5v@PLL filter	2.5@VCOin code 100			1	ns
	Closed loop	CVin=15.734KHz, Code 100, fclk=27MHz		6	12	ns
	Capture Range	fin=15.734+500Hz to 15.625-500Hz	200			Hz
PLLFilter	Sink/source current		±150	240	±350	µA
CLDIV	VOL @ 4mA				0.8	V
	VOH		3.5			V

Typical Application

Figure 6 shows the RC6100 Horizontal Line Genlock used in a video signal-processing system. The part provides the clock that is required to synchronize the various elements of the system. Note that the clamp gate output of the RC6100 is applied to the convert input of the TMC1175 ADC.

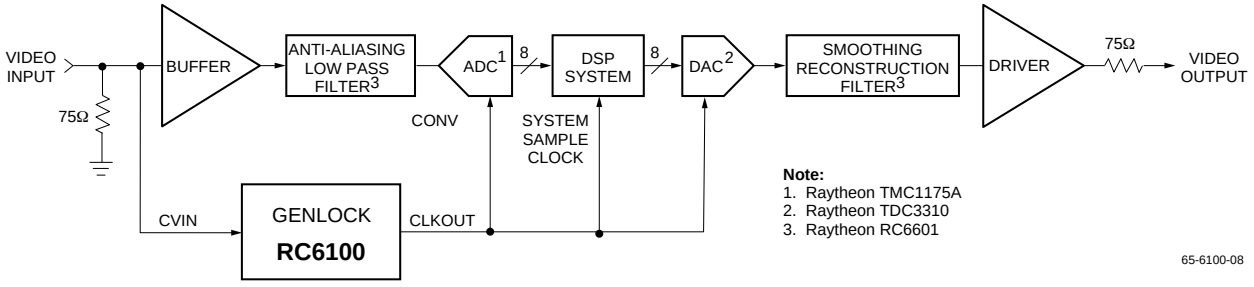
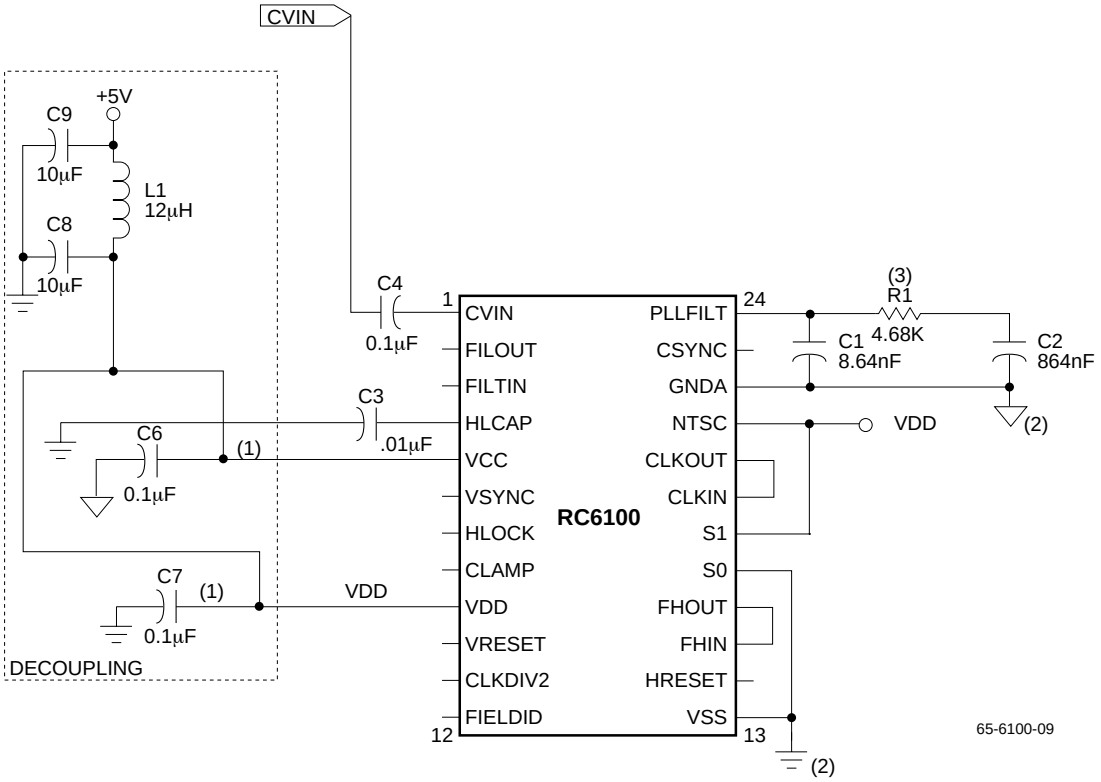


Figure 6. Application of RC6100 with TMC1175 and TDC3310 in Video Processing System

Application Circuit with Minimum Parts



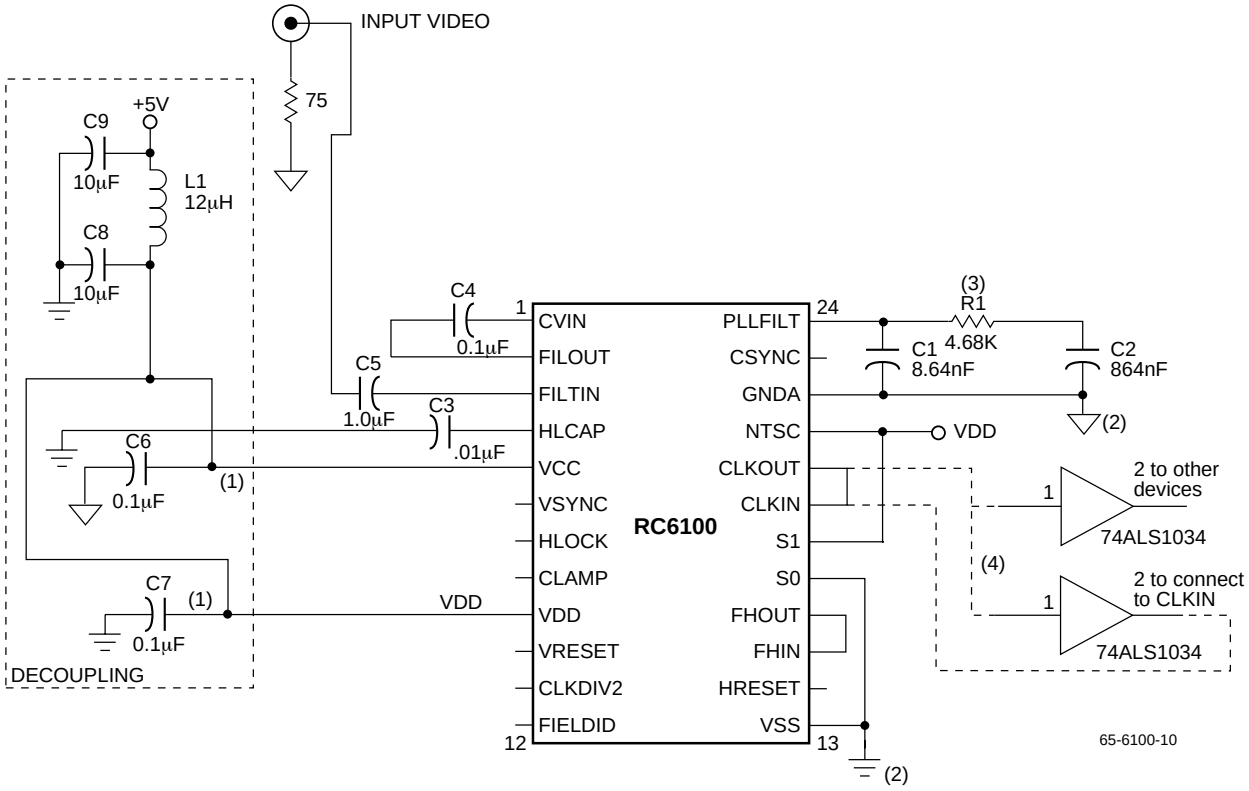
Notes:

1. Use a separate trace to each power pin and place capacitors C6 and C7 next to part.
2. Use separate ground plane for digital signals and PLL signals.

DIGITAL PLL

3. Place PLL filter components as close as possible to pin 24. Code 110.

Hook-up for Internal Filter



1. Use a separate trace to each power pin and place capacitors C6 and C7 next to part.
2. Use separate ground plane for digital signals and PLL signals.

DIGITAL PLL

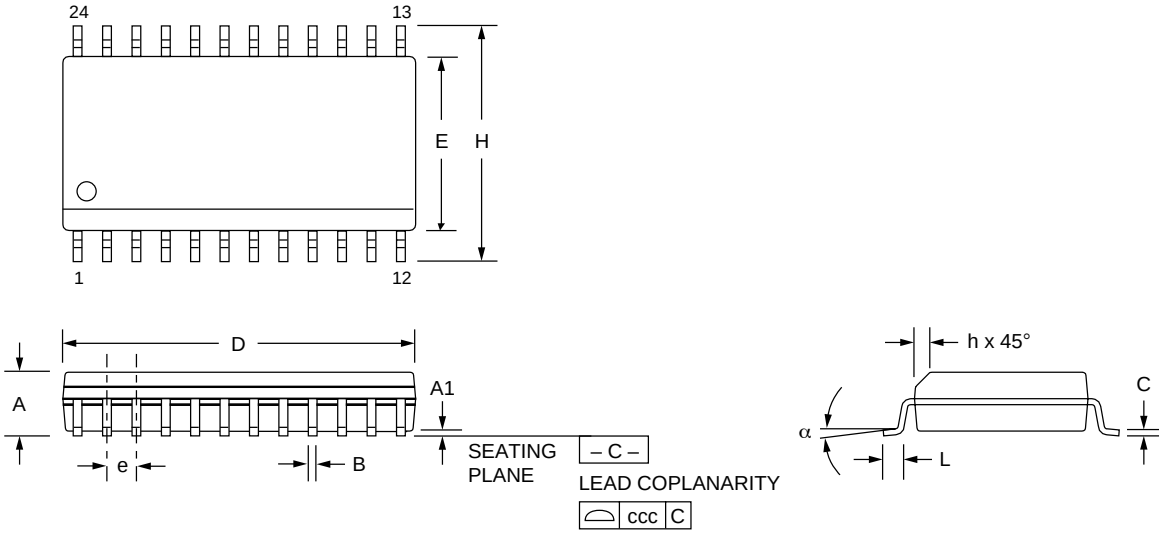
3. Place PLL filter components as close as possible to pin 24.
4. CLKOUT should be buffered for large trace runs or large fanout. Break CLKOUT, CLKIN, SHORT, and add buffers as shown.

Mechanical Dimensions – 24 Pin SOIC Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.599	.614	15.20	15.60	2
E	.290	.299	7.36	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.020	0.25	0.51	
L	.016	.050	0.40	1.27	3
N	24		24		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
RC6100M	0°C to +70°C	Commercial	24 Pin Wide SOIC	RC6100M

5/20/98 0.0m 001
Stock#DS30006100

Embedded Secure Document

The file *http://www.fairchildsemi.com/ds/RC/RC6120.pdf* is a secure document that has been embedded in this document. Double click the pushpin to view RC6120.pdf.

RC6302

Dual Video Amplifier

Features

- Unity gain stable
- 70 MHz -3 dB Bandwidth
- 20 MHz ±0.1 dB gain flatness
- 0.06% differential gain (R_L = 150Ω)
- 0.06° differential phase (R_L = 150Ω)
- High CMRR (100dB), High PSRR (80 dB)
- Dual ±5V power supply
- Low offset 1.0 mV
- 8-pin narrow SO package
- 160 V/μs slew rate
- Fast settling time: 0.1% in 35 ns

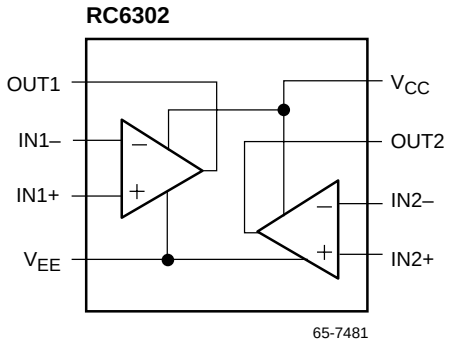
Applications

- Video amplifier
- Video instrumentation amplifier
- Active filter

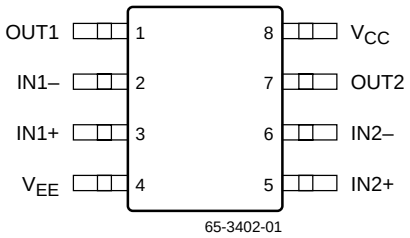
Description

The RC6302 consists of two low power, wide band voltage feedback operational amplifiers. Each channel is capable of delivering a load current of at least 35mA. The amplifiers are optimized for video applications where low differential gain and low phase distortion are significant requirements.

Block Diagram



Pin Assignments



Pin Definitions

Pin Name	Pin Number	Pin Function Description
IN1–	2	Amplifier 1 inverting input
IN1+	3	Amplifier 1 non-inverting input
IN2–	6	Amplifier 2 inverting input
IN2+	5	Amplifier 2 non-inverting input
OUT1	1	Amplifier 1 output
OUT2	7	Amplifier 2 output
V_{EE}	4	Negative supply voltage
V_{CC}	8	Positive supply voltage

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Min	Typ	Max	Units
Positive power supply, V_{CC}			7	V
Negative power supply, V_{EE}			-7	V
Differential input voltage			10	V
Operating Temperature	0		+70	°C
Storage Temperature	-40		+125	°C
Junction Temperature			150	°C
Lead Soldering Temperature (10 seconds)			300	°C
Operating Temperature	0		+70	°C
Short circuit tolerance: No more than one output can be shorted to ground.				

Note:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter		Min	Typ	Max	Units
V_{CC}	Power Supply Voltage	4.75	5.0	5.25	V
V_{EE}	Negative Supply Voltage	-4.75	-5.0	-5.25	V
θ_{JA}	SO8 Thermal Resistance		140		°C/W

DC Electrical Characteristics

V_{CC} = 5V, V_{EE} = -5V, A_V = 2, T_A = 0°C to 70°C, R_{LOAD} = 150Ω, unless otherwise specified.

Parameter		Conditions	Min	Typ	Max	Units
V_{OS}	Input Offset Voltage	No load		1.0	±5	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Drift[1]			6.0	±50	μV/°C
I_B	Input Bias Current			±1.0	±5	μA
$\Delta I_B/\Delta T$	Input Bias Current Drift[1]			±8.0	±50	nA/°C
R_{IN}	Input Resistance[1]		1			MΩ
C_{IN}	Input Capacitance[1]			0.5	2	pF
CMIR	Common Mode Input Range		±2.5			V
CMRR	Common Mode Rejection Ratio	No Load	70	100		dB
PSRR	Power Supply Rejection Ratio	No Load	60	80		dB
Is	Quiescent Supply Current	No Load, Whole IC		15	25	mA
R_{OUT}	Output Impedance[1]	At DC		0.2		Ω
I_{OUT}	Output Current			35		mA
V_{OUT}	Output Voltage Swing	No Load	±2.5	±3.0		V
		RL=150Ω	±2.5	±3.0		V
A_{VOL}	Open-loop Gain		58	68		dB

Note:

1. Guaranteed by design.

AC Electrical Characteristics

V_{CC} = 5V, V_{EE} = -5V, R_{LOAD} = 150Ω, R_G = R_F = 250Ω, A_V = 2, T_A = 0 to 70°C, C_L = 10 pF, C_F = 3 pF unless otherwise specified. Closed Loop. See Typical Test Circuit.

Parameter		Conditions	Min	Typ	Max	Units
Frequency Response						
BW	-3 dB Bandwidth (A_V = 2)[1]	V_{OUT} = 0.4 Vpp		70		MHz
		V_{OUT} = 0.8 Vpp		55		MHz
Flat	±0.1 dB Bandwidth[1]		15	20		MHz
Peak	Maximum Small Signal AC Peaking			0.3		DB
X_{TALK}	Crosstalk Isolation[1]	@ 5 MHz		60		dB
Time Domain Response						
t_{r1}, t_{f1}	Rise and Fall Time 10% to 90%[1]	2V Output Step		6	8	ns
t_S	Settling Time to 0.1 %[1]	2V Output Step		35		ns
OS	Overshoot[1]	2V Output Step		13		%
US	Undershoot[1]	2V Output Step		4		%
SR	Slew Rate[1]	V_{OUT} = ±2.0V		160		V/µs
Distortion						
HD_2	2nd Harmonic Dist. @ 20 MHz[1]	V_{OUT} = 0.8 Vpp		-50		dB
HD_3	3nd Harmonic Dist. @ 20 MHz[1]	V_{OUT} = 0.8 Vpp		-50		dB
Equivalent Input Noise						
NF	Noise Floor > 100 KHz[1]			-140		dBm
SND	Spectral Noise Density[1]	100 kHz to 200 MHz		10		nV/$\sqrt{Hz}$
Video Performance						
DG	Diff. Gain (p-p), NTSC & PAL[1]	R_L = 150Ω, V_{OUT} = ±1.5V		0.06		%
DP	Diff. Phase (p-p), NTSC & PAL[1]	R_L = 150Ω, V_{OUT} = ±1.5V		0.06		Deg.

Note:

1. Guaranteed by design.

Applications Discussion

Capacitive Load

The RC6302 can drive a capacitive load from 10 to over 100 pF. In back terminated video applications, bandwidth will only be limited by the RC time constants of the external output components. A minimum 10 pF capacitive load is required. When driving a 75Ω cable, place the 75Ω source termination resistor as close to the amplifier output as possible.

DC Accuracy

Since the RC6302 is a voltage-feedback amplifier, the inverting and non-inverting inputs have similar impedances and bias currents. To minimize offset voltage, match the source resistances seen by inverting and non-inverting inputs.

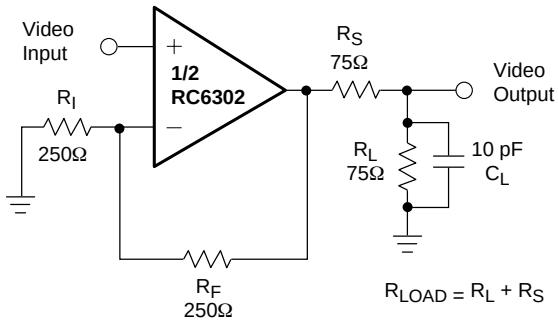
Feedback Components

Because the RC6302 is a voltage-feedback amplifier, it facilitates using reactive (capacitive and inductive) feedback components for implementing filters, integrators, sample/hold circuits, etc. The feedback network and the parasitic capacitance at the inverting (summing junction) input create a pole and affect the transfer function of the circuit. For stable operation, minimize the parasitic capacitance and equivalent resistance of the components used in the feedback circuit.

Circuit Board

High-frequency applications require good grounding, power supply decoupling, low parasitic capacitance and inductance, and good isolation between the three inputs to minimize their crosstalk. Minimal coupling from output to input should exist to prevent positive feedback.

Typical Test Circuit

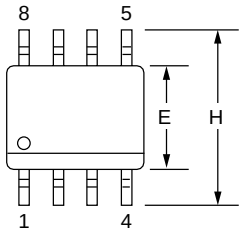


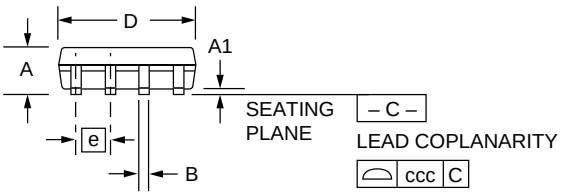
Mechanical Dimensions – 8-Lead SOIC Package

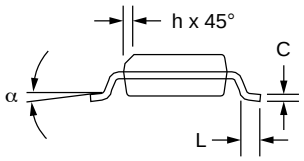
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.20	0.25	5
D	.189	.197	4.80	5.00	2
E	.150	.158	3.81	4.01	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	8		8		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
RC6302M8	0° to 70°C	Commercial	8 Pin Narrow SOIC	RC6302M8

RC6303

Triple Video Amplifier

with Separate Enable Inputs

Features

- Triple video amplifier
- Independently enabled amplifiers
- 90 MHz -3 dB Bandwidth (A_V = 2)
- 20 MHz ±0.1 dB gain flatness
- Stable at $A_V \geq 2$
- 0.06% differential gain (A_V = 2, R_L = 150Ω)
- 0.06° differential phase (A_V = 2, R_L = 150Ω)
- High CMRR (100dB), High PSRR (80 dB)
- Dual ±5V power supply
- Low offset 1.0 mV
- 16-pin narrow SO package
- 300 V/μs slew rate
- Fast settling time: 0.1% in 35 ns
- TTL or CMOS compatible enable inputs

Applications

- RGB amplifier
- 3:1 crosspoint switch
- RGB switch
- Video instrumentation amplifier
- Selectable gain amplifier
- Active filter

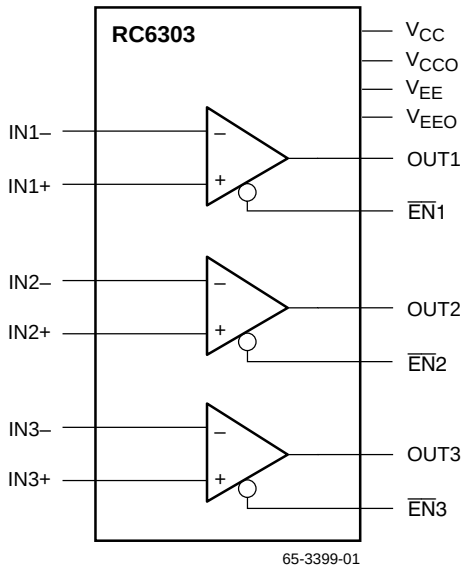
Description

The RC6303 consists of three low power, wide band voltage feedback operational amplifiers. Each channel is capable of delivering a load current of at least 35mA. Each amplifier can be independently enabled or disabled with a TTL or CMOS signal. When disabled, the amplifier is in a high impedance output state, presenting a very high input to output isolation.

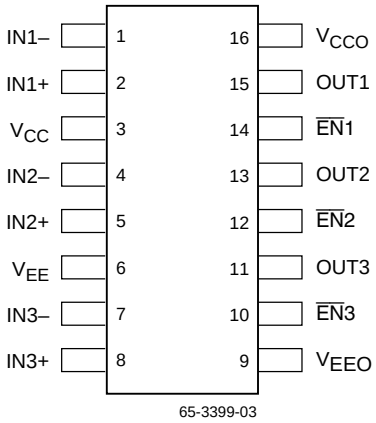
The amplifiers are optimized for video applications with gain ≥ 2 where low differential gain and low phase distortion are significant requirements.

The layout is optimized for minimal crosstalk between amplifiers.

Block Diagram



Pin Assignments



65-3399-03

Pin Definitions

Pin Name	Pin Number	Pin Function Description
$\overline{EN1}$	14	Enables amplifier 1 when low
$\overline{EN2}$	12	Enables amplifier 2 when low
$\overline{EN3}$	10	Enables amplifier 3 when low
IN1–	1	Amplifier 1 inverting input
IN1+	2	Amplifier 1 non-inverting input
IN2–	4	Amplifier 2 inverting input
IN2+	5	Amplifier 2 non-inverting input
IN3–	7	Amplifier 3 inverting input
IN3+	8	Amplifier 3 non-inverting input
OUT1	15	Amplifier 1 output
OUT2	13	Amplifier 2 output
OUT3	11	Amplifier 3 output
V_{CC}	3	Analog positive supply
V_{CCO}	16	Positive supply for output stages
V_{EE}	6	Analog negative supply
V_{EEO}	9	Negative supply for output stages

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Min	Typ	Max	Units
Positive power supply, V_{CC}			7	V
Negative power supply, V_{EE}			-7	V
Differential input voltage			10	V
Operating Temperature	0		+70	°C
Storage Temperature	-40		+125	°C
Junction Temperature			150	°C
Lead Soldering Temperature (10 seconds)			300	°C
Short circuit tolerance: No more than one output can be shorted to ground.				

Note:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter		Min	Typ	Max	Units
V_{CC}	Power Supply Voltage	4.75	5.0	5.25	V
V_{EE}	Negative Supply Voltage	-4.75	-5.0	-5.25	V
θ_{JA}	SO16 thermal resistance		105		°C/W

DC Characteristics

V_{CC} = 5V, V_{EE} = -5V, A_V = 2, R_{LOAD} = 150Ω, T_A = 0°C to 70°C, unless otherwise specified. Open Loop.

Parameter		Conditions	Min	Typ	Max	Units
V_{OS}	Input Offset Voltage	No Load		1.0	±5	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Drift[1]			6.0	±50	µV/°C
I_B	Input Bias Current			±1.0	±5	µA
$\Delta I_B/\Delta T$	Input Bias Current Drift[1]			±8.0	±50	nA/°C
Rin	Input Resistance[1]		1			MΩ
Cin	Input Capacitance[1]			0.5	2	pF
CMIR	Common Mode Input Range		±2.5			V
CMRR	Common Mode Rejection Ratio	No Load	70	100		dB
PSRR	Power Supply Rejection Ratio	No Load	60	80		dB
Is	Quiescent Supply Current	No Load, Whole IC		25	33	mA
Isd	Supply Current Disabled			3	4	mA
R_{OUT}	Output Impedance (Closed Loop) [1]	Enabled, At DC		0.2		Ω
		Disabled, V_O = ±2V	10	200		kΩ
C_{OUT}	Output Capacitance[1]	Disabled		0.5	2	pF
I_{OUT}	Output Current		35			mA
V_{OUT}	Output Voltage Swing	No Load	±2.5	±3.0		V
		R_L = 150Ω	±2.5	±3.0		V
A_{VOL}	Open-loop Gain		58	68		dB
Venh	Enable High Voltage		2.4			V
Venl	Enable Low Voltage				0.8	V
Ien	Enable Input Current			3	10	µA
t_{off}	Disable Time [1]			200		ns
t_{on}	Enable Time [1]	Settling to 1%		160		ns
Iso	Off Isolation (Input to Output)[1]	@ 5 MHz		60		dB

Note:

1. Guaranteed by design.

AC Characteristics

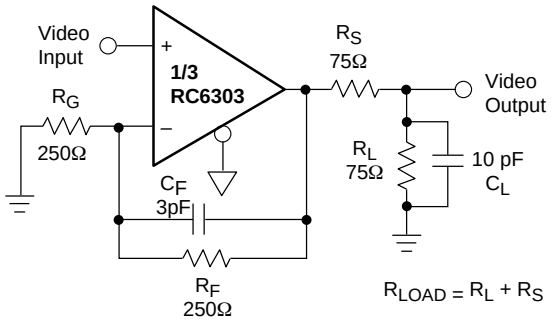
V_{CC} = 5V, V_{EE} = -5V, A_V = 2, T_A = 0 to 70°C, R_{LOAD} = 150Ω, R_G = R_F = 250Ω, C_L = 10 pF, C_F = 3 pF unless otherwise specified. Closed Loop. See Typical Test Circuit.

Parameter		Conditions	Min	Typ	Max	Units
Frequency Response						
BW	-3 dB Bandwidth (A_V = 2)[1]	V_{OUT} = 0.4 Vpp		90		MHz
		V_{OUT} = 0.8 Vpp	70	85		MHz
Flat	±0.1 dB Bandwidth[1]		15	20		MHz
Peak	Maximum Small Signal AC Peaking[1]			0.3		dB
X_{TALK}	Crosstalk Isolation[1]	@ 5 MHz		60		dB
Time Domain Response						
t_{r1}, t_{f1}	Rise and Fall Time 10% to 90%[1]	2V Output Step		6	8	ns
ts	Settling Time to 0.1 %[1]	2V Output Step		35		ns
OS	Overshoot[1]	2V Output Step		13		%
US	Undershoot[1]	2V Output Step		4		%
SR	Slew Rate[1]	V_{OUT} = ±2.0V	200	300		V/µs
Distortion						
HD_2	2nd Harmonic Dist. @ 20 MHz[1]	V_{OUT} = 0.8 Vpp		-50		dB
HD_3	3nd Harmonic Dist. @ 20 MHz[1]	V_{OUT} = 0.8 Vpp		-50		dB
Equivalent Input Noise						
NF	Noise Floor > 100 KHz[1]			-140		dBm
SND	Spectral Noise Density[1]	100 kHz to 200 MHz		10		nV/√Hz
Video Performance						
DG	Diff. Gain (p-p), NTSC & PAL[1]	R_L = 150Ω, V_{OUT} = ±1.5V		0.06		%
DP	Diff. Phase (p-p), NTSC & PAL[1]	R_L = 150Ω, V_{OUT} = ±1.5V		0.06		Deg.

Note:

1. Guaranteed by design.

Test Circuit



Applications Discussion

Each of the three sections of the RC6303 is provided with an Enable input, thus the part is useful for selecting and multiplexing. A three-channel video multiplexer can be built with just one RC6303 and a decoder, as shown in Figure 1.

Note that RC6303 enable time is shorter than its disable time, hence a make-before-break action is provided, minimizing switching transients on the signal output.

An RGB switch is shown in Figure 2.

Capacitive Load

The RC6303 can drive a capacitive load from 10 to over 100 pF. In back terminated video applications, bandwidth will only be limited by the RC time constants of the external output components. A minimum 10 pF capacitive load is required. When driving a 75Ω cable, place the 75Ω source termination resistor as close to the amplifier output as possible.

Enable/Disable

The enable pins (10, 12, 14), when pulled to a TTL or CMOS logic low or when tied to ground, activate each amplifier individually. When pulled to a TTL or CMOS logic high, the amplifier is tri-stated and presents a high impedance at its output. When disabled the amplifier's power consumption drops, and the non-inverting input signal is isolated from its respective output.

DC Accuracy

Since the RC6303 is a voltage-feedback amplifier, the inverting and non-inverting inputs have similar impedances and bias currents. To minimize offset voltage, match the source resistances seen by inverting and non-inverting inputs.

Feedback Components

Because the RC6303 is a voltage-feedback amplifier, it facilitates using reactive (capacitive and inductive) feedback components for implementing filters, integrators, sample/hold circuits, etc. The feedback network and the parasitic capacitance at the inverting (summing junction) input create a pole and affect the transfer function of the circuit. For stable operation, minimize the parasitic capacitance and equivalent resistance of the components used in the feedback circuit.

Circuit Board

High-frequency applications require good grounding, power supply decoupling, low parasitic capacitance and inductance, and good isolation between the inputs to minimize their crosstalk. Avoid coupling from output to input to prevent positive feedback.

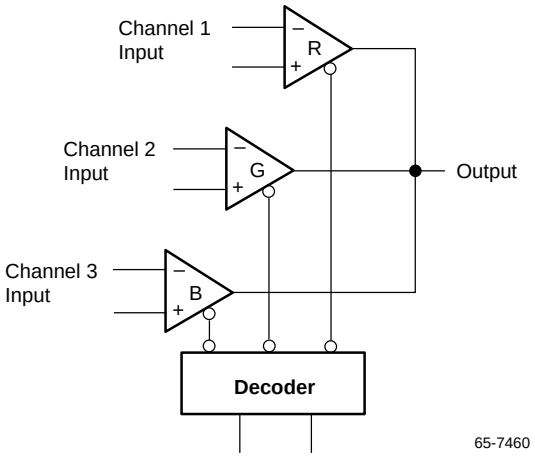


Figure 1.

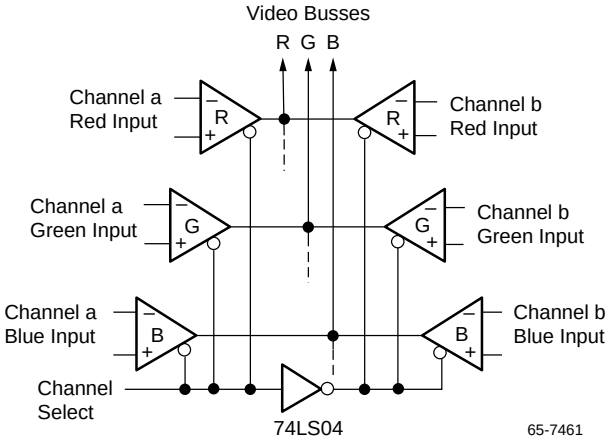


Figure 2.

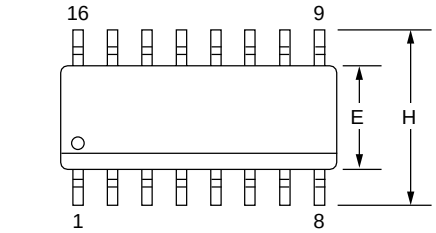
Notes:

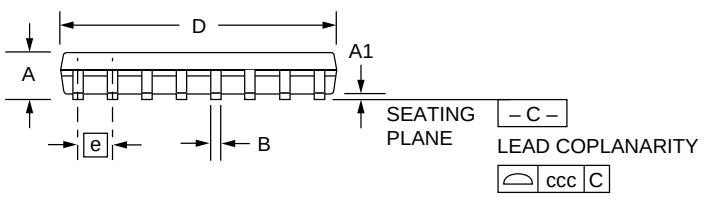
Mechanical DImensions – 16-Lead SOIC Package

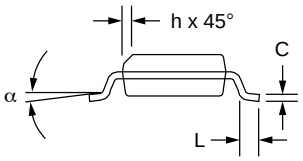
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.19	0.25	5
D	.386	.394	9.80	10.00	2
E	.150	.158	3.81	4.00	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.80	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	16		16		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
RC6303M	0° to 70°C	Commercial	16 Pin Narrow SOIC	RC6303M

5/20/98 0.0m 001
Stock#DS30006303

RC6333

Triple Video Amplifier

Features

- Triple video amplifier
- 175 MHz -3 dB Bandwidth (A_V = 2)
- 50 MHz ±0.1 dB gain flatness
- Unity gain stable
- 0.06% differential gain (A_V = 1, R_L = 150Ω)
- 0.06° differential phase (A_V = 1, R_L = 150Ω)
- High CMRR (95dB), High PSRR (80 dB)
- Dual ±5V power supply
- Low offset 3.0 mV typical
- 14-pin narrow SO package
- 250V/µs slew rate
- Fast settling time: 0.1% in 15 ns
- TTL or CMOS compatible

Applications

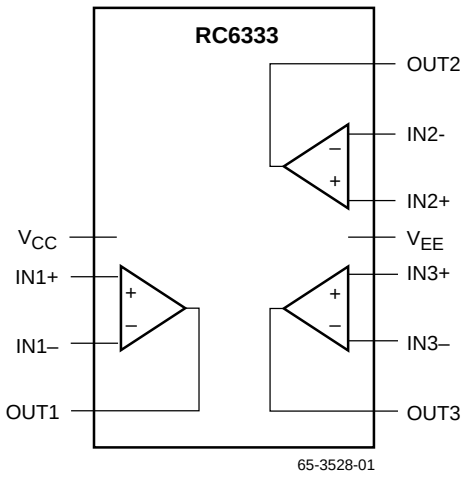
- RGB amplifiers
- Video instrumentation amplifier
- Selectable gain amplifier
- Active filters
- Set-top Buffers/Drivers

Description

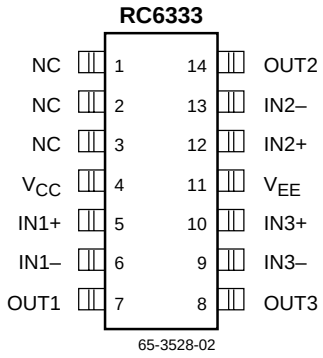
The RC6333 consists of three low power, wide band voltage feedback operational amplifiers. Each channel is capable of delivering a load current of at least 35mA.

The amplifiers are optimized for video applications where low differential gain and low phase distortion are significant requirements.

Block Diagram



Pin Assignments



Pin Definitions

Pin Name	Pin Number	Pin Function Description
IN1–	6	Amplifier 1 inverting input
IN1+	5	Amplifier 1 non-inverting input
IN2–	13	Amplifier 2 inverting input
IN2+	12	Amplifier 2 non-inverting input
IN3–	9	Amplifier 3 inverting input
IN3+	10	Amplifier 3 non-inverting input
NC	1–3	Not Connected.
OUT1	7	Amplifier 1 output
OUT2	14	Amplifier 2 output
OUT3	8	Amplifier 3 output
V_{CC}	4	Analog positive supply
V_{EE}	11	Analog negative supply

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min	Typ	Max	Units
V_{CC}	Positive power supply			7	V
V_{EE}	Negative power supply			-7	V
	Differential input voltage			10	V
	Operating Temperature	0		+70	°C
	Storage Temperature	-40		±125	°C
	Junction Temperature			150	°C
	Lead Soldering (10 seconds)			240	°C
Short circuit tolerance: No more than one output can be shorted to ground.					

Notes:

1. Functional operation under any of these conditions is NOT implied.

Operating Conditions

Parameter		Min	Typ	Max	Units
V_{CC}	Power Supply Voltage	4.75	5.0	5.25	V
V_{EE}	Negative Supply Voltage	-4.75	-5.0	-5.25	V
θ_{JA}	SO14 Thermal Resistance		105		°C/W

DC Characteristics

V_{CC} = 5V, V_{EE} = -5V, A_V = 2, R_{LOAD} = 150Ω, T_A = 0°C to 70°C, unless otherwise specified. Open Loop.

Parameter		Conditions	Min	Typ	Max	Units
V_{OS}	Input Offset Voltage	No Load		3	±10	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Drift[1]			±6	±30	µV/°C
I_B	Input Bias Current			±1	±5	µA
$\Delta I_B/\Delta T$	Input Bias Current Drift[1]			±8	±40	nA/°C
Rin	Input Resistance[1]		1			MΩ
Cin	Input Capacitance[1]			0.5	2	pF
CMIR	Common Mode Input Range		±2.5			V
CMRR	Common Mode Rejection Ratio	No Load	70	100		dB
PSRR	Power Supply Rejection Ratio	No Load	65	80		dB
Is	Quiescent Supply Current	No Load		26	40	mA
R_{OUT}	Output Impedance (Closed Loop)[1]	Enabled, At DC		0.2		Ω
I_{OUT}	Output Current	Per Amplifier	35			mA
V_{OUT}	Output Voltage Swing	No Load	±2.5	±3.0		V
		R_L = 150Ω	±2.5	±3.0		V
A_{VOL}	Open-loop Gain		60	75		dB

Note:

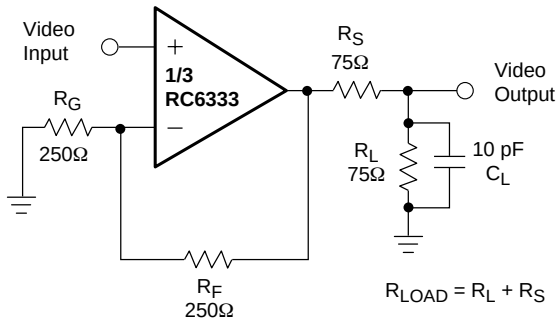
1. Guaranteed by design.

AC Characteristics

V_{CC} = 5V, V_{EE} = -5V, A_V = 2, T_A = 0 to 70°C, R_{LOAD} = 150Ω, R_G = R_F = 250Ω, C_L = 10 pF, unless otherwise specified. Closed Loop. Guaranteed by Design. See Typical Test Circuit.

Parameter		Conditions	Min	Typ	Max	Units
Frequency Response						
BW	-3 dB Bandwidth (A_V = 2)	V_{OUT} = 0.4 Vpp		+175		MHz
		V_{OUT} = 0.8 Vpp	75	90		MHz
Flat	±0.1 dB Bandwidth	V_{OUT} = 0.4 Vpp	50	75		MHz
Peak	Maximum Small Signal AC Peaking	V_{OUT} = 0.8 Vpp		0.01		dB
X_{TALK}	Crosstalk Isolation	@ 5 MHz		50		dB
Time Domain Response						
t_{r1}, t_{f1}	Rise and Fall Time 10% to 90%	2V Output Step		10	15	ns
ts	Settling Time to 0.1%	2V Output Step		15		ns
OS	Overshoot	2V Output Step		5		%
US	Undershoot	2V Output Step		2		%
SR	Slew Rate	V_{OUT} = ±2.0V	200	250		V/µs
Distortion						
HD_2	2nd Harmonic Dist. @ 20 MHz	V_{OUT} = 0.8 Vpp		-48		dB
HD_3	3nd Harmonic Dist. @ 20 MHz	V_{OUT} = 0.8 Vpp		-56		dB
Video Performance						
DG	Diff. Gain (p-p), NTSC & PAL	R_L = 150Ω, V_{OUT} = ±1.5V		0.06		%
DP	Diff. Phase (p-p), NTSC & PAL	R_L = 150Ω, V_{OUT} = ±1.5V		0.06		Deg.
NF	Noise Floor	>100kHz		-130		dB rms

Test Circuit



Applications Discussion

Capacitive Load

The RC6333 can drive a capacitive load from 10 to over 50 pF. In back terminated video applications, bandwidth will only be limited by the RC time constants of the external output components. When driving a 75Ω cable, place the 75Ω source termination resistor as close to the amplifier output as possible.

DC Accuracy

Since the RC6333 is a voltage-feedback amplifier, the inverting and non-inverting inputs have similar impedances and bias currents. To minimize offset voltage, match the source resistances seen by inverting and non-inverting inputs.

Feedback Components

Because the RC6333 is a voltage-feedback amplifier, it facilitates using reactive (capacitive and inductive) feedback components for implementing filters, integrators, sample/hold circuits, etc. The feedback network and the parasitic capacitance at the inverting (summing junction) input create a pole and affect the transfer function of the circuit. For stable operation, minimize the parasitic capacitance and equivalent resistance of the components used in the feedback circuit.

Circuit Board

High-frequency applications require good grounding, power supply decoupling, low parasitic capacitance and inductance, and good isolation between the inputs to minimize their crosstalk. Avoid coupling from output to input to prevent positive feedback.

Notes:

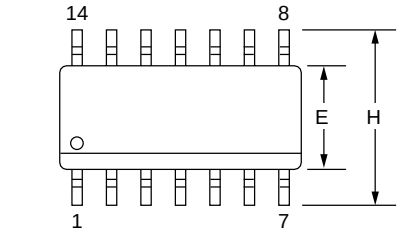
Notes:

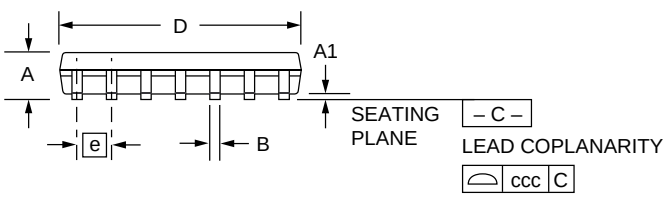
Mechanical Dimensions – 14 Pin SOIC Package

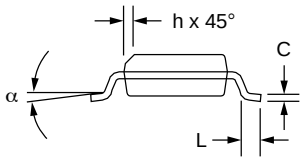
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.19	0.25	5
D	.336	.345	8.54	8.76	2
E	.150	.158	3.81	4.01	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	14		14		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
RC6333M	0° to 70°C	Commercial	14 Pin Narrow SOIC	RC6333M

RC6334

Quad Video Amplifier

Features

- Quad video amplifier
- 175 MHz -3 dB Bandwidth (A_V = 2)
- 50 MHz ±0.1 dB gain flatness
- Unity gain stable
- 0.06% differential gain (A_V = 1, R_L = 150Ω)
- 0.06° differential phase (A_V = 1, R_L = 150Ω)
- High CMRR (95dB), High PSRR (80 dB)
- Dual ±5V power supply
- Low offset 3.0 mV typical
- 14-pin narrow SO package
- 250V/µs slew rate
- Fast settling time: 0.1% in 15 ns
- TTL or CMOS compatible

Applications

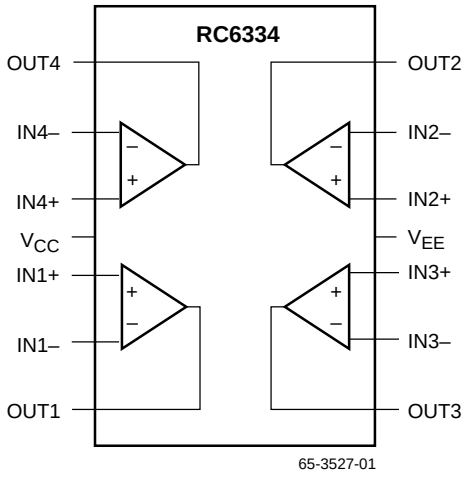
- RGB amplifiers
- Video instrumentation amplifier
- Selectable gain amplifier
- Active filters
- Set-top box Buffers/Drivers

Description

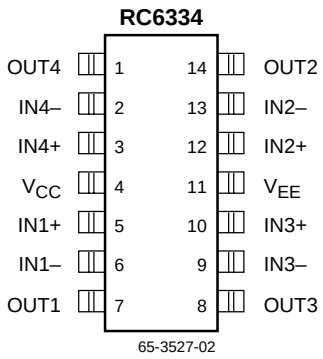
The RC6334 consists of four low power, wide band voltage feedback operational amplifiers. Each channel is capable of delivering a load current of at least 35mA.

The amplifiers are optimized for video applications where low differential gain and low phase distortion are significant requirements.

Block Diagram



Pin Assignments



Pin Definitions

Pin Name	Pin Number	Pin Function Description
IN1–	6	Amplifier 1 inverting input
IN1+	5	Amplifier 1 non-inverting input
IN2–	13	Amplifier 2 inverting input
IN2+	12	Amplifier 2 non-inverting input
IN3–	9	Amplifier 3 inverting input
IN3+	10	Amplifier 3 non-inverting input
IN4–	2	Amplifier 4 inverting input
IN4+	3	Amplifier 4 non-inverting input
OUT1	7	Amplifier 1 output
OUT2	14	Amplifier 2 output
OUT3	8	Amplifier 3 output
OUT4	1	Amplifier 4 output
V_{CC}	4	Analog positive supply
V_{EE}	11	Analog negative supply

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min	Typ	Max	Units
V_{CC}	Positive power supply			7	V
V_{EE}	Negative power supply			-7	V
	Differential input voltage			10	V
	Operating Temperature	0		+70	°C
	Storage Temperature	-40		±125	°C
	Junction Temperature			150	°C
	Lead Soldering (10 seconds)			240	°C
Short circuit tolerance: No more than one output can be shorted to ground.					

Notes:

1. Functional operation under any of these conditions is NOT implied.

Operating Conditions

Parameter		Min	Typ	Max	Units
V_{CC}	Power Supply Voltage	4.75	5.0	5.25	V
V_{EE}	Negative Supply Voltage	-4.75	-5.0	-5.25	V
θ_{JA}	SO14 Thermal Resistance		105		°C/W

DC Characteristics

V_{CC} = 5V, V_{EE} = -5V, A_V = 2, R_{LOAD} = 150Ω, T_A = 0°C to 70°C, unless otherwise specified. Open Loop.

Parameter		Conditions	Min	Typ	Max	Units
V_{OS}	Input Offset Voltage	No Load		3	±10	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Drift[1]			±6	±30	µV/°C
I_B	Input Bias Current			±1	±5	µA
$\Delta I_B/\Delta T$	Input Bias Current Drift[1]			±8	±40	nA/°C
Rin	Input Resistance[1]		1			MΩ
Cin	Input Capacitance[1]			0.5	2	pF
CMIR	Common Mode Input Range		±2.5			V
CMRR	Common Mode Rejection Ratio	No Load	70	100		dB
PSRR	Power Supply Rejection Ratio	No Load	65	80		dB
Is	Quiescent Supply Current	No Load		33	48	mA
R_{OUT}	Output Impedance (Closed Loop)[1]	Enabled, At DC		0.2		Ω
I_{OUT}	Output Current	Per Amplifier	35			mA
V_{OUT}	Output Voltage Swing	No Load	±2.5	±3.0		V
		R_L = 150Ω	±2.5	±3.0		V
A_{VOL}	Open-loop Gain		60	75		dB

Note:

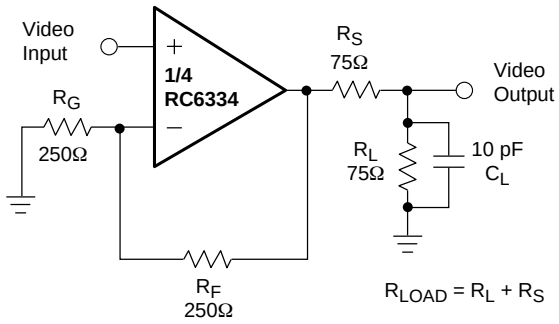
1. Guaranteed by design.

AC Characteristics

V_{CC} = 5V, V_{EE} = -5V, A_V = 2, T_A = 0 to 70°C, R_{LOAD} = 150Ω, R_G = R_F = 250Ω, C_L = 10 pF, unless otherwise specified. Closed Loop. Guaranteed by Design. See Typical Test Circuit.

Parameter		Conditions	Min	Typ	Max	Units
Frequency Response						
BW	-3 dB Bandwidth (A_V = 2)	V_{OUT} = 0.4 Vpp		+175		MHz
		V_{OUT} = 0.8 Vpp	75	90		MHz
Flat	±0.1 dB Bandwidth	V_{OUT} = 0.4 Vpp	50	60		MHz
Peak	Maximum Small Signal AC Peaking	V_{OUT} = 0.8 Vpp		0.01		dB
X_{TALK}	Crosstalk Isolation	@ 5 MHz		50		dB
Time Domain Response						
t_{r1}, t_{f1}	Rise and Fall Time 10% to 90%	2V Output Step		10	15	ns
ts	Settling Time to 0.1%	2V Output Step		15		ns
OS	Overshoot	2V Output Step		5		%
US	Undershoot	2V Output Step		2		%
SR	Slew Rate	V_{OUT} = ±2.0V	200	250		V/µs
Distortion						
HD_2	2nd Harmonic Dist. @ 20 MHz	V_{OUT} = 0.8 Vpp		-48		dB
HD_3	3nd Harmonic Dist. @ 20 MHz	V_{OUT} = 0.8 Vpp		-56		dB
Video Performance						
DG	Diff. Gain (p-p), NTSC & PAL	R_L = 150Ω, V_{OUT} = ±1.5V		0.06		%
DP	Diff. Phase (p-p), NTSC & PAL	R_L = 150Ω, V_{OUT} = ±1.5V		0.06		Deg.
NF	Noise Floor	>100kHz		-130		dB rms

Test Circuit



Applications Discussion

Capacitive Load

The RC6334 can drive a capacitive load from 10 to over 50 pF. In back terminated video applications, bandwidth will only be limited by the RC time constants of the external output components. When driving a 75Ω cable, place the 75Ω source termination resistor as close to the amplifier output as possible.

DC Accuracy

Since the RC6334 is a voltage-feedback amplifier, the inverting and non-inverting inputs have similar impedances and bias currents. To minimize offset voltage, match the source resistances seen by inverting and non-inverting inputs.

Feedback Components

Because the RC6334 is a voltage-feedback amplifier, it facilitates using reactive (capacitive and inductive) feedback components for implementing filters, integrators, sample/hold circuits, etc. The feedback network and the parasitic capacitance at the inverting (summing junction) input create a pole and affect the transfer function of the circuit. For stable operation, minimize the parasitic capacitance and equivalent resistance of the components used in the feedback circuit.

Circuit Board

High-frequency applications require good grounding, power supply decoupling, low parasitic capacitance and inductance, and good isolation between the inputs to minimize their crosstalk. Avoid coupling from output to input to prevent positive feedback.

Notes:

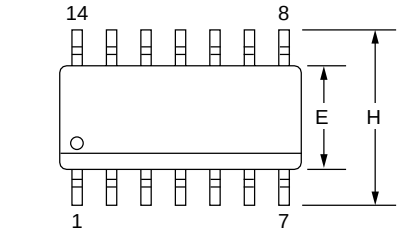
Notes:

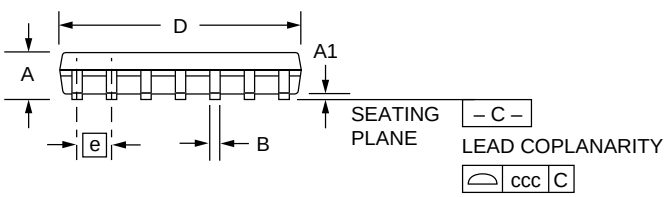
Mechanical Dimensions – 14 Pin SOIC Package

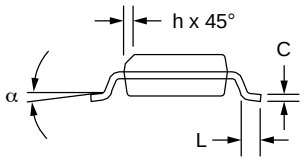
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.19	0.25	5
D	.336	.345	8.54	8.76	2
E	.150	.158	3.81	4.01	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	14		14		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
RC6334M	0° to 70°C	Commercial	14 Pin Narrow SOIC	RC6334M

RC6505

Differential IF Front-End

Features

- Integrated Analog IF Front-End
- Fully differential I/O
- IF flat bandwidth from 25 MHz to 55 MHz
- 48dB minimum gain at IF frequency
- Simple interface to SAW filter
- 9dB input noise figure
- Direct interface to A/D converter
- XTAL oscillator operating to 80MHz
- More than 50dB IMD3
- Industry standard 24-lead SOIC package

Applications

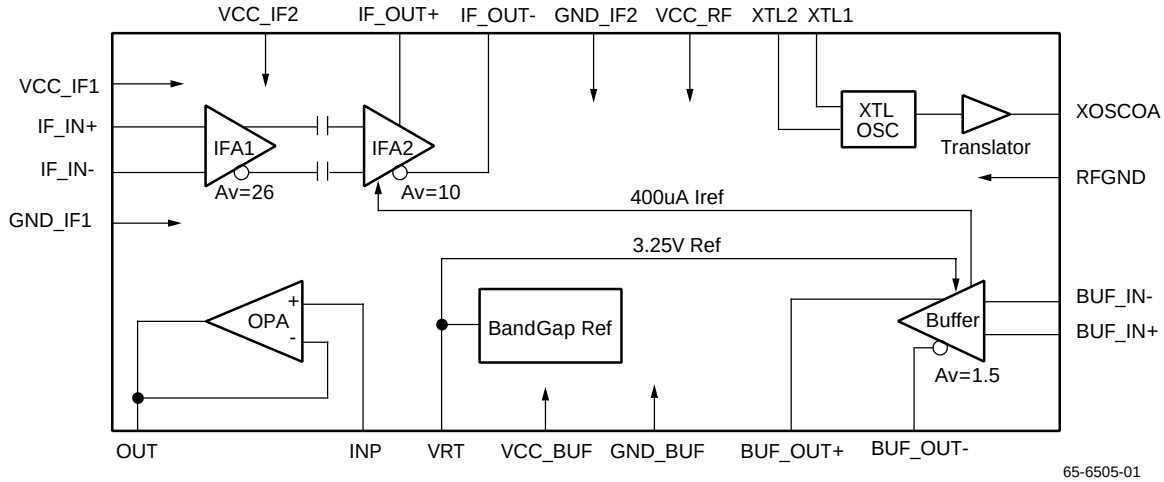
- IF sampling decoders
- QAM Receivers (up to 256 Constellations)
- Set-top receivers for digital cable
- Internet surf boards
- Cable modems
- Desktop video Conferencing

Description

The RC6505 incorporates IF gain stages, reference generators and a crystal oscillator on a single chip. The high input impedance enables direct interface to a SAW filter, while maintaining a low noise figure. The IF output can be further filtered externally and fed to the on-chip fully differential buffer/driver. This buffer is extremely useful when driving low impedance terminations like a differential input to an A/D. The RC6505 is specially suited in IF sampling applications for minimizing the parts count and thus achieving smaller board sizes and lower system costs.

The IF section works on a 12V supply voltage. The oscillator section runs on 5V supply. The RC6505 is available in a 24 Lead SOIC package.

Block Diagram



Preliminary Information

Functional Description

The RC6505 as shown in the block diagram performs several analog signal processing typically required in modern wide-band digital receivers. These include:

- IF Sections
- Bias Voltage Generation
- Crystal Oscillator

IF Gain Section

The front end IF section provides greater than 48dB of stable gain at IF frequencies.

The input has high impedance while maintaining a low noise figure. The input and output sections are on different supplies to minimize parasitic couplings and prevent oscillations. The differential signal fed at IF_IN + /IF_IN- is available at IF_OUT+ /IF_OUT- after amplification.

This output can be filtered externally and fed back into the IC at pins BUF_IN+ & BUF_IN- to enhance the drive capability of the output and also to reduce any 'kick-back' from the A/D sampling.

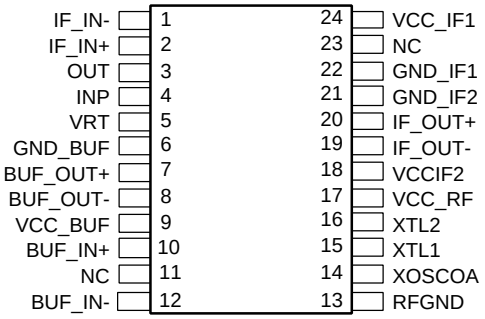
Bias Reference Voltage

The RC6505 has a built-in 3.25V references and an operational amplifier (OPA) with the ability to drive 10mA of load. The OPA will serve as a voltage follower to provide certain flexibility on application. Note that, the 3.25V reference has sourcing capability only.

Crystal Oscillator

This section has a crystal oscillator that can be used to generate timing signals like an A/D clock. The output level of Crystal Oscillator will be TTL compatible at the XOSCOA terminal.

Pin Assignments



65-6505-02

Pin Descriptions

Pin Number	Pin Name	Description
1	IF_IN-	IF Input Complement.
2	IF_IN+	IF Input.
3	OUT	Output of OPA.
4	INP	Non-Inverting Input of OPA.
5	VRT	Output Reference Voltage for Top of A/D Input Range.
6	GND_BUF	Ground for Output Buffer.
7	BUF_OUT+	Differential Buffer/Driver Output.
8	BUF_OUT-	Differential Buffer/Driver Output Complement.
9	VCC_BUF	Supply Voltage for Output Buffer.
10	BUF_IN+	Differential Buffer/Driver Input.
11	NC	No Connect or Ground.
12	BUF_IN-	Differential Buffer/Driver Input Complement.
13	RFGND	Ground for High Frequency Crystal Oscillator.

Pin Descriptions (continued)

Pin Number	Pin Name	Description
14	XOSCOA	Crystal Oscillator Output (TTL compatible).
15	XTL1	Crystal Oscillator Frequency Select Circuit Connection.
16	XTL2	Crystal Oscillator Feedback Pin.
17	VCC_RF	Supply Voltage for High Frequency Crystal Oscillator.
18	VCCIF2	Supply Voltage for IF Output Sections.
19	IF_OUT-	IF Output Amplified, Complement.
20	IF_OUT+	IF Output Amplified.
21	GND_IF2	Ground for Amplified IF Output.
22	GND_IF1	Ground for IF Input Section.
23	NC	No Connect or Ground.
24	VCC_IF1	Supply Voltage for IF Input Section.

Absolute Maximum Ratings (Beyond which the device may be damaged)[1]

Parameter	Description	Min.	Typ.	Max.	Units
V_{CC}	Supply Voltages ,VCC_IF1, VCC_IF2, VCC_BUF, VCC-RF			13.5	V
V_{in}	Input Voltages IF_IN+, IF_IN-, BUF_IN+, BUF_IN-, XTL1, XTL2	GND−0.3		VCC+0.3	V
I_{in}	Input Current (Power On or Off)			±10	mA
T_{stg}	Storage Temperature	-40		125	°C
T_j	Junction Temperature			150	°C
Θ_{JA}	SO24 Thermal Resistance		70		°C/W
Lead soldering	10 seconds			300	°C
Short Circuit Tolerence	No output can be shorted to ground				

Note:

1. Functional Operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Units
VCC_IF1, VCC_IF2, VCC_BUF	Supply Voltages	8.5	12	13	V
VCC_RF	Supply Voltage	4.75	5	5.25	V
TA	Ambient Temperature	0	25	70	°C

Preliminary Information

DC Electrical Characteristics

VCC_RF = 5V; VCC_IF1, VCC_IF2, VCC_BUF = 12V; TA = 0 to 70°C, unless otherwise specified.

Parameter		Conditions	Min.	Typ.	Max.	Units
PW	Total Power Consumption			0.72	0. 87	W
ICCIF1 + ICCIF2	IF Gain Stages total Supply Current	12V Supply		30	35	mA
ICCBUF	Buffer Supply Current (Including 10mA allocated for Band-gap Reference and OPA)	12V Supply		28	35	mA
ICCRF	XTL OSC Supply Current	5V Supply		12	15	mA
VRT	Top Reference Output Voltage	@ 5mA output	3.08	3.25	3.45	V
IOPA	Output Drive of OPA		-0.1		-15	mA
Vos	Output Offset of OPA	V_{OUT} = 2V	-8		+8	mV
I_{BIAS}	Input Bias Current of OPA	V_{INP} = 2V			-5	μA
PSRR	Power Rejection Ratio of OPA	VCC_BUF = 8.5 - 13.5V	55			dB
Avf	Gain of OPA (Voltage Follower)	V_{INP} = 2V	0.98	1.0	1.02	
Vi_{OPA}	Input Range of OPA	I_O = 1mA	0.6		VCC_BUF - 3.0	V
IIF2O	Output Current Drive at IF_OUT+ and IF_OUT-				±15	mA
IBUFO	Output Current Drive at BUF_OUT+ and BUF_OUT-		±5		±15	mA
ΔVIFO	IFA DC Output Swing at IF_OUT+ and IF_OUT- (Differential)		4			Vpp
ΔVBUFO	Buffer DC Output Swing at BUF_OUT+ and BUF_OUT- (Differential)		4.0			Vpp
V_{OH}	High Level Output Voltage of XOSCOA		3.0			V
V_{OL}	Low Level Output Voltage of XOSCOA				0.5	V
I_{OH}	High Level Output Current of XOSCOA				-8	mA
I_{OL}	Low Level Output Current of XOSCOA		8			mA

Note:

1. All currents specified herein are quiescent current without loading on outputs.

AC Electrical Characteristics

VCC_RF = 5V; VCC_IF1, VCC_IF2, VCC_BUF = 12V; TA = 0 to 70°C, unless otherwise specified.

Parameter		Conditions	Min.	Typ.	Max.	Units
ZIFin	AC Input Impedance of IF Amplifier	@36MHz	2			KΩ
CIFin	AC Equivalent Input Cap	IF_IN+ & IF_IN-		6		pF
Vis	Input Sensitivity at Maximum Gain		50			dBμV
Zo_{IF2}	AC Output Impedance of IF Amplifier	@36MHz			10	Ω
Zi_{BUF}	AC Input Impedance of Buffer	@36MHz		7.5K Ω// 3.5pF		
Zo_{IF2}	AC Output Impedance of Buffer	@36MHz			10	Ω
IMD3	Two Tone Intermodulation	Differential Output, BUF_OUT = +10dBm Differential AC Rload = 200Ω at IF_OUT+ & IF_OUT- f1/f2 = 35.5/36.5MHz	50			dBc
G	IF to Baseband Gain	Diff. Input and diff. Output	48		55	dB
NF	Noise Figure	@36MHz		9	12	dB
BW_IF	IF Bandwidth	±0.2dB for 10MHz bands	25	36	55	MHz
ΔBW	Bandwidth Roll-Off	31MHz-41MHz		0.1	0.15	dB
IΦ	Integrated Phase Noise	With TBD crystal@57.6MHz from 100Hz - 1MHz			0.5	deg r.m.s
ΦnXTL	XTAL OSC Phase Noise	@± 10KHz offset			-100	dBC/ Hz
dt/dv	Output Transition Rise or Fall Rate	XTL Oscillator Output, C_L = 10pF			2.5	nS/V
d_{OSC}	Duty Cycle of Output Pulse	XTL Oscillator Output, C_L = 10pF	40		60	%

Performance Curves

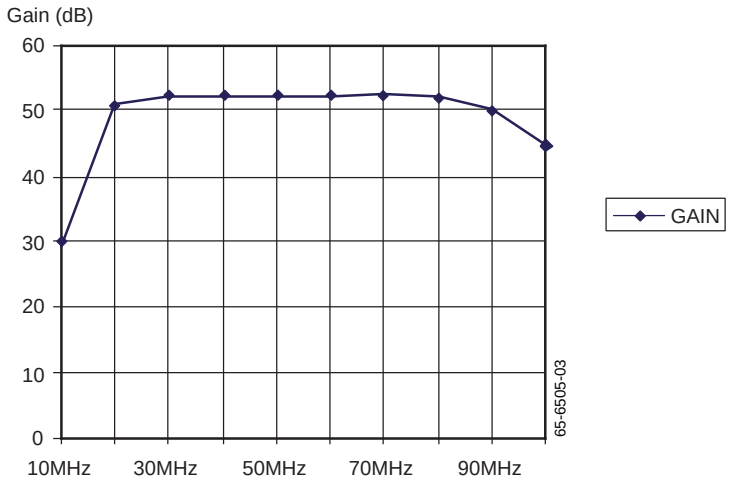


Figure 1. IF Input Bandwidth

Preliminary Information

Application Discussion

The RC6505 is specially suited for use in set-top boxes and cable modems for decoding QAM modulated signals based on IF sub-sampling techniques. The RC6505 simplifies the front-end design and makes it more cost effective by integrating in a single chip all the analog processing functions needed between the standard tuner and high performance A/Ds. The other major components required for the front-end of the modem are the tuner, a SAW filter, crystal and the appropriate DSP demodulator/decoder.

DVB Set-top Application

Figure 2 shows the application of RC6505 in IF bandpass sampling decoder for 256QAM cable transmissions. Here, the sampling clock for the A/D conversion can be generated using the crystal oscillator operating in the 3rd overtone mode at 57.6MHz and an external divided by 2 prescaler. The reference signals for A/D are the VRT and OUT outputs. The application is shown with the Fairchild Semiconductor Division's 10-bit ADC TMC1185. Other high performance A/Ds needing fully differential input can also be used. The A/D inputs are referenced to be in the mid-scale using the output from TMC1185. The filtered and buffered IF outputs can be a.c. coupled to the A/D inputs. In this application an external differential band-pass roofing filter is used to band-limit the signals before conversion.

Figure 3 shows details of circuits used to evaluate the performance of RC6505 with the TMC1185 A/D.

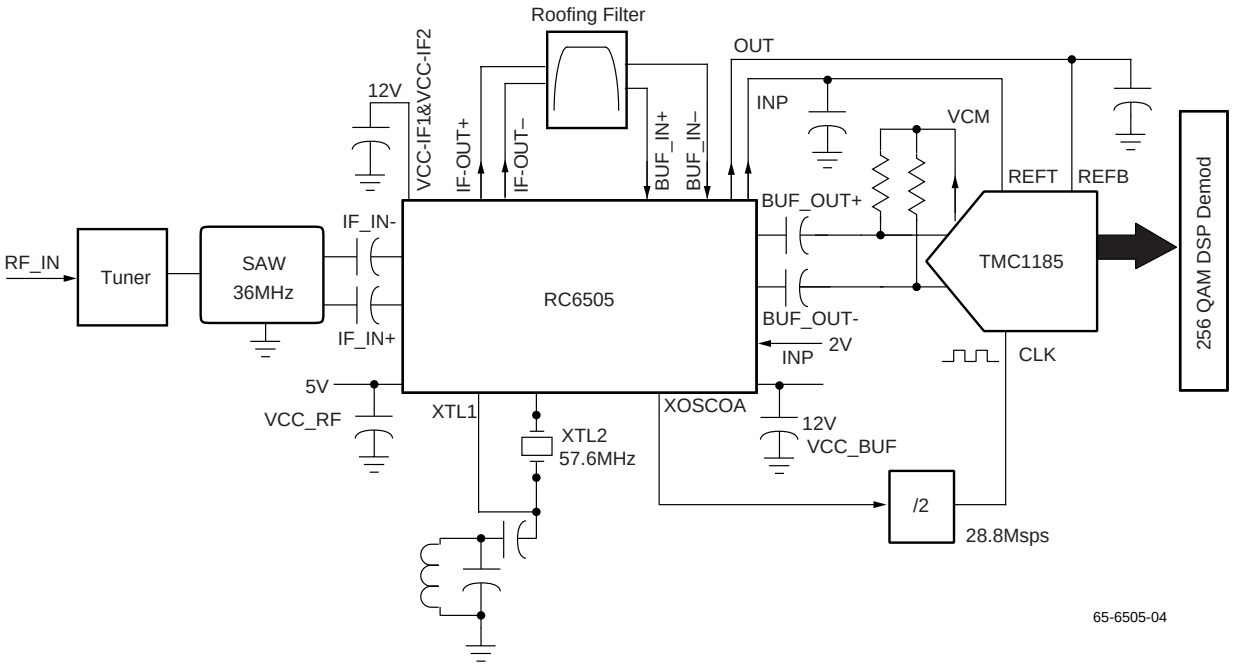


Figure 2. RC6505 Application in a Sub-sampling Digital Receiver for 256 QAM

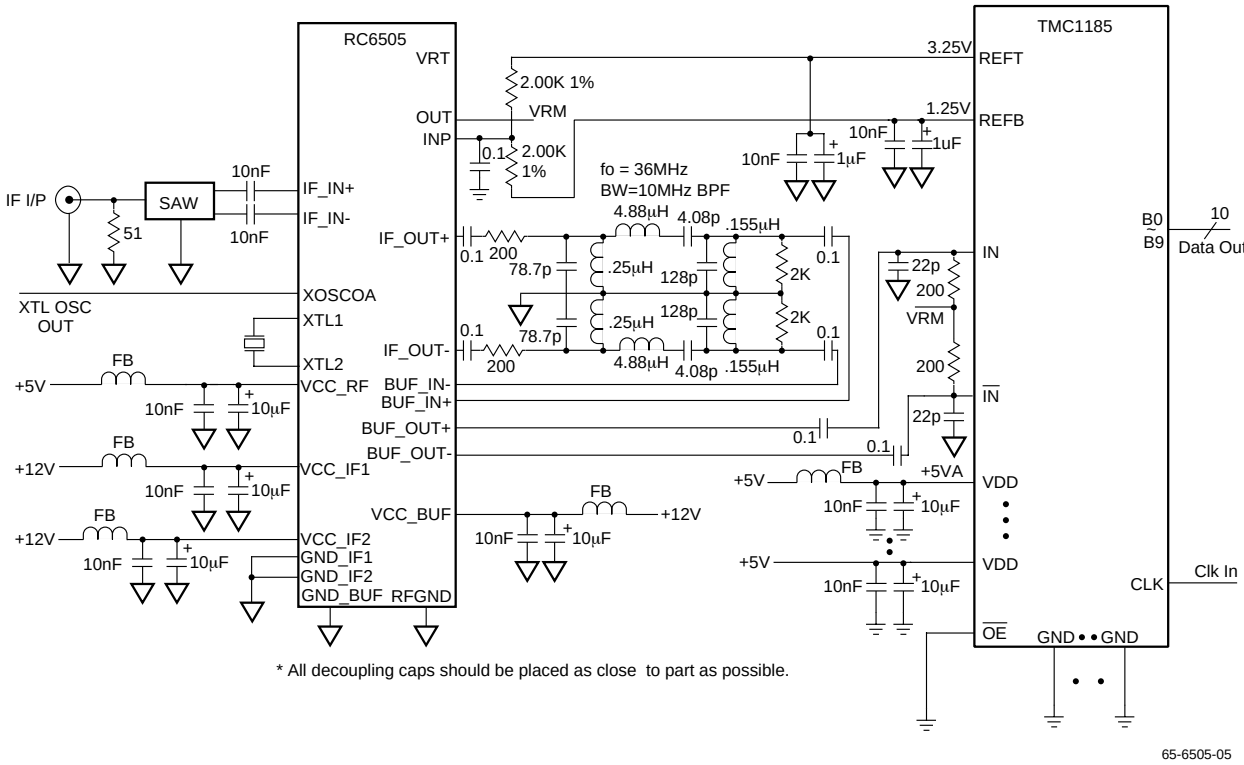
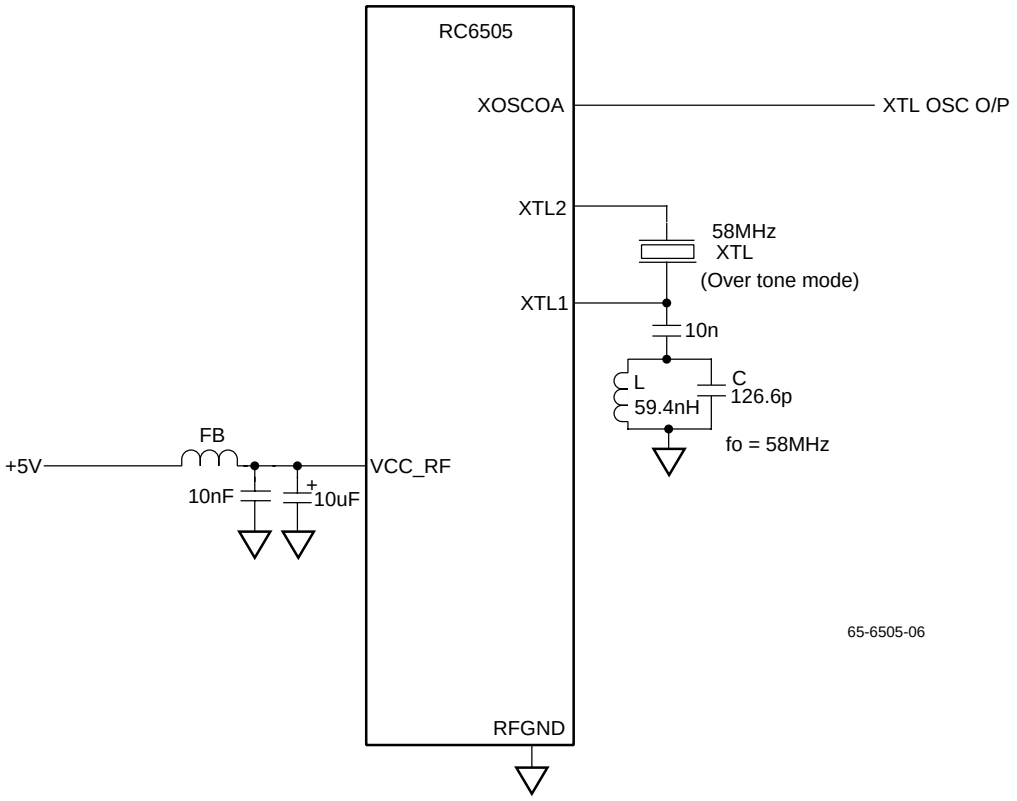


Figure 3. RC6505 interface with Fairchild Semiconductor Division's TMC1185 10-bit 40MSPS ADC (for reference only)

Preliminary Information

Crystal Oscillator Operating in Over Tone Mode



Choose Q = 12 then using the following equations to calculate L and C. (Note that, Rin = 260 Ω and f_O is given.)

$2\pi f_O = (LC)^{-1/2}$
$Q = 2\pi f_O C Rin$

Notes:

Notes:

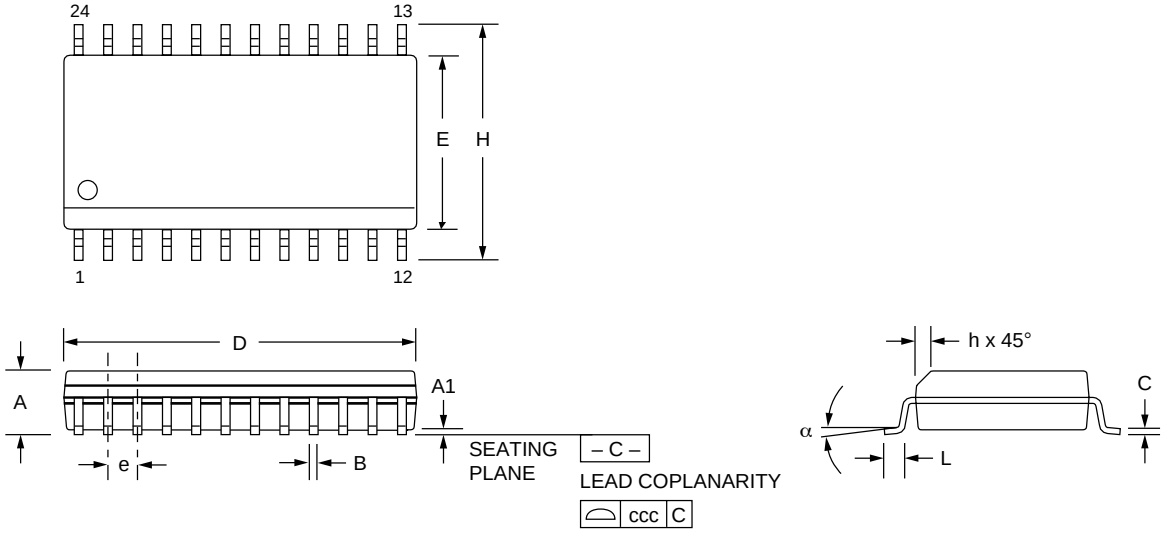
Mechanical Dimensions

24 Lead Small Outline IC (SOIC) – .300" Body Width

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.599	.614	15.20	15.60	2
E	.290	.299	7.36	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.020	0.25	0.51	
L	.016	.050	0.40	1.27	3
N	24		24		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.



Preliminary Information

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
RC6505M	0°C – 70°C	Commercial	24 Lead SOIC	RC6505M

Preliminary Information

5/20/98 0.0m 001
Stock#DS30006505

RC6508

QAM IF Downconverter

Features

- Integrated IF Down Converter
- IF bandwidth from 30 MHz to 80 MHz
- Operating range between 8.5V to 13.2V
- 63dB peak conversion gain from IF to baseband
- 40dB minimum AGC range
- Simple interface to SAW filter and A/D converter
- Gain control minimizes noise figure and distortion
- Tuner control feature interfaces with variety of tuners
- Industry standard 24 Lead SSOP package

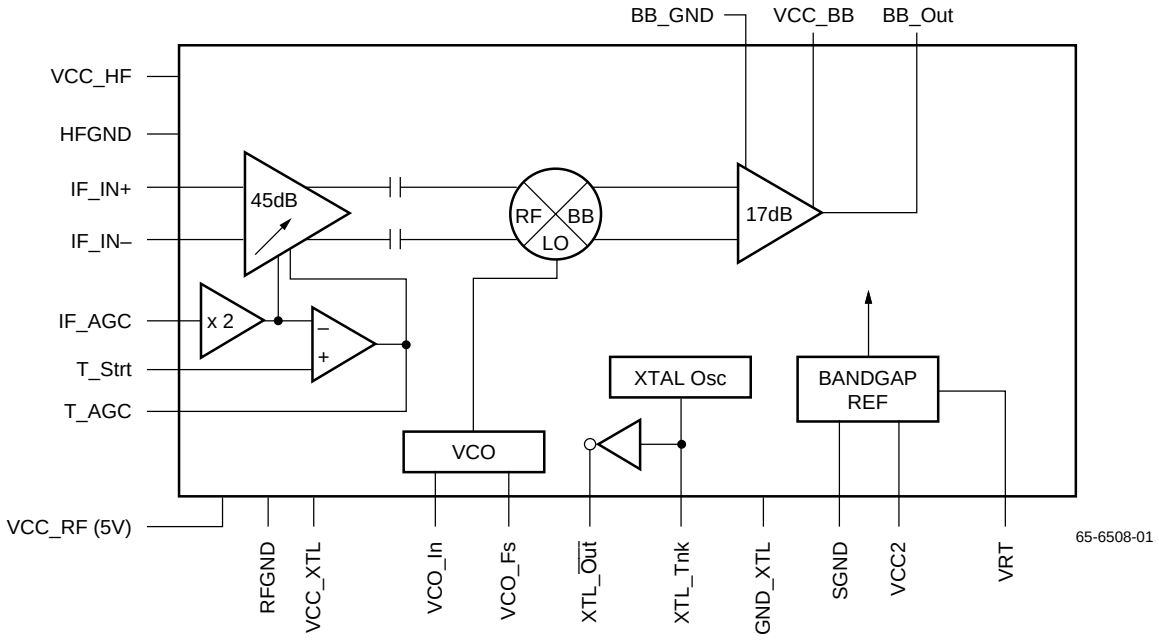
Applications

- Digital Set-top Receivers
- Cable Modems

Description

The RC6508 simplifies the front-end design of cable modem and set-top receivers. It is a cost-effective solution, since it integrates IF amplifier, AGC, mixer, amplifier, tuner AGC, VCO, XTAL OSC, and bandgap reference on a single chip. The RC6508 downconverts the IF signal to baseband signal for cable modem and set top receivers. The baseband signal can be digitized and decoded with an external A/D converter and a custom DSP demodulator. The input can directly interface to a SAW filter and maintain a low noise figure. The gain can be controlled over a 40dB range through an external analog input signal. The gain reduction is done in two stages with minimum noise figure and signal distortion. The IF output is then down converted and filtered using a double balanced mixer. The output can be further filtered with an external filter prior to A/D conversion. The RC6508 has an added feature that it provides an optimum tuner AGC control voltage which is used to control the front end tuner gain. The IF and Mixer section works at 9V and the oscillator works on 5V supply. The RC6508 is available in a 24 Lead SSOP package.

Block Diagram



Functional Description

The RC6508 shown in the block diagram performs all the IF and baseband signal conversion with the minimal external components. It consists of three general sections:

- IF Gain Section
- IF Down Conversion and Frequency Synthesis
- Reference Voltage

IF Gain Section

This is the first stage of the IF-to-Baseband conversion**.** The IF input signal is fed into a variable gain control amplifier that is capacitively coupled to the subsequent stages. The gain control amplifier has stabilized gain over temperature and supply variations. The amplifier gain is directly proportional to the IF_AGC voltage. The gain in various stages is not reduced at the same time in order to minimize the noise figure degradation. The transition point is set by the voltage on T_Strt pin. T_strt sets the T_AGC trigger to control the front end tuner gain.

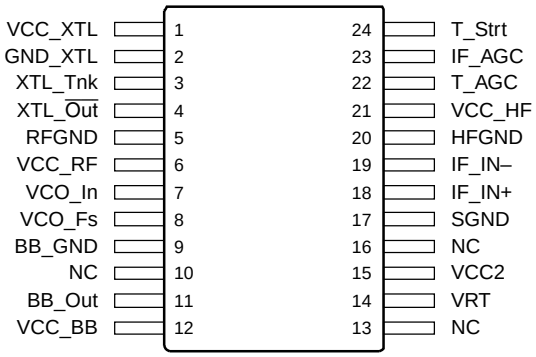
IF Down Conversion and Frequency Synthesis

This is the second stage of the IF-to-Baseband conversion. It consists of a double balanced linear mixer. The output of the front end gain stage is capacitively coupled to the input (RF port) of the mixer. The LO signal for the mixer can be directly driven or synthesized with the Voltage Controlled Oscillator (VCO). This section has also a crystal oscillator that can be used to generate a master clock for the frequency synthesis. The mixer translates the signal to a second IF frequency equal to the symbol rate and passes through an amplifier. The final output is a baseband signal, BB_Out. This signal can be further filtered externally before connecting it to an external ADC and QAM demodulator.

Reference Voltage

The RC6508 has a built-in 2.0V reference with capability of driving 10mA load and can be used to set up A/D reference.

Pin Assignments



65-6508-02

Pin Descriptions

Pin Name	Pin Number	Pin Function Description
BB_GND	9	Ground Connection.
BB_Out	11	Baseband Voltage output.
GND_XTL	2	Crystal Oscillator Ground.
HFGND	20	Analog Ground Connection.
IF_AGC	23	Input Voltage for IF Front End Gain Control.
IF_IN+,IF_IN–	18,19	IF inputs.
NC	10,13,16	No Connection.
RFGND	5	Ground Connection for High Frequency Mixed Signal Sections.
SGND	17	Analog Ground Connection.
T_AGC	22	Output Voltage for Tuner Gain Control.
T_Strt	24	Threshold Voltage Input for Starting Tuner Gain Control.
VCC_BB	12	Baseband Supply Voltage, typically 9V.
VCC2	15	Analog Supply Voltage (9V).
VCC_HF	21	Analog Supply Voltage (9V).
VCC_RF	6	Supply Voltage (5V) for High Frequency Mixed Signal Sections.
VCC_XTL	1	Supply Voltage for Crystal Oscillator.
VCO_Fs	8	VCO External Frequency Select Circuit Connection.
VCO_In	7	VCO Input, can be used for directly feeding external LO.
VRT	14	Output reference voltage for top of A/D input range.
XTL_Out	4	Crystal Oscillator Output.
XTL_Tnk	3	Crystal Oscillator Frequency Select Circuit Connection.

Absolute Maximum Ratings

Parameter		Min.	Typ.	Max.	Units
IF_IN+, IF_IN–, IF_AGC, T_Strt	Input Voltages	GND – 0.3		VCC + 0.3	V
VCC_RF, VCC_BB, VCC_HF, VCC2, VCC_XTL	Analog Supply Voltages			13.5	V
Tstg	Storage Temperature	-40		125	°C

Operating Conditions

Parameter		Min.	Typ.	Max.	Units
VCC	Analog Supply Voltage	8.5	9	13.2	V
VCC_RF	Supply Voltage for IF and Mixer	4.75	5	5.25	V
VCC_XTL	Supply Voltage for XTLOSC and VCO				
T	Temperature	0		70	°C

DC Electrical Characteristics

VCC_RF, VCC_XTL = 5V; VCC_HF, VCC_BB, VCC2 = 9V; T_A = 0 to 70°C, unless otherwise specified.

Parameter		Conditions	Min.	Typ.	Max.	Units
PWIF	Power Consumption in IF			0.4	0.5	W
ICCHF	Front End Supply Current	9V Supply		20	25	mA
		12V Supply		27	35	
ICCBB	Back and Baseband Current	9V Supply		21	25	mA
ICCRF	RF Supply Current	5V Supply		6	10	mA
VRT	Reference Output Voltage		1.95	2.05	2.15	V
ΔVBBo	Baseband DC Output Swing		3.5			Vpp
Tagc_hi	Tuner AGC for Maximum Gain	IF_AGC = 5V		7.5		V
Tagc_lo	Tuner AGC for Minimum Gain	IF_AGC = 2V		2		V

AC Electrical Characteristics

VCC_XTL, VCC_RF = 5V; VCC_HF, VCC_BB = 9V; IF_AGC = 2V; Tsrt = 5V; T_A = 0 to 70°C, unless otherwise specified.

Parameter		Conditions	Min.	Typ.	Max.	Units
ZIFin	AC Input Impedance	@43.75MHz	2			KΩ
CIFin	AC Equivalent Input Cap	IF_IN±		6		pF
Vis	Input Sensitivity at Maximum Gain	Vagc=2.5V		250		μV
IMD3	Two Tone Intermodulation	f1/f2 = 43.75/42.75 MHz, IF_IN = -16dBm, VCO_IN = 0.1Vpp, LO = 38.75MHz[1]		45		dB
G	IF to Baseband Gain	IF_AGC = 2V	35	40		dB
NF	Noise Figure (Maximum Gain)			9		dB
Ragc	AGC Gain Range	IF_AGC = 0V-4V	40	43		dB
Sagc	AGC Sensitivity Average Slope	T_Strt = 5V, F_AGC = 0.8V-4V		10		dB/V
BW_IF	IF Bandwidth	0.1dB for 10MHz bands	30	43.75	75	MHz
		0.1dB for 5MHz bands	30		80	
fLO	Down Conversion Frequency	VCO-IN=0.1Vpp			100	MHz
ΦnLO	VCO Phase Noise	@ ±10KHz offset			-80	dBC/Hz
ΦnXTL	XTAL OSC Phase Noise	@ ±3KHz offset			-80	dBC/Hz

Note:

1. With the application of antialiasing filter as load.

Typical Performance Characteristics

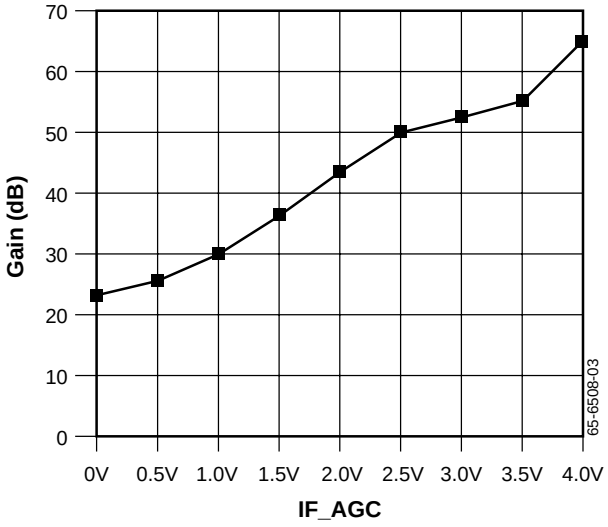


Figure 1. Typical IF_AGC Control Characteristics

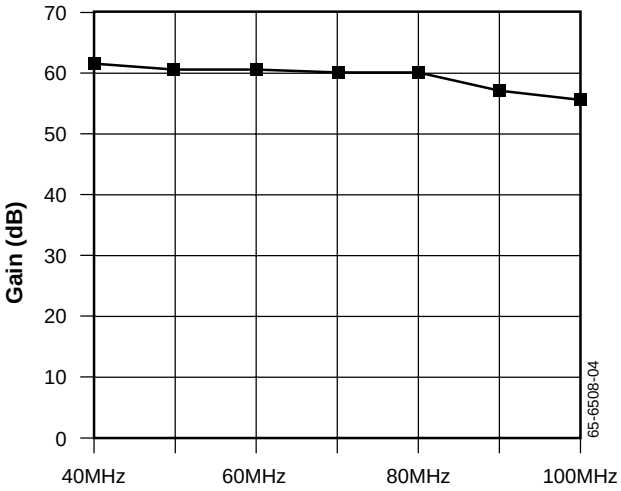


Figure 2. IF Input Bandwidth

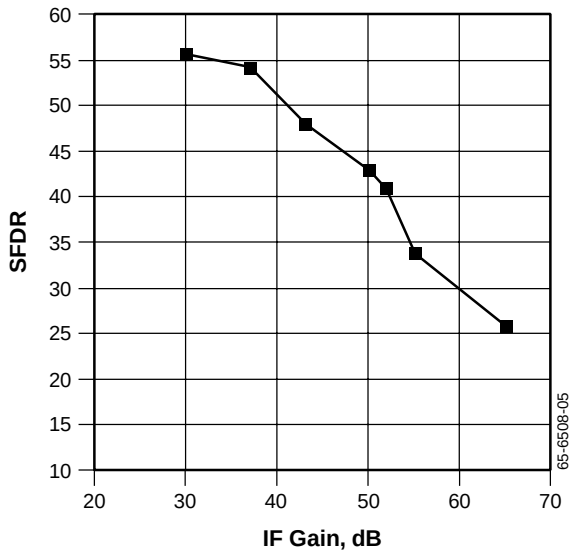


Figure 3. SFDR vs. RC6508/TMC1175AM7C40 (Fairchild Semiconductor Demo Board with 64 QAM demodulator)

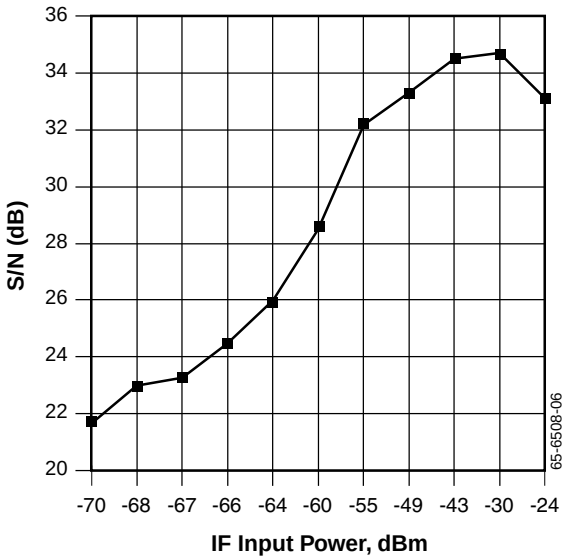


Figure 4. S/N vs. IF Input Power RC6508/TMC1175AM7C40 (A/D IN = 2Vpp) (Fairchild Semiconductor Demo Board with 64 QAM demodulator)

Applications

The RC6508 is designed to down convert QAM IF signals. It interfaces easily with Fairchild Semiconducto's TMC1175A A/D converter and a DSP.

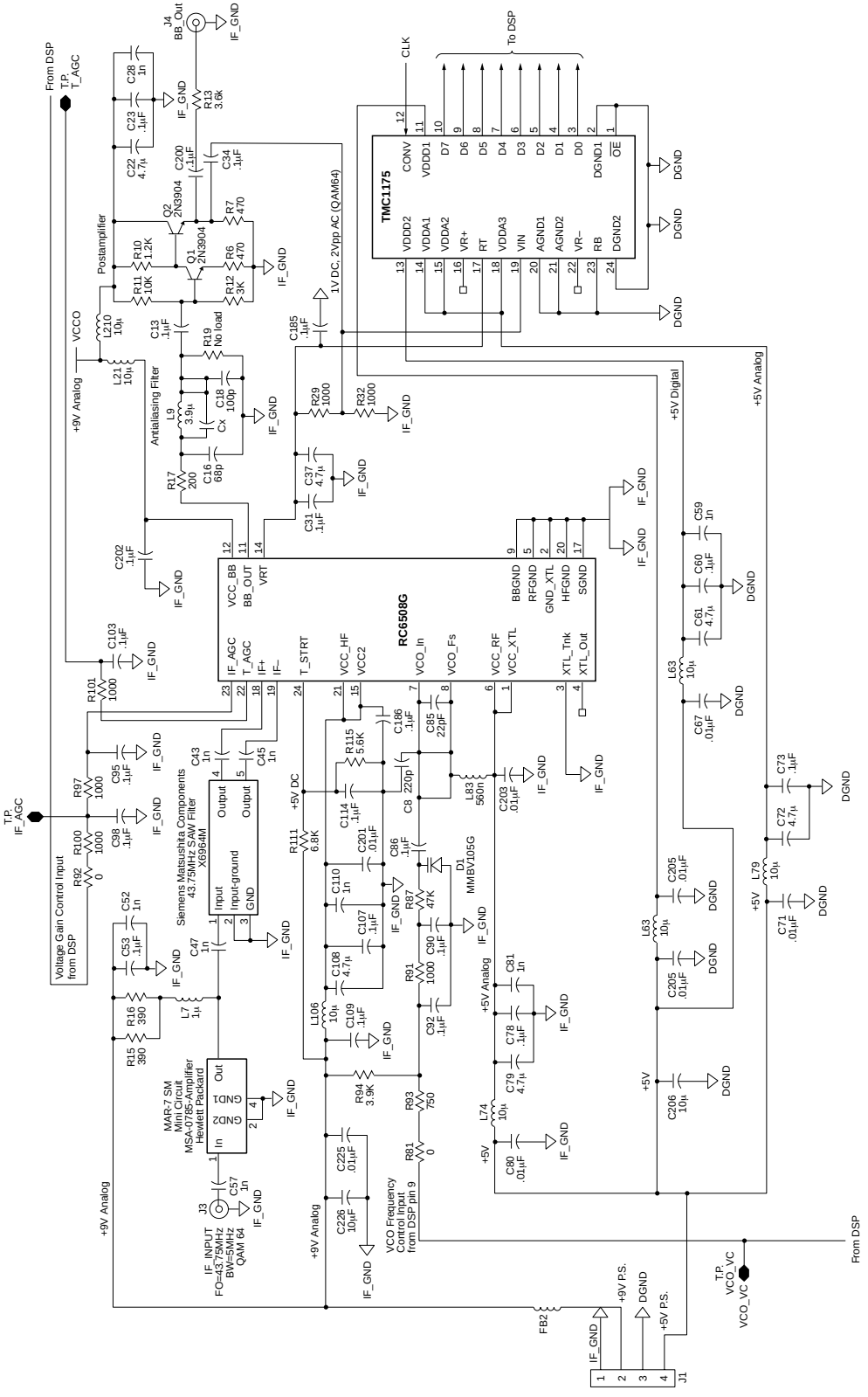
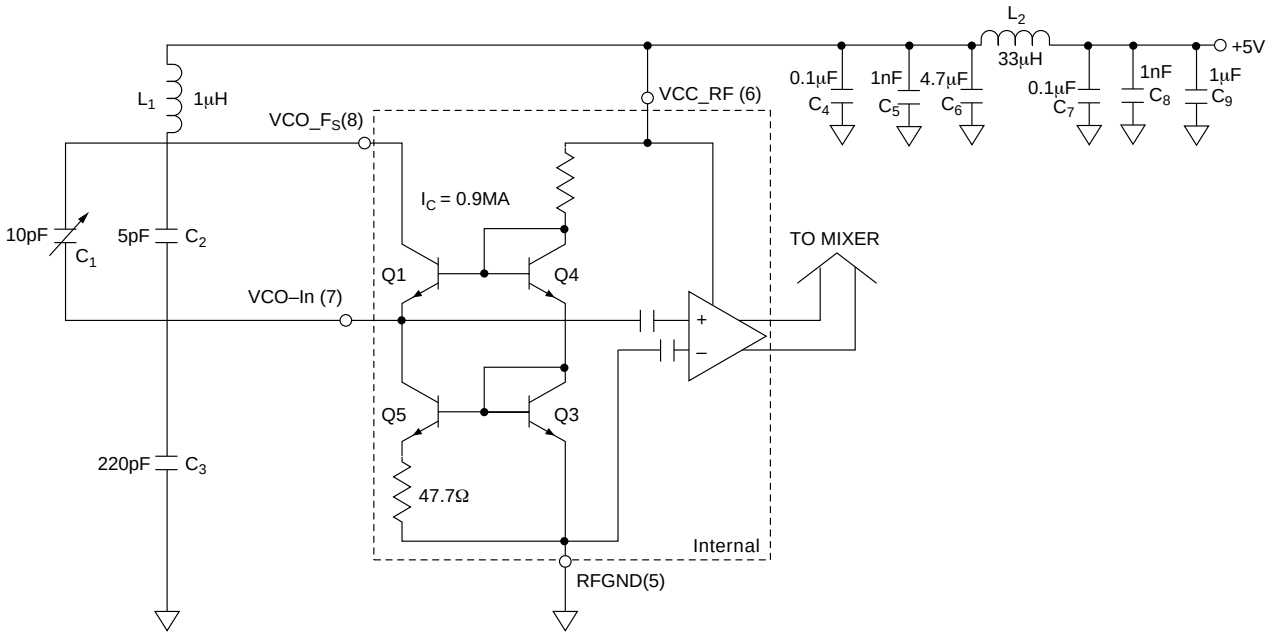


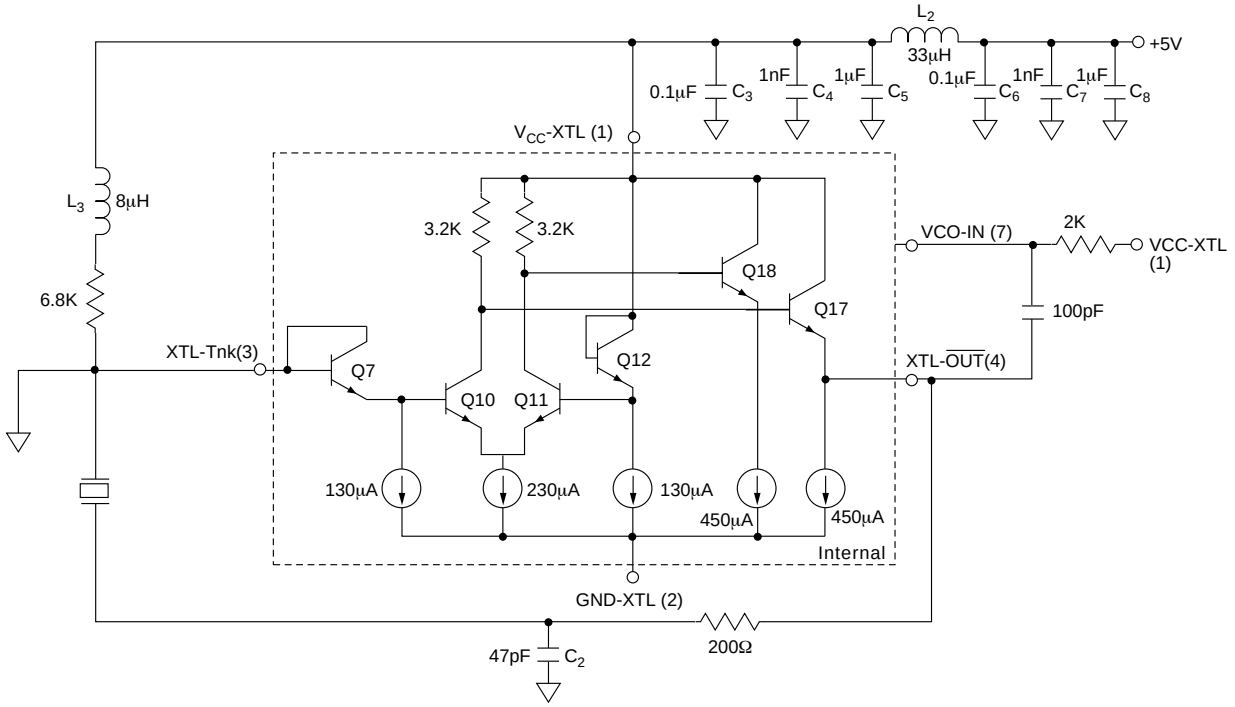
Figure 5. Application of RC6508 in Cable Modem Receivers (Fairchild Semiconductor Demo Board with 64 QAM Demod-

VCO Internal Schematic



The VCO can be designed as a Colpitts oscillator. The above circuit application shows VCO with adjustable typical value of 38.75 MHz. The frequency is controlled by the external resonance circuit. The oscillating transistor is Q1 in common base configuration. To inject signal in the mixer in place of LO, the VCO_Fs must be open. The signal on the pin VCO_In should be under 100mVp-p and AC coupled.

Crystal Oscillator Internal Schematic



The crystal oscillator is an ECL inverter. It is necessary to bias the XTL-Tnk with a choke to 5V VCC_XTL power supply. The output is about 0.7V DC lower than VCC_XTL with an approximate swing of 0.5Vpp at the output. If the oscillator is not used, it is good to ground XTL_Tnk pin.

Notes:

Notes:

Notes:

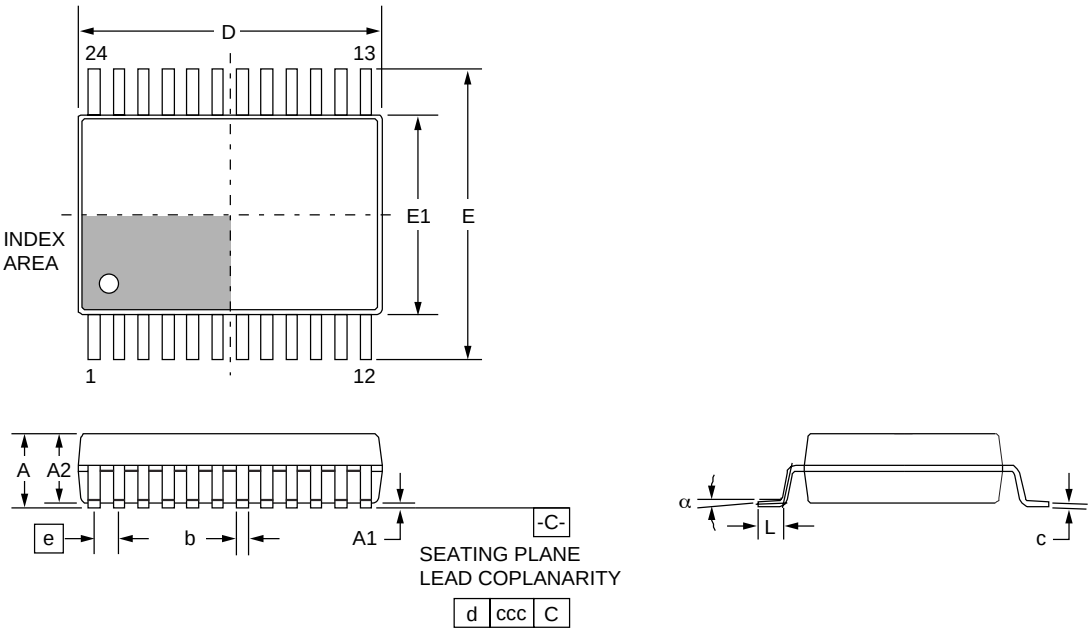
Mechanical Dimensions

24 Lead SSOP Package (5.3mm Body Width)

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.0.78	—	2.00	
A1	.002	—	0.05	—	
A2	.065	.073	1.65	1.85	
b	.010	.015	0.22	0.38	
c	.0035	.010	0.09	0.25	
D	.311	.335	7.90	8.50	
E	.291	.323	7.40	8.20	
E1	.197	.220	5.00	5.60	
e	.026 BSC		0.65 BSC		
L	.022	.037	0.55	0.95	
N	24		24		
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M – 1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .006 inch (0.15mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
RC6508G	0°C–70°C	Commercial	24 Lead SSOP	RC6508G

RC6516

IF Demodulator for Vestigial Side Band Receivers

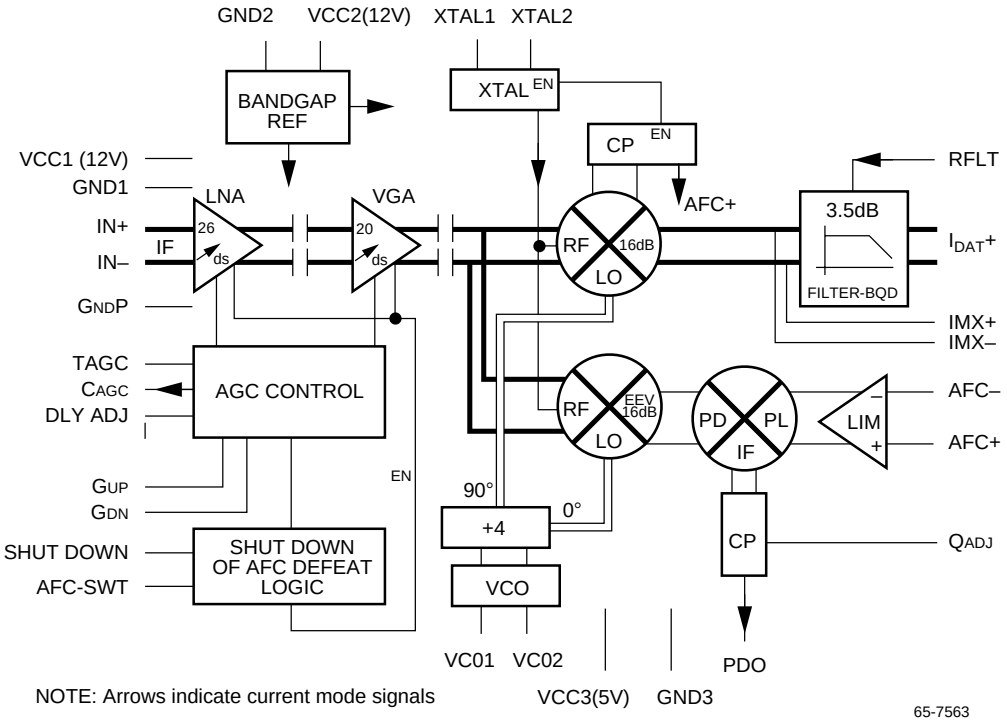
Features

- Demodulates 16 level to 2 level VSB signals
- Versatile delayed AGC & Tuner Controls
- 60dB Gain from IF to baseband
- 45dB AGC range with a digital control
- <1% distortion @ 2 Vpp baseband output
- 50dB typical IMD3
- On-chip low phase noise VCO (100dBc/Hz @ 20KHz from 200MHz)
- Wideband Quadrature Prescalers
- <2° Quadrature phase error
- Programmable Video Filter-Amplifier
- Direct input interface for SAW filters
- 9dB input Noise Figure at max gain
- On-chip band gap reference and temperature compensation
- Available in 28 lead PLCC package

Description

The RC6516 is fully integrated IF Demodulator customized for Vestigal Side Band (VSB) receivers. As shown in the Block Diagram, the IC performs IF amplification with gain control, synchronous demodulation of I & Q channels and carrier recovery using a Frequency & Phase Lock Loop (FPLL). The RC6516 directly provides delayed AGC control for a front end tuner. The demodulated output is filtered and amplified. The device accepts direct digital control inputs from a microprocessor for gain control, calibration and shut down functions. The IC is packaged in a 28-pin PLCC.

Block Diagram



Rev. 0.9.0

Functional Description

The block diagram of the RC6516 consists of three general sections:

1. IF amplifiers with gain control
2. Synchronous demodulator
3. Frequency phase lock loop (FPLL) and auxiliary circuits

The IF Section

There are two IF amplifiers capacitatively coupled to each other and the subsequent stages. The first amplifier has a maximum gain of 24dB and an AGC range of more than 14dB. The second amplifier has a maximum gain of 16dB and gain reduction capability of 30dB. To minimize the Noise Figure degradation with gain reduction the second stage fully gain reduces before the first stage gain reduces. The transition point is set by the voltage on the DLYADJ pin. The voltage on CAGC pin directly determines the gain of the two IF stages. When the voltage on CAGC is lower the IF gain is lower. When the CGAC voltage is higher than the DLYADJ the gain reduction is primarily in the second stage. When the CAGC voltage is lower than DLYADJ, only the first stage gain is reduced at a much slower rate. The tuner AGC control voltage TAGC also changes this range to gain reduce the external tuner. This avoids the amplifiers from being overdriven into distortion. During AFC defeat mode these IF amplifiers are disabled with more than 50dB of signal isolation.

Gain Control

The gain control signal is developed on the capacitor at the CAGC pin, by charge pump and AGC control circuits. TTL/CMOS signals on the G_{UP}, G_{DN} pins build the voltage through the charge pump current at CAGC pin. Continuous pulses on GUP pin increases the CAGC voltage and pulses on the GDN pin reduces the CAGC voltage. Table 1 shows the truth table for gain control.

Synchronous Demodulator

This section consists of In-phase (I) and Quadrature (Q) multipliers/mixers.

During normal operation the incoming signal processed by the two IF stages is capacitatively coupled to the linear (RF) port of both the mixers. The signals for the LO port of the I & Q mixers come from the FPLL section. The switching signals are in quadrature and phase locked to a small pilot present in the IF signal. The signal levels for this multiplying port use limiting amplitudes. The I channel output is then filtered to reject the high frequency components while not distorting the video band signals. The filtered output is also amplified to cover the full range of A/D converter that follows. The Q channel signal is used by the FPLL section described below.

The FPLL Section

The FPLL consists of a VCO working at 4 times the pilot frequency. The frequency is set by external LC components and also controlled with a varactor. This VCO signal is passed through a divide by 4 prescaler to provide two signals in quadrature at the frequency of the pilot. These signals are used by the I & Q multipliers. The VCO is frequency and phase locked to the 4x pilot frequency which is typically 46.69MHz. The VCO thus operates at 186.7MHz in a typical 16 VSB decoder. Frequency acquisition is possible by means of the third multiplier on chip and AFC filter off-chip. The PLL circuit is formed by the Q channel mixer, third multiplier-charge pump, external PLL filter and the VCO.

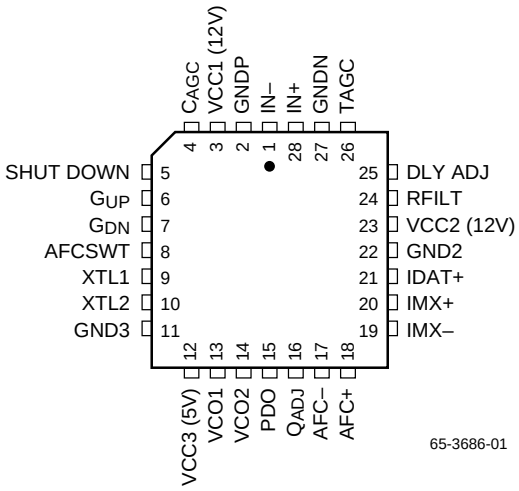
Due to component variations, the VCO frequency may not be within the pull in range of the FPLL. The AFCSW signal is used for activating this start up calibration. An auxiliary crystal oscillator signal at the pilot frequency of 46.6MHz is injected into the input port of the mixers, to pull the VCO to the desired frequency during the start up mode. During this mode the XTAL oscillator and the I-channel charge pump are activated and the IF gain stages are disabled. There is also the shutdown mode during which the VCO, the crystal oscillator and the tuner control are disabled. These various states are determined as shown in Table 1.

Table 1. Truth Table for Digital Circuitry

V_{CC3} = 5V, $V_{CC1,2}$ = 12V, T_A = 0 to 70°C unless otherwise specified

AGC Control		
G_{UP}	**G_{DN}**	**Description**
LO	LO	No Gain Change (over symbol period)
HI	LO	Increase Gain
LO	HI	Decrease Gain
HI	HI	Disallowed
AFC Control		
AFC_SWT	**SHTDWN**	**Description**
LO	LO	Crystal is OFF, VCO is ON
X	HI	Crystal is OFF, VCO is OFF, Tuner AGC is Hi-Z
HI	LO	Crystal is ON, VCO is on, I-channel Charge Pump is ON for acquisition

Pin Assignments



Pin Descriptions

Pin Name	Pin Number	Description
AFC+, AFC–	18, 17	Inputs to the limiter that sets the polarity of the third multiplier in the FPLL loop.
AFCSWT	8	This digital input is LO during normal operation. A TTL/CMOS high input enable the crystal oscillator and an extra I-channel charge pump, while disabling the IF input sections. The crystal oscillator outputs are switched into the input ports of the quadrature mixers. The VCO then locks to 4 x crystal frequency.
C_{AGC}	4	An internal charge pump will develop a voltage across any capacitance on this pin. Voltage on this node directly determines the front end IF gain. When operating on a 12 volt supply, moving this voltage from 9V to 2V reduces the gain by at least 40dB.
DLYADJ	25	The input voltage on this pin determines the transition point for delayed AGC.
G_{DN}	7	A TTL/CMOS high level input on this pin activates internal charge up to decrease the voltage on the CAGC pin.
GND2	22	Ground line for backend. Also the substrate connection to the IC. Should be at the lowest potential to the IC.
GND3	11	Ground line for digital section.
GNDN	27	Shield ground for input.
GNDP	2	Ground signals for front end sections.
G_{UP}	6	A TTL/CMOS high level input on this pin activates internal charge up to increase the voltage on the CAGC pin.
IDAT+	21	Demodulated & filtered output to be ac coupled to A/D converter.
IMX+, IMX–	20, 19	Demodulated output before filtering. DC coupled back to AFC limiter inputs AFC+/AFC– though an external low pass filter.
IN+, IN–	28, 1	IF inputs to be demodulated. Internal dc restoration. External ac coupling required. Usually interfaced to a SAW filter.
PDO	15	Charge pump output from third multiplier. This output can be fed to an external lead-lag filter to develop the voltage required to drive the varactor in feedback till a lock is established with the pilot.

Preliminary Information

Pin Descriptions (continued)

Pin Name	Pin Number	Description
QADJ	16	Offset adjust input pin effectively corrects quadrature phase error. A 20KΩ variable resistor to ground can cover the range of correction.
RFILT	24	Resistor at this pin sets the dominant filter cut-off frequency for the filter internal to the chip between IMX± and IDAT pins. A 4KΩ at this pin gives a 3dB point of 8.3MHz.
SHUTDOWN	5	This digital input should be LOW during normal operation. A TTL/CMOS high input on this pin shuts down all the oscillators
TAGC	26	This voltage output can be used to gain control the tuner front-end.
VCC1	3	Supply voltage for front end sections. Usually 12V.
VCC2	23	Supply voltage for the synchronous demodulator and backend sections. Usually 12V.
VCC3	12	Supply for digital logic, prescalers and oscillators. Usually 5V.
VCO1, VCO2	13, 14	The frequency setting network and the varactor are connected at these pins.
XTL1, XTL2	9, 10	Crystal oscillator pins.

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Positive power supply, VCC		7	V
Negative power supply, VEE		-7	V
Differential input voltage		10	V
Operating temperature	0	70	°C
Storage temperature	-40	125	°C
Lead temperature (10 seconds soldering)		300	°C
Thermal resistance, Θ_{JA}		90	°C/W
Short circuit tolerance: One output can be shorted to ground.			

Note:

1. Absolute maximum ratings are those beyond which operation and reliability of the device cannot be guaranteed. Subjecting devices to these limits for extended periods of time may result in actual failure of the device.

Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
VCC1, VCC2	Analog supply voltages	10.8	12	13.2	V
VCC3	HF supply voltage	4.5	5	5.5	V

DC Characteristics

V_{CC3} = 5V, $V_{CC1,2}$ = 12V, AFC_SWT = OFF, T_A = 0 to 70°C unless otherwise specified

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
ICC – Supply Currents						
ICC1	Front-end Supply Current	VCC1=13.2V		32	40	mA
ICC2	Backend Supply Current	AFC_SW=OFF, AFC_SW=ON, VCC2=13.2		28	34	mA
ICC3	HF Supply Current	AFC_SW=OFF, AFC_SW=ON		16	20	mA
Pw	Total Power Consumption	VCC1,2=13.2V, VCC3=5.5		0.88	1	W
Signals – DC Compliance						
Viout	I-Data Output		4.5	6	7	V
VImix±	I-channel mixer ouput dc		3	4	5	V
δVImix±	I-channel mixer output Differential Offset		-16		16	mV
δAFC±	AFC limiter input Offset	Rs = 2K to 5V.	-4		4	mV
VIoff	Total I-channel Offset		-15		15	mV
ZIout	I-Filter Output impedance			5	10	Ohms
ΔI_{PDO}	PDO charge-pump current swing	PDO to 5V with 10K		±50		mA
δI_{PDO}	PDO charge-pump offset current with offset null over temperature.	Minimized by adjusting 12K variable resistor on Qadj pin.		±200		nA
ΔI_{AFC}	AFC charge pump current swing			±0.6		mA
δI_{AFC}	AFC charge pump offset				±10	μA
I_{OAFC}	AFC charge pump leakage	AFC_SWT=LO			±1.0	μA
I_{VCO1}	VCO external current	VCO1=V_{CC3}		0.5		mA
VCO2	VCO voltage Compliance		0.6		1	V
VX2	Xtal Oscillator Input		2.9		4.9	V
ΔI_{AGC}	AGC charge current swing	Toggle GUP & GDN. Measure current @ 5V		±1		mA
I_{OAGC}	AGC charge pump leakage	G_{UP} & G_{DN} = LO		±125	±250	nA
IF – Signals						
IN±	IF input DC levels			8		V
Rin	Input impedance			3		KΩ
Tagc_hi	Tuner AGC for maximum gain	RLmax=4K,VCC=10.8, VDLY=6V, CAGC=10V		10		V
Tagc_lo	Tuner AGC for minimum gain	VDLY=6V, CAGC=2V		2		V
Tagc_off	Tuner AGC for shutdown	VDLY=6V, CAGC=2-10 SHUTDWN=H	2		10	V
ZTagc	Tuner Impedance during shutdown	VDLY=6V, CAGC=2-10		60		KΩ

Preliminary Information

Digital Signal Characteristics for G_{UP}, G_{DN}, AFC_SWT, SHUTDOWN

V_{CC3} = 5V, $V_{CC1,2}$ = 12V, T_A = 0 to 70°C unless otherwise specified

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
Vth	Logic Threshold	VCC3 = 4.5V, 5.5V		1.4		V
HI-VG+	Gain Control Input Logic High	VCC3 = 4.5V, 5.5V	2.4	3.6	V	
LO-VG+	Gain Control Input Logic Low	VCC3 = 4.5V, 5.5V			0.8	V
I(vg)	Logic Input Currents	VCC3 = 4.5V, 5.5V			10	μA

AC Characteristics

V_{CC3} = 5V, $V_{CC1,2}$ = 12V, AFC_SWT = OFF, T_A = 0 to 70°C unless otherwise specified. Refer to Figure 2.

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
IF input						
Rin	AC Input imp. @ Max Gain	44MHz	1.5			KΩ
Rin	AC Input imp.@ minimum gain	44MHz	1.5			KΩ
Cin	Ac equivalent input cap			6		pF
NF	Noise Figure @ Max Gain	Rs = 75Ω, 44MHz		8.2	10	dB
Vins	Input Sensitivity @ Max Gain	44 MHz		1000		μVpp
IMD3	Inter-modulation Distortion for two-tone input	VCO=4x46.69, f1/f2=41.69/42.69MHz, Idat=0.7Vpp		-50	-45	dBC
Gain Control Characteristics						
Gmax	IF to baseband max Gain	Vin=-30dBmV@ 44MHz	57	60	63	dB
Ragc	AGC gain range	Vin-30 to +30 dBmV, Cagc=2V to 10V	40	46		dB
Sagc1	AGC sensitivity to gain control at maximum slope	V@ Cagc=8.5V to 9.5V DLYADJ=6V		15	22	dB/V
Sagc2	AGC sensitivity to gain control	V@ Cagc=3.5V to 4.5V DLYADJ=6V		3		dB/V
TPagc	Response time of AGC circuit	From GUP/GDN edge to CAGC current change			20	nS
NF0	Noise figure at no gain reduction	Cagc ≥ 10V, with SAW DLYADJ = 6V		10	12	dB
NF25	Noise figure at 25dB gain reduction	Cagc = 6V, with SAW DLYADJ = 6V			14	dB
NF40	Noise figure at 40dB gain reduction	Cagc = 3C, with SAW DLYADJ = 6V			30	dB
S/N	Signal-to-noise at min. gain	V = 1Vpp, 1MHz	45	47		dB

AC Characteristics

V_{CC3} = 5V, $V_{CC1,2}$ = 12V, AFC_SWT=OFF, T_A = 0 to 70°C unless otherwise specified

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
QMDD04 – Quadrature Demodulator						
LO	4 x Demodulating Freq.		100	186.76	250	MHz
BW_Mx	Mixer input bandwidth (+0.1dB)	Over 6MHz bands	30		60	MHz
BW_IFO	IF output from AGC into QDMD		30		60	MHz
DCG	Differential Conversion Gain			10.8		dB
Vo1dB	IMixer Vout @1dB compression	Diff Output, Δf=1MHz		1.5		Vpp
VoqdB	IMixer Vout @ 0.25 dB compression	Diff Output, Δf=1MHz		0.75		Vpp
ephase	I & Q phase error	On-chip	-2		2	deg
I-channel Filtering at Baseband						
APB	Pass Band Attn. @5.8MHz				0.5	dB
f-3dB	-3db Frequency		8.1			MHz
GF	Filter gain Diff In/Single Out			3.5		dB
A90	Attenuation @ IF+LO	see 14.1, (46.69+41.69)	50	54		dB
A46	Attenuation @ 46.69MHz	Vout=1.4Vpp @1MHz		5		mVpp
V_{O1DB}	Ida compression @2Vpp	Diff Output @ 1MHz,			1	dB
V_{OQDB}	Idat compression @0.75Vpp	Diff Output @ 1MHz			0.25	Vpp
FPLL Characteristics						
TSfc	VCO Long Term Stability	fc=186.76MHz,Vpll1=6	fc-500		fc+500	KHz
Svco	VCO sensitivity	fc=186.76MHz,Vpll1=6		400		KHz/V
dVafc±	AFC limiter input beat note	Pilot In = 46.69MHz, IMx±=88mVpp, Vco @ (46.69M±75K)		50		mVpp
DVafc±	AFC limiter input with Crystal ON i.e. AFC_SWT=ON	Xtal @ 46.69MHz Vco @ (46.69M±750K)		100		mVpp
fn	VCO phase noise	At ±20KHz offset			-105	dBC/Hz
BWpll	PLL Bandwidth			2.2		KHz
DIPDO	PLL Output Current Swing			±50		uA
Gpd	Phase Detector Gain	Imix± = 88mVpp, 1KHz PDO connected with 10K resistor to 5V.		4.5		uA/rad
TGpd	PD Gain temperature Coeff.			1000		ppm/K
edc	Static Phase Error due to Prescaler & DC offsets	With Offset Adjust	-4		4	deg
Auxiliary Section (see Figure 1)						
fXCL	Crystal Oscillator Freq	Series , 3rd Overtone		46.69056		MHz
TfXCL	Crystal Temperature Stability	See Figure 1		50		ppm/°C
TXon	Crystal Turn On Time	from AFC_SWT=HI (on)		100		ns
TXon	Crystal Turn OFF Time	frm AFC_SWT=LO (off)		100		ns

Preliminary Information

Applications Discussion

System Overview

The RC6516 is used in a Zenith Digital Cable Modem using multi-level VSB formats. The RC6516 performs IF amplification with gain control, synchronous demodulation of I and Q channels and carrier recovery using a Frequency and Phase Lock Loop. The I Channel analog output is digitized in an A/D converter at a rate of 10.76 MHz. The digital data is then used by the Digital Logic IC to perform segment sync recovery, signal polarity correction, symbol clock recovery, AGC and AFC control, channel equalization, phase error tracking, data de-interleaving, Reed Solomon error control and data slicing. (The block diagram of a typical receiver system using RC6516 is shown in Figure 1.

The RC6516 is between a SAW filter and an A/D. The RC6516 output is AC coupled to an 8 bit or 10 bit A/D. An FPLL circuit is used for carrier recovery and synchronous demodulation. A small pilot signal is present in the received signal to aid in carrier recovery. A microprocessor is used to tune the two local oscillators, initialize the system during start up and monitor system performance.

Figure 2 shows the typical external components and connections required for the operation of the RC6516.

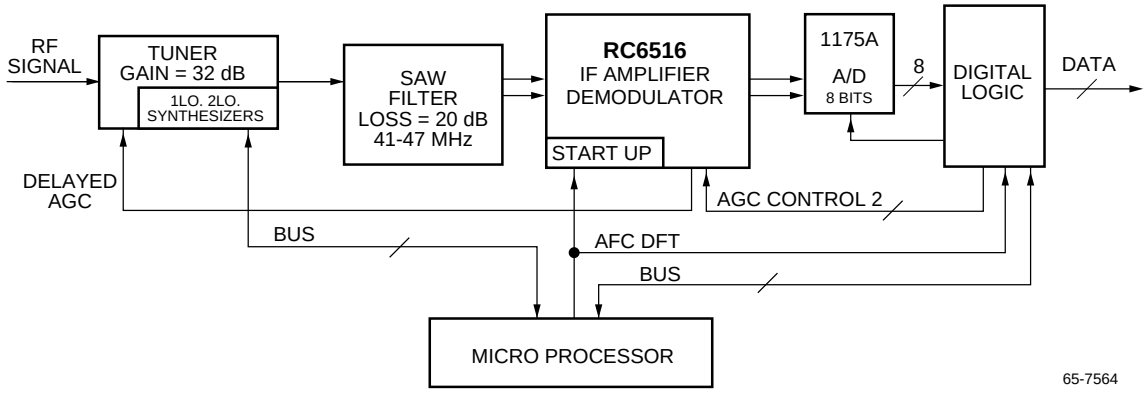


Figure 1. VSB Receiver Front End

Table 2. Signal Levels and Gain Distribution in Receiver Front-End

V_{CC3} = 15V, $V_{CC1,2}$ = 12V, T_A = 0 to 70°C unless otherwise specified.

Parameter	Max. Level	High Level	Mean Level	Low Level	Min Level	Unit
Tuner Input	-28.9	-21.3	-1.3	18.7	23.7	dBmV
Tuner Gain	34	34	33.5	21.4	19.1	dB
SAW Filter Gain (-Loss)	-18	-18	-18	-18	-18	dB
IF Input (Diff-in)	-12.9	-5.3	14.2	22.1	24.8	dBmV
LNA Gain	25.8	25.8	25.8	22.8	20.1	dB
VGA Gain	19.6	12.0	-7.5	-12.4	-12.4	dB
Mixer Input (Diff-in)	32.5	32.5	32.5	32.5	32.5	dBmV
Mixer Input rms	42.2	42.2	42.2	42.2	42.2	mVrms
Mixer Gain	10.9	10.9	10.9	10.9	10.9	dB
Max. Output (Diff-out)	148	148	148	148	148	mVrms
Filter Amp (Diff-in Sng-out) GAIN	3.6	3.6	3.6	3.6	3.6	dB
Iout+ Output (rms)	224	224	224	224	224	mVrms
Iout (peak-to-peak)	1	1	1	1	1	Vpp

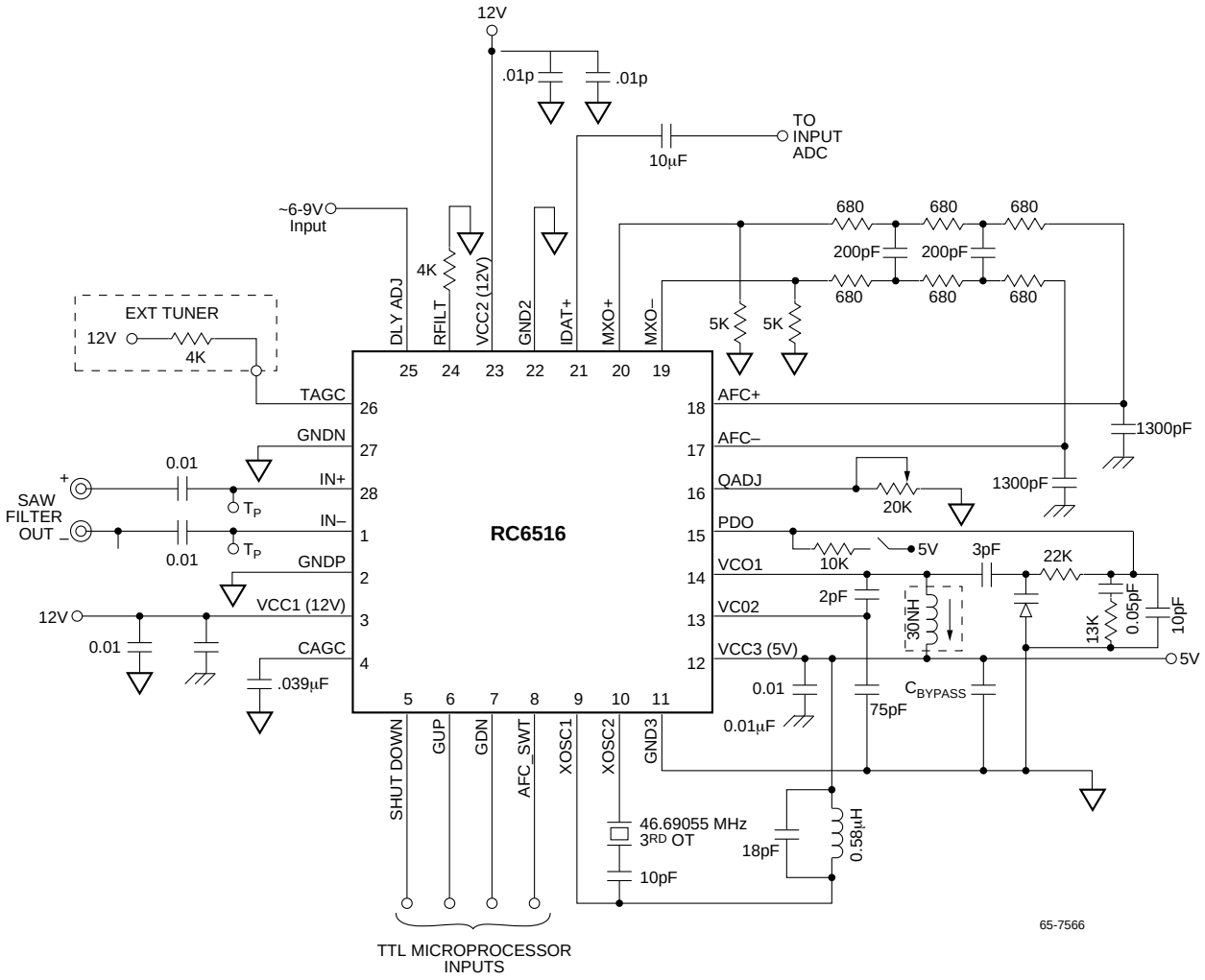
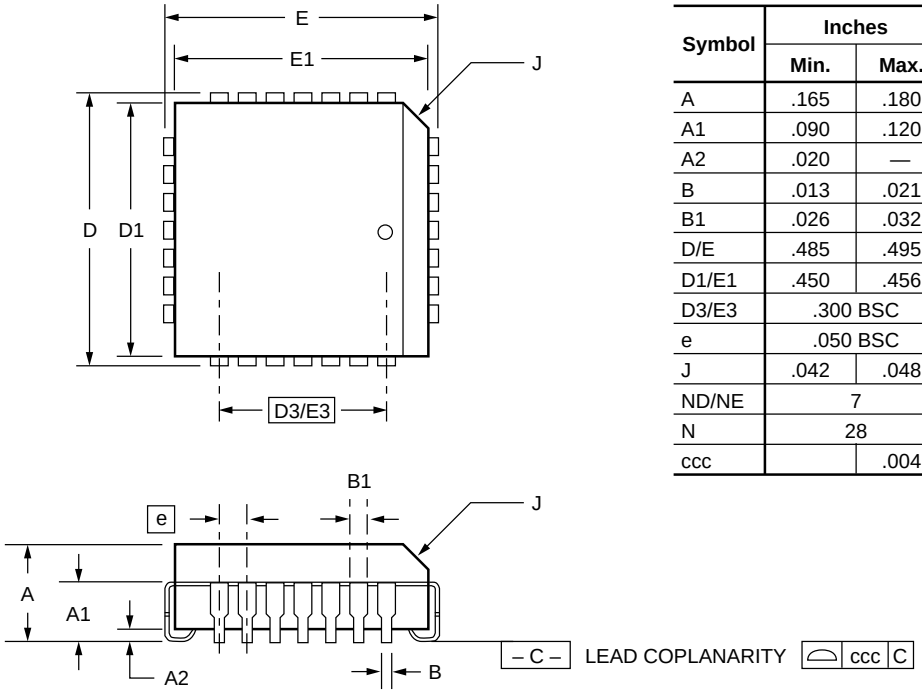


Figure 2. Typical External Components for RC6516

Preliminary Information

Notes:

Mechanical Dimensions – 28-Lead PLCC (QA) Package



Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.180	4.19	4.57	
A1	.090	.120	2.29	3.04	
A2	.020	—	.51	—	
B	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D/E	.485	.495	12.32	12.57	
D1/E1	.450	.456	11.43	11.58	
D3/E3	.300 BSC		7.62 BSC		
e	.050 BSC		1.27 BSC		
J	.042	.048	1.07	1.22	8
ND/NE	7		7		
N	28		28		
ccc		.004		0.10	

Notes:

1. Cavity mismatch = .004 (0.10mm)
2. Cavity frame offset = .002 (0.05mm) excluding leadframe tolerances.
3. Mold protrusions: Parting Line = .006 (0.15mm), Top or Bottom = .001 (0.025mm)
4. Variation in lead position = .005 (0.13mm)
5. Shoulder instrusions & protrusions: Intrusions = .002 (0.05mm), Protrusions = .003 (0.08mm)
6. Package warpage, WARP FACTOR = 2.5 = $\frac{\text{WARP (mils)}}{\text{PACKAGE LENGTH (inches)}}$
7. Ejector pin depth = .010 (0.25mm) maximum.
8. Corner and edge chamfer = 45°C.

Preliminary Information

Ordering Information

Product Number	Temperature Range	Screening	Packaging	Package Marking
RC6516	0° to 70°C	Commercial	28 Pin PLCC	RC6516V

Preliminary Information

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RC6564

IF-to-Digital™ Converter

Features

- Integrates almost all active components for conversion
- Simple interface to SAW filter and digital demodulator
- Gain control minimizes noise figure and distortion
- Tuner control feature interfaces with variety of tuners
- Demodulation of 64QAM constellations
- 40Msps ADC with >7.4 EFB @ 20Msps
- Low phase noise LO generation
- Crystal oscillator for fundamental or 3rd overtone mode
- 63dB peak conversion gain from IF to baseband
- 30dB minimum AGC range
- 45dB IMD3 end-to-end
- 9dB input noise figure at maximum gain
- On-chip stable voltage reference
- 44-pin PLCC package

Applications

- QAM receivers
- Set-top receivers for digital cable
- Internet surf-boards
- Cable modems
- ITV transceivers
- Desktop video conferencing
- IF sampling decoders

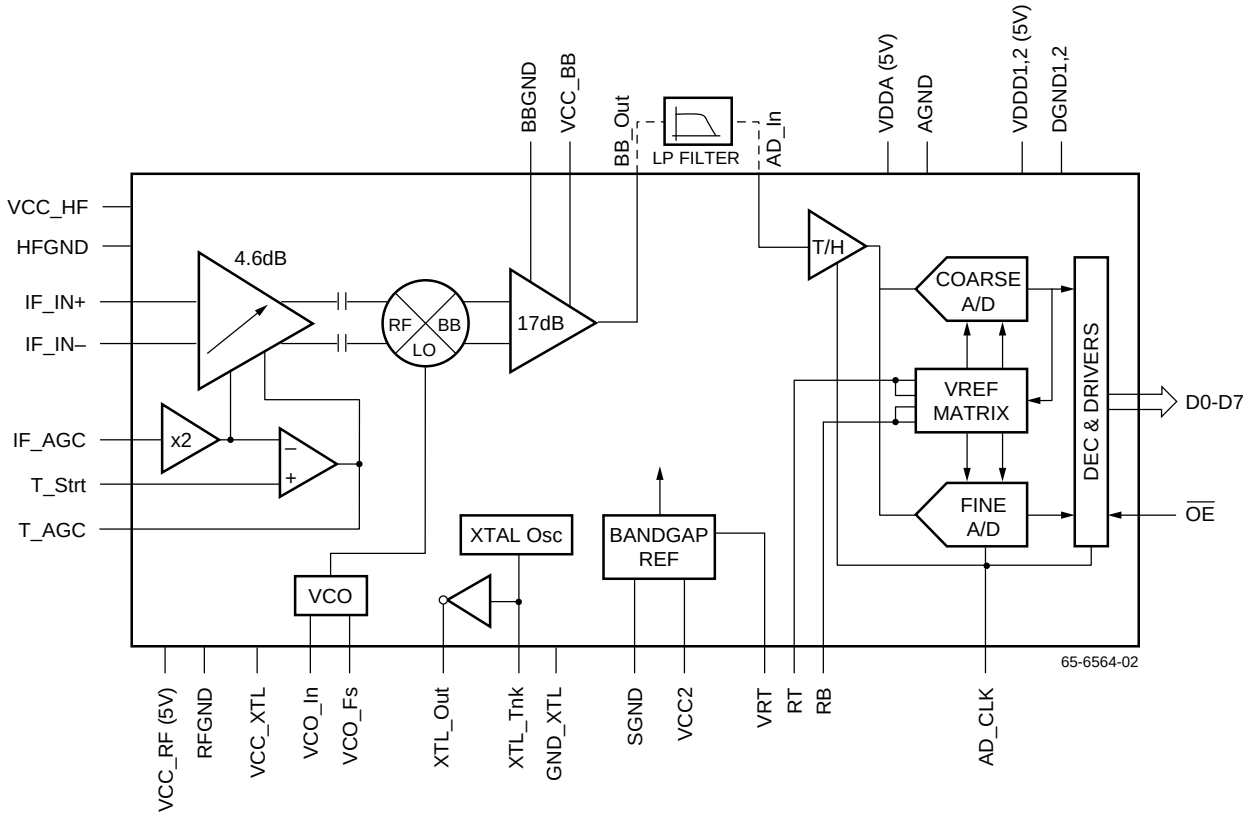
Preliminary Information

General Description

The RC6564 is a single chip solution for downconverting and digitizing QAM signals so that they can be decoded in the digital domain by custom DSP demodulators. The RC6564 performs IF amplification with gain control, frequency down conversion, frequency synthesis for mixer Local Oscillator (LO) & system clock generation, and baseband quantization with an Analog to Digital converter. The input can directly interface to a SAW filter and maintain low noise figure. Depending on the signal input level the gain may be controlled over a 30dB range through an external analog input signal. The gain reduction is done in two stages and orchestrated in such a manner as to minimize noise figure and signal distortion. The IF output is then down converted and filtered using a double balanced mixer. This output may be filtered even further, externally, before being quantized by the on-chip A/D converter.The digital data output can be processed to derive information for automatic gain control (AGC) and automatic frequency control (AFC). RC6564 is optimized to work with DSP decoders based on IF sampling. The RC6564 also provides an optimum tuner AGC control voltage useful for controlling the front-end tuner gain.

For best performance Analog sections work on 12V & 5V supplies. The digital sections work on a regulated 5V supply. RC6564 is available in a single 44-pin PLCC package.

Block Diagram



Functional Description

The RC6564 performs all the IF and baseband signal processing/conversion with the help of external filters. As shown in the Block Diagram, the RC6564 consists of three general sections:

1. IF Gain blocks with Gain Control
2. IF down conversion with LO & Clock Generation
3. Analog to Digital Conversion

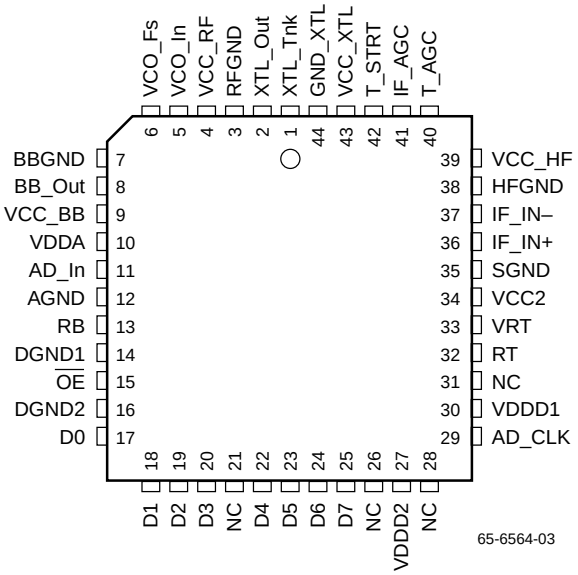
The IF Section: The signal input is into a variable gain amplifier capacitively coupled to the subsequent stages. When the voltage on IF_AGC pin is higher, the gain is higher and when it is lower the gain is lower too. To minimize the noise figure degradation with gain reduction the gains in various stages are not reduced simultaneously. The transition point is set by the voltage on T_Strt pin. When the IF_AGC voltage is higher than half the T_Strt voltage the gain reduction rate is steepest. When the IF_AGC voltage is lower than roughly half the T_Strt voltage the gain reduction is at a slower rate. The T_AGC output voltage also changes and can be used to gain reduce the front-end tuner. The gain control amplifier has stabilized gain over temperature and supply variations.

IF Down Conversion & Frequency Synthesis: This section consists of a double balanced linear mixer. The output of the front-end gain stage is capacitively coupled to the input (RF port) of the mixer. The mixer output is further amplified. The signals for the Local Oscillator (LO) port of the mixer can be directly driven or synthesized through the VCO (Voltage Controlled Oscillator). The mixer output is partially filtered on-chip but may need to be further filtered externally before being fed to the A/D input. The RC6564 also has a crystal oscillator circuit that can be used for generating a master clock for frequency synthesis.

Analog-to-Digital Converter: The analog-to-digital converter employs a two-step 9-bit architecture to convert analog signals into digital words at sample rates up to 40 Msps (Mega samples per second). An integral Track/Hold circuit delivers excellent performance on signals with full-scale components up to 12MHz. A dynamic performance of more than 7.4 effective bits is delivered at the outputs D0 through D7. The A/D digital outputs are three-state and TTL/CMOS compatible. The down converted output at BB_OUT can be externally filtered and directly connected to the A/D input. Sampling of the applied input signals takes place on the falling edge of the AD_CLK. The output word is delayed by 2.5 AD_CLK cycles. An output enable control $\overline{OE}$ places the outputs in high impedance state when HIGH. The outputs are enabled when $\overline{OE}$ is LOW as described in the Timing Diagrams section.

Preliminary Information

Pin Assignments



Pin Descriptions

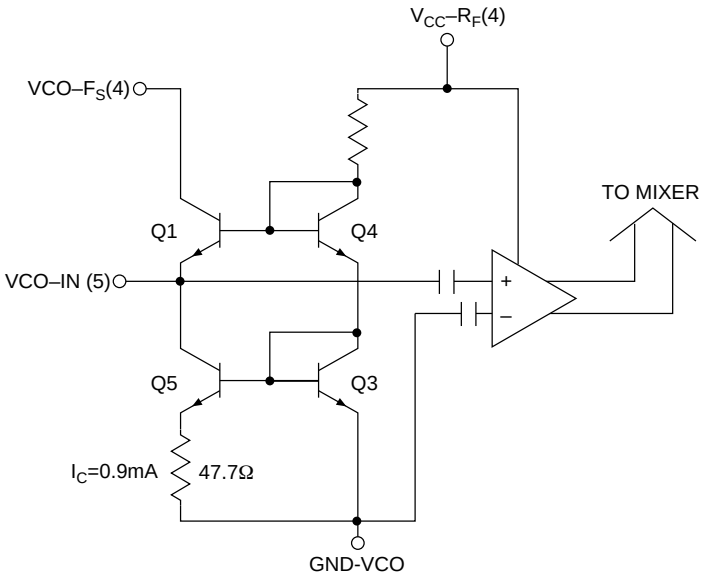
Pin Name	Pin Number	Pin Function Description
AD_CLK	29	Clock input for A/D converter. AD_In sampled on the falling edge.
AGND	12	Analog Ground Connection
AD_In	11	Analog Input to the A/D Converter section.
BBGND	7	Ground Connection
BB_Out	8	Base-band Voltage Output
D0-D3	17, 18, 19, 20	Output Lower Significant Bits. Valid data on rising edge of AD_CLK.
D4-D7	22, 23, 24, 25	Output Upper Significant Bits. Valid data on rising edge of AD_CLK.
DGND1	14	Ground Connection.
DGND2	16	Ground Connection
GND_XTL	44	Crystal Oscillator Ground
HFGND	38	Analog Ground Connection
IF_AGC	41	Input Voltage for IF front end gain control
IF_IN+, IF_IN–	36, 37	IF inputs.
N/C	21, 26, 28, 31	No Connection
$\overline{OE}$	15	Input for enabling digital outputs. When LOW, D0-D7 are enabled. When HIGH D0-D7 are in high impedance state.
RB	13	Input Reference Voltage for A/D Conversion
RFGND	3	Ground Connection for High Frequency Mixed Signal Sections
RT	32	Input Reference Voltage for A/D Conversion Range Top (see also RB, pin #13)
SGND	35	Analog Ground Connection
T_AGC	40	Output Voltage for Tuner Gain Control
T_STRT	42	Threshold Voltage Input for Starting Tuner Gain Control
VCC_BB	9	Baseband Supply Voltage, typically 12V

Preliminary Information

Pin Descriptions (continued)

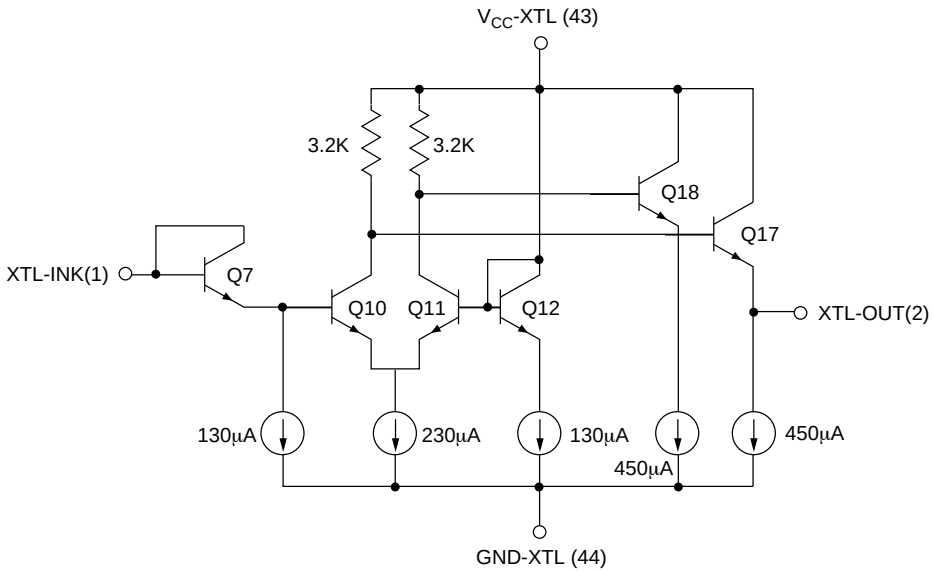
Pin Name	Pin Number	Pin Function Description
VCC2	34	Analog Supply Voltage (12V)
VCC_HF	39	Analog Supply Voltage (12V)
VCC_RF	4	Supply Voltage (5V) for High Frequency Mixed Signal Sections
VCC_XTL	43	Supply voltage for Crystal Oscillator
VCO_Fs	6	VCO External Frequency Select Circuit Connection
VCO_In	5	VCO Input. Can be used for directly feeding external LO.
VDDD1	30	+5V Digital supply
VDDD2	27	+5V Digital supply
VDDA	10	+5V power supply voltage
VRT	33	Output reference voltage for top of A/D input range
XTL_Out	2	Crystal Oscillator Output
XTL_Tnk	1	Crystal Oscillator Frequency Select Circuit Connection

VCO Internal Schematic



The VCO is designed as a Colpitts oscillator. The frequency is controlled by the external resonance circuit. The oscillating transistor is Q1 in common base configuration. In case it is necessary to inject the signal in place of LO in the mixer pin VCO_Fs is recommended to be open and the injected signal on pin VCO_In to be under 100mVpp.

Crystal Oscillator Internal Schematic



The crystal oscillator is an ECL inverter. In order to function correctly it needs to bias the XTL-Tnk with a choke to 5V VCC_XTL power supply. The output is about 0.7V DC lower than VCC_XTL with an approximate swing of 0.5Vpp at the output. If the oscillator is note used, it is necessary to ground XTL_Tnk with a decoupling capacitor. This minimizes the high frequency parasitic oscillations at the XTL_Out.

Logic Feedthrough

The Logic Feedthrough in the IF section can be minimized by taking the following precautions:

1. The digital ground of ADC should be separate from analog ground of IF section.
2. All logic circuits in the neighborhood of RC6564 must be decoupled with a T-filter (choke and capacitors). This will minimize the noize radiated from the logic circuits.
3. All logic lines from the ADC must be surrounded be a good ground plane.

Absolute Maximum Ratings (beyond which the device may be damaged)[1]

Parameter		Conditions	Min	Typ	Max	Units
IF_IN+, IF_IN–, IF_AGC, T_Strt	Input Voltages		Gnd–0.3		V_{CC}+0.3	V
AD_IN	A/D input voltage		AGND		VDDA	V
VCC_{RF}, VCC_{BB}, VCC_{HF}, VCC_2	Analog Supply Voltages				13.5	V
VDDA, VDDD 1,2	Digital Supply Voltages				7	V

Note:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

Preliminary Information

Operating Conditions

Parameter		Conditions	Min	Typ	Max	Units
V_{CC}	Analog Supply Voltage		10.8	12	13.2	V
Vcc3	HF Supply Voltage		4.5	5	5.5	V
VDDA,D	Digital Supply Voltages		4.75	5	5.25	V
T	Temperature		0		70	°C
RT	A/D Top Reference Voltage		1	2.5		V
RB	A/D Bottom ref. Voltage			0	0.7	V
VIN	Analog input to A/D		RB		RT	V
VIH	Digital Inputs – Logic HIGH		0.7VDDD		VDDD	V
VIL	Digital Input – Logic LO		GND		0.3VDDD	V
θJA	Thermal Coefficient Junction to Ambient			43		°C/W
θJC	Thermal Coefficient Junction to Case			16		°C/W

DC Electrical Characteristics

V_{CCRF}, VCC_XTL = 5V; V_{CCHF}, VCC_BB, VCC2 = 12V; T_A = 0 to 70°C, unless otherwise specified.

Parameter		Conditions	Min	Typ	Max	Units
PWIF	Power Consumption in IF			0.6	0.74	W
PWAD	Power Consumption in ADC	ADCLK = 20 Msps		0.1	0.16	W
ICCDD	Digital Supply Current	5V, 20Msps		20	30	mA
ICCHF	Front End Supply Current	12V supply		27	35	mA
ICCBB	Back and Baseband Current	12V supply		16	25	mA
ICCRF	RF Supply Current	5V supply		6	10	mA
VRT	Reference Output Voltage			2.0		V
ΔVBBo	Base-band DC output swing		6			Vpp
Tagc_hi	Tuner AGC for max gain	IF_AGC=5V		7.5		V
Tagc_lo	Tuner AGC for min gain	IF_AGC=2V		2.3		V
RAD_IN	A/D input impedance		500	1000		KΩ
VOH	Output Voltage, HIGH, D0-D7	Ioh= 2.5mA	3.5			V
VOL	Output Voltage, LOW, D0-D7	Iol=4mA			0.4	V
IOZ	Hi-Z Output leakage	Max Ref. Current Output			±5	μA

AC Electrical Characteristics

V_{CCRF} = 5V; V_{CCHF}, VCC_BB = 12V; IF_AGC = 2V; AD_CLK = 20Msps; Tstrt = 5V;
T_A = 0 to 70°C, unless otherwise specified.

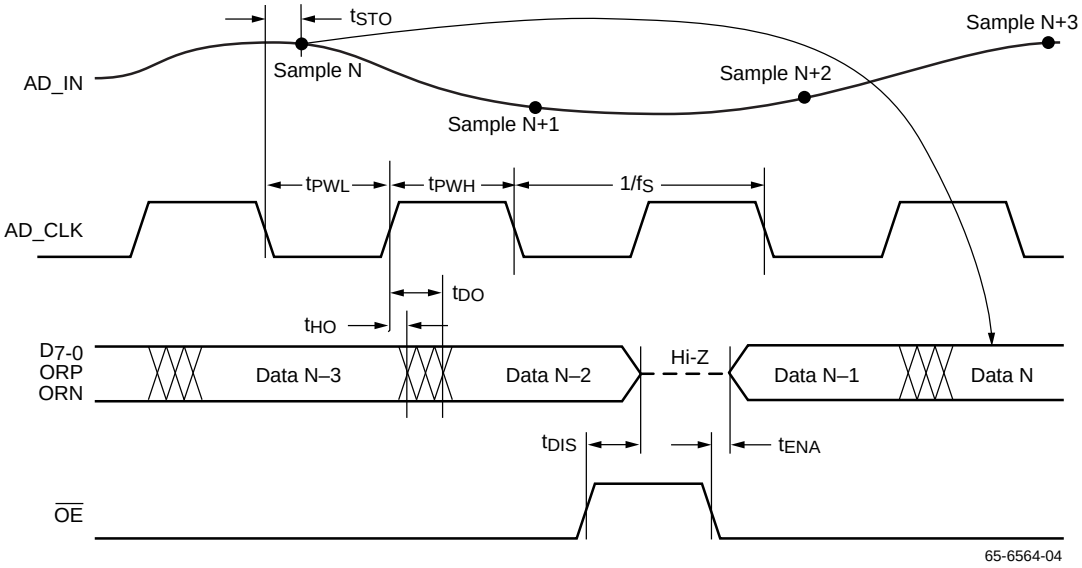
Parameter		Conditions	Min	Typ	Max	Units
ZIFin	AC Input Impedance	@43.75MHz	2			K Ω
CIFin	AC equivalent input cap	IF_IN±		6		pF
NFmx	Noise Figure at Max gain			9	12	dB
Vis	Input sensitivity at max gain	Vagc = 2.5V		250		μV
IMD3	Two tone Intermod	f1/f2=43.75 /42.75 Mhz, IF_IN= -16dBm, VCO_IN = 0.1Vpp, LO=38.75MHz, VBBo=1.35Vpp, Note 1		45		dB
G	IF to baseband Max gain	Vin=-46dBm @ 44MHz	35	40		dB
Ragc	AGC Gain range	IF_AGC=0.8V–2.5V	30	35		dB
Sagc	AGC Sensitivity Average Slope	T_Strt=5V, IF_AGC=0.8V–2.5V		13		dB/V
BW_IF	IF Bandwidth	0.1dB for 10MHz bands 0.1dB for 5MHz bands	30 30	43.75	75 80	MHz
fLO	Down conversion Freq.	VCO_IN = 0.1Vpp			100	MHz
ϕnLO	VCO Phase Noise	@ ±10KHz offset			-100	dBC/Hz
ϕnXTL	XTAL OSC Phase Noise	@ ±10KHz offset			-100	dBC/Hz
CAD	ADC input capacitance			4		pF
Eli	Integral Linearity Error			±0.5	±0.75	LSB
Eld	Differential Linearity Error			±0.3	±0.5	LSB
BW	A/D sine wave Bandwidth				12	MHz
Eap	Aperture Error			30		pS
SNR	Signal-to-Noise ratio	AD_CLK = 20MSPS, AD_IN = 5MHz		45		dB
SFDR	Spurious-Free Dynamic Range	AD_CLK = 20MSPS, AD_IN = 5MHz		45		dB
tHO	Output Hold time	Cload = 15pF	5			nS
tDo	Output Delay time	Cload = 15pF			20	nS
tsto	Sampling time offset		2	5	8	nS

Notes:

1. With the application of antialiasing filter as load.

Preliminary Information

Analog to Digital Conversion Timing Diagram



Typical Performance Characteristics

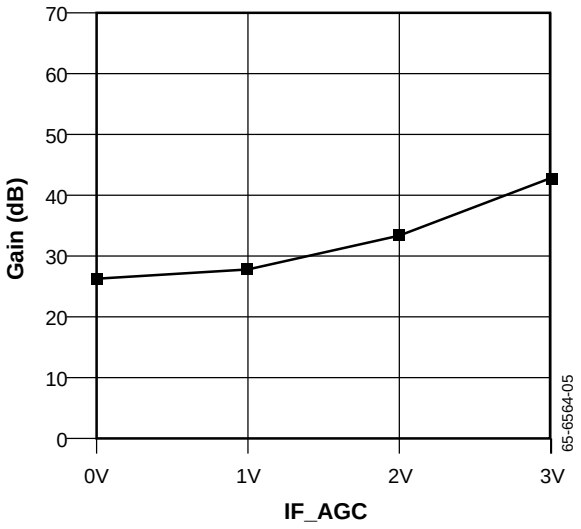


Figure 1. Typical IF AGC Control Characteristics

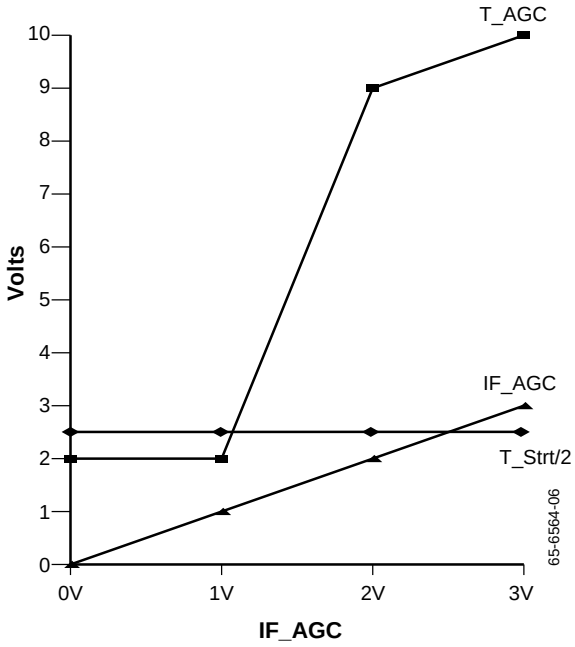


Figure 2. Typical Tuner AGC Control Characteristics

Typical Performance Characteristics (Continued)

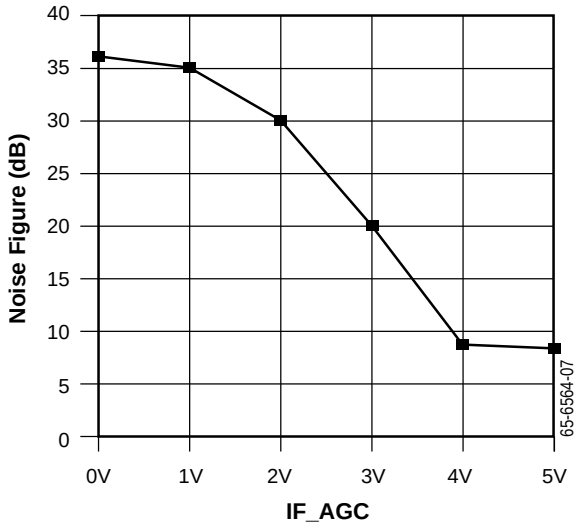


Figure 3. Noise Figure over Gain Control Range

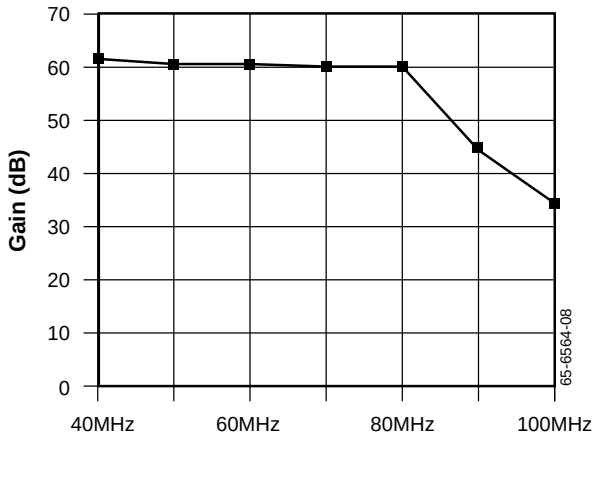


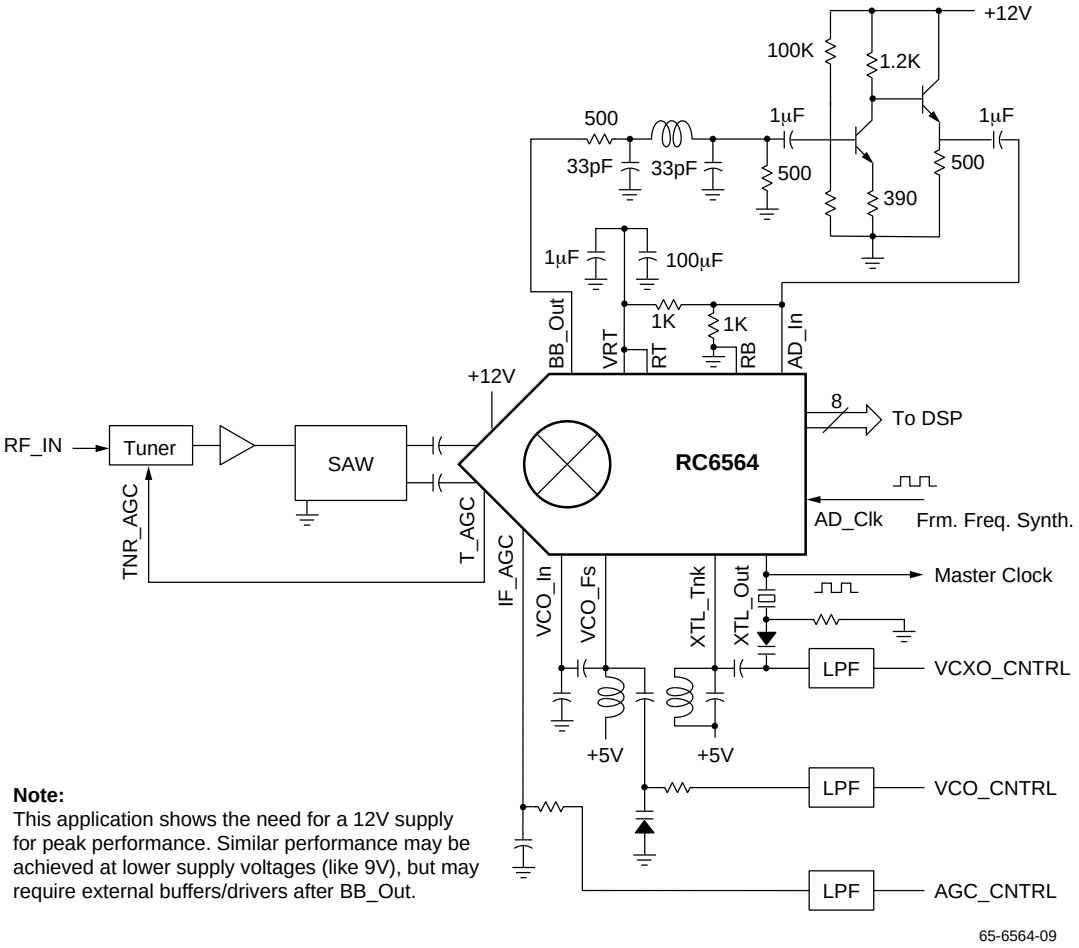
Figure 4. IF Input Bandwidth

Applications

The RC6564 is specially suited for use in set-top boxes and cable modems for decoding QAM modulated signals based on IF sampling techniques. The RC6564 simplifies the front-end design and makes it more cost effective by integrating in a single chip the IF-to-Digital functionality. The other major components required for the front-end of the modem are the tuner, a SAW filter and the appropriate DSP demodulator/ decoder.

Modem Applications

Figure 5 below shows the application of RC6564 in IF band-pass sampling decoding for cable access. Here, the master clock for the Digital Demodulator can be generated using the crystal oscillator that is configured as a VCXO. The mixer down conversion clock can also be pulled in using the varac-tor control circuitry shown below. The on-chip VCO provides low-phase noise characteristics. The VCO and VCXO oscillator frequencies can be pulled by the voltage control on VCO_CNTRL and VCXO_CNTRL lines respec-tively. The sampling clock for the A/D conversion can be derived from the master clock through external frequency synthesis. The full scale reference signal for A/D is conve-niently derived from the VRT output. The baseband output is referenced such that the filtered output is automatically in the mid-scale of the A/D input. The filtered output can be a.c. coupled to the AD_In. In the application below an external low-pass filter is used to bandlimit the signals before conver-sion. The gain is adjusted by the average voltage on the IF_AGC line to keep the signal in the optimum range of the A/D input. The T_AGC output is used to control the tuner gain when the input levels into the RC6564 are too high.



Note:
This application shows the need for a 12V supply for peak performance. Similar performance may be achieved at lower supply voltages (like 9V), but may require external buffers/drivers after BB_Out.

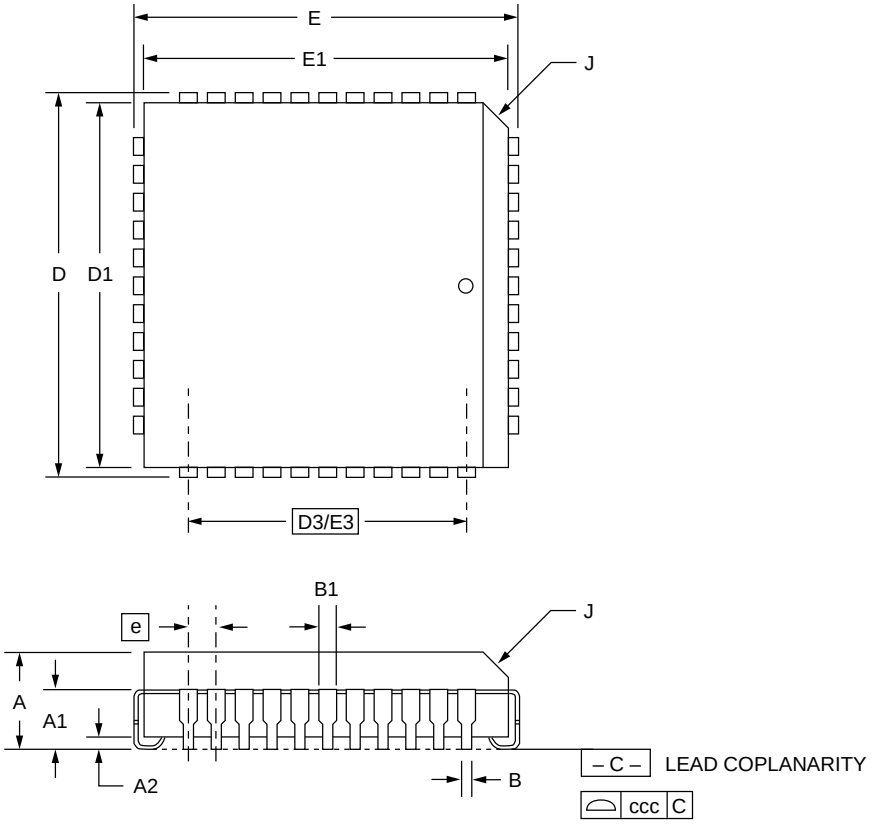
Figure 5. Application of RC6564 in Cable Modem Receivers

Mechanical Dimensions – 44-Lead PLCC (QB) Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.180	4.19	4.57	
A1	.090	.120	2.29	3.05	
A2	.020	—	.51	—	
B	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D/E	.685	.695	17.40	17.65	
D1/E1	.650	.656	16.51	16.66	3
D3/E3	.500 BSC		12.7 BSC		
e	.050 BSC		1.27 BSC		
J	.042	.056	1.07	1.42	2
ND/NE	11		11		
N	44		44		
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982
2. Corner and edge chamfer (J) = 45°
3. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is .101" (.25mm)



Preliminary Information

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
RC6564V	0 °C – 70 °C	Commercial	44-Lead PLCC	RC6564V

Preliminary Information

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RC6564A

IF-to-Digital™ Converter

Features

- Integrated IF-to-Digital™ conversion
- IF bandwidth from 30 to 80MHz
- 40MHz 8 bit ADC
- Operating range between 8.5V to 13.2V
- Demodulation of 64QAM constellations
- Simple interface to SAW filter and digital demodulator
- Tuner control feature interfaces with variety of tuners
- Low phase noise LO generation
- Crystal oscillator for fundamental or 3rd overtone mode
- 63dB peak conversion gain from IF to baseband
- 30dB minimum AGC range
- 45dB IMD3 end-to-end
- On-chip 2V stable voltage reference
- 44-pin PLCC package

Applications

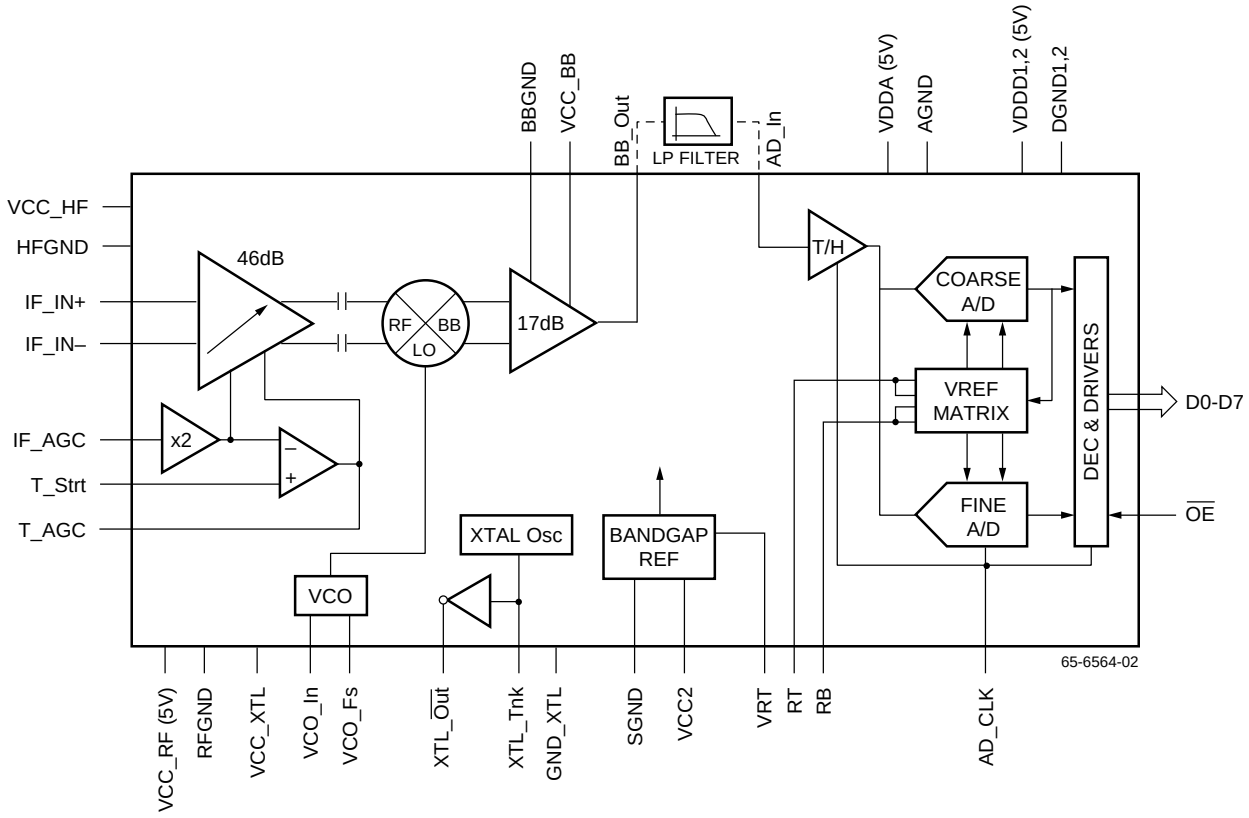
- QAM receivers
- Set-top receivers for digital cable
- Internet surf-boards
- Cable modems
- Desktop video conferencing
- IF sampling decoders

General Description

The RC6564A is a single chip solution for downconverting and digitizing QAM signals that can be decoded in the digital domain by custom DSP demodulators. The RC6564A performs IF amplification with gain control, frequency down conversion, frequency synthesis for mixer Local Oscillator (LO) and system clock generation, and baseband quantization with an Analog to Digital converter. The input can directly interface to a SAW filter and maintain low noise figure. Depending on the signal input level the gain may be controlled over a 30dB range through an external analog input signal. The gain reduction is done in two stages and orchestrated in such a manner as to minimize noise figure and signal distortion. The IF output is then down converted and filtered using a double balanced mixer. This output can be filtered even further, externally, before being quantized by the on-chip A/D converter.The digital data output can be processed to derive information for automatic gain control (AGC) and automatic frequency control (AFC). RC6564A is optimized to work with DSP decoders based on IF sampling. The RC6564A also provides an optimum tuner AGC control voltage useful for controlling the front-end tuner gain.

The IF and mixer section works at 9V. The oscillator works on 5V supply. The A/D converter has one analog 5V supply and two digital 5V supplies. The RC6564A is available in a 44 pin PLCC package.

Block Diagram



Functional Description

The RC6564A performs all the IF and baseband signal processing/conversion with minimal external components. As shown in the Block Diagram, the RC6564A consists of three general sections:

1. IF Gain blocks with Gain Control
2. IF down conversion with LO & Clock Generation
3. Analog to Digital Conversion

The IF Section

The signal input is fed into a variable gain amplifier capacitively coupled to the subsequent stages. The gain is directly proportional to IF_AGC voltage. To minimize the noise figure degradation with gain reduction the gains in various stages are not reduced simultaneously. The transition point is set by the voltage on T_Strt pin. T_Strt sets the T_AGC trigger to control the front tuner gain.

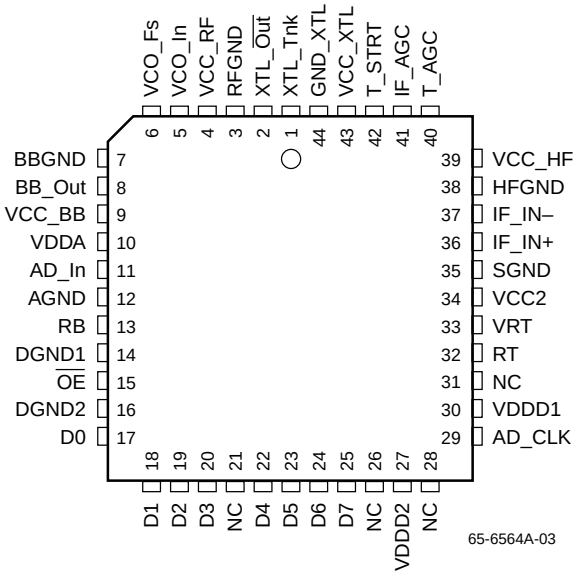
IF Down Conversion & Frequency Synthesis

This section consists of a double balanced linear mixer. The output of the front-end gain stage is capacitively coupled to the input (RF port) of the mixer. The mixer output is further amplified. The signals for the Local Oscillator (LO) port of the mixer can be directly driven or synthesized through the VCO (Voltage Controlled Oscillator). The mixer output is partially filtered on-chip but may need to be further filtered externally before being fed to the A/D input. The RC6564A also has a crystal oscillator circuit that can be used for generating a master clock for frequency synthesis.

Analog-to-Digital Converter

The analog-to-digital converter employs a two-step 9-bit architecture to convert analog signals into digital words at sample rates up to 40 Msps (Mega samples per second). An integral Track/Hold circuit delivers excellent performance on signals with full-scale components up to 12MHz. A dynamic performance of more than 7.4 effective bits is delivered at the outputs D0 through D7. The A/D digital outputs are three-state and TTL/CMOS compatible. The down converted output at BB_OUT can be externally filtered and directly connected to the A/D input. Sampling of the applied input signals takes place on the falling edge of the AD_CLK. The output word is delayed by 2.5 AD_CLK cycles. An output enable control $\overline{OE}$ places the outputs in high impedance state when HIGH. The outputs are enabled when $\overline{OE}$ is LOW as described in the Timing Diagrams section.

Pin Assignments



Pin Descriptions

Pin Name	Pin Number	Pin Function Description
AD_CLK	29	Clock Input for A/D Converter. AD_In sampled on the falling edge.
AGND	12	Analog Ground Connection for A/D.
AD_In	11	Analog Input to the A/D Converter Section.
BBGND	7	Ground Connection for IF.
BB_Out	8	Base-band Voltage Output.
D0-D3	17, 18, 19, 20	Output Lower Significant Bits. Valid data on rising edge of AD_CLK.
D4-D7	22, 23, 24, 25	Output Upper Significant Bits. Valid data on rising edge of AD_CLK.
DGND1	14	Ground Connection for A/D.
DGND2	16	Ground Connection for A/D.
GND_XTL	44	Crystal Oscillator Ground for IF.
HFGND	38	Analog Ground Connection for IF.
IF_AGC	41	Input Voltage for IF Front End Gain Control
IF_IN+, IF_IN–	36, 37	IF Inputs.
N/C	21, 26, 28, 31	No Connection
$\overline{OE}$	15	Input for Enabling Digital Outputs. When LOW, D0-D7 are enabled. When HIGH D0-D7 are in high impedance state.
RB	13	Bottom Input Reference for A/D.
RFGND	3	Ground Connection for High Frequency Mixed Signal Sections for IF.
RT	32	Top Input Reference Voltage for A/D.
SGND	35	Analog Ground Connection for IF.
T_AGC	40	Output Voltage for Tuner Gain Control.
T_STRT	42	Threshold Voltage Input for Starting Tuner Gain Control.
VCC_BB	9	Baseband Supply Voltage. Typically 9V for IF.

Pin Descriptions (continued)

Pin Name	Pin Number	Pin Function Description
VCC2	34	Analog Supply Voltage (9V) for IF.
VCC_HF	39	Analog Supply Voltage (9V) for IF.
VCC_RF	4	Supply Voltage (5V) for High Frequency Mixed Signal Sections for IF.
VCC_XTL	43	Supply voltage for Crystal Oscillator for IF.
VCO_Fs	6	VCO External Frequency Select Circuit Connection.
VCO_In	5	VCO Input. Can be used for directly feeding external LOW.
VDDD1	30	+5V Digital Supply for A/D.
VDDD2	27	+5V Digital Supply for A/D.
VDDA	10	+5V Power Supply Voltage for A/D.
VRT	33	Output Reference Voltage from IF for Top of A/D Input Range.
XTL_$\overline{\text{Out}}$	2	Crystal Oscillator Output (inverted).
XTL_Tnk	1	Crystal Oscillator Frequency Select Circuit Connection.

Absolute Maximum Ratings (beyond which the device may be damaged)[1]

Parameter		Conditions	Min	Typ	Max	Units
IF_IN+, IF_IN–, IF_AGC, T_Strt	Input Voltages		Gnd–0.3		V_{CC}+0.3	V
AD_IN	A/D input voltage		AGND		VDDA	V
VCC_RF, VCC_BB, VCC_HF, VCC2, VCC_XTL	Analog Supply Voltages				13.5	V
VDDA, VDDD 1,2	Digital Supply Voltages				7	V
Tstg	Storage Temperature		-40		125	°C

Note:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter		Min	Typ	Max	Units
V_{CC}	Analog Supply Voltage	8.5	9	13.2	V
VCC_RF, VCC_XTL	Supply Voltage for IF and Mixer, Supply Voltage for XTLOSC and VCO	4.75	5	5.25	V
VDDA,D	Digital Supply Voltages	4.75	5	5.25	V
T	Temperature	0		70	°C
RT	A/D Top Reference Voltage	1	2.5		V
RB	A/D Bottom Reference Voltage		0	0.7	V
VIN	Analog Input to A/D	RB		RT	V
VIH	Digital Inputs – Logic HIGH	0.7VDDD		VDDD	V
VIL	Digital Input – Logic LOW	GND		0.3VDDD	V
θJA	Thermal Coefficient Junction to Ambient		43		°C/W
θJC	Thermal Coefficient Junction to Case		16		°C/W

DC Electrical Characteristics

V_{CCRF}, VCC_XTL = 5V; V_{CCHF}, VCC_BB, VCC2 = 9V; T_A = 0 to 70°C, unless otherwise specified.

Parameter		Conditions	Min	Typ	Max	Units
PWIF	Power Consumption in IF			0.4	0.5	W
PWAD	Power Consumption in ADC	ADCLK = 20 Msps		0.1	0.16	W
ICCDD	Digital Supply Current	5V, 20Msps		20	30	mA
ICCHF	Front End Supply Current	9V Supply		20	25	mA
		12V Supply		27	35	
ICCBB	Back and Baseband Current	9V Supply		21	25	mA
ICCRF	RF Supply Current	5V Supply		6	10	mA
VRT	Reference Output Voltage		1.95	2.05	2.15	V
ΔVBBo	Base-band DC Output Swing		3.5			Vpp
Tagc_hi	Tuner AGC for Maximum Gain	IF_AGC = 5V		7.5		V
Tagc_lo	Tuner AGC for Minimum Gain	IF_AGC = 2V		2		V
RAD_IN	A/D Input Impedance		500	1000		KΩ
VOH	Output Voltage, HIGH, D0-D7	Ioh = 2.5mA	3.5			V
VOL	Output Voltage, LOW, D0-D7	Iol = 4mA			0.4	V
IOZ	Hi-Z Output Leakage	Maximum Reference Current Output			±5	μA

AC Electrical Characteristics

VCC_XTL, VCC_RF = 5V; VCC_HF, VCC_BB = 9V; IF_AGC = 2V; AD_CLK = 20Msps; Tstrt = 5V; T_A = 0 to 70°C, unless otherwise specified.

Parameter		Conditions	Min	Typ	Max	Units
ZIFin	AC Input Impedance	@43.75MHz	2			K Ω
CIFin	AC Equivalent Input Cap	IF_IN±		6		pF
Vis	Input Sensitivity at Maximum Gain			250		μV
IMD3	Two Tone Intermod	f1/f2 = 43.75 /42.75 Mhz, IF_IN= -16dBm, VCO_IN = 0.1Vpp, LO = 38.75MHz, See Note 1		45		dB
G	IF to Baseband Gain	IF_AGC = 2V	35	40		dB
NF	Noise Figure (Maximum Gain)			9		dB
Ragc	AGC Gain Control Range	IF_AGC = 0.8V–4V	30	35		dB
Sagc	AGC Sensitivity Average Slope	T_Strt = 5V, IF_AGC = 0.8V–4V		10		dB/V
BW_IF	IF Bandwidth	0.1dB for 10MHz Bands 0.1dB for 5MHz Bands	30 30	43.75	75 80	MHz
fLO	Down Conversion Frequency	VCO_IN = 0.1Vpp			100	MHz
ϕnLO	VCO Phase Noise	@ ±10KHz Offset			-100	dBC/Hz
ϕnXTL	XTAL OSC Phase Noise	@ ±10KHz Offset			-100	dBC/Hz
CAD	ADC Input Capacitance			4		pF
Eli	Integral Linearity Error			±0.5	±0.75	LSB
Eld	Differential Linearity Error			±0.3	±0.5	LSB

AC Electrical Characteristics (continued)

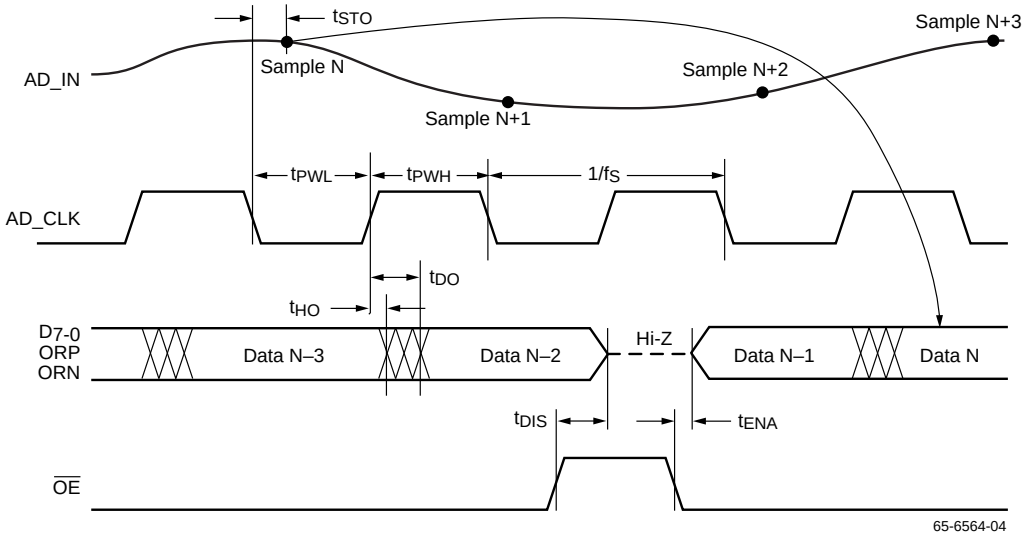
VCC_XTL, VCC_RF = 5V; VCC_HF, VCC_BB = 9V; IF_AGC = 2V; AD_CLK = 20Msps; Tstrt = 5V;
T_A = 0 to 70°C, unless otherwise specified.

Parameter		Conditions	Min	Typ	Max	Units
BW	A/D sine wave Bandwidth				12	MHz
Eap	Aperture Error			30		pS
SNR	Signal-to-Noise ratio	AD_CLK = 20MSPS, AD_IN = 5MHz		45		dB
tHO	Output Hold time	Cload = 15pF	5			nS
tDO	Output Delay time	Cload = 15pF			20	nS
tSTO	Sampling time offset		2	5	8	nS

Notes:

1. With the application of antialiasing filter as load and 2Vpp at A/D input.

Analog to Digital Conversion Timing Diagram



Typical Performance Characteristics

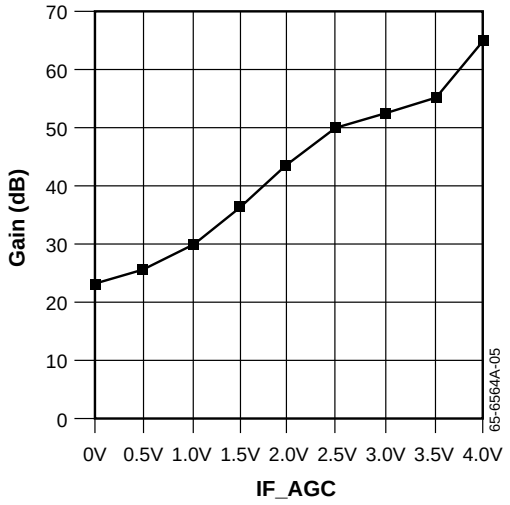


Figure 1. Typical IF AGC Control Characteristics

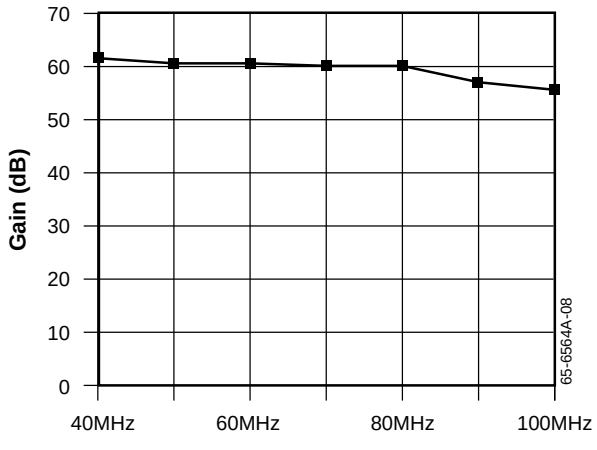


Figure 2. IF Input Bandwidth

Typical Performance Characteristics (Continued)

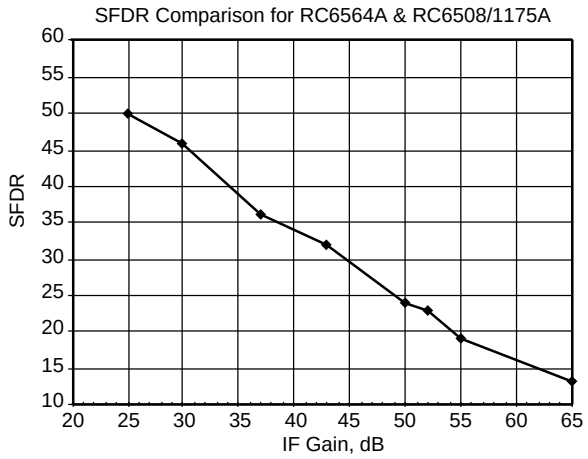
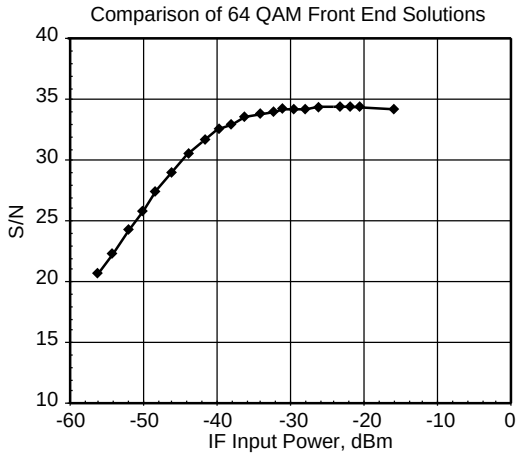


Figure 3. SFDR vs RC6564A (Fairchild Semiconductor Demo Board with 64 QAM demodulator)



S/N vs. IF Input Power RC6564 (Fairchild Semiconductor Demo Board with 64 QAM demodulator)

Applications

The RC6564A is specially suited for use in set-top boxes and cable modems for decoding QAM modulated signals based on IF sampling techniques. The RC6564A simplifies the front-end design and makes it more cost effective by integrating in a single chip the IF-to-Digital functionality. The other major components required for the front-end of the modem are the tuner, a SAW filter and the appropriate DSP demodulator/decoder.

Modem Applications

Figure 4 below shows the application of RC6564A in IF bandpass sampling decoding for cable access. The on-chip VCO provides low-phase noise characteristics. The VCO can be pulled by the voltage control on VCO_CNTRL. The sampling clock for the A/D conversion can be derived from the master clock through external frequency synthesis. The full scale reference signal for A/D is conveniently derived from the VRT output. The baseband output is referenced such that the filtered output is automatically in the mid-scale of the A/D input. The filtered output can be a.c. coupled to the AD_In. In the application below an external low-pass filter is used to bandlimit the signals before conversion. The gain is adjusted by the average voltage on the IF_AGC line to keep the signal in the optimum range of the A/D input. The T_AGC output is used to control the tuner gain when the input levels into the RC6564A are too high.

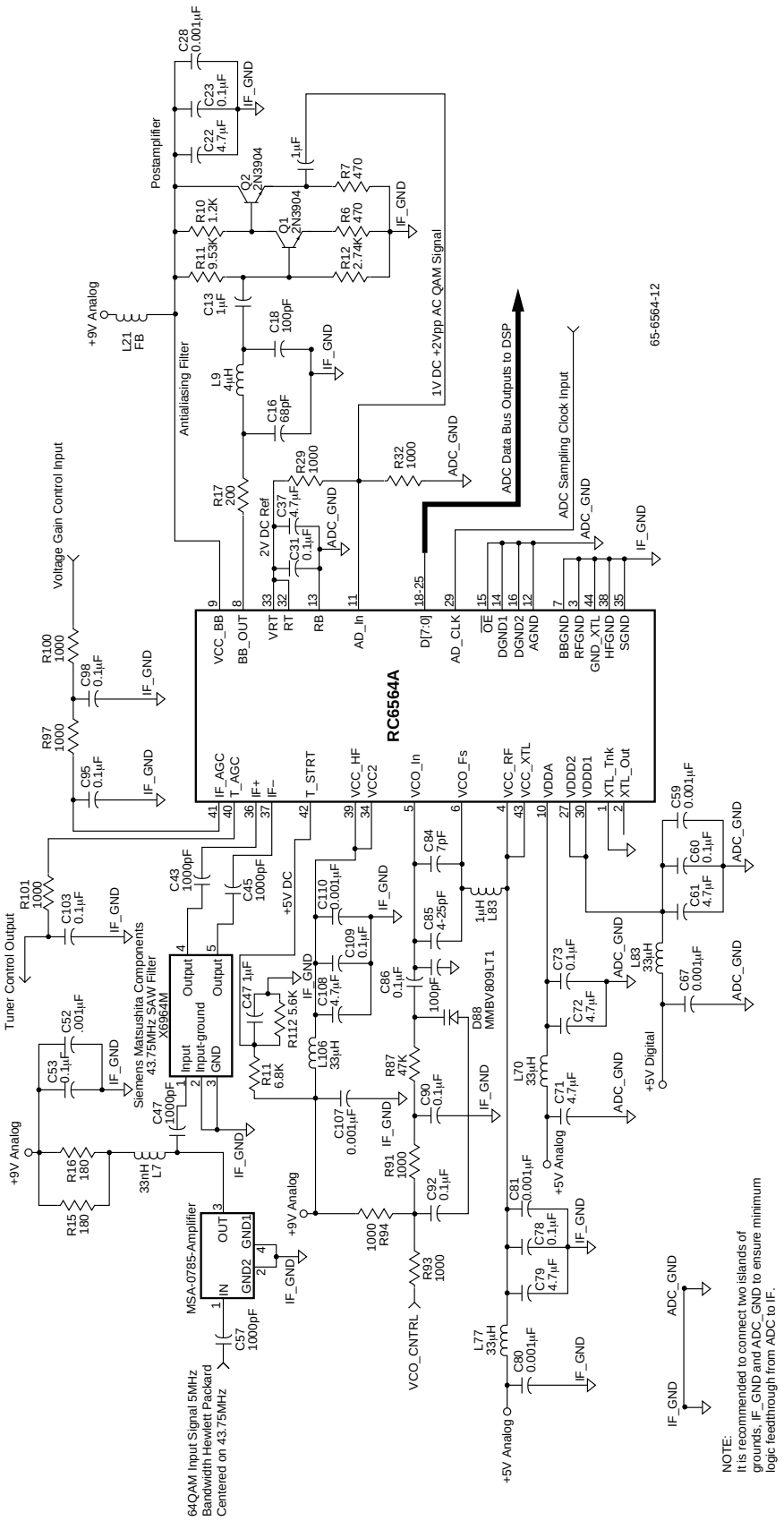
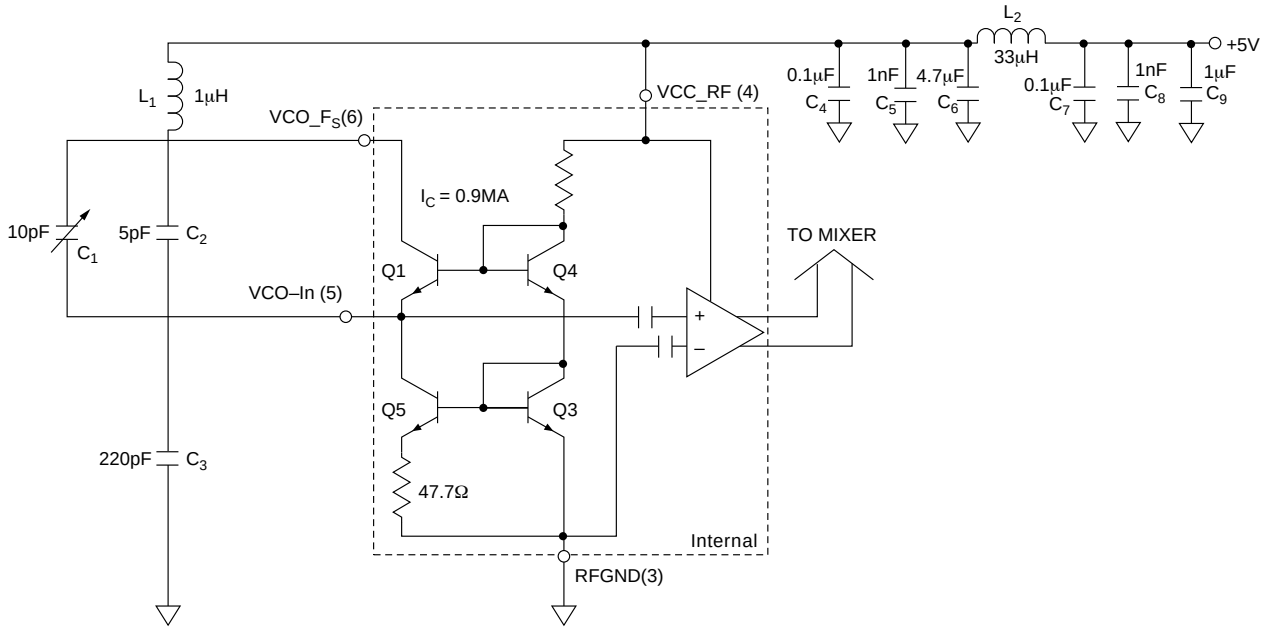


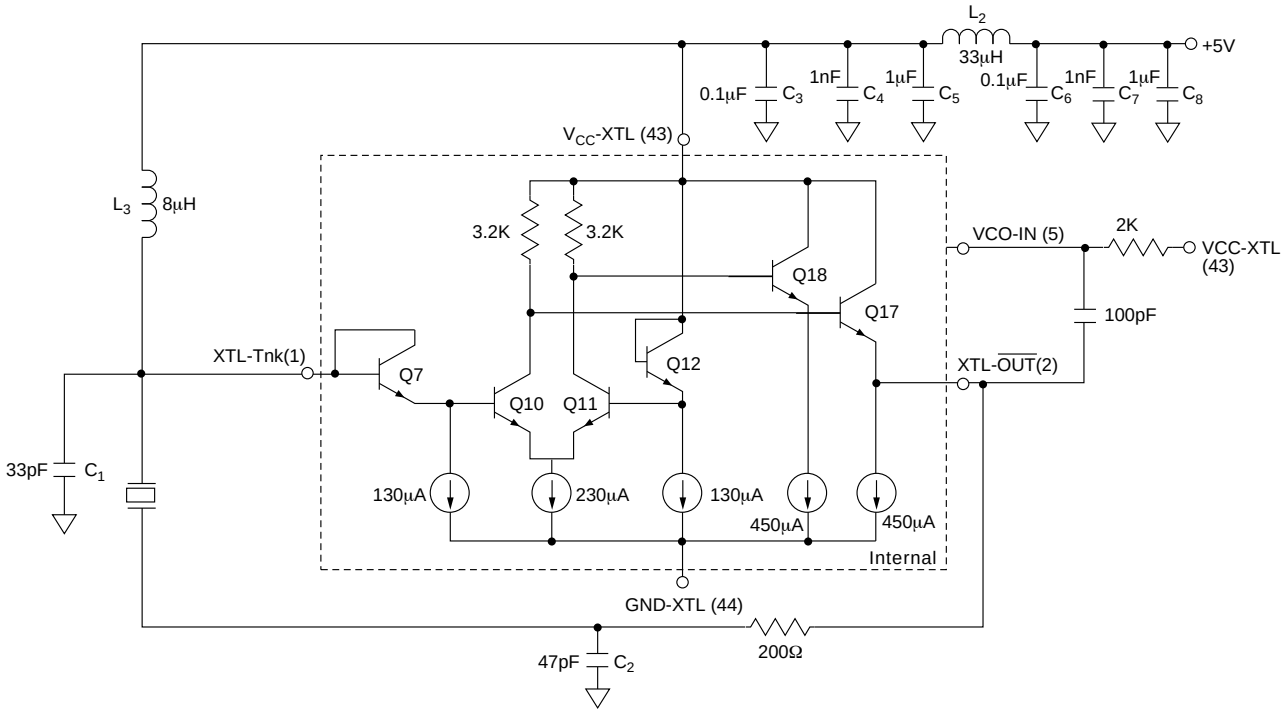
Figure 4. Application of RC6564A in Cable Modem Receivers (Fairchild Semiconductor Demo Board with 64 QAM demodulator)

VCO Internal Schematic



The VCO can be designed as a Colpitts oscillator. The above circuit application shows VCO with adjustable typical value of 38.75 MHz. The frequency is controlled by the external resonance circuit. The oscillating transistor is Q1 in common base configuration. To inject signal in the mixer in place of LO, the VCO_Fs must be open. The signal on the pin VCO_In should be under 100mVp-p and AC coupled.

Crystal Oscillator Internal Schematic



The crystal oscillator is an ECL inverter. It is necessary to bias the XTL-Tnk with a choke to 5V VCC_XTL power supply. The output is about 0.7V DC lower than VCC_XTL with an approximate swing of 0.5Vpp at the output. If the oscillator is not used, it is good to ground XTL_Tnk pin.

Logic Feedthrough

The Logic Feedthrough in the IF section can be minimized by taking the following precautions:

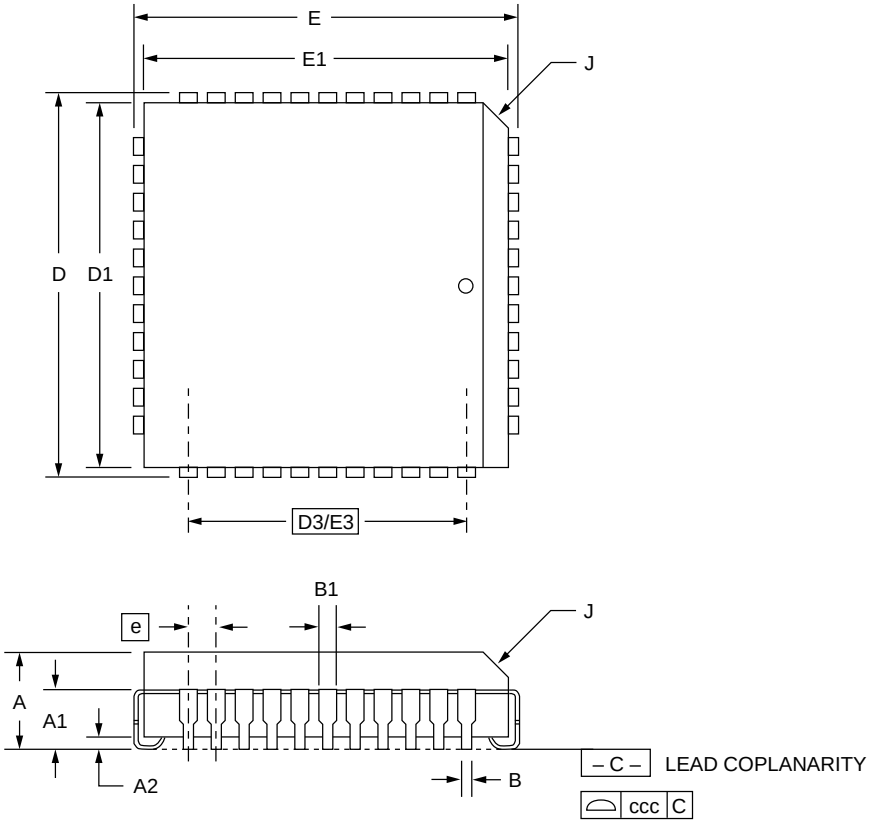
1. It is recommended to have a separate isle for the IF section and the A/D section.
2. All logic circuits in the neighborhood of RC6564A must be isolated. This can be accomplished by carefully decoupling all power supplies and all logic layout signals.
3. It is recommended to have as much ground plane as possible on the top and bottom of the board.

Mechanical Dimensions – 44-Lead PLCC (QB) Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.180	4.19	4.57	
A1	.090	.120	2.29	3.05	
A2	.020	—	.51	—	
B	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D/E	.685	.695	17.40	17.65	
D1/E1	.650	.656	16.51	16.66	3
D3/E3	.500 BSC		12.7 BSC		
e	.050 BSC		1.27 BSC		
J	.042	.056	1.07	1.42	2
ND/NE	11		11		
N	44		44		
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982
2. Corner and edge chamfer (J) = 45°
3. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is .101" (.25mm)



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
RC6564AV	0 °C – 70 °C	Commercial	44-Lead PLCC	RC6564AV

Fairchild Semiconductor Corporation
Americas
Customer Response Center
Tel:1-888-522-5372

Fairchild Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
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Deutsch Tel: +49 (0) 8 141-35-0
English Tel: +44 (0) 1 793-85-68-56
Italy Tel: +39 (0) 2 57 5631

Fairchild Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
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Fax:+852 2314-0061

National Semiconductor Japan Ltd.
Tel:81-3-5620-6175
Fax:81-3-5620-6179

www.fairchildsemi.com

2/98 0.0m
Stock#DS30006564A

RC6601

Voltage Programmable Video Filter

Features

- 250 kHz to 10 MHz minimum programmable range
- Precision factory-trimmed cutoff frequency of 5.5MHz
- Approximates CCIR601 digital video standard
- Phase corrected for minimum group delay variation
- External voltage or current control of cutoff frequency
- 0.25 % differential gain, R_L = 150Ω
- 0.20° differential phase, R_L = 150Ω
- Minimum external components required
- Single ended input/output
- ±5V power supply
- 16-pin SOIC package

Applications

- Video filtering
- Communication filters
- ADC anti-aliasing filter
- HDTV
- Set top boxes
- Satellite modems

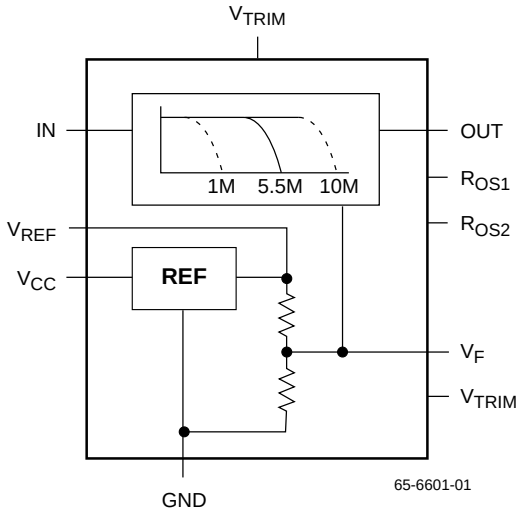
Description

The RC6601 is a fully integrated continuous time filter, designed for various video filtering applications. The RC6601 approximates the requirements of the CCIR601 standard for digitizing NTSC and PAL video signals. It provides factory-set pass band ripple of ±0.25 dB typical up to 5.5 MHz with a -40 dB stop band, beginning at 8 MHz.

The structure of the filter assures wide dynamic range operation with low noise and low distortion. The cutoff frequency is factory set at 5.5 MHz (±5% typical). It can be varied over a range of 250 kHz–10 MHz by a user supplied voltage V_F. The voltage V_F can be readily derived from the on-chip precision reference voltage V_{REF} as shown in the typical application circuit.

The RC6601 is packaged in a 300 mil wide body, 16-pin SOIC package. The package dimensions are included in this data sheet.

Block Diagram



Functional Description

Digitizing video signals requires high-order anti-aliasing filters that can handle large signal swings with low distortion. CCIR601 standards recommend equi-ripple gain and group delay characteristics for filtering NTSC and PAL signals. RC6601 is a single-chip solution that matches the requirements with less than ±0.25dB gain ripple, ±20ns group delay variation in the passband, and more than 40dB attenuation in the stop band. The block diagram in Figure 1a shows the direct synthesis of the filter transfer function as a fifth order elliptic with third order phase equalization. The cut-off frequency, nominally set at 5.5MHz, is continuously programmable over a decade. Using current mode techniques, the IC can drive 2Vpp signals into 75Ω load drawing only 35mA quiescent current.

The architecture of the complete filter as illustrated by Figure 1a is a 5th-order elliptic transfer function in tandem with a 3rd-order all-pass phase equalizer. The Cauer-elliptic response function has an equi-ripple passband with a sharp roll-off into stop-band in the magnitude transfer function but causes excessive group delay peaking. The equalizer maintains this magnitude response while compensating for the group delay peaking. These two filters are represented in Figure 1a by a series of 2nd-order expressions that can be realized as biquads using transimpedance-based integrators.

Elliptic poles and zeros give a flat magnitude response in passband and a 40dB roll-off from 5.5MHz to 8MHz. The equalizer transfer function corrects group delay to ±15ns to 90% of the cut-off frequency. These pole-zero values determine biquad coefficients as shown in Figure 1b. A supply-independent band-gap cell generates and distributes bias currents for all the transimpedance integrators as in Figure 1b. The cut-off frequency is programmed by globally scaling the currents, using a single external setting.

The entire filter, including the programmable bias generators, is integrated on a single chip using complementary bipolar technology. The npn and pnp transistors have a cut-off frequency of 4GHz and of 1.5GHz respectively. Gate-oxide-based capacitors and thin film resistors with 0.5% match set filter time constants. At 5.5MHz cut-off, the filter averages 2.5mA/pole. Nearly 15mA of the supply current is used for the output driver. The cut-off frequency is actually programmable beyond the 1–10 MHz, with an external voltage control. Measured differential gain of 0.25% and a differential phase of 0.2° make it well suited for video applications.

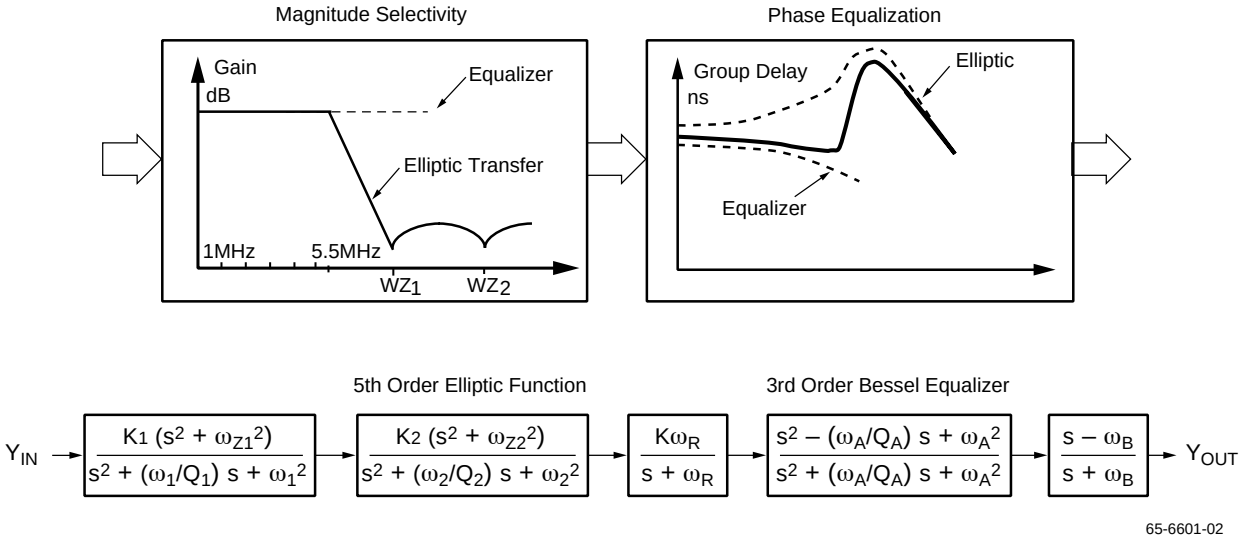
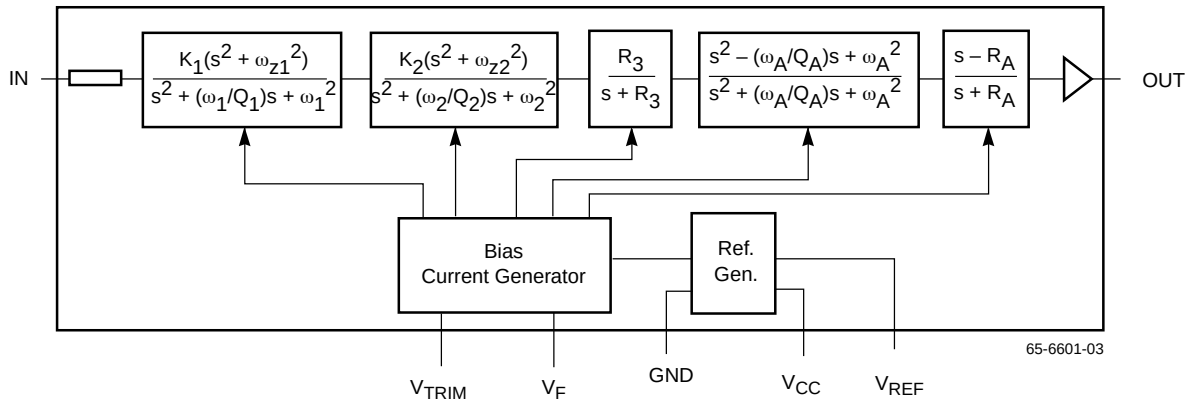


Figure 1a. Composite Video Filter

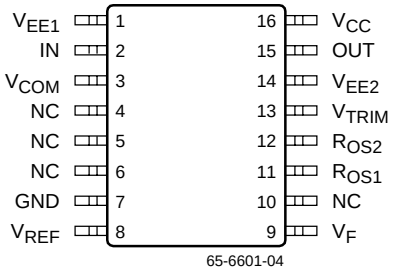


$K_1, K_2 = 0.09293$ $\omega_{Z1} = 1.415\omega_C$ $\omega_1 = 1.046\omega_C$
$Q_1 = 5.67$ $\omega_{Z2} = 2.0733\omega_C$ $\omega_2 = 0.855\omega_C$
$Q_2 = 1.1776$ $R_3 = 0.59678\omega_C$ $\omega_A = 1.44868\omega_C$
$Q_A = 0.691$ $R_A = 1.323\omega_C$

where ω_C = cut off frequency (in radians)
e.g. for default filter: $\omega_C = 2\pi \bullet (5.5)10^6 = 34.5575 \times 10^6$
Scaling bias currents directly scales the frequency ω_C

Figure 1b. Internal Programming Architecture

Pin Assignments



Pin Descriptions

Pin Name	Pin Number	Description
GND	7	Supply Ground
IN	2	Signal Input
NC	4–6, 10	No Connect
OUT	15	Signal Output
R_{OS1}	11	Offset Adjust 1
R_{OS2}	12	Offset Adjust 2
V_{CC}	16	Positive Supply Voltage
V_{COM}	3	Common Mode Input Voltage (See Note)
V_{EE1}	1	Negative Supply Voltage (Input Section)
V_{EE2}	14	Negative Supply Voltage (Output Section)
V_F	9	Filter Control Voltage for Cut-off Frequency
V_{REF}	8	Precision Reference Voltage
V_{TRIM}	13	Pass Band Peaking Voltage

Note: V_{COM} pin is typically connected to ground for ±5V supply.

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Min.	Typ.	Max.	Units
Positive Power Supply (V_{CC})			6	V
Negative Power Supply (V_{EE1}, V_{EE2})			-6	V
Input Voltage	(V_{EE1}, V_{EE2}) -0.3 V to V_{CC} to +0.3V			V
Input Current (Power On or Off)			±10	mA
Operating Temperature	0		70	°C
Storage Temperature	-40		125	°C
Junction Temperature		150		°C
Lead Soldering (10 seconds)			300	°C
Short Circuit Tolerance	No more than one output may be shorted to ground.			

Note:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter		Min.	Typ.	Max.	Units
V_{CC}	Power Supply Voltage	4.75	5.0	5.25	V
V_{EE}	Negative Supply Voltage	-5.25	-5.0	-4.75	V
I_S	Quiescent Supply Current		40	50	mA
θ_{JA}	SO16 Thermal Resistance		105		°C/W

DC Electrical Characteristics

V_{CC} = 5V, $V_{EE1,2}$ = -5V, C_L = 15pF, R_L = 150Ω, T_A = 25°C, unless otherwise specified.

Parameter		Conditions	Min.	Typ.	Max.	Units
A_V	DC gain accuracy	V_{IN} = 2 Vpp	0.90	1	1.10	V/V
R_{IN}	Input resistance	DC		4		kΩ
I_O	Output current			±10		mA
V_{OFF}	Output offset voltage	Without offset adjust	-500		+500	mV
		With offset adjust	-10		+10	mV
V_{REF}	Reference voltage		2.30	2.48	2.60	V
I_{REF}	Reference output current	Max reference out current		5		mA
V_F	Frequency set voltage (FC = 5.5 MHz ±10%)	I_F = 0, Measure V_F		1.24		V
R_F	Frequency set input resistance			5.0		kΩ

AC Electrical Characteristics

V_{CC} = 5V, $V_{EE1,2}$ = -5V, C_L = 15pF, R_L = 150Ω, f_{PB} = 5.5 MHz, T_A = 25°C, unless otherwise specified.

Parameter		Conditions	Min.	Typ.	Max.	Units
Filter Characteristics						
f_{PB}	Passband frequency	$V_F \approx 0V$	10	15		MHz
		$V_F = V_{REF} \approx 2.5V$	.25		1	MHz
f_{CA}	Filter cutoff accuracy[5,6]	f_{PB} = 5.5MHz	-5		+5	%
f_{CT}	Filter cutoff drift[5]	f_{PB} = 5.5MHz	-5		+5	%
Δt_{GD}	Group delay flatness	f_{in} = 100 kHz to 4,9 MHz		±20		ns
V_{IN}	Input signal range	THD < 1 %(7)	1	2		Vpp
C_{IN}	Input capacitance			10		pF
ΔG	Diff. gain, NTSC & PAL	V_{IN} = 286 mVpp, 4.43 MHz		.25		%
ΔP	Diff. phase, NTSC & PAL	V_{IN} = 286 mVpp, 4.43 MHz		.20		°
e_n	RMS output noise voltage	R_S = 75 Ω, 10 MHz BW(7)		1.3	2.0	mV
SR	Positive slew rate[3]	V_{IN} = 2 Vpp		60		V/µs
	Negative slew rate[3]	V_{IN} = 2 Vpp		60		V/µs
R_O	Output resistance			3		Ω
ATT	Attenuation[1]	$f_{in} \le$ 5.0 MHz, V_{IN} = 1 Vpp		±0.10	±0.25	dB
	Attenuation[2]	$f_{in} \le$ 5.0 MHz, V_{IN} = 1 Vpp		±0.5	± 1	dB
	Attenuation[2]	f_{in} = 6.75 MHz, V_{IN} = 1 Vpp		-12	-8	dB
	Attenuation[2]	f_{in} = 8 MHz, V_{IN} = 1 Vpp		-40		dB
	Attenuation[2]	8 MHz < f_{in} < 50 MHz, V_{IN} = 1 Vpp		-40	-35	dB
	Attenuation[1,4]	$f_{IN} \le$ 2.5 MHz, V_{IN} = 1 Vpp		±0.10	±0.25	dB
	Attenuation[2,4]	$f_{IN} \le$ 2.5 MHz, V_{IN} = 1 Vpp		±0.5	± 1	dB
	Attenuation[2,4]	f_{IN} = 3.375 MHz, V_{IN} = 1 Vpp			-8	dB
	Attenuation[2,4]	f_{IN} = 4 MHz, V_{IN} = 1 Vpp		-40		dB
	Attenuation[2,4]	4 MHz < f_{IN} < 50 MHz, V_{IN} = 1 Vpp			-35	dB
SPW	Sensitivity of cutoff frequency vs. supply voltages	V_S = ±5 V, V_F = 1.25 V		1		%/V

Notes:

1. V_{TRIM} adjusted for optimum response.
2. No external adjustments.
3. Guaranteed no slew limit on 2V p-p input at 9 MHz.
4. Filter programmed for 2.75 MHz cutoff, V_F = 1.85V.
5. Filter cutoff defined to edge of ripple spec.
6. Initial setpoint accuracy of cutoff, excluding temperature and long term drift.
7. Guaranteed by design.

Performance Curves

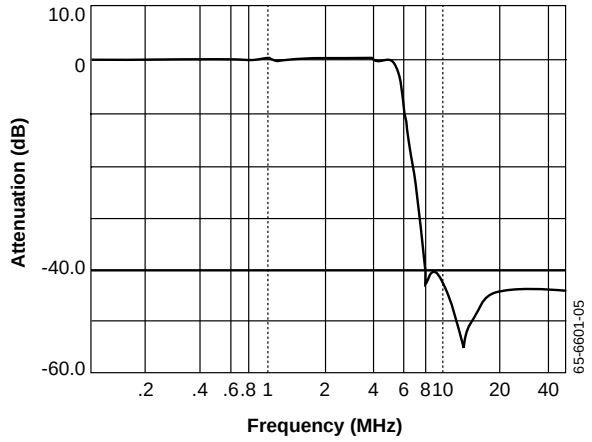


Figure 2. Amplitude Response—Default Setting

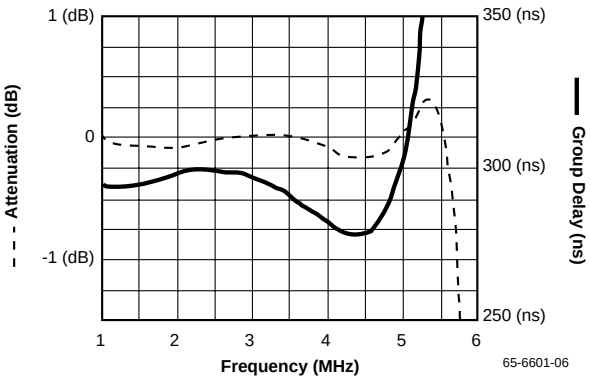


Figure 3. Attentuation and Group Delay

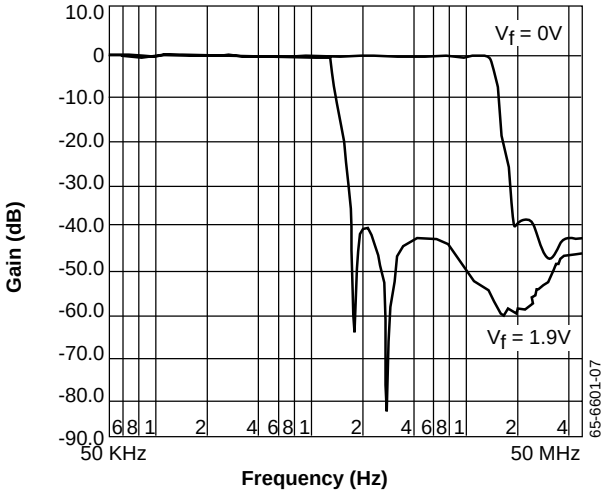


Figure 4. Amplitude Responses Over Programming Range

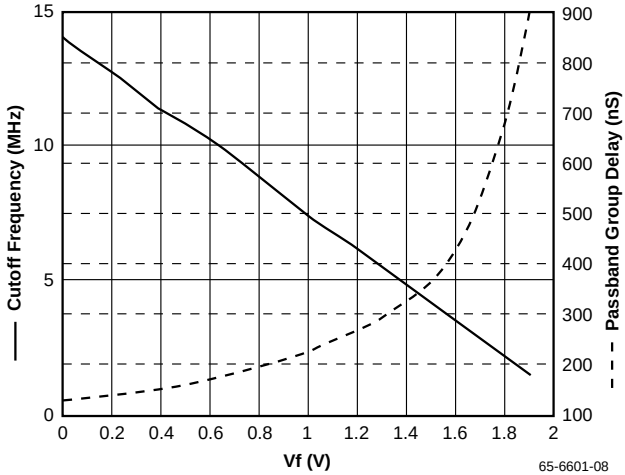


Figure 5. Frequency Programming Using V_f and Passband Group Delay

Application Discussion

The RC6601 is fully integrated in the sense that no critical external components are required for the low pass filtering function. For luminance filtering at a cut-off frequency of 5.5MHz, the only off-chip components are the decoupling capacitors and termination resistors shown in Figure 6. The part also provides temperature and supply independent band-gap reference voltages (2.48V and 1.24V) that can be used for setting the ADC converters or DACs in the system.

The programmable feature of the RC6601 makes it versatile for use in applications with other standard cut-off frequencies. There are three ways of changing the cut-off frequency.

1. **External Voltage setting on V_F:** A higher voltage on V_F than 1.2V gives a lower frequency than 5.5MHz cut-off. The highest frequency (above 10MHz) is obtained by grounding the V_F pin.

2. **Potentiometer at V_{REF} (pin 8) and/or V_F (pin 9):** There is an internal resistor divider of roughly 10K each that sets the default voltage of 1.2V at half the value of V_{REF}. Using a lower value external pot of 1K–2K, the internal setting can be overridden.

3. **Current Source/Sink at V_F:** The typical current output from a DAC can be tied to the V_F pin to program the cut-off frequency from a controller.

In applications requiring dynamic programming of the filter cut-off, a combination of above techniques may be used. Use of the RC6601 in such applications eliminates the need for multiplexers and filter banks. The other adjustment possible on the RC6601 is the output d.c. level. The output d.c. level can be adjusted by connecting a potentiometer between pins R_{OS1} and R_{OS2} (pins 11 and 12) and taking the center tap to V_{CC}. These adjustments are shown in Figure 7 below.

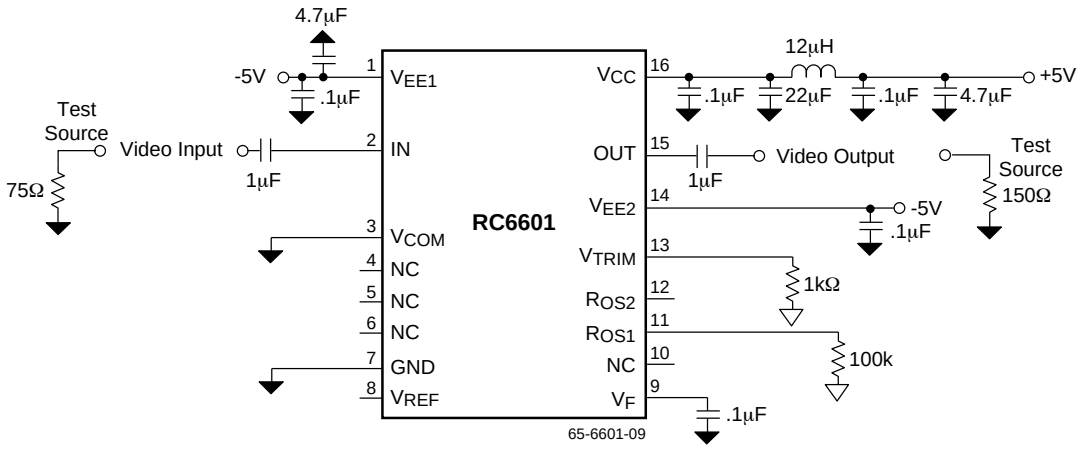


Figure 6. Fixed Configuration CCIR601 (Cutoff frequency is factory set to 5.5MHz)

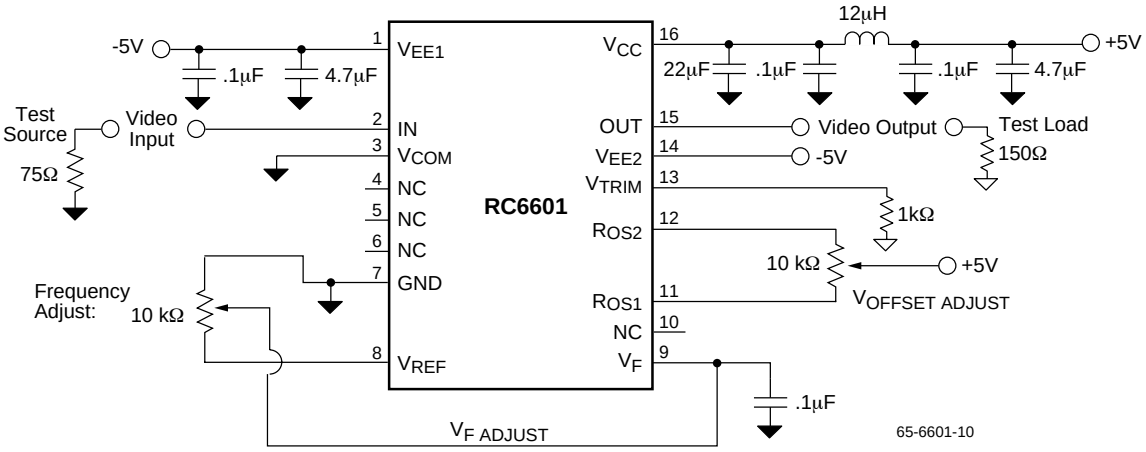


Figure 7. Cutoff Frequency and Offset Tunable Filter

Notes:

Notes:

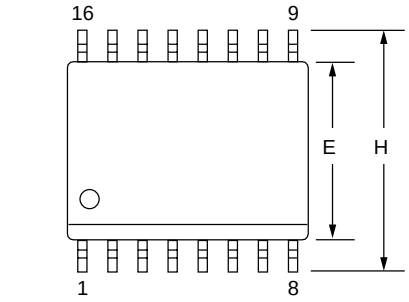
Notes:

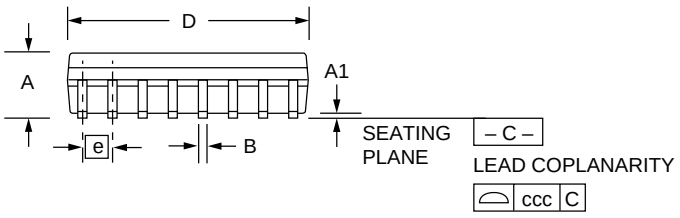
Mechanical Dimensions – 16 Pin SOIC Package

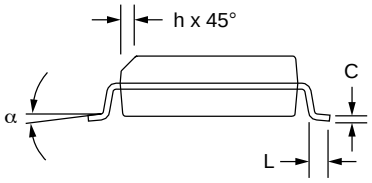
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.398	.413	10.10	10.50	2
E	.291	.299	7.40	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.020	0.25	0.51	
L	.016	.050	0.40	1.27	3
N	16		16		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
RC6601M	0° to 70°C	Commercial	16 Pin Wide SOIC	RC6601M

Embedded Secure Document

The file *http://www.fairchildsemi.com/ds/RC/RC6702.pdf* is a secure document that has been embedded in this document. Double click the pushpin to view RC6702.pdf.

Embedded Secure Document

The file *http://www.fairchildsemi.com/ds/RC/RC6704.pdf* is a secure document that has been embedded in this document. Double click the pushpin to view RC6704.pdf.

RC7100

100MHz Motherboard System Clock

Features

- Four copies of CPU clock
- Eight copies of PCI Clock (Synchronous w/CPU clock)
- Two copies of IOAPIC clock @ 14.318MHz
- Two copies of 48MHz clock
- Three copies of REF clock @ 14.318MHz
- Reference crystal oscillator (14.318MHz)
- Spread Spectrum (-0.5%) clocking
- Power management controls
- Low frequency test mode

Applications

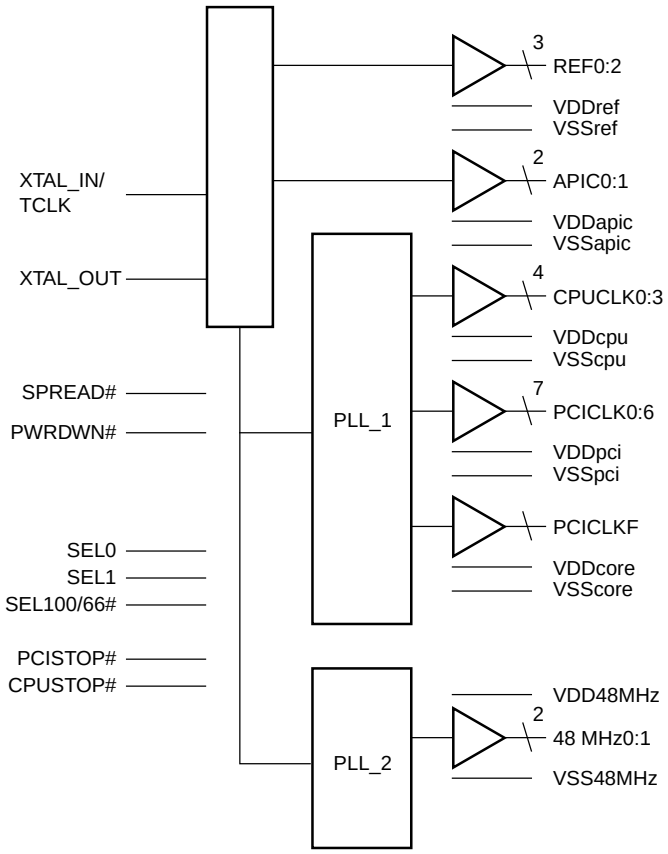
- 100MHz motherboard clock synthesizers for Pentium II CPU based Desktop and Notebook Systems.

Description

The RC7100 is a clock synthesizer for 100MHz operation on Pentium II based motherboard systems.
It contains 4 copies of the CPU clock, 8 copies of the PCI clock, 3 copies of the REF clock, 2 copies of the 48MHz clock and 2 copies of the IOAPIC clock. The CPU and PCI clocks are generated through a phase locked loop and are stable within 3mS after power-up meeting the Pentium II stabilization specifications. The 48MHz clocks are generated through a second phase locked loop.

The RC7100 accepts a 14.318MHz crystal as its reference frequency and operates at a core voltage of 3.3V. A 14.318MHz external clock can also be used instead of the

Block Diagram



Advanced Information

Pentium is a registered trademark of Intel Corporation

Rev. 0.5.3

Description (continued)

crystal. The REF and IOAPIC clocks are generated directly from the reference frequency.

The PWRDWN# pin when low powers down the crystal oscillator and the two phase locked loops. Other pins to control power are the CPUSTOP# and PCISTOP#. The CPUSTOP# when low causes the CPU clocks to go to a low state. The PCISTOP# when low causes the PCI clocks with the exception of the PCICLK_F to go to a low state. The PCICLK_F is a free-running clock. All clock outputs will be tristated when SEL0, SEL1 and SEL100/66# are all low.

Frequency selection between 100 MHz and 66 MHz can be accomplished with the SEL100/66#. SEL100/66# high will provide the 100 MHz operation and low will provide a clock frequency of 66 MHz. Additional frequency selections including TEST MODE can be had with other combinations of the SEL0 and SEL1 pins. See Table 1 for more details.

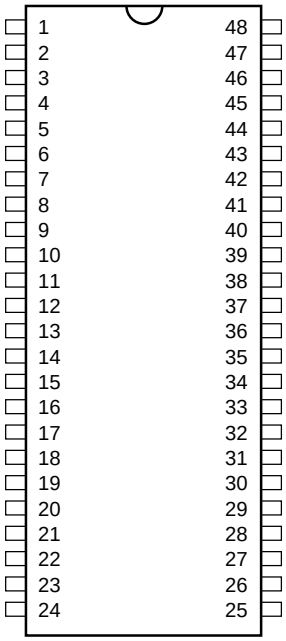
Spread Spectrum clocking is available for the CPU and PCI clocks. It can be activated by bringing the SPREAD# pin to a low state. the REF, IOAPIC and 48MHz clocks are not affected by the SPREAD#.

Advanced Information

Table 1. Selectable Modes

SEL0	SEL 1	SEL100/66	CPU	PCI	REF	IOAPIC	48
0	0	0	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z
1	0	0	75	37.5	14.318	14.318	48
0	1	0	75	30	14.318	14.318	48
1	1	0	66	33	14.318	14.318	48
0	0	1	TC/2	TC/6	TC/2	TC	TC
1	0	1	83.3	41.65	14.318	14.318	48
0	1	1	83.3	33.3	14.318	14.318	48
1	1	1	100	33	14.318	14.318	48

Pin Assignments



Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	REF0	13	PCICLK3	25	SEL100/66#	37	VDDcpu
2	REF1	14	PCICLK4	26	SEL1	38	VSScpu
3	VSSref	15	VDDpci	27	SEL0	39	CPUCLK1
4	XTALIN	16	PCICLK5	28	SPREAD#	40	CPUCLK0
5	XTALOUT	17	PCICLK6	29	PWRDWN#	41	VDDcpu
6	VSSpci	18	VSSpci	30	CPUSTOP#	42	NC
7	PCICLKF	19	VDDcore	31	PCISTOP#	43	VSSapic
8	PCICLK0	20	VSScore	32	VSScore	44	APIC1
9	VDDpci	21	VDD48MHz	33	VDDcore	45	APIC0
10	PCICLK1	22	48MHz0	34	VSScpu	46	VDDapic
11	PCICLK2	23	48MHz1	35	CPUCLK3	47	REF2
12	VSSpci	24	VSS48MHz	36	CPUCLK2	48	VDDref

Pin Descriptions

Pin Name	Pin Number	Type	Pin Function Description
REF0:2	2, 1, 47	OUT	Reference clock outputs running at a fixed frequency equal to the reference crystal or external frequency (14.318MHz). These operate from a 3.3V power source.
APIC0:1	44, 45	OUT	APIC clocks running at a fixed frequency equal to the reference crystal or external frequency. It is usually 14.318MHz. These operate from a 2.5V power source.
CPUCLK0:3	35, 36, 39, 40	OUT	CPU clocks used to drive the CPU processor. These clock outputs operate from a 2.5V power source.
PCICLKF	7	OUT	Free-running PCI clock which is not affected by PCISTOP#.
PCICLK0:6	8, 10, 11, 13, 14, 16, 17	OUT	PCI clocks for generating all PCI timing requirements. These clock outputs operate from a 3.3V power source.
48MHz0:1	22, 23	OUT	48MHz clocks are fixed frequency outputs for USB or super I/O requirements.
XTALIN	4	IN	Crystal oscillator input or external reference generator input.
XTALOUT	5	OUT	Crystal oscillator output.
SEL100/66#	25	IN	Selects 100MHz or 66MHz for CPU clocks. When this input is at a “1” level, the CPU frequency will be 100MHz and if at a “0” level the frequency will be 66MHz.
SEL1, SEL0	26, 27	IN	Control select pins for selecting different modes of operation.
PWRDWN#	29	IN	PWRDWN# is an input pin used to power-down the chip when low.
PCISTOP#	31	IN	Stops PCI clocks at low state when low
CPUSTOP#	30	IN	Stops CPU clocks at a low state when low
SPREAD#	28	IN	SPREAD# is active low and when activated the CPU and PCI clocks are spread from 0.5% below the maximum frequency to the maximum frequency.
VDDpci, VDDref, VDDcore, VDD48MHz	9, 15, 19, 21, 33, 48	POWER	3.3V supply for PCICLK, PCICLKF, REF, 48MHz drivers and PLL core
VDDcpu, VDDapic	37, 41, 46	POWER	2.5V supply for CPU and APIC drivers
VSSref, VSSpci, VSS48MHz, VSScore, VSScpu, VSSapic	3, 6, 12, 18, 20, 24, 32, 34, 38, 43	GROUND	Ground
NC	42	reserved	No connect - reserved for future use

Advanced Information

Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Units
Supply Voltage, VDD	-0.5		5	V
Input Voltage	-0.5		V_{DD}+.5	V
Output, Applied Voltage	-0.5		V_{DD}+.5	V
Junction Temperature			140	°C
Storage Temperature	-65		150	°C
Lead Soldering (10 seconds)			300	°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current, flowing into the device.

Operating Conditions

Parameter	Min.	Typ.	Max.	Units
VDDapic 2.5V Power Supply Voltage VDDcpu	2.375	2.5	2.625	V
VDDref 3.3V Power Supply Voltage VDD48MHz VDDpci VDDcore	3.135	3.3	3.465	V
Ambient Temperature	0		70	°C

Advanced Information

Electrical Characteristics

Parameter		Min.	Typ.	Max.	Units
Logic inputs					
V_{IL}	Input low voltage	-0.3		0.8	V
V_{IH}	Input high voltage	2.0		VDD+.3	V
I_{IL}	Input low current			-5	μA
I_{IH}	Input high current			5	μA
Clock Outputs					
V_{OL}	Outputs @ 1mA			0.4	V
V_{OH}	Outputs @ -1mA	2.4			V
I_{OL}	CPU0:3@ vol = 1.4V	28		100	mA
	PCI_F, PCI1:7 @ vol = 1.4V	26.5		139	mA
	APIC0:1 @ vol = 1.4V	42		150	mA
	REF0:2 @ vol = 1.4V	25		76	mA
	48MHz0:1 @ vol = 1.4V	25		76	mA
I_{OH}	CPU0:3 @ voh = 1.4V	-24		-94	mA
	PCI_F, PCI1:7 @ voh = 1.4V	-31		-189	mA
	APIC0:1 @ voh = 1.4V	-36		-140	mA
	REF0:2 @ voh = 1.4V	-27		-94	mA
	48MHz0:1 @ voh = 1.4V	-27		-94	mA
Crystal oscillator					
V_{TH}	Input threshold voltage				V
C_{LOAD}	Load capacitance imposed on external crystal		18		pF
C_{IN}(XIN)	Input capacitance	13.5	18	22.5	pF
Pin Capacitance/Inductance					
C_{IN}	Input Pin Capacitance			5	pF
C_{OUT}	Output Pin Capacitance			6	pF
L_{IN}	Input Pin Inductance			7	nH

Advanced Information

Switching Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
CPU Clocks CPU0:3	C_{LOAD} = 20pF				
Period	100MHz 66MHz	10 15		10.5 15.5	nS
High time	100MHz 66MHz	3.0 5.2			nS
Low time	100MHz 66MHz	2.8 5.0			nS
Tr	100MHz, 66MHz	0.4		1.6	nS
Tf	100MHz, 66MHz	0.4		1.6	nS
tjitter	100MHz, 66MHz			250	pS
Duty cycle @ V = 1.25V	100MHz, 66MHz	45		55	%
tskew	100MHz, 66MHz			175	pS
tpZL, tpZH	100MHz, 66MHz	1.0		8.0	nS
tpLZ, tpHZ	100MHz, 66MHz	1.0		8.0	nS
tstabilization	100MHz, 66MHz			3.0	mS
toffset (CPU to PCI)	100MHz, 66MHz	1.5		4.0	nS
IOAPIC APIC0:1					
tskew	100MHz, 66MHz			250	pS
PCI PCICLK_F, PCICLK1:7					
tperiod	100MHz, 66MHz	30.0			nS
tperiod stability	100MHz, 66MHz			500	pS
thigh	100MHz, 66MHz	12.0			nS
tlow	100MHz, 66MHz	12.0			nS
tskew	100MHz, 66MHz			500	pS
tstabilization	100MHz, 66MHz			3	mS

Advanced Information

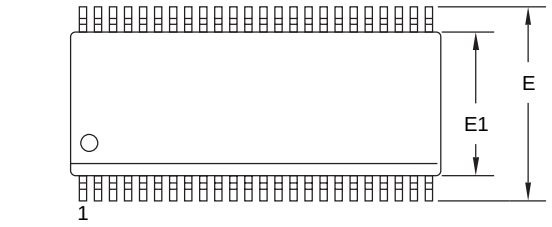
Mechanical Dimensions

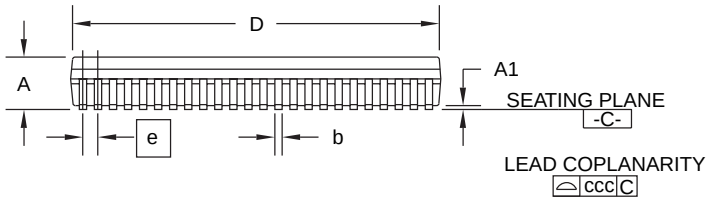
48 pin SSOP

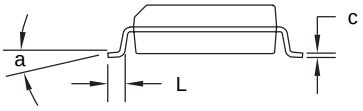
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.095	.110	2.41	2.79	
A1	.008	.016	0.20	0.41	
b	.008	.0135	0.20	0.34	5
c	.005	.010	0.13	0.25	5
D	.620	.630	15.75	16.00	2, 4
E	.395	.420	10.03	10.67	
E1	.291	.299	7.39	7.59	2
e	.025 BSC		0.64 BSC		
L	.020	.040	0.51	1.02	3
N	48		48		6
a	0°	8°	0°	8°	
ccc	---	.004	---	0.13	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
2. "D" and "E1" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "b" & "c" dimensions include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Advanced Information

Ordering Information

Product Number	Temperature	Screening	Package	Package Marking
RC7100	0°C to 70°C		48 SSOP	RC7100

Advanced Information

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

5/20/98 0.0m 001
Stock#DS50007100

RC7101

Low Skew Buffers

100MHz SDRAM Clock Buffers

Features

- 18 skew controlled outputs
- Supports up to four SDRAM DIMMs
- Skew between any two outputs is less than 250 pS
- I^2C Serial Interface for programming options
- Multiple power and ground pins for noise reduction
- Single 3.3V power supply
- 48 Pin SSOP package

Applications

- SDRAM Clock Buffers for Intel's 440BX chip set

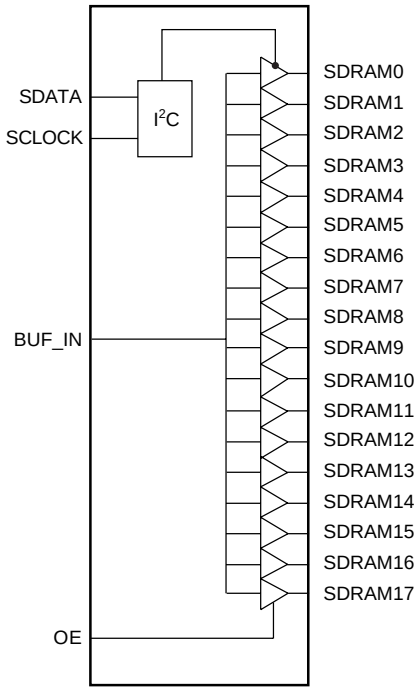
Description

The RC7101 is a low voltage eighteen output clock buffer which supports 4 DIMMs. The skew between any two outputs is less than 250 pS and the buffers can be individually enabled or disabled by programming via the I^2C serial interface. The SDATA and SCLK serial inputs both have internal pull-up resistors.

An Output Enable (OE) pin is also provided so that all the outputs can be tri-stated when held low. This pin is normally high and has an internal pull-up resistor.

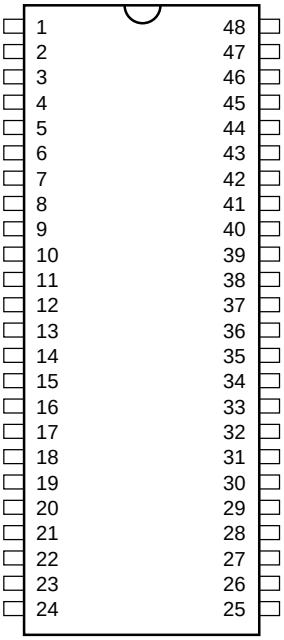
OE	SDRAM0:3	SDRAM4:7	SDRAM8:11	SDRAM12:15	SDRAM16:17
0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
1	BUF_IN	BUF_IN	BUF_IN	BUF_IN	BUF_IN

Block Diagram



Advanced Information

Pin Assignments



48 Pin SSOP

Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name
1	NC	13	SDRAM4	25	SCLOCK	37	VDD
2	NC	14	SDRAM5	26	VSS	38	OE
3	VDD	15	VSS	27	VSS	39	VSS
4	SDRAM0	16	VDD	28	SDRAM17	40	SDRAM12
5	SDRAM1	17	SDRAM6	29	VDD	41	SDRAM13
6	VSS	18	SDRAM7	30	VSS	42	VDD
7	VDD	19	VSS	31	SDRAM8	43	VSS
8	SDRAM2	20	VDD	32	SDRAM9	44	SDRAM14
9	SDRAM3	21	SDRAM16	33	VDD	45	SDRAM15
10	VSS	22	VSS	34	VSS	46	VDD
11	BUF_IN	23	VDD	35	SDRAM10	47	NC
12	VDD	24	SDATA	36	SDRAM11	48	NC

Advanced Information

Pin Descriptions

Pin Name	Pin Number	Type	Pin Function Description
BUF_IN	11	IN	Input for clock buffers
SDRAM0:3	4, 5, 8, 9	OUT	SDRAM Byte 0 clock outputs
SDRAM4:7	13, 14, 17, 18	OUT	SDRAM Byte 1 clock outputs
SDRAM8:11	31, 32, 35, 36	OUT	SDRAM Byte 2 clock outputs
SDRAM12:15	40, 41, 44, 45	OUT	SDRAM Byte 3 clock outputs
SDRAM16:17	21, 28	OUT	SDRAM clock outputs
OE	38	IN	Output enable which will tri-state all the outputs when held low
SDATA	24	I/O	Serial Data Line
SCLOCK	25	IN	Serial Clock input
VDD	3, 7, 12, 16, 20, 29, 33, 37, 42, 46	Power	Power supply at 3.3V for SDRAM buffers
VDD	23	Power	Power supply at 3.3V for I^2C circuit
VSS	6, 10, 15, 19, 22, 27, 30, 34, 39, 43	Ground	Ground for SDRAM buffers
VSS	26	Ground	Ground for I^2C circuit
NC	1, 2, 47, 48	NC	No Connections.

Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Units
Supply Voltage, V_{DD}	-0.5		5	V
Input Voltage	-0.5		V_{DD}+0.5	V
Output Applied Voltage	-0.5		V_{DD}+0.5	V
Junction Temperature			140	°C
Storage Temperature	-65		150	°C
Lead Soldering (10 seconds)			300	°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current, flowing into the device.

Operating Conditions

Parameter	Min.	Typ.	Max.	Units
V_{DD}	3.135	3.3	3.465	V
Ambient Temperature	0		70	°C

Electrical Characteristics T_A = 0°C to 70°C, V_{DD} = 3.3V±5%

Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IL}, Input low voltage		-0.3		0.8	V
V_{IH}, Input high voltage		2.0		V_{DD}+0.3	V
I_{IL}, Input low current (BUF_IN)				-25	µA
I_{IH}, Input high current (BUF_IN)				10	µA
I_{IL}, Input low current OE, SDATA, SCLOCK)				-50	µA
I_{IH}, Input high current (OE, SDATA, SCLOCK)				10	µA
V_{OL}, Output low voltag	I_{OL} = 23mA			0.4	V
V_{OH}, Output high voltage	I_{OH} = -30mA	2.6			V
I_{OL}, Output low current	V_{OL} = 0.8V	40			mA
I_{OH}, Output high current	V_{OH} = 2.0V			-54	mA
I_{DD}, Supply current	f = 100MHz				mA
I_{DD}, Supply current	f = 66MHz				mA
I_{DD}, Supply current	OE = 0				mA
C_{IN}, Input capacitance				5	pF
F_{IN}, Input frequency				150	MHz

Advanced Information

Switching Characteristics

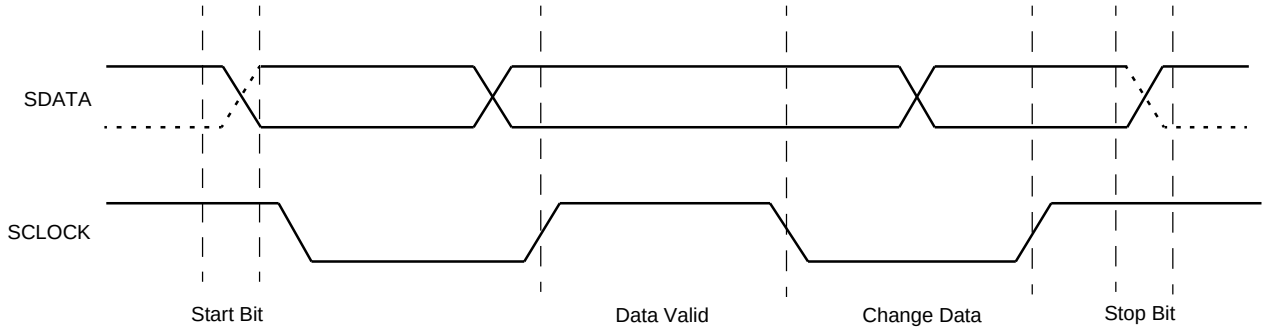
Parameter	Conditions	Min.	Typ.	Max.	Units
T_{PD}, Propagation delay	V_T = 1.5V	1		5	ns
T_R, Rise time	0.4 to 2.4V	0.5		1.5	ns
T_F, Fall time	2.4 to 0.4V	0.5		1.5	ns
T_D, Duty cycle	V_T = 1.5V	45		55	%
T_{EN}, Output enable time	V_T = 1.5V	1		8	ns
T_{DIS}, Output disable time	V_T = 1.5V	1		8	ns
T_{SK}, Skew	V_T = 1.5V			250	ps
Z_O, Output impedance			15		Ω

Advanced Information

Serial Data Interface

Signaling Requirements for the I²C Serial Port

To initiate communications with the serial port, a start bit is invoked. The start bit is defined as the SDATA line is brought low while the SCLOCK is held high. Once the start bit is initiated, valid data can then be sent. Data is considered to be valid when the clock goes to and remains in the high state. The data can change when the clock goes low. To terminate the transmission, a stop bit is invoked. The stop bit occurs when the SDATA line goes from a low to a high state while the SCLOCK is held high. See Figure below.



The data transfer rate is 100kbits/s in the standard mode and 400kbits/s in the fast mode. The serial protocol uses block writes only. Bytes are written with the lowest first and the highest last with the ability to stop after any complete byte has been transferred. The clock driver is a slave/receiver only and is only capable of receiving data with the exception of sending acknowledgements. It is not capable of sending data.

Byte writing sequence

The buffer is accessed when the slave address byte is received. Each byte of data is followed by an acknowledge bit. The address bit sequence is 1 1 0 1 0 0 1 followed by the R/W# bit (0). Bits are written with the Most Significant Bit (MSB) first. The MSB Bit is bit 7 and the LSB is bit 0. The Byte writing sequence is as shown in the table below.

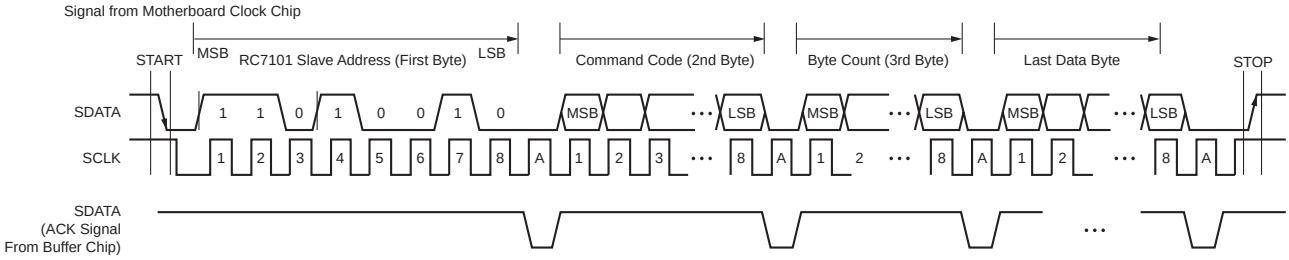
Byte Sequence	Byte name	Bit sequence 7	6	5	4	3	2	1	0
1	Slave address	1	1	0	1	0	0	1	0
2	Command Code	X	X	X	X	X	X	X	X
3	Byte Count	X	X	X	X	X	X	X	X
4	Data Byte 0	see table below							
5	Data Byte 1	see table below							
6	Data Byte 2	see table below							
7	Data Byte 3	X	X	X	X	X	X	X	X
8	Data Byte 4	X	X	X	X	X	X	X	X
9	Data Byte 5	X	X	X	X	X	X	X	X
10	Data Byte 6	X	X	X	X	X	X	X	X

Data Bytes 0 to 2 Map

Bit	Pin	Name	Description
Data Byte 0: SDRAM Active/Inactive Register (1 = enable, 0 = disable)			
7	18	SDRAM7	(ACTIVE/INACTIVE)
6	17	SDRAM6	(ACTIVE/INACTIVE)
5	14	SDRAM5	(ACTIVE/INACTIVE)
4	13	SDRAM4	(ACTIVE/INACTIVE)
3	9	SDRAM3	(ACTIVE/INACTIVE)
2	8	SDRAM2	(ACTIVE/INACTIVE)
1	5	SDRAM1	(ACTIVE/INACTIVE)
0	4	SDRAM0	(ACTIVE/INACTIVE)
Data Byte 1: SDRAM Active/Inactive Register (1 = enable, 0 = disable)			
7	45	SDRAM15	(ACTIVE/INACTIVE)
6	44	SDRAM14	(ACTIVE/INACTIVE)
5	41	SDRAM13	(ACTIVE/INACTIVE)
4	40	SDRAM12	(ACTIVE/INACTIVE)
3	36	SDRAM11	(ACTIVE/INACTIVE)
2	35	SDRAM10	(ACTIVE/INACTIVE)
1	32	SDRAM9	(ACTIVE/INACTIVE)
0	31	SDRAM8	(ACTIVE/INACTIVE)
Data Byte 2: SDRAM Active/Inactive Register (1 = enable, 0 = disable)			
7	28	SDRAM17	(ACTIVE/INACTIVE)
6	21	SDRAM16	(ACTIVE/INACTIVE)
5		reserved	reserved
4		reserved	reserved
3		reserved	reserved
2		reserved	reserved
1		reserved	reserved
0		reserved	reserved

Advanced Information

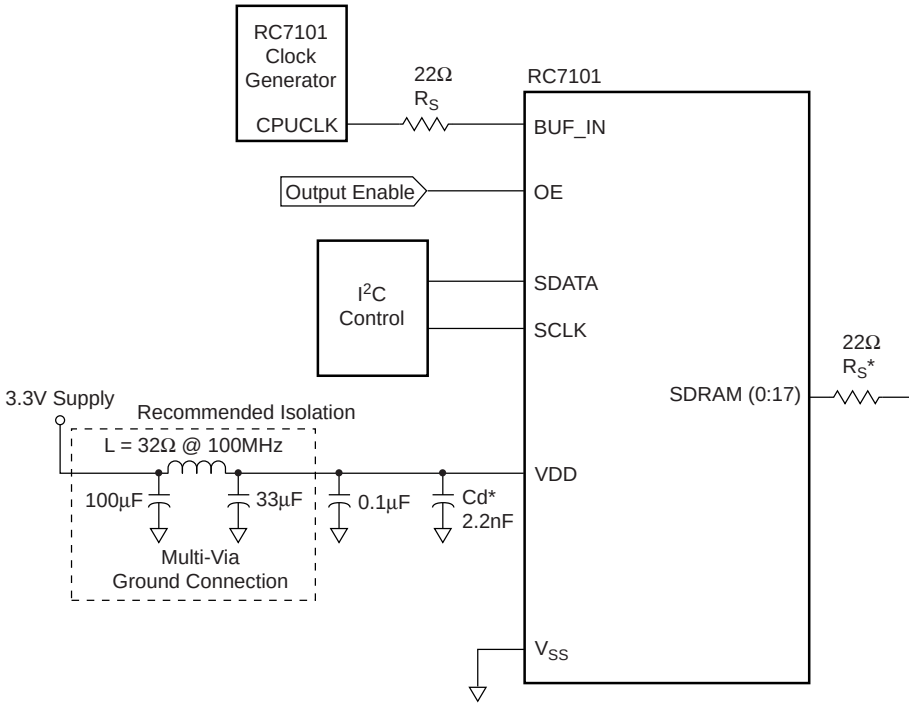
RC7101 I²C Interface Write Sequence



Note: Once the clock detects the start condition and its ADDRESS is matched, the clock chip will pull down the SDATA at every 8th bit. The 8 bit data from SDATA is latched into the Buffer Chip when the ACK is generated. This ACK signal will continue as long as STOP condition is detected The COMMAND CODE and BYTE COUNT is not used by the Buffer Chip.

Advanced Information

Application Circuit



*Each VDD pin should be separately decoupled with a 2.2nF capacitor.

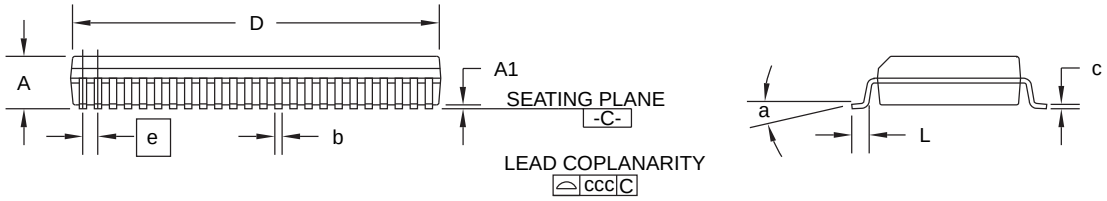
Mechanical Dimensions

48 pin SSOP

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.095	.110	2.41	2.79	
A1	.008	.016	0.20	0.41	
b	.008	.0135	0.20	0.34	5
c	.005	.010	0.13	0.25	5
D	.620	.630	15.75	16.00	2, 4
E	.395	.420	10.03	10.67	
E1	.291	.299	7.39	7.59	2
e	.025 BSC		0.64 BSC		
L	.020	.040	0.51	1.02	3
N	48		48		6
a	0°	8°	0°	8°	
ccc	---	.004	---	0.13	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
2. "D" and "E1" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "b" & "c" dimensions include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.



Advanced Information

Ordering Information

Product Number	Temperature	Screening	Package	Package Marking
RC7101	0°C to 70°C		48 SSOP	RC7101

Advanced Information

RC7102

BX Spread Spectrum Frequency Synthesizer for Pentium II®

Features

- Maximized EMI suppression using Fairchild's proprietary Spread Spectrum Technology
- Single chip system frequency synthesizer for Intel BX chip set
- Two copies of CPU output
- Six copies of PCI output
- One 48MHz output for USB
- One 24MHz output for SIO
- Two buffered reference outputs
- One IOAPIC output
- Fourteen SDRAM outputs provide support for 3 DIMMs
- Supports frequencies up to 150MHz
- I^2C interface for programming
- Power management control inputs
- Smooth CPU frequency switching from 66.8

Description

The RC7102 was developed as a single chip device to meet the clocking needs of the Intel BX™ chipset. In addition to the typical outputs provided by standard 100 MHz BX™ FTG's, the RC7102 adds a fourteen output buffer, supporting SDRAM DIMM modules in conjunction with the chipset.

Fairchild's proprietary spread spectrum frequency synthesis technique is a feature of the CPU and PCI outputs. When enabled, this feature reduces the peak EMI measurements by up to 10dB.

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Block Diagram

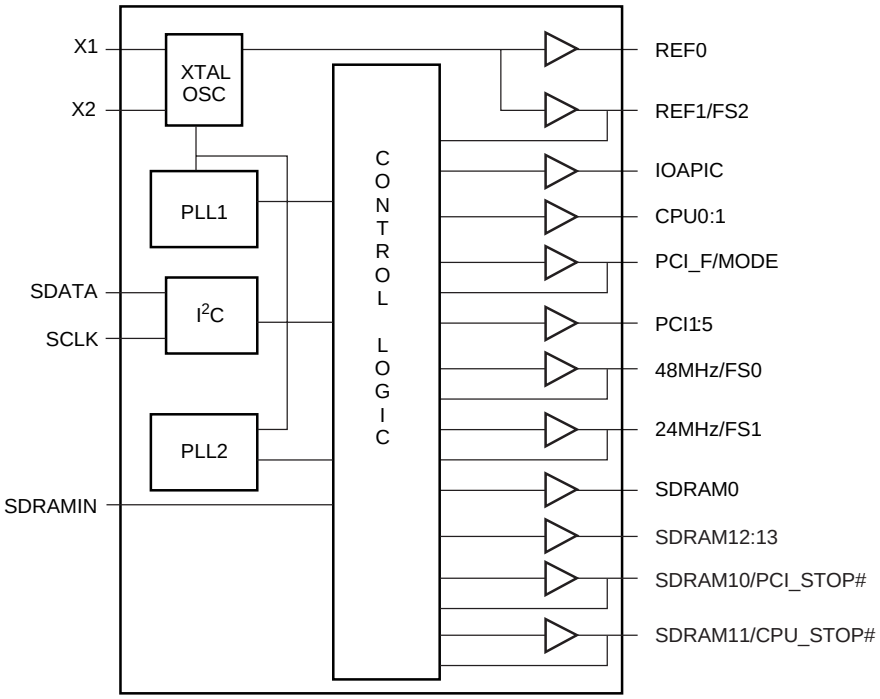


Table 1. Mode Input Table

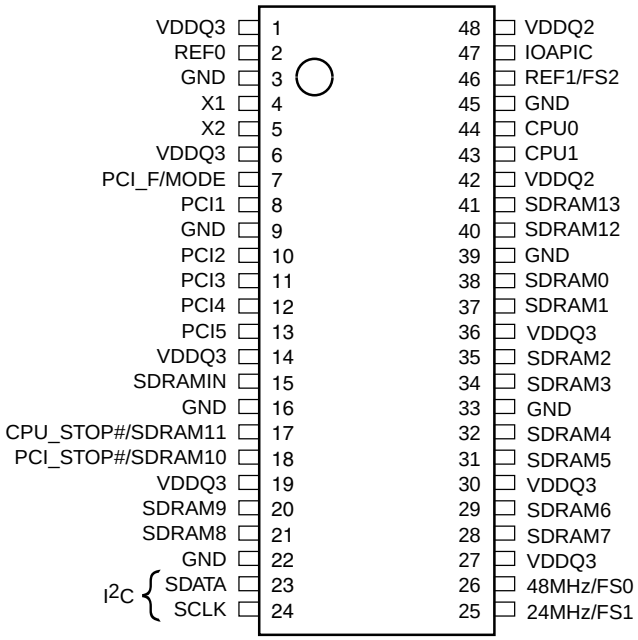
Mode	Pin 17	Pin 18
0	CPU-STOP#	PCI_STOP#
1	SDRAM11	SDRAM10

Table 2. Pin Selectable Frequency

Input Address			CPU Outputs (MHz)	PCI Outputs (MHz)
FS2	FS1	FS0		
1	1	1	100	33.3 (CPU/3)
1	1	0	133.3	44.4 (CPU/3)
1	0	1	112	37.3 (CPU/3)
1	0	0	103	34.3 (CPU/3)
0	1	1	66.8	33.4 (CPU/2)
0	1	0	83.3	41.7 (CPU/2)
0	0	1	75	37.5 (CPU/2)
0	0	0	124	41.3 (CPU/3)

Pin Assignments

48 pin SSOP



Advanced Information

Pin Assignments

Pin Name	Pin Number	Type	Pin Function Description
CPU0:1	43, 44	OUT	**CPU Outputs:** The CPU clock outputs are controlled by the CLK_STOP# control pin.
PCI1:5	8, 10, 11, 12, 13	OUT	**PCI Clock Outputs 1 through 5:** These five PCI clock outputs are controlled by the PCI_STOP# control pin.
MODE/PCI_F	7	IN/OUT	**Fixed PCI Clock Output:** Frequency is set by the FS0:2 inputs or through serial input interface. (see Tables 2 and 6) This output is not affected by the PCI_STOP# input. Upon power-up MODE input will be latched, which will enable or disable SDRAM10 and SDRAM11. (see Tables 1 and 2)
CPU_STOP#/ SDRAM11	17	IN/OUT	**$\overline{\text{CPU\_STOP}}$ Input:** When brought low, the CPU clock outputs are stopped low after completing a full clock cycle.
IOAPIC	47	OUT	**IOAPIC Clock Output:** Provides 14.318MHz fixed frequency. The output voltage swing is controlled by VDDQ2..
48MHz/FS0	26	IN/OUT	**48MHz Output:** 48MHz is provided in normal operation. In standard systems, this output can be used as the reference for the Universal Serial Bus. Upon power-up FS0 input will be latched, which will set clock frequencies as described in Table 2.
24MHz/FS1	25	IN/OUT	**24MHz Output:** 24MHz is provided in normal operation. In standard systems, this output can be used as the clock input for a Super I/O chip. Upon power-up FS1 input will be latched, which will set clock frequencies as described in Table 2.
REF1/FS2	46	IN/OUT	**I/O Dual Function REF1 and FS2 pin:** Upon power-up, FS2 input will be latched which will set clock frequencies as described in Table 2. When an output, this pin provides a fixed clock signal equal in frequency to the reference signal provided at the X1/X2 pins.
REF0	2	OUT	REF0 output, this pin provides a fixed clock signal equal in frequency to the reference signal provided at the X1/X2 pins.
SDRAMIN	15	IN	**Buffered Input Pin:** The signal provided to this input pin is buffered to 14 outputs (SDRAM0:13).
SDRAM0:13	38, 37, 35, 34, 32, 31, 29, 28, 21, 20, 18, 17, 40, 41	OUT	**Buffered Outputs:** These fourteen dedicated outputs provide copies of the signal provided at the SDRAMIN input. The swing is set by VDDQ3, and if the CPU clock is used to drive the SDRAMIN then they are deactivated when CPU_STOP# input is set low.
SCLK	24	IN	Clock pin for I^2C Circuitry.
SDATA	23	IN/OUT	Data pin for I^2C Circuitry.
X1	4	IN	**Crystal Connection or External Reference Frequency Input:** This pin has dual functions. It can be used as an external 14.318MHz crystal connection or as an external reference frequency input.
PCI_STOP#/ SDRAM10	18	IN/OUT	**SDRAM10 or PCI_STOP# Pin:** Function determined by MODE pin. The PCI_STOP# input enables the PCI 1:5 outputs when high and causes them to remain at logic 0 when low.
X2	5	IN	**Crystal Connection:** An input connection for an external 14.318MHz crystal. If using an external reference, this pin must be left unconnected.
VDDQ3	1, 6, 14, 19, 27, 30, 36	POWER	**Power Connection:** Power supply for core logic, PLL circuitry, SDRAM outputs, PCI outputs, reference outputs, 48MHz output, and 24MHz output. Connect to 3.3V supply

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Pin Assignments (continued)

Pin Name	Pin Number	Type	Pin Function Description
VDDQ2	42, 48	POWER	**Power Connection:** Power supply for IOAPIC, CPU_F, and CPU1 output buffers. Connect to 2.5V.
GND	3, 9, 16, 22, 33, 39, 45	GROUND	**Ground Connections:** Connect all ground pins to the common system ground plane.

Absolute Maximum Ratings[1]

(beyond which the device will be damaged)

Symbol	Parameter	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
T_A	Operating Temperature	0 to +70	°C
ESD_{PROT}	Input ESD Protection	2 (min)	kV

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

Advanced Information

DC Electrical Characteristics

T_A = 0°C to +70°C; VDDQ3 = 3.3V±5%; VDDQ2 = 2.5V±5%

Parameter			Min.	Typ	Max	Unit	Test Condition
Supply Current							
I_{DD}	3.3V Supply Current			TBD		mA	CPU0:1 = 100Mhz Outputs Loaded[1]
I_{DD}	2.5V Supply Current			TBD		mA	CPU0:1 = 100Mhz Outputs Loaded[1]
Logic Inputs							
V_{IL}	Input Low Voltage		GND -.3		0.8	V	
V_{IH}	Input High Voltage		2.0		VDD +.3	V	
I_{IL}	Input Low Current[2]				-25	µA	
I_{IH}	Input High Current[2]				10	µA	
Clock Outputs							
V_{OL}	Output Low Voltage				0.4	V	I_{OL} = 1mA
V_{OH}	Output High Voltage		2.4			V	I_{OH} = 1mA
V_{OH}	Output High Voltage	CPU0:1, IOAPIC	2.0			V	I_{OH} = -1mA
I_{OL}	Output Low Current:	CPU0:1	27		93	mA	V_{OL} = 1.2V
		IOAPIC	27		93	mA	V_{OL} = 1.2V
		PCI_F, PCI1:5	26.5		139	mA	V_{OL} = 1.4V
		SDRAM0:13	55		152	mA	V_{OL} = 1.4V
		REF0:1	25		76	mA	V_{OL} = 1.4V
		48MHz	25		76	mA	V_{OL} = 1.4V
		24Mhz	25		76	mA	V_{OL} = 1.4V
I_{OH}	Output High Current	CPU_F, CPU1	-101		-26	mA	V_{OH} = 1.2V
		IOAPIC	-101		-26	mA	V_{OH} = 1.2V
		PCI_F, PCI1:5	-189		-31	mA	V_{OH} = 1.4V
		SDRAM0:13	-188		-50	mA	V_{OH} = 1.4V
		REF0:1	-94		-27	mA	V_{OH} = 1.4V
		48MHz	-94		-27	mA	V_{OH} = 1.4V
		24MHz	-94		-27	mA	V_{OH} = 1.4V
Crystal Oscillator							
V_{TH}	X1 Input threshold Voltage (Note 3)			1.65		V	VDDQ3 = 3.3V
$C_{IN,X1}$	X1 Input Capacitance (Note 5)			18		pF	Pin X2 unconnected
Pin Capacitance/Inductance							
C_{IN}	Input Pin Capacitance				5	pF	Except X1 and X2
C_{OUT}	Output Pin Capacitance				6	pF	
L_{IN}	Input Pin Inductance				7	nH	

Notes:

1. All clock outputs loaded with 6" 60 ohm traces with 22pF capacitors.
2. RC7102 logic inputs have internal pull-up devices (pull-ups not full CMOS level).
3. X1 input threshold voltage (typical) is VDD/2.
4. The RC7102 contains an internal crystal load capacitor between pin X1 and ground and another between pin X2 and ground. Total load placed on crystal is 14pF; this includes typical stray capacitance of short PCB traces to crystal.
5. X1 input capacitance is applicable when driving X1 with an external clock source (X2 is left unconnected).

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AC Electrical Characteristics

T_A = 0°C to +70°C; VDDQ3 = 3.3V±5%; VDDQ2 = 2.5V±5%; f_{XTL} = 14.31818MHz

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output; Spread Spectrum clocking is disabled.

CPU Clock Outputs, CPU0:1 (Lump Capacitance Test Load = 20pF)

Parameter		CPU = 66.6MHz			CPU = 100MHz			Units	Test Condition/Comments
		Min.	Typ.	Max.	Min.	Typ.	Max.		
t_P	Period	15		15.5	10		10.5	ns	Measured on rising edge at 1.25.
t_H	High Time	5.2			3.0			ns	Duration of clock cycle above 2.0V.
t_L	Low Time	5.0			2.8			ns	Duration of clock cycle below 0.4V.
t_R	Output Rise Edge Rate	1		4	1		4	V/ns	Measured from 0.4V to 2.0V.
t_F	Output Fall Edge Rate	1		4	1		4	V/ns	Measured from 2.0V to 0.4V.
t_D	Duty Cycle	45		55	45		55	%	Measured on rising and falling edge at 1.25V.
t_{JC}	Jitter, Cycle-to-Cycle			250			250	ps	Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles.
t_{SK}	Output Skew			175			175	ps	Measured on rising edge at 1.25V.
f_{ST}	Frequency Stabilization from Power-up (cold start)			3			3	ms	Assumes full supply voltage reached within 1ms from power-up.
Z_0	AC Output Impedance		20			20		ohm	Average value during switching transition. Used for determining series termination value.

PCI Clock Outputs, PCI_F and PCI_1:5 (Lump Capacitance Test Load = 30pF)

Parameter		CPU = 66.6/ 100MHz			Units	Test Condition/Comments
		Min.	Typ.	Max.		
t_P	Period	30			ns	Measured on rising edge at 1.5V.
t_H	High Time	12.0			ns	Duration of clock cycle above 2.4V.
t_L	Low Time	12.0			ns	Duration of clock cycle below 0.4V.
t_R	Output Rise Edge Rate	1		4	V/ns	Measured from 0.4V to 2.4V.
t_F	Output Fall Edge Rate	1		4	V/ns	Measured from 2.4V to 0.4V.
t_D	Duty Cycle	45		55	%	Measured on rising and falling edge at 1.5V.
t_{JC}	Jitter, Cycle-to-Cycle			500	ps	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.
t_{SK}	Output Skew			500	ps	Measured on rising edge at 1.5V.
t_O	CPU to PCI Clock Skew	1.5		4.0	ns	Covers all CPU/PCI outputs. Measured on rising edge at 1.5V. CPU leads PCI output.
f_{ST}	Frequency Stabilization from Power-up (cold start)				ms	Assumes full supply voltage reached within 1ms from power-up.

PCI Clock Outputs, PCI_F and PCI_1:5 (Lump Capacitance Test Load = 30pF) (continued)

Parameter		CPU = 66.6/ 100MHz			Units	Test Condition/Comments
		Min.	Typ.	Max.		
Z_0	AC Output Impedance		30		ohm	Average value during switching transition. Used for determining series termination value.

IOAPIC Clock Output (Lump Capacitance Test Load = 20pF)

Parameter		CPU = 66.6/ 100MHz			Units	Test Condition/Comments
		Min.	Typ.	Max.		
f	Frequency, Actual		14.3818		MHz	Frequency generated by crystal oscillator.
t_R	Output Rise Edge Rate	1		4	V/ns	Measured from 0.4V to 2.0V.
t_F	Output Fall Edge Rate	1		4	V/ns	Measured from 2.0V to 0.4V.
t_D	Duty Cycle	45		55	%	Measured on rising and falling edge at 1.25V.
f_{ST}	Frequency Stabilization from Power-up (cold start)			1.5	ms	Assumes full supply voltage reached within 1ms from power-up.
Z_0	AC Output Impedance		15		ohm	Average value during switching transition. Used for determining series termination value.

REF0:1 Clock Output (Lump Capacitance Test Load = 20pF)

Parameter		CPU = 66.6/ 100MHz			Units	Test Condition/Comments
		Min.	Typ.	Max.		
f	Frequency, Actual		14.3818		MHz	Frequency generated by crystal oscillator.
t_R	Output Rise Edge Rate	0.5		2	V/ns	Measured from 0.4V to 2.4V.
t_F	Output Fall Edge Rate	0.5		2	V/ns	Measured from 2.4V to 0.4V.
t_D	Duty Cycle	45%		55	%	Measured on rising and falling edge at 1.5V.
f_{ST}	Frequency Stabilization from Power-up (cold start)			3	ms	Assumes full supply voltage reached within 1ms from power-up.
Z_0	AC Output Impedance		40		ohm	Average value during switching transition. Used for determining series termination value.

48MHz Clock Output (Lump Capacitance Test Load = 20pF)

Parameter		CPU = 66.6MHz			Units	Test Condition/Comments
		Min.	Typ.	Max.		
f	Frequency, Actual		48.008		MHz	Determined by PLL divider ratio (see n/m below).
f_D	Deviation from 48MHz		+167		ppm	(48.008 – 48)/48
m/n	PLL Ratio		57/17			(14.31818MHz x 57/17 = 48.008MHz)
t_R	Output Rise Edge Rate	0.5		2	V/ns	Measured from 0.4V to 2.4V.
t_F	Output Fall Edge Rate	0.5		2	V/ns	Measured from 2.4V to 0.4V.
t_D	Duty Cycle	45%		55	%	Measured on rising and falling edge at 1.5V.

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48MHz Clock Output (Lump Capacitance Test Load = 20pF) (continued)

Parameter		CPU = 66.6MHz Min.	Typ.	Max.	Units	Test Condition/Comments
f_{ST}	Frequency Stabilization from Power-up (cold start)			3	ms	Assumes full supply voltage reached within 1ms from power-up.
Z_0	AC Output Impedance		40		ohm	Average value during switching transition. Used for determining series termination value.

24MHz Clock Output (Lump Capacitance Test Load = 20pF)

Parameter		CPU = 66.6MHz Min.	Typ.	Max.	Units	Test Condition/Comments
f	Frequency, Actual		24.004		MHz	Determined by PLL divider ratio (see n/m below).
f_D	Deviation from 24MHz		+167		ppm	(24.004 – 24)/24
m/n	PLL Ratio		57/34			(14.31818MHz x 57/34 = 24.004MHz)
t_R	Output Rise Edge Rate	0.5		2	V/ns	Measured from 0.4V to 2.4V.
t_F	Output Fall Edge Rate	0.5		2	V/ns	Measured from 2.4V to 0.4V.
t_D	Duty Cycle	45%		55	%	Measured on rising and falling edge at 1.5V.
f_{ST}	Frequency Stabilization from Power-up (cold start)			3	ms	Assumes full supply voltage reached within 1ms from power-up.
Z_0	AC Output Impedance		40		ohm	Average value during switching transition. Used for determining series termination value.

SDRAM Clock Outputs, SDRAM0:13 (Lump Capacitance Test Load =30pF)

Parameter		Min.	Typ.	Max.	Units	Test Conditions/Comments
f_{IN}	Input Frequency	0		150	MHz	
t_R	Output Rise Time	0.5		1.33	nS	Measured from 0.4V to 2.4V
t_F	Output Fall Time	0.5		1.33	nS	Measured from 2.4V to 0.4V
t_{SR}	Output Skew, Rising Edge			250	pS	
t_{SF}	Output Skew, Falling Edge			250	pS	
t_{EN}	Output Enable Time	1.0		8.0	nS	
t_{DIS}	Output Disable Time	1.0		8.0	nS	
t_{PR}	Rising Edge Propagation Delay	1.0		5.0	nS	
t_{PF}	Falling Edge Propagation Delay	1.0		5.0	nS	
t_D	Duty Cycle	45		55	%	Measured at 1.5V
Z_O	AC Output Impedance		15		Ω	

Advanced Information

Functional Description

I/O Pin Operation

Pins 7, 17, 18, 25, 26, 46 are dual purpose l/O pins. Upon power up these pins act as logic inputs, allowing the determination of assigned device functions. A short time after power up, the logic state of each pin is latched and the pins become clock outputs. This feature reduces device pin count by combining clock outputs with input select pins.

An external 10k ohm “strapping” resistor is connected between the l/O pin and ground or VDD. Connection to ground sets a latch to "0", connection to VDD sets a latch to "1". Figure 1 and Figure 2 show two suggested methods for strapping resistor connections.

Upon RC7102 power up, the first 2ms of operation is used for input logic selection. During this period, the six I/O pins(7, 17, 18, 25, 26, 46) are tristated, allowing the output strapping resistor on the l/O pins to pull the pin and their associated capacitive clock load to either a logic high or low state. At the end of the 2ms period, the established logic "0" or "1" condition of the l/O pin is latched. Next the output buffer is enabled which converts the l/O pins into operating clock outputs. The 2ms timer is started when VDD reaches 2.0V. The input bits can only be reset by turning VDD off and then back on again.

It should be noted that the strapping resistors have no significant effect on clock output signal integrity. The drive impedance of clock output is <40 ohms (nominal) which is minimally affected by the 10k ohm strap to ground or VDD. As with the series termination resistor, the output strapping resistor should be placed as close to the l/O pin as possible in order to keep the interconnecting trace short. The trace from the resistor to ground or VDD should be kept less than two inches in length to prevent system noise coupling during input logic sampling.

When the clock outputs are enabled following the 2ms input period, the specified output frequency is delivered on the pin, assuming that VDD has stabilized. If VDD has not yet reached full value, output frequency initially may be below target but will increase to target once VDD voltage has stabilized. In either case, a short output clock cycle may be produced from the CPU clock outputs when the outputs are enabled.

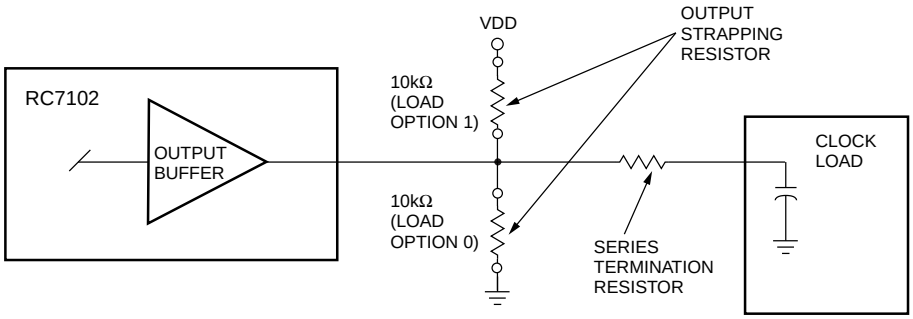

Figure 1. Input Logic Selection through Resistor Load Option

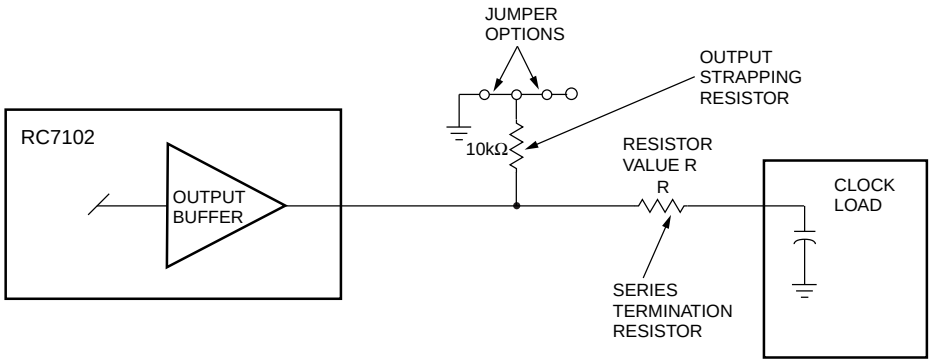

Figure 2. Input Logic Selection through Jumper Option

Advanced Information

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Serial Data Interface

The RC7102 features a two-pin, serial data interface that can be used to configure internal register settings that control particular device functions. Upon power-up, the RC7102 initializes with default register settings, therefore the use of this serial data interface is optional. The serial interface is write-only (to the clock chip) and is the dedicated function of device pins SDATA and SCLOCK. In motherboard applications, SDATA and SCLOCK are typically driven by two logic outputs of the chipset. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions. Table 3 summarizes the control functions of the serial data interface.

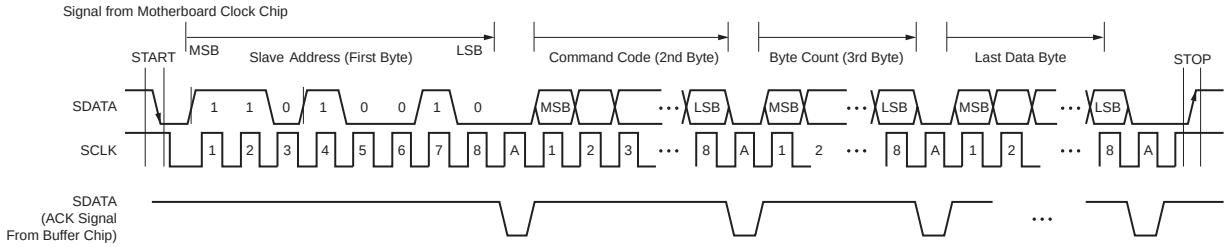
Table 3. Serial Data Interface Control Functions Summary

Control Function	Description	Common Applications
Clock Output Disable	Any individual clock output(s) can be disabled. Disabled outputs are actively held low.	Unused outputs are disabled to reduce EMI and system power. Examples are clock outputs to unused PCI slots.
CPU Clock Frequency Selection	Provides CPU/PCI frequency selections through software. Frequency is changed in a smooth and controlled fashion.	For alternate microprocessors and power management options. Smooth frequency transition allows CPU frequency change under normal system operation.
Spread Spectrum Enabling	Enables or disables spread spectrum clocking.	For EMI reduction.
Output Tristate	Puts clock output into a high impedance state.	Production PCB testing.
(Reserved)	Reserved function for future device revision or production device testing.	No user application. Register bit must be written as 0.
Test Mode	All clock outputs toggle in relation to X1 input, internal PLL is bypassed. Refer to Table 7.	Production PCB Testing

Signaling Requirements for the I²C Serial Port

To initiate communications with the serial port, a start bit is invoked. The start bit is defined as the SDATA line is brought low while the SCLOCK is held high. Once the start bit is initiated, valid data can then be sent. Data is considered to be valid when the clock goes to and remains in the high state. The data can change when the clock goes low. To terminate the transmission, a stop bit is invoked. The stop bit occurs when the SDATA line goes from a low to a high state while the SCLOCK is held high. See Figure below.

RC7104 I²C Interface Write Sequence Example



Note: Once the clock detects the start condition and its ADDRESS is matched, the clock chip will pull down the SDATA at every 8th bit. The 8 bit data from SDATA is latched into the Buffer Chip when the ACK is generated. This ACK signal will continue as long as STOP condition is detected The COMMAND CODE and BYTE COUNT is not used by the Buffer Chip.

Operation

Data is written to the RC7102 in eleven bytes of eight bits each. Bytes are written in the order shown in Table 4.

Table 4. Byte Writing Sequence

Byte Sequence	Byte Name	Bit Sequence	Byte Description
1	Slave Address	11010010	Commands the RC7102 to accept the bits in Data Bytes 0-6 for internal register configuration. Since other devices may exist on the same common serial data bus, it is necessary to have a specific slave address for each potential receiver. The slave receiver address for the RC7102 is 11010010. Register setting will not be made if the Slave Address is not correct (or is for an alternate slave receiver).
2	Command Code	Don't Care	Unused by the RC7102, therefore bit values are ignored (don't care). This byte must be included in the data write sequence to maintain proper byte allocation. The Command Code Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
3	Byte Count	Don't Care	Unused by the RC7102, therefore bit values are ignored (don't care). This byte must be included in the data write sequence to maintain proper byte allocation. The Byte Count Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
4	Data Byte 0	Refer to Table 6	The data bits in Data Bytes 0-7 set internal RC7102 registers that control device operation. The data bits are only accepted when the Address Byte bit sequence is 11010010, as noted above. For description of bit control functions, refer to Table 5, Data Byte Serial Configuration Map.
5	Data Byte 1		
6	Data Byte 2		
7	Data Byte 3		
8	Data Byte 4		
9	Data Byte 5		

Advanced Information

Writing Data Bytes

Each bit in Data Bytes 0-5 control a particular device function except for the "reserved" bits which must be written as a logic 0. Bits are written MSB (most significant bit) first, which is bit 7. Table 5 gives the bit formats for registers located in Data Bytes 0-5.

Table 6 details additional frequency selections that are available through the serial data interface.

Table 7 details the select functions for Byte 0, bits 1 and 0.

Table 5. Data Bytes 0-5 Serial Configuration Map

Bit(s)	Affected Pin		Control Function	Bit Control		Default
	Pin No.	Pin Name		0	1	
Data Byte 0						
7	—	CPU and PCI	Spread Amount - Must equal 1 for Down Spread	± 0.25	± 0.5	0
6	—	—	SEL_2	See Table 6		0
5	—	—	SEL_1	See Table 6		0
4	—	—	SEL_0	See Table 6		0
3	—	—	Hardware/Software Frequency Select	Hardware	Software	0
2	—	CPU and PCI	Spread Type	Center	Down	0
1	7, 8, 10, 11, 12, 13, 43, 44	CPU and PCI	Spread Spectrum Clock	Normal	Spread	0
0	All Clocks	All Clocks	Clock Output Tristate	Active	Tristate	0
Data Byte 1						
7	—	—	(Reserved)	—	—	1
6	—	—	(Reserved)	—	—	1
5	—	—	(Reserved)	—	—	1
4	—	—	Test Mode	see Table 7		1
3	40	SDRAM12	Clock Output Disable	Low	Active	1
2	41	SDRAM13	Clock Output Disable	Low	Active	1
1	43	CPU1	Clock Output Disable	Low	Active	1
0	44	CPU0	Clock Output Disable	Low	Active	1
Data Byte 2						
7	—	—	(Reserved)	—	—	1
6	7	PCI_F	Clock Output Disable	Low	Active	1
5	—	—	(Reserved)	—	—	1
4	13	PCI5	Clock Output Disable	Low	Active	1
3	12	PCI4	Clock Output Disable	Low	Active	1
2	11	PCI3	Clock Output Disable	Low	Active	1
1	10	PCI2	Clock Output Disable	Low	Active	1
0	8	PCI1	Clock Output Disable	Low	Active	1

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Table 5. Data Bytes 0-5 Serial Configuration Map (continued)

Bit(s)	Affected Pin		Control Function	Bit Control		Default
	Pin No.	Pin Name		0	1	
Data Byte 3						
7	—	—	(Reserved)	—	—	1
6	—	—	(Reserved)	—	—	1
5	26	48Mhz	Clock Output Disable	Low	Active	1
4	25	24MHz	Clock Output Disable	Low	Active	1
3	—	—	(Reserved)	—	—	1
2	21, 20, 18, 17	SDRAM8:11	Clock Output Disable (SDRAM 10, 11 only when MODE=1)	Low	Active	1
1	32, 31, 29, 28	SDRAM4:7	Clock Output Disable	Low	Active	1
0	38, 37, 35, 34	SDRAM0:3	Clock Output Disable	Low	Active	1
Data Byte 4						
7	—	—	(Reserved)	—	—	1
6	—	—	(Reserved)	—	—	1
5	—	—	(Reserved)	—	—	1
4	—	—	(Reserved)	—	—	1
3	—	—	(Reserved)	—	—	1
2	—	—	(Reserved)	—	—	1
1	—	—	(Reserved)	—	—	1
0	—	—	(Reserved)	—	—	1
Data Byte 5						
7	—	—	(Reserved)	—	—	1
6	—	—	(Reserved)	—	—	1
5	—	—	(Reserved)	—	—	1
4	47	IOAPIC	Clock Output Disable	Low	Active	1
3	—	—	(Reserved)	—	—	1
2	—	—	(Reserved)	—	—	1
1	46	REF1	Clock Output Disable	Low	Active	1
0	2	REF0	Clock Output Disable	Low	Active	1

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Table 6. Additional Frequency Selections through Serial Data Interface Data Bytes

Input Conditions			Output Frequency	
Data Byte 0, Bit 3 = 1				
Bit 6 SEL_2	Bit 5 SEL_1	Bit 4 SEL_0	CPU, SDRAM Clocks (MHz)	PCI Clocks (MHz)
1	1	1	100. 2	33.4
1	1	0	133.3	44.4
1	0	1	112	37.3
1	0	0	103	34.3
0	1	1	66.8	33.4
0	1	0	83.3	41.65
0	0	1	75	37.5
0	0	0	124	41.3

Table 7. Test Mode

	Input Conditions	Output Frequency				
	Data Byte 1					
Function	Bit 4	CPU0:1	PCI_F, PCI1:5	REF, IOAPIC	48MHz	24MHz
Normal Operation	1	Note 1	Note 1	14.318 MHz	48 MHz	24 MHz
Test Mode	0	X1/2	CPU/2 or 3	X1	X1/2	X1/4

Note 1: CPU and PCI frequency selections are listed in Table 2 and Table 6.

Advanced Information

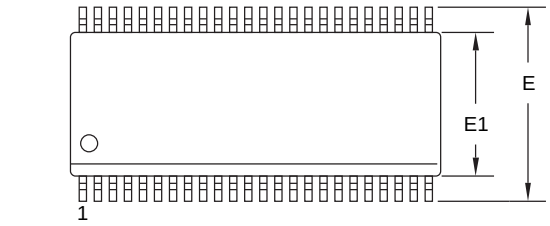
Mechanical Dimensions

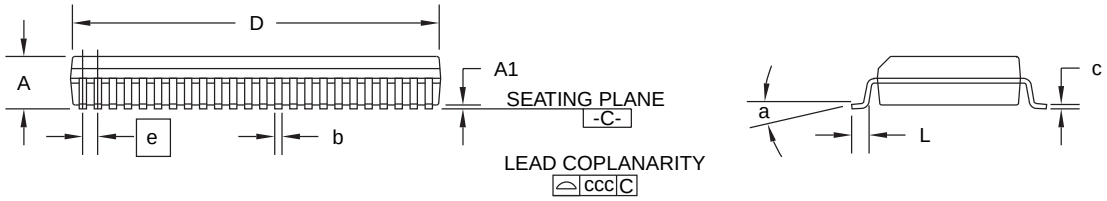
48 pin SSOP

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.095	.110	2.41	2.79	
A1	.008	.016	0.20	0.41	
b	.008	.0135	0.20	0.34	5
c	.005	.010	0.13	0.25	5
D	.620	.630	15.75	16.00	2, 4
E	.395	.420	10.03	10.67	
E1	.291	.299	7.39	7.59	2
e	.025 BSC		0.64 BSC		
L	.020	.040	0.51	1.02	3
N	48		48		6
a	0°	8°	0°	8°	
ccc	---	.004	---	0.13	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
2. "D" and "E1" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "b" & "c" dimensions include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.





Advanced Information

Ordering Information

Product Number	Temperature	Screening	Package	Package Marking
RC7102			48 SSOP	RC7102

Advanced Information

RC7104

100MHz Spread Spectrum Motherboard Clock

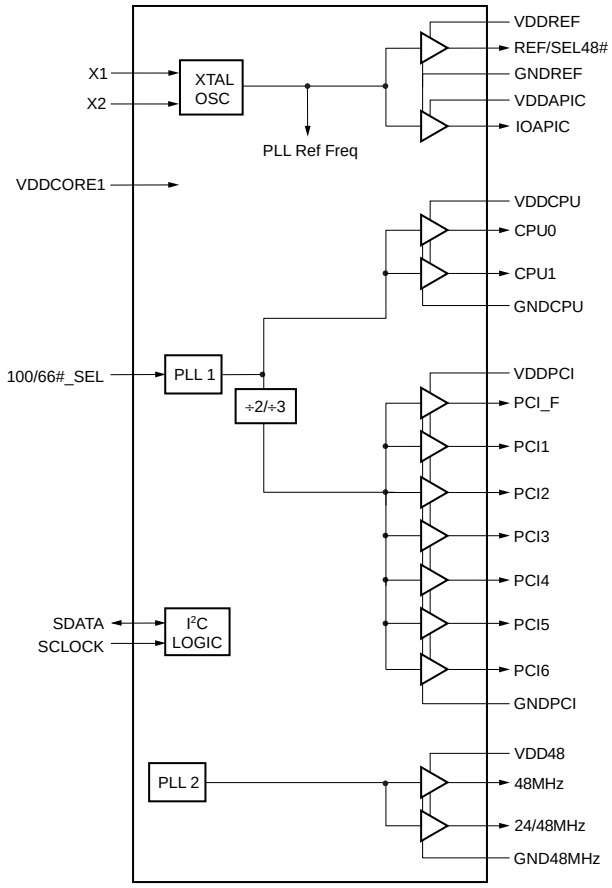
Features

- Employs Fairchild's proprietary Spread Spectrum Technology
- Reduces measured EMI by as much as 10dB
- I^2C programmable
- Two skew-controlled copies of CPU clock
- SEL100/66# selects CPU frequency (100 or 66.8MHz)
- Overclocking up to 133MHz
- Seven copies of PCI clock (synchronous w/CPU clock)
- One copy of 14.31818 MHz IOAPIC clock
- One copy of 48MHz USB clock
- 24 or 48MHz clock is determined by resistor straps on power up
- One copy of 14.31818MHz REF clock

Description

The RC7104 is a clock synthesizer for Pentium II based motherboard systems. The CPU output frequency can be "over driven" through a command to the serial I^2C interface.

Block Diagram



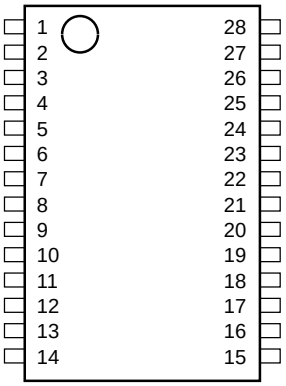
Advanced Information

Rev. 0.0.9

Table 1. Pin Selectable Frequency

SEL100/66	CPU(0:1)	PCI
1	100MHz	33.3MHz
0	66.8MHz	33.4MHz

Pin Assignments



Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	X1	8	PCI4	15	GND48	22	CPU0
2	X2	9	VDDPCI	16	SEL100/66#	23	VDDCPU
3	GNDPCI	10	PCI5	17	SCLOCK	24	IOAPIC
4	PCIF	11	PCI6	18	SDATA	25	VDDAPIC
5	PCI1	12	VDD48	19	GNDCPU	26	VDDREF
6	PCI2	13	48MHz	20	VDDCORE1	27	REF/SEL48#
7	PCI3	14	24/48MHz	21	CPU1	28	GNDREF

Advanced Information

Pin Descriptions

Pin Name	Pin Number	Type	Pin Function Description
CPU0:1	22, 21	OUT	**CPU Clock Outputs 0 through 1:** These two CPU clocks run at a frequency set by SEL100/66# and the I^2C bus.
PCI_F PCI1:6	4, 5, 6, 7, 8, 10, 11	OUT	**PCI Bus Clock Outputs 1 through 6 and PCI_F:** These seven PCI clock outputs run synchronously to the CPU clock.
IOAPIC	24	OUT	**I/O APIC Clock Output:** Provides 14.318MHz fixed frequency.
48MHz	13	OUT	**48MHz Output:** Fixed 48MHz USB clock.
24/48MHz	14	OUT	**24MHz or 48MHz Output:** Frequency is set by the state of pin 27 on power up.
REF/SEL48#	27	IN/OUT	**I/O Dual Function REF and SEL48# pin:** Upon power-up, the state of SEL48# is latched. The initial state is set by either a 10K resistor to GND or to VDD. A 10K resistor to GND causes pin 14 to output 48MHz. If the pin is strapped to VDD, pin 14 will output 24MHz. After 2ms, the pin becomes a high drive output that produces a copy of 14.318MHz.
SEL100/66#	16	IN	**Frequency Selection Input:** Selects CPU clock frequency as shown in Table 1.
SDATA	18	IN/OUT	**I^2C Data Pin:** Data should be presented to this input as described in the I^2C section of this data sheet. Internal 250K ohm pull-up resistor.
SCLOCK	17	IN	**I^2C clock Pin:** The I^2C Data clock should be presented to this input as described in the I^2C section of this data sheet.
X1	1	IN	**Crystal Connection or External Reference Frequency Input:** Connect to either a 14.318MHz crystal or other reference signal.
X2	2	IN	**Crystal Connection:** An input connection for an external 14.318MHz crystal. If using an external reference, this pin must be left unconnected.
VDDCORE1	20	POWER	**Power Connection:** Power supply for core logic and PLL circuitry. Connect to 3.3V supply.
VDDPCI	9	POWER	**Power Connection:** Power supply for PCI_F and PCI1:6. Connect to 3.3V supply.
VDDAPIC	25	POWER	**Power Connection:** Power supply for IOAPIC output buffer. Connect to 2.5V supply.
VDDCPU	23	POWER	**Power Connection:** Power supply for CPU0:1 output buffers. Connect to 2.5V supply.
VDD48	12	POWER	**Power Connection:** Power supply for 48MHz USB clock. Connect to 3.3V supply.
VDDREF	26	POWER	**Power Connection:** Power supply for 14.318MHz ISA clock. Connect to 3.3V supply.
GNDPCI, GND48, GND-CPU, GNDREF	3, 15, 19, 28	GROUND	**Ground Connections:** Connect all ground pins to the common system ground plane.

Advanced Information

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Symbol	Parameter	Rating	Units
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
T_A	Operating Temperature	0 to +70	°C
V_{ESD}	Input ESD Protection	2 (min)	kV

Advanced Information

DC Electrical Characteristics

T_A = 0°C to +70°C; VDDREF = VDDPCI = VDD48MHz = 3.3V±5%; VDDAPIC = VDDCPU = 2.5V±5%

Parameter		Test Condition	Min.	Typ.	Max.	Units
Supply Current						
I_{DD}	Combined 3.3V Supply Current	CPUCLK = 100MHz Outputs Loaded[1]				mA
Logic inputs						
V_{IL}	Input Low Voltage		GND -.3		0.8	V
V_{IH}	Input High Voltage		2.0		VDD+.3	V
I_{IL}	Input Low Current[2]				-25	µA
I_{IH}	Input High Current[2]				10	µA
I_{IL}	Input Low Current (SEL100/66#)				-5	µA
I_{IH}	Input High Current (SEL100/66#)				+5	µA
Clock Outputs						
V_{OL}	Output Low Voltage	I_{OL} = 1mA			0.4	mV
V_{OH}	Output High Voltage CPU0, IOAPIC	I_{OH} = 1mA	2			V
	PCI, REF, 24MHz		2.4			
I_{OL}	Output Low Current CPU, IOAPIC	V_{OL} = 1.2V	27		93	mA
	PCI	V_{OL} = 1.4V	26.5		139	
	REF, 48MHz, 24MHz		25		76	
I_{OH}	Output High Current CPU, IOAPIC	V_{OH} = 1.2V	-101		-26	mA
	PCI	V_{OH} = 1.4V	-189		-31	
	REF, 48MHz, 24MHz		-94		-27	
Crystal oscillator						
V_{TH}	X1 Input threshold Voltage[3]			1.5		V
$C_{IN, X1}$	X1 Input Capacitance[5]	Pin X2 unconnected	13.5	18	22.5	pF
Pin Capacitance/Inductance						
C_{IN}	Input Pin Capacitance	Except X1 and X2			5	pF
C_{OUT}	Output Pin Capacitance				6	pF
L_{IN}	Input Pin Inductance				7	nH

Notes:

1. All clock outputs loaded with maximum lump capacitance test load specified in AC Electrical Characteristics section.
2. RC7104 logic inputs have internal pull-up resistors, except SEL100/66#.
3. X1 input threshold voltage (typical) is VDD/2.
4. The RC7104 contains an internal crystal load capacitor between pin X1 and ground and another between pin X2 and ground. Total load placed on crystal is 14pF; this includes typical stray capacitance of short PCB traces to crystal.
5. X1 input capacitance is applicable when driven X1 with an external clock source (X2 is left unconnected).

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AC Electrical Characteristics

T_A = 0°C to +70°C; VDDREF = VDDPCI = VDD48MHz = 3.3V±5%; VDDAPIC = VDDCPU = 2.5V±5%; f_{XTL} = 14.31818MHz

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output; Spread Spectrum clocking is disabled

CPU Clock Outputs, CPU0:1 (Lump Capacitance Test Load = 20pF)

Parameter		CPU = 66.6MHz			CPU = 100MHz			Units	Test Condition/Comments
		Min.	Typ.	Max.	Min.	Typ.	Max.		
t_P	Period	15		15.5	10		10.5	ns	Measured on rising edge at 1.25.
t_H	High Time	5.2			3.0			ns	Duration of clock cycle above 2.0V.
t_L	Low Time	5.0			2.8			ns	Duration of clock cycle below 0.4V.
t_R	Output Rise Edge Rate	.4		1.6	.4		1.6	ns	Measured from 0.4V to 2.0V.
t_F	Output Fall Edge Rate	.4		1.6	.4		1.6	ns	Measured from 2.0V to 0.4V.
t_D	Duty Cycle	45		55	45		55	%	Measured on rising and falling edge at 1.25V.
t_{JC}	Jitter, Cycle-to-Cycle			200			200	ps	Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles.
t_{SK}	Output Skew			175			175	ps	Measured on rising edge at 1.25V.
f_{ST}	Frequency Stabilization from Power-up (cold start)			3			3	ms	Assumes full supply voltage reached within 1ms from power-up.
Z_0	AC Output Impedance		20			20		Ω	Average value during switching transition. Used for determining series termination value.

PCI Clock Outputs, PCI1:6 and PCI_F (Lump Capacitance Test Load = 30pF)

Parameter		CPU = 66.6/100MHz			Units	Test Condition/Comments
		Min.	Typ.	Max.		
t_P	Period	30			ns	Measured on rising edge at 1.5V.
t_H	High Time	12.0			ns	Duration of clock cycle above 2.4V.
t_L	Low Time	12.0			ns	Duration of clock cycle below 0.4V.
t_R	Output Rise Edge Rate	1		4	V/ns	Measured from 0.4V to 2.4V.
t_F	Output Fall Edge Rate	1		4	V/ns	Measured from 2.4V to 0.4V.
t_D	Duty Cycle	45		55	%	Measured on rising and falling edge at 1.5V.
t_{JC}	Jitter, Cycle-to-Cycle			250	ps	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.
t_{SK}	Output Skew			500	ps	Measured on rising edge at 1.5V.
t_O	CPU to PCI Clock Offset	1.5		4.0	ns	Covers all CPU/PCI outputs. Measured on rising edge at 1.5V. CPU leads PCI output.

PCI Clock Outputs, PCI1:6 and PCI_F (Lump Capacitance Test Load = 30pF) (continued)

Parameter		CPU = 66.6/100MHz Min.	Typ.	Max.	Units	Test Condition/Comments
f_{ST}	Frequency Stabilization from Power-up (cold start)			3	ms	Assumes full supply voltage reached within 1ms from power-up.
Z_0	AC Output Impedance		30		Ω	Average value during switching transition. Used for determining series termination value.

IOAPIC Clock Output (Lump Capacitance Test Load = 20pF)

Parameter		CPU = 66.6/100MHz Min.	Typ.	Max.	Units	Test Condition/Comments
f	Frequency, Actual		14.3818		MHz	Frequency generated by crystal oscillator.
t_R	Output Rise Edge Rate	1		4	V/ns	Measured from 0.4V to 2.0V.
t_F	Output Fall Edge Rate	1		4	V/ns	Measured from 2.0V to 0.4V.
t_D	Duty Cycle	45		55	%	Measured on rising and falling edge at 1.25V.
t_A	Jitter, Absolute			500	ps	Measured on rising edge at 1.25V. Maximum deviation of clock period.
f_{ST}	Frequency Stabilization from Power-up (cold start)			1.5	ms	Assumes full supply voltage reached within 1ms from power-up.
Z_0	AC Output Impedance		20		Ω	Average value during switching transition. Used for determining series termination value.

REF Clock Output (Lump Capacitance Test Load = 20pF)

Parameter		CPU = 66.6/100MHz Min.	Typ.	Max.	Units	Test Condition/Comments
f	Frequency, Actual		14.3818		MHz	Determined by PLL divider ratio (see n/m below).
t_R	Output Rise Edge Rate	0.5		2	V/ns	Measured from 0.4V to 2.4V.
t_F	Output Fall Edge Rate	0.5		2	V/ns	Measured from 2.4V to 0.4V.
t_D	Duty Cycle	45%		55	%	Measured on rising and falling edge at 1.5V.
t_{JC}	Jitter, Cycle-to-Cycle			500	ps	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.
f_{ST}	Frequency Stabilization from Power-up (cold start)			3	ms	Assumes full supply voltage reached within 1ms from power-up.
Z_0	AC Output Impedance		20		Ω	Average value during switching transition. Used for determining series termination value.

Advanced Information

48MHz and 24MHz Clock Output (Lump Capacitance Test Load = 20pF=66.6/100MHz)

Parameter		CPU = 66.6MHz			Units	Test Condition/Comments
		Min.	Typ.	Max.		
f	Frequency, Actual		48.008 24.004		MHz	Determined by PLL divider ratio (see n/m below).
f_D	Deviation from 48MHz		+167		ppm	(48.008 – 48)/48
n/m	PLL Ratio		57/17			(14.31818MHz x 57/17 = 48.008MHz)
t_R	Output Rise Edge Rate	0.5		2	V/ns	Measured from 0.4V to 2.4V.
t_F	Output Fall Edge Rate	0.5		2	V/ns	Measured from 2.4V to 0.4V.
t_D	Duty Cycle	45%		55	%	Measured on rising and falling edge at 1.5V.
t_{JC}	Jitter, Cycle-to-Cycle			500	ps	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.
f_{ST}	Frequency Stabilization from Power-up (cold start)			3	ms	Assumes full supply voltage reached within 1ms from power-up.
Z_0	AC Output Impedance		20		ohm	Average value during switching transition. Used for determining series termination value.

Advanced Information

Functional Description

I/O Pin Operation

Pin 27 is a dual purpose l/O pin. The RC7104 upon power up, the first 2ms of operation is used for input logic selection, (allowing the determination of assigned device functions).

During this period, the 48MHz clock output buffer is tristated, allowing the output strapping resistor on the l/O pin to pull the pin and its associated capacitive clock load to either a logic high or low state. At the end of the 2ms period, the established logic "0" or "1" condition of the l/O pin is then latched. Next the output buffer is enabled which converts the l/O pin into an operating clock output. The 2ms timer is started when VDD reaches 2.0V. The input bits can only be re-set by turning VDD off and then back on again. (This feature reduces device pin count by combining clock outputs with input select pins.)

It should be noted that the strapping resistors have no significant effect on clock output signal integrity. The drive impedance of clock output is 20 ohms (nominal) which is minimally affected by the 10 kohm strap to ground or VDD. As with the series termination resistor, the output strapping resistor should be placed as close to the l/O pin as possible in order to keep the interconnecting trace short. The trace from the resistor to ground or VDD should be kept less than two inches in length to prevent system noise coupling during input logic sampling.

An external 10 kohm "strapping" resistor is connected between the l/O pin and ground or VDD. Connection to ground sets a "0" bit, connection to VDD sets a "1" bit. Figure 1 and Figure 2 show two suggested methods for strapping resistor connections.

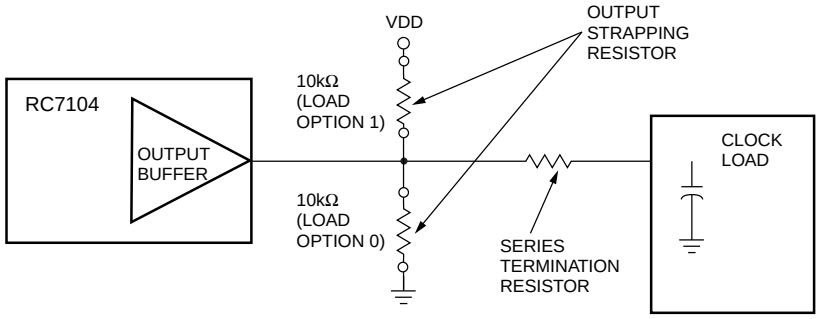


Figure 1. Input Logic Selection through Resistor Load Option

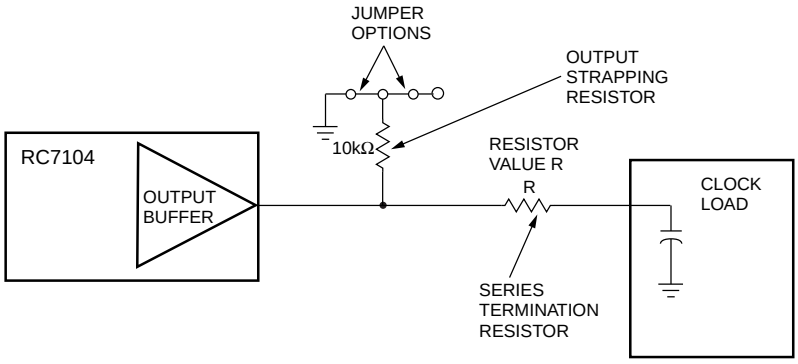


Figure 2. Input Logic Selection through Jumper Option

Serial Data Interface

The RC7104 features a two-pin, serial data interface that can be used to configure internal register settings that control particular device functions. Upon power-up, the RC7104 initializes with default register settings. Therefore, the use of this serial data interface is optional. The serial interface is write-only (to the clock chip) and is the dedicated function of device pins SDATA and SCLOCK. In motherboard applications, SDATA and SCLOCK are typically driven by two logic outputs of the chipset.

Advanced Information

Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions. Table 2 summarizes the control functions of the serial data interface.

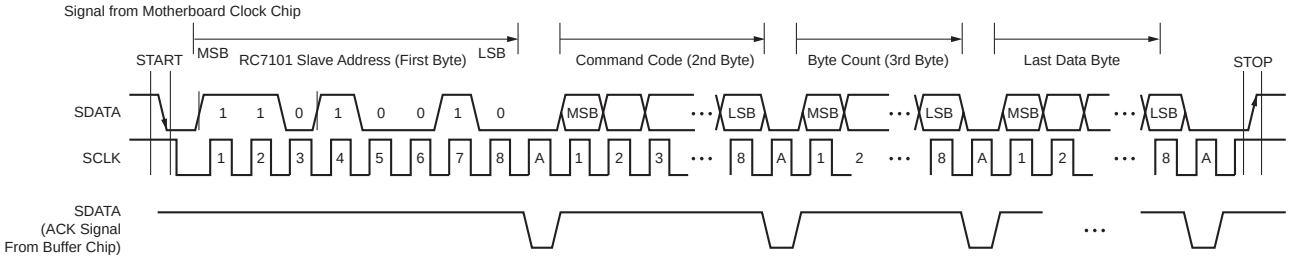
Table 2. Serial Data Interface Control Functions Summary

Control Function	Description	Common Application
Clock Output Disable	Any individual clock output(s) can be disabled. Disabled outputs are actively held low.	Unused outputs are disabled to reduce EMI and system power. Examples are clock outputs to unused PCI slots.
CPU Clock Frequency Selection	Provides CPU/PCI frequency selections beyond the 100 and 66.66MHz selections that are provided by the SEL100/66# pin. Frequency is changed in a smooth and controlled fashion.	For alternate microprocessors and power management options. Smooth frequency transition allows CPU frequency change under normal system operation.
Output Tristate	Puts all clock outputs into a high impedance state.	Production PCB testing.
Test Mode	All clock outputs toggle in relation to X1 input, internal PLL is bypassed. Refer to Table 4.	Production PCB testing.
(Reserved)	Reserved function for future device revision or production device testing.	No user application. Register bit must be written as 0.

Signaling Requirements for the I²C Serial Port

To initiate communications with the serial port, a start bit is invoked. The start bit is defined as the SDATA line is brought low while the SCLOCK is held high. Once the start bit is initiated, valid data can then be sent. Data is considered to be valid when the clock goes to and remains in the high state. The data can change when the clock goes low. To terminate the transmission, a stop bit is invoked. The stop bit occurs when the SDATA line goes from a low to a high state while the SCLOCK is held high. See Figure below.

RC7104 I²C Interface Write Sequence Example



Note: Once the clock detects the start condition and its ADDRESS is matched, the clock chip will pull down the SDATA at every 8th bit. The 8 bit data from SDATA is latched into the Buffer Chip when the ACK is generated. This ACK signal will continue as long as STOP condition is detected The COMMAND CODE and BYTE COUNT is not used by the Buffer Chip.

The data transfer rate is 100kbits/s in the standard mode and 400kbits/s in the fast mode. The serial protocol uses block writes only. Bytes are written with the lowest first and the highest last with the ability to stop after any complete byte has been transferred. The clock driver is a slave/receiver only and is only capable of receiving data with the exception of sending acknowledgements. It is not capable of sending data.

Operation

The RC7104 is programmed by writing 10 bytes of eight bits each. See Table 3 for byte order.

Table 3. Byte Writing Sequence

Byte Sequence	Byte Name	Bit Sequence	Byte Description
1	Slave Address	11010010	Commands the RC7104 to accept the bits in Data Bytes 3-6 for internal register configuration. Since other devices may exist on the same common serial data bus, it is necessary to have a specific slave address for each potential receiver. The slave receiver address for the RC7104 is 11010010. Register setting will not be made if the Slave Address is not correct (or is for an alternate slave receiver).
2	Command Code	Don' t Care	Unused by the RC7104, therefore bit values are ignored (don' t care). This byte must be included in the data write sequence to maintain proper byte allocation. The Command Code Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
3	Byte Count	Don't Care	Unused by the RC7104, therefore bit values are ignored (don' t care). This byte must be included in the data write sequence to maintain proper byte allocation. The Byte Count Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
4	Data Byte 0	Don' t Care	Refer to Fairchild SDRAM Buffers. These bytes are not used by the RC7104.
5	Data Byte 1		
6	Data Byte 2		
7	Data Byte 3	Refer to Table 5	The data bits in these bytes set internal RC7104 registers that control device operation. The data bits are only accepted when the Address Byte bit sequence is 11010010, as noted above. For description of bit control functions, refer to Table 4, Data Byte Serial Configuration Map.
8	Data Byte 4		
9	Data Byte 5		
10	Data Byte 6		

Advanced Information

Writing Data Bytes

Each bit of the 10 data bytes controls a particular device function except for the "reserved" bits. These must by preserved by writing a logic 0. Bit 7, the MSB, is written first. See Table 4 for bit descriptions of Data Bytes 3–6.

Table 5 shows additional frequency selections that are programmable via the serial data interface.

Table 7 shows the mode select functions for Byte 3, bits 1 and 0.

Table 4. Data Bytes 3-6 Serial Configuration Map

Bit(s)	Affected Pin		Control Function		Bit Control		Default
	Pin No.	Pin Name			0	1	
Data Byte 3							
7	—	—	(Reserved)		—	—	0
6	—	—	SEL_2		Refer to Table 5		0
5	—	—	SEL_1		Refer to Table 5		0
4	—	—	SEL_0		Refer to Table 5		0
3	—		BYT0 _FS#		Frequency Controlled by external SEL100/ 66# pin	Frequency Controlled by BYT0 SEL (2:0)	0
2	—		(Reserved)				0
1-0	—	—	Bit 1	Bit 0	Function (See Table 7 for function details)		00
			0	0	Normal Operation		
			0	1	Test Mode		
			1	0	Spread Spectrum on (See Table 6 for frequency & spread selections, when Spread Spectrum is on. See Table 5 for frequency selections when Spread Spectrum is off).		
			1	1	All Outputs Tristated		
Data Byte 4							
7	—	—	(Reserved)		—	—	0
6	14	24/48MHz	Clock Output disable		Low	Active	1
5	—	—	(Reserved)		—	—	0
4	—	—	(Reserved)		—	—	0
3	—	—	(Reserved)		—	—	0
2	21	CPU1	Clock Output disable		Low	Active	1
1	—	—	(Reserved)		—	—	0
0	22	CPU0	Clock Output disable		Low	Active	1
Data Byte 5							
7	4	PCICLK_F	Clock Output disable		Low	Active	1
6	11	PCI6	Clock Output disable		Low	Active	1
5	10	PCI5	Clock Output disable		Low	Active	1
4	—	—	(Reserved)		—	—	0
3	8	PCI4	Clock Output disable		Low	Active	1
2	7	PCI3	Clock Output disable		Low	Active	1
1	6	PCI2	Clock Output disable		Low	Active	1
0	5	PCI1	Clock Output disable		Low	Active	1

Table 4. Data Bytes 3-6 Serial Configuration Map (continued)

Bit(s)	Affected Pin		Control Function	Bit Control		Default
	Pin No.	Pin Name		0	1	
Data Byte 6						
7	—	—	(Reserved)	—	—	0
6	—	—	(Reserved)	—	—	0
5	24	IOAPIC	Clock Output disable	Low	Active	1
4	—	—	(Reserved)	—	—	0
3	—	—	(Reserved)	—	—	0
2	—	—	(Reserved)	—	—	0
1	27	REF	Clock Output disable	Low	Active	1
0	—	—	(Reserved)	—	—	0

Table 5. Additional Frequency Selections through Serial Data Interface Data Bytes when Spread Spectrum is turned off

Input Conditions			Output Frequency	
Data Byte 3, Bit 3 = 1				
Bit 6 SEL_2	Bit 5 SEL_1	Bit 4 SEL_0	CPU, SDRAM Clocks (MHz)	PCI Clocks (MHz)
0	0	0	124.3	62.2
0	0	1	75.2	37.6
0	1	0	83.5	41.8
0	1	1	66.8	33.4
1	0	0	103.2	34.4
1	0	1	112.3	37.4
1	1	0	133.6	44.5
1	1	1	100.2	33.4

Table 6. Additional Frequency Selections through Serial Data Interface Data Bytes when Spread Spectrum is turned on

Input Conditions			Output Frequency		
Data Byte 3, Bit 3 = 1					
Bit 6 SEL_2	Bit 5 SEL_1	Bit 4 SEL_0	CPU, SDRAM Clocks (MHz)	PCI Clocks (MHz)	Spread Percentage
0	0	0	124	41.3	±0.25% Center
0	0	1	75	37.5	±0.25% Center
0	1	0	83.3	41.6	±0.25% Center
0	1	1	66.8	33.4	±0.25% Center
1	0	0	103	34.25	±0.25% Center
1	0	1	112	33.3	±0.25% Center
1	1	0	133.3	44.43	±0.25% Center
1	1	1	100	33.3	±0.25% Center

Advanced Information

Table 7. Select Function for Data Byte 3, Bits 0:1

Function	Input Conditions		Output Frequency				
	Data Byte 3						
	Bit 1	Bit 0	CPU0:1	PCI_F, PCI1:6	REF, IOAPIC	48MHz	24MHz
Normal Operation	0	0	[1]	[1]	14.318MHz	48MHz	24MHz
Test Mode	0	1	X1/2	CPU/2 or 3	X1	X1/2	X1/4
Spread Spectrum	1	0	±0.5%	±0.5%	14.318MHz	48MHz	24MHz
Tristate	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

Notes:

1. CPU and PCI frequency selections are listed in Table 1 and Table 5.

Advanced Information

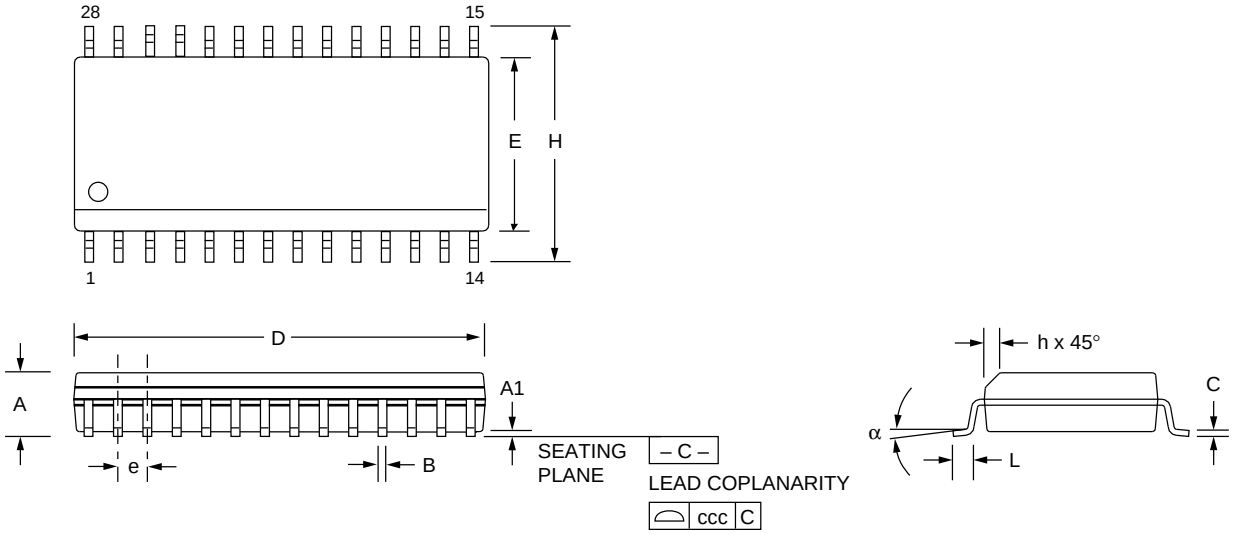
Mechanical Dimensions

28 pin SOIC

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	
D	.697	.713	17.70	18.10	2
E	.291	.299	7.40	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.030	0.25	0.75	
L	.016	.050	0.40	1.27	
N	28		28		5
α	0°	7°	0°	7°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. Symbol "N" is the maximum number of terminals.



Advanced Information

Ordering Information

Product Number	Temperature	Screening	Package	Package Marking
RC7104			28 SOIC	RC7104

Advanced Information

RC7105

Clock Buffer/Driver

Features

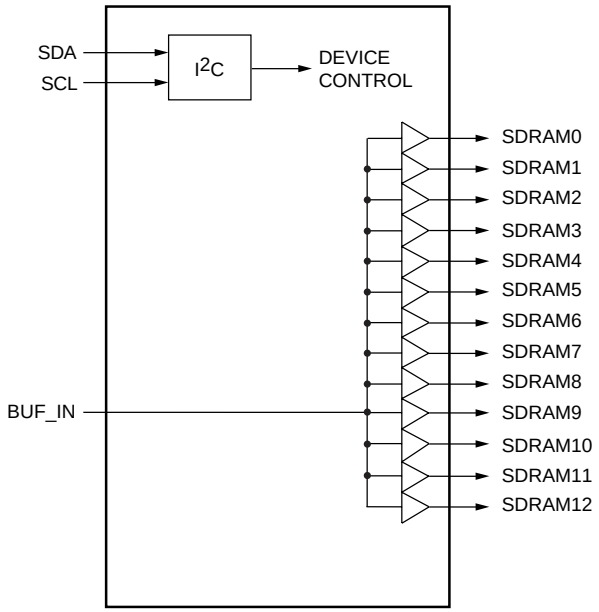
- Thirteen skew controlled CMOS clock outputs (SDRAM0:12)
- Drives three SDRAM DIMMs
- I^2C interface
- Clock Skew between any two outputs is less than 250 ps
- 1 to 5ns propagation delay
- DC to 133MHz operation
- Single 3.3V supply voltage
- Low power CMOS design in a 28-pin, SOIC package

Description

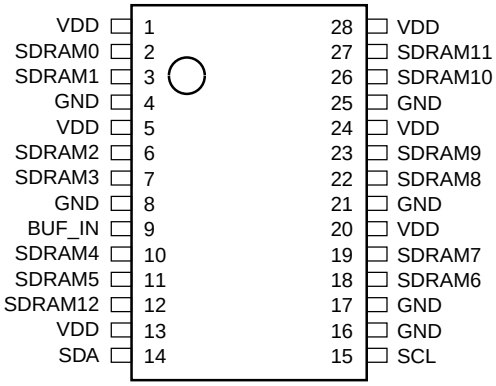
The Fairchild RC7105 is a low-voltage, thirteen-output clock buffer. The skew between any two outputs is less than 250 ps and the buffers can be individually enabled or disabled by programming via the I^2C serial interface. Output buffer impedance is approximately 15Ω which is ideal for driving SDRAM DIMMs.

Advanced Information

Block Diagram



Pin Assignments



Pin Descriptions

Pin Name	Pin Number	Type	Pin Function Description
SDRAM0:12	2, 3, 6, 7, 10, 11, 18, 19, 22, 23, 26, 27, 12	OUT	**SDRAM Outputs:** Provides buffered copy of BUF_IN. The propagation delay from a rising input edge to a rising output edge is 1 to 5ns. All outputs are skew controlled to within ±250ps of each other.
BUF_IN	9	IN	**Clock Input:** This clock input has an input threshold voltage of 1.5V (typ).
SDA	14	IN/OUT	**I^2C Data input:** Data should be presented to this input as described in the I^2C section of this data sheet.
SCL	15	IN	**I^2C clock input:** The I^2C clock should be presented to this input as described in the I^2C section of this data sheet.
VDD	1, 5, 13, 20, 24, 28	POWER	**Power Connection:** Power supply for core logic and output buffers. Connected to 3.3V supply.
GND	4, 8, 16, 17, 21, 25	GROUND	**Ground Connection:** Connect all ground pins to the common system ground plane.

Advanced Information

Absolute Maximum Ratings[1]

(beyond which the device will be damaged)

Symbol	Parameter	Min.	Units
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	-0.5 to +7.0	V
T_{STG}	Storage Temperature	-65 to +150	°C
T_B	Ambient Temperature under Bias	-55 to +125	°C
T_A	Operating Temperature	0 to +70	°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

DC Electrical Characteristics

T_A = 0°C to +70°C; V_{DD} = 3.3V±5%

Parameter		Test Condition	Min.	Typ.	Max.	Units
Supply Current						
I_{DD}	3.3V Supply Current	BUF_IN = 100MHZ			250	mA
Logic Input						
V_{IL}	Input Low Voltage		GND -0.3		0.8	V
V_{IH}	Input High Voltage		2.0		VDD+.5	V
I_{ILEAK}	Input Leakage Current, BUF_IN		-5		+5	µA
I_{ILEAK}	Input Leakage Current (Note)		-20		+5	µA
Logic Outputs (SDRAM0:12)						
V_{OL}	Output Low Voltage	I_{OL} = 1mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = 1mA	2.4			V
I_{OL}	Output Low Current	V_{OL} = 1.4V	55		159	mA
I_{OH}	Output High Current	V_{OH} = 1.4V	-188		-50	mA
Pin Capacitance/Inductance						
C_{IN}	Input Pin Capacitance				5	pF
C_{OUT}	Output Pin Capacitance				6	pF
L_{IN}	Input Pin Inductance				7	nH

Note: SDA and SCL logic pins have an internal pull-up resistor.

Advanced Information

AC Electrical Characteristics

T_A = 0°C to +70°C; V_{DD} = 3.3V±5%; (Lump Capacitance Test Load = 30pF)

Parameter		Min.	Typ.	Max.	Units	Test Condition/Comments
f_{IN}	Input Frequency	0		133	MHz	
t_R	Output Rise Time	0.5		1.33	ns	Measured from 0.4V to 2.4V
t_F	Output Fall Time	0.5		1.33	ns	Measured from 2.4V to 0.4V
t_{SR}	Output Skew, Rising Edges			250	ps	
t_{SF}	Output Skew, Falling Edges			250	ps	
t_{EN}	Output Enable Time	1.0		8.0	ns	
t_{DIS}	Output Disable Time	1.0		8.0	ns	
t_{PR}	Rising Edge Propagation Delay	1.0		5.0	ns	
f_{PF}	Falling Edge Propagation Delay	1.0		5.0	ns	
t_D	Duty Cycle	45		55	%	Measured at 1.5V
Z_0	AC Output Impedance		15		Ω	Average value during switching transition. Used for determining series termination value.

Advanced Information

How To Use the Serial Data Interface

Electrical Requirements

Figure 1 shows the architecture for the I^2C serial interface bus used with the RC7105. Devices on the bus signal with an open drain logic output that actively pulls the bus line low, or lets the bus default to VDD (logic 1). The pull-up resistor on each bus line, SCL and SDA, establishes a default logic 1.

Although the RC7105 is a slave device which cannot write data on the bus, it does transmit an “acknowledge” data pulse after each byte is received. Thus, the SDA line is an I/O pin.

The pull-up resistor value should be designed to meet the rise and fall times specified in AC parameters, based on total bus line capacitance.

Signaling Requirements

As demonstrated in Figure 2, the I^2C protocol defines valid data bits as stable logic 0 or 1 condition on the SDA line during an SCL high (logic 1) pulse. A transitioning SDA line during an SCL high pulse may be read as a start or stop pulse.

Figure 3 shows how a “start bit” commands the beginning of a write sequence. The “stop bit” shown signifies that the sequence has ended. The RC7105 sends an “acknowledge” pulse after receiving eight data bits by asserting a low pulse on SDA, as shown in Figure 4.

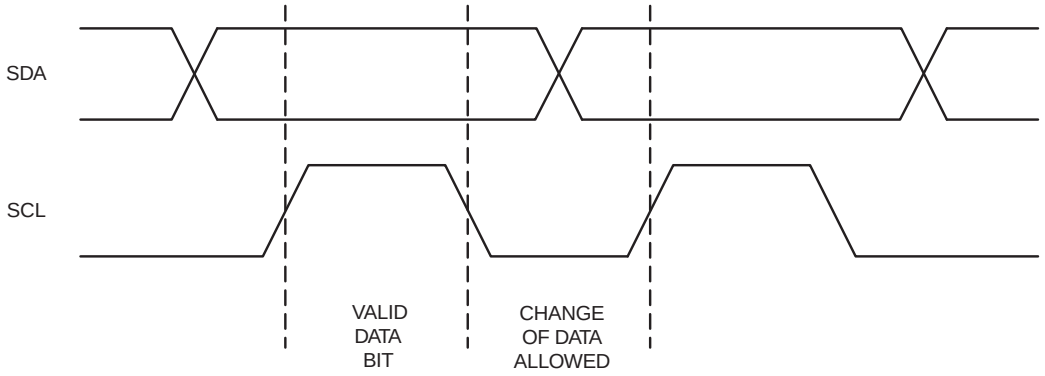


Figure 2. Serial Data Bus Valid Data Bit

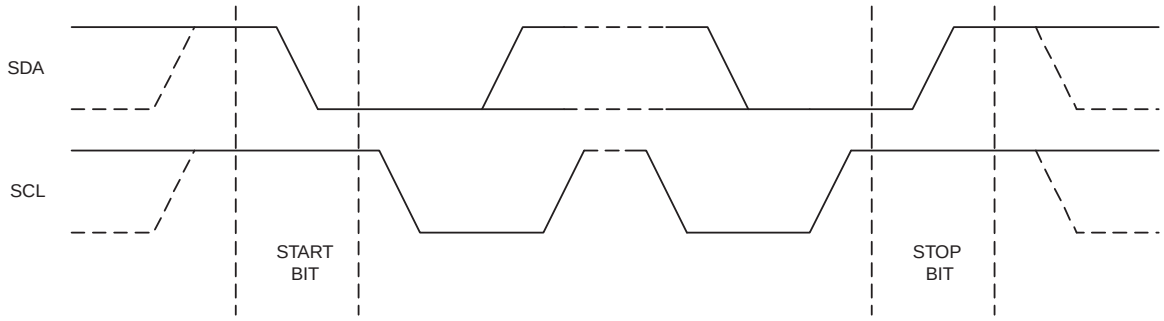


Figure 3. Serial Data Bus Start and Stop Bit

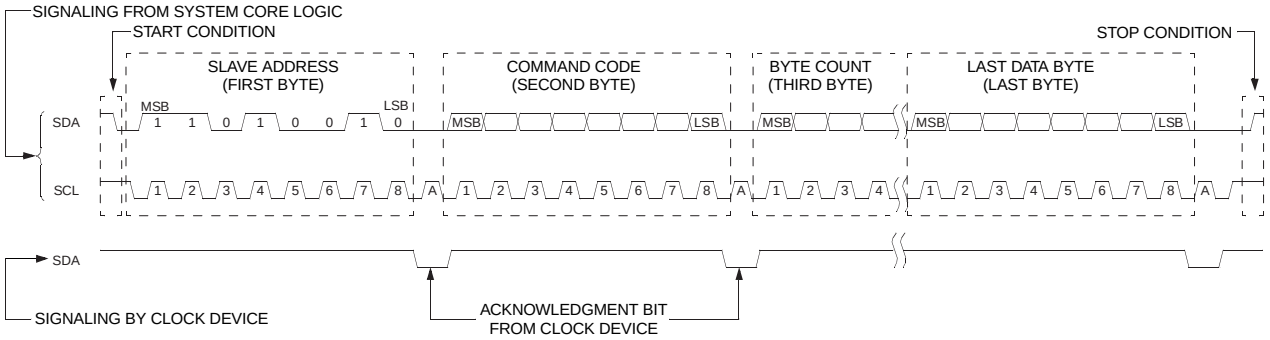


Figure 4. Serial Data Bus Write Sequence

Advanced Information

Functional Description

Output Drivers

The RC7105 uses CMOS type output buffers which drive the output rail-to-rail (GND to VDD) into typical capacitive loads. Because of this the outputs are both TTL and CMOS level compatible. Nominal output buffer impedance is 15Ω.

Operation

The RC7105 is programmed by writing ten bytes of eight bits each. See Table 1 for byte sequence.

Table 1. Byte Writing Sequence

Byte Sequence	Byte Name	Bit Sequence	Byte Description
1	Slave Address	11010010	Commands the RC7105 to accept the bits in Data Bytes 0-6 for internal register configuration. Since other devices may exist on the same common serial data bus, it is necessary to have a specific slave address for each potential receiver. The slave receiver address for the RC7105 is 11010010. Register setting will not be made if the Slave Address is not correct (or is for an alternate slave receiver).
2	Command Code	Don't Care	Unused by the RC7105, therefore bit values are ignored (don't care). This byte must be included in the data write sequence to maintain proper byte allocation. The Command Code Byte is part of the standard serial communication protocol and may be used when writing ot another addressed slave receiver on the serial data bus.
3	Byte Count	Don't Care	Unused by the RC7105, therefore bit values are ignored (don' t care). This byte must be included in the data write sequence to maintain proper byte allocation. The Byte Count Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
4	Data Byte 0	Refer to Table 2	The data bits in these bytes set internal RC7105 registers that control device operation. The data bits are only accepted when the Address Byte bit sequence is 11010010, as noted above. For description of bit control functions, refer to Table 2, Data Byte Serial Configuration Map.
5	Data Byte 1		
6	Data Byte 2		
7	Data Byte 3	Don't Care	Refer to Fairchild clock drivers.
8	Data Byte 4		
9	Data Byte 5		
10	Data Byte 6		

Advanced Information

Advanced Information

Writing Data Bytes

Each bit of the 10 data bytes controls a particular device function within the RC7105. Bit 7, the MSB, is written first. See Table 2 for bit descriptions of Data Bytes 0–2.

Table 2. Data Bytes 0-2 Serial Configuration Map

Bit(s)	Affected Pin		Control Function	Bit Control	
	Pin No.	Pin Name		0	1
Data Byte 0 SDRAM Active/Inactive Register (1=Enable, 0=Disable)					
7	11	SDRAM5	Clock Output Disable	Low	Active
6	10	SDRAM4	Clock Output Disable	Low	Active
5	N/A	Reserved	(Reserved)	—	—
4	N/A	Reserved	(Reserved)	—	—
3	7	SDRAM3	Clock Output Disable	Low	Active
2	6	SDRAM2	Clock Output Disable	Low	Active
1	3	SDRAM1	Clock Output Disable	Low	Active
0	2	SDRAM0	Clock Output Disable	Low	Active
Data Byte 1 SDRAM Active/Inactive Register (1=Enable, 0=Disable)					
7	27	SDRAM11	Clock Output Disable	Low	Active
6	26	SDRAM10	Clock Output Disable	Low	Active
5	23	SDRAM9	Clock Output Disable	Low	Active
4	22	SDRAM8	Clock Output Disable	Low	Active
3	N/A	Reserved	(Reserved)	—	—
2	N/A	Reserved	(Reserved)	—	—
1	19	SDRAM7	Clock Output Disable	Low	Active
0	18	SDRAM6	Clock Output Disable	Low	Active
Data Byte 2 SDRAM Active/Inactive Register (1=Enable, 0=Disable)					
7	N/A	Reserved	(Reserved)	—	—
6	12	SDRAM12	Clock Output Disable	Low	Active
5	N/A	Reserved	(Reserved)	—	—
4	N/A	Reserved	(Reserved)	—	—
3	N/A	Reserved	(Reserved)	—	—
2	N/A	Reserved	(Reserved)	—	—
1	N/A	Reserved	(Reserved)	—	—
0	N/A	Reserved	(Reserved)	—	—

Note:
At power up all SDRAM outputs are enabled and active. Program all reserved bits to a”0”.

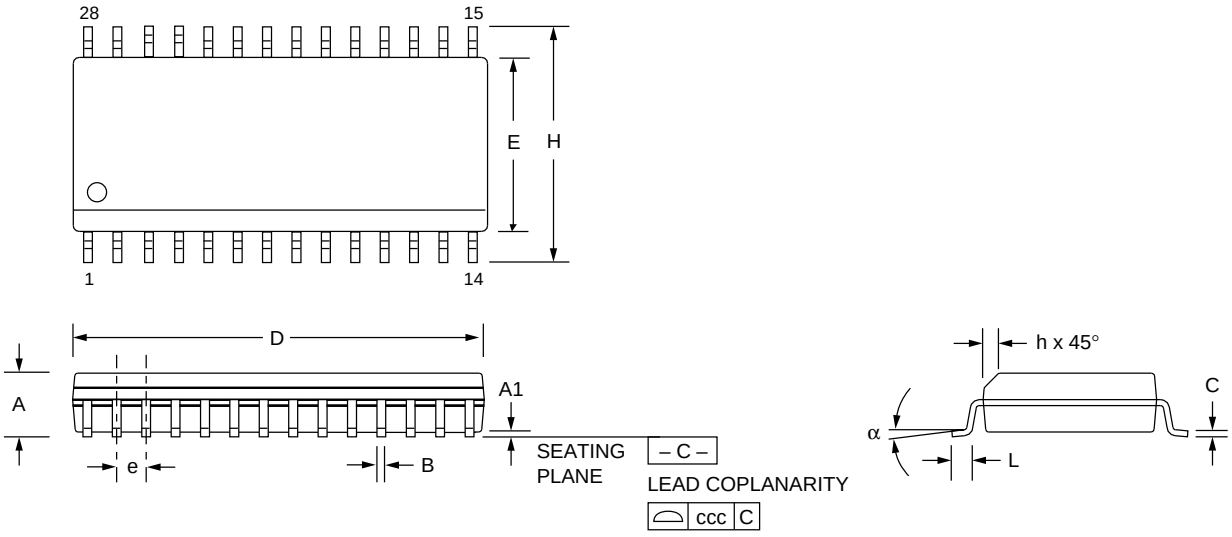
Mechanical Dimensions

28 pin SOIC

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	
D	.697	.713	17.70	18.10	2
E	.291	.299	7.40	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.030	0.25	0.75	
L	.016	.050	0.40	1.27	
N	28		28		5
α	0°	7°	0°	7°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. Symbol "N" is the maximum number of terminals.



Advanced Information

Ordering Information

Product Number	Temperature	Screening	Package	Package Marking
RC7105	0°C to +70°C		28 SOIC	RC7105

Advanced Information

RC7106

133MHz Spread Spectrum Clock for Motherboards

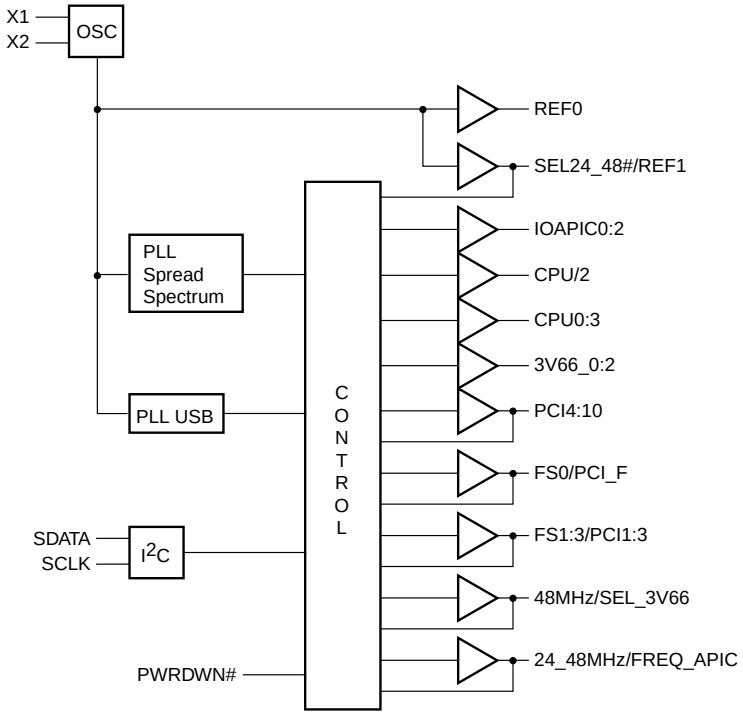
Features

- Employs Fairchild's proprietary Spread Spectrum Technology
- Reduces measured EMI by as much as 10dB
- Supports up to 150MHz
- I^2C programmable
- Three skew-controlled copies of the CPU clock
- One copy CPU/2 @ 3.3V
- Three copies of 3V66 clock
- One copy 24MHz or 48MHz clock
- One copy 48MHz clock
- Three copies IOAPIC
- Two copies REF 14.318MHz clock (3.3V)
- Eleven copies PCI clock
- Power down capability

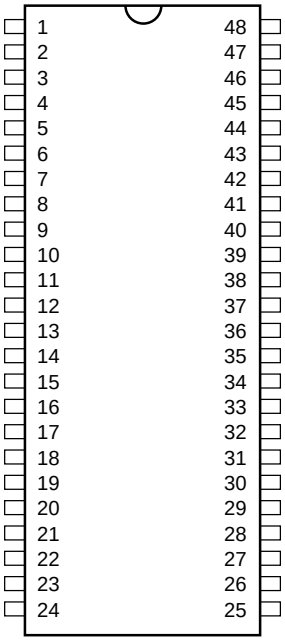
Description

The RC7106 is a clock synthesizer for motherboard applications. It meets the requirements for 133MHz Camino chipset. The clock frequencies can be set with the 4 select pins or be set via the I^2C interface.

Block Diagram



Pin Assignments



48 SSOP

Pin Assignments

Pin #	Pin Name	Pin #	Pin name	Pin #	Pin Name
1	VSS	17	PCI6	33	3V66-1
2	REF0	18	PCI7	34	3V66-0
3	SEL24_48#/REF1	19	VSS	35	VDD
4	VDD	20	PCI8	36	VSSL
5	X1	21	PCI9	37	CPU2
6	X2	22	PCI10	38	CPU1
7	VSS	23	VDD	39	VDDL
8	FS0/PCI_F	24	PWRDWN#	40	CPU0
9	FS1/PCI1	25	VSS	41	VSSL
10	VDD	26	24_48MHz/FREQ_APIC	42	CPU/2
11	FS2/PCI2	27	48MHz/SEL_3V66	43	VDDL
12	FS3/PCI3	28	VDD	44	IOAPIC2
13	VSS	29	SCLK	45	VSSL
14	PCI4	30	SDATA	46	IOAPIC1
15	PCI5	31	VSS	47	IOAPIC0
16	VDD	32	3V66-2	48	VDDL

PWRDWN#

PWRDWN#	CPU	SDRAM	IOAPIC	3V66	PCI	REF, 24MHz, 48MHz	OSC.	PLL
0	LOW	LOW	LOW	LOW	LOW	LOW	OFF	OFF
1	ON	ON	ON	ON	ON	ON	ON	ON

Frequency Selection

FS3	FS2	FS1	FS0	CPU MHz	CPU/2 MHz	PCI MHz	3V66 (MHz)		IOAPIC (MHz)	
							3V66_SYNC = 0	3V66_SYNC = 1	FREQ_APIC = 0	FREQ_APIC = 1
0	0	0	0	105	52.5	35	70	70	17.5	35
0	0	0	1	75	37.5	37.5	64*	75	18.75	37.5
0	0	1	0	100.3	50.15	33.4	66.6	66.6	16.7	33.4
0	0	1	1	66.8	33.4	33.4	66.6	66.6	16.67	33.4
0	1	0	0	110	55	36.6	64*	73.3	18.3	36.6
0	1	0	1	115	57.5	38.3	64*	76.6	19.16	38.3
0	1	1	0	117	58.5	39	64*	78	19.5	39
0	1	1	1	120	60	40	64*	80	20	40
1	0	0	0	125	62.5	41.6	64*	83.3	20.8	41.6
1	0	0	1	127	63.5	42.3	64*	84.6	21.16	42.3
1	0	1	0	133.3	66.5	33.3	66.6	66.6	16.6	33.3
1	0	1	1	135	67.5	33.75	67.5	67.5	16.8	33.75
1	1	0	0	137	68.5	34.25	68.5	68.5	17.125	34.25
1	1	0	1	140	70	35	70	70	17.5	35
1	1	1	0	145	72.5	36.25	64*	72.5	18.125	36.25
1	1	1	1	150	75	37.5	64*	75	18.75	37.5

***Note:** These output frequencies are not synchronous to the CPU Clock and do not have Spread Spectrum modulation.

Pin Descriptions

Pin Name	Pin Number	Type	Pin Function Description
CPU0:2	40,38,37	OUT	CPU Clock Outputs: The frequency of these three CPU clocks are determined by the 4 select pins FS0:3 or via the I^2C interface.
CPU/2	42	OUT	CPU/2 Clock Output: The frequency of this clock is determined by the 4 select pins FS0:3 or via the I^2C interface.
PCI4:10	14,15,17,18, 20,21,22	OUT	PCI BUS Clock Outputs: These seven PCI clock outputs run synchronously to the CPU.
FS0/PCI_F	8	IN/OUT	I/O Dual Function FS0 and PCI_F pin: See table for frequency selection. After power-on, this pin becomes a free-running PCI clock.
FS1:3/ PCI1:3	9,11,12	IN/OUT	I/O Dual Function FS1:3 and PCI1:3 pin: See table for frequency selection. After power-on, these pins become normal PCI clock.
3V66-0:2	34,33,32	OUT	3V66 Clock Outputs: See table for frequency selection
REF0	1	OUT	REF Clock Output: This output provides a 14.318MHz high drive clock .
SEL24_48#/ REF1	3	IN/OUT	I/O Dual Function SEL24_48# and REF1 Pin: During power-up, if the input is “0”, 48MHz would be selected on pin 26. If the input is latched “1”, 24MHz would be selected. After power-on, this pin becomes a REF1 output. There is an internal pull-up resistor on this pin.
IOAPIC0:2	47,46,44	OUT	IOAPIC Clock Outputs: See table for frequency selection.
24_48MHz/ FREQ_APIC	26	OUT/IN	I/O Dual Function 24_48MHz and Freq_APIC pin: See table for frequency selection. After power-on the pin becomes a normal 24MHz or 48MHz clock depending on pin 3 during power-up.
48MHz/ SEL_3V66	27	OUT/IN	I/O Dual Function 48MHz and FS3 pin: See table for frequency selection. After power-on the pin becomes a normal 48MHz clock.
X1	5	IN	Crystal Connection: An input connection for an external14.318MHz crystal. Connect to either a 14.318MHz crystal or other reference signal.
X2	6	OUT	Crystal Connection: If using an external reference, this pin must be left unconnected.
PWRDWN#	24	IN	Power-down Input pin: This pin shuts down the clock PLL bring all clocks to a low state.
SCLK	29	IN	I^2C Clock Pin: The I^2C clock should be applied to this input as described in the I^2C section of this datasheet.
SDATA	30	IN/OUT	I^2C Data Pin: Data should be presented to this input as described by the I^2C section of this datasheet. There is an internal pull-up resistor on this pin.
VDD	4,10,16,23, 28,35	POWER	3.3V Power Pins:
VDDL	39,43,48	POWER	2.5V Power Pins:
VSS	1,7,13,19,25, 31,36,41,45	POWER	Ground Pins:

Functional Description

I/O Pin Operation

Dual Purpose I/O pins such as pin 8 FS0/PCI_F, act as a logic input upon power up. This allows the determination of assigned device function. For this example, FS0 along with the other three select pins will determine the clock frequencies as shown in the table. A short time after power up, the logic state is latched and the pin becomes a clock output pin. In this case, pin 8 becomes a PCI free-running clock output. This feature reduces device pin count by combining clock outputs with input select pins.

An external 10kohm “strapping” resistor is connected between the I/O pin and VDD or VSS (ground). A connection to ground sets a “0” bit and a connection to VDD sets a “1” bit. See Figure 1.

Upon power up, the first 2mS of operation is used for input logic selection. The clock output pins are tri-stated, allowing the output strapping resistor on the I/O pin to pull the pin and its associated capacitive clock load to either a logic high or low state. At the end of the 2mS period, the established logic “0” or “1” condition of the I/O pin is then latched. Next the output buffer is enabled which converts the I/O pin into an operating clock output. The 2mS timer is started when VDD reaches 2.0V. The input bits can only be reset by turning the VDD off and then back on again.

It should be noted that the strapping resistors have no significant effect on clock output signal integrity. The drive impedance of clock output is 20 ohms (nominal) which is minimally affected by the 10kohm strap to ground or VDD. As with the series termination resistor, the output strapping resistor should be placed as close to the I/O pin as possible in order to keep the interconnecting trace short. The trace from the resistor to ground or VDD should be kept less than two inches in length to prevent system noise coupling during input logic sampling.

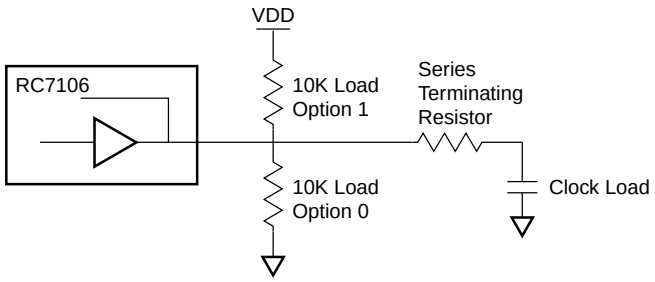


Figure 1. Input Logic Selection through Resistor Load Option

Serial Data Interface

The RC7106 features a two-pin, serial data interface that can be used to configure internal register settings that control particular device functions. Upon power-up, the RC7106 initializes with default register settings. Therefore, the use of this serial data interface is optional. The serial interface is write-only (to the clock chip) and is the dedicated function of device pins SDATA and SCLK. In motherboard applications, SDATA and SCLK are typically driven by two logic outputs of the chipset. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions. Table 2 summarizes the control functions of the serial data interface.

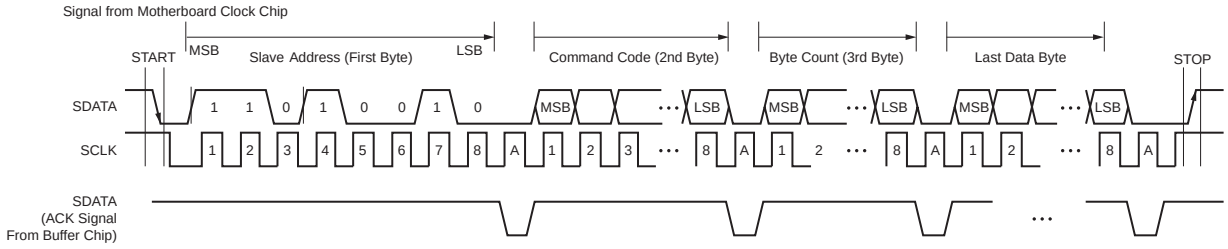
Table 2. Serial Data Interface Control Functions Summary

Control Function	Description	Common Application
Clock Output Disable	Any individual clock output(s) can be disabled. Disabled outputs are actively held low.	Unused outputs are disabled to reduce EMI and system power. Examples are clock outputs to unused PCI slots.
CPU Clock Frequency Selection	Provides CPU/PCI frequency selections beyond the 133MHz provided upon power-on. Frequency is changed in a smooth and controlled fashion.	For alternate microprocessors and power management options. Smooth frequency transition allows CPU frequency change under normal system operation.
Output Tristate	Puts all clock outputs into a high impedance state.	Production PCB testing.
Test Mode	All clock outputs toggle in relation to X1 input, internal PLL is bypassed. Refer to Table 4.	Production PCB testing.
Reserved	Reserved function for future device revision or production device testing.	No user application. Register bit must be written as 0.

Signaling Requirements for the I^{2}C Serial Port

To initiate communications with the serial port, a start bit is invoked. The start bit is defined as the SDATA line is brought low while the SCLOCK is held high. Once the start bit is initiated, valid data can then be sent. Data is considered to be valid when the clock goes to and remains in the high state. The data can change when the clock goes low. To terminate the transmission, a stop bit is invoked. The stop bit occurs when the SDATA line goes from a low to a high state while the SCLOCK is held high. See Figure below.

RC7106 I^{2}C Interface Write Sequence Example



Note: Once the clock detects the start condition and its ADDRESS is matched, the clock chip will pull down the SDATA at every 8th bit. The 8 bit data from SDATA is latched into the Buffer Chip when the ACK is generated. This ACK signal will continue as long as STOP condition is detected The COMMAND CODE and BYTE COUNT is not used by the Buffer Chip.

Operation

The RC7106 is programmed by writing 10 bytes of eight bits each. See Table 3 for byte order.

Table 3. Byte Writing Sequence

Byte Sequence	Byte Name	Bit Sequence	Byte Description
1	Slave Address	11010010	Commands the RC7106 to accept the bits in Data Bytes 3-6 for internal register configuration. Since other devices may exist on the same common serial data bus, it is necessary to have a specific slave address for each potential receiver. The slave receiver address for the RC7106 is 11010010. Register setting will not be made if the Slave Address is not correct (or is for an alternate slave receiver).
2	Command Code	Don't Care	Unused by the RC7106, therefore bit values are ignored (don't care). This byte must be included in the data write sequence to maintain proper byte allocation. The Command Code Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
3	Byte Count	Don't Care	Unused by the RC7106, therefore bit values are ignored (don't care). This byte must be included in the data write sequence to maintain proper byte allocation. The Byte Count Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
4	Data Byte 0	Refer to Table 5	The data bits in these bytes set internal RC7106 registers that control device operation. The data bits are only accepted when the Address Byte bit sequence is 11010010, as noted above. For description of bit control functions, refer to Table 4, Data Byte Serial Configuration Map.
5	Data Byte 1		
6	Data Byte 2		
7	Data Byte 3		
8	Data Byte 4		
9	Data Byte 5		
10	Data Byte 6		

Writing Data Bytes

Each bit of the 10 data bytes controls a particular device function except for the “reserved bits”. These must be preserved by writing a logic 0. Bit 7, the MSB, is written first. See Table 4 for bit descriptions of Data Bytes 1-4.

Table 5 shows additional frequency selections that are programmable via the serial data interface.

Table 7 shows the mode select functions for Byte 3, bits 1 and 0.

Table 4. Data Bytes 1-4 Serial Configuration Map

Bit(s)	Affected Pin		Control Function	Bit Control		Default
	Pin No.	Pin Name		0	1	
Data Byte 1						
7	40	CPU0	Clock Output Disable	Disable	Enable	1
6	38	CPU1	Clock Output Disable	Disable	Enable	1
5	37	CPU2	Clock Output Disable	Disable	Enable	1
4	42	CPU/2	Clock Output Disable	Disable	Enable	1
3	47	IOAPIC0	Clock Output Disable	Disable	Enable	1
2	46	IOAPIC1	Clock Output Disable	Disable	Enable	1
1	2	REF0	Clock Output Disable	Disable	Enable	1
0	3	REF1	Clock Output Disable	Disable	Enable	1
Data Byte 2						
7	18	PCI7	Clock Output Disable	Disable	Enable	1
6	17	PCI6	Clock Output Disable	Disable	Enable	1
5	15	PCI5	Clock Output Disable	Disable	Enable	1
4	14	PCI4	Clock Output Disable	Disable	Enable	1
3	12	PCI3	Clock Output Disable	Disable	Enable	1
2	11	PCI2	Clock Output Disable	Disable	Enable	1
1	9	PCI1	Clock Output Disable	Disable	Enable	1
0	8	PCI_F	Clock Output Disable	Disable	Enable	1
Data Byte 3						
7	34	3V66_0	Clock Output Disable	Disable	Enable	1
6	33	3V66_1	Clock Output Disable	Disable	Enable	1
5	32	3V66_2	Clock Output Disable	Disable	Enable	1
4	-	-	(Reserved)	-	-	0
3	-	-	(Reserved)	-	-	0
2	-	-	(Reserved)	-	-	0
1	-	-	(Reserved)	-	-	0
0	-	-	(Reserved)	-	-	0
Data Byte 4						
7	26	24_48MHz	Clock Output Disable	Disable	Enable	1
6	27	48MHz	Clock Output Disable	Disable	Enable	1
5	-	-	(Reserved)	-	-	0
4	22	PCI10	Clock Output Disable	Disable	Enable	1
3	21	PCI9	Clock Output Disable	Disable	Enable	1
2	20	PCI8	Clock Output Disable	Disable	Enable	1
1	-	-	(Reserved)	-	-	0
0	-	-	(Reserved)	-	-	0

Table 5. Byte 0: Functionality and frequency select register (Default = 0)

Bit	Description							Default
Bit 7	0- ±0.25% Center Spread Spectrum							0
	1- Down Spread Spectrum 0 to							
Bit (2, 6:4)				3V66		IOAPIC		Note 1
	Bit(2,6:4)	CPU	PCI	3V66_SEL =0	3V66_SEL =1	FREQ_APIC =0	FREQ_APIC =1	
	0000	105	35	70	70	17.5	35	
	0001	75	37.5	64*	75	18.75	37.5	
	0010	100.3	33.4	66.6	66.6	16.7	33.4	
	0011	66.8	33.4	66.6	66.6	16.67	33.4	
	0100	110	36.6	64*	73.3	18.3	36.6	
	0101	115	38.3	64*	76.6	19.16	38.3	
	0110	117	39	64*	78	19.5	39	
	0111	120	40	64*	80	20	40	
	1000	125	41.6	64*	83.3	20.8	41.6	
	1001	127	42.3	64*	84.6	21.16	42.3	
	1010	133.3	33.3	66.6	66.6	16.6	33.3	
	1011	135	33.75	67.5	67.5	16.8	33.75	
	1100	137	34.25	68.5	68.5	17.125	34.25	
	1101	140	35	70	70	17.5	35	
	1110	145	36.25	64*	72.5	18.125	36.25	
	1111	150	37.5	64*	75	18.75	37.5	
Bit 3	0- frequency is selected by hardware select, latched inputs 1- Frequency is selected by Bit 2,6:4							0
Bit 1	0- Normal 1- Spread Spectrum							0
Bit 0	0- Enabled 1- Tristate all outputs							0

Note 1: Default at power-up will be for latched logic inputs to define frequency, Bit 2, 6:4 are defaulted to 0000.
*These output frequencies are not synchronous to the CPU Clock and do not have Spread Spectrum modulation.

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Symbol	Parameter	Ratings	Units
V_{DD}, V_{IN}	Voltage on any pin with respect to V_{SS}	-0.5 to +7.0	V
T_{STG}	Storage Temperature	-65 to +150	^{o}C
T_B	Ambient Temperature	-55 to +125	^{o}C
T_A	Operating Temperature	0 to +70	^{o}C
ESD_{PROT}	Input ESD Protection	2 (min)	kV

DC Electrical Characteristics

T_A = 0°C to +70°C; VDD = 3.3V±5%; VDDL = 2.5V±5%

Parameter		Test Condition	Min.	Typ.	Max.	Units
Supply Current						
IDD3	Combined 3.3V Supply Current	CPU = 133MHz Outputs Loaded		TBD		mA
IDD2	Combined 2.5V Supply Current	CPU = 133MHz Outputs Loaded		TBD		mA
Logic Inputs						
V_{IL}	Input Low Voltage		VSS-0.3		0.8	V
V_{IH}	Input High Voltage		2.0		VDD+0.3	V
I_{IL}	Input Low Current[1]				-25	µA
I_{IH}	Input High Current[1]				10	µA
I_{IL}	Input Low Current				-5	µA
I_{IH}	Input High Current				5	µA
Clock Outputs[2]						
V_{OL}	Output Low Voltage	I_{OL}=1mA			0.4	V
V_{OH}	Output High Voltage CPU, CPU/2 and IOAPIC	I_{OH}=-1mA	2.0			V
	PCI, 3V66, 24MHz,48MHz,REF		2.4			
I_{OL}	Output Low Current CPU, CPU/2	V_{OL}=1.2V	27		93	mA
	PCI, 3V66	V_{OL}=1.4V	26.5		139	
	REF, 24MHz,48MHz		25		76	
I_{OH}	Output High Current CPU and CPU/2	V_{OH}=1.4V	-101		-26	mA
	PCI and 3V66	V_{OH}=1.4V	-189		-31	
	REF, 24MHz,48MHz		-94		-27	
Crystal Oscillator						
V_{TH}	X1 Input Threshold Voltage	VDD=3.3V		1.5		V
C_{IN}	X1 Input Capacitance[5]	X2 unconnected		18		pF
Pin Capacitance/Inductance						
C_{IN}	Input Pin Capacitance	Except X1 and X2			5	pF
C_{OUT}	Output Pin Capacitance				6	pF
L_{IN}	Input Pin Inductance				7	nH

Notes:

1. RC7106 logic inputs have internal pull-up resistors.
2. All clock outputs loaded with maximum lump capacitance test load specified in AC Electrical Characteristics section.
3. X1 input threshold voltage (typical) is VDD/2
4. The RC7106 contains an internal crystal load capacitor between X1 and VSS and another between X2 and VSS. The total load placed on the crystal is 18pF; this includes typical stray capacitance of short PCB traces to the crystal.
5. X1 input capacitance is applicable when X1 is driven with an external clock source (X2 is left unconnected).

AC Electrical Characteristics

T_A=0°C to 70°C; VDD=3.3V±5%; VDDL=2.5V±5%; f_{XTL}=14.31818MHz

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output; Spread Spectrum clocking is disabled.

CPU Clock Outputs, CPU0:1 (C_{LOAD}=20pF)

Parameter		CPU=133MHz			Units	Test Condition/Comments
		Min.	Typ.	Max.		
t_P	Period	7.5		8	nS	Meas. at rising edge at 1.25V.
t_H	High Time		2		nS	Duration of clock cycle above 2V.
t_L	Low Time		1.8		nS	Duration of clock cycle below 0.4V
t_R	Output Rise Time	.4		1.6	nS	0.4V to 2.0V
t_F	Output Fall Time	.4		1.6	nS	2.0V to 0.4V
t_D	Duty Cycle	45		55	%	Measured at 1.25V
t_{JC}	Jitter, Cycle to Cycle			250	pS	Measured on rising edge at 1.25V.
t_{SK}	Output Skew			175	pS	Measured on rising edge at 1.25V.
f_{ST}	Frequency Stabilization from Power-up (cold start)			3	mS	Assumes full supply voltage reached within 1mS from power-up. Short cycles exist prior to frequency stabilization.
Z_O	AC output Impedance		20		Ω	Average value during switching transition. Used for determining series termination value.

PCI Clock Outputs, PCI0:7 (Lump Capacitance Test Load = 30pF)

Parameter		PCI = 33.3MHz			Units	Test Condition/Comment
		Min.	Typ.	Max.		
t_P	Period	30			nS	Meas. at rising edge at 1.5V.
t_H	High Time	12.0			nS	Duration of clock cycle above 2.4V.
t_L	Low Time	12.0			nS	Duration of clock cycle below 0.4V
t_R	Output Rise Time	0.5		2	nS	0.4V to 2.4V
t_F	Output Fall Time	0.5		2	nS	2.4V to 0.4V
t_D	Duty Cycle	45		55	%	Measured at 1.5V
t_{JC}	Jitter, Cycle to Cycle			500	pS	Measured on rising edge at 1.5V.
t_{SK}	Output Skew			500	pS	Measured on rising edge at 1.5V.
t_O	CPU to PCI Clock Offset	1.5		4.0	nS	Covers all CPU/PCI outputs. Measured on rising edge at 1.5V. CPU leads PCI output.

3V66 Clock Outputs (Lump Capacitance Test Load = 30pF)

Parameter		CPU = 133MHz			Units	Test Condition/Comment
		Min.	Typ.	Max.		
f	Frequency		66.6		MHz	
t_R	Output Rise Time	0.5		2	nS	0.4V to 2.4V
t_F	Output Fall Time	0.5		2	nS	2.4V to 0.4V
t_D	Duty Cycle	45		55	%	Measured at 1.5V
t_{jc}	Jitter, Cycle-to-cycle			500	pS	Measured on rising edge at 1.5V
t_{SK}	Output Skew			250	pS	Measured at 1.5V
f_{ST}	Frequency Stabilization from Power-up			3	mS	Assumes full supply voltage reached within 1mS from power-up.
Z_O	AC Output Impedance		20		ohm	Average value during switching transition. Used for determining series termination value.

CPU/2 Clock Output (Lump Capacitance Test Load = 20pF)

Parameter		CPU = 133MHz			Units	Test Condition/Comment
		Min.	Typ.	Max.		
f	Frequency		66.6		MHz	
t_R	Output Rise Time	0.5		2	nS	0.4V to 2.4V
t_F	Output Fall Time	0.5		2	nS	2.4V to 0.4V
t_D	Duty Cycle	45		55	%	Measured at 1.5V
t_{jc}	Jitter, Cycle-to-cycle			250	pS	Measured on rising edge at 1.5V
t_{SK}	Output Skew			175	pS	Measured at 1.25V
f_{ST}	Frequency Stabilization from Power-up			3	mS	Assumes full supply voltage reached within 1mS from power-up.
Z_O	AC Output Impedance		20		ohm	Average value during switching transition. Used for determining series termination value.

24MHz and 48MHz Clock Outputs (Lump Capacitance Test Load = 20pF)

Parameter		CPU = 133MHz Min.	Typ.	Max.	Units	Test Condition/Comment
f	Frequency		48.008 24.004		MHz	Determined by PLL divider ratio.
f_D	Frequency deviation		+167		ppm	(48.008-48)/48
n/m			57/17, 114/17		-	
t_R	Output Rise Time	0.5		2	nS	0.4V to 2.4V
t_F	Output Fall Time	0.5		2	nS	2.4V to 0.4V
t_D	Duty Cycle	45		55	%	Measured at 1.5V
t_A	Jitter, Absolute			500	pS	Measured on rising edge at 1.5V.
f_{ST}	Frequency Stabilization from Power-up			3	mS	Assumes full supply voltage reached within 1mS from power-up.
Z_O	AC Output Impedance		20		ohm	Average value during switching transition. Used for determining series termination value.

IOAPIC Clock Output (Lump Capacitance Test Load = 20pF)

Parameter		CPU = 133MHz Min.	Typ.	Max.	Units	Test Condition/Comment
f	Frequency		33.3		MHz	Frequency generated by crystal oscillator.
t_R	Output Rise Time	0.4		1.6	nS	0.4V to 2.0V
t_F	Output Fall Time	0.4		1.6	nS	2.0V to 0.4V
t_D	Duty Cycle	45		55	%	Measured at 1.25V
t_A	Jitter, Absolute			500	pS	Measured on rising edge at 1.25V.
t_{SK}	Output Skew			175	pS	Measured at 1.25V
f_{ST}	Frequency Stabilization from Power-up			1.5	mS	Assumes full supply voltage reached within 1mS from power-up.
Z_O	AC Output Impedance		20		ohm	Average value during switching transition. Used for determining series termination value.

REF Clock Output (Lump Capacitance Test Load = 20pF)

Parameter		CPU = 133MHz Min.	Typ.	Max.	Units	Test Condition/Comment
f	Frequency		14.31818		MHz	Frequency generated by crystal oscillator.
t_R	Output Rise Time	0.5		2	nS	0.4V to 2.4V
t_F	Output Fall Time	0.5		2	nS	2.4V to 0.4V
t_D	Duty Cycle	45		55	%	Measured at 1.5V
t_{jc}	Jitter, Cycle-to-cycle			1	nS	Measured on rising edge at 1.5V.
t_{SK}	Output Skew			1	nS	Measured at 1.5V
f_{ST}	Frequency Stabilization from Power-up			3	mS	Assumes full supply voltage reached within 1mS from power-up.
Z_O	AC Output Impedance		20		ohm	Average value during switching transition. Used for determining series termination value.

Group Skews (CPU and IOAPIC load = 20pF; PCI, 3V66 load = 30pF)

Parameter		CPU = 133MHz			Units	Test Condition/Comment
		Min.	Typ.	Max.		
$t_{CPU-3V66}$	CPU (66.6MHz) to 3V66	0		1.5	nS	CPU @ 1.25V and 3V66 @ 1.5V
$t_{3V66-PCI}$	3V66 to PCI	1.5	2.1	4	nS	3V66 and PCI @ 1.5V, 3V66 Leads
$t_{CPU-IOAPIC}$	CPU to IOAPIC	1.5	2.1	4	nS	CPU and IOAPIC @ 1.25V, CPU Leads

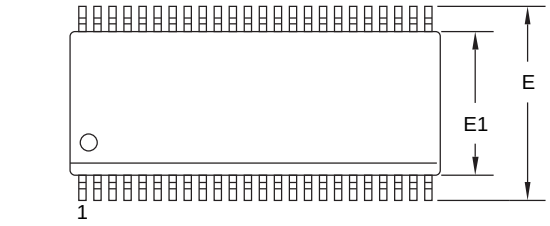
Mechanical Dimensions

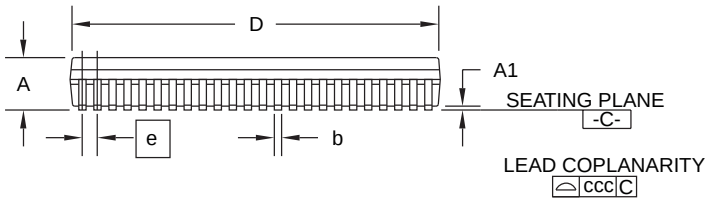
48 pin SSOP

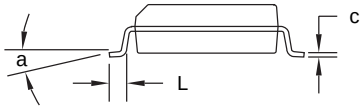
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.095	.110	2.41	2.79	
A1	.008	.016	0.20	0.41	
b	.008	.0135	0.20	0.34	5
c	.005	.010	0.13	0.25	5
D	.620	.630	15.75	16.00	2, 4
E	.395	.420	10.03	10.67	
E1	.291	.299	7.39	7.59	2
e	.025 BSC		0.64 BSC		
L	.020	.040	0.51	1.02	3
N	48		48		6
a	0°	8°	0°	8°	
ccc	---	.004	---	0.13	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
2. "D" and "E1" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "b" & "c" dimensions include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Ordering Information

Product Number	Temperature	Screening	Package	Package Marking
RC7106			48 SSOP	RC7106

RC7108

133MHz Spread Spectrum Clock for Motherboards

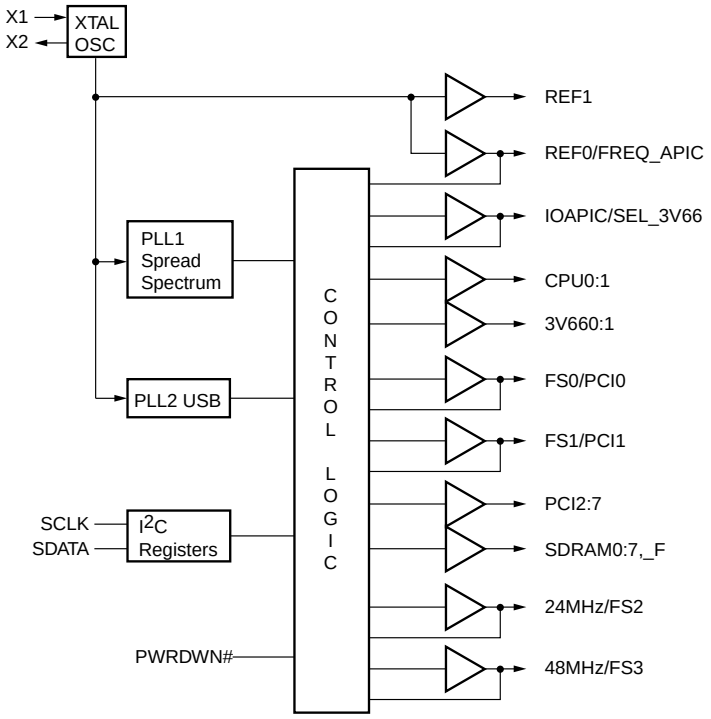
Features

- Employs Fairchild's proprietary Spread Spectrum Technology
- Reduces measured EMI by as much as 10dB
- Supports up to 150MHz
- Two skew-controlled copies of the CPU clock
- I^2C programmable
- Two copies of 3V66 clock
- One copy 24MHz clock
- One copy 48MHz clock
- One copy IOAPIC
- Two copy REF 14.318MHz clock (3.3V)
- Eight copies PCI clock
- Nine copies of SDRAM clock with one Free-running
- Power down capability

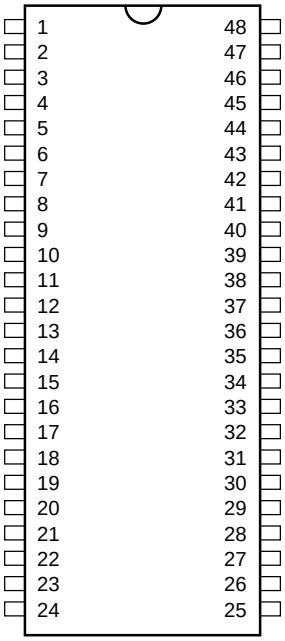
Description

The RC7108 is a clock synthesizer for motherboard applications. It meets the requirements for 133MHz Whiting chipset. The clock frequencies can be set with the 4 select pins and/or be set via the I^2C interface.

Block Diagram



Pin Assignments



Pin Assignments

Pin #	Pin Name	Pin #	Pin name	Pin #	Pin Name
1	REF1	17	PCI5	33	VSS
2	VDD	18	VDD	34	SDRAM5
3	X1	19	PCI6	35	SDRAM4
4	X2	20	PCI7	36	SDRAM3
5	VSS	21	VSS	37	VDD
6	VSS	22	PWRDWN#	38	SDRAM2
7	3V66-0	23	SCLK	39	SDRAM1
8	3V66-1	24	SDATA	40	SDRAM0
9	VDD	25	VDD	41	VSS
10	VDD	26	48MHz/FS3	42	VSSL
11	FS0/PCI0	27	24MHz/FS2	43	CPU1
12	FS1/PCI1	28	VSS	44	CPU0
13	PCI2	29	VDD	45	VDDL
14	VSS	30	SDRAM_F	46	IOAPIC/SEL_3V66
15	PCI3	31	SDRAM7	47	VDDL
16	PCI4	32	SDRAM6	48	REF0/FREQ_APIC

PWRDWN#

PWRDWN#	CPU	SDRAM	IOAPIC	3V66	PCI	REF, 24MHz, 48MHz	OSC.	PLL
0	LOW	LOW	LOW	LOW	LOW	LOW	OFF	OFF
1	ON	ON	ON	ON	ON	ON	ON	ON

Frequency Selection

FS3	FS2	FS1	FS0	CPU MHz	SDRAM MHz	PCI MHz	3V66 (MHz)		IOAPIC (MHz)	
							3V66_SYNC =0	3V66_SYNC =1	FREQ_APIC =0	FREQ_APIC =1
0	0	0	0	100.3	100.3	33.3	66.6	66.6	16.67	33.3
0	0	0	1	100.9	100.9	33.67	67.34	67.34	16.84	33.67
0	0	1	0	105	105	35	70	70	17.5	35
0	0	1	1	115	115	38.33	64*	76.66	19.17	38.33
0	1	0	0	120	120	40	64*	80	20	40
0	1	0	1	124	124	41.33	64*	82.66	20.67	41.33
0	1	1	0	133.3	133.3	44.33	64*	88.66	22.17	44.33
0	1	1	1	133.3	133.3	33.3	66.6	66.6	16.67	33.3
1	0	0	0	140	140	35	70	70	17.5	35
1	0	0	1	150	150	37.5	64*	75	18.75	37.5
1	0	1	0	66.8	100.2	33.4	66.6	66.6	16.67	3.3
1	0	1	1	70	105	35	70	70	17.5	35
1	1	0	0	75	112.5	37.5	64*	75	18.75	37.5
1	1	0	1	83.3	124.5	41.5	64*	83	20.75	41.5
1	1	1	0	90	90	30	60	60	15	30
1	1	1	1	95	95	31.67	63.34	63.34	15.84	31.67

***Note:** These output frequencies are not synchronous to the CPU Clock and do not have Spread Spectrum modulation.

Pin Descriptions

Pin Name	Pin Number	Type	Pin Function Description
CPU0:1	44,43	OUT	CPU Clock Outputs: These two CPU clocks are determined by the 4 select pins FS0:3
PCI2:7	13,15,16, 17,19,20	OUT	PCI BUS Clock Outputs: These 6 PCI clock outputs run synchronously to the CPU.
PCI0/FS0	11	OUT/IN	I/O Dual Function PCI0 and FS0 pin: See table for frequency selection. After power-on, this pin becomes a normal PCI clock.
PCI1/FS1	12	OUT/IN	I/O Dual Function PCI1 and FS1 pin: See table for frequency selection. After power-on, this pin becomes a normal PCI clock.
3V66-0:1	7,8	OUT	3V66 Clock Outputs: These 2 outputs are fixed at 66MHz operating from 3.3V.
REF1	1	OUT	REF Clock Output: This output provides a 14.318MHz high drive clock .
REF0/ FREQ_APIC	48	OUT/IN	I/O Dual Function REF0 and FREQ_APIC Pin: During power-up, if the input is “0”, the IOAPIC output would operate at 16.67MHz. If the input is latched “1”, the IOAPIC output would operate at 33.3MHz. After power-on, this pin becomes a REF0 output. There is an internal pull-up resistor on this pin.
IOAPIC/ SEL_3V66	46	OUT/IN	I/O Dual Function IOAPIC and SEL_3V66 Pin: See table for frequency selection.
SDRAM0:7 SDRAM_F	40,39,38,36, 35,34,32,31, 30	OUT	SDRAM Clock Outputs: SDRAM0:7 clocks are determined by FS0:FS3. SDRAM_F is a free-running clock which is not controlled by the I^2C.
24MHz/FS2	27	OUT/IN	I/O Dual Function 24MHz and FS2 pin: See table for frequency selection. After power-on the pin becomes a normal 24MHz clock.
48MHz/FS3	26	OUT/IN	I/O Dual Function 48MHz and FS3 pin: See table for frequency selection. After power-on the pin becomes a normal 48MHz clock.
X1	3	IN	Crystal Connection: An input connection for an external14.318MHz crystal. If using an external reference, this pin must be left unconnected.
X2	4	OUT	Crystal Connection or External Reference Frequency Input: Connect to either a 14.318MHz crystal or other reference signal.
PWRDWN#	22	IN	Power-down Input pin: This pin shuts down the clock PLL bring all clocks to a low state.
SCLK	23	IN	I^2C Clock Pin: The I^2C clock should be applied to this input as described in the I^2C section of this datasheet.
SDATA	24	IN/OUT	I^2C Data Pin: Data should be presented to this input as described by the I^2C section of this datasheet. There is an internal pull-up resistor on this pin.
VDD	2,9,10,18,25, 29,37	POWER	3.3V Power Pins:
VDDL	45,47	POWER	2.5V Power Pins:
VSS	5,6,14,21,28, 33,41,42	POWER	Ground Pins:

Functional Description

I/O Pin Operation

Dual Purpose I/O pins such as pin 11 FS0/PCI0, act as a logic input upon power up. This allows the determination of assigned device function. For this example, FS0 along with the other three select pins will determine the clock frequencies as shown in the table. A short time after power up, the logic state is latched and the pin becomes a clock output pin. In this case, pin 11 becomes a PCI clock output. This feature reduces device pin count by combining clock outputs with input select pins.

An external 10kohm “strapping” resistor is connected between the I/O pin and VDD or VSS (ground). A connection to ground sets a “0” bit and a connection to VDD sets a “1” bit. See Figure 1.

Upon power up, the first 2mS of operation is used for input logic selection. The clock output pins are tri-stated, allowing the output strapping resistor on the I/O pin to pull the pin and its associated capacitive clock load to either a logic high or low state. At the end of the 2mS period, the established logic “0” or “1” condition of the I/O pin is then latched. Next the output buffer is enabled which converts the I/O pin into an operating clock output. The 2mS timer is started when VDD reaches 2.0V. The input bits can only be reset by turning the VDD off and then back on again.

It should be noted that the strapping resistors have no significant effect on clock output signal integrity. The drive impedance of clock output is 20 ohms (nominal) which is minimally affected by the 10kohm strap to ground or VDD. As with the series termination resistor, the output strapping resistor should be placed as close to the I/O pin as possible in order to keep the interconnecting trace short. The trace from the resistor to ground or VDD should be kept less than two inches in length to prevent system noise coupling during input logic sampling.

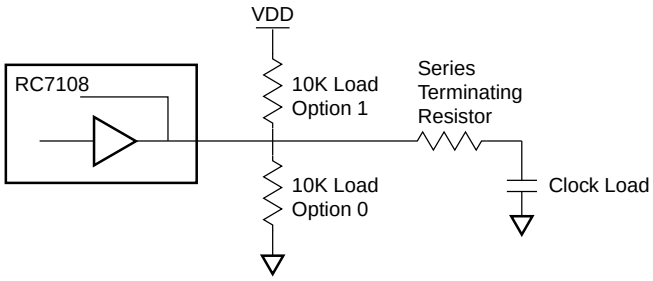


Figure 1. Input Logic Selection through Resistor Load Option

Serial Data Interface

The RC7108 features a two-pin, serial data interface that can be used to configure internal register settings that control particular device functions. Upon power-up, the RC7108 initializes with default register settings. Therefore, the use of this serial data interface is optional. The serial interface is write-only (to the clock chip) and is the dedicated function of device pins SDATA and SCLK. In motherboard applications, SDATA and SCLK are typically driven by two logic outputs of the chipset. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions. Table 2 summarizes the control functions of the serial data interface.

Table 2. Serial Data Interface Control Functions Summary

Control Function	Description	Common Application
Clock Output Disable	Any individual clock output(s) can be disabled. Disabled outputs are actively held low.	Unused outputs are disabled to reduce EMI and system power. Examples are clock outputs to unused PCI slots.
CPU Clock Frequency Selection	Provides CPU/PCI frequency selections beyond the 133MHz provided upon power-on. Frequency is changed in a smooth and controlled fashion.	For alternate microprocessors and power management options. Smooth frequency transition allows CPU frequency change under normal system operation.
Output Tristate	Puts all clock outputs into a high impedance state.	Production PCB testing.
Test Mode	All clock outputs toggle in relation to X1 input, internal PLL is bypassed. Refer to Table 4.	Production PCB testing.
Reserved	Reserved function for future device revision or production device testing.	No user application. Register bit must be written as 0.

Operation

The RC7108 is programmed by writing 10 bytes of eight bits each. See Table 3 for byte order.

Table 3. Byte Writing Sequence

Byte Sequence	Byte Name	Bit Sequence	Byte Description
1	Slave Address	11010010	Commands the RC7108 to accept the bits in Data Bytes 3-6 for internal register configuration. Since other devices may exist on the same common serial data bus, it is necessary to have a specific slave address for each potential receiver. The slave receiver address for the RC7108 is 11010010. Register setting will not be made if the Slave Address is not correct (or is for an alternate slave receiver).
2	Command Code	Don't Care	Unused by the RC7108, therefore bit values are ignored (don't care). This byte must be included in the data write sequence to maintain proper byte allocation. The Command Code Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
3	Byte Count	Don't Care	Unused by the RC7108, therefore bit values are ignored (don't care). This byte must be included in the data write sequence to maintain proper byte allocation. The Byte Count Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
4	Data Byte 0	Refer to Table 5	The data bits in these bytes set internal RC7108 registers that control device operation. The data bits are only accepted when the Address Byte bit sequence is 11010010, as noted above. For description of bit control functions, refer to Table 4, Data Byte Serial Configuration Map.
5	Data Byte 1		
6	Data Byte 2		
7	Data Byte 3		
8	Data Byte 4		
9	Data Byte 5		
10	Data Byte 6		

Writing Data Bytes

Each bit of the 10 data bytes controls a particular device function except for the “reserved bits”. These must be preserved by writing a logic 0. Bit 7, the MSB, is written first. See Table 4 for bit descriptions of Data Bytes 1-4.

Table 5 shows additional frequency selections that are programmable via the serial data interface.

Table 7 shows the mode select functions for Byte 3, bits 1 and 0.

Table 4. Data Bytes 1-4 Serial Configuration Map

Bit(s)	Affected Pin		Control Function	Bit Control		Default
	Pin No.	Pin Name		0	1	
Data Byte 1						
7	-	-	(Reserved)	-	-	0
6	-	-	(Reserved)	-	-	0
5	-	-	(Reserved)	-	-	0
4	27	24MHz	Clock Output Disable	Disable	Enable	1
3	26	48MHz	Clock Output Disable	Disable	Enable	1
2	-	-	(Reserved)	-	-	0
1	-	-	(Reserved)	-	-	0
0	-	-	(Reserved)	-	-	0
Data Byte 2						
7	31	SDRAM7	Clock Output Disable	Disable	Enable	1
6	32	SDRAM6	Clock Output Disable	Disable	Enable	1
5	34	SDRAM5	Clock Output Disable	Disable	Enable	1
4	35	SDRAM4	Clock Output Disable	Disable	Enable	1
3	36	SDRAM3	Clock Output Disable	Disable	Enable	1
2	38	SDRAM2	Clock Output Disable	Disable	Enable	1
1	39	SDRAM1	Clock Output Disable	Disable	Enable	1
0	40	SDRAM0	Clock Output Disable	Disable	Enable	1
Data Byte 3						
7	20	PCI7	Clock Output Disable	Disable	Enable	1
6	19	PCI6	Clock Output Disable	Disable	Enable	1
5	17	PCI5	Clock Output Disable	Disable	Enable	1
4	16	PCI4	Clock Output Disable	Disable	Enable	1
3	15	PCI3	Clock Output Disable	Disable	Enable	1
2	13	PCI2	Clock Output Disable	Disable	Enable	1
1	12	PCI1	Clock Output Disable	Disable	Enable	1
0	11	PCI0	Clock Output Disable	Disable	Enable	1
Data Byte 4						
7	-	-	(Reserved)	-	-	0
6	8	3V66-1	Clock Output Disable	Disable	Enable	1
5	7	3V66-0	Clock Output Disable	Disable	Enable	1
4	-	-	(Reserved)	-	-	0
3	46	IOAPIC	Clock Output Disable	Disable	Enable	1
2	-	-	(Reserved)	-	-	0
1	43	CPU1	Clock Output Disable	Disable	Enable	1
0	44	CPU0	Clock Output Disable	Disable	Enable	1

Table 5. Byte 0: Functionality and frequency select register (Default = 0)

Bit	Description								Default
Bit 7	0- ±0.25% Center Spread Spectrum								0
	1- Down Spread Spectrum 0 to -0.5%								
Bit (2, 6:4)					3V66		IOAPIC		Note 1
	Bit(2,6:4)	CPU	SDRAM	PCI	3V66_SEL =0	3V66_SEL =1	FREQ_APIC =0	FREQ_APIC =1	
	0000	100.3	100.3	33.3	66.6	66.6	16.67	33.3	
	0001	100.9	100.9	33.67	67.34	67.34	16.84	33.67	
	0010	105	105	35	70	70	17.5	35	
	0011	115	115	38.33	64*	76.66	19.17	38.33	
	0100	120	120	40	64*	80	20	40	
	0101	124	124	41.33	64*	82.66	20.67	41.33	
	0110	133.3	133.3	44.33	64*	88.66	22.17	44.33	
	0111	133.3	133.3	33.3	66.6	66.6	16.67	33.3	
	1000	140	140	35	70	70	17.5	35	
	1001	150	150	37.5	64*	75	18.75	37.5	
	1010	66.8	100.2	33.4	66.6	66.6	16.67	3.3	
	1011	70	105	35	70	70	17.5	35	
	1100	75	112.5	37.5	64*	75	18.75	37.5	
	1101	83.3	124.5	41.5	64*	83	20.75	41.5	
	1110	90	90	30	60	60	15	30	
	1111	95	95	31.67	63.34	63.34	15.84	31.67	
Bit 3	0- frequency is selected by hardware select, latched inputs 1- Frequency is selected by Bit 2,6:4								0
Bit 1	0- Normal 1- Spread Spectrum								0
Bit 0	0- Enabled 1- Tristate all outputs								0

Note 1: Default at power-up will be for latched logic inputs to define frequency, Bit 2, 6:4 are defaulted to 0000.
*These output frequencies are not synchronous to the CPU Clock and do not have Spread Spectrum modulation.

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Symbol	Parameter	Ratings	Units
V_{DD}, V_{IN}	Voltage on any pin with respect to V_{SS}	-0.5 to +7.0	V
T_{STG}	Storage Temperature	-65 to +150	^{o}C
T_B	Ambient Temperature	-55 to +125	^{o}C
T_A	Operating Temperature	0 to +70	^{o}C
ESD_{PROT}	Input ESD Protection	2 (min)	kV

DC Electrical Characteristics

T_A = 0°C to +70°C; VDD = 3.3V±5%; VDDL = 2.5V±5%

Parameter		Test Condition	Min.	Typ.	Max.	Units
Supply Current						
IDD3	Combined 3.3V Supply Current	CPU = 133MHz Outputs Loaded		TBD		mA
IDD2	Combined 2.5V Supply Current	CPU = 133MHz Outputs Loaded		TBD		mA
Logic Inputs						
V_{IL}	Input Low Voltage		VSS-0.3		0.8	V
V_{IH}	Input High Voltage		2.0		VDD+0.3	V
I_{IL}	Input Low Current[1]				-25	µA
I_{IH}	Input High Current[1]				10	µA
I_{IL}	Input Low Current				-5	µA
I_{IH}	Input High Current				5	µA
Clock Outputs[2]						
V_{OL}	Output Low Voltage	I_{OL}=1mA			0.4	V
V_{OH}	Output High Voltage CPU and IOAPIC	I_{OH}=-1mA	2.0			V
	PCI, SDRAM, 3V66, 24MHz,48MHz,REF		2.4			
I_{OL}	Output Low Current CPU	V_{OL}=1.2V	27		93	mA
	IOAPIC		40		138	
	PCI, 3V66	V_{OL}=1.4V	26.5		139	
	REF, 24MHz,48MHz		25		76	
	SDRAM		61		152	

DC Electrical Characteristics (Continued)

T_A = 0°C to +70°C; VDD = 3.3V±5%; VDDL = 2.5V±5%

Parameter		Test Condition	Min.	Typ.	Max.	Units
I_{OH}	Output High Current CPU	V_{OH}=1.2V	-26		-101	mA
	IOAPIC		-39		-150	
	PCI, 3V66	V_{OH}=1.4V	-31		-189	
	REF, 24MHz,48MHz		-27		-94	
	SDRAM		-68		-188	
Crystal oscillator						
V_{TH}	X1 Input Threshold Voltage[3]	VDD=3.3V		1.5		V
C_{LOAD}	Load Capacitance, as seen by external Xtal.[4]			18		pF
C_{IN}	X1 Input Capacitance[5]	X2 unconnected		28		pF
Pin Capacitance/Inductance						
C_{IN}	Input Pin Capacitance	Except X1 and X2			5	PF
C_{OUT}	Output Pin Capacitance				6	pF
L_{IN}	Input Pin Inductance				7	NH

Notes:

1. RC7108 logic inputs have internal pull-up resistors.
2. All clock outputs loaded with maximum lump capacitance test load specified in AC Electrical Characteristics section.
3. X1 input threshold voltage (typical) is VDD/2
4. The RC7108 contains an internal crystal load capacitor between X1 and VSS and another between X2 and VSS. The total load placed on the crystal is 18pF; this includes typical stray capacitance of short PCB traces to the crystal.
5. X1 input capacitance is applicable when X1 is driven with an external clock source (X2 is left unconnected).

AC Electrical Characteristics

T_A=0°C to 70°C; VDD=3.3V±5%; VDDL=2.5V±5%; f_{XTL}=14.31818MHz

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output; Spread Spectrum clocking is disabled.

CPU Clock Outputs, CPU0:1 (C_{LOAD}=20pF)

Parameter		CPU=133MHz			Units	Test Condition/Comments
		Min.	Typ.	Max.		
t_P	Period	7.5		8	nS	Meas. at rising edge at 1.25V.
t_H	High Time		2		nS	Duration of clock cycle above 2V.
t_L	Low Time		1.8		nS	Duration of clock cycle below 0.4V
t_R	Output Rise Time	.4		1.6	nS	0.4V to 2.0V
t_F	Output Fall Time	.4		1.6	nS	2.0V to 0.4V
t_D	Duty Cycle	45		55	%	Measured at 1.25V
t_{JC}	Jitter, Cycle to Cycle			250	pS	Measured on rising edge at 1.25V.
t_{SK}	Output Skew			175	pS	Measured on rising edge at 1.25V.
f_{ST}	Frequency Stabilization from Power-up (cold start)			3	mS	Assumes full supply voltage reached within 1mS from power-up. Short cycles exist prior to frequency stabilization.
Z_O	AC output Impedance		20		Ω	Average value during switching transition. Used for determining series termination value.

PCI Clock Outputs, PCI0:7 (Lump Capacitance Test Load = 30pF)

Parameter		PCI = 33.3MHz			Units	Test Condition/Comment
		Min.	Typ.	Max.		
t_P	Period	30			nS	Meas. at rising edge at 1.5V.
t_H	High Time	12.0			nS	Duration of clock cycle above 2.4V.
t_L	Low Time	12.0			nS	Duration of clock cycle below 0.4V
t_R	Output Rise Time	0.5		2	nS	0.4V to 2.4V
t_F	Output Fall Time	0.5		2	nS	2.4V to 0.4V
t_D	Duty Cycle	45		55	%	Measured at 1.5V
t_{JC}	Jitter, Cycle to Cycle			500	pS	Measured on rising edge at 1.5V.
t_{SK}	Output Skew			500	pS	Measured on rising edge at 1.5V.
t_O	CPU to PCI Clock Offset	1.5		4.0	nS	Covers all CPU/PCI outputs. Measured on rising edge at 1.5V. CPU leads PCI output.

3V66 Clock Outputs (Lump Capacitance Test Load = 30pF)

Parameter		CPU = 133MHz			Units	Test Condition/Comment
		Min.	Typ.	Max.		
f	Frequency		66.6		MHz	
t_R	Output Rise Time	0.5		2	nS	0.4V to 2.4V
t_F	Output Fall Time	0.5		2	nS	2.4V to 0.4V
t_D	Duty Cycle	45		55	%	Measured at 1.5V
t_{jc}	Jitter, Cycle-to-cycle			500	pS	Measured on rising edge at 1.5V
t_{SK}	Output Skew			250	pS	Measured at 1.5V
f_{ST}	Frequency Stabilization from Power-up			3	mS	Assumes full supply voltage reached within 1mS from power-up.
Z_O	AC Output Impedance		20		ohm	Average value during switching transition. Used for determining series termination value.

SDRAM Clock Output (Lump Capacitance Test Load = 20pF)

Parameter		CPU = 133MHz			Units	Test Condition/Comment
		Min.	Typ.	Max.		
f	Frequency		66.6		MHz	
t_R	Output Rise Time	0.5		2	nS	0.4V to 2.4V
t_F	Output Fall Time	0.5		2	nS	2.4V to 0.4V
t_D	Duty Cycle	45		55	%	Measured at 1.5V
t_{jc}	Jitter, Cycle-to-cycle			250	pS	Measured on rising edge at 1.5V
t_{SK}	Output Skew			250	pS	Measured at 1.5V
f_{ST}	Frequency Stabilization from Power-up			3	mS	Assumes full supply voltage reached within 1mS from power-up.
Z_O	AC Output Impedance		20		ohm	Average value during switching transition. Used for determining series termination value.

24MHz and 48MHz Clock Outputs (Lump Capacitance Test Load = 20pF)

Parameter		CPU = 133MHz			Units	Test Condition/Comment
		Min.	Typ.	Max.		
f	Frequency		48.008 24.004		MHz	Determined by PLL divider ratio.
f_D	Frequency deviation		+167		ppm	(48.008-48)/48
n/m			57/17, 114/17		-	
t_R	Output Rise Time	0.5		2	nS	0.4V to 2.4V
t_F	Output Fall Time	0.5		2	nS	2.4V to 0.4V
t_D	Duty Cycle	45		55	%	Measured at 1.5V
t_A	Jitter, Absolute			500	pS	Measured on rising edge at 1.5V.
f_{ST}	Frequency Stabilization from Power-up			3	mS	Assumes full supply voltage reached within 1mS from power-up.
Z_O	AC Output Impedance		20		ohm	Average value during switching transition. Used for determining series termination value.

IOAPIC Clock Output (Lump Capacitance Test Load = 20pF)

Parameter		CPU = 133MHz			Units	Test Condition/Comment
		Min.	Typ.	Max.		
f	Frequency		14.31818		MHz	Frequency generated by crystal oscillator.
t_R	Output Rise Time	0.4		1.6	nS	0.4V to 2.0V
t_F	Output Fall Time	0.4		1.6	nS	2.0V to 0.4V
t_D	Duty Cycle	45		55	%	Measured at 1.25V
t_A	Jitter, Absolute			500	pS	Measured on rising edge at 1.25V.
f_{ST}	Frequency Stabilization from Power-up			1.5	mS	Assumes full supply voltage reached within 1mS from power-up.
Z_O	AC Output Impedance		20		ohm	Average value during switching transition. Used for determining series termination value.

REF Clock Output (Lump Capacitance Test Load = 20pF)

Parameter		CPU = 133MHz			Units	Test Condition/Comment
		Min.	Typ.	Max.		
f	Frequency		14.31818		MHz	Frequency generated by crystal oscillator.
t_R	Output Rise Time	0.5		2	nS	0.4V to 2.4V
t_F	Output Fall Time	0.5		2	nS	2.4V to 0.4V
t_D	Duty Cycle	45		55	%	Measured at 1.5V
t_{jc}	Jitter, Cycle-to-cycle			500	nS	Measured on rising edge at 1.5V.
f_{ST}	Frequency Stabilization from Power-up			3	mS	Assumes full supply voltage reached within 1mS from power-up.
Z_O	AC Output Impedance		20		ohm	Average value during switching transition. Used for determining series termination value.

Group Skews (CPU and IOAPIC load = 20pF; PCI, SDRAM, 3V66 load = 30pF)

Parameter		CPU = 133MHz			Units	Test Condition/Comment
		Min.	Typ.	Max.		
$t_{CPU-3V66}$	CPU (66.6MHz) to 3V66			500	pS	CPU @ 1.25V and 3V66 @ 1.5V Note 180^{o} offset between outputs
$t_{CPU-SDRAM}$	CPU (133MHz) to SDRAM			500	pS	CPU @ 1.25V and SDRAM @1.5V Note 180^{o} offset between outputs
$t_{3V66-PCI}$	3V66 to PCI	1.5	2.1	4	nS	3V66 and PCI @ 1.5V (prefer 2.0 to 2.5nS)
$t_{IOAPIC-PCI}$	IOAPIC to PCI			500	pS	IOAPIC @ 1.25V and PCI @ 1.5V

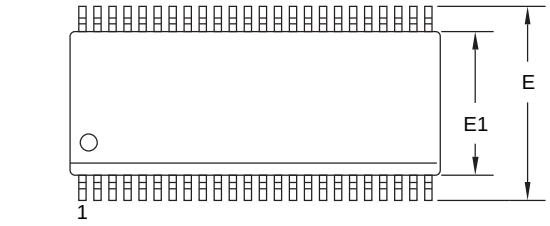
Mechanical Dimensions

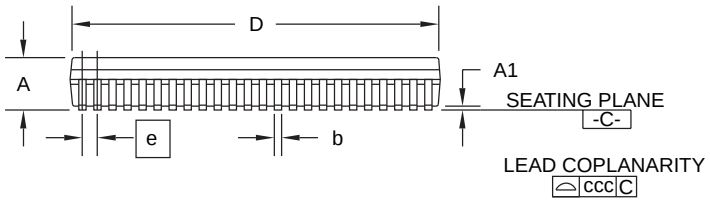
48 pin SSOP

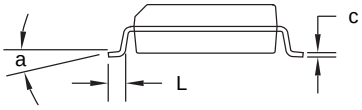
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.095	.110	2.41	2.79	
A1	.008	.016	0.20	0.41	
b	.008	.0135	0.20	0.34	5
c	.005	.010	0.13	0.25	5
D	.620	.630	15.75	16.00	2, 4
E	.395	.420	10.03	10.67	
E1	.291	.299	7.39	7.59	2
e	.025 BSC		0.64 BSC		
L	.020	.040	0.51	1.02	3
N	48		48		6
a	0°	8°	0°	8°	
ccc	---	.004	---	0.13	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
2. "D" and "E1" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "b" & "c" dimensions include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







RC7144

133MHz Spread Spectrum Motherboard Integrated Clock/Buffer

Features

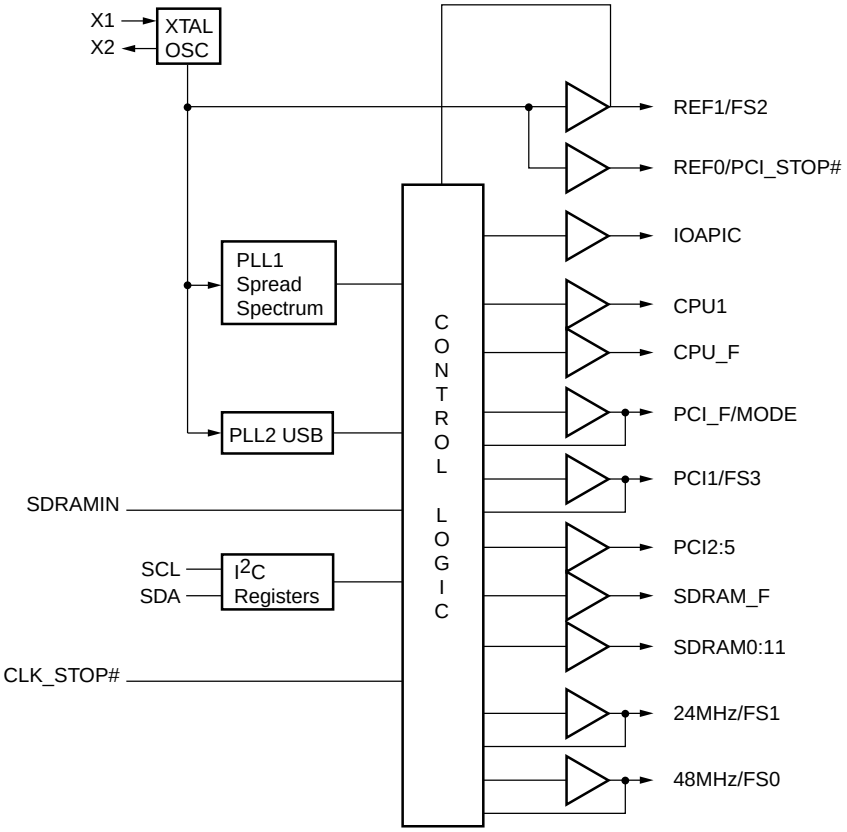
- Employs Fairchild's proprietary Spread Spectrum Technology
- Reduces measured EMI by as much as 10dB
- Supports up to 150MHz
- I^2C programmable
- Two copies of CPU clock with one free running
- One copy 24MHz clock
- One copy 48MHz clock
- One copy IOAPIC
- Two copy REF 14.318MHz clock (3.3V)
- Six copies PCI clock
- Thirteen copies of SDRAM clock with one free running
- PCI/CPU stop capability

Description

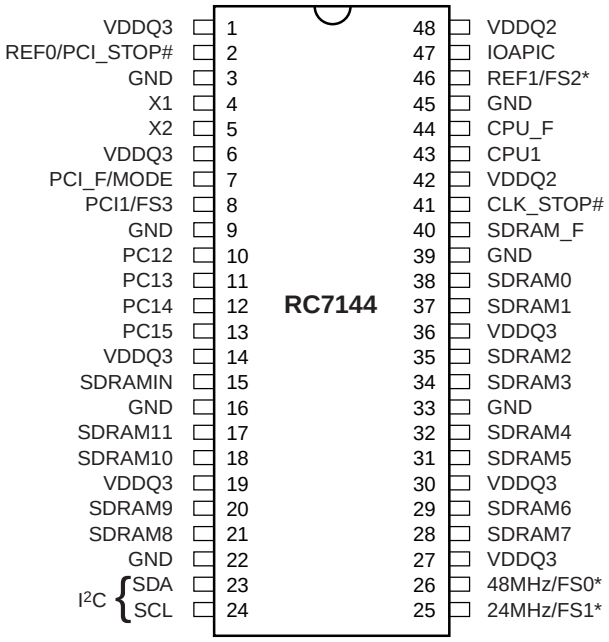
The RC7144 is a clock synthesizer for motherboard applications. It meets the requirements for the 133MHz 13x/zx chipset. The clock frequencies can be set with the 4 select pins or can be set via the I^2C interface.

Preliminary Information

Block Diagram



Pin Assignments



Preliminary Information

Pin Description

Pin Name	Pin #	Pin Type	Pin Function
V_{DDQ3}	1, 6, 14, 19, 27, 30, 36	PWR	**Power connection:** Power supply for core logic, PLL circuitry SDRAM outputs, PCI outputs, reference, 48 & 24 MHz outputs. Connect to 3.3 Volts.
REF0/ PCI_STOP#	2	OUT/IN	**I/O Dual function REF0 & PCI_STOP#:** Function determined by MODE pin. When high, this pin is an output with 14.31818 MHz of reference clock. When MODE is low, PCI_STOP# stops all the PCI clocks.
GND	3, 9, 16, 22, 33, 39, 45	PWR	**Ground connection:** Connect all ground pins to the common system ground plane.
X1	4	IN	**Crystal Connection:** An input connection for an external 14.318 MHz crystal. 18 pF internal cap.
X2	5	OUT	**Crystal Connection or External Reference Frequency:** This pin has dual functions. It can be used as an external 14.318 MHz crystal connection or as an external reference frequency input.
PCI_F/MODE	7	OUT/IN	**Fixed PCI clock output:** Upon power up MODE input will be latched, which will enable or disable REF0.
PCI1/FS3	8	OUT/IN	**PCI clock output:** Upon power up FS3 input will be latched, which will set clock frequencies as frequency selection table. This pin has internal pull down.
PCI2:5	10, 11, 12, 13	OUT	**PCI clock output 2 through 5:** These five PCI clock outputs are controlled by the PCI_STOP# control pin.
SDRAM_IN	15	IN	**Buffered input pin:** The signal provided to this input pin is buffered to 13 outputs.
SDRAM0:11; SDRAM_F	17, 18, 20, 21, 28, 29, 31, 32, 34, 35, 37, 38, 40	OUT	**SDRAM Clock Ouputs:** SDRAM0:11 clock are determined by FS0: FS3. SDRAM_F is a free running clock which is not controlled by the I^2C.
SDA	23	IN/OUT	Data pin for I^2C circuitry.
SCL	24	IN	Clock pin for I^2C circuitry.
24MHz/FS1	25	OUT/IN	**24 MHz clock output:** 24 MHz is provided in normal operation. In standard systems, this output can be used as the clock input for Super I/O chip. Upon power up FS1 input will be latched, which will set clock frequencies as frequency selection table.
48MHz/FS0	26	OUT/IN	**48 MHz clock output:** 48 MHz is provided in normal operation. In standard systems, this output can be used as the reference for universal Serial Bus. Upon power up FS0 input will be latched, which will set clock frequencies as frequency selection table.
CLK_STOP#	41	IN	**CLK_STOP# Input:** When 0, this pin stops the CPU outputs after completing a full clock cycle. This pin does not effect CPU_F.
V_{DDQ2}	42, 48	PWR	Power supply for IOAPIC & all CPU outputs. Connect to 2.5 or 3.3 Volts.
CPU1, CPU_F	43, 44	OUT	**CPU output clocks:** V_{DDQ2} controls output Voltage. Stopped when CLK_STOP# is 0. CPU_F is not affected by CLK_STOP#.
REF1/FS2	46	OUT/IN	**Reference Clock output:** 14.31818 MHz reference output. Upon power up FS2 input will be latched, which will set clock frequencies as frequency selection table.
IOAPIC	47	OUT	**IOAPIC clock:** Provides 14.31818 MHz fixed clock. V_{DDQ2} contols the output Voltage.

Preliminary Information

Frequency Selection Table

Input Address				CPU (MHz)	PCI (MHz)
FS3	FS2	FS1	FS0		
1	1	1	1	133.3	33.3
1	1	1	0	124	31
1	1	0	1	150	37.5
1	1	0	0	140	35
1	0	1	1	105	35
1	0	1	0	110	36.7
1	0	0	1	115	38.3
1	0	0	0	120	40
0	1	1	1	100	33.3
0	1	1	0	133.3	44.43
0	1	0	1	112	37.3
0	1	0	0	103	34.3
0	0	1	1	66.8	33.4
0	0	1	0	83.3	41.7
0	0	0	1	75	37.5
0	0	0	0	124	41.3

Power Management Control

Mode	PCI_STOP#	PCI	REF0	PCI_F
0	0	Stopped	Disable	Running
0	1	Running	Disable	Running
1	X	Running	Running	Running

CLK_STOP#	CPU	CPU_F	REF1, 24/48MHZ, SDRAM 0:11
0	Stopped	Running	Running
1	Running	Running	Running

Functional Description

I/O Pin Operation

Dual Purpose I/O pins such as pin 8 FS3/PCI1, act as a logic input upon power up. This allows the determination of assigned device function. For example, FS3 along with the other three select pins will determine the clock frequencies as shown in the table. A short time after power up, the logic state is latched and the pin becomes a clock output pin. For example, pin 8 becomes a PCI clock output. This feature reduces device pin count by combining clock outputs with input select pins.

An external 10k ohm “strapping” resistor is connected between the I/O pin and VDD or VSS (ground). A connection to ground sets a “0” bit and a connection to VDD sets a “1” bit. See Figure 1.

Upon power up, the first 2mS of operation is used for input logic selection. The clock output pins are tri-stated, allowing the output strapping resistor on the I/O pin to pull the pin and its associated capacitive clock load to either a logic high or low state. At the end of the 2mS period, the established logic “0” or “1” condition of the I/O pin is then latched. Next the output buffer is enabled which converts the I/O pin into an operating clock output. The 2mS timer is started when VDD (3.3V) reaches 2.0V. The input bits can only be reset by turning the VDD off and then back on again.

It should be noted that the strapping resistors have no significant effect on clock output signal integrity. The drive impedance of outputs is 20 ohms (nominal) which is minimally affected by the 10kohm strap to ground or VDD. As with the series termination resistor, the output strapping resistor should be placed as close to the I/O pin as possible in order to keep the interconnecting trace short. The trace from the resistor to ground or VDD should be kept less than two inches in length to prevent system noise coupling during input logic sampling.

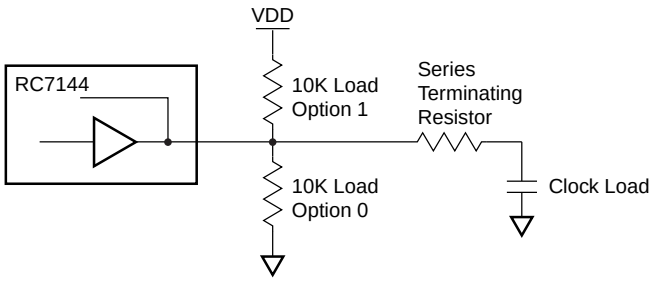


Figure 1. Input Logic Selection through Resistor Load Option

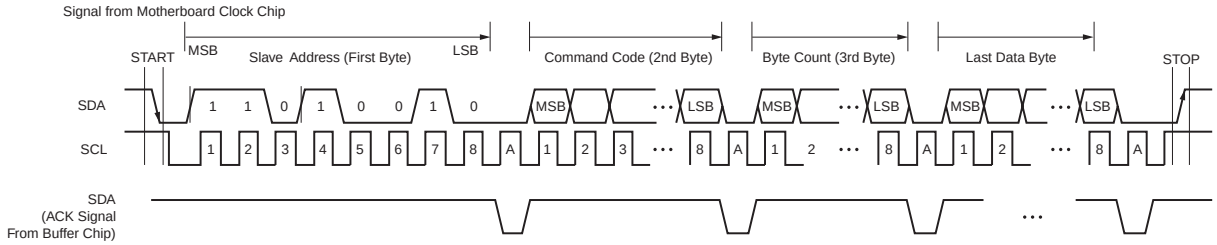
I²C Interface Information

The RC7144 features a two-pin, serial data interface that can be used to configure internal register settings that control particular device functions. Upon power-up, the RC7144 initializes with default register settings therefore, the use of this serial data interface is optional. The serial interface is write-only (to the clock chip) and is the dedicated function of device pins SDA and SCL. In motherboard applications, SDA and SCL are typically driven by two logic outputs of the chipset. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions. Table 1 summarizes the control functions of the serial data interface.

Table 1. Serial Data Interface Control Functions Summary

Control Function	Description	Common Application
Clock Output Disable	Any individual clock output(s) can be disabled. Disabled outputs are actively held low.	Unused outputs are disabled to reduce EMI and system power. Examples are clock outputs to unused PCI slots.
CPU Clock Frequency Selection	Provides CPU/PCI frequency selections other than the 100MHz provided upon power-on. Frequency is changed in a smooth and controlled fashion.	For alternate microprocessors and power management options. Smooth frequency transition allows CPU frequency change under normal system operation.
Spread Spectrum Enabling	Turns spread spectrum on or off.	EMI reduction.
Output Tristate	Puts all clock outputs into a high impedance state.	Production PCB testing.
Test Mode	All clock ouputs toggle in relation to X1 input, internal PLL is bypassed. Refer to Table 6.	Production PCB testing.
Reserved	Reserved function for future device revision or production device testing.	No user application. Register bit must be written as 0.

RC7144 I²C Interface Write Sequence Example



Note: Once the clock detects the start condition and its ADDRESS is matched, the clock chip will pull down the SDA at every 8th bit. The 8 bit data from SDA is latched into the Buffer Chip when the ACK is generated. This ACK signal will continue as long as STOP condition is detected The COMMAND CODE and BYTE COUNT is not used by the Buffer Chip.

I²C Register Operation

The RC7144 is programmed by writing 10 bytes of eight bits each. See Table 2 for byte order.

Table 2. Byte Writing Sequence

Byte Sequence	Byte Name	Bit Sequence	Byte Description
1	Slave Address	11010010	Commands the RC7144 to accept the bits in Data Bytes 0-6 or internal register configuration. Since other devices may exist on the same common serial data bus, it is necessary to have a specific slave address for each potential receiver. The slave receiver address for the RC7144 is 11010010. Register setting will not be made if the Slave Address is not correct (or is for an alternate slave receiver).
2	Command Code	Don't Care	Unused by the RC7144, therefore, bit values are ignored (don't care). This byte must be included in the data write sequence to maintain proper byte allocation. The Command Code Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
3	Byte Count	Don't Care	Unused by the RC7144, therefore, bit values are ignored (don't care). This byte must be included in the data write sequence to maintain proper byte allocation. The Byte Count Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
4	Data Byte 0	Refer to Table 3	The data bits in these bytes set internal RC7144 registers that control device operation. The data bits are only accepted when the Address Byte bit sequence is 11010010, as noted above. For description of bit control functions, refer to Table 5, Data Byte Serial Configuration Map.
5	Data Byte 1		
6	Data Byte 2		
7	Data Byte 3		
8	Data Byte 4		
9	Data Byte 5		
10	Data Byte 6		

Writing Data Bytes

Each bit of the 8 data bytes controls a particular device function except for the “reserved bits”. These must be preserved by writing a logic 0. Bit 7, the MSB, is written first. See Table 3 for bit descriptions of Data Bytes 1-4.

Table 5 shows additional frequency selections that are programmable via the serial data interface.

Table 4 shows the mode select for byte 0, Bit 1and 0.

Table 3. Data Bytes 0–7 Serial Configuration Map

Bit(s)	Affected Pin		Control Function	Bit Control		Default
	Pin No.	Pin Name		0	1	
Data Byte 0						
7	-	-	Spread Mode	Center	Down	0
6	-	-	FS 2	-	-	0
5	-	-	FS 1	-	-	0
4	-	-	FS 0	-	-	0
3	-	-	Hardware/Software Frequency Select	Hardware	Software	0
2	-	-	FS3	-	-	0
1–0	-	-	Bit 1 Bit 0 Function (see Table 4) 0 0 Normal Operation 0 1 Reserved 1 0 Spread Spectrum on 1 0 All Outputs Tristated			00
Data Byte 1						
7	-	-	Reserved	-	-	0
6	-	-	Reserved	-	-	0
5	-	-	Reserved	-	-	0
4	-	-	Test Mode	Test Mode	Normal	1
3	40	SDRAM_F	Clock Output Disabled	Low	Active	1
2	-	-	Reserved	-	-	0
1	43	CPU1	Clock Output Disabled	Low	Active	1
0	44	CPU_F	Clock Output Disabled	Low	Active	1
Data Byte 2						
7	-	-	Reserved	-	-	0
6	7	PCI_F	Clock Output Disabled	Low	Active	1
5	-		Reserved	-	-	0
4	13	PCI5	Clock Output Disabled	Low	Active	1
3	12	PCI4	Clock Output Disabled	Low	Active	1
2	11	PCI3	Clock Output Disabled	Low	Active	1
1	10	PCI2	Clock Output Disabled	Low	Active	1
0	8	PCI1	Clock Output Disabled	Low	Active	1
Data Byte 3						
7	-	-	Reserved	-	-	0
6	-	-	Reserved	-	-	0
5	26	48 MHz	Clock Output Disabled	Low	Active	1
4	25	24MHz	Clock Output Disabled	Low	Active	1
3	-	-	Reserved	-	-	0

Table 3. Data Bytes 0–7 Serial Configuration Map (Continued)

Bit(s)	Affected Pin		Control Function	Bit Control		Default
	Pin No.	Pin Name		0	1	
2	21, 20, 18, 17	SDRAM8:11	Clock Output Disabled	Low	Active	1
1	32, 31, 29, 28	SDRAM4:7	Clock Output Disabled	Low	Active	1
0	38, 37, 35, 34	SDRAM0:3	Clock Output Disabled	Low	Active	1
Data Byte 4						
7	-	-	Reserved	-	-	0
6	-	-	Reserved	-	-	0
5	-	-	Reserved	-	-	0
4	-	-	Reserved	-	-	0
3	-	-	Reserved	-	-	0
2	-	-	Reserved	-	-	0
1	-	-	Reserved	-	-	0
0	-	-	Reserved	-	-	0
Data Byte 5						
7	-	-	Reserved	-	-	0
6	-	-	Reserved	-	-	0
5	-	-	Reserved	-	-	0
4	47	IOAPIC	Clock Output Disabled	Low	Active	1
3	-	-	Reserved	-	-	0
2	-	-	Reserved	-	-	0
1	46	REF1	Clock Output Disabled	Low	Active	1
0	2	REF0	Clock Output Disabled	Low	Active	1
Data Byte 6						
7	-	-	Reserved	-	-	0
6	-	-	Reserved	-	-	0
5	-	-	Reserved	-	-	0
4	-	-	Reserved	-	-	0
3	-	-	Reserved	-	-	0
2	-	-	Reserved	-	-	0
1	-	-	Reserved	-	-	0
0	-	-	Reserved	-	-	0
Data Byte 7						
7	-	-	Reserved	-	-	0
6	-	-	Reserved	-	-	0
5	-	-	Reserved	-	-	0
4	-	-	Reserved	-	-	0
3	-	-	Reserved	-	-	0
2	-	-	Reserved	-	-	0
1	-	-	Reserved	-	-	0
0	-	-	Reserved	-	-	0

Table 4. Select Function for Data Byte 0, Bits 0:1

Function	Input Conditions		Output Conditons				
	Data Byte 0						
	Bit 1	Bit 0	CPU	PC1	IOAPIC REF0:1	48 MHz	24 MHz
Normal Operation	0	0	NOTE 1	NOTE 1	14.318 M	48 M	24 M
Spread Spectrum	1	0	±0.5%	±0.5%	14.318 M	48 M	24 M
Tristate	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

Table 5. Frequency Selection Table Through I^2C Programming

Input Conditons					
Data Byte 0, Bit 3 = 1					
Bit 2 FS3	Bit 6 FS2	Bit 5 FS1	Bit 4 FS0	CPU (MHz)	PCI (MHz)
1	1	1	1	133.3	33.3
1	1	1	0	124	31
1	1	0	1	150	37.5
1	1	0	0	140	35
1	0	1	1	105	35
1	0	1	0	110	36.7
1	0	0	1	115	38.3
1	0	0	0	120	40
0	1	1	1	100	33.3
0	1	1	0	133.3	44.43
0	1	0	1	112	37.3
0	1	0	0	103	34.3
0	0	1	1	66.8	33.4
0	0	1	0	83.3	41.7
0	0	0	1	75	37.5
0	0	0	0	124	41.3

Preliminary Information

Table 6. Test Mode

Function	Input Condition Data Byte4	CPU	PCI	REF, IOAPIC	48MHz	24MHz
Normal	1	Note 1	Note 1	14.318	48	24
Test Mode	0	X1	CPU/2 or 3	X1	X1/2	X1/4

Note:
1. See table 5 for frequency selection.

Absolute Maximum Ratings

Symbol	Parameter	Ratings	Units
V_{DD}, V_{IN}	Voltage on any pin with respect to ground	-0.5 to 7.0	V
T_{STG}	Storage Temperature	-65 to 150	^{o}C
T_B	Ambient Temperature	-55 to 125	^{o}C
T_A	Operating Temperature	0 to 70	^{o}C
ESD_{PROT}	Input ESD Protection	2 (min)	kV

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Electrical Characteristics—Common Parameters

T_A = 0°C to 70°C; Supply Voltage 3.3V±5% (unless otherwise stated)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{IL}	Input Low Voltage		V_{SS}-0.3		0.8	V
V_{IH}	Input High Voltage		2.0		V_{DD}+0.3	V
I_{IL}	Input Low Current	V_{IN}=0; inputs with no pull-up resistors	-5		5	µA
		V_{IN}=0; inputs with pull-up resistors			-25	µA
I_{IH}	Input High Current	V_{IN}=V_{DD}	-5		-5	µA
C_{IN}	Input Capacitance[1]	All except X1 and X2.			5	pF
		X1 and X2 Pins. X2 unconnected.		18		pF
C_{OUT}	Output Capacitance[1]				6	pF
LIN	Input Pin Inductance[1]				7	nH
V_{TH}	Crystal Input Threshold[1]	V_{DD}=3.3V		1.5		V
I_{DD}	Supply Current	Freq=100M: C_L max. on all outputs		300		mA
I_{DDL}		V_{DD}=2.5V 0.5%; Freq-100M		24		mA
T_{STAB}	Clock Stabilization[1]	From V_{DD}=3.3V to 1% Target			3	mS
$T_{CPU-PCI}$	Skew[1]	V_{DDL}=2.5V; V_{DD}=3.3V; CPU V_{TH}=1.25V, PCI V_{TH}=1.5V	1.5		4	nS

Note:

1. Guaranteed by design, not subject to 100% production testing.

Preliminary Information

Electrical Characteristics—CPU Outputs

T_A=0°C to 70°C; Supply Voltage V_{DD}=3.3V±5%; V_{DDL}=2.5V±5% (unless otherwise stated)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{OL}	Output Low Voltage	I_{OL}=1 mA			0.5	V
V_{OH}	Output High Voltage	I_{OH}=-1 mA	2.0			V
I_{OL}	Output Low Current	V_{OL}=1.2 V	27		93	mA
I_{OH}	Output High Currents	V_{OH}=1.2 V	-101		-25	mA
T_R	Rise Time[1]	0.4 to 2.0 V: C_L=20 pF	0.4		1.6	nS
T_F	Fall Time[1]	2.0 to 0.4 V; C_L=20 pF	0.4		1.6	nS
D_T	Duty Cycle[1]	V_{TH}=1.25 V; C_L=20 pF	45		55	%
T_{JIT}	Jitter (Cycle-cycle)[1]	V_{TH}=1.25 V; C_L=20 pF			200	pS
T_{SK}	Skew[1]	V_{TH}=1.25 V; C_L=20 pF			175	pS
Z_O	AC Output Impedance[1]			20		Ω

Note:

1. Guaranteed by design, not subject to 100% production testing.

Electrical Characteristics—IOAPIC Outputs

T_A=0°C to 70°C; Supply Voltage V_{DD}=3.3V±5%; V_{DDL}=2.5V±5% (unless otherwise stated)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{OL}	Output Low Voltage	I_{OL}=1 mA			0.5	V
V_{OH}	Output High Voltage	I_{OH}=-1 mA	2.0			V
I_{OL}	Output Low Current	V_{OL}=1.25 V	27		93	mA
I_{OH}	Output High Currents	V_{OH}=1.2 V	-101		-25	mA
T_R	Rise Time[1]	0.4 to 2.0 V: C_L=20 pF	0.4		1.6	nS
T_F	Fall Time[1]	2.0 to 0.4 V; C_L=20 pF	0.4		1.6	nS
D_T	Duty Cycle[1]	V_{TH}=1.25 V; C_L=20 pF	45		55	%
T_{JIT}	Jitter (Cycle-cycle)[1]	V_{TH}=1.25 V; C_L=20 pF			500	pS
Z_O	AC Output Impedance[1]			15		Ω

Note:

1. Guaranteed by design, not subject to 100% production testing.

Electrical Characteristics—PCI Outputs

T_A=0°C to 70°C; Supply Voltage V_{DD}=3.3V±5%; V_{DDL}=2.5V±5% (unless otherwise stated)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{OL}	Output Low Voltage	I_{OL}=1 mA			0.5	V
V_{OH}	Output High Voltage	I_{OH}=-1 mA	2.4			V
I_{OL}	Output Low Current	V_{OL}=1.5 V	26		139	mA
I_{OH}	Output High Currents	V_{OH}=1.5 V	-189		-31	mA
T_R	Rise Time[1]	0.4 to 2.4 V: C_L=30 pF	0.5		2.0	nS
T_F	Fall Time[1]	2.4 to 0.4 V; C_L=30 pF	0.5		2.0	nS
D_T	Duty Cycle[1]	V_{TH}=1.5 V; C_L=30 pF	45		55	%
T_{JIT}	Jitter (Cycle-cycle)[1]	V_{TH}=1.5 V; C_L=30 pF			250	pS
T_{SK}	Skew[1]	V_{TH}=1.5 V; C_L=30 pF			500	pS
Z_O	AC Output Impedance[1]			30		Ω

Note:

1. Guaranteed by design, not subject to 100% production testing.

Electrical Characteristics—REF Outputs

T_A=0°C to 70°C; Supply Voltage V_{DD}=3.3V±5%; V_{DDL}=2.5V±5% (unless otherwise stated)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{OL}	Output Low Voltage	I_{OL}=1 mA			0.5	V
V_{OH}	Output High Voltage	I_{OH}=-1 mA	2.4			V
I_{OL}	Output Low Current	V_{OL}=1.5 V	25		76	mA
I_{OH}	Output High Currents	V_{OH}=1.5 V	-94		-27	mA
T_R	Rise Time[1]	0.4 to 2.4 V: C_L=20 pF	1		4	nS
T_F	Fall Time[1]	2.4 to 0.4 V; C_L=20 pF	1		4	nS
D_T	Duty Cycle[1]	V_{TH}=1.5 V; C_L=20 pF	45		55	%
T_{JIT}	Jitter (Cycle-cycle)[1]	V_{TH}=1.5 V; C_L=20 pF			500	pS
Z_O	AC Output Impedance[1]			30		Ω

Note:

1. Guaranteed by design, not subject to 100% production testing.

Preliminary Information

Electrical Characteristics—48/24 MHz Outputs

T_A=0°C to 70°C; Supply Voltage V_{DD}=3.3V±5%; V_{DDL}=2.5V±5% (unless otherwise stated)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{OL}	Output Low Voltage	I_{OL}=1 mA			0.5	V
V_{OH}	Output High Voltage	I_{OH}=-1 mA	2.4			V
I_{OL}	Output Low Current	V_{OL}=1.5 V	25		76	mA
I_{OH}	Output High Currents	V_{OH}=1.5 V	-94		-27	mA
F_{ACCU}	Frequency Accuracy[1]				167	ppm
T_R	Rise Time[1]	0.4 to 2.4 V: C_L=20 pF	1		4.0	nS
T_F	Fall Time[1]	2.4 to 0.4 V; C_L=20 pF	1		4.0	nS
D_T	Duty Cycle[1]	V_{TH}=1.5 V; C_L=20 pF	45		55	%
Z_O	AC Output Impedance[1]			40		Ω

Note:

1. Guaranteed by design, not subject to 100% production testing.

Electrical Characteristics—SDRAM outputs

T_A=0°C to 70°C; Supply Voltage V_{DD}=3.3V±5%; V_{DDL}=2.5V±5% (unless otherwise stated)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{OL}	Output Low Voltage	I_{OL}=1 mA			0.5	V
V_{OH}	Output High Voltage	I_{OH}=-1 mA	2.4			V
I_{OL}	Output Low Current	V_{OL}=0.4 V	53			mA
I_{OH}	Output High Currents	V_{OH}=2.0 V			-54	mA
T_R	Rise Time[1]	0.4 to 2.4 V: C_L=30 pF	0.5		1.6	nS
T_F	Fall Time[1]	2.4 to 0.4 V; C_L=30 pF	0.5		1.6	nS
D_T	Duty Cycle[1]	V_{TH}=1.5 V; C_L=30 pF	45		55	%
T_{JIT}	Jitter (Cycle to Cycle)[1]	V_{TH}=1.5 V; C_L=30 pF			250	pS
T_{SK}	Skew[1]	V_{TH}=1.5 V; C_L=30 pF			250	pS
Z_O	AC Output Impedance[1]			40		Ω

Note:

1. Guaranteed by design, not subject to 100% production testing.

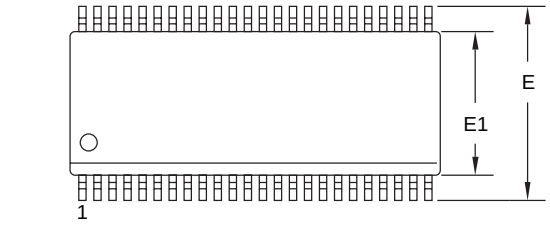
Mechanical Dimensions

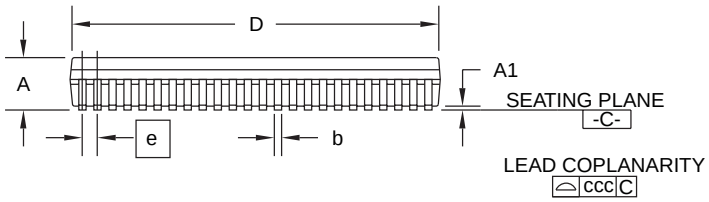
48 pin SSOP

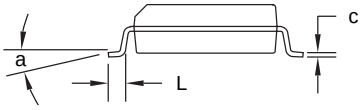
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.095	.110	2.41	2.79	
A1	.008	.016	0.20	0.41	
b	.008	.0135	0.20	0.34	5
c	.005	.010	0.13	0.25	5
D	.620	.630	15.75	16.00	2, 4
E	.395	.420	10.03	10.67	
E1	.291	.299	7.39	7.59	2
e	.025 BSC		0.64 BSC		
L	.020	.040	0.51	1.02	3
N	48		48		6
a	0°	8°	0°	8°	
ccc	---	.004	---	0.13	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
2. "D" and "E1" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "b" & "c" dimensions include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Preliminary Information

Ordering Information

Product Number	Package
RC7144	48 pin SSOP

Preliminary Information

RC7310

High Speed Driver

Features

- High output slew rate (1.2 V/ns minimum)
- Wide output voltage range (-3.0V to +8V), and up to 10 Vp-p swings
- 250 MHz minimum operation for ECL swings
- Wide input common mode range for ease of interface to ECL as well as TTL and CMOS
- Output short-circuit protection with current limiter and thermal shutdown
- 100 mA dynamic switching current drive
- Absolute slew rate control
- Low output voltage offset (30 mV typ.) and output offset drift (0.1 mV/°C typ.)
- Low input bias current (1 μA typ.) and current drift (40 nA/°C typ.) for output level program voltage allows direct coupling to a DAC output
- Available in 28-pin PLCC

Applications

- Differential line driver/receiver
- Precision waveform generator
- Level translator
- Switch driver
- Laser driver
- CRT preamplifier

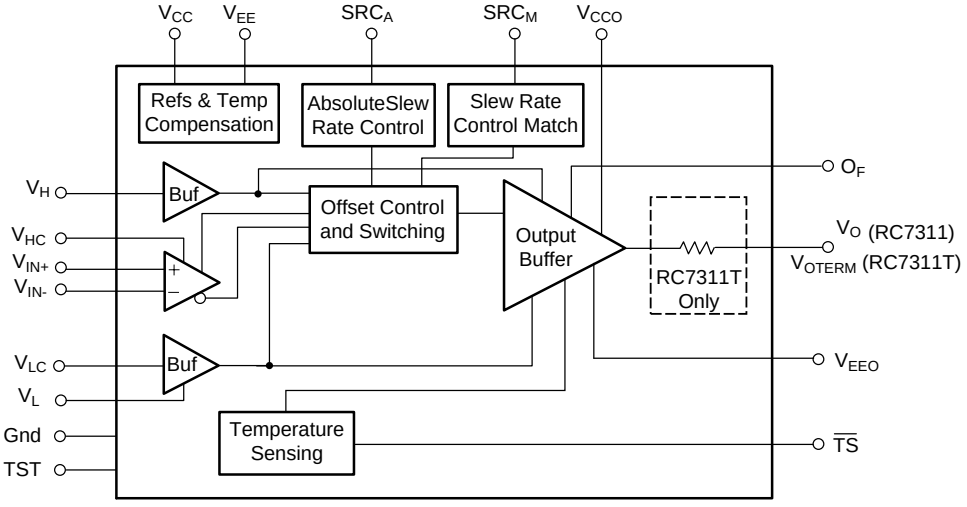
Description

The RC7310 is a low cost High Speed Driver capable of over 250 MHz operation at ECL levels and greater than 1.2 V/ns slew rate for 5 Vp-p output. The driver offers programmable output levels between -3.0V and +8V and an output amplitude up to 10 Vp-p. It is therefore capable of driving any logic family such as ECL, TTL and CMOS. The high and low limits of the output swing are set through the program pins V_H and V_L, respectively. The transfer characteristic from the program pins to the output pin is unity gain with low offset (30 mV typical) and offset drift (0.1 mV/°C typical). The V_H and V_L inputs have been buffered to operate with low bias currents (1.0 μA typical) allowing direct coupling to the output of a DAC.

The RC7310 is normally driven by ECL levels. However, the input common mode range, -2V to +6V, is wide enough to accommodate TTL or CMOS input signals. When driven with a single ended signal the other input of the RC7310 must be tied to the appropriate threshold voltage.

The RC7310 is specified at nominal power supply values of 10V and -5.2V, and commensurate output voltage swing limits of -3.0V and +8V.

Block Diagram



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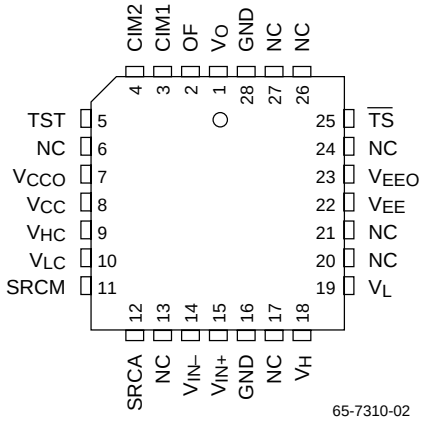
Description (continued)

The supply rails may be raised by 2V to achieve an output high level (V_{OH}) of +1 0V, or towered by 2V to achieve an output low level (V_{OL}) of -5V. At all times there must be at least a 2V margin between the positive supply and the maximum value of V_{OH}, and between the negative supply and the minimum value of V_{OL}.

The RC7310 is implemented using Fairchild Semiconductor's high performance precision Complementary Bipolar Process (CBiP).

Pin Assignments



Pin Definitions

Pin Name	Pin Number	Pin Function Description
CIM1, CIM2	3, 4	An optional 10,000 pF chip capacitor could be placed between CIM1 and CIM2 to improve impedance matching across different voltage swings. With this capacitor, output impedance stays more constant with changes in voltage swings. If not used, leave pins CIM1 and CIM2 open.
GND	16, 28	Chip ground. These pins should be connected to the printed circuit board's ground plane at the pins.
OF	2	On chip filter to improve output waveform (optional). This pin connection is optional and should be left unconnected if not used. When used, the OF pin should be fed to the termination node that is directly connected to the DUT.
SRCA	12	Absolute slew rate control. By applying current at this pin, small changes in slew rate can be programmed with an external DAC. This control pin affects both positive and negative edge rates. If this slew rate control is not desired this pin should be left open.
SRCM	11	Slew rate control matching. By applying current at this pin, small changes in slew rate can be programmed with an external DAC. This control pin adjusts the match between positive and negative edges . If this slew rate control is not desired this pin should be left open.
$\overline{TS}$	25	Active low output notifies thermal shutdown has occurred. In the event of a short-circuit or other fault that causes the die temperature to rise between 115°C and 160°C, the thermal shutdown will activate. If the fault persists, the device will toggle back and forth between shutdown and normal operation at a frequency in the tens of Hertz. $\overline{TS}$ is an open collector output capable of driving two standard TTL loads. The $\overline{TS}$ pins of several drivers may be wired together and input to a latch to indicate an alarm condition.
TST	5	Pin used for factory testing the thermal characteristics of the device. The pin should be left unconnected or tied to GND.

Pin Definitions (continued)

Pin Name	Pin Number	Pin Function Description
V_{CC}	8	Quiet positive supply. The nominal value is 10V ±3%. For output high voltage levels (V_{OH}) greater than the nominal value of +8V, V_{CC} should be raised 2V above the maximum V_{OH} value. Whenever V_{EE} is lowered to provide margin at the output low level, V_{CC} should also be lowered by the same amount. V_{CC} should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible.
V_{CCO}	7	Positive supply for the output stage. This supply is brought out separately to minimize the supply noise generated when the output switches. V_{CCO} should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible and then immediately connected to V_{CC}.
V_{EE}	22	Quiet negative supply. The nominal value is -5.2V to ±5%. For output low voltage levels (V_{OL}) less than 3V, V_{EE} should be lowered 2V below the minimum V_{OL} value. Whenever V_{CC} is raised to provide margin at the output high level, V_{EE} should be raised by the same amount. V_{EE} should be bypassed to ground with a 10,000 pF chip capacitor placed as close to the pins as possible.
V_{EEO}	23	Negative supply for the output stage. This supply is brought out separately to minimize the supply noise generated when the output switches. V_{EEO} should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible and then immediately connected to V_{EE}.
V_H	18	Analog program input that sets the output high level (V_{OH}). The transfer characteristic from V_H to V_{OH} is nominally unity gain.
V_{HC}	9	Bypass for analog program input high, V_H. V_{HC} should be bypassed to the ground plane with a 1000 pF chip capacitor placed as close to the pin as possible.
V_{IN+}, V_{IN-}	15, 14	Differential digital inputs. The output will toggle between the two levels dictated by V_H and V_L as the differential signal is switched. Although these inputs will normally be driven by ECL signals, they have a wide enough common mode range that any one of the inputs may be driven by a TTL or CMOS signal provided that the other input is tied to the appropriate threshold voltage.
V_L	19	Analog program input that sets the output low level (V_{OL}). The transfer characteristic from V_L to V_{OL} is nominally unity gain.
V_{LC}	10	Bypass for analog program input low, V_L. V_{LC} should be bypassed to the ground plane with a 1000 pF chip capacitor placed as close to the pin as possible.
V_O	1	Driver output of RC7310. The output impedance is 12.6Ω ±1.5Ω. The output is usually back terminated in the characteristic impedance of the driven transmission line. For a 50Ω line, a 37.4Ω ±1% or better resistor should be placed externally as close to the output pin as possible to minimize reflections and ringing. The resistor should also be able to dissipate 0.8Ω to sustain the short circuit current of the output.
NC	6, 13, 17, 20, 21, 24, 26, 27	No connection.

Absolute Maximum Ratings[1]

Parameter		Min.	Max.	Unit
Positive power supply, V_{CC}			13	V
Negative power supply, V_{EE}			-8.2	V
Difference between V_{CC} and V_{EE}			16	V
Input voltage at V_{IN+}, V_{IN-}	V_{CC}	-12		V
	V_{EE}		+12	
Input voltage at V_H, V_L	V_{CC}	-13		V
	V_{EE}		+13	
Differential input voltage, $\lvert V_{IN+} - V_{IN-} \rvert$			6	V
Difference between V_H and V_L, ($\lvert V_H - V_L \rvert$)			13	V
Driver output voltage	V_{CC}	-13		V
	V_{EE}		+13	
Output voltage at $\overline{TS}$			7	V
Duration of short-circuit to ground		Indefinite		
Operating temperature range		0	70	°C
Storage temperature range		-65	+125	°C
Lead temperature range (soldering 10 seconds)			300	°C

Notes:

1. Absolute Maximum Ratings are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. If the device is subjected to the limits in the absolute maximum ratings for extended periods, its reliability may be impaired. The tables of Electrical Characteristics provide conditions for actual device operation.

Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
TC	Case operating temperature[1]	0		70	°C
V_{CC}	Positive supply voltage	9.7	10.0	10.3	V
V_{EE}	Negative supply voltage	-5.45	-5.2	-4.95	V
$V_{CC} – V_{EE}$	Difference between positive and negative supply		15.2	15.8	V
V_{OH}, V_{OL}	Range for output high level and output low level	V_{EE}+2		V_{CC}–2	V
$\lvert V_{OH} – V_{OL}\rvert$	Output amplitude	0.4		10.0	V
R_T	Output back-termination resistor for RC7310		37.4		Ω

Note:

1. With air flow >300 lfpm.

DC Electrical Characteristics

V_{CC} = 10V ±3%, V_{EE} = -5.2V ±5%, T_A = 25°C (still air), no load, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Differential Inputs, V_{IN+}, $V_{IN–}$						
V_{IN+}, $V_{IN–}$	Absolute Input Voltage		-2.0		+6.0	V
V_{ID}	Differential Input Range	$\lvert V_{IN+} – V_{IN–}\rvert$	0.4	ECL	5.0	V
I_{IN+}, $I_{IN–}$	Bias Current	-2V ≤ $V_{IN±}$ ≤ +6V		-100	-250	µA
Absolute SLR Control, SRCA						
V_{SRCA}	Compliance Voltage Range	V_H = +5V, V_L= 0V	-2.3	-1.6	-0.9	V
I_{SRCA}	Control Current Range		-1.0		+1.0	mA
$\%_{SLR}$Max	%SLR Absolute Change	V_{com} = -2.0		-20		%
$\%_{SLR}$Max	%SLR Absolute Change	V_{com} = -2.4		-40/+25		%
Matching SLR Control, SRCM						
V_{SRCM}	Compliance Voltage Range	V_H = +5V, V_L= 0V	0.4	0.6	0.9	V
I_{SRCM}	Control Current Range		-0.5		+0.5	mA
$\%_{SLR}$	Max % SLR Matching Change			30		%
Voltage Program Inputs V_H, V_L						
V_H	V_H Range	V_{CC} = 10V, V_{EE} = -5.2V	-1.0		+8.0	V
		V_{CC} = 12V, V_{EE} = -3.2V	+1.0		+10.0	V
		V_{CC} = 8V, V_{EE} = -7.2V	-3.0		+6.0	V
V_L	V_L Range	V_{CC} = 10V, V_{EE} = -5.2V	-3.0		+5.5	V
		V_{CC} = 12V, V_{EE} = -3.2V	-1.0		+7.5	V
		V_{CC} = 8V, V_{EE} = -7.2V	-5.0		+3.5	V
V_A	$\lvert V_{OH} – V_{OL}\rvert$	Output Voltage Amplitude	0.40		10	V
I_H	Bias Current @ V_H	-1.0V ≤ V_H ≤ +8V; V_L = -3.0V		-1.0	-5.0	µA
I_L	Bias Current @ V_L	-3V ≤ V_L ≤ +5.5V; V_H +8.0V		-1.0	-5.0	µA
TCI_H	Max. Temperature Drift in I_H	V_H = 7.0V; 25°C ≤ T_A ≤ 70°C; (output not switching)			40	nA/°C
TCI_L	Max. Temperature Drift in I_L	VL = -2.0V; 25°C ≤ TC ≤ 70°C; (output not switching)			40	nA/°C

DC Electrical Characteristics (continued)

V_{CC} = 10V ±3%, V_{EE} = -5.2V ±5%, T_A = 25°C (still air), no load, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ΔIBDC	Variation in I_H, I_L with Power Supply and DC Voltage at V_H or V_L	V_H = -1.0V to +8V; V_L = -3V to +5.5V	-2.0		+2.0	µA
$V_{H,L}$BW	$V_{H,L}$ BW	-3 dB point from $V_{H,L}$BW to V_{OUT}		50		kHz
Signal Output V_O, V_{OTERM}						
V_{OH}	Range for High Level Voltage	V_{CC} = 10V, V_{EE} = -5.2V	-1.0		+8.0	V
		V_{CC} = 12V, V_{EE} = -3.2V	+1.0		+10.0	V
		V_{CC} = 8V, V_{EE} = -7.2V	-3.0		+6.0	V
V_{OL}	Range for Low Level Voltage	V_{CC} = 10V, V_{EE} = -5.2V	-3.0		+5.5	V
		V_{CC} = 12V, V_{EE} = -3.2V	+1.0		+7.5	V
		V_{CC} = 8V, V_{EE} = -7.2V	-5.0		+3.5	V
δV_{OH}	Offset to Output High Level	$\delta V_{OH} = \lvert V_H - V_{OH} \rvert$, V_H = 0V, V_L = -3V, -1.0V ≤ V_H ≤ +8V, V_L = -2V		30	100	mV
δV_{OL}	Offset to Output Low Level	$\delta V_{OL} = \lvert V_L - V_{OL} \rvert$, V_H = 8V, V_L = 0V, -3V ≤ V_L ≤ +5.5V, V_L = +7V		30	100	mV
VTC	Output Voltage Drift	-3V ≤ V_L ≤ +5.5V, -1.0V ≤ V_H ≤ +8V		0.1	0.5	mV/°C
ε_G	Gain Error	-3.0V ≤ V_L ≤ +5.5V, V_H = +8V, -1.0V ≤ V_H ≤ +7.5V, V_L = -3V	-1.0		+1.0	%V_{SET}
ε_L	Linearity Error	0V ≤ V_L ≤ +5V, V_H = +8V, 0V ≤ V_H ≤ +5V, V_L = -3V	-0.3		+0.3	%V_{SET}
		-3.0V ≤ V_L ≤ +5.5V, V_H = +8V, -1.0V ≤ V_H ≤ +7.5V, V_L = -3V	-0.5		+0.5	%V_{SET}
Z_{OUT}	Output Impedance	V_O (RC7310)		12.6		Ω
I_{AC}	AC Current Drive		70	100		mA
I_{DC}	DC Current Drive		50			mA
Thermal Shutdown Output (TS)						
V_{OL}	Output Low Level	I_{OL} = 4 mA			0.5	V
I_{CL}	DC Current Limit		70	110	130	mA
TS	Shutdown Die Temperature		115	130	160	°C
Other						
I_{CC}	Positive Supply Current			60		mA
I_{EE}	Negative Supply Current			60		mA
$PSRV_O$	Output Level to Power Supply Rejection Ratio	V_{CC}; ΔV_{CC} = ±2.5% V_{EE}; ΔV_{EE} = ±2.5%	40 40			dB dB
$PSRV_{SL}$	Output Slew Rate to Power Supply Rejection Ratio	V_{CC}; ΔV_{CC} = ±200mV V_{EE}; ΔV_{EE} = ±200mV			4 4	% %
T_A	Operating Temperature Range	Still Air	0	25	50	°C
		Air Flow > 300 lfpm	0	25	70	°C

AC Electrical Characteristics

V_{CC} = 10V ±3%, V_{EE} = -5.2V ±5%, T_A = 25°C (still air) and the load is a 50Ω transmission line with 2.0 ns one-way delay, unless otherwise specified. The transmission line should be back-terminated in 50Ω (±1%) using an extemal resistor. The measurement probe is a high impedance FET probe with capacitance no greater than 6 pF and resistance no smaller than 10 kΩ.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SLR	Slew Rate (SRCM and SRCA Adjusted)	$V_H - V_L$ = 5V; measured between 20% and 80% points				
		With probe only as load	1.2	1.6		V/ns
		With probe and transmission line	1.1	1.5		V/ns
SLR	Slew Rate (No SRCM and SRCA Adjustment)	$V_H - V_L$ = 5V; measured between 20% and 80% points				
		With probe only as load	1.0	1.4		V/ns
		With probe and transmission line	1.0	1.4		V/ns
t_R, t_F	Rise Time and Fall Time (SRCM and SRCA Adjusted)	Load is Probe Only				
		Amplitude = 0.8V (20% to 80%)		0.6	0.8	ns
		3V (10% to 90%)		1.7	2.0	ns
		5V (10% to 90%)		2.4	2.9	ns
		9V (10% to 90%)		4.0	4.8	ns
t_R, t_F	Rise Time and Fall Time (No SRCM and SRCA Adjustment)	Load is Probe Only				
		Amplitude = 0.8V (20% to 80%)		0.7	1.0	ns
		3V (10% to 90%)		2.0	2.4	ns
		5V (10% to 90%)		2.8	3.6	ns
		9V (10% to 90%)		4.8		ns
f	Toggle Rate	Amplitude = 0.8V	250	270		MHz
		Amplitude = 5.0V	105	110		MHz
Propagation Delay						
t_{PLH}	Low to High	f = 10 MHz; V_{OH} = +0.4V; V_{OL}= -0.4V		1.6	2.0	ns
t_{PHL}	High to Low			1.6	2.0	ns
Δt_P	Matching $\lvert t_{PLH} - t_{PHL} \rvert$			150	175	ps
$\Delta t_P TC$	Temperature Coefficient			2		ps/°C
tPW_{MIN}	Minimum Pulse Width	$V_H - V_L$ = 2.0V; Pulse Width at which amplitude drops by 50mV, measured between 50% points	2.0			ns
$\Delta t_P PW$	Propagation Delay Variation with Pulse Width	2ns < PW < 98ns; f = 10 MHz; V_{OH} = +0.4V; V_{OL} = -0.4V	-75		+75	ps
PS	Preshoot	0.5V < $\lvert V_{OH} - V_{OL} \rvert$ < 5V		15 mV + 3% of VA		mV
OS	Overshoot	0.5V < $\lvert V_{OH} - V_{OL} \rvert$ < 5V		50 mV + 4% of VA		mV
t_S	Output Setting Time	$\lvert V_{OH} - V_{OL} \rvert$ = 5V				
		To within 3% of $\lvert V_{OH} - V_{OL} \rvert$		5		ns
		To within 1% of $\lvert V_{OH} - V_{OL} \rvert$		10		ns

Notes:

Notes:

Notes:

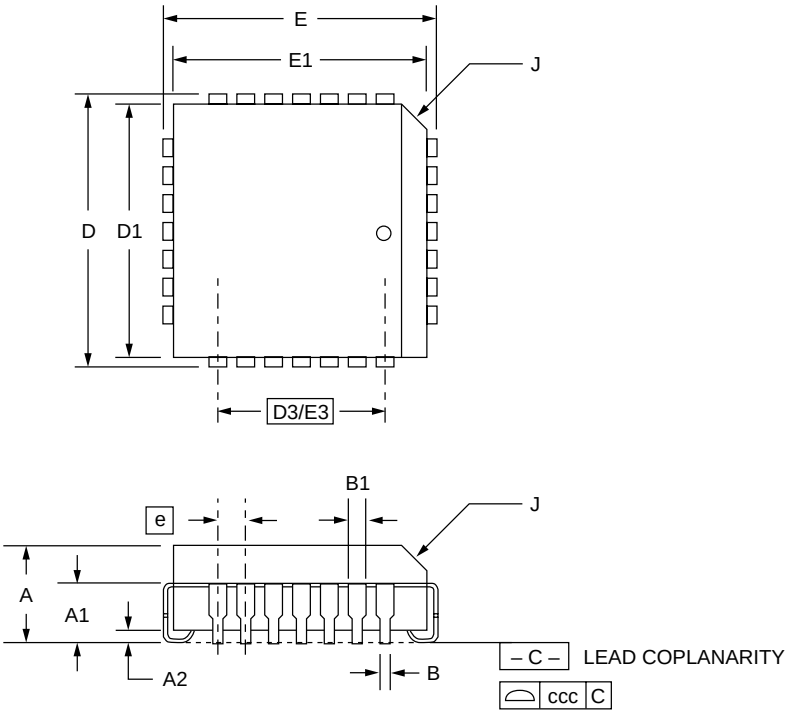
Mechanical Dimensions

28-Lead PLCC

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.180	4.19	4.57	
A1	.090	.120	2.29	3.05	
A2	.020	—	.51	—	
B	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D/E	.485	.495	12.32	12.57	
D1/E1	.450	.456	11.43	11.58	3
D3/E3	.300 BSC		7.62 BSC		
e	.050 BSC		1.27 BSC		
J	.042	.048	1.07	1.22	2
ND/NE	7		7		
N	28		28		
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982
2. Corner and edge chamfer (J) = 45°
3. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is .101" (.25mm)



Ordering Information

Part Number	Package	Operating Temperature Range
RC7310QA	28-Pin PLCC	0°C to +70°C

RC7311

250MHz ATE Pin Electronics Driver

Features

- High output slew rate (1.8 V/ns typical)
- Wide output voltage range (-3.0V to +8V), and up to 10 Vp-p swings
- 250MHz minimum operation for ECL swings
- Wide input common mode range for ease of interface to ECL as well as TTL and CMOS
- Output short-circuit protection with current limiter and thermal shutdown
- 100mA dynamic switching current drive
- Absolute slew rate control
- Available in 28-Lead PLCC
- Low output voltage offset (30mV) and output offset drift (0.1 mV/°C typ.)
- Low input bias current (1 μA typical) and current drift (40 nA/°C) for output level program allows direct coupling to a DAC output

Applications

- ATE pin electronics driver
- Precision waveform generator
- Level translator
- Differential line receiver
- General purpose driver
- Switch driver
- Laser driver
- CRT preamplifier

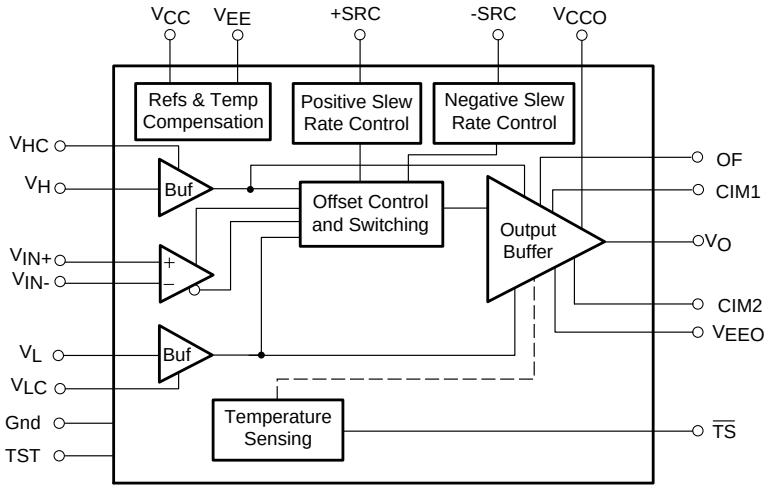
Description

The RC7311 Pin Electronics Driver is an economical alternative to standard pin electronics drivers in applications that do not require three state capability in the driver. An example of such an application would be the large number of input address pins found in memory testers.

The driver output levels are programmable between -3.0V and +8V to drive ECL, TTL and CMOS logic families. The peak to peak output swing can vary from values lower than 300mV to values as high as 10V. With toggle rates greater than 250MHz for ECL signals and typical slew rates of 2 V/ns for 5 Vp-p signal amplitudes, the RC7311 is comparable with the requirements of state-of-the-art testers. The high and low limits of the output swing are set through the program pins V_H and V_L, respectively. The transfer characteristic from the program pins to the output pin is unity gain with low offset (30mV) and offset drift (0.1 mV/°C typical). The V_H and V_L inputs have been buffered to operate with low bias currents (1.0 μA typical) allowing direct coupling to the output of a DAC.

The RC7311 is provided with high speed differential ECL inputs for ease of interface with the differential ECL outputs of a timing generator. The inputs have a wide voltage range, -2V to +6V, so that if required, an input may be driven by TTL or CMOS devices provided that the other input is tied to the appropriate threshold value.

Block Diagram



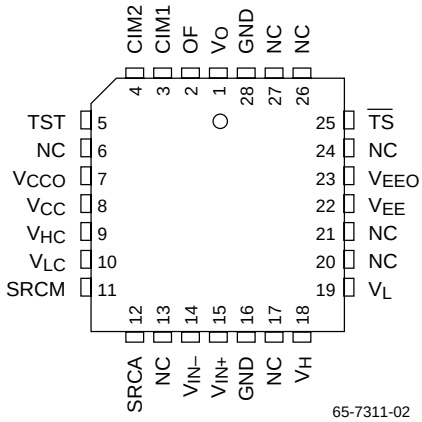
65-7311-01

Description (continued)

The RC7311 is specified at nominal power supply values of 10V and -5.2V, and commensurate output voltage swing limits of -3.0V and +8V. The supply rails may be raised by 2V to achieve an output high level (V_{OH}) of +10V, or lowered by 2V to achieve an output low level (V_{OL}) of -5V. At all times there must be at least a 2V margin between the positive supply and the maximum value of V_{OH}, and between the negative supply and the minimum value of V_{OL}.

The RC7311 is implemented using Fairchild Semiconductor's high performance precision complementary bipolar process.

Pin Assignments



Pin Definitions

Pin Name	Pin Number	Pin Function Description
CIM1, CIM2	3, 4	An optional 10,000 pF chip capacitor could be placed between CIM1 and CIM2 to improve impedance matching across different voltage swings. With this capacitor, output impedance stays more constant with changes in voltage swings. If not used, leave pins CIM1 and CIM2 open.
GND	16, 28	Chip ground. These pins should be connected to the printed circuit board's ground plane at the pins.
OF	2	On chip filter to improve output waveform (optional). This pin connection is optional and should be left unconnected if not used. When used, the OF pin should be fed to the termination node that is directly connected to the DUT.
SRCA	12	Absolute slew rate control. By applying current at this pin, small changes in slew rate can be programmed with an external DAC. This control pin affects both positive and negative edge rates. If this slew rate control is not desired this pin should be left open.
SRCM	11	Slew rate control matching. By applying current at this pin, small changes in slew rate can be programmed with an external DAC. This control pin adjusts the match between positive and negative edges . If this slew rate control is not desired this pin should be left open.
$\overline{TS}$	25	Active low output notifies thermal shutdown has occurred. In the event of a short-circuit or other fault that causes the die temperature to rise between 115°C and 160°C, the thermal shutdown will activate. If the fault persists, the device will toggle back and forth between shutdown and normal operation at a frequency in the tens of Hertz. $\overline{TS}$ is an open collector output capable of driving two standard TTL loads. The $\overline{TS}$ pins of several drivers may be wired together and input to a latch to indicate an alarm condition.
TST	5	Pin used for factory testing the thermal characteristics of the device. The pin should be left unconnected or tied to GND.

Pin Definitions (continued)

Pin Name	Pin Number	Pin Function Description
V_{CC}	8	Quiet positive supply. The nominal value is 10V ±3%. For output high voltage levels (V_{OH}) greater than the nominal value of +8V, V_{CC} should be raised 2V above the maximum V_{OH} value. Whenever V_{EE} is lowered to provide margin at the output low level, V_{CC} should also be lowered by the same amount. V_{CC} should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible.
V_{CCO}	7	Positive supply for the output stage. This supply is brought out separately to minimize the supply noise generated when the output switches. V_{CCO} should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible and then immediately connected to V_{CC}.
V_{EE}	22	Quiet negative supply. The nominal value is -5.2V to ±5%. For output low voltage levels (V_{OL}) less than 3V, V_{EE} should be lowered 2V below the minimum V_{OL} value. Whenever V_{CC} is raised to provide margin at the output high level, V_{EE} should be raised by the same amount. V_{EE} should be bypassed to ground with a 10,000 pF chip capacitor placed as close to the pins as possible.
V_{EEO}	23	Negative supply for the output stage. This supply is brought out separately to minimize the supply noise generated when the output switches. V_{EEO} should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible and then immediately connected to V_{EE}.
V_H	18	Analog program input that sets the output high level (V_{OH}). The transfer characteristic from V_H to V_{OH} is nominally unity gain.
V_{HC}	9	Bypass for analog program input high, V_H. V_{HC} should be bypassed to the ground plane with a 1000 pF chip capacitor placed as close to the pin as possible.
V_{IN+}, V_{IN-}	15, 14	Differential digital inputs. The output will toggle between the two levels dictated by V_H and V_L as the differential signal is switched. Although these inputs will normally be driven by ECL signals, they have a wide enough common mode range that any one of the inputs may be driven by a TTL or CMOS signal provided that the other input is tied to the appropriate threshold voltage.
V_L	19	Analog program input that sets the output low level (V_{OL}). The transfer characteristic from V_L to V_{OL} is nominally unity gain.
V_{LC}	10	Bypass for analog program input low, V_L. V_{LC} should be bypassed to the ground plane with a 1000 pF chip capacitor placed as close to the pin as possible.
V_O	1	Driver output of RC7311. The output impedance is 12.6Ω ±1.5Ω. The output is usually back terminated in the characteristic impedance of the driven transmission line. For a 50Ω line, a 37.4Ω ±1% or better resistor should be placed externally as close to the output pin as possible to minimize reflections and ringing. The resistor should also be able to dissipate 0.8Ω to sustain the short circuit current of the output.
NC	6, 13, 17, 20, 21, 24, 26, 27	No connection.

Absolute Maximum Ratings[1]

Parameter		Min.	Max.	Unit
Positive power supply, V_{CC}			13	V
Negative power supply, V_{EE}			-8.2	V
Difference between V_{CC} and V_{EE}			16	V
Input voltage at V_{IN+}, V_{IN-}	V_{CC}	-12		V
	V_{EE}		+12	
Input voltage at V_H, V_L	V_{CC}	-13		V
	V_{EE}		+13	
Differential input voltage, $\lvert V_{IN+} - V_{IN-}\rvert$			6	V
Difference between V_H and V_L, ($\lvert V_H - V_L\rvert$)			13	V
Driver output voltage	V_{CC}	-13		V
	V_{EE}		+13	
Output voltage at $\overline{TS}$			7	V
Duration of short-circuit to ground		Indefinite		
Operating temperature range		0	70	°C
Storage temperature range		-65	+125	°C
Lead temperature range (soldering 10 seconds)			300	°C

Notes:

1. Absolute Maximum Ratings are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. If the device is subjected to the limits in the absolute maximum ratings for extended periods, its reliability may be impaired. The tables of Electrical Characteristics provide conditions for actual device operation.

Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
TC	Case operating temperature[1]	0		70	°C
V_{CC}	Positive supply voltage	9.7	10.0	10.3	V
V_{EE}	Negative supply voltage	-5.45	-5.2	-4.95	V
$V_{CC} - V_{EE}$	Difference between positive and negative supply		15.2	15.8	V
V_{OH}, V_{OL}	Range for output high level and output low level	V_{EE}+2		V_{CC}–2	V
$\lvert V_{OH} - V_{OL}\rvert$	Output amplitude	0.4		10.0	V
R_T	Output back-termination resistor for RC7310		37.4		Ω

Note:

1. With air flow >300 lfpm.

DC Electrical Characteristics

V_{CC} = 10V ±3%, V_{EE} = -5.2V ±5%, T_A = 25°C (still air), no load, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Differential Inputs, V_{IN+}, V_{IN-}						
V_{IN+}, V_{IN-}	Absolute Input Voltage		-2.0		+6.0	V
V_{ID}	Differential Input Range	$\lvert V_{IN+} - V_{IN-} \rvert$	0.4	ECL	5.0	V
I_{IN+}, I_{IN-}	Bias Current	-2V ≤ $V_{IN\pm}$ ≤ +6V		-100	-250	µA
Absolute SLR Control, SRCA						
V_{SRCA}	Compliance Voltage Range	V_H = +5V, V_L= 0V	-2.3	-1.6	-0.9	V
I_{SRCA}	Control Current Range		-1.5		+1.5	mA
$\%_{SLR}$Max	%SLR Absolute Change	V_{com} = -2.0		-20		%
$\%_{SLR}$Max	%SLR Absolute Change	V_{com} = -2.4		-40/+25		%
Matching SLR Control, SRCM						
V_{SRCM}	Compliance Voltage Range	V_H = +5V, V_L= 0V	0.3	0.6	0.9	V
I_{SRCM}	Control Current Range		-0.5		+0.5	mA
$\%_{SLR}$	Max % SLR Matching Change			30		%
Voltage Program Inputs V_H, V_L						
V_H	V_H Range	V_{CC} = 10V, V_{EE} = -5.2V	-1.0		+8.0	V
		V_{CC} = 12V, V_{EE} = -3.2V	+1.0		+10.0	V
		V_{CC} = 8V, V_{EE} = -7.2V	-3.0		+6.0	V
V_L	V_L Range	V_{CC} = 10V, V_{EE} = -5.2V	-3.0		+5.5	V
		V_{CC} = 12V, V_{EE} = -3.2V	-1.0		+7.5	V
		V_{CC} = 8V, V_{EE} = -7.2V	-5.0		+3.5	V
V_A	$\lvert V_{OH} - V_{OL} \rvert$	Output Voltage Amplitude	0.30		10	V
I_H	Bias Current @ V_H	-1.0V ≤ V_H ≤ +8V; V_L = -3.0V		-1.0	-5.0	µA
I_L	Bias Current @ V_L	-3V ≤ V_L ≤ +5.5V; V_H +8.0V		-1.0	-5.0	µA
TCI_H	Max. Temperature Drift in I_H	V_H = 7.0V; 25°C ≤ T_A ≤ 70°C; (output not switching)			40	nA/°C
TCI_L	Max. Temperature Drift in I_L	VL = -2.0V; 25°C ≤ TC ≤ 70°C; (output not switching)			40	nA/°C
ΔIBDC	Variation in I_H, I_L with Power Supply and DC Voltage at V_H or V_L	V_H = -1.0V to +8V; V_L = -3V to +5.5V	-1.8		+1.8	µA
$V_{H,L}$BW	$V_{H,L}$ BW	-3 dB point from $V_{H,L}$BW to V_{OUT}		50		kHz
Signal Output V_O, V_{OTERM}						
V_{OH}	Range for High Level Voltage	V_{CC} = 10V, V_{EE} = -5.2V	-1.0		+8.0	V
		V_{CC} = 12V, V_{EE} = -3.2V	+1.0		+10.0	V
		V_{CC} = 8V, V_{EE} = -7.2V	-3.0		+6.0	V
V_{OL}	Range for Low Level Voltage	V_{CC} = 10V, V_{EE} = -5.2V	-3.0		+5.5	V
		V_{CC} = 12V, V_{EE} = -3.2V	+1.0		+7.5	V
		V_{CC} = 8V, V_{EE} = -7.2V	-5.0		+3.5	V
δV_{OH}	Offset to Output High Level	$\delta V_{OH} = \lvert V_H - V_{OH} \rvert$, V_H = 0V, V_L = -3V, -1.0V ≤ V_H ≤ +8V, V_L = -2V		30	50	mV

DC Electrical Characteristics (continued)

V_{CC} = 10V ±3%, V_{EE} = -5.2V ±5%, T_A = 25°C (still air), no load, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
δV_{OL}	Offset to Output Low Level	$\delta V_{OL} = \lvert V_L - V_{OL} \rvert$, V_H = 8V, V_L = 0V, -3V ≤ V_L ≤ +5.5V, V_L = +7V		30	50	mV
VTC	Output Voltage Drift	-3V ≤ V_L ≤ +5.5V, -1.0V ≤ V_H ≤ +8V		0.1	0.5	mV/°C
ε_G	Gain Error	-3.0V ≤ V_L ≤ +5.5V, V_H = +8V, -1.0V ≤ V_H ≤ +7.5V, V_L = -3V	-1.0		+1.0	%V_{SET}
ε_L	Linearity Error	0V ≤ V_L ≤ +5V, V_H = +8V, 0V ≤ V_H ≤ +5V, V_L = -3V	-0.3		+0.3	%V_{SET}
		-3.0V ≤ V_L ≤ +5.5V, V_H = +8V, -1.0V ≤ V_H ≤ +7.5V, V_L = -3V	-0.5		+0.5	%V_{SET}
Z_{OUT}	Output Impedance	V_O (RC7311)		12.6		Ω
I_{AC}	AC Current Drive		70	100		mA
I_{DC}	DC Current Drive		50			mA
Thermal Shutdown Output (TS)						
V_{OL}	Output Low Level	I_{OL} = 4 mA			0.5	V
I_{CL}	DC Current Limit		70	110	130	mA
TS	Shutdown Die Temperature		115	130	160	°C
Other						
I_{CC}	Positive Supply Current			60		mA
I_{EE}	Negative Supply Current			60		mA
$PSRV_O$	Output Level to Power Supply Rejection Ratio	V_{CC}; ΔV_{CC} = ±2.5% V_{EE}; ΔV_{EE} = ±2.5%	40 40			dB dB
$PSRV_{SL}$	Output Slew Rate to Power Supply Rejection Ratio	V_{CC}; ΔV_{CC} = ±200mV V_{EE}; ΔV_{EE} = ±200mV			4 4	% %
T_A	Operating Temperature Range	Still Air	0	25	50	°C
		Air Flow > 300 lfpm	0	25	70	°C

AC Electrical Characteristics

V_{CC} = 10V ±3%, V_{EE} = -5.2V ±5%, TA = 25°C (still air) and the load is a 50Ω transmission line with 2.0 ns one-way delay, unless otherwise specified. The transmission line should be back-terminated in 50Ω (±1%) using an extemal resistor. The measurement probe is a high impedance FET probe with capacitance no greater than 6 pF and resistance no smaller than 10 kΩ.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SLR	Slew Rate (SRCM and SRCA Adjusted)	$V_H - V_L$ = 5V; measured between 20% and 80% points				
		With probe only as load	1.6	1.8		V/ns
		With probe and transmission line	1.5	1.7		V/ns
SLR	Slew Rate (No SRCM and SRCA Adjustment)	$V_H - V_L$ = 5V; measured between 20% and 80% points				
		With probe only as load	1.4	1.6		V/ns
		With probe and transmission line	1.35	1.5		V/ns
t_R, t_F	Rise Time and Fall Time (SRCM and SRCA Adjusted)	Load is Probe Only				
		Amplitude = 0.8V (20% to 80%)		0.60	0.5	ns
		Amplitude = 3V (10% to 90%)		1.7	1.9	ns
		Amplitude = 5V (10% to 90%)		2.4	2.8	ns
		Amplitude = 9V (10% to 90%)		4.0	4.5	ns
t_R, t_F	Rise Time and Fall Time (No SRCM and SRCA Adjustment)	Load is Probe Only				
		Amplitude = 0.8V (20% to 80%)		0.7	0.9	ns
		Amplitude = 3V (10% to 90%)		1.8	2.2	ns
		Amplitude = 5V (10% to 90%)		2.6	3.2	ns
		Amplitude = 9V (10% to 90%)		4.5	5.2	ns
f	Toggle Rate	Amplitude = 0.8V	250	270		MHz
		Amplitude = 5.0V	105	110		MHz
Propagation Delay						
t_{PLH}	Low to High	f = 10 MHz; V_{OH} = +0.4V; V_{OL}= -0.4V		1.6	1.9	ns
t_{PHL}	High to Low			1.6	1.9	ns
Δt_P	Matching $\lvert t_{PLH} - t_{PHL} \rvert$			150		ps
$\Delta t_P TC$	Temperature Coefficient			2		ps/°C
tPW_{MIN}	Minimum Pulse Width	$V_H - V_L$ = 2.0V; Pulse Width at which amplitude drops by 50mV, measured between 50% points	2.0			ns
$\Delta t_P PW$	Propagation Delay Variation with Pulse Width	2ns < PW < 98ns; f = 10 MHz; V_{OH} = +0.4V; V_{OL} = -0.4V	-75		+75	ps
PS	Preshoot	0.5V < $\lvert V_{OH} - V_{OL} \rvert$ < 5V			15 mV + 3% of VA	mV
OS	Overshoot	0.5V < $\lvert V_{OH} - V_{OL} \rvert$ < 5V			50 mV + 4% of VA	mV
t_S	Output Setting Time	$\lvert V_{OH} - V_{OL} \rvert$ = 5V				
		To within 3% of $\lvert V_{OH} - V_{OL} \rvert$		5		ns
		To within 1% of $\lvert V_{OH} - V_{OL} \rvert$		10		ns

Notes:

Notes:

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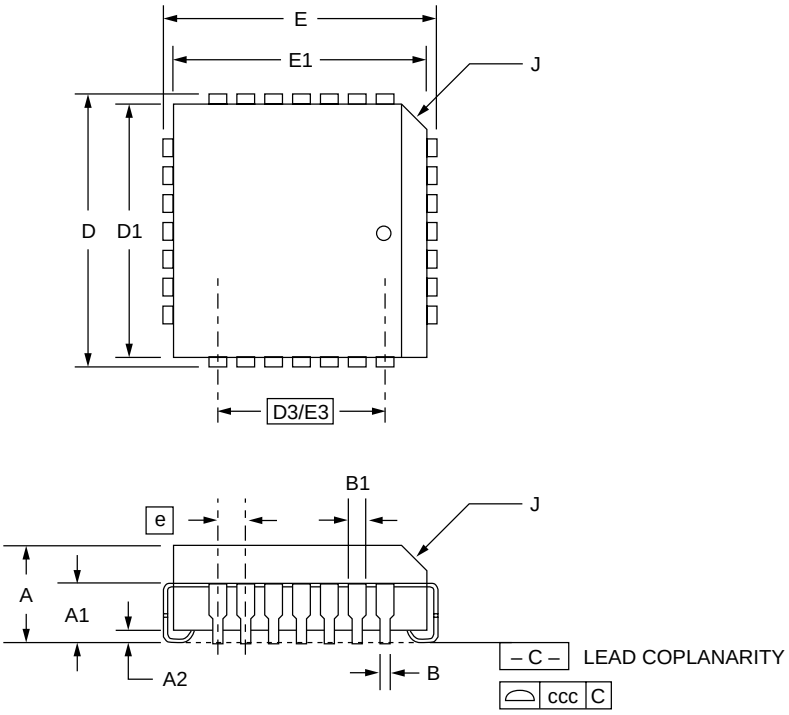
Mechanical Dimensions

28-Lead PLCC

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.180	4.19	4.57	
A1	.090	.120	2.29	3.05	
A2	.020	—	.51	—	
B	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D/E	.485	.495	12.32	12.57	
D1/E1	.450	.456	11.43	11.58	3
D3/E3	.300 BSC		7.62 BSC		
e	.050 BSC		1.27 BSC		
J	.042	.048	1.07	1.22	2
ND/NE	7		7		
N	28		28		
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982
2. Corner and edge chamfer (J) = 45°
3. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is .101" (.25mm)



Ordering Information

Part Number	Package	Operating Temperature Range
RC7311QA	28-Pin PLCC	0°C to +70°C

RC7315

Three-State ATE Pin Electronics Driver

Features

- High output slew rate (1.8 V/ns typical)
- Wide output voltage range (-2.5V to +7V), and up to 9.5 Vp-p swings
- Three-state/high impedance output
- High repetition rate (250 MHz for ECL swings)
- Low output offset (20 mV typical) and output offset drift (0.1 mV/°C typical).
- Low leakage (10 nA typical) and low output capacitance (3 pF typical) in high impedance inhibit mode
- High speed differential inputs with wide common mode range for ease of interface to ECL as well as TTL and CMOS levels
- Output short circuit protection (Safe Operating Area protection with current limiting and thermal shutdown)
- 100 mA typical dynamic current drive capability
- Absolute slew rate control
- Available in 28-pin PLCC
- Packaged parts available in unterminated configurations

Applications

- ATE pin electronics driver
- Precision waveform generator
- Level translator
- Differential line receiver
- General purpose driver
- Laser driver
- CRT preamplifier

Description

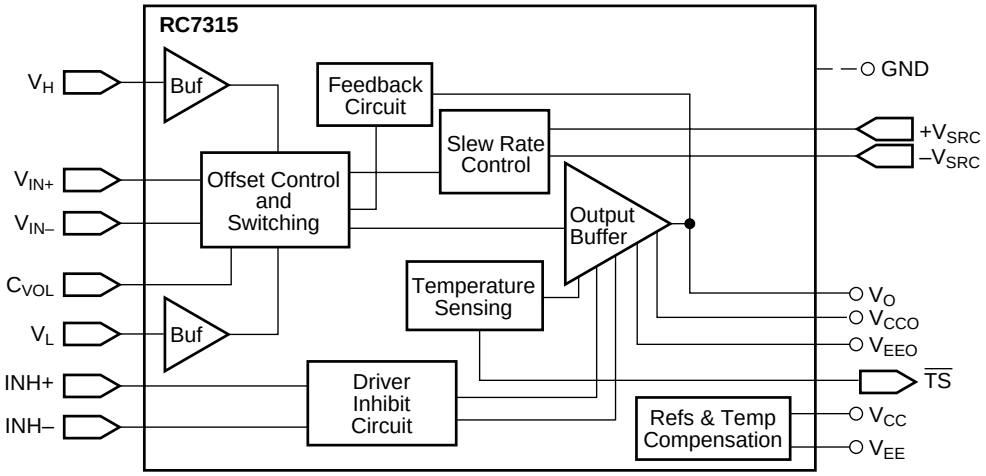
The RC7315 Pin Electronics Driver is designed for use in all high speed ATE systems which require pin drivers with three state capability and high slew rates. The RC7315 has the ability to drive a 50Ω transmission line of up to 2 feet in length with a slew rate of 1.8 V/ns and repetition rate of over 250 MHz for ECL output levels. These features, combined with a maximum output swing of 9.5 Vp-p over the range of -2.5V to +7V, provide this circuit with the ability to test TTL, CMOS, ECL and GaAs devices. The high and low limits of the output swing are set through the program pins V_H and V_L, respectively. The transfer characteristic from the program pins to the output pin is unity gain with very low offset drift. The V_H and V_L inputs have been buffered to operate with low bias currents (1 μA typical) allowing direct coupling to the output of a DAC.

When the RC7315 is used on an I/O pin, it may be forced into the high impedance state through the INH+ and INH- differential inputs. In the high impedance state, excellent isolation is provided between the output of the disabled driver and the pin by virtue of low driver output capacitance (3.0 pF typical) and low output leakage (10 nA typical).

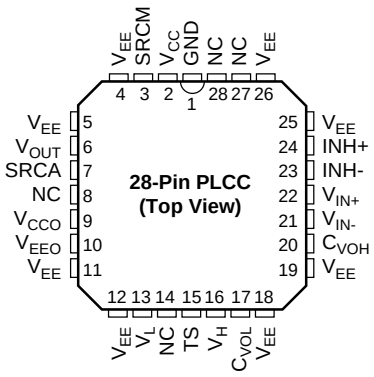
The RC7315 is provided with high speed differential ECL inputs for ease of interface with the differential ECL outputs of a timing generator. The inputs have a voltage range of -2V to +6V, so that if required, an input may be driven by TTL or CMOS devices provided that the other input is fed to the appropriate threshold value.

The RC7315 is implemented using Fairchild Semiconductor's high frequency complementary bipolar process.

Block Diagram



Pin Assignments



Pin Description

Name	Pin Number	Function
C_{VOL}, C_{VOH}	17	**Bypass capacitor for V_{OH} and V_{OL} respectively**. Pins C_{VOL} and C_{VOH} should be bypassed to the ground plane with a 1,000 pF chip capacitor placed as close to the pin as possible.
GND	1	**Chip ground**. Should be connected to the printed circuit board's ground plane at the pin.
INH+ INH-	23, 24	**Differential digital inputs**. When INH is true (i.e. INH+ > INH-) the driver is forced into the high impedance state. Although these inputs are normally driven by ECL signals, they have a wide enough common mode range that any one of the inputs may be driven by a TTL or CMOS signal provided that the other input is tied to the appropriate threshold voltage.
SRCA	7	**Slew rate control for both edges**. Slew rate of both rising and falling edges decreases as the control current is changed from 0 mA to -0.5 mA. SRC can be programmed with a current DAC or set to a fixed value using a resistor.
SRCM	3	Increases the speed of the falling edge to match the rising edge.
$\overline{TS}$	15	**Active low output notifies thermal shutdown has occurred**. In the event of a short circuit or other fault that causes the die temperature to become excessively large, the thermal shutdown will kick in at a die temperature between 115°C and 160°C. If the fault persists, the device will toggle back and forth between shutdown and normal operation at a frequency in the tens of Hertz. $\overline{TS}$ is an open collector output capable of driving two standard TTL loads. The $\overline{TS}$ pins of several drivers may be wire-ORed together and input to a latch to indicate an alarm condition.
V_{CC}	2	**Quiet positive supply**. The nominal value is 10V ±3%. For output high voltage levels (V_{OH}) greater than the nominal value of +7V, V_{CC} should be raised 3V above the maximum value of V_{OH}. Whenever V_{EE} is lowered to provide margin at the output low level, V_{CC} should also be lowered by the same amount. V_{CC} should be bypassed to ground with a 10,000 pF chip capacitor placed as close to the pins as possible.
V_{CCO}	9	**Positive supply for the RC7315 output stage**. This supply is brought out separately to minimize the supply noise generated when the output switches. V_{CCO} should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible and then immediately connected to V_{CC}.
V_{EE}	4, 5, 11, 12, 18, 19, 25, 26	**Quiet negative supply**. The nominal value is -5.2V ±5%. For output low voltage levels (V_{OL}) less than the nominal value of -2.2V, V_{EE} should be lowered 3V below the minimum value of V_{OL}. Whenever V_{CC} is raised to provide margin at the output high level, V_{EE} should also be raised by the same amount. V_{EE} should be bypassed to ground with a 10,000 pF chip capacitor placed as close to the pins as possible.

Pin Descriptions (continued)

Name	Pin Number	Function
V_{EEO}	10	**Negative supply for the RC7315 output stage**. This supply is brought out separately to minimize the supply noise generated when the output switches. V_{EEO} should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible and then immediately connected to V_{EE}.
V_H	16	Analog program input that sets the output high level (V_{OH}). The transfer characteristic from V_H to V_{OH} is nominally unity gain.
V_{IN+}, V_{IN-}	21, 22	**Differential digital inputs**. The output will toggle between the two levels dictated by V_H and V_L as the differential signal is switched. Although these inputs are normally driven by ECL signals, they have a wide enough common mode range that any one of the inputs may be driven by a TTL or CMOS signal provided that the other input is tied to the appropriate threshold voltage.
V_L	13	Analog program input that sets the output low level (V_{OL}). The transfer characteristic from $V_L$to V_{OL} is nominally unity gain.
V_O		**Driver output on RC7315**. The output impedance is 8Ω ±2Ω. The output is usually back terminated in the characteristic impedance of the transmission line it drives. For a 50Ω line, a 40Ω ±1% resistor should be placed externally as close to the output pin as possible to minimize reflections and ringing. The resistor should also be able to dissipate 0.8Ω to sustain the short circuit current of the output.
NC	8, 14, 27, 28	**No connection**.

Absolute Maximum Ratings[1]

Parameter	Min.	Max.	Units
Positive power supply, V_{CC}		13	V
Negative power supply, V_{EE}	-8.2		V
Difference between V_{CC} and V_{EE}		17	V
Input voltage at V_{IN+}, V_{IN-}, INH+, and INH-	V_{CC}-12	V_{EE}+12	V
Input Voltage at V_H, V_L	V_{CC}-13	V_{EE}+13	V
Differential input voltage, $\lvert V_{IN+} - V_{IN-} \rvert$, $\lvert V_{INH+} - V_{INH-} \rvert$		6	V
Difference between V_H & V_L ($\lvert V_H - V_L \rvert$)		11	V
Input voltage at SRCA	-3	+7	V
Slew rate control current	-2.0		mA
Driver Output Voltage	V_{CC}-13	V_{EE}+13	V
Output voltage at $\overline{TS}$		5	V
Duration of short-circuit to ground		Indefinite	
Operating temperature range	0	70	°C
Storage temperature range	-65	+125	°C
Lead temperature range (Soldering 10 seconds)		300	°C

Notes:

1. “Absolute maximum ratings” are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. If the device is subjected to the limits in the absolute maximum ratings for extended periods, its reliability may be impaired. The tables of Electrical Characteristics provide conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameters	Min.	Typ.	Max.	Units
T_C	Case operating temperature		25		°C
V_{CC}	Positive supply voltage	9.7	10.0	10.3	°C
V_{EE}	Negative supply voltage	-5.45	-5.2	-4.95	V
V_{CC}-V_{EE}	Difference between positive and negative supply		15.2	15.8	V
V_{OH}, V_{OL}	Range for output high level and output low level	-2.0		7.0	V
V_{OH}-V_{OL}	Output amplitude	0.1		10.0	V

DC Electrical Characteristics

V_{CC} = 10V ±3%, V_{EE} = -5.2V ±5%, T_A = 25°C (still air) and the load is a 50Ω transmission line with 2.0 ns one-way delay, unless otherwise specified. The transmission line is back-terminated in 50Ω (±5%) using an external resistor.

Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Units
Differential Inputs V_{IN+}, V_{IN-}, V_{INH+}, V_{INH-}						
V_{IN+}, V_{IN-}	Absolute Voltage @ Data Inputs		-2.0		+6.0	V
V_{INH+}, V_{INH-}	Absolute Voltage @ Inhibit Inputs INH+, INH-		-2.0		+6.0	V
V_{ID}	Differential Input Range	$\lvert V_{IN+} - V_{IN-} \rvert$	0.4	ECL	5.0	V
V_{DINH}	Differential Inhibit Input Range	$\lvert V_{INH+} - V_{INH} \rvert$	0.4	ECL	5.0	V
I_{IN+}, I_{IN-}	Input Bias Current @ Data Inputs	-2V ≤ V_{IN+}, V_{IN-} ≤ +6V		-100		µA
I_{INH+}, I_{INH-}	Input Bias Current @ Inhibit Inputs	-2V ≤ V_{INH+}, V_{INH-} ≤ +5V		-100		µA
Absolute Slew Rate Control Input SRCA						
V_{SRCA}	Compliance Voltage Range		-2.0		+2.0	V
I_{SRCA}	Control Current Range		-0.5		+0.5	V
Matching Slew Rate Control Input SRCM						
V_{SRCM}	Compliance Voltage Range		-2.0		+2.0	V
I_{SRCM}	Control Current Range		-0.5		+0.5	V
Voltage Program Inputs V_H, V_L						
V_H	V_H Range	V_{CC} = 10V; V_{EE} = -5.2V	-2.0		+7.0	V
		V_{CC} = 12V; V_{EE} = -3.2V	0		+9.0	V
		V_{CC} = 8V; V_{EE} = -7.2V	-4.0		+5.0	V
V_L	V_L Range	V_{CC} = 10V; V_{EE} = -5.2V	-2.5		+6.0	V
		V_{CC} = 12V; V_{EE} = -3.2V	-0.5		+8.0	V
		V_{CC} = 8V; V_{EE} = -7.2V	-4.5		+4.0	V
I_H	Bias Current @ V_H	-1V ≤ V_H ≤ +7V; V_L = -2.0V		-1		µA
I_L	Bias Current @ V_L	-2V ≤ V_L +5V; V_H = 6.0V		-1		µA
TCI_H	Temperature Drift in I_H	V_H = 7.0V; 25°C ≤ T_C ≤ 70°C output not switching			0.1	µA/°C
TCI_L	Temperature Drift in I_L	V_L= -2.0V; 25°C ≤ T_C ≤ 70°C output not switching			0.1	µA/°C
$V_{H,L}BW$	-3 dB bandwidth from V_H or V_L to the output	-1V ≤ V_H ≤ +7V; -2V ≤ V_L ≤ +6V; V_H-V_L= 2.0V		50		kHz

DC Electrical Characteristics (continued)

Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Units
Signal Output V_O, V_{OTERM}						
V_O	Output Voltage Range	V_{CC} = 10V; V_{EE} = -5.2V	-2.5		+7.0	V
		V_{CC} = 12V; V_{EE} = -3.2V	-0.5		+9.0	V
		V_{CC} = 8V; V_{EE} = -7.2V	-4.5		+5.0	V
V_A	Amplitude	$\lvert V_{OH} - V_{OL} \rvert$	0.3		9.5	V
δV_{OH}	Offset to Output High Level	V_H = 0, no load; V_L = -2V		±30		mV
		$\delta V_{OH} = \lvert V_H - V_{OH} \rvert$				
δV_{OL}	Offset to Output Low Level	V_H = 0, no load; V_H = +7V		±30		mV
		$\delta V_{OL} = \lvert V_L - V_{OL} \rvert$				
VTC	Output Voltage Drift	-1V ≤ V_{OH} ≤ +7V;		0.1		mV/°C
		-2V ≤ V_{OL} ≤ +6V;		0.1		
ε_G	Gain Error	-1V ≤ V_{OH} ≤ +7V;		1	2	$\%V_{SET}$
		-2V ≤ V_{OL} ≤ +6V		1		
ε_L	Linearity Error	-2V ≤ V_{OUTPUT} ≤ +7		0.7		$\%V_{SET}$
Z_{OUT}	Output Impedance I_{OUT} 50 mA	V_O		8		Ω
I_{ZL}	Output Leakage Current in Inhibit Mode	-2.0V ≤ V_O ≤ +7V		0.5	2	µA
I_{DC}	DC Current Drive		50			mA
I_{AC}	AC Current Drive		70	100		mA
Thermal Shutdown Output (TS)						
I_{CL}	Short Circuit Current Limit				145	mA
VTS	TS Flag Output Level	I_{OL} = 4 mA			0.5	V
T_{TS}	Shutdown Die Temperature			145		°C
Other						
$V_{S\ MAX}$	Maximum Rail to Rail Supply Voltage	V_{CC} - V_{EE}			16	V
V_{CC}	Positive Supply		+8.0	+10.0	+12.0	V
V_{EE}	Negative Supply		-7.2	-5.2	-3.2	V
I_{CC}	Positive Supply Current			85		mA
IEE	Negative Supply Current			90		mA
$PSRV_O$	Output Level Power Supply	V_{CC}; ΔV_{CC} = ±2.5%	40			dB
	Rejection Ratio	V_{EE}; ΔV_{EE} = ±2.5%	40			dB
$PSRV_{SL}$	Output Slew Rate Power Supply	V_H = 5V				
	Rejection Ratio @ V_{CC}	and ΔV_{CC} = ±200 mV		4		
	@ V_{EE}	V_L = 0V ΔV_{EE} = ±200 mV		4		%
T_A	Operating Temperature Range	Still Air	0	25	40	°C
		Air Flow > 300 l_{fpm}	0	25	70	°C

AC Electrical Characteristics

V_{CC} = 10V ±3%, V_{EE} = -5.2V ±5%, T_A = 25°C (still air) and the load is a 50Ω transmission line with 2.0 ns one-way delay, unless otherwise specified. The transmission line is back-terminated in 50Ω (±5%) using an external resistor. The measurement probe is a high impedance FET probe with capacitance no greater than 3 pF and resistance no smaller than 10 kΩ.

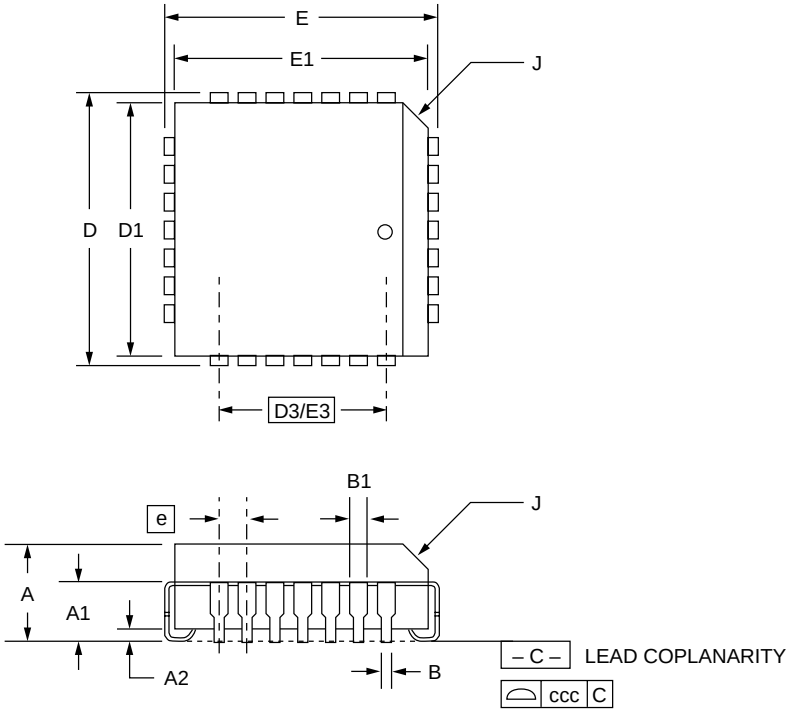
Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Units
SLR	Slew Rate (Slew rate not adjusted)	V_H - V_L = 5V; Measured between 20% and 80% points.				
		With probe only as load	1.3	1.8		V/ns
		With probe and transmission line	1.2	1.7		V/ns
t_R,	Rise Time, and	Load is Probe Only;				
t_F	Fall Time	V_A = 1V (20% to 80%)		0.6		ns
	(Slew rate not adjusted)	V_A = 3V (10% to 90%)		1.6		ns
		V_A = 5V (10% to 90%)		2.5		ns
f	Toggle Rate	Amplitude = 0.8 Vp-p	250			MHz
		Amplitude = 5.0 Vp-p	125			MHz
t_{PLH}	Low to High Propagation Delay	f = 10 MHz; V_{OH} = +0.4V;				
		V_{OL} = -0.4V		1.6		ns
t_{PHL}	High to Low Propagation Delay	f = 10 MHz; V_{OH} = +0.4V;				
		V_{OL} = -0.4V		1.4		ns
Δt_P	Propagation Delay Match	$\lvert t_{PLH} - t_{PHL} \rvert$		200		ps
t_PTC	Propagation Delay Temperature Coefficient			2		ps/°C
tPW_{min}	Minimum Pulse Width	V_H - V_L - 2.0V; pulsewidth at which amplitude drops by 50 mV, measured between 50% points.		2.0		ns
Δt_PPW	Propagation Delay Variation with Pulse Width	2 ns < PW < 98 ns; f = 10 MHz; V_{OH} = +0.4V; V_{OL} = -0.4V		±75		ps
t_{PS}	Preshoot	0.5V < V_A < 5.0V			15mV + 3% of V_A	
t_{OS}	Overshoot	0.5V < V_A < 5.0V			50mV + 4% of V_A	
t_S	Output Settling Time	V_A < 5V;				
		To within 3% of V_A		8		ns
		To within 1% of V_A		10		ns
t_{PHZ}	Propagation Delay from Logic High to Inhibit Mode	V_{OH} = 1V; V_{OL} = -1V Load = 100Ω // 15pF		2.9		ns
t_{PLZ}	Propagation Delay from Logic Low to Inhibit Mode	Propagation delay is measured to the point at which voltage has changed by 200 mV.		2.9		ns
t_{PZH}	Propagation Delay from Inhibit Mode from Logic High			2.9		ns
t_{PZL}	Propagation Delay from Inhibit Mode to Logic Low			2.9		ns
C_Z	Output capacitance in Inhibit Mode			3		pF

Mechanical Dimensions — 28-pin PLCC

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.180	4.19	4.57	
A1	.090	.120	2.29	3.05	
A2	.020	—	.51	—	
B	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D/E	.485	.495	12.32	12.57	
D1/E1	.450	.456	11.43	11.58	3
D3/E3	.300 BSC		7.62 BSC		
e	.050 BSC		1.27 BSC		
J	.042	.048	1.07	1.22	2
ND/NE	7		7		
N	28		28		
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982
2. Corner and edge chamfer (J) = 45°
3. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is .101" (.25mm)



Ordering Information

Part Number	Package	Operating Temperature Range
RC7315QF	28-pin PLCC	0°C to +70°C

RC7316

Three-State ATE Pin Electronics Driver

Features

- High output slew rate (3.2 V/ns) typical driving coax
- Wide output voltage range (-2.0V to +7V), and up to 9 Vp-p swings
- Three-state/high impedance output
- High repetition rate (550 MHz for ECL swings)
- Low output offset (40 mV typical) and output offset drift (0.1 mV/°C typical
- Low leakage (10 nA typical) and low output capacitance (3.0 pF typical) in high impedance inhibit mode
- 100 mA typical dynamic current drive capability
- High speed differential inputs with wide common mode range for ease of interface to ECL as well as TTL and CMOS levels
- Output short circuit protection (Safe Operating Area protection with current limiting and thermal shutdown)
- Available in 16 Lead Hybrid Flatpack
- RC7316TEL is pin-for-pin compatible with AD1321, AD1322, and AD1324

Applications

- ATE pin electronics driver
- Precision waveform generator
- Level translator
- Differential line receiver
- General purpose driver
- Laser driver
- CRT preamplifier

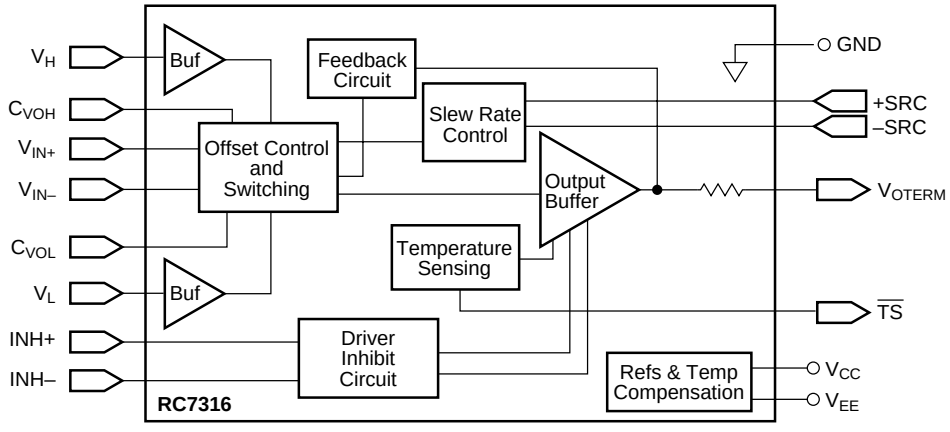
Description

The RC7316 Pin Electronics Driver is designed for use in ultra high speed ATE systems which require pin drivers with three state capability and high slew rates. The RC7316 has the ability to drive a 50Ω transmission line of up to 2 feet in length with a slew rate of 3.2 V/ns and repetition rate of over 550 MHz for ECL output levels. These features, combined with a maximum output swing of 9.5 Vp-p over the range of -3.0V to +7V, provide this circuit with the ability to test TTL, CMOS, ECL and GaAs devices. The high and low limits of the output swing are set through the program pins V_H and V_L, respectively. The transfer characteristic from the program pins to the output pin is unity gain with very low offset drift. The V_H and V_L inputs have been buffered to operate with low bias currents (1 μA typical) allowing direct coupling to the output of a DAC.

When the RC7316 is used on an I/O pin, it may be forced into the high impedance state through the INH+ and INH- differential inputs. In the high impedance state, excellent isolation is provided between the output of the disabled driver and the pin by virtue of low driver output capacitance (3.0 pF typical) and low output leakage (10 nA typical).

The RC7316 is provided with high speed differential ECL inputs for ease of interface with the differential ECL outputs of a timing generator. The inputs have a voltage range of -2V to +6V, so that if required, an input may be driven by TTL or CMOS devices provided that the other input is fed to the appropriate threshold value.

Block Diagram



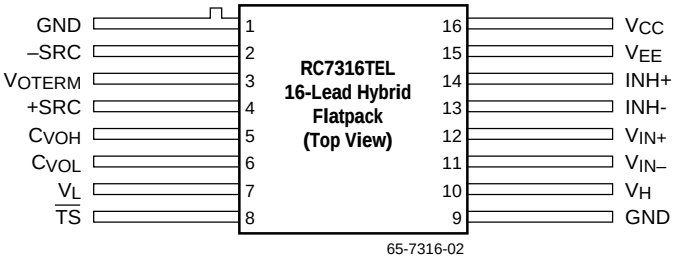
65-7316-01

Description (continued)

The pin driver is available in 50Ω series terminated RC7316 (TEL) configurations. The RC7316TEL is pin-for-pin compatible with Analog Devices' AD1321, AD1322 and AD1324 drivers.

The RC7316 is implemented using Fairchild Semiconductor's high frequency BiCMOS process.

Pin Assignments



65-7316-02

Pin Descriptions

Pin Name	Pin Number	Pin Function Description
C_{VOL}, C_{VOH}	6, 5	Bypass capacitor for V_{OH} and V_{OL} respectively. Pins C_{VOL} and C_{VOH} should be bypassed to the ground plane with a 1,000 pF chip capacitor placed as close to the pin as possible.
GND	1, 9	Chip ground. Should be connected to the printed circuit board's ground plane at the pin.
INH+, INH-	13, 14	Differential digital inputs. When INH is true (i.e. INH+ > INH-) the driver is forced into the high impedance state. Although these inputs are normally driven by ECL signals, they have a wide enough common mode range that any one of the inputs may be driven by a TTL or CMOS signal provided that the other input is tied to the appropriate threshold voltage.
+SRC	4	Slew rate control for the positive edge. Slew rate of the positive edge changes as the control voltage is changed from -2.0V to +2.0V. +SRC can also be programmed with a current DAC or set to a fixed value using a resistor. Optionally, pin 4 can be NC. (No Connection)
–SRC	2	Slew Rate Control for the negative edge. Slew rate of the negative edge changes as the control voltage is changed from -2.0V to +2.0V. -SRC can also be programmed with a current DAC or set to a fixed value using a resistor. Optionally, pin 2 can be NC. (No Connection)
$\overline{TS}$	8	Active low output notifies thermal shutdown has occurred. In the event of a short circuit or other fault that causes the die temperature to become excessively large, the thermal shutdown will kick in at a die temperature between 115°C and 160°C. If the fault persists, the device will toggle back and forth between shutdown and normal operation at a frequency in the tens of Hertz. TS is an open collector output capable of driving two standard TTL loads. The TS pins of several drivers may be wire-ORed together and input to a latch to indicate an alarm condition. Optionally, pin 8 can be NC.
V_{CC}	16	Quiet positive supply. The nominal value is 10V ±3%. For output high voltage levels (V_{OH}) greater than the nominal value of +7V, V_{CC} should be raised 3V above the maximum value of V_{OH}. Whenever V_{EE} is lowered to provide margin at the output low level, V_{CC} should also be lowered by the same amount. V_{CC} should be bypassed to ground with a 10,000 pF chip capacitor placed as close to the pins as possible.

Pin Descriptions (continued)

Pin Name	Pin Number	Pin Function Description
V_{CCO}		Positive supply for the RC7316 output stage. This supply is brought out separately to minimize the supply noise generated when the output switches. V_{CCO} should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible and then immediately connected to V_{CC}.
V_{EE}	15	Quiet negative supply. The nominal value is -5.2V ±5%. For output low voltage levels (V_{OL}) less than the nominal value of -2.5V, V_{EE} should be lowered 3V below the minimum value of V_{OL}. Whenever V_{CC} is raised to provide margin at the output high level, V_{EE} should also be raised by the same amount. V_{EE} should be bypassed to ground with a 10,000 pF chip capacitor placed as close to the pins as possible.
V_{EEO}		Negative supply for the RC7316 output stage. This supply is brought out separately to minimize the supply noise generated when the output switches. V_{EEO} should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible and then immediately connected to V_{EE}.
V_H	10	Analog program input that sets the output high level (V_{OH}) The transfer characteristic from V_H to V_{OH} is nominally unity gain.
V_{IN+}, V_{IN-}	11,12	Differential digital inputs. The output will toggle between the two levels dictated by V_H and V_L as the differential signal is switched. Although these inputs are normally driven by ECL signals, they have a wide enough common mode range that any one of the inputs may be driven by a TTL or CMOS signal provided that the other input is tied to the appropriate threshold voltage.
V_L	7	Analog program input that sets the output low level (V_{OL}). The transfer characteristic from $V_L$to V_{OL} is nominally unity gain.
V_O		Driver output on RC7316. The output impedance is 10Ω ±2Ω. The output is usually back terminated in the characteristic impedance of the transmission line it drives. For a 50Ω line, a 40Ω ±1% resistor should be placed externally as close to the output pin as possible to minimize reflections and ringing. The resistor should also be able to dissipate 0.8Ω to sustain the short circuit current of the output.

Absolute Maximum Ratings[1]

Parameter	Min.	Max.	Units
Positive power supply, V_{CC}		13	V
Negative power supply, V_{EE}	-8.2		V
Difference between V_{CC} and V_{EE}		16	V
Input voltage at V_{IN+}, V_{IN-}, INH+, INH-	V_{CC}-12	V_{EE}+12	V
Input Voltage at V_H, V_L	V_{CC}-13	V_{EE}+13	V
Differential input voltage, $\lvert V_{IN+} - V_{IN-} \rvert$, $\lvert V_{INH+} - V_{INH-} \rvert$		6	V
Difference between V_H & V_L ($\lvert V_H - V_L \rvert$)		11	V
Input voltage at +SRC, -SRC	-3	+7	V
Slew rate control current	-2.0		mA
Driver Output Voltage	V_{CC}-13	V_{EE}+13	V
Output voltage at TS		5	V
Duration of short-circuit to ground		Indefinite	
Operating temperature range	0	70	°C
Storage temperature range	-65	+125	°C
Lead temperature range (Soldering 10 seconds)		300	°C

Notes:

1. “Absolute maximum ratings” are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. If the device is subjected to the limits in the absolute maximum ratings for extended periods, its reliability may be impaired. The tables of Electrical Characteristics provide conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameters	Min.	Typ.	Max.	Units
T_C	Case operating temperature	0	25	+70	°C
V_{CC}	Positive supply voltage	9.7	10.0	10.3	°C
V_{EE}	Negative supply voltage	-5.45	-5.2	-4.95	V
V_{CC}-V_{EE}	Difference between positive and negative supply		15.2	15.8	V
V_{OH}, V_{OL}	Range for output high level and output low level	-3.0		7.0	V
V_{OH}-V_{OL}	Output amplitude	0.1		9.5	V
R_T	Output back-termination resistor		41		

DC Electrical Characteristics

V_{CC} = 10V ±3%, V_{EE} = -5.2V ±5%, T_A = 25°C (flow ≥ 300 Lfm) and the load is a 50Ω transmission line with 2.0 ns one-way delay, unless otherwise specified. The transmission line is back-terminated in 50Ω (±5%) using an external resistor (RC7316).

Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Units
Diffential Inputs V_{IN+}, V_{IN-}, V_{INH+}, V_{INH-}						
V_{IN+}, V_{IN-}	Absolute Voltage @ Data Inputs		-2.0		+6.0	V
V_{INH+}	Absolute Voltage @ Inhibit					
V_{INH-}	Inputs INH+, INH-		-2.0		+5.0	V
V_{ID}	Differential Input Range	$\lvert V_{IN+} - V_{IN-} \rvert$	0.4	ECL	5.0	V
V_{DINH}	Differential Inhibit Input Range	$\lvert V_{INH+} - V_{INH} \rvert$	0.4	ECL	5.0	V
I_{IN+}, I_{IN-}	Input Bias Current @ Data Inputs	-2V ≤ V_{IN+}, V_{IN-} ≤ +6V	-100	-35		µA
I_{INH+}, I_{INH-}	Input Bias Current @ Inhibit Inputs	-2V ≤ V_{INH+}, V_{INH-} ≤ +5V	-150	-50		µA
Voltage Program Inputs V_H, V_L						
V_H	V_H Range	V_{CC} = 10V; V_{EE} = -5.2V	-2.0		+7.0	V
		V_{CC} = 12V; V_{EE} = -3.2V	0		+9.0	V
		V_{CC} = 8V; V_{EE} = -7.2V	-4.0		+5.0	V
V_L	V_L Range	V_{CC} = 10V; V_{EE} = -5.2V	-2.0		+6.0	V
		V_{CC} = 12V; V_{EE} = -3.2V	0		+8.0	V
		V_{CC} = 8V; V_{EE} = -7.2V	-4.0		+4.0	V
I_H	Bias Current @ V_H	-1V ≤ V_H ≤ +7V; V_L = -3.0V		1.0	5.0	µA
I_L	Bias Current @ V_L	-3V ≤ V_L ≤ +5V; V_H = 6.0V	-5.0	-1.0		µA
TCI_H	Temperature Drift in I_H	V_H = 7.0V; 25°C ≤ T_C ≤ 70°C output not switching			0.1	µA/°C
TCI_L	Temperature Drift in I_L	V_L= -3.0V; 25°C ≤ T_C ≤ 70°C output not switching			0.1	µA/°C
ΔIBDC	Variation in I_H, $I_L$with power supply and DC voltage at V_H or V_L	-1V ≤ V_H ≤ +7V -2V ≤ V_L ≤ + 6V	-1		1	µA
$V_{H,L}$BW	-3 dB bandwidth from V_H or V_L to the output	-1V ≤ V_H ≤ +7V; -2V ≤ V_L ≤ +6V; V_H-V_L= 2.0V			50	kHz
Signal Output V_O, V_{OTERM}						
V_O	Output Voltage Range	V_{CC} = 10V; V_{EE} = -5.2V	-2.0		+7.0	V
		V_{CC} = 12V; V_{EE} = -3.2V	0		+9.0	V
		V_{CC} = 8V; V_{EE} = -7.2V	-4.0		+5.0	V
V_A	Amplitude	$\lvert V_{OH} - V_{OL} \rvert$	0.1		9.5	V
δV_{OH}	Offset to Output High Level	-1V ≤ V_H ≤ +6V; V_L = -2V	-100	-40	100	mV
		$\delta V_{OH} = \lvert V_H - V_{OH} \rvert$				
δV_{OL}	Offset to Output Low Level	-2V ≤ V_L ≤ +6V; V_H = +7V	-100	-40	100	mV
		$\delta V_{OL} = \lvert V_L - V_{OL} \rvert$				
VTC	Output Voltage Drift	-1V ≤ V_{OH} ≤ +7V		0.1		mV/°C
ε_G	Gain Error	-2V ≤ V_{OL} ≤ +7V	-1.0	±0.5	+1.0	%V_{SET}
ε_L	Linearity Error	0V ≤ V_{OUTPUT} ≤ +5V	-0.5	±0.2	+0.5	%V_{SET}
		-2V≤ V_{OUTPUT} ≤ +7V	-1.0	±0.6	+1.0	%V_{SET}
Z_{OUT}	Output Impedance			50		

DC Electrical Characteristics (continued)

Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Units
I_{ZL}	Output Leakage Current in Inhibit Mode	$-2.0V \le V_O \le +6.5V$	-200	±10	+200	nA
I_{DC}	DC Current Drive		50			mA
I_{AC}	AC Current Drive		70	100		mA
Thermal Shutdown Output (TS) (Open Collector Output)						
I_{CL}	DC Current Limit		70	110	130	mA
V_{OL}	Output Low Level	I_{OL} = 4 mA			0.5	V
T_{TS}	Shutdown Die Temperature		115	135	160	°C
Other						
V_S	Rail to Rail Supply Voltage	$V_{CC} - V_{EE}$			17	V
V_{CC}	Positive Supply		+8.0	+10.0	+12.0	V
V_{EE}	Negative Supply		-7.2	-5.2	-3.2	V
I_{CC}	Positive Supply Current			85		mA
I_{EE}	Negative Supply Current			95		mA
$PSRV_O$	Output Level Power Supply	V_{CC}; ΔV_{CC} = ±2.5%		40		dB
	Rejection Ratio	V_{EE}; ΔV_{EE} = ±2.5%		40		dB
$PSRV_{SL}$	Output Slew Rate Power Supply	V_H = 5V				
	Rejection Ratio @ V_{CC}	and ΔV_{CC} = ±200 mV			4	
	@ V_{EE}	V_L = 0V ΔV_{EE} = ±200 mV			4	%

AC Electrical Characteristics

V_{CC} = 10V ±3%, V_{EE} = -5.2V ±5%, T_A = 25°C (still air) and the load is a 50Ω transmission line with 2.0 ns one-way delay, unless otherwise specified. The transmission line is back-terminated in 50Ω (±5%) using both internal and external termination resistance. The measurement probe is a high impedance FET probe with capacitance no greater than 3 pF and resistance no smaller than 10 kΩ.

Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Units
SLR	Slew Rate	$V_H - V_L$ = 5V; Measured between 20% and 80% points. With probe only as load	3.0	3.5		V/ns
		With probe and transmission line	2.7	3.2		V/ns
+SRC	Positive SLR Control + SRC					
	Control Voltage Range	V_H = +5V, V_L = 0V	-2.0		+2.0	V
	Slew Rate Change		0.5		+3.5	V/ns
–SRC	Negative SLR Control –SRC					
	Control Voltage Range	V_H = +5V, V_L= 0V	-2.0		+2.0	V
	Slew Rate Change		0.5		+3.5	V/ns
t_R,	Rise Time, and	C_L = 5.0 pF				
t_F	Fall Time	V_A = 0.8V (20% to 80%)		0.5	0.8	ns
		V_A = 3V (10% to 90%)		1.0	1.4	ns
		V_A = 5V (10% to 90%)		1.4	1.8	ns

AC Electrical Characteristics (continued)

Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Units
f	Toggle Rate	Amplitude = 0.8 Vp-p	500	550		MHz
	(Probe only)	Amplitude = 3.0 Vp-p	275	300		MHz
		Amplitude = 5.0 Vp-p	200	220		MHz
t_{PHL}	High to Low Propagation Delay	f = 10 MHz; V_{OH} = +0.4V;				
		V_{OL} = -0.4V		1.7	2.0	ns
Δt_P	Propagation Delay Match	$\lvert t_{PLH} - t_{PHL} \rvert$		30	100	ps
t_PTC	Propagation Delay Temperature Coefficient			2		ps/°C
tPW_{min}	Minimum Pulse Width	V_H - V_L - 2.0V; pulsewidth at which amplitude drops by 50 mV, measured between 50% points. C_L = 5.0 pF		1.1		ns
Δt_PPW	Propagation Delay Variation with Pulse Width	2 ns < PW < 98 ns; f = 10 MHz; V_{OH} = +0.4V; V_{OL} = -0.4V		40	150	ps
t_{PS}	Preshoot	0.5V < V_A < 5.0V		15mV + 3% of V_A		ns
t_{OS}	Overshoot	0.5V < V_A < 5.0V		50mV + 4% of V_A		ns
t_S	Output Settling Time	V_A = 5V;				
		To within 3% of V_A		5.0		ns
		To within 1% of V_A		12.0		ns
t_{PHZ}	Propagation Delay from Logic High to Inhibit Mode	V_{OH} = 1V; V_{OL} = -1V Load = 100Ω to 2.5V; Propagation delay is measured to the point at which voltage has changed by 200 mV.		1.5	2.0	ns
t_{PLZ}	Propagation Delay from Logic Low to Inhibit Mode			2.0	2.5	ns
t_{PZH}	Propagation Delay from Inhibit Mode from Logic High			2.2	2.5	ns
t_{PZL}	Propagation Delay from Inhibit Mode to Logic Low			2.2	2.5	ns
C_Z	Output Capacitance in Inhibit Mode			3.0		pf

Notes:

Notes:

Notes:

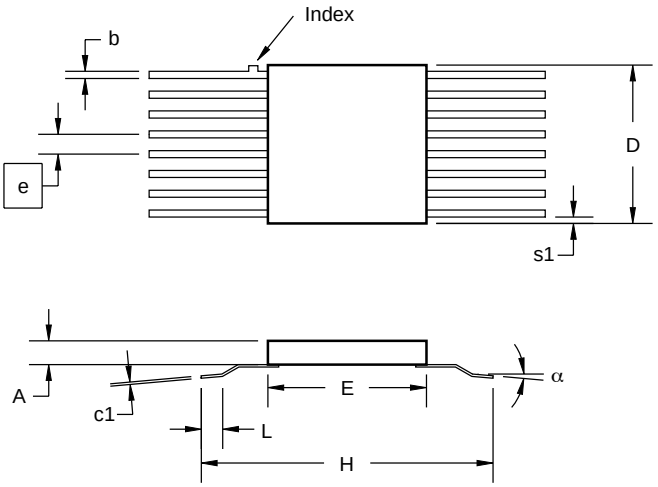
Mechanical Dimensions

16-Lead Hybrid Flatpack

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.072	.088	1.83	2.24	
b	.013	.017	0.33	0.43	
c1	.007	.010	0.18	.15	
D/E	.442	.458	11.23	11.63	
e	.050 BSC		1.27 BSC		
H	.675	.685	17.15	17.40	
L	.050	.065	1.40	1.65	
s1	.005	-	.13	-	
α	0°	5°	0°	5°	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Gold plate 80 μ" min. nickel over 80 μ" min. nickel.
3. Leads 1 and 9 connect to ground, seal ring, and heat sink pad.



Ordering Information

Part Number	Package	Operating Temperature Range
RC7316TEL	EL	0°C to +70°C

Notes:
TEL = 16 Lead Hybrid Flatpack, 50Ω termination (AD1322 pinout)

RC7321

Three-State ATE Pin Electronics Driver

Features

- High output slew rate (1.3 V/ns typical)
- Wide output voltage range (-2.2V to +7V), and up to 9.2 Vp-p swings
- Three-state/high impedance output
- High repetition rate (250 MHz for ECL swings)
- Low output offset (40 mV typical) and output offset drift (0.1 mV/°C typical).
- Low leakage (10 nA typical) and low output capacitance (3 pF typical) in high impedance inhibit mode
- High speed differential inputs with wide common mode range for ease of interface to ECL as well as TTL and CMOS levels
- Output short circuit protection (Safe Operating Area protection with current limiting and thermal shutdown)
- 100 mA typical dynamic current drive capability
- Absolute slew rate control
- Available in 28-pin PLCC

Applications

- ATE pin electronics driver
- Precision waveform generator
- Level translator
- PCB & Burn-in ATE Driver
- General purpose driver for PCB & burn-in test systems
- Laser driver
- CRT preamplifier

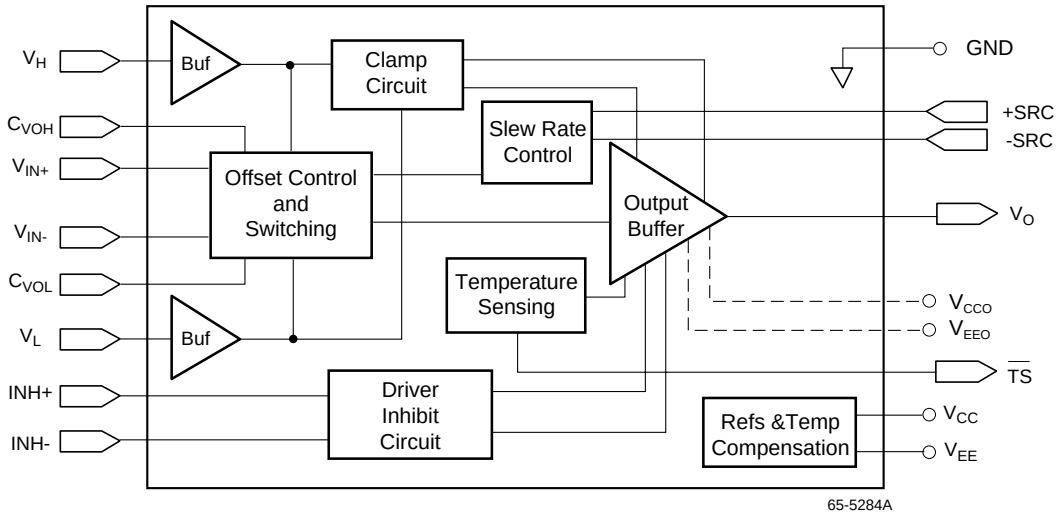
Description

The RC7321 is a low cost Pin Electronics Driver designed for use in all high speed ATE systems which require pin drivers with three state capability and high slew rates. The RC7321 has the ability to drive a 50Ω transmission line of up to 2 feet in length with a slew rate of 1.2 V/ns and repetition rate of over 250 MHz for ECL output levels. These features, combined with a maximum output swing of 9.5 Vp-p over the range of -2.5V to +7V, provide this circuit with the ability to test TTL, CMOS, ECL and GaAs devices. The high and low limits of the output swing are set through the program pins V_H and V_L, respectively. The transfer characteristic from the program pins to the output pin is unity gain with very low offset drift. The V_H and V_L inputs have been buffered to operate with low bias currents (1 μA typical) allowing direct coupling to the output of a DAC.

When the RC7321 is used on an I/O pin, it may be forced into the high impedance state through the INH+ and INH- differential inputs. In the high impedance state, excellent isolation is provided between the output of the disabled driver and the pin by virtue of low driver output capacitance (3.0 pF typical) and low output leakage (10 nA typical).

The RC7321 is provided with high speed differential ECL inputs for ease of interface with the differential ECL outputs of a timing generator. The inputs have a voltage range of -2V to +6V, so that if required, an input may be driven by TTL or CMOS devices provided that the other input is tied to the

Block Diagram

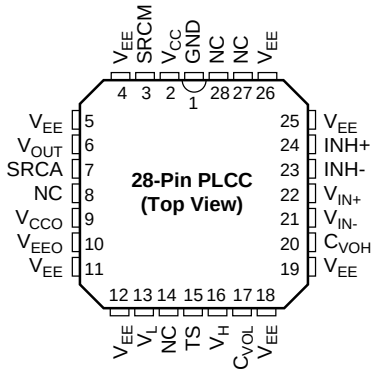


Description (continued)

appropriate threshold value. The pin driver is available in unterminated configuration.

The RC7321 is implemented using Fairchild Semiconductor's high frequency complementary bipolar process.

Pin Assignments



Pin Description

Name	Pin Number	Function
C_{VOL}, C_{VOH}	17	Bypass capacitor for V_{OH} and V_{OL} respectively. Pins C_{VOL} and C_{VOH} should be bypassed to the ground plane with a 1,000 pF chip capacitor placed as close to the pin as possible.
GND	1	Chip ground. Should be connected to the printed circuit board's ground plane at the pin.
INH+ INH-	23, 24	Differential digital inputs. When INH is true (i.e. INH+ > INH-) the driver is forced into the high impedance state. Although these inputs are normally driven by ECL signals, they have a wide enough common mode range that any one of the inputs may be driven by a TTL or CMOS signal provided that the other input is tied to the appropriate threshold voltage.
V_{CC}	2	Quiet positive supply. The nominal value is 10V ±3%. For output high voltage levels (V_{OH}) greater than the nominal value of +7V, V_{CC} should be raised 3V above the maximum value of V_{OH}. Whenever V_{EE} is lowered to provide margin at the output low level, V_{CC} should also be lowered by the same amount. V_{CC} should be bypassed to ground with a 10,000 pF chip capacitor placed as close to the pins as possible.
V_{CCO}	9	Positive supply for the RC7321 output stage. This supply is brought out separately to minimize the supply noise generated when the output switches. V_{CCO} should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible and then immediately connected to V_{CC}.
V_{EE}	4, 5, 11, 12, 18, 19, 25, 26	Quiet negative supply. The nominal value is -5.2V ±5%. For output low voltage levels (V_{OL}) less than the nominal value of -2.2V, V_{EE} should be lowered 3V below the minimum value of V_{OL}. Whenever V_{CC} is raised to provide margin at the output high level, V_{EE} should also be raised by the same amount. V_{EE} should be bypassed to ground with a 10,000 pF chip capacitor placed as close to the pins as possible.
V_{EEO}	10	Negative supply for the RC7321 output stage. This supply is brought out separately to minimize the supply noise generated when the output switches. V_{EEO} should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible and then immediately connected to V_{EE}.

Pin Description (continued)

Name	Pin Number	Function
V_H	16	Analog program input that sets the output high level (V_{OH}). The transfer characteristic from V_H to V_{OH} is nominally unity gain.
V_{IN+}, V_{IN-}	21, 22	Differential digital inputs. The output will toggle between the two levels dictated by V_H and V_L as the differential signal is switched. Although these inputs are normally driven by ECL signals, they have a wide enough common mode range that any one of the inputs may be driven by a TTL or CMOS signal provided that the other input is tied to the appropriate threshold voltage.
V_L	13	Analog program input that sets the output low level (V_{OL}). The transfer characteristic from $V_L$to V_{OL} is nominally unity gain.
V_O		Driver output on RC7321. The output impedance is 8W ±2Ω. The output is usually back terminated in the characteristic impedance of the transmission line it drives. For a 50Ω line, a 40W±1% resistor should be placed externally as close to the output pin as possible to minimize reflections and ringing. The resistor should also be able to dissipate 0.8Ω to sustain the short circuit current of the output.
SRCA	7	Slew rate control for both edges. Slew rate of both rising and falling edges decreases as the control current is changed from 0 mA to -0.5 mA. SRC can be programmed with a current DAC or set to a fixed value using a resistor. Increases the speed of the falling edge to match the rising edge.
SRCM	3	
$\overline{TS}$	15	Active low output notifies thermal shutdown has occurred. In the event of a short circuit or other fault that causes the die temperature to become excessively large, the thermal shutdown will kick in at a die temperature between 125°C and 150°C. If the fault persists, the device will toggle back and forth between shutdown and normal operation at a frequency in the tens of Hertz. $\overline{TS}$ is an open collector output capable of driving two standard TTL loads. The $\overline{TS}$ pins of several drivers may be wire-ORed together and input to a latch to indicate an alarm condition.
NC	8, 14, 27, 28	No connection.

Absolute Maximum Ratings[1]

Parameter	Min.	Max.	Units
Positive power supply, V_{CC}		13	V
Negative power supply, V_{EE}	-8.2		V
Difference between V_{CC} and V_{EE}		16	V
Input voltage at V_{IN+}, V_{IN-}, INH+, INH-	V_{CC}-12	V_{EE}+12	V
Input Voltage at V_H, V_L	V_{CC}-13	V_{EE}+13	V
Differential input voltage, | V_{IN+} – V_{IN-} I, | V_{INH+} – V_{INH-} I		6	V
Difference between V_H & V_L (IV_H – V_LI)		11	V
Input voltage at SRCA	-3	+7	V
Slew rate control current	-2.0		mA
Driver Output Voltage	V_{CC}-13	V_{EE}+13	V
Output voltage at $\overline{TS}$		5	V
Duration of short-circuit to ground		Indefinite	
Operating temperature range	0	70	°C

Absolute Maximum Ratings[1] (continued)

Parameter	Min.	Max.	Units
Storage temperature range	-65	+125	°C
Lead temperature range (Soldering 10 seconds)		300	°C

Notes:

1. "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. If the device is subjected to the limits in the absolute maximum ratings for extended periods, its reliability may be impaired. The tables of Electrical Characteristics provide conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameters	Min.	Typ.	Max.	Units
T_C	Case operating temperature		25		°C
V_{CC}	Positive supply voltage	9.7	10.0	10.3	°C
V_{EE}	Negative supply voltage	-5.45	-5.2	-4.95	V
V_{CC}-V_{EE}	Difference between positive and negative supply		15.2	15.8	V
V_{OH}, V_{OL}	Range for output high level and output low level	-2.0		7.0	V
V_{OH}-V_{OL}	Output amplitude	0.1		9.5	V

DC Electrical Characteristics

V_{CC} = 10V ±3%, V_{EE} = -5.2V ±5%, T_A = 25°C (still air) and the load is a 50Ω transmission line with 2.0 ns one-way delay, unless otherwise specified. The transmission line is back-terminated in 50Ω (±5%) using an external resistor.

Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Units
Differential Inputs V_{IN+}, V_{IN-}, V_{INH+},V_{INH-}						
V_{IN+}, V_{IN-}	Absolute Voltage @ Data Inputs		-2.0		+6.0	V
V_{INH+}, V_{INH-}	Absolute Voltage @ Inhibit Inputs INH+, INH-		-2.0		+6.0	V
V_{ID}	Differential Input Range	$\lvert V_{IN+} - V_{IN-} \rvert$	0.4	ECL	5.0	V
V_{DINH}	Differential Inhibit Input Range	$\lvert V_{INH+} - V_{INH} \rvert$	0.4	ECL	5.0	V
I_{IN+}, I_{IN-}	Input Bias Current @ Data Inputs	-2V ≤ V_{IN+}, V_{IN-} ≤ +6V		100	200	µA
I_{INH+}, I_{INH-}	Input Bias Current @ Inhibit Inputs	-2V ≤ V_{INH+}, V_{INH-} ≤ +5V		100	200	µA
Absolute Slew Rate Control Input SRCA						
V_{SRCA}	Compliance Voltage Range		-2.0		+2.0	V
I_{SRCA}	Control Current Range		-0.5		+0.5	V
Matching Slew Rate Control Input SRCM						
V_{SRCM}	Compliance Voltage Range		-2.0		+2.0	V
I_{SRCM}	Control Current Range		-0.5		+0.5	V
Voltage Program Inputs V_H, V_L						
V_H	V_H Range	V_{CC} = 10V; V_{EE} = -5.2V	-2.0		+7.0	V
		V_{CC} = 12V; V_{EE} = -3.2V	0		+9.0	V
		V_{CC} = 8V; V_{EE} = -7.2V	-4.0		+5.0	V
V_L	V_L Range	V_{CC} = 10V; V_{EE} = -5.2V	-2.5		+6.0	V
		V_{CC} = 12V; V_{EE} = -3.2V	-0.5		+8.0	V
		V_{CC} = 8V; V_{EE} = -7.2V	-4.5		+4.0	V

DC Electrical Characteristics (continued)

Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Units
I_H	Bias Current @ V_H	$-1V \le V_H \le +7V$; $V_L = -2.0V$		1.0	2.0	µA
I_L	Bias Current @ V_L	$-2V \le V_L +5V$; $V_H = 6.0V$		1.0	2.0	µA
TCI_H	Temperature Drift in I_H	$V_H = 7.0V$; $25°C \le T_C \le 70°C$ output not switching			0.1	µA/°C
TCI_L	Temperature Drift in I_L	$V_L = -2.0V$; $25°C \le T_C \le 70°C$ output not switching			0.1	µA/°C
$V_{H, L}BW$	-3 dB bandwidth from V_H or V_L to the output	$-1V \le V_H \le +7V$ $-2V \le V_L \le +6V$; $V_H - V_L = 2.0V$		50		kHz
Signal Output V_O, V_{OTERM}						
V_O	Output Voltage Range	$V_{CC} = 10V$; $V_{EE} = -5.2V$ $V_{CC} = 12V$; $V_{EE} = -3.2V$ $V_{CC} = 8V$; $V_{EE} = -7.2V$	-2.2 -0.5 -4.5		+7.0 +9.0 +5.0	V V V
V_A	Amplitude	$\lvert V_{OH} - V_{OL} \rvert$	0.3		9.2	V
ΔV_{OH}	Offset to Output High Level	$V_H = 0$, no load; $V_L = -2V$ $\Delta V_{OH} = \lvert V_H - V_{OH} \rvert$		±30	±60	mV
ΔV_{OL}	Offset to Output Low Level	$V_H = 0$, no load; $V_H = +7V$ $\Delta V_{OL} = \lvert V_L - V_{OL} \rvert$		±30	±60	mV
ΔV_{OH} ΔV_{OL}	Change in V_{OH} output level with change in V_L	$V_{OH} = +5V$, $\Delta V_L = 0$ to $+1V$		±10	±15	mV
ΔV_{OL} ΔV_{OH}	Change in V_{OL} output level with change in V_H	$V_{OL} = +5V$, $DV_H = +4$ to $+5V$		±10	±15	mV
VTC	Output Voltage Drift	$-1V \le V_{OH} \le +7V$; $-2V \le V_{OL} \le +6V$;		0.1 0.1		mV/°C
ε_G	Gain Error	$-1V \le V_{OH} \le +7V$; $-2V \le V_{OL} \le +6V$		1.0 1.0	2.0 2.0	%FS
ε_L	Linearity Error	$-2V \le V_{OUTPUT} \le +7V$		0.7	1.0	%FS
Z_{OUT}	Output Impedance (I_{OUT} = 50 mA)		7.0	9.0	11	Ω
I_{ZL}	Output Leakage Current in Inhibit Mode (maintain the following: $\lvert V_L - 1.0V \rvert \le V_O \le \lvert V_H + 1.0V \rvert$)	$-2.0V \le V_O \le +7V$		0.5	2.0	µA
I_{DC}	DC Current Drive		50			mA
I_{AC}	AC Current Drive		70	100		mA
Thermal Shutdown Output (TS)						
I_{CL}	Short Circuit Current Limit				145	mA
VTS	TS Flag Output Level	I_{OL} = 4 mA			0.5	V
T_{TS}	Shutdown Die Temperature			130	145	°C
Other						
$V_{S\ MAX}$	Maximum Rail-to-Rail Supply Voltage	$V_{CC} - V_{EE}$			16	V
V_{CC}	Positive Supply		+8.0	+10.0	+12.0	V

DC Electrical Characteristics (continued)

Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Units
V_{EE}	Negative Supply		-7.2	-5.2	-3.2	V
I_{CC}	Positive Supply Current			85	90	mA
IEE	Negative Supply Current			90	100	mA
$PSRV_O$	Output Level Power Supply	V_{CC}; ΔV_{CC} = ±2.5%	40			dB
	Rejection Ratio	V_{EE}; ΔV_{EE} = ±2.5%	40			dB
$PSRV_{SL}$	Output Slew Rate Power Supply	V_H = 5V, V_L = 0V, ΔV_{CC} = ±200 mV		4.0		%
	Rejection Ratio	V_H = 5V, V_L = 0V, ΔV_{CC} = ±200 mV		4.0		%
T_A	Operating Temperature Range	Still Air	0	25	40	°C
		Air Flow > 300 l_{fpm}	0	25	70	°C

AC Electrical Characteristics

V_{CC} = 10V ±3%, V_{EE} = -5.2V ±5%, T_A = 25°C (still air) and the load is a 50Ω transmission line with 2.0 ns one-way delay, unless otherwise specified. The transmission line is back-terminated in 50Ω (±5%) using an external resistor. The measurement probe is a high impedance FET probe with capacitance no greater than 3 pF and resistance no smaller than 10 kΩ.

Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Units
SLR	Slew Rate	V_H - V_L = 5V; Measured between 20% and 80% points.				
		With probe only as load		1.6		V/ns
		With probe and transmission line		1.5		V/ns
t_R,	Rise Time, and	Load is Probe Only;				
t_F	Fall Time	V_A = 1V (20% to 80%)		0.6	0.9	ns
	(Slew rate not adjusted)	V_A = 3V (10% to 90%)		1.6	2.1	ns
		V_A = 5V (10% to 90%)		2.5	3.0	ns
f	Toggle Rate	Amplitude = 0.8 Vp-p	250			MHz
	(Probe only)	Amplitude = 5.0 Vp-p	125			MHz
t_{PLH}	Low to High Propagation Delay	f = 10 MHz; V_{OH} = +0.4V;				
		V_{OL} = -0.4V		1.6		ns
t_{PHL}	High to Low Propagation Delay	f = 10 MHz; V_{OH} = +0.4V;				
		V_{OL} = -0.4V		1.4		ns
Δt_P	Propagation Delay Match	$\lvert t_{PLH} - t_{PHL} \rvert$		200		ps
t_PTC	Propagation Delay Temperature Coefficient			2.0		ps/°C
tPW_{min}	Minimum Pulse Width	V_H - V_L - 2.0V; pulsewidth at which amplitude drops by 50 mV, measured between 50% points.		2.0		ns
Δt_PPW	Propagation Delay Variation with Pulse Width	2 ns < PW < 98 ns; f = 10 MHz; V_{OH} = +0.4V; V_{OL} = -0.4V		±75		ps
t_{PS}	Preshoot	0.5V < V_A < 5.0V			15mV + 3% of V_A	mV

AC Electrical Characteristics (continued)

Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Units
t_{OS}	Overshoot	$0.5V < V_A < 5.0V$			50mV + 4% of V_A	mV
t_S	Output Settling Time	V_A < 5V; To within 3% of V_A To within 1% of V_A		 8 10		 ns ns
t_{PHZ}	Propagation Delay from Logic High to Inhibit Mode	V_{OH} = 1V; V_{OL} = -1V Load = 100Ω || 15pF		2.9		ns
t_{PLZ}	Propagation Delay from Logic Low to Inhibit Mode	Propagation delay is measured to the point at which voltage has changed by 200 mV.		2.9		ns
t_{PZH}	Propagation Delay from Inhibit Mode from Logic High			2.9		ns
t_{PZL}	Propagation Delay from Inhibit Mode to Logic Low			2.9		ns
C_Z	Output capacitance in Inhibit Mode			3.0		pF

Notes:

Notes:

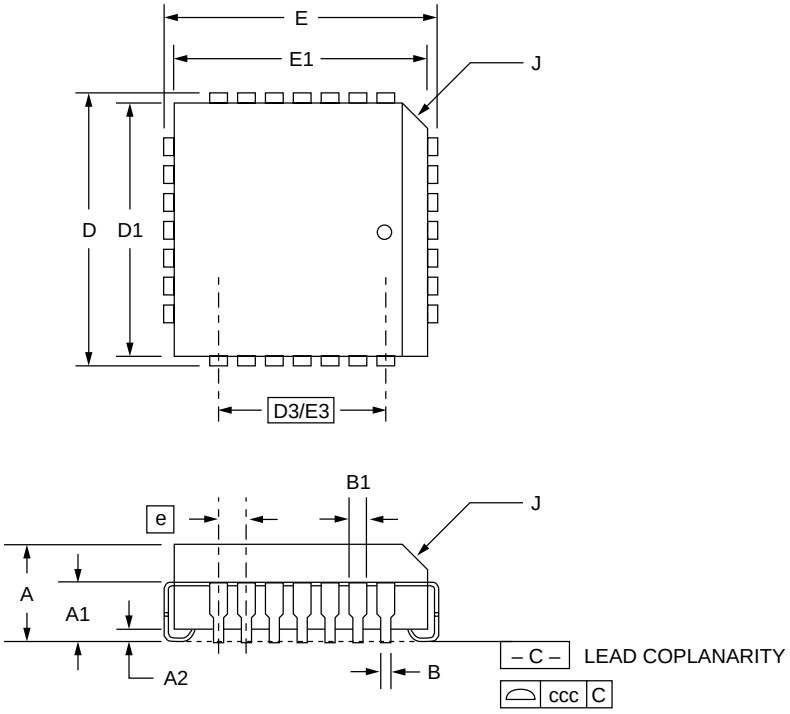
Notes:

Mechanical Dimensions — 28-pin PLCC

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.180	4.19	4.57	
A1	.090	.120	2.29	3.05	
A2	.020	—	.51	—	
B	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D/E	.485	.495	12.32	12.57	
D1/E1	.450	.456	11.43	11.58	3
D3/E3	.300 BSC		7.62 BSC		
e	.050 BSC		1.27 BSC		
J	.042	.048	1.07	1.22	2
ND/NE	7		7		
N	28		28		
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Corner and edge chamfer (J) = 45°.
3. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is .101" (.25mm).



Ordering Information

Package	Order Number
28-pin PLCC	RC7321QF

RC7352

Parametric Measurement Unit

Features

- Force voltage/measure current and force current measure voltage functions
- Forced voltage range (-5V to +15V)
- Four programmable measured current ranges:
  Range A = ±20μA max
  Range B = ±200μA max
  Range C = ±1.0mA max
  Range D = ±40mA max
- High resolution current force/measure ±0.05% = 2 bits
- Internal control circuitry for selecting ranges
- High accuracy: 12 bit linearity and 0.5% gain error
- High current range D current limit protection set externally by the value of resistor R_{DIL}
- Measurement output voltage can be disabled
- Forced current ranges:
  Range A = ±20μA max
  Range B = ±200μA max
  Range C = ±1.0mA max
  Range D = ±40mA max
- Measured voltage range: -5V to +15V
- High resolution voltage measurement (±0.05%) and accuracy: (±10mV max. offset) and 0.5% gain error
- Internal current limit for ranges (A, B, & C)

Applications

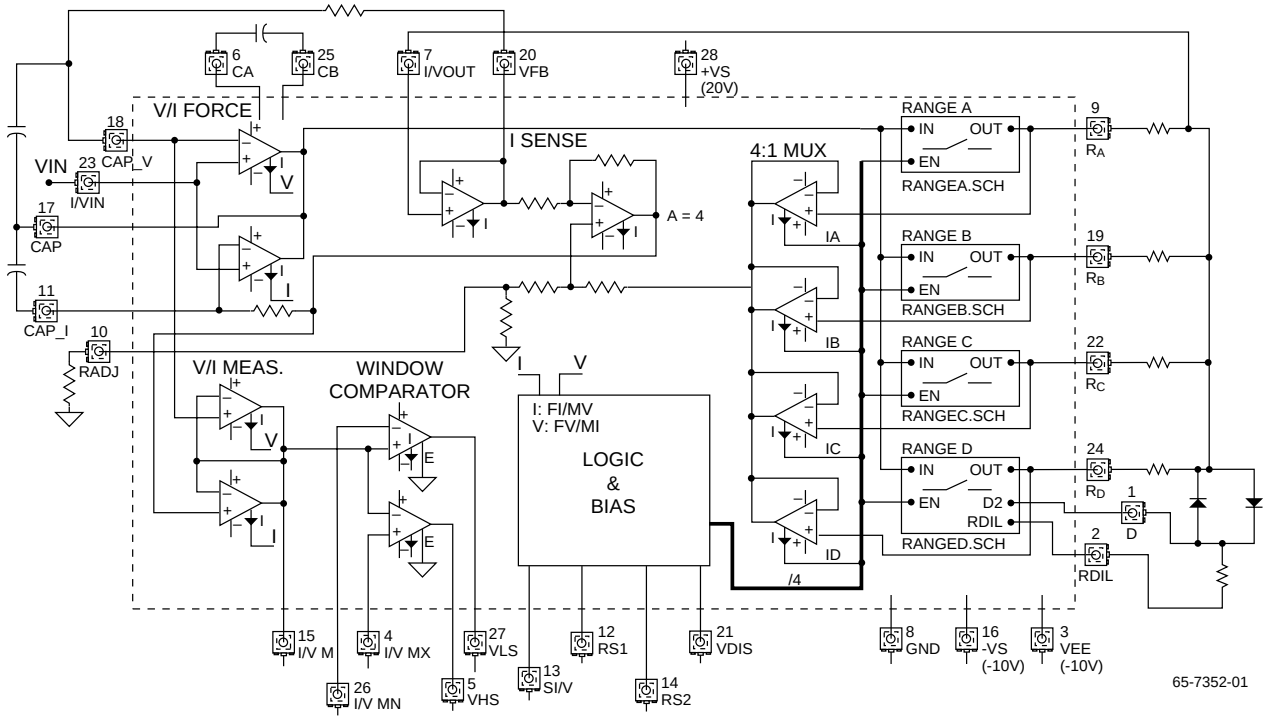
- ATE pin electronics measurements
- Instrumentation, meters
- Programmable voltage or current supply

Description

The RC7352 is a “Per Pin” Parametric Measurement Unit (PMU) that can force voltage and measure current or force current and measure voltage. The RC7352 forces voltages from +15V to -5V when $+V_S$ is 20V and $–V_S$ is -10V, or currents up to ±40mA. All logic inputs for the RC7352 are TTL compatible, while the open collector logic outputs are TTL/CMOS compatible.

Setting the SI/V (Select I/V) pin low puts the RC7352 in the force voltage and measure current mode. The resulting output voltage at the DUT matches the input applied to the

Block Diagram



I/VIN pin (please refer to block diagram). The I/VM pin provides a voltage proportional to the DUT current. V(I/VM) = (4 x R x I(DUT)), where R is the external range resistor (0.05% tolerance) and I(DUT) is the current supplied to the load. The resistors in the application circuit were chosen using this formula R range = (2V/Imax), for Range A this is RA = 2/20 μA or 100K.

When SI/V is high the RC7352 will force current and measure voltage. The range select pins RS1 and RS2 control the maximum output current (see Table 1), while magnitude of the forced current is given by the expresion

I(DUT) = V(I/VIN)/(4 x R)

where R is the range resistor. In the FI/MV mode the voltage at the I/VM pin equals the device voltage. The I/VM pin can be connected to an A/D convertor to monitor the current or voltage at the load device.

The RC7352 also has a window comparator that can provide upper or lower limit fail information. I/Vmx and I/Vmn are voltage inputs for the upper and lower limits respectively. You must use the formulas listed above to calculate current limits for each range while voltage limits are 1:1. Their corresponding outputs, VHF (V high fail) and VLF (V low fail) can be used individually or “Wire ORed” to obtain a composite signal. Additionally the VDIS pin can be set high to disable the window comparator and its I/O lines. Although this reduces overall power consumption, it also disables the I/VM output.

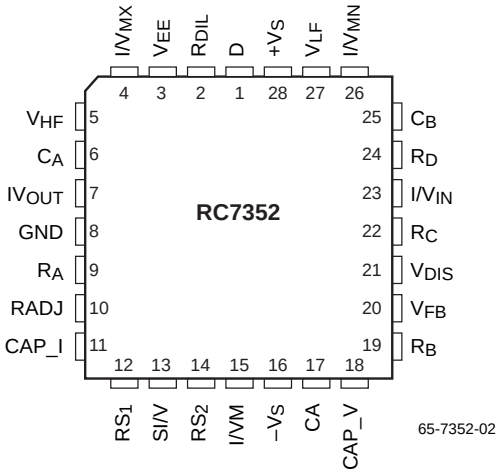
Table 1. Maximum Output Current on Pin Select

SI/V	RS2	RS1	Mode
0	0	0	FV/MI Range A, Imax = ±20 μA
0	0	1	FV/MI Range B, Imax = ±200 μA
0	1	1	FV/MI Range C, Imax = ±1.0 mA
0	1	0	FV/MI Range D, Imax = ±40 mA
1	0	0	FI/MV Range A, Imax = ±20 μA
1	0	1	FI/MV Range B, Imax = ±200 μA
1	1	1	FI/MV Range C, Imax = ±1.0 mA
1	1	0	FI/MV Range D, Imax = ±40 mA

Notes:

1. FV/MI = Force Voltage Measure Current.
2. FI/MV = Force Current Measure Voltage.
3. $+V_S - 5 \geq V_{OUT} \geq -V_S + 5$

Pin Assignments



Pin Description

Pin Name	Pin Number	Pin Description
$+V_S$	28	$+V_S$ should be bypassed to ground with a 10.0 μF tantalium capacitor placed as close to the pin as possible.
$-V_S$	16	$-V_S$ should be bypassed to ground with a 10.0 μF tantalium capacitor placed as close to the pins as possible.
V_{EE}	3	V_{EE} is the negative supply for range D. This pin should be bypassed with a 0.1 μF ceramic capacitor to ground.
GND	8	This pin should be connected to the printed circuit board's ground plane.
I/V_{IN}	23	Input reference voltage for V_{OUT} or I_{OUT}. In the force voltage measure current mode (FV/MI) $V(I/V_{OUT}) = V(I/V_{IN})$ and $V(I/VM) = 4 \times I_{OUT} \times R$ Where I_{OUT} is the device output current and R is the range resistor. In the Force Current/Measure Voltage Mode $I_{OUT} = \frac{V(I/VIN)}{4 \times R}$ $V(I/VM) = V(I/V_{OUT})$
I/V_{OUT}	7	The Load or Device under test is connected to I/V_{OUT}. The current to the load is supplied via the appropriate range resistor with I/V_{OUT} serving as the voltage feedback point for the PMUs internal instrumentation amplifier.
SI/V	13	A TTL/CMOS signal applied to this pin selects either Force Voltage/Measure Current or Force Current/Measure Voltage mode. A TTL/CMOS low level will select Force Voltage/Measure Current function. A TTL/CMOS high level selects Force Current/ Measure Voltage mode.
R_A	9	Resistor R_A should be placed between R_A and I/V_{OUT}. R_A tolerance should be better than +0.05% to improve gain error. Maximum current for range A is shown in the equation below. $I_A = \frac{\pm 2V}{R_A}$ The ±2 volts represents the maximum voltage V_A across R_A. For Range A, I_A should not exceed ±20 μA, i.e., R_A should be higher than or equal to 100 kΩ. A metal film resistor should be used to reduce inherent resistor noise (schott and pop corn noise) and improve resolution. For maximum stability, a 300 pF capacitor should be connected across R_A.
R_B	19	For Range B, I_B should not exceed ±200 μA, i.e., R_B should be higher than or equal to 10 kΩ with ±0.05% tolerance. For maximum stability a 1,000 pF capacitor should be connected across R_B.
R_C	22	For Range C, I_C should not exceed ±1 mA, i.e., R_C should be higher than or equal to 2 kΩ with ±0.05% tolerance.
R_D	24	For Range D, I_D should not exceed ±40 mA, i.e., R_D should be higher than or equal to 50 Ω with ±0.05% tolerance.
D	1	Two diodes must be connected between D & R_D as shown in the block diagram.
C_A, C_B	6, 25	A 30pF capacitor placed between these pins will improve stability.
R_{DIL}	2	Range D output for current limiting. An external resistor is connected between RDIL and D to limit current to a value $I_{LIM} = 0.8V/R_{LM}$.

Pin Description (continued)

Pin Name	Pin Number	Pin Description
R_{S1}, R_{S2}	12, 14	R_{S1} and R_{S2} are TTL or CMOS compatible. The truth table below shows the range selection table. R_{S1} R_{S2} Range Selected L L A L H B H H C H L D
I/V_{MX}, I/V_{MN}	4, 26	The voltage applied to pin 4 sets the upper current or voltage limit for the measurement at pin 15 I/VM. To set the desired limit for current measurement a voltage equaling (4 x I_L x R) must be applied on this pin. R is the external resistor of the selected range (A, B, C, or D). For voltage measurement the voltage applied to this pin is the limit.
V_{HF}	5	V_{HF}, High Fail, is an open collector output that requires a pull-up to the logic supply. If the voltage at pin 15, I/VM, is greater than the threshold voltage at pin 4, I/V_{MX}, V_{HF} will become a logic low. The open collector structure makes wire-ORing of multiple PMU's possible. Connect a 3,000 pF capacitor to GND to minimize oscillation at the cross-over point.
V_{LF}	29	V_{LF} mirror V_{HF} for the lower threshold I/V_{MN}. Connect a 3,000 pF capacitor to GND to minimize oscillation at the cross over point.
V_{DIS}	21	When V_{DIS} is tied to ground output I/VM, V_{HF} and V_{LF} are enabled. If V_{DIS} is open V_{HF} and V_{LF} will require external pullups to maintain a logic high. And I/VM will be in a high impedance state.
I/VM	15	In the Force Voltage/Measure Current mode this output voltage is equal to four times the voltage across external resistor R of selected range A, B, C, or D through which the measured current is flowing ($(I/V)_M = 4.0 \times I_M \times R$). In the Force Current/ Measure Voltage mode this output is equal to the voltage at I/V out. This output can be disabled by applying a TTL HI on the V_{DIS} pin. (Pin 21)
V_{FB}	20	V_{FB}, voltage feedback, is the buffered output voltage, I/V_{OUT}. This pin should not be loaded. Connect a 50K 1% resistor from V_{FB} to CAP_V.
RADJ	10	The RADJ pin is provided to adjust the offset for the I_{SENSE} function. The best accuracy for V/IM is obtained when RADJ is shorted to analog ground. The point is terminated with a 100 Ω resistor in the block diagram.
CAP_I CAP_V CA	11 18 17	CA is the common point for two 50 pF compensation capacitors that improve the stability of the PMU. These components are optional and can be omitted for some loads.

Absolute Maximum Ratings[1]

Parameter	Min.	Max.	Units
Absolute Difference, $+V_S$+|–VS|		32	V
Digital Control Inputs			
SI/V, RS_1, RS_2, V_{DIS}	-2	+6	V
Comparator Inputs			
I/V_{MN}, I/V_{MX}	$I/V_{MN} \le +V_S$	$-V_S \le I/V_{MX}$	V
I/V_{IN}		$-V_S \le I/V_{IN} \le +V_S$	V

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Recommended Operating Conditions

Symbol	Parameters	Min.	Typ.	Max.	Units
T_C	Case operating temperature	0		70	°C
$+V_S$	Positive supply voltage[1]	10.4	20.0	20.6	V
–VS	Negative supply voltage[1]	-15.75	-10.0	-9.5	V
V_{EE}	Negative supply voltage for range D[2]		$-V_S$		V
R_A	Resistor for I_A current range	100		2000	KΩ
R_B	Resistor for I_B current range	10		200	KΩ
R_C	Resistor for I_C current range	2		40	KΩ
R_D	Resistor for I_D current range	50		1000	Ω

Notes:

1. $+V_S$ + |–VS| ≤ 30V $+V_S$ + |–VS| ≥ 24
2. $-V_S$ & V_{EE} are always at the same voltage.

DC Electrical Characteristics

$+V_S$ = 20V ±3%, $–V_S$ = -10V ±5% T_A = 25°C, and external ±0.05% tolerance resistors R_A = 1000kΩ, R_B = 10kΩ, R_C = 2kΩ, and R_D = 50Ω unless otherwise specified.

Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Units
Forced Current/Measure Voltage						
I/V_{IN}	Input Voltage Range For Setting Forced Current (I_F)	I/VF_{IN} = 4 x I_F x R	-8		+8	V
I/V_M	Measured Voltage Output @ $(I/V)_M$	All ranges, full scale current	-5		+15	V
	Output Sink/Source Current	$(I/V)_M$ = -5V, +15V	-200		+200	µA
V_{MR}	Voltage Measured Resolution		-.05	±0.025	+0.05	%FSR
V_{OR}	Voltage Measurement Offset	I/V_{IN} = 0V; Measured @ I/VM	-6.0	±2	+6.0	mV
V_{GE}	Voltage Gain Error	Gain of 4	-2.0	+0.5	+2.0	%
CMRR[1] I_{OER}	I_{OUT} Error Due to Common Mode Load Voltage	-5V ≤ I/V_{OUT} ≤ +15V; Measured @ $(I/V)_M$	45	60		dB
Forced Voltage/Measure Current						
I/V_{IN}	Force Input Voltage Range	All ranges, full scale current	-5		+15	V
I/VF_{VOS}	Forced Voltage Offset	I/V_{IN} = 0V, measure I/V_{OUT} and VFB	-6.0	±2	+6.0	mV
	Forced Voltage Linearity Error			±0.025	±0.05	FSR%
CMRR[2] VLER	I_{OUT} Measure Error Due to I/VM Common Mode Voltage	-FSR ≤ I_{OUT} ≤ +FSR; Measured @ $(I/V)_M$	45	60		dB
I/V_{OUT}	Forced Output Voltage Range	All ranges, full scale current	-5		+15	V
I/V_M	Voltage Output Equivalent to Measured Current: $(I/V)_M$ = 4 x I_F x R	All ranges, full scale voltage	-8		+8	V
I	I measured; I = $(I/_{VM})/(4R)$	I/V_M = -8.0V, +8.0V; full scale	-200		+200	µA
Current Ranges						
Range A						
I_A	Maximum Full Scale Current	R_A = 100kΩ (0.05%)			±20	µA
I_{AMR}	Current Measurement Resolution	guaranteed by design		±0.025		%
I_{LIN}	Linearity[3]		-0.05	±0.025	+0.05	
I_{GE}	Current Gain Error[4]		-2.0	0.5	+2.0	%
I_{FIOS}	Force Current Offset[5]	I/V_{IN} = 0V	-25	±10	+25	nA
I_{MIOS}	Measure Current Offset[6]	I/V_{IN} = 0V	-25	±10	+25	nA
Range B						
I_B	Maximum Full Scale Current	R_B = 10kΩ (0.05%)			±200	µA
I_{BMR}	Current Measurement Resolution	guaranteed by design		±0.025		%
I_{LIN}	Linearity[3]		-0.05	±0.025	+0.05	
I_{GE}	Current Gain Error[4]		-2.0	±0.5	+2.0	%
I_{FIOS}	Force Current Offset[5]		-250	±100	+250	nA
I_{MIOS}	Measure Current Offset[6]		-250	±100	+250	nA

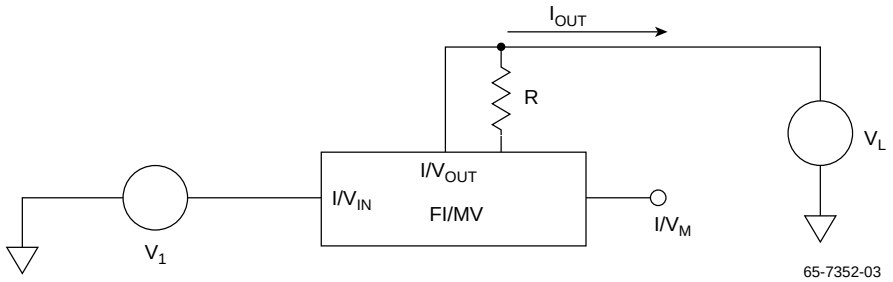
DC Electrical Characteristics (continued)

Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Units
Range C						
I_C	Maximum Full Scale Current	R_C = 2kΩ (0.05%)			±1	mA
I_{CMR}	Current Measurement Resolution	guaranteed by design		±.025		%
I_{LIN}	Linearity[3]		-0.05	±.025	+0.05	%
I_{GE}	Current Gain Error[4]		-2.0	±0.5	+2.0	%
I_{FIOS}	Force Current Offset[5]		-1.5	±0.5	+1.5	µA
I_{MIOS}	Measure Current Offset[6]		-1.5	±0.5	+1.5	µA
Range D						
I_C	Maximum Full Scale Current	R_D = 50Ω (0.05%)			±40	mA
I_{DMR}	Current Measurement Resolution Current Measurement Accuracy	guaranteed by design		±.025		%
I_{LIN}	Linearity[3]		-0.05	±.025	+0.05	%
I_{GE}	Current Gain Error[4]		-2.0	±0.5	+2.0	%
I_{FIOS}	Force Current Offset[5]		-50	±20	+50	µA
I_{MIOS}	Measure Current Offset[6]		-50	±20	+50	µA
Digital Control Inputs (SI/V, RS_1, RS_2)						
V_{IH}	Internal Threshold Voltage		0.8	1.4	2.0	V
I_{LH}	Logic High Bias Current	V_H = 2.0V		200		nA
I_{LL}	Logic Low Bias Current	V_L = 0.8V		2.0		nA
Digital Control Input V_{DIS}						
V_{IH}	Internal Threshold Voltage		0.8	1.4	2.0	V
I_{LH}	Logic High Bias Current	V_H = 2.0V		1.0		µA
I_{LL}	Logic Low Bias Current	V_L = 0.8V		2.0		nA
Comparator Input; I/V_{MAX}, I/V_{MIN}						
$I/V_{MX,MN}$	Input Voltage Range		-8.0		+15	V
I_H	Input Bias Current (Logic High)	V_H = +15V		0.4		µA
I_L	Input Bias Current (Logic Low)	V_L = 0.8V		0.4		µA
Comparator Status Outputs; V_{HF}, V_{LF}						
V_{OH}	Output Voltage (Logic High)	R_{PULLUP} = 10kΩ	3.5			V
V_{OL}	Output Voltage (Logic Low)	R_{PULLUP} = 10kΩ			0.8	V
I_{OH}	Output Current High	V_{OUT} = 5.0V		0.1		µA
I_{OL}	Output Current Low				1.0	mA
I_Z	Output Leakage Current Disable State	V_{OUT} = 5.0V		0.1		µA
Other						
I+ (1.0)	Positive Supply Current	No load Range A		4.0	11.0	mA
I- (2.0)	Positive Supply Current	No load Range A		4.0	11.0	mA

Notes:

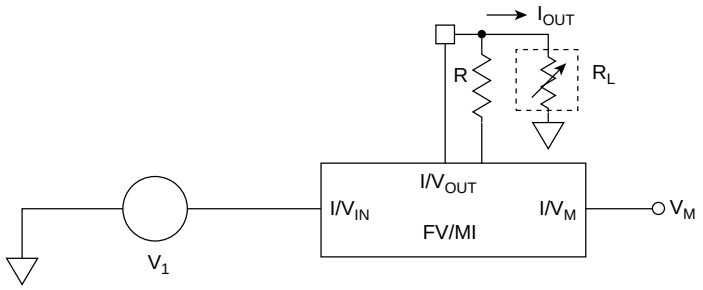
1. CMRR is measured with V_L=15V/-5V; R is R_A, R_B, R_C or R_D; V_1 = constant; This parameter is to define the I_{OUT} current error due to the V_L common mode voltage for a constant V_1. This parameter is guaranteed to full V_1 range. (±8V)

$$CMRR = 20 \log\left(\frac{\Delta I_{OUT} \times 4 \times R}{\Delta V_L}\right)$$



2. CMRR is measured with V_1 = +15V/-5V; R is R_A, R_B, R_C or R_D; I_{OUT} = constant. This parameter is to define the current measurement error due to the input voltage V_1. It guarantees all ranges and ± full scale I_{OUT}.

$$CMRR = 20 \log\left(\frac{\Delta V_M}{\Delta V_1}\right)$$



3. Linearity is measured against two point straight line calibration with five measurement points.
4. Current Gain Error is measured with –full scale current to +full scale current. The ideal gain is 4.

$$\text{Current Gain Error} = \left|\frac{VM_2 - VM_1}{R(I_{OUT2} - I_{OUT1})}\right|$$

5. Force current is measured with I/V_{OUT} to ground with I/V_{IN} = 0V.
6. Measured current offset is measured with I/V_{IN} = 0V, Offset = (I/VM)/4R where R is R_A, R_B, R_C, and R_D.

AC Electrical Characteristics

$+V_S$ = 20V ±3%, $-V_S$ = -10V ±5%, T_A = 25°C, and external ±0.05% tolerance resistors R_A = 100kΩ, R_B = 10kΩ, R_C = 2kΩ, and R_D = 50Ω unless otherwise specified.

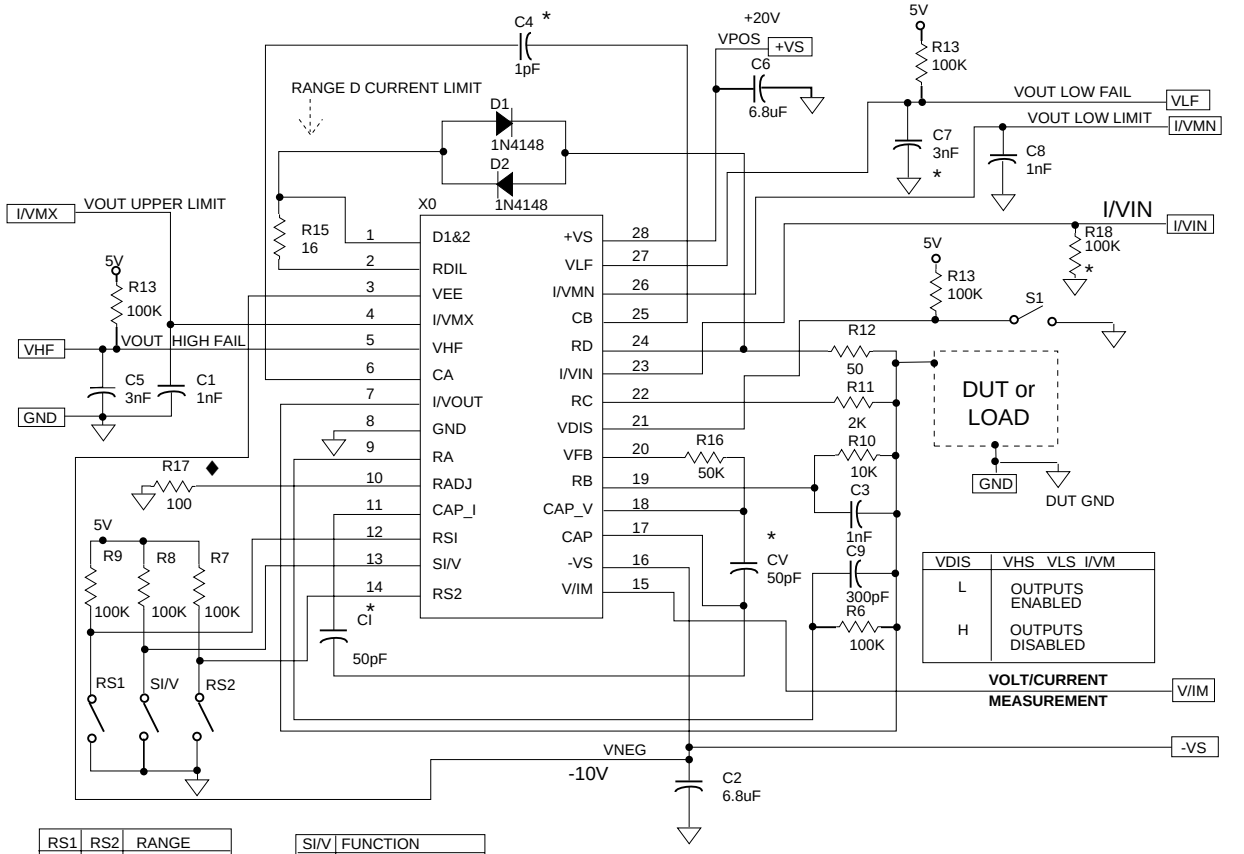
Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Units
Comparator						
t_{HL}	Response Time High to Low	R_{LOAD} = 10k, 5mV Overdrive		1.1		µs
t_{LH}	Response Time Low to High	R_{LOAD} = 10k, 5mV Overdrive		450		ns
Differential Amplifier						
t_{MZF}	Response Time (setting time)[1] Force Current/Measure Voltage	Range A Range B Range C Range D Voltage @ I/V_M = -5.0V to +15V I_F = Max		2.4 2.3 2.6 2.6		ms
t_{MZF}	Response Time (settling time)[1] Force Voltage/Measure Current	Ranges A Ranges B Ranges C Ranges D Voltage @ I/V_{OUT} = 5.0V to +15V I_M = Max		2.4 2.5 2.6 2.7		ms
t_{MZF}	Response Time (Settling time)[1]	Ranges A, B, C, & D Voltage @ I/V_{OUT} = -2.0V to +6.0V 30pF from CA to CB No Load		1.0	3	ms
t_{DS}	Output Disable to Enable Time			20		µs

Notes:

1. Response Time (settling time) for Force Current/Measure Voltage mode is measured with 30pF from CA to CB and I/V_{IN} Voltage Swings from -8.0V to +8.0V, and RL value for Range placed between I/V_{OUT} and 5V.

500KΩ	A
50KΩ	B
10KΩ	C
250Ω	D

Application Example



RS1	RS2	RANGE
L	L	A +/-20uA
L	H	B +/-200uA
H	H	C +/-1mA
H	L	D +/-40mA

SI/V	FUNCTION
L	FORCE VOLTAGE
H	FORCE CURRENT

* OPTIONAL PART

♦ SHORT RADJ TO GND FOR BEST DC ACCURACY

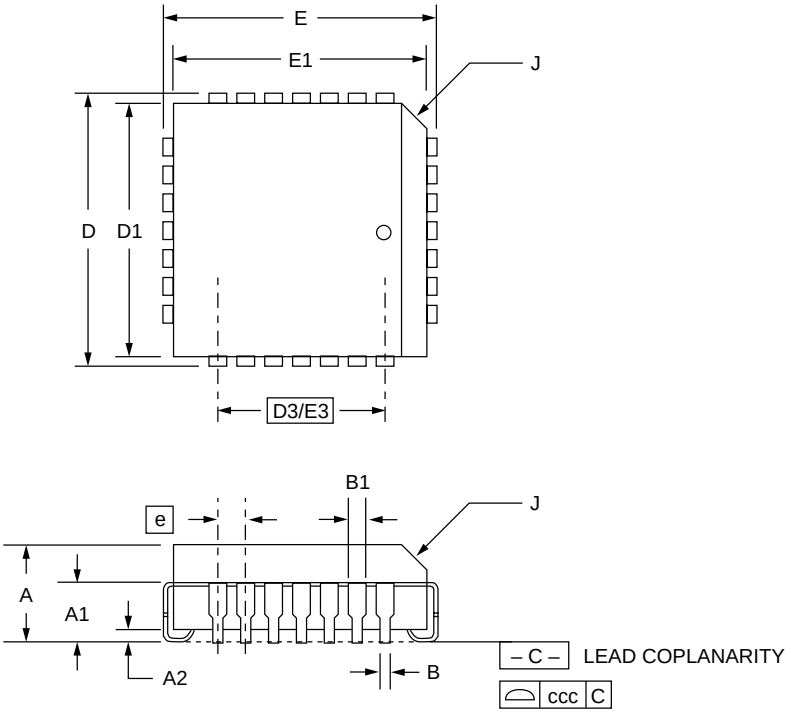
65-7352-05

Mechanical Dimensions

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.180	4.19	4.57	
A1	.090	.120	2.29	3.05	
A2	.020	—	.51	—	
B	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D/E	.485	.495	12.32	12.57	
D1/E1	.450	.456	11.43	11.58	3
D3/E3	.300 BSC		7.62 BSC		
e	.050 BSC		1.27 BSC		
J	.042	.048	1.07	1.22	2
ND/NE	7		7		
N	28		28		
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Corner and edge chamfer (J) = 45°.
3. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is .101" (.25mm).



Ordering Information

Part Number	Package
RC7352QA	28-pin PLCC

RC73687

High Speed Dual Comparator

2.2 ns Propagation Delay

Features

- 12 V max differential input voltage (for V_{CC} = +10V, V_{EE} = -5.2V)
- Low propagation delays: -1.8 ns typical
- Low delay dispersion (±65 ps typical) and drift (4 ps/°C typical)
- ±5 mV maximum input offset and 10 μV/°C max. drift
- ±3 μA typical bias current; 50 pA typ. in **disable mode**
- Common mode rejection ≥ 70 dB
- Input disable mode (transparent to user)
- Latch function
- RC73687 is pin-for-pin compatible with 9687 comparators
- Available in 16-pin SOIC, 20-pin PLCC or 16-pin PDIP

Applications

- ATE pin electronics
- Threshold/peak voltage detector
- Level line receiver
- Limiting amplifier

Description

The RC73687 is a very high speed dual comparator with latched input option and ECL compatible outputs capable of driving 50Ω terminated lines. The RC73687 is configured as two independent comparators and is pin-for-pin compatible with the industry standard 9687 comparators. The RC73687 low propagation delay (2.2 ns maximum), wide input common range (-4V to +8V) and low bias current (±5 μA maximum) makes it ideal for monitoring outputs from TTL, CMOS, ECL and even GaAs devices in ATE applications. The propagation delay dispersion is only ±80 ps (typical).

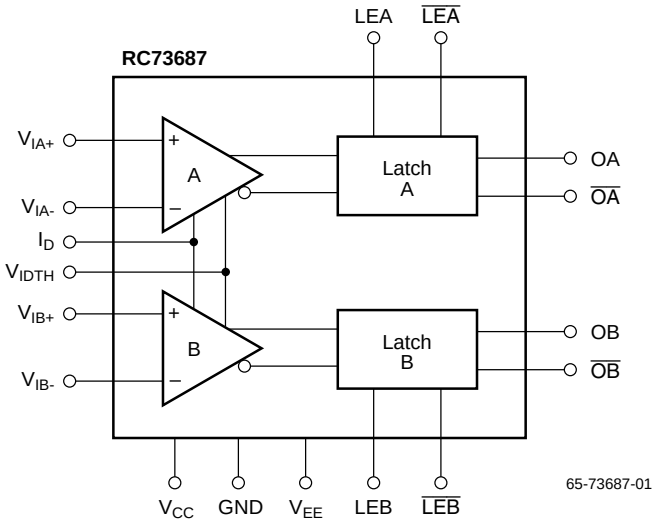
The RC73687 features a high impedance input mode (I_D) that reduces the bias current to ±50 pA (typical), effectively removing the DC electrical load of the comparator inputs. The RC73687 also has a latch function to sample the input waveforms. Latches A and B are controlled by differential latch enable (LEA and LEB) ECL signals.

The RC73687 is designed to operate with VCC supply voltages of +5.0V to +10V.

Operation at +10V will provide a wider input common mode voltage range, (-4V to +8V) versus (-4V to +3V). It also provides a lower input capacitance (1.0 pF) versus (1.5 pF)

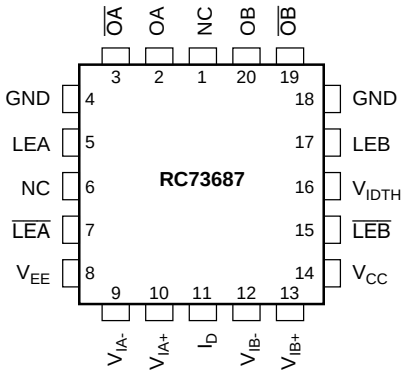
The RC73687 is fabricated using Fairchild's high performance complementary bipolar process.

Block Diagram

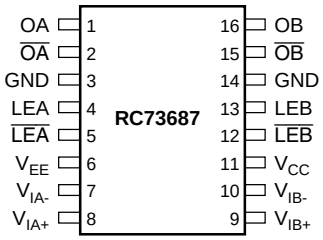


Pin Assignments

PLCC



SOIC and PDIP



Note: Input disable mode not available on RC73687 SOIC package.

65-73687-02

Pin Description

Name	Pin Number PLCC	Pin Number SOIC, PDIP	Function
GND	4, 18	3, 14	**Chip ground.** This pin should be connected to the printed circuit board's ground plane at the pin.
LEA, LEB $\overline{LEA}$, $\overline{LEB}$	5, 17, 7, 15	4, 13, 5, 12	**Differential digital enable inputs for latches A and B.** Although these inputs will be normally driven by ECL signals, they have a wide enough common mode range that they may be driven by a TTL or CMOS signal provided the other input is tied to the appropriate threshold. If LEA or LEB inputs are tied to a logic high, then latches A and B are transparent, and output A or B will track changes to comparator A or B respectively. A logic low on LEA or LEB will disable the latch, and the outputs will reflect the input state just prior to the latch disable command.
I_D, V_{IDTH}	11, 16	—	**I_D is the differential non-inverting input and V_{IDTH} is the inverting input for enabling/disabling the comparator.** Although the inputs will normally be driven by ECL signals, they have a wide enough common mode range that they may be driven by a TTL or CMOS signal provided the other input is tied to the appropriate threshold. When I_D and V_{IDTH} pins are left open they remain internally biased a +2.5 volt and -1.3 volts respectively and the circuit defaults to a comparator input enable state. A differential voltage of 400 mV must be exceeded to disable the comparator input. The disabled inputs will have a typical bias current of ±50 pA.
OA, $\overline{OA}$	2, 3	1, 2	**Differential outputs for comparator A.**
OB, $\overline{OB}$	20, 19	16, 15	**Differential outputs for comparator B.** Each comparator can drive 50Ω terminated lines to 2 V_{TT}.
V_{CC}	14	11	**Quiet positive supply.** The nominal voltage is 10V ±3%. V_{CC} should be bypassed to ground with a 0.01μF chip ceramic capacitor placed as close to the pins as possible.
V_{EE}	8	6	**Quiet negative supply.** The nominal voltage is -5.2 ±5%. V_{EE} should be bypassed to ground with a 0.01 μF chip capacitor placed as close to the pins as possible.
V_{IA+}, V_{IB+}	1, 13	8, 9	**Differential non-inverting inputs.**
V_{IA-}, V_{IB-}	9, 12	7, 10	**Differential inverting inputs.**

Absolute Maximum Ratings[1]

Parameter	Min.	Max.	Units
Positive power supply, V_{CC}		+11.0	V
Negative power supply, V_{EE}	-6.3		V
Difference between V_{CC} and V_{EE}		16.6	V
Input voltage at V_{IA+}, V_{IB+}		V_{CC}+0.7	V
Input Voltage at V_{IA-}, V_{IB-}	V_{EE}–0.7		V
Differential input voltage, $\lvert V_{IA+} - V_{IA-} \rvert$, $\lvert V_{IB+} - V_{IB-} \rvert$		12	V
Input voltage at LEA, LEB		V_{CC}	V
Input voltage at $\overline{LEA}$, $\overline{LEB}$		V_{EE}	V
Input voltage at I_{D+}, I_{D-}		V_{CC}, V_{EE}	V
Differential input voltage, $\lvert LEA - \overline{LEA} \rvert$ $\lvert LEB - \overline{LEB} \rvert$		7	V
Operating temperature range	-40	+85	°C
Storage temperature range	-65	+125	°C
Lead temperature range (Soldering 10 seconds)		+260	°C

Notes:

1. “Absolute maximum ratings” are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. If the device is subjected to the limits in the absolute maximum ratings for extended periods, its reliability may be impaired. The tables of Electrical Characteristics provide conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameters	Min.	Typ.	Max.	Units
T_C	Case operating temperature	0		+70	°C
V_{CC}	Positive supply voltage	4.75	5.0	10.3	V
V_{EE}	Negative supply voltage	-5.45	-5.2	-4.95	V
V_{CC}–V_{EE}	Difference between positive and negative supply		15.2	15.8	V
R_T	Output termination load resistance	45	50	100	Ω
V_{TT}	Load termination supply voltage	-3.0	-2.0	-2.0	V

DC Electrical Characteristics (Normal Operating Conditions)

V_{CC} = 5V ±3%, V_{EE} = -5.2V ±5%, T_A = 25°C.

Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Units
Differential Analog Inputs V_{IA+}, V_{IA-}, V_{IB+}, V_{IB-}						
V_{IA+}, V_{IA-} V_{IB+}, V_{IB-}	Absolute Input Voltage (Input Common Mode Range)		-4.0		+3.0	V
V_{IAD} , V_{IBD}	Differential Input Range	$\lvert V_{IX+} - V_{IX-} \rvert$			±7.0	V
V_O	Input Voltage Offset			±3	±7.0	mV
TCV_O	Input Voltage Offset Drift			±33		µV/°C
I_{IX+}, I_{IX-}	Input Bias Current	-3.0V to +3.0V		±5.0	±15	µA
$I_{BOFFSET}$	Input Bias Current Offset	Enabled Mode, -3.0V to +3.0V		5.0	12	µA
V_{IA+}, V_{IA-} V_{IB+}, V_{IB-}	Analog Input Capacitance			1.0	2.0	pF
Z_I	Input Impedance			500		KΩ
CMRR	Common Mode Rejection Ratio	-3V to +3V	60	75		dB

DC Electrical Characteristics (continued)

Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Units
Digital Inputs (Latch & Disable)						
V_{IA+}, V_{IA-}	Absolute Input Voltage		-2.0		+5.0	V
V_{ID}	Differential Range	$\lvert V_{ID+} - V_{ID-} \rvert$	0.4	ECL	+5.0	V
I_D	Digital Input Current			20	35	µA
Digital Outputs						
V_{OH}	Output Voltage High		-1.05			V
V_{OL}	Output Voltage Low				-1.55	V
Power Supply						
I_{CC}	Positive Supply Current			24	28	mA
I_{EE}	Negative Supply Current			44	50	mA
PSRR	Power Supply Rejection Ratio	V_{CC} ±2.5%, V_{EE} ±2.5%	60	80		dB
P_D	Power Dissipation	V_{CC} = 5.0V, V_{EE} = -5.2V		360	400	mW

DC Electrical Characteristics (High Supply Voltage Conditions)

V_{CC} = 10V ±3%, V_{EE} = -5.2V ±5%, T_A = 25°C.

Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Units
Differential Analog Inputs V_{IA+}, V_{IA-}, V_{IB+}, V_{IB-}						
V_{IA+}, V_{IA-} V_{IB+}, V_{IB-}	Absolute Input Voltage (Input Common Mode Range)		-4.0		+8.0	V
V_{IAD}, V_{IBD}	Differential Input Range	$\lvert V_{IX+} - V_{IX-} \rvert$			12	V
V_O	Input Voltage Offset			±5.0		mV
TCV_O	Input Voltage Offset Drift			±33		µV/°C
I_{IX+}, I_{IX-}	Input Bias Current	-2.0V to +7.0V		±7.0	±20	µA
$I_{BOFFSET}$	Input Bias Current Offset	-2.0V to +7.0V		7.0		µA
V_{IA+}, V_{IA-} V_{IB+}, V_{IB-}	Analog Input Capacitance			1.0	2.0	pF
Z_I	Input Impedance			500		K
CMRR	Common Mode Rejection Ratio	-3.0V to +7.0V		70		dB
Digital Inputs (Latch & Disable)						
V_{IA+}, V_{IA-}	Absolute Input Voltage		-2.0		+5.0	V
V_{ID}	Differential Range	$\lvert V_{ID+} - V_{ID-} \rvert$	0.4	ECL	+5.0	V
I_D	Digital Input Current			20	35	µA
Digital Outputs						
V_{OH}	Output Voltage High		-1.05			V
V_{OL}	Output Voltage Low				-1.55	V
Power Supply						
I_{CC}	Positive Supply Current			30	35	mA
I_{EE}	Negative Supply Current			55	65	mA
PSRR	Power Supply Rejection Ratio	V_{CC} ±2.5%, V_{EE} ±2.5%		75		dB
P_D	Power Dissipation	V_{CC} = 10V, V_{EE} = -5.2V		586	700	mW

AC Electrical Characteristics

V_{CC} = +10.0V ±3%, V_{EE} = -5.2V ±5%, T_A = 25°C.

Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Units
t_{PD}	Propagation Delay H to L and L to H			1.8	2.2	ns
t_S	Delay Slew Between A and B Sides			100	200	ps
t_D	Delay Dispersion	(0.2 V/ns ≤ Input slew rate ≤ 2.0 V/ns) ECL: V_{TH} = -1V, +0.2V overdrive; V_{TL} = -1.6V, -0.2V underdrive rising and falling edges TTL: V_{TH} = +2.5V, +0.5V overdrive; VTL = 0.5V; -0.5V underdrive rising and falling edges		±150 ±150		ps ps
Δt_{PDTC}	Prop. Delay Temp. Drift			4		ps/°C
Δt_{PDTC}	Delta Prop. Delay with Duty Cycle	0.01% and 99.99% duty cycle 50 kHz, V_{Ip-p} = 5V, V_{TH} = 2.5V (10 ns between measurements)		50		ps
tPW_{min}	Minimum Pulse Width	0 ≤ V_S ≤ 3V; V_{THA} = 2.8V, V_{THB} = 0.2V; t_{IS} = 2.5 V/ns, $\lvert V_{OH} - V_{OL} \rvert \geq 600\ mV_{p-p}$		1.0		ns
t_S	Data to latch enable set up time			1.0		ns
t_H	Latch enable to data in hold time			0.5		ns
t_{IPD}	Latch enable to output high or low			1.5		ns
t_{ID}	Active to Inhibit			5.0		ns
t_{IE}	Inhibit to Active			10.0		ns

Notes:

Notes:

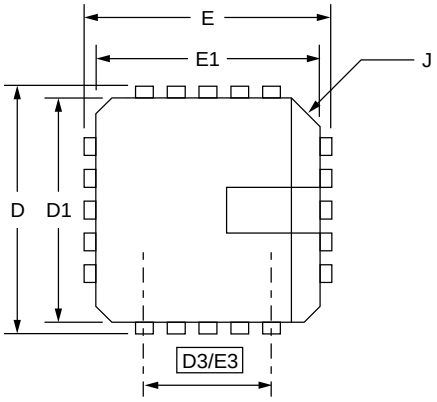
Notes:

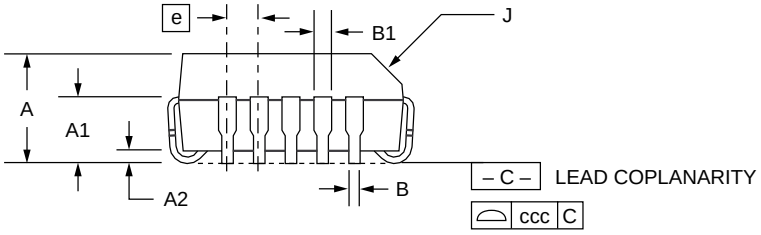
20 Lead Plastic Leaded Chip Carrier (PLCC)

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.180	4.19	4.57	
A1	.090	.120	2.29	3.05	
A2	.020	—	.51	—	
B	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D/E	.385	.395	9.78	10.03	
D1/E1	.350	.356	8.89	9.04	3
D3/E3	.200 BSC		5.08 BSC		
e	.050 BSC		1.27 BSC		
J	.042	.048	1.07	1.22	2
ND/NE	5		5		
N	20		20		
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Corner and edge chamfer (J) = 45°.
3. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is .245" (.101mm).



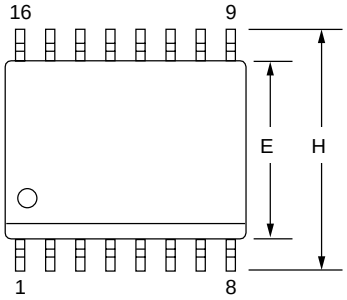


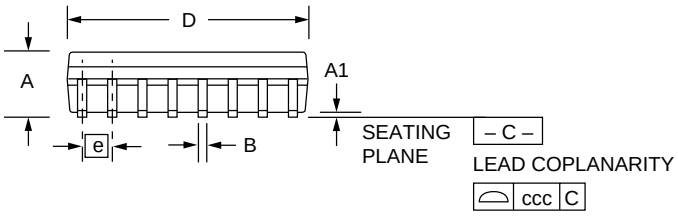
16 Lead Small Outline IC (SOIC) – .300" Body Width

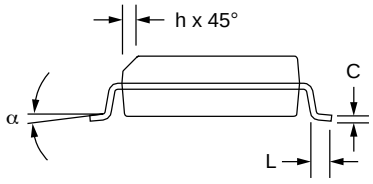
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.398	.413	10.10	10.50	2
E	.291	.299	7.40	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.020	0.25	0.51	
L	.016	.050	0.40	1.27	3
N	16		16		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.





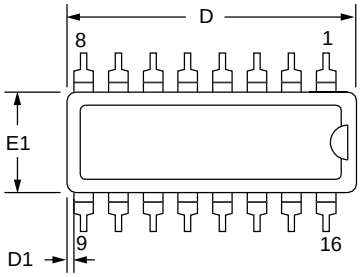


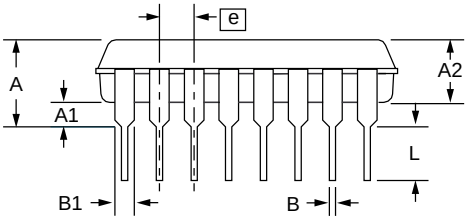
16 Lead Plastic Dual Inline Package (PDIP) – .300" Body Width

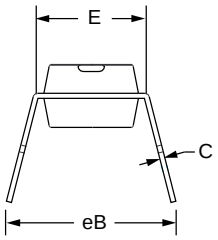
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	.745	.840	18.92	21.33	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.160	2.92	4.06	
N	16		16		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are shown for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.







Ordering Information

Part Number	Package	Operating Temperature Range
RC73687NE	16-lead SOIC	0°C to +70°C
RC73687QC	20-lead PLCC	0°C to +70°C
RC73687MK	16-lead PDIP	0°C to +70°C

RC7B00

Low Skew Buffers

100MHz SDRAM Clock Buffers

Features

- 18 Skew Controlled Output
- Supports up to four SDRAM DIMMs
- Skew between any two outputs is less than 250 pS
- I2C Serial Interface for Programming options
- Multiple Power and Ground Pins for Noise Reduction
- Single 3.3V Power Supply
- 48 Pin SSOP package

Applications

- SDRAM Clock Buffers for Intel's 440BX chip set

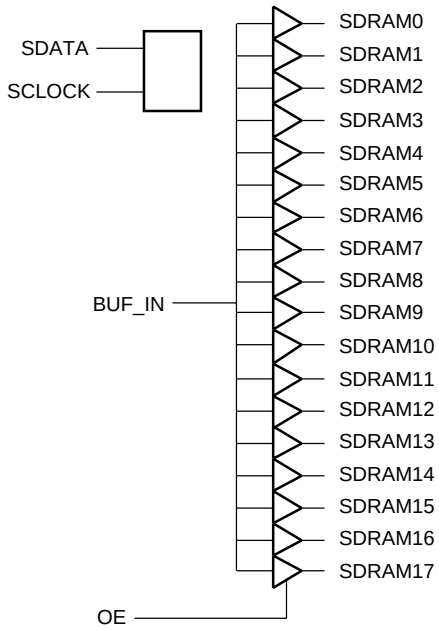
Description

The RC7B00 is a low voltage eighteen output clock buffer which supports 4 DIMMs. The skew between any two outputs is less than 250 pS and the Buffers can be enabled or disabled by programming via the I^2C serial interface. The SDATA and SCLK serial inputs both have internal pull-up resistors.

An Output Enable (OE) pin is also provided so that all the outputs can be tri-stated when held low. This pin is normally high and has an internal pull-up resistor.

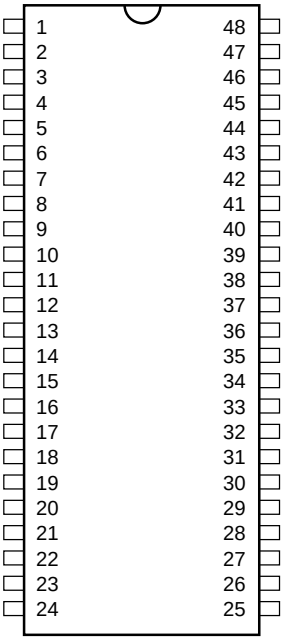
OE	SDRAM0:3	SDRAM4:7	SDRAM8:11	SDRAM12:15	SDRAM16:17
0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
1	BUF_IN	BUF_IN	BUF_IN	BUF_IN	BUF_IN

Block Diagram



Advanced Information

Pin Assignments



48 Pin SSOP

Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name
1	NC	13	SDRAM4	25	SCLOCK	37	VDD
2	NC	14	SDRAM5	26	VSS	38	OE
3	VDD	15	VSS	27	VSS	39	VSS
4	SDRAM0	16	VDD	28	SDRAM17	40	SDRAM12
5	SDRAM1	17	SDRAM6	29	VDD	41	SDRAM13
6	VSS	18	SDRAM7	30	VSS	42	VDD
7	VDD	19	VSS	31	SDRAM8	43	VSS
8	SDRAM2	20	VDD	32	SDRAM9	44	SDRAM14
9	SDRAM3	21	SDRAM16	33	VDD	45	SDRAM15
10	VSS	22	VSS	34	VSS	46	VDD
11	BUF_IN	23	VDD	35	SDRAM10	47	NC
12	VDD	24	SDATA	36	SDRAM11	48	NC

Pin Descriptions

Pin Name	Pin Number	Type	Pin Function Description
BUF_IN	11	IN	Input for clock buffers
SDRAM0:3	4, 5, 8, 9	OUT	SDRAM Byte 0 clock outputs
SDRAM4:7	13, 14, 17, 18	OUT	SDRAM Byte 1 clock outputs
SDRAM8:11	31, 32, 35, 36	OUT	SDRAM Byte 2 clock outputs
SDRAM12:15	40, 41, 44, 45	OUT	SDRAM Byte 3 clock outputs
SDRAM16:17	21, 28	OUT	SDRAM clock outputs
OE	38	IN	Output enable which will tri-state all the outputs when held low
SDATA	24	I/O	Serial Data input
SCLOCK	25	IN	Serial Clock input
VDD	3, 7, 12, 16, 20, 29, 33, 37, 42, 46	Power	Power supply at 3.3V for SDRAM buffers
VDD	23	Power	Power supply at 3.3V for I^2C circuit
VSS	6, 10, 15, 19, 22, 27, 30, 34, 39, 43	Power	Ground for SDRAM buffers
VSS	26	Power	Ground for I^2C circuit
NC	1, 2, 47, 48	NC	No Connections.

Advanced Information

Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Units
Supply Voltage, V_{DD}	-0.5		7	V
Input Voltage	-0.5		V_{DD}+0.5	V
Output Applied Voltage	-0.5		V_{DD}+0.5	V
Junction Temperature			140	°C
Storage Temperature	-65		150	°C
Lead Soldering (10 seconds)			300	°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current, flowing into the device.

Operating Conditions

Parameter	Min.	Typ.	Max.	Units
V_{DD}	3.135	3.3	3.465	V
Ambient Temperature	0		70	°C

Electrical Characteristics T_A = 0°C to 70°C, V_{DD} = 3.3V+5%

Parameter	Min.	Typ.	Max.	Units
V_{IL}, Input low voltage	V_{SS}-0.3		0.8	V
V_{IH}, Input high voltage	2.0		V_{DD}+0.5	V
I_{IL}, Input low current (BUF_IN)	-5			µA
I_{IH}, Input high current (BUF_IN)			5	µA
I_{IL}, Input low current (OE, SDATA, SCLOCK)	-50			µA
I_{IH}, Input high current (OE, SDATA, SCLOCK)			5	µA
V_{OL}, Output low voltage @ I_{OL} = 23mA			0.4	V
V_{OH}, Output high voltage @ I_{OH} = -30mA	2.6			V
I_{OL}, Output low current @ V_{OL} = 0.8V	40			mA
I_{OH}, Output high current @ V_{OH} = 2.0V			-54	mA
I_{DD}, Supply current @ f = 100MHz				mA
I_{DD}, Supply current @ f = 66MHz				mA
I_{DD}, Supply current @ OE = 0				mA
C_{IN}, Input capacitance			5	pF
F_{IN}, Input frequency			150	MHz

Advanced Information

Switching Characteristics

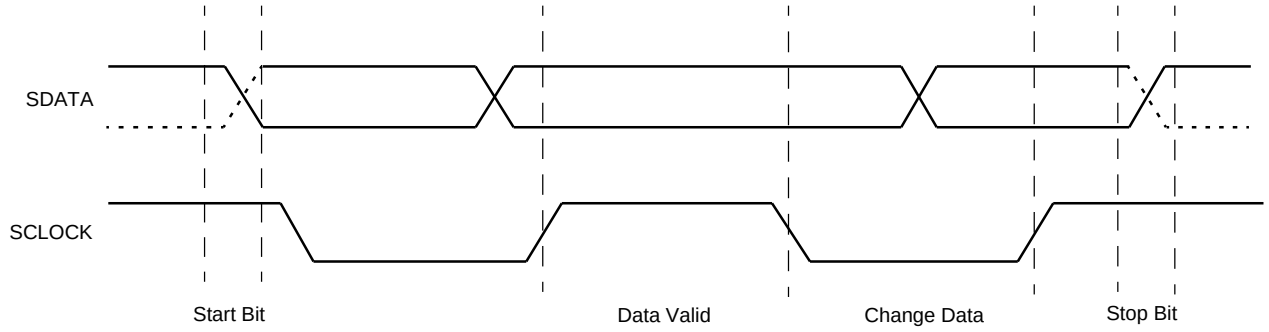
Parameter	Conditions	Min.	Typ.	Max.	Units
T_{PD}, Propagation delay	V_T = 1.5V	1		5	ns
T_R, Rise time	0.4 to 2.4V	0.5		1.5	ns
T_F, Fall time	2.4 to 0.4V	0.5		1.5	ns
T_D, Duty cycle	V_T = 1.5V	45		55	%
T_{EN}, Output enable time	V_T = 1.5V	1		8	ns
T_{DIS}, Output disable time	V_T = 1.5V	1		8	ns
T_{SK}, Skew	V_T = 1.5V			250	ps
Z_O, Output impedance			15		Ω

Serial Data Interface

Signaling Requirements for the I²C Serial Port

To initiate communications with the serial port, a start bit is invoked. The start bit is defined as the SDATA line is brought low while the SCLOCK is held high. Once the start bit is initiated, valid data can then be sent. Data is considered to be valid when the clock goes to and remains in the high state.

The data can change when the clock goes low. To terminate the transmission, a stop bit is invoked. The stop bit occurs when the SDATA line goes from a low to a high state while the SCLOCK is held high. See Figure below.



The data transfer rate is 100kbits/s in the standard mode and 400kbits/s in the fast mode. The serial protocol uses block writes only. Bytes are written with the lowest first and the highest last with the ability to stop after any complete byte has been transferred. The clock driver is a slave/receiver only and is only capable of receiving data with the exception of sending acknowledgements. It is not capable of sending data.

Byte writing sequence

The buffer is accessed when the slave address byte is received. Each byte of data is followed by an acknowledge bit. The address bit sequence is 1 1 0 1 0 0 1 followed by the R/W# bit (0). Bits are written with the Most Significant Bit (MSB) first. The MSB Bit is bit 7 and the LSB is bit 0. The Byte writing sequence is as shown in the table below.

Byte Sequence	Byte name	Bit sequence 7	6	5	4	3	2	1	0
1	Slave address	1	1	0	1	0	0	1	0
2	Command Code	X	X	X	X	X	X	X	X
3	Byte Count	X	X	X	X	X	X	X	X
4	Data Byte 0	see table below							
5	Data Byte 1	see table below							
6	Data Byte 2	see table below							
7	Data Byte 3	X	X	X	X	X	X	X	X
8	Data Byte 4	X	X	X	X	X	X	X	X
9	Data Byte 5	X	X	X	X	X	X	X	X
10	Data Byte 6	X	X	X	X	X	X	X	X

Data Bytes 0 to 2 Map

Bit	Pin	Name	Description
Data Byte0: SDRAM Active/Inactive Register (1 = enable, 0 = disable)			
7	18	SDRAM7	(ACTIVE/INACTIVE)
6	17	SDRAM6	(ACTIVE/INACTIVE)
5	14	SDRAM5	(ACTIVE/INACTIVE)
4	13	SDRAM4	(ACTIVE/INACTIVE)
3	9	SDRAM3	(ACTIVE/INACTIVE)
2	8	SDRAM2	(ACTIVE/INACTIVE)
1	5	SDRAM1	(ACTIVE/INACTIVE)
0	4	SDRAM0	(ACTIVE/INACTIVE)
Data Byte1: SDRAM Active/Inactive Register (1 = enable, 0 = disable)			
7	45	SDRAM15	(ACTIVE/INACTIVE)
6	44	SDRAM14	(ACTIVE/INACTIVE)
5	41	SDRAM13	(ACTIVE/INACTIVE)
4	40	SDRAM12	(ACTIVE/INACTIVE)
3	36	SDRAM11	(ACTIVE/INACTIVE)
2	35	SDRAM10	(ACTIVE/INACTIVE)
1	32	SDRAM9	(ACTIVE/INACTIVE)
0	31	SDRAM8	(ACTIVE/INACTIVE)
Data Byte 2: SDRAM Active/Inactive Register (1 = enable, 0=disable)			
7	28	SDRAM17	(ACTIVE/INACTIVE)
6	21	SDRAM16	(ACTIVE/INACTIVE)
5		reserved	reserved
4		reserved	reserved
3		reserved	reserved
2		reserved	reserved
1		reserved	reserved
0		reserved	reserved

Advanced Information

Notes:

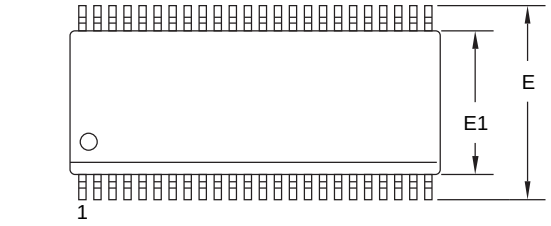
Mechanical Dimensions

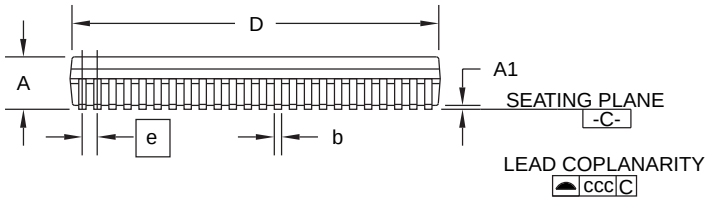
48 pin SSOP

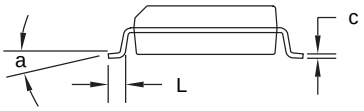
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.095	.110	2.41	2.79	
A1	.008	.016	0.20	0.41	
b	.008	.0135	0.20	0.34	5
c	.005	.010	0.13	0.25	5
D	.620	.630	15.75	16.00	2, 4
E	.395	.420	10.03	10.67	
E1	.291	.299	7.39	7.59	2
e	.025 BSC		0.64 BSC		
L	.020	.040	0.51	1.02	3
N	48		48		6
a	0°	8°	0°	8°	
ccc	---	.004	---	0.13	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
2. "D" and "E1" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "b" & "c" dimensions include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Advanced Information

Ordering Information

Product Number	Temperature	Screening	Package	Package Marking
RC7B00	0°C to 70°C		48 SSOP	RC7B00

Advanced Information

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RCB001

Voltage Regulator Module (VRM) for Pentium® Pro Processors

Features

- Programmable 2.0V to 3.5V output from 5V supply
- Maximum output current 12.4A
- Typical Efficiency > 84%
- Total output accuracy typically ±3%
- Short circuit protection
- Power Good output
- Output Enable function
- Excellent transient response
- Meets Intel Pentium Pro VRM specifications

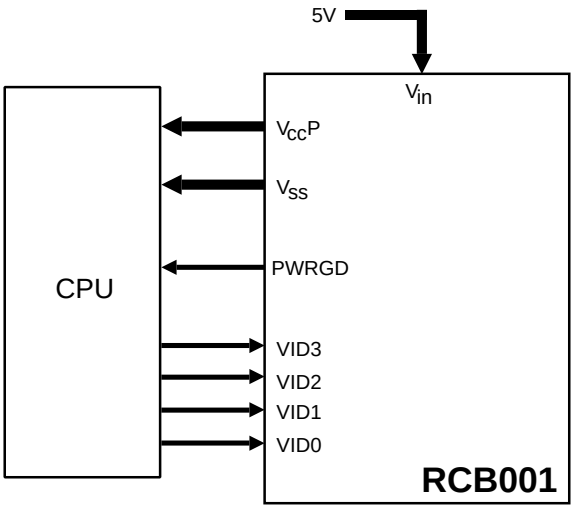
Applications

- Pentium Pro motherboard VRM module
- Programmable power supply module
- Template for motherboard implementation

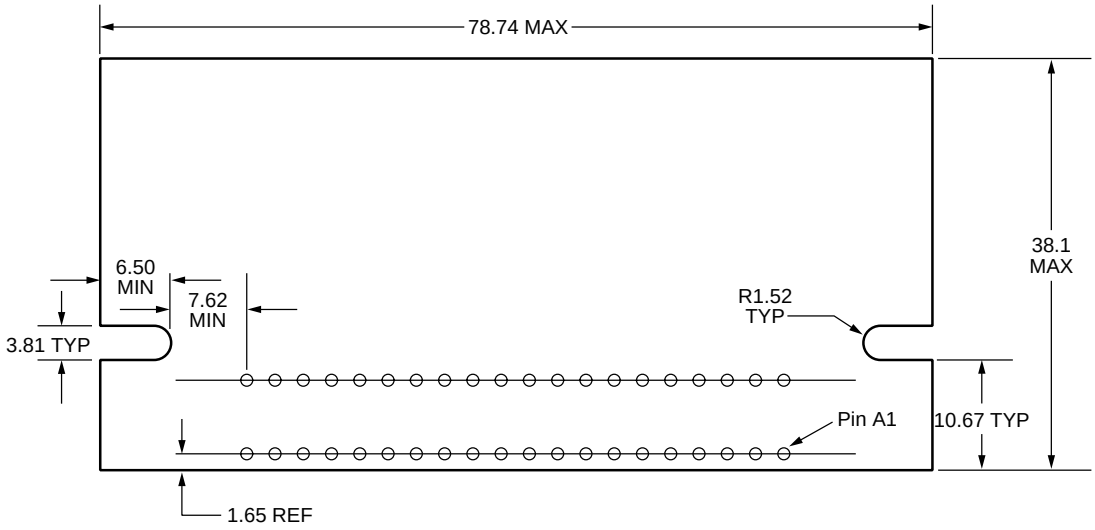
Description

The RCB001 VRM module is a programmable DC-DC voltage regulator module designed to deliver the selectable processor core voltage required by the Pentium Pro microprocessor family. This VRM module provides the flexibility to board designers to support the entire Pentium Pro processor family with a single motherboard design. The RCB001 design takes full advantage of a proprietary Fairchild programmable DC-DC voltage controller IC which integrates the DAC function as well as the Power Good and Output Enable features. The result is a voltage regulator module that uses a minimum number of external components to achieve high reliability at a competitive cost. The RCB001 provides an extremely well regulated voltage selectable from 2.0V to 3.5V. Voltage selection is accomplished through a 4 bit digital input (VID0 - VID3) and can be incremented in 100mV steps. The Power Good open collector output provides a logic LOW state when an out-of-tolerance voltage is detected at the VRM output. Other features include high efficiency, short circuit protection, output enable and low package weight. The RCB001 VRM module is designed as a point-of-load converter for the Pentium Pro processor, thus minimizing the distribution losses normally occuring when drawing high currents from a centralized power supply.

Block Diagram



Mechanical Dimensions (mm):



Pin Orientation
(Top View)

(socket: AMPMOD2 532956-7 or equivalent)

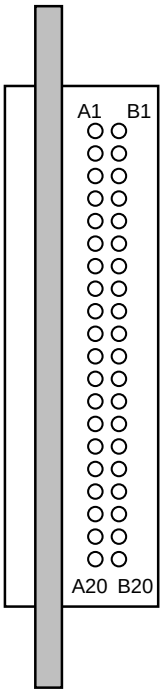


Table 1. VRM Pin Definitions

Pin#	Row A	Row B
1	$5V_{IN}$	$5V_{IN}$
2	$5V_{IN}$	$5V_{IN}$
3	$5V_{IN}$	$5V_{IN}$
4	NC[1]	NC[1]
5	NC[1]	NC[1]
6	NC[1]	OUTEN[2]
7	VID0	VID1
8	VID2	VID3
9	NC[1]	PWRGD
10	$V_{CC}P$	V_{SS}
11	V_{SS}	$V_{CC}P$
12	$V_{CC}P$	V_{SS}
13	V_{SS}	$V_{CC}P$
14	$V_{CC}P$	V_{SS}
15	V_{SS}	$V_{CC}P$
16	$V_{CC}P$	V_{SS}
17	V_{SS}	$V_{CC}P$
18	$V_{CC}P$	V_{SS}
19	V_{SS}	$V_{CC}P$
20	$V_{CC}P$	V_{SS}

Notes:
1. Not used on module; no current is drawn.
2. This pin is not used on the RCB001-12A.

VRM Connector Pin Reference

Pin Name	Input/Output	Function
Power-Good (PWRGD) (Open collector TTL output)	O	PWRGD = High, output voltage within specifications PWRGD = Low, output voltage not within specifications (nominal or selected voltage ±10%) The PWRGD signal will change to the proper state within 5ms of the output coming into or going out of its specified range.
Output Enable (OUTEN)[1] (Open collector TTL input)	I	OUTEN = Floating or high, output enabled OUTEN = Low, output disabled and PWRGD = Low
Voltage Identification (VID0 to VID3) (Open collector TTL input)	I	These four signals are used to indicate the voltage required by the processor. See Table 2.
5 V_{IN}	I	Module supply voltage.
$V_{CC}P$	O	Processor core V_{CC}
V_{SS}	I, O	Ground reference voltage.

Note:

1. This pin is not used on the RCB001-12A.

Electrical Specifications

(V_{IN} = +5V, T_A = 0 to 70°C unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Units
Input Specifications					
Input Voltage, V_{IN}		4.75	5	5.25	V
Output Specifications					
Output Voltage ($V_{CC}P$) Range	Intel VID code, Table 2	2.0		3.5	V
DC Output Current, I_{OUT}	RCB001-12 and RCB001-12A	0.5		12.4	A
Set Point Accuracy[1]	I_{LOAD} = 5.25A, T_A = 25°C		±0.8	±1.5	%
DC Load Regulation	I_{LOAD} = 0.5A to 12.4A		0.8	±1.5	%
Line Regulation	4.75 ≤ V_{IN} ≤ 5.25		0.1	±0.2	%
Output Ripple and Noise	I_{LOAD} = 10A, BW = 20MHz		30		mVpp
Output Temperature Drift			+20		ppm/°C
Load Transient	I_{LOAD} = 0.5A to 10A, 30A/µSec VID code 0010 ($V_{CC}P$ =3.3V)		100	120	mV
Cumulative Accuracy	All Conditions, see Note 2		±3	±5	%
Efficiency	I_{LOAD} = 0.5A	40	67		%
	I_{LOAD} = 10A	80	84		%
General Specifications					
Switching Frequency			650		kHz
Short Circuit Protection			16		A

Notes:

1. Set Point Accuracy is defined as the static accuracy of the output voltage at 5.25A @ T_A = 25°C.
2. Cumulative Accuracy includes Setpoint Accuracy, Output Temperature Drift, Line and Load Regulation, Output Ripple/Noise and Load Transient Response.

Table 2. Voltage Identification (VID) and Overall Regulation[1]

Pentium Pro Processor Pins				Output ($V_{CC}P$)		
VID3	VID2	VID1	VID0	Min.	Nominal	Max.
1	1	1	1	1.900 V	2.0V	2.100V
1	1	1	0	1.995V	2.1V	2.205V
1	1	0	1	2.090V	2.2V	2.310V
1	1	0	0	2.185V	2.3V	2.415V
1	0	1	1	2.280V	2.4V	2.520V
1	0	1	0	2.375V	2.5V	2.625V
1	0	0	1	2.470V	2.6V	2.730V
1	0	0	0	2.565V	2.7V	2.835V
0	1	1	1	2.660V	2.8V	2.940V
0	1	1	0	2.755V	2.9V	3.045V
0	1	0	1	2.850V	3.0V	3.150V
0	1	0	0	2.945V	3.1V	3.255V
0	0	1	1	3.040V	3.2V	3.360V
0	0	1	0	3.135V	3.3V	3.465V
0	0	0	1	3.230V	3.4V	3.570V
0	0	0	0	3.325V	3.5V	3.675V

0 = Processor pin connected to V_{SS}

1 = Processor pin open

Note:

1. Includes set point accuracy, load transient, ripple and noise, thermal drift, load regulation and line regulation.

Ordering Information

Part Number[1]	Input	Maximum DC Output Current	Comments
RCB001-12	5V	12.4A	
RCB001-12A	5V	12.4A	No Output Enable

Note:

1. Please refer to our Application Note 42 (AP-42) for more information on the board level voltage regulator design using Fairchild's DC-DC voltage controllers (RC5040 and RC5042).

RCB002

Voltage Regulator Module (VRM) for Pentium® P55C and K6™ Processors

Features

- Fixed 2.8V, 2.9V or 3.2V output from 5V supply
- Maximum output current 7.5A for RCB002-8
- Maximum output current 10A for RCB002-10
- Typical efficiencies > 80%
- Short circuit protection
- Power Good output
- Excellent transient response
- Meets Intel's Pentium P55C and AMD's K6 power specifications

Applications

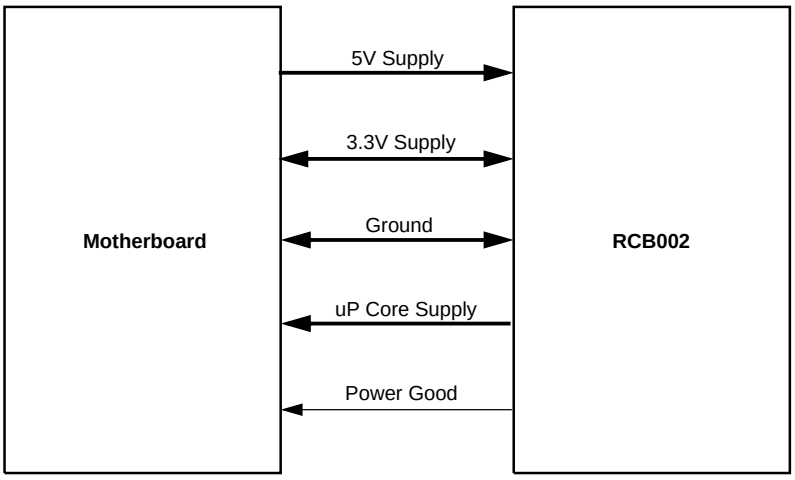
- Pentium and K6 motherboard 30-pin VRM module
- Add-in power supply upgrade for P55C and K6 CPUs
- Flexible motherboard designs

Description

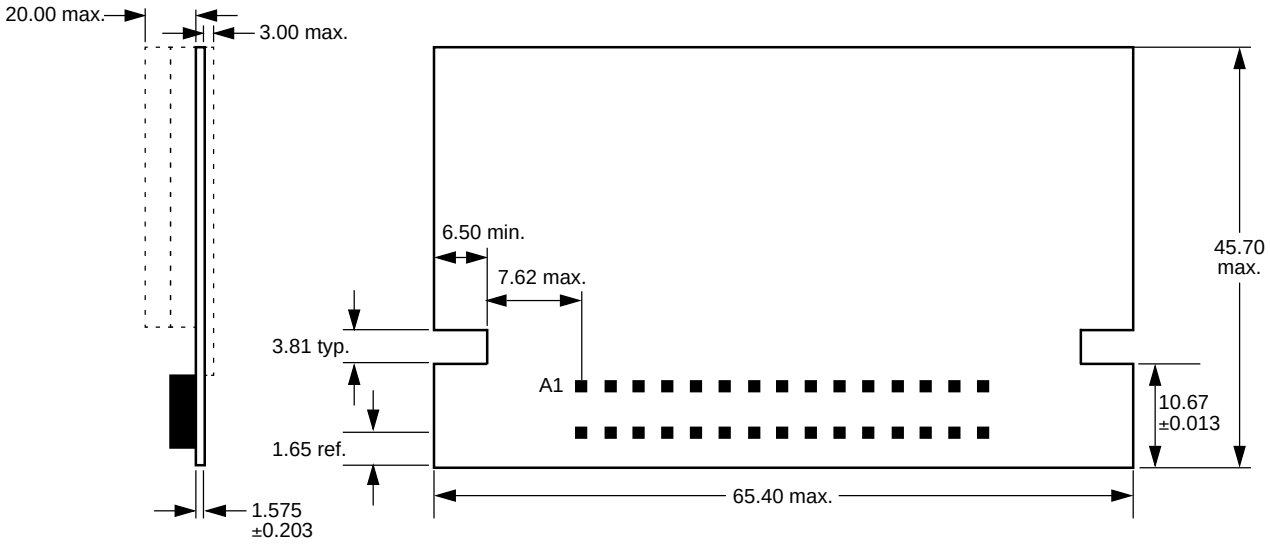
The RCB002 VRM module is a DC-DC voltage regulator module designed to deliver the processor core voltage required by the P55C and K6 microprocessors. It offers board designers the flexibility to support the P55C and K6 processors with a modular add-in power supply. The RCB002 uses a proprietary Fairchild programmable DC-DC controller IC to deliver a precise output voltage to the CPU core without the need for external precision resistors. The result is a voltage regulator module with a minimum number of components to achieve high reliability at a competitive cost.

The RCB002-8 can deliver 2.8V or 2.9V (factory preset) of extremely well regulated voltage at 6A of continuous current. This voltage can be used to address the P55C and the 166/200MHz K6. The RCB002-10 delivers 3.2V at 10A for the 233MHz K6. In addition, the Power Good open collector outputs a logic LOW when an out-of-tolerance voltage is detected at the VRM output. Other features include high efficiency, short circuit protection, and low package weight.

Block Diagram



Mechanical Dimensions (mm) – Viewed from connector side



Pin Orientation – Top View
(Socket: AMPMOD2 532956-5 or equivalent)

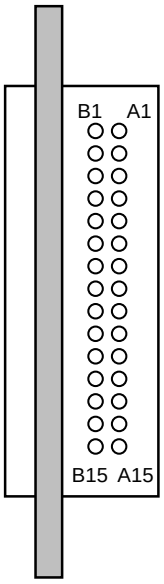


Table 1. VRM Connector Pin Definitions

Pin #	Row A	Row B
1	GND	GND
2	GND	GND
3	V12[1]	$V_{I/O}$[1]
4	$V_{I/O}$[1]	$V_{I/O}$[1]
5	V3[1]	V3[1]
6	V3[1]	V3[1]
7	V_{CORE}	V_{CORE}
8	V_{CORE}	V_{CORE}
9	GND	V_{CORE}
10	V_{CORE}	V_{CORE}
11	PWRGD	UPVRM#[1]
12	SENSE[1]	DISABLE[1]
13	GND	GND
14	V5	V5
15	V5	V5

Note:
1. Not used by VRM module

VRM Connector Pin Reference

Pin Description	Input/ Output	Function
V5	I	+5V supply voltage to support power to the CPU core.
V3	I	+3.3V supply to support power to the CPU I/O. These pins are connected directly to the $V_{I/O}$ pins so the 3.3V supply can be routed through the module header.
PWRGD (Power Good) for Pentium Open collector TTL output	O	If PWRGD = HIGH, the output voltage is within specifications. If PWRGD = LOW, the output voltage not within ±10% of nominal. The PWRGD output will change to the proper state within 5ms of the output coming into or going out of its specified range.
V_{CORE}	O	Processor core VCC.
$V_{I/O}$	O	CPU I/O VCC. These pins are connected to the +3.3V input pins.
GND	I,O	Ground Reference.

Electrical Specifications

(V_{IN} = +5V, T_A = 25°C unless otherwise specified.)

Parameter	Test Conditions	Min.	Typ.	Max.	Units
Input Specifications					
Controller supply voltage, V_{IN}		4.75	5	5.25	V
Output Specifications (RCB002-8)					
Output Voltage, V_{CORE}			2.8 2.9		V V
Output Current, I_{CORE}			6	8.0	A
Load Transient[1]	I_{CORE} = 0.5A to 7.5A, 20A/µs		±40	±100	mV
Load Regulation	I_{CORE} = 0.5A to 7.5A		±0.8		%
Efficiency	I_{CORE} = 6A		83		%
Short Circuit Protection			10		A
Output Specifications (RCB002-10)					
Output Voltage, V_{CORE}			3.2		V
Output Current, I_{CORE}			8.5	10	A
Load Transient	I_{CORE} = 0.5A to 10A, 20A/µs		±50	±100	mV
Load Regulation	I_{CORE} = 0.5A to 10A		±1.0		%
Efficiency	I_{CORE} = 8A		80		%
Short Circuit Protection			13		A
General Specifications					
Set Point Accuracy[2]	I_{CORE} = 3A	‘	±1.0		%
Line Regulation	V_{IN} = 5.0V ± 0.25V		±0.1		%
Output Temperature Drift	T_A = 0 to 60°C		20		ppm/°C
Switching Frequency			300		kHz
Cumulative Accuracy[3]			±50	±100	mV

Notes:

1. Refer to Intel’s AP-580 for bulk capacitance decoupling recommendations. Four 100 µF Tantalum capacitors with 25mΩ ESR are recommended for optimum transient response.
2. Set Point Accurcy is defined as the static accuracy of the output voltage at 3A and T_A = 25°C.
3. Cumulative Accuracy includes Set Point Accuracy, Output Temperature Drift, Line and Load Regulation, and Output Ripple/Noise.

Ordering Information

Part Number	Output Current	Output Voltage	Input
RCB002-8/2.8	8A	2.8V	5V DC
RCB002-8/2.9	8A	2.9V	5V DC
RCB002-10	10A	3.2V	5V DC

RCB004

Voltage Regulator Module (VRM) for Pentium® Pro and Pentium II Processors

Features

- Programmable 1.3V to 3.5V output from 5V supply using 5-bit digital input
- Maximum output current 13A
- Typical efficiency > 83%
- Output initial setpoint tolerance typically ±1%
- Short circuit protection with current foldback
- Power Good output
- Output Enable function
- Excellent transient response
- Meets Intel Pentium II VRM 8.1 specification

Applications

- Motherboard VRM module
- Programmable power supply module
- Template for motherboard implementation

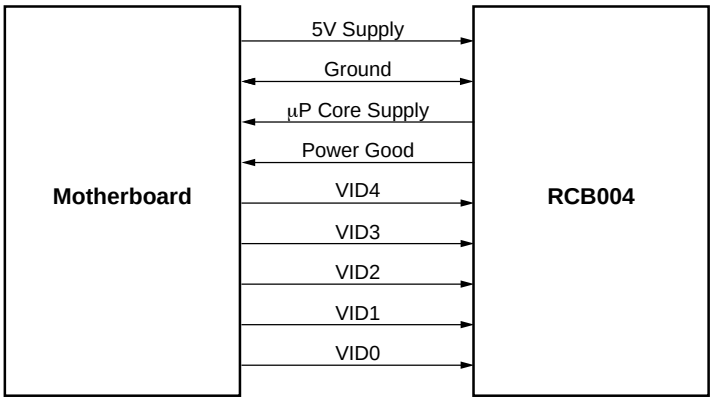
Description

The RCB004 is a non-synchronous programmable DC-DC VRM designed to deliver the selectable processor core voltage required by Pentium Pro and Pentium II microprocessors. This VRM offers the flexibility to support both the Pentium Pro and Pentium II processors with a single motherboard design. The RCB004 takes full advantage of a proprietary Fairchild Electronics programmable DC-DC controller IC that integrates the 5-bit DAC function, and Power Good and Output Enable features. The result is a VRM with a minimum number of components that achieves high reliability at a competitive cost. The synchronous counterpart to the RCB004, the RCB005, offers higher efficiency, which can be significant in the lower output range.

The RCB004 provides an extremely well regulated selectable output voltage from 1.3V to 3.5V. Voltage selection is accomplished throught a 5-bit digital input (VID0 to VID4). The Power Good open collector outputs a logic LOW when an out-of-tolerance voltage is detected at the VRM output. Other features include high efficiency, short circuit protection, output enable, and low package weight. The RCB004 VRM module is designed as a point-of-load converter for Pentium Pro and Pentium II processors, minimizing the distribution losses normally occuring when drawing high currents from a centralized power supply.

Preliminary Information

Block Diagram



65-RCB004-01

Pin Orientation - Top View
(Socket: AMPMOD2 532956-7 or equivalent)

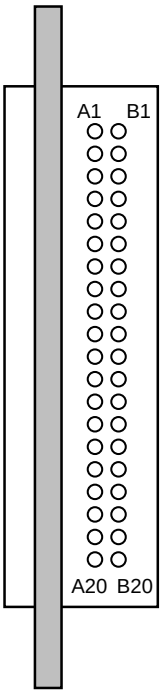


Table 1. RCB004 Pin Definitions

Pin #	Row A	Row B
1	5Vin	5Vin
2	5Vin	5Vin
3	5Vin	5Vin
4	12Vin	12Vin
5	NC[1]	NC[1]
6	NC[1]	OUTEN
7	VID0	VID1
8	VID2	VID3
9	VID4	PWRGD
10	$V_{CC}P$	V_{SS}
11	V_{SS}	$V_{CC}P$
12	$V_{CC}P$	V_{SS}
13	V_{SS}	$V_{CC}P$
14	$V_{CC}P$	V_{SS}
15	V_{SS}	$V_{CC}P$
16	$V_{CC}P$	V_{SS}
17	V_{SS}	$V_{CC}P$
18	$V_{CC}P$	V_{SS}
19	V_{SS}	$V_{CC}P$
20	$V_{CC}P$	V_{SS}

Note:
1. Not used on module; no current is drawn.

VRM Connector Pin Reference

Pin Description	Input/ Output	Function
PWRGD (Power Good) Open collector TTL output.	O	If PWRGD = HIGH, output voltage withing specifications. If PWRGD = LOW, output voltage not within ±10% of nominal. The PWRGD output will change to the proper state within 5ms of the output coming into or going out of its specified range.
OUTEN (Output Enable) Open collector TTL input.	I	If OUTEN = HIGH (floating), output enabled. If OUTEN = LOW, output disabled and PWRGD output LOW.
VID0 to VID4 (Voltage ID) Open collector TTL inputs.	I	These five signals are used to indicate the voltage required by the processor. See Table 2.
$5V_{IN}$	I	Primary module supply voltage.
$12V_{IN}$	I	MOSFET bias supply voltage
$V_{CC}P$	O	Processor core VCC.
V_{SS}	I,O	Ground.

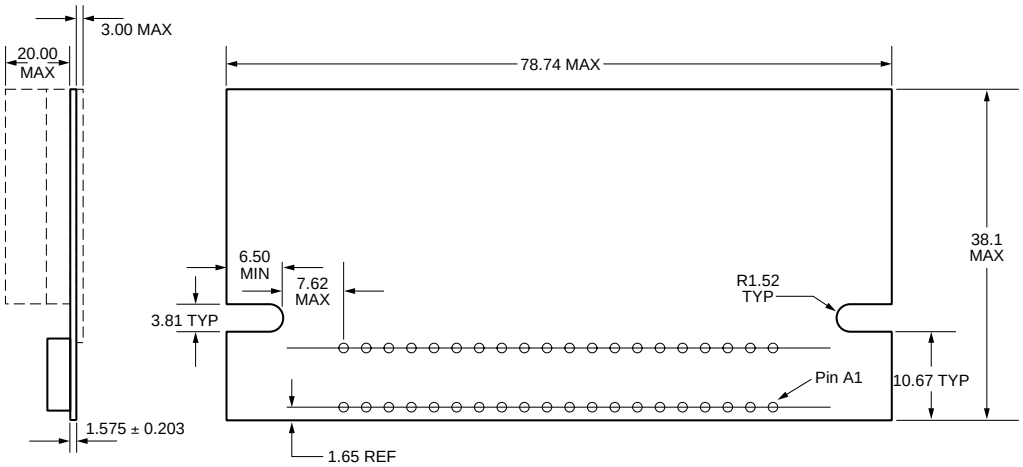
Electrical Specifications (V_{IN} = +5V, T_A = 0°C to 60°C, VID4–VID0 = 10111 ($V_{CC}P$ = 2.8V), 100LFM airflow, unless otherwise specified.)

Parameter	Test Conditions	Min.	Typ.	Max.	Units
Input Specifications					
Primary Module Supply, 5Vin		4.75	5	5.25	V
MOSFET Bias Supply, 12Vin		11.4	12	12.6	V
Output Specifications					
Output Voltage Range, Vcc_{CORE}	See Table 2	1.3		3.5	V
Output Voltage Regulation Steady State[1] Transient[2]	 Vcc_{CORE} = 2.8V Icc_{CORE} = 0.8 to 13.2A, 20A/µs	 2.74 2.66	 2.80 2.80	 2.90 2.94	 V V
Output Voltage Regulation Steady State[1] Transient[2]	 Vcc_{CORE} = 1.8V Icc_{CORE} = 0.8 to 11.7A, 20A/µs	 1.74 1.70	 1.80 1.80	 1.90 1.90	 V V
Output Current, Icc_{CORE}				13.2	A
Initial Voltage Setpoint	Icc_{CORE} = 6A, T_A = 25°C		±20		mV
Load Regulation	Icc_{CORE} = 0.8A to 13.2A		±30		mV
Line Regulation	5Vin = 4.75V to 5.25V		±2		mV
Output Ripple	20MHz BW, Icc_{CORE} = 13.2A		20		mVp-p
Output Temperature Drift			+10		mV
Efficiency	Icc_{CORE} = 0.8A Icc_{CORE} = 13.2A	40 80	67 84		%
Turn-on Response Time				10	ms
General Specifications					
Switching Frequency			300		KHz
Short Circuit Protection			18		A

Notes:

1. Steady State Voltage Regulation includes Initial Voltage Setpoint, DC load regulation, output ripple/noise and temperature drift.
2. The output voltage measured at the converter output will be within the voltage range specified as a result of a load transient occuring at a slew rate of 20A/µs. These specifications assume a minimum of 20 x 0.1µF ceramic capacitors are placed directly next to the CPU in order to provide adequate high-speed decoupling. Additional bulk capacitors may be required directly next to the CPU when using any VRM; see Application Bulletin AB 5 for details.

Mechanical Dimensions (mm)



Preliminary Information

Table 2. Output Voltage vs. Voltage Identification Code

VID4	VID3	VID2	VID1	VID0	Nominal Voltage to CPU ($V_{CC_{CORE}}$)
0	1	1	1	1	1.30V
0	1	1	1	0	1.35V
0	1	1	0	1	1.40V
0	1	1	0	0	1.45V
0	1	0	1	1	1.50V
0	1	0	1	0	1.55V
0	1	0	0	1	1.60V
0	1	0	0	0	1.65V
0	0	1	1	1	1.70V
0	0	1	1	0	1.75V
0	0	1	0	1	1.80V
0	0	1	0	0	1.85V
0	0	0	1	1	1.90V
0	0	0	1	0	1.95V
0	0	0	0	1	2.00V
0	0	0	0	0	2.05V

VID4	VID3	VID2	VID1	VID0	Nominal Voltage to CPU ($V_{CC_{CORE}}$)
1	1	1	1	1	2.0V
1	1	1	1	0	2.1V
1	1	1	0	1	2.2V
1	1	1	0	0	2.3V
1	1	0	1	1	2.4V
1	1	0	1	0	2.5V
1	1	0	0	1	2.6V
1	1	0	0	0	2.7V
1	0	1	1	1	2.8V
1	0	1	1	0	2.9V
1	0	1	0	1	3.0V
1	0	1	0	0	3.1V
1	0	0	1	1	3.2V
1	0	0	1	0	3.3V
1	0	0	0	1	3.4V
1	0	0	0	0	3.5V

Note:

1. "0" indicates processor pin is tied to 0V (V_{SS}), "1" indicates it is tied to 5V or is open.

Ordering Information

Part Number	Input	Output Current
RCB004-12	5V DC	13A

Preliminary Information

RCB005-K

5 Bit Voltage Regulator Module (VRM) for Pentium® II Processors

For 5V Input Voltage

Features

- Programmable 1.3V to 3.5V output
- Output current to 15A
- 5-bit digital input selects output voltage
- Current limiting short-circuit protection
- Power Good output
- Output Enable function
- Excellent transient response
- Meets Intel VRM specifications

Applications

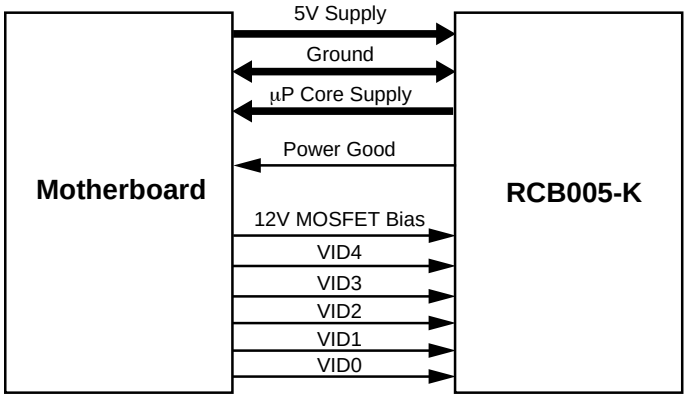
- Pentium II (Klamath type) 233—300MHz VRM

Description

The RCB005-K is a programmable DC-DC VRM designed to deliver the selectable processor core voltage required by Pentium II microprocessors. This VRM converts the +5V power supply voltage to the voltage required by the CPU. The RCB005-K takes full advantage of Fairchild's RC5051 programmable DC-DC controller IC, utilizing synchronous architecture for maximum efficiency. This VRM integrates a 5-bit DAC function, Power Good, and Output Enable features. The result is a VRM with a minimum number of components that achieves high reliability at a competitive cost.

The RCB005-K provides an extremely well regulated selectable output voltage from 1.3V to 3.5V. Voltage selection is accomplished through a 5-bit digital input. The Power Good output provides a logic LOW when an out-of-tolerance voltage is detected at the VRM output. Other features include high efficiency, short-circuit and over-voltage protection, output enable, and low package weight. The RCB005-K VRM module is designed as a point-of-load converter for Pentium II (Klamath type) processors, minimizing the distribution losses normally occurring when drawing high currents from a centralized power supply.

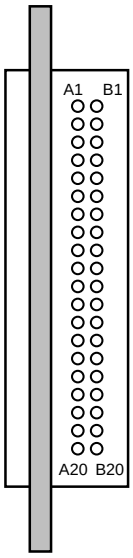
Block Diagram



65-RCB005-1

Pin Orientation — Top View

(Socket: AMPMOD2 532956-7 or equivalent)



65-RCB005-2

Table 1. RCB005-K Pin Definitions

Pin #	Row A	Row B
1	5Vin	5Vin
2	5Vin	5Vin
3	5Vin	5Vin
4	12Vin	12Vin
5	12Vin	NC[1]
6	NC[1]	OUTEN
7	VID0	VID1
8	VID2	VID3
9	VID4	PWRGD
10	$V_{CC_{CORE}}$	Vss
11	Vss	$V_{CC_{CORE}}$
12	$V_{CC_{CORE}}$	Vss
13	Vss	$V_{CC_{CORE}}$
14	$V_{CC_{CORE}}$	Vss
15	Vss	$V_{CC_{CORE}}$
16	$V_{CC_{CORE}}$	Vss
17	Vss	$V_{CC_{CORE}}$
18	$V_{CC_{CORE}}$	Vss
19	Vss	$V_{CC_{CORE}}$
20	$V_{CC_{CORE}}$	Vss

Note:
1. Not used on module; no current is drawn.

VRM Connector Pin Reference

Pin Description	Input/Output	Function
5Vin	I	Primary module supply voltage.
12Vin	I	MOSFET bias supply voltage.
OUTEN (Output Enable) Open collector TTL input.	I	If OUTEN = HIGH (floating), output enabled.If OUTEN = LOW, output disabled and PWRGD output LOW.
VID0 to VID4 (Voltage Identification Code) Open collector TTL inputs.	I	These five signals are used to indicate the voltage required by the processor. See Table 2.
PWRGD (Power Good) Open collector TTL output.	O	If PWRGD = HIGH, output voltage within specifications. If PWRGD = LOW, output voltage not within ±10% of nominal. The PWRGD output will change to the proper state within 5ms of the output coming into or going out of its specified range.
$V_{CC_{CORE}}$	O	Processor core voltage.
Vss	I, O	Ground.

Table 2. Output Voltage vs. Voltage Identification Code

VID4	VID3	VID2	VID1	VID0	Nominal Voltage to CPU (Vcc_{CORE})
0	1	1	1	1	1.30V
0	1	1	1	0	1.35V
0	1	1	0	1	1.40V
0	1	1	0	0	1.45V
0	1	0	1	1	1.50V
0	1	0	1	0	1.55V
0	1	0	0	1	1.60V
0	1	0	0	0	1.65V
0	0	1	1	1	1.70V
0	0	1	1	0	1.75V
0	0	1	0	1	1.80V
0	0	1	0	0	1.85V
0	0	0	1	1	1.90V
0	0	0	1	0	1.95V
0	0	0	0	1	2.00V
0	0	0	0	0	2.05V

VID4	VID3	VID2	VID1	VID0	Nominal Voltage to CPU (Vcc_{CORE})
1	1	1	1	1	2.0V
1	1	1	1	0	2.1V
1	1	1	0	1	2.2V
1	1	1	0	0	2.3V
1	1	0	1	1	2.4V
1	1	0	1	0	2.5V
1	1	0	0	1	2.6V
1	1	0	0	0	2.7V
1	0	1	1	1	2.8V
1	0	1	1	0	2.9V
1	0	1	0	1	3.0V
1	0	1	0	0	3.1V
1	0	0	1	1	3.2V
1	0	0	1	0	3.3V
1	0	0	0	1	3.4V
1	0	0	0	0	3.5V

Note:

1. "0" indicates processor pin is tied to 0V (V_{SS})
   "1" indicates it is tied to 5V or is open.

Electrical Specifications

5Vin = +5V, 12Vin = +12V, T_A = 0°C to 60°C, Vcc_{CORE} = 2.8V, and airflow of 100LFM, unless otherwise specified.

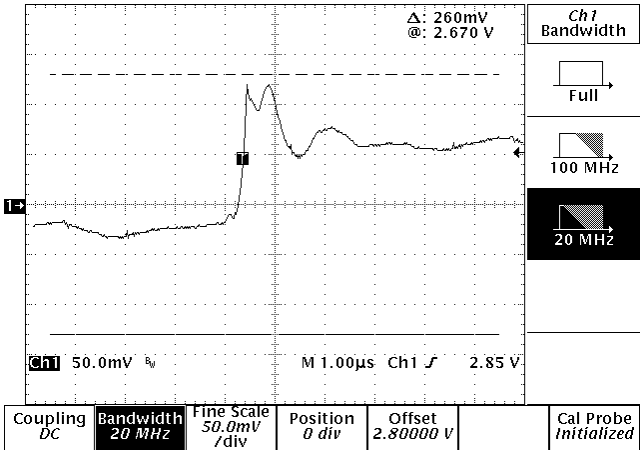
Parameter		Test Conditions	Min.	Typ.	Max.	Units
Input Specifications						
Primary Module Supply, 5Vin			4.75	5	5.25	V
MOSFET Bias Supply, 12Vin			11.4	12	12.6	V
Output Specifications						
Output Voltage Range, Vcc_{CORE}		See Table 2	1.3		3.5	V
Output Voltage Regulation	Steady State[1,2]	Vcc_{CORE} = 2.8V, $Icc_{CORE, Max}$ = 14.2A	2.74	2.80	2.90	V
	Transient[1,3]	Vcc_{CORE} = 2.8V, Icc_{CORE} = 1.0 to 14.2A	2.67	2.80	2.93	
Output Current, Icc_{CORE}			0.3		15	A
Initial Voltage Setpoint		Icc_{CORE} = 6A, T_A = 25°C		±20		mV
Load Regulation		Icc_{CORE} = 0.8A to 14.2A		-40		mV
Line Regulation		5Vin = 4.75V to 5.25V		±2		mV
Output Ripple		20MHz BW, Icc_{CORE} = 14.2A		20		mVp-p
Output Temperature Drift				+10		mV
Efficiency		Icc_{CORE} = 0.5A Icc_{CORE} = 14.2A	40 80	67 82		%
Turn-on Response Time					10	ms
General Specifications						
Switching Frequency				300		kHz
Short Circuit Protection				18		A

Notes:

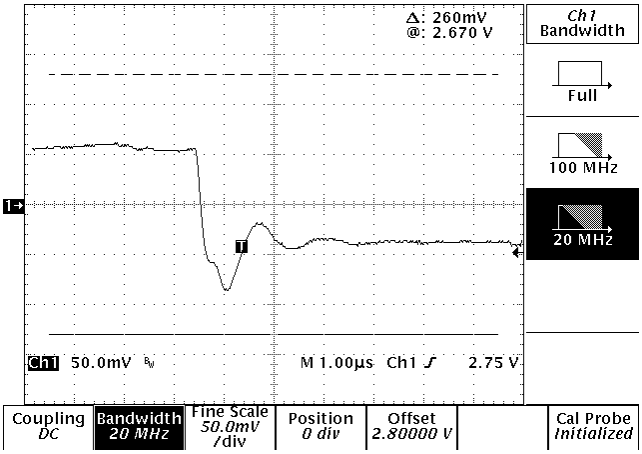
1. The voltage tolerance is measured at the DC-DC converter Header Output on the motherboard.
2. The Steady State Voltage Regulation includes Initial Voltage Setpoint, DC load regulation, Output Ripple and temperature drift, measured with a digital voltmeter with 1mV resolution. $Icc_{CORE, MIN}$ = 0.1A unless otherwise specified.
3. The output voltage is measured using the Intel provided EMT Tester (Rev. 1.0). It is assumed that a minimum of 20 x 0.1µF ceramic capacitors are placed directly next to the CPU to provide adequate high-speed decoupling. Additional bulk capacitors may be required as close as possible to the CPU socket on the motherboard when using the VRM. See Application Bulletin AB 5 for details.

Transient Plots

Transient Plot, Vout =2.8V, Iload=14.2A to 0.8A
RCB005 VRM

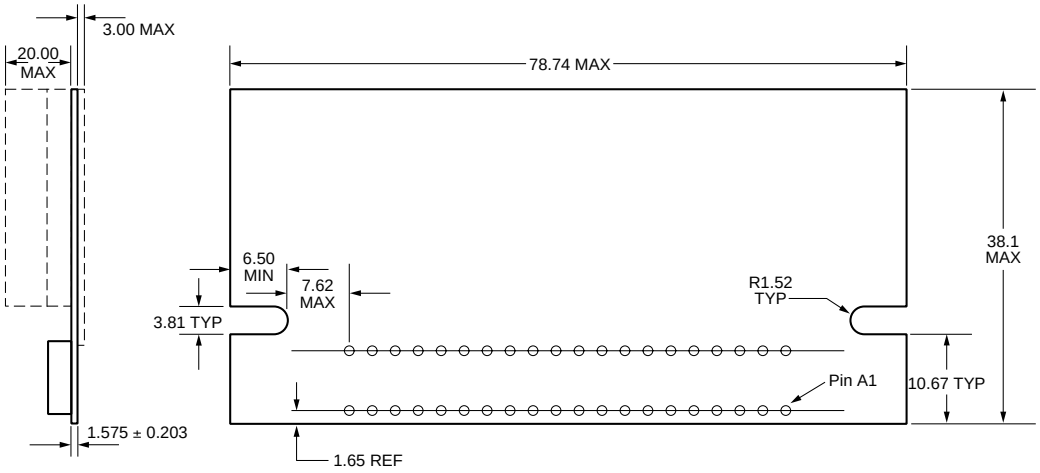


Transient Plot, Vout=2.8V, Iload=0.5A to 14.2A
RCB005 VRM



Notes:

Mechanical Dimensions (mm)



Ordering Information

Part Number	Input	Output Current
RCB005-K	5V DC	15A

RCB005

5 Bit Voltage Regulator Module (VRM) for Pentium® II Processors

For 5V Power Supply

Features

- Programmable 1.3V to 3.5V output
- Output current to 15A
- 5-bit digital input selects output voltage
- Typical efficiency > 82%
- DC output accuracy within ±60mV
- Current limiting short-circuit protection
- Power Good output
- Output Enable function
- Excellent transient response
- Meets Intel VRM specifications

Applications

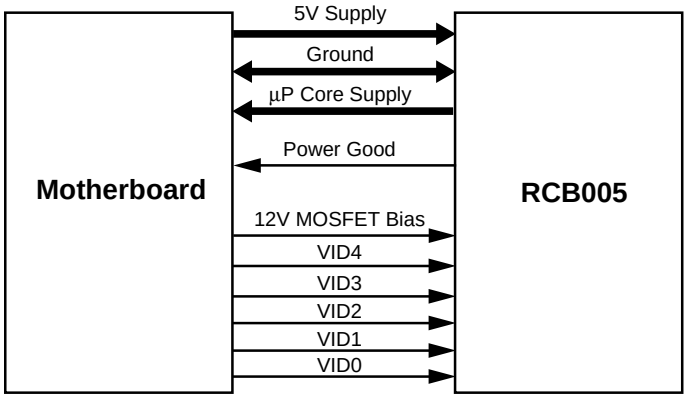
- Pentium II Klamath VRM
- Next generation Pentium II VRM

Description

The RCB005 is a programmable DC-DC VRM designed to deliver the selectable processor core voltage required by Pentium II microprocessors. This VRM converts the +5V power supply voltage to the voltage required by the CPU. The RCB005 takes full advantage of Raytheon's RC5051 programmable DC-DC controller IC, utilizing synchronous architecture for maximum efficiency. This VRM integrates a 5-bit DAC function, Power Good, and Output Enable features. The result is a VRM with a minimum number of components that achieves high reliability at a competitive cost.

The RCB005 provides an extremely well regulated selectable output voltage from 1.3V to 3.5V. Voltage selection is accomplished through a 5-bit digital input. The Power Good output provides a logic LOW when an out-of-tolerance voltage is detected at the VRM output. Other features include high efficiency, short-circuit and over-voltage protection, output enable, and low package weight. The RCB005 VRM module is designed as a point-of-load converter for Pentium II processors, minimizing the distribution losses normally occuring when drawing high currents from a centralized power supply.

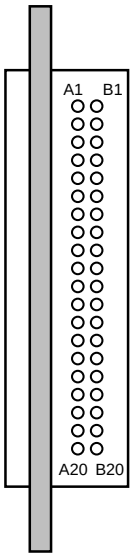
Block Diagram



65-RCB005-1

Pin Orientation — Top View

(Socket: AMPMOD2 532956-7 or equivalent)



65-RCB005-2

Table 1. RCB005 Pin Definitions

Pin #	Row A	Row B
1	5Vin	5Vin
2	5Vin	5Vin
3	5Vin	5Vin
4	12Vin	12Vin
5	12Vin	NC[1]
6	NC[1]	OUTEN
7	VID0	VID1
8	VID2	VID3
9	VID4	PWRGD
10	$V_{CC_{CORE}}$	Vss
11	Vss	$V_{CC_{CORE}}$
12	$V_{CC_{CORE}}$	Vss
13	Vss	$V_{CC_{CORE}}$
14	$V_{CC_{CORE}}$	Vss
15	Vss	$V_{CC_{CORE}}$
16	$V_{CC_{CORE}}$	Vss
17	Vss	$V_{CC_{CORE}}$
18	$V_{CC_{CORE}}$	Vss
19	Vss	$V_{CC_{CORE}}$
20	$V_{CC_{CORE}}$	Vss

Note:
1. Not used on module; no current is drawn.

VRM Connector Pin Reference

Pin Description	Input/Output	Function
5Vin	I	Primary module supply voltage.
12Vin	I	MOSFET bias supply voltage.
OUTEN (Output Enable) Open collector TTL input.	I	If OUTEN = HIGH (floating), output enabled.If OUTEN = LOW, output disabled and PWRGD output LOW.
VID0 to VID4 (Voltage Identification Code) Open collector TTL inputs.	I	These five signals are used to indicate the voltage required by the processor. See Table 2.
PWRGD (Power Good) Open collector TTL output.	O	If PWRGD = HIGH, output voltage within specifications. If PWRGD = LOW, output voltage not within ±10% of nominal. The PWRGD output will change to the proper state within 5ms of the output coming into or going out of its specified range.
$V_{CC_{CORE}}$	O	Processor core voltage.
Vss	I, O	Ground.

Table 2. Output Voltage vs. Voltage Identification Code

VID4	VID3	VID2	VID1	VID0	Nominal Voltage to CPU (Vcc_{CORE})
0	1	1	1	1	1.30V
0	1	1	1	0	1.35V
0	1	1	0	1	1.40V
0	1	1	0	0	1.45V
0	1	0	1	1	1.50V
0	1	0	1	0	1.55V
0	1	0	0	1	1.60V
0	1	0	0	0	1.65V
0	0	1	1	1	1.70V
0	0	1	1	0	1.75V
0	0	1	0	1	1.80V
0	0	1	0	0	1.85V
0	0	0	1	1	1.90V
0	0	0	1	0	1.95V
0	0	0	0	1	2.00V
0	0	0	0	0	2.05V

VID4	VID3	VID2	VID1	VID0	Nominal Voltage to CPU (Vcc_{CORE})
1	1	1	1	1	2.0V
1	1	1	1	0	2.1V
1	1	1	0	1	2.2V
1	1	1	0	0	2.3V
1	1	0	1	1	2.4V
1	1	0	1	0	2.5V
1	1	0	0	1	2.6V
1	1	0	0	0	2.7V
1	0	1	1	1	2.8V
1	0	1	1	0	2.9V
1	0	1	0	1	3.0V
1	0	1	0	0	3.1V
1	0	0	1	1	3.2V
1	0	0	1	0	3.3V
1	0	0	0	1	3.4V
1	0	0	0	0	3.5V

Note:

1. "0" indicates processor pin is tied to 0V (V_{SS})
   "1" indicates it is tied to 5V or is open.

Electrical Specifications

5Vin = +5V, 12Vin = +12V, T_A = 0°C to 60°C, Vcc_{CORE} = 2.8V, and airflow of 100LFM, unless otherwise specified.

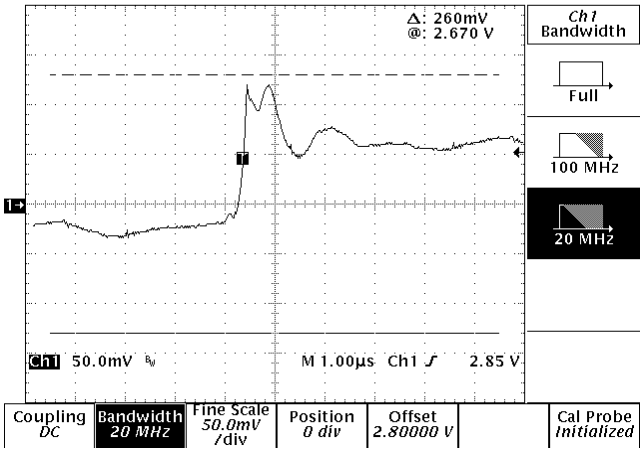
Parameter		Test Conditions	Min.	Typ.	Max.	Units
Input Specifications						
Primary Module Supply, 5Vin			4.75	5	5.25	V
MOSFET Bias Supply, 12Vin			11.4	12	12.6	V
Output Specifications						
Output Voltage Range, Vcc_{CORE}		See Table 2	1.3		3.5	V
Output Voltage Regulation	Steady State[2]	Vcc_{CORE} = 2.8V, $Icc_{CORE, Max}$ = 14.2A	2.74	2.80	2.90	V
	Transient[3]	Vcc_{CORE} = 2.8V, Icc_{CORE} = 1.0 to 14.2A	2.67	2.80	2.93	
Output Voltage Regulation	Steady State[2]	Vcc_{CORE} = 2.0V, $Icc_{CORE, Max}$ = 11.1A	1.94	2.0	2.06	V
	Transient[3]	Vcc_{CORE} = 2.0V, Icc_{CORE} = 0.5 to 11.1A	1.90	2.0	2.10	
Output Current, Icc_{CORE}			0.3		15	A
Initial Voltage Setpoint		Icc_{CORE} = 6A, T_A = 25°C		±20		mV
Load Regulation		Icc_{CORE} = 0.8A to 14.2A		-40		mV
Line Regulation		5Vin = 4.75V to 5.25V		±2		mV
Output Ripple		20MHz BW, Icc_{CORE} = 14.2A		20		mVp-p
Output Temperature Drift				+10		mV
Efficiency		Icc_{CORE} = 0.5A Icc_{CORE} = 14A	40 80	67 82		%
Turn-on Response Time					10	ms
General Specifications						
Switching Frequency				300		kHz
Short Circuit Protection				18		A

Notes:

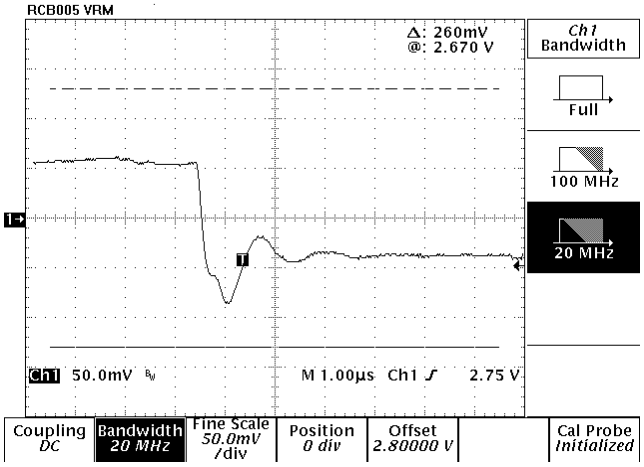
1. The voltage tolerance is measured at the DC-DC converter Header Output on the motherboard.
2. The Steady State Voltage Regulation includes Initial Voltage Setpoint, DC load regulation, Output Ripple and temperature drift, measured with a digital voltmeter with 1mV resolution. $Icc_{CORE, MIN}$ = 0.1A unless otherwise specified.
3. The output voltage is measured using the Intel provided EMT Tester (Rev. 1.0). It is assumed that a minimum of 20 x 0.1µF ceramic capacitors are placed directly next to the CPU to provide adequate high-speed decoupling. Additional bulk capacitors may be required as closely as possible to the CPU socket on the motherboard when using the VRM. See Application Bulletin AB 5 for details.

Transient Plots

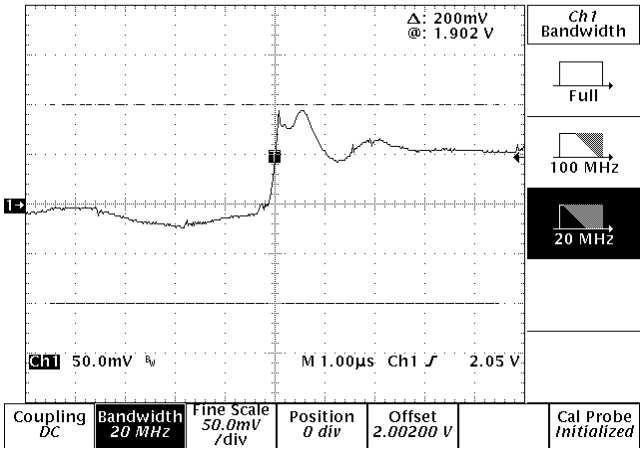
Transient Plot, Vout =2.8V, Iload=14.2A to 0.8A
RCB005 VRM



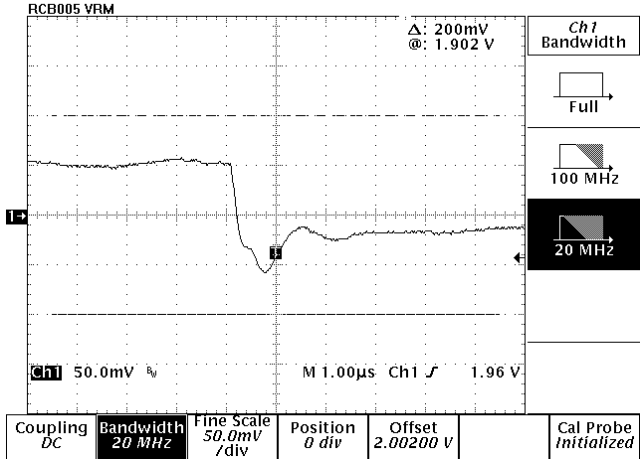
Transient Plot, Vout=2.8V, Iload=0.5A to 14.2A
RCB005 VRM



Transient Plot Vout=2.0V, Iload=11.1A to 0.5A
RCB005 VRM

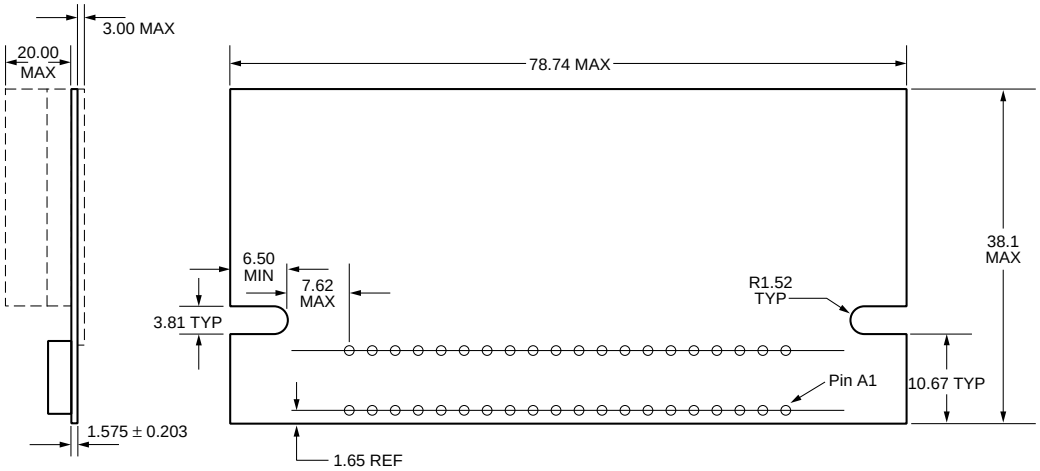


Transient Plot Vout=2.0V, Iload=0.5A to 11.1A
RCB005 VRM



Notes:

Mechanical Dimensions (mm)



Ordering Information

Part Number	Input	Output Current
RCB005	5V DC	15A

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RCB006-K

5 Bit Voltage Regulator Module (VRM) for Pentium® Pro and Pentium II Processors

For 12V Input Voltage

Features

- Programmable 1.3V to 3.5V output
- Output current to 15A
- 5-bit digital input selects output voltage
- Current limiting short-circuit protection
- Power Good output
- Output Enable function
- Excellent transient response
- Meets Intel VRM specifications

Applications

- Pentium Pro VRM
- Pentium II (Klamath type) VRM

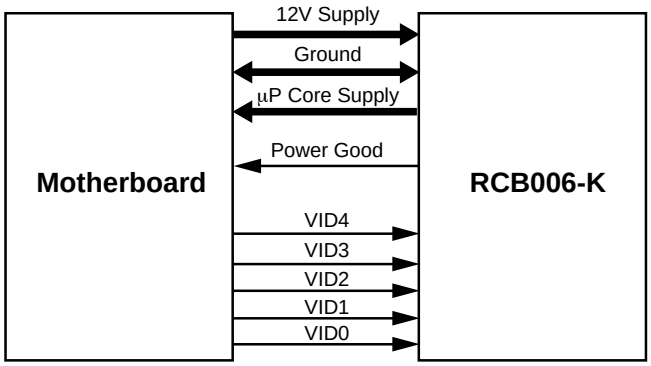
Description

The RCB006-K is a programmable DC-DC VRM designed to deliver the selectable processor core voltage required by Pentium Pro and Pentium II (Klamath type) processors. This VRM converts the +12V power supply voltage to the voltage required by the CPU core.

By taking advantage of Fairchild's RC5051 programmable DC-DC controller IC, the RCB006-K utilizes a synchronous architecture for maximum efficiency. In addition, this VRM integrates a 5-bit DAC function, Power Good, and Output Enable features. The result is a VRM with a minimum number of components that achieves high reliability at a competitive cost.

The RCB006-K provides an extremely well regulated selectable output voltage from 1.3V to 3.5V. Voltage selection is accomplished through a 5-bit digital input. The Power Good output provides a logic LOW when an out-of-tolerance voltage is detected at the VRM output. Other features include high efficiency, short-circuit and over-voltage protection, output enable, and low package weight. The RCB006-K has been designed as a point-of-load converter for Pentium II and Pentium Pro processors, minimizing the distribution losses normally occurring when drawing high currents from a centralized power supply.

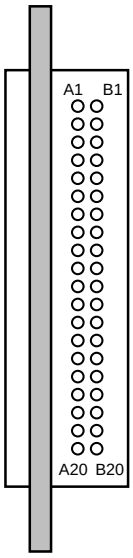
Block Diagram



65-RCB006-1

Pin Orientation — Top View

(Socket: AMPMOD2 532956-7 or equivalent)



65-RCB005-2

Table 1. RCB006-K Pin Definitions

Pin #	Row A	Row B
1	5Vin	5Vin
2	5Vin	5Vin
3	5Vin	5Vin
4	12Vin	12Vin
5	12Vin	NC[1]
6	NC[1]	OUTEN
7	VID0	VID1
8	VID2	VID3
9	VID4	PWRGD
10	$V_{CC_{CORE}}$	Vss
11	Vss	$V_{CC_{CORE}}$
12	$V_{CC_{CORE}}$	Vss
13	Vss	$V_{CC_{CORE}}$
14	$V_{CC_{CORE}}$	Vss
15	Vss	$V_{CC_{CORE}}$
16	$V_{CC_{CORE}}$	Vss
17	Vss	$V_{CC_{CORE}}$
18	$V_{CC_{CORE}}$	Vss
19	Vss	$V_{CC_{CORE}}$
20	$V_{CC_{CORE}}$	Vss

Note:
1. Not used on module; no current is drawn.

VRM Connector Pin Reference

Pin Description	Input/Output	Function
12Vin	I	Primary module supply voltage.
5Vin	I	IC bias supply voltage.
OUTEN (Output Enable) Open collector TTL input.	I	If OUTEN = HIGH (floating), output enabled.If OUTEN = LOW, output disabled and PWRGD output LOW.
VID0 to VID4 (Voltage Identification Code) Open collector TTL inputs.	I	These five signals are used to indicate the voltage required by the processor. See Table 2.
PWRGD (Power Good) Open collector TTL output.	O	If PWRGD = HIGH, output voltage within specifications. If PWRGD = LOW, output voltage not within ±10% of nominal. The PWRGD output will change to the proper state within 5ms of the output coming into or going out of its specified range.
$V_{CC_{CORE}}$	O	Processor core voltage.
Vss	I, O	Ground.

Table 2. Output Voltage vs. Voltage Identification CodeNote:

VID4	VID3	VID2	VID1	VID0	Nominal Voltage to CPU (V_{CCCORE})
0	1	1	1	1	1.30V
0	1	1	1	0	1.35V
0	1	1	0	1	1.40V
0	1	1	0	0	1.45V
0	1	0	1	1	1.50V
0	1	0	1	0	1.55V
0	1	0	0	1	1.60V
0	1	0	0	0	1.65V
0	0	1	1	1	1.70V
0	0	1	1	0	1.75V
0	0	1	0	1	1.80V
0	0	1	0	0	1.85V
0	0	0	1	1	1.90V
0	0	0	1	0	1.95V
0	0	0	0	1	2.00V
0	0	0	0	0	2.05V

VID4	VID3	VID2	VID1	VID0	Nominal Voltage to CPU (V_{CCCORE})
1	1	1	1	1	2.0V
1	1	1	1	0	2.1V
1	1	1	0	1	2.2V
1	1	1	0	0	2.3V
1	1	0	1	1	2.4V
1	1	0	1	0	2.5V
1	1	0	0	1	2.6V
1	1	0	0	0	2.7V
1	0	1	1	1	2.8V
1	0	1	1	0	2.9V
1	0	1	0	1	3.0V
1	0	1	0	0	3.1V
1	0	0	1	1	3.2V
1	0	0	1	0	3.3V
1	0	0	0	1	3.4V
1	0	0	0	0	3.5V

Note:

1. "0" indicates processor pin is tied to 0V (V_{SS})
   "1" indicates it is tied to 5V or is open.

Electrical Specifications

5Vin = +5V, 12Vin = +12V, T_A = 0°C to 60°C, Vcc_{CORE} = 2.8V, and airflow of 100LFM, unless otherwise specified.

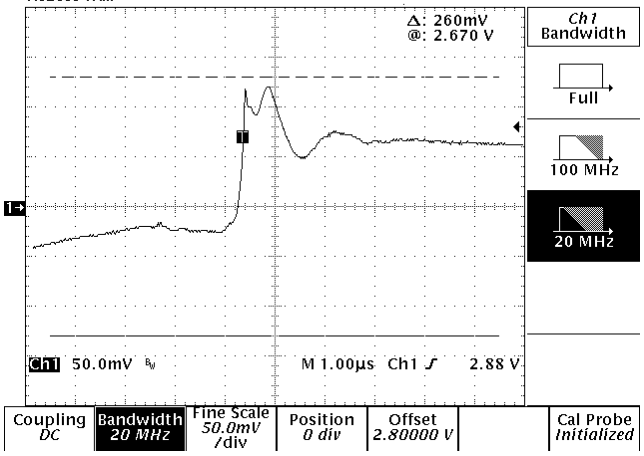
Parameter		Test Conditions	Min.	Typ.	Max.	Units
Input Specifications						
Primary Module Supply, 12Vin			11.4	12.0	12.6	V
IC Bias Supply, 5Vin			4.75	5.0	5.25	V
Output Specifications						
Output Voltage Range, Vcc_{CORE}		See Table 2	1.3		3.5	V
Output Voltage Regulation	Steady State[1,2]	Vcc_{CORE} = 2.8V, $Icc_{CORE, Max}$ = 14.2A	2.74	2.80	2.90	V
	Transient[1,3]	Vcc_{CORE} = 2.8V, Icc_{CORE} = 1.0 to 14.2A	2.67	2.80	2.93	
Output Current, Icc_{CORE}			0.3		15	A
Initial Voltage Setpoint		Icc_{CORE} = 6A, T_A = 25°C		±20		mV
Load Regulation		Icc_{CORE} = 0.8A to 14.2A		-40		mV
Line Regulation		5Vin = 4.75V to 5.25V		±2		mV
Output Ripple		20MHz BW, Icc_{CORE} = 14.2A		20		mVp-p
Output Temperature Drift				+10		mV
Efficiency		Icc_{CORE} = 0.5A Icc_{CORE} = 14.2A	40 80	65 82		%
Turn-on Response Time					10	ms
General Specifications						
Switching Frequency				120		kHz
Short Circuit Protection				18		A

Notes:

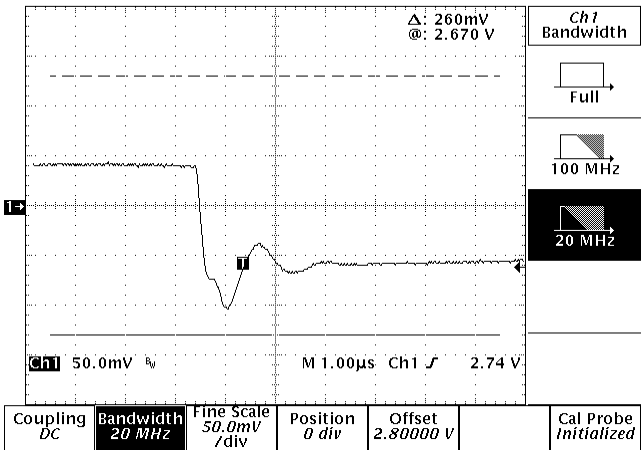
1. The voltage tolerance is measured at the DC-DC converter Header Output on the motherboard.
2. The Steady State Voltage Regulation includes Initial Voltage Setpoint, DC load regulation, Output Ripple and temperature drift, measured with a digital voltmeter with 1mV resolution. $Icc_{CORE, MIN}$ = 0.1A unless otherwise specified.
3. The output voltage is measured using the Intel provided EMT Tester (Rev. 1.0). It is assumed that a minimum of 20 x 0.1µF ceramic capacitors are placed directly next to the CPU to provide adequate high-speed decoupling. Additional bulk capacitors may be required as close as possible to the CPU socket on the motherboard when using the VRM. See Application Bulletin AB 5 for details.

Transient Plots

Transient Plot, Vout=2.8v, Iload=14.2A to 0.8A
RCB006 VRM

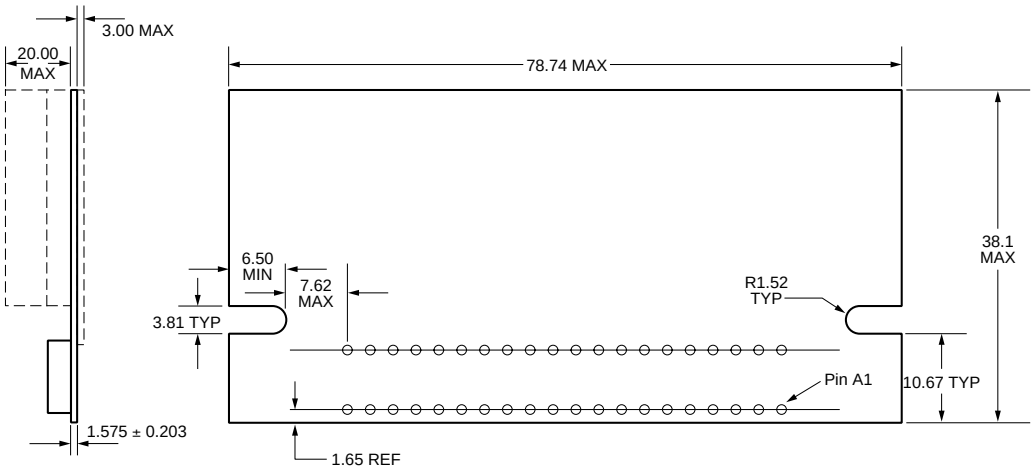


Transient Plot, Vout = 2.8V, Iload = 0.8A to 14.2A
RCB006 VRM



Notes:

Mechanical Dimensions (mm)



Ordering Information

Part Number	Input	Output Current
RCB006-K	12V DC	15A

RCB006

5 Bit Voltage Regulator Module (VRM) for Pentium® II Processors

For 12V Input Voltage

Features

- Programmable 1.3V to 3.5V output
- Output current to 15A
- 5-bit digital input selects output voltage
- Typical efficiency > 82%
- DC output accuracy within ±60mV
- Current limiting short-circuit protection
- Power Good output
- Output Enable function
- Excellent transient response
- Meets Intel VRM specification 8.2

Applications

- Pentium II Klamath VRM
- Next generation Pentium II VRM

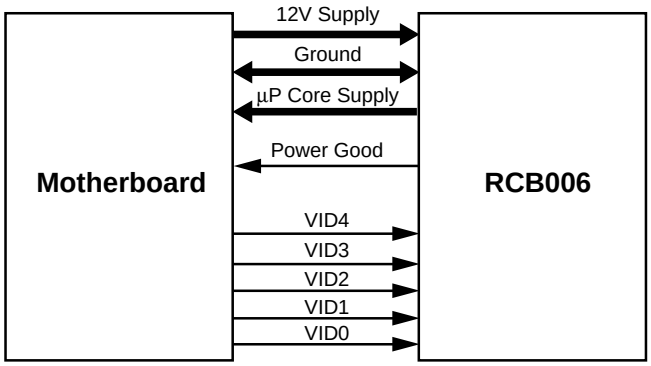
Description

The RCB006 is a programmable DC-DC VRM designed to deliver the selectable processor core voltage required by Pentium II and Pentium Pro processors. This VRM converts the +12V power supply voltage to the voltage required by the CPU core.

By taking advantage of Raytheon's RC5051 programmable DC-DC controller IC, the RCB006 utilizes a synchronous architecture for maximum efficiency. In addition, this VRM integrates a 5-bit DAC function, Power Good, and Output Enable features. The result is a VRM with a minimum number of components that achieves high reliability at a competitive cost.

The RCB006 provides an extremely well regulated selectable output voltage from 1.3V to 3.5V. Voltage selection is accomplished through a 5-bit digital input. The Power Good output provides a logic LOW when an out-of-tolerance voltage is detected at the VRM output. Other features include high efficiency, short-circuit and over-voltage protection, output enable, and low package weight. The RCB006 has been designed as a point-of-load converter for Pentium II and Pentium Pro processors, minimizing the distribution losses normally occuring when drawing high currents from a centralized power supply.

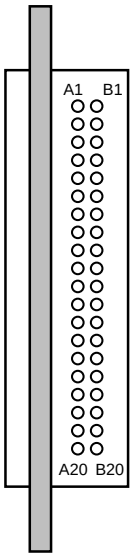
Block Diagram



65-RCB006-1

Pin Orientation — Top View

(Socket: AMPMOD2 532956-7 or equivalent)



65-RCB005-2

Table 1. RCB006 Pin Definitions

Pin #	Row A	Row B
1	5Vin	5Vin
2	5Vin	5Vin
3	5Vin	5Vin
4	12Vin	12Vin
5	12Vin	NC[1]
6	NC[1]	OUTEN
7	VID0	VID1
8	VID2	VID3
9	VID4	PWRGD
10	$V_{CC_{CORE}}$	Vss
11	Vss	$V_{CC_{CORE}}$
12	$V_{CC_{CORE}}$	Vss
13	Vss	$V_{CC_{CORE}}$
14	$V_{CC_{CORE}}$	Vss
15	Vss	$V_{CC_{CORE}}$
16	$V_{CC_{CORE}}$	Vss
17	Vss	$V_{CC_{CORE}}$
18	$V_{CC_{CORE}}$	Vss
19	Vss	$V_{CC_{CORE}}$
20	$V_{CC_{CORE}}$	Vss

Note:
1. Not used on module; no current is drawn.

VRM Connector Pin Reference

Pin Description	Input/Output	Function
12Vin	I	Primary module supply voltage.
5Vin	I	IC bias supply voltage.
OUTEN (Output Enable) Open collector TTL input.	I	If OUTEN = HIGH (floating), output enabled.If OUTEN = LOW, output disabled and PWRGD output LOW.
VID0 to VID4 (Voltage Identification Code) Open collector TTL inputs.	I	These five signals are used to indicate the voltage required by the processor. See Table 2.
PWRGD (Power Good) Open collector TTL output.	O	If PWRGD = HIGH, output voltage within specifications. If PWRGD = LOW, output voltage not within ±10% of nominal. The PWRGD output will change to the proper state within 5ms of the output coming into or going out of its specified range.
$V_{CC_{CORE}}$	O	Processor core voltage.
Vss	I, O	Ground.

Table 2. Output Voltage vs. Voltage Identification CodeNote:

VID4	VID3	VID2	VID1	VID0	Nominal Voltage to CPU (V_{CCCORE})
0	1	1	1	1	1.30V
0	1	1	1	0	1.35V
0	1	1	0	1	1.40V
0	1	1	0	0	1.45V
0	1	0	1	1	1.50V
0	1	0	1	0	1.55V
0	1	0	0	1	1.60V
0	1	0	0	0	1.65V
0	0	1	1	1	1.70V
0	0	1	1	0	1.75V
0	0	1	0	1	1.80V
0	0	1	0	0	1.85V
0	0	0	1	1	1.90V
0	0	0	1	0	1.95V
0	0	0	0	1	2.00V
0	0	0	0	0	2.05V

VID4	VID3	VID2	VID1	VID0	Nominal Voltage to CPU (V_{CCCORE})
1	1	1	1	1	2.0V
1	1	1	1	0	2.1V
1	1	1	0	1	2.2V
1	1	1	0	0	2.3V
1	1	0	1	1	2.4V
1	1	0	1	0	2.5V
1	1	0	0	1	2.6V
1	1	0	0	0	2.7V
1	0	1	1	1	2.8V
1	0	1	1	0	2.9V
1	0	1	0	1	3.0V
1	0	1	0	0	3.1V
1	0	0	1	1	3.2V
1	0	0	1	0	3.3V
1	0	0	0	1	3.4V
1	0	0	0	0	3.5V

Note:

1. "0" indicates processor pin is tied to 0V (V_{SS})
   "1" indicates it is tied to 5V or is open.

Electrical Specifications

5Vin = +5V, 12Vin = +12V, T_A = 0°C to 60°C, Vcc_{CORE} = 2.8V, and airflow of 100LFM, unless otherwise specified.

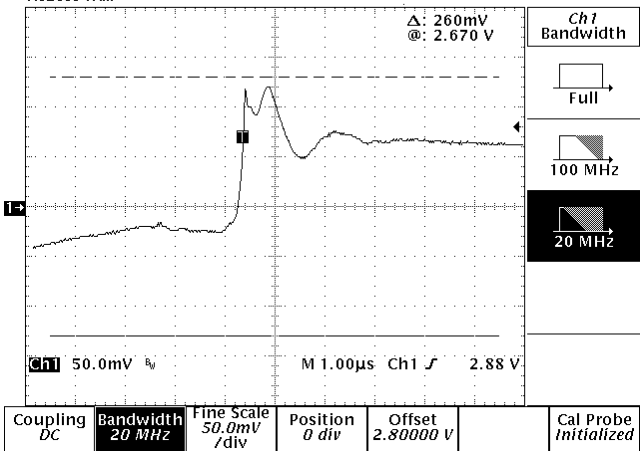
Parameter		Test Conditions[1]	Min.	Typ.	Max.	Units
Input Specifications						
Primary Module Supply, 12Vin			11.4	12.0	12.6	V
IC Bias Supply, 5Vin			4.75	5.0	5.25	V
Output Specifications						
Output Voltage Range, Vcc_{CORE}		See Table 2	1.3		3.5	V
Output Voltage Regulation	Steady State[2]	Vcc_{CORE} = 2.8V, $Icc_{CORE, Max}$ = 14.2A	2.74	2.80	2.90	V
	Transient[3]	Vcc_{CORE} = 2.8V, Icc_{CORE} = 1.0 to 14.2A	2.67	2.80	2.93	
Output Voltage Regulation	Steady State[2]	Vcc_{CORE} = 2.0V, $Icc_{CORE, Max}$ = 11.1A	1.94	2.0	2.06	V
	Transient[3]	Vcc_{CORE} = 2.0V, Icc_{CORE} = 0.5 to 11.1A	1.90	2.0	2.10	
Output Current, Icc_{CORE}			0.3		15	A
Initial Voltage Setpoint		Icc_{CORE} = 6A, T_A = 25°C		±20		mV
Load Regulation		Icc_{CORE} = 0.8A to 14.2A		-40		mV
Line Regulation		5Vin = 4.75V to 5.25V		±2		mV
Output Ripple		20MHz BW, Icc_{CORE} = 14.2A		20		mVp-p
Output Temperature Drift				+10		mV
Efficiency		Icc_{CORE} = 0.5A Icc_{CORE} = 14A	40 80	65 82		%
Turn-on Response Time					10	ms
General Specifications						
Switching Frequency				120		kHz
Short Circuit Protection				18		A

Notes:

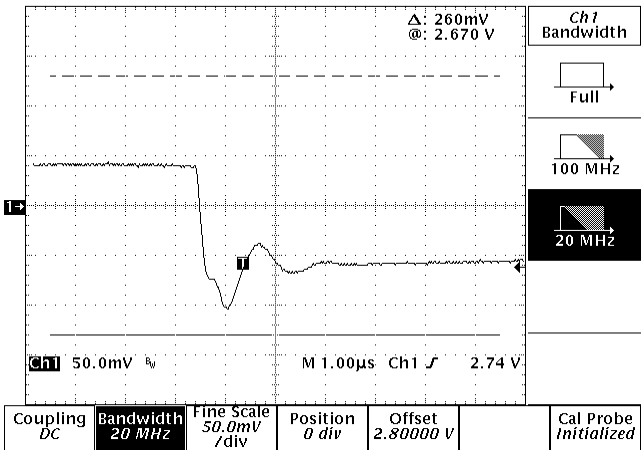
1. The voltage tolerance is measured at the DC-DC converter Header Output on the motherboard.
2. The Steady State Voltage Regulation includes Initial Voltage Setpoint, DC load regulation, Output Ripple and temperature drift, measured with a digital voltmeter with 1mV resolution. $Icc_{CORE, MIN}$ = 0.1A unless otherwise specified.
3. The output voltage is measured using the Intel provided EMT Tester (Rev. 1.0). It is assumed that a minimum of 20 x 0.1µF ceramic capacitors are placed directly next to the CPU to provide adequate high-speed decoupling. Additional bulk capacitors may be required as closely as possible to the CPU socket on the motherboard when using the VRM. See Application Bulletin AB 5 for details.

Transient Plots

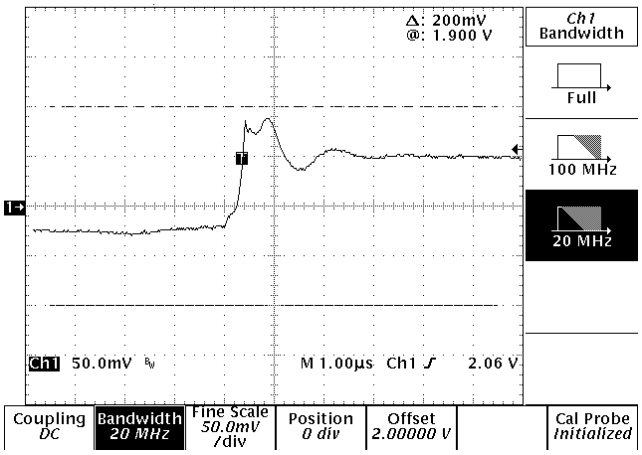
Transient Plot, Vout=2.8v, Iload=14.2A to 0.8A
RCB006 VRM



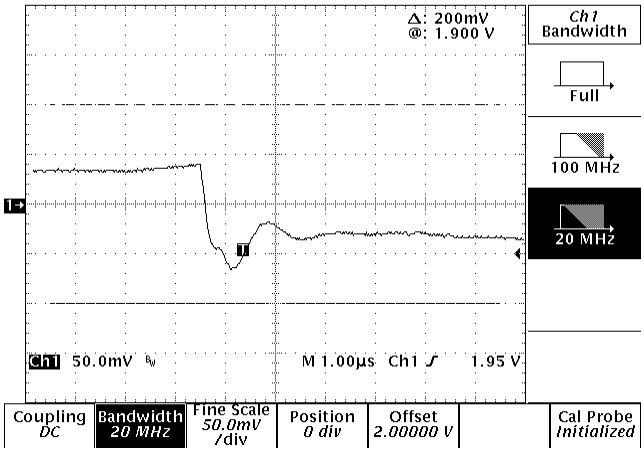
Transient Plot, Vout = 2.8V, Iload = 0.8A to 14.2A
RCB006 VRM



Transient Plot, Vout=2.0V, Iload=11.1A to 0.5A
RCB006 VRM

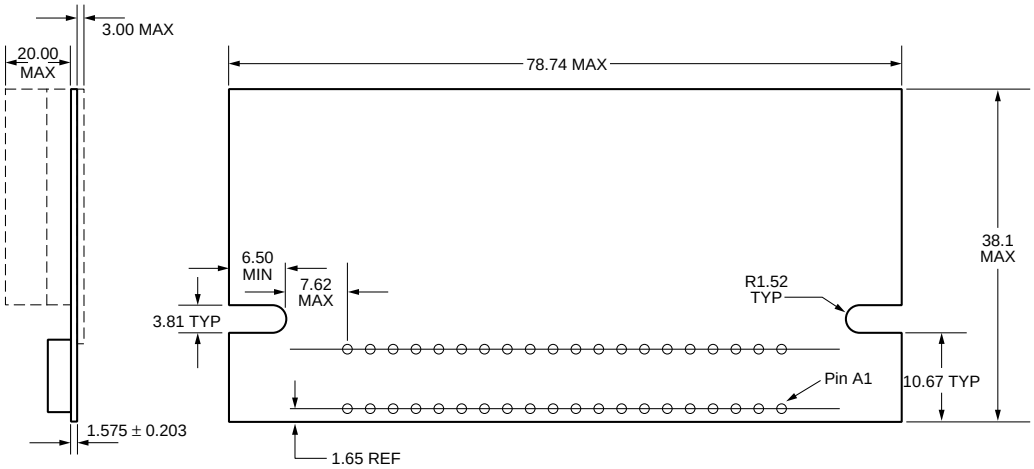


Transient Plot, Vout=2.0v, Iload=0.5A to 11.1A
RCB006 VRM



Notes:

Mechanical Dimensions (mm)



Ordering Information

Part Number	Input	Output Current
RCB006	12V DC	15A

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RCB007

5 Bit Voltage Regulator Module (VRM) for Pentium® II Processors

For 5V Power Supply

Features

- Programmable 1.3V to 3.5V output
- Output current to 15A
- 5-bit digital input selects output voltage
- Typical efficiency > 85%
- DC output accuracy within ±60mV
- Current limiting short-circuit protection
- Power Good output
- Output Enable function
- Excellent transient response
- Meets Intel VRM specifications

Applications

- Pentium II motherboard VRM module
- Programmable power supply module
- Template for motherboard implementation

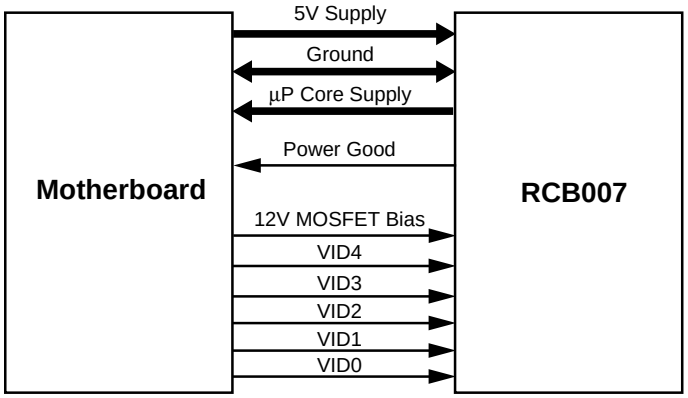
Description

The RCB007 is a programmable DC-DC VRM designed to deliver the selectable processor core voltage required by Pentium II microprocessors. This VRM allows board designers to support the entire Pentium II processor family with a single motherboard design, by converting the +5V power supply voltage to the voltage required by the CPU. The RCB007 takes full advantage of Raytheon's RC5051 programmable DC-DC controller IC, utilizing synchronous architecture for maximum efficiency. This VRM integrates a 5-bit DAC function, Power Good, and Output Enable features. The result is a VRM with a minimum number of components that achieves high reliability at a competitive cost.

The RCB007 provides an extremely well regulated selectable output voltage from 1.3V to 3.5V. Voltage selection is accomplished through a 5-bit digital input. The Power Good output provides a logic LOW when an out-of-tolerance voltage is detected at the VRM output. Other features include high efficiency, short-circuit and over-voltage protection, output enable, and low package weight. The RCB007 VRM module is designed as a point-of-load converter for Pentium II processors, minimizing the distribution losses normally occuring when drawing high currents from a centralized power supply.

Preliminary Information

Block Diagram



65-RCB007-1

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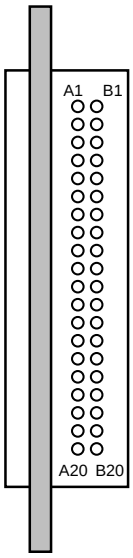
Rev 0.9.1

Preliminary Information

Pin Orientation —Top View

(Socket: AMPMOD2 532956-7 or equivalent)



65-RCB007-2

Table 1. RCB007 Pin Definitions

Pin #	Row A	Row B
1	5Vin	5Vin
2	5Vin	5Vin
3	5Vin	5Vin
4	12Vin	12Vin
5	12Vin	NC[1]
6	NC[1]	OUTEN
7	VID0	VID1
8	VID2	VID3
9	VID4	PWRGD
10	$V_{CC_{CORE}}$	Vss
11	Vss	$V_{CC_{CORE}}$
12	$V_{CC_{CORE}}$	Vss
13	Vss	$V_{CC_{CORE}}$
14	$V_{CC_{CORE}}$	Vss
15	Vss	$V_{CC_{CORE}}$
16	$V_{CC_{CORE}}$	Vss
17	Vss	$V_{CC_{CORE}}$
18	$V_{CC_{CORE}}$	Vss
19	Vss	$V_{CC_{CORE}}$
20	$V_{CC_{CORE}}$	Vss

Note:
1. Not used on module; no current is drawn.

VRM Connector Pin Reference

Pin Description	Input/Output	Function
5Vin	I	Primary module supply voltage.
12Vin	I	MOSFET bias supply voltage.
OUTEN (Output Enable) Open collector TTL input.	I	If OUTEN = HIGH (floating), output enabled.If OUTEN = LOW, output disabled and PWRGD output LOW.
VID0 to VID4 (Voltage Identification Code) Open collector TTL inputs.	I	These five signals are used to indicate the voltage required by the processor. See Table 2.
PWRGD (Power Good) Open collector TTL output.	O	If PWRGD = HIGH, output voltage within specifications. If PWRGD = LOW, output voltage not within ±10% of nominal. The PWRGD output will change to the proper state within 5ms of the output coming into or going out of its specified range.
$V_{CC_{CORE}}$	O	Processor core voltage.
Vss	I, O	Ground.

Electrical Specifications

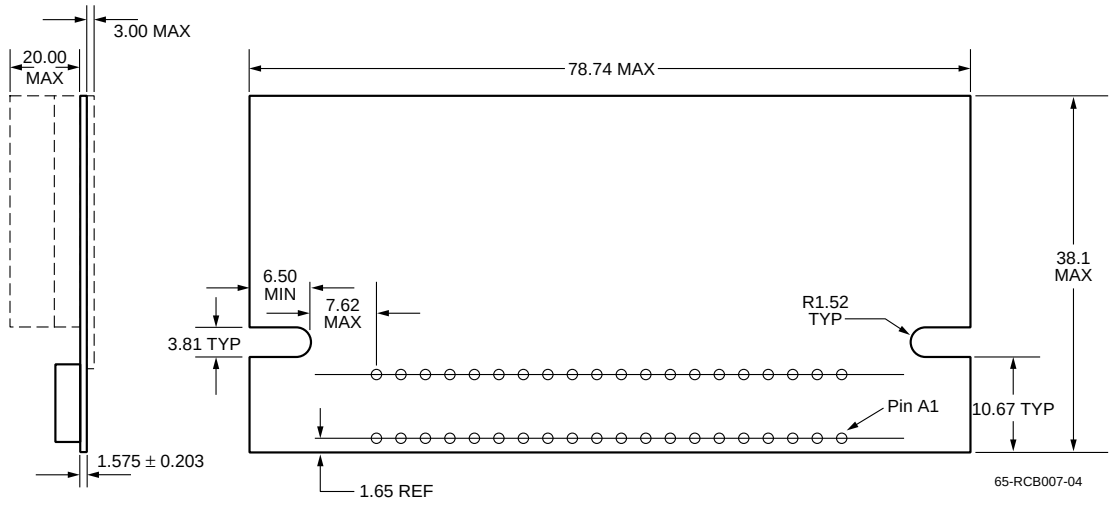
5Vin = +5V, 12Vin = +12V, T_A = 0°C to 60°C, Vcc_{CORE} = 2.8V, and airflow of 100LFM, unless otherwise specified.

Parameter		Test Conditions	Min.	Typ.	Max.	Units
Input Specifications						
Primary Module Supply, 5Vin			4.75	5	5.25	V
MOSFET Bias Supply, 12Vin			11.4	12	12.6	V
Output Specifications						
Output Voltage Range, Vcc_{CORE}		See Table 2	1.3		3.5	V
Output Voltage Regulation	Steady State[2]	Vcc_{CORE} = 2.8V, $Icc_{CORE, Max}$ = 14.2A	2.74	2.80	2.90	V
	Transient[3]	Vcc_{CORE} = 2.8V, Icc_{CORE} = 0.8 to 13.8A	2.67	2.80	2.93	
Output Voltage Regulation	Steady State[2]	Vcc_{CORE} = 2.0V, $Icc_{CORE, Max}$ = 15.0A	1.94	2.00	2.06	V
	Transient[3]	Vcc_{CORE} = 2.0V, Icc_{CORE} = 0.8 to 14.8A	1.90	2.00	2.10	
Output Current, Icc_{CORE}			0.3		15	A
Initial Voltage Setpoint		Icc_{CORE} = 6A, T_A = 25°C		±20		mV
Load Regulation		Icc_{CORE} = 0.8A to 15A		-40		mV
Line Regulation		5Vin = 4.75V to 5.25V		±2		mV
Output Ripple		20MHz BW, Icc_{CORE} = 15A		20		mVp-p
Output Temperature Drift				+10		mV
Efficiency		Icc_{CORE} = 0.5A Icc_{CORE} = 15A	40 80	67 83		%
Turn-on Response Time					10	ms
General Specifications						
Switching Frequency				300		kHz
Short Circuit Protection				18		A

Notes:

1. The voltage tolerance is measured at the DC-DC converter Header Output on the motherboard.
2. The Steady State Voltage Regulation includes Initial Voltage Setpoint, DC load regulation, Output Ripple and temperature drift, measured with a digital voltmeter with 1mV resolution. $Icc_{CORE, MIN}$ = 0.1A unless otherwise specified.
3. The output voltage is measured using the Intel provided EMT Tester (Rev. 1.0). It is assumed that a minimum of 20 x 0.1µF ceramic capacitors are placed directly next to the CPU to provide adequate high-speed decoupling. Additional bulk capacitors may be required as closely as possible to the CPU socket on the motherboard when using the VRM. See Application Bulletin AB 5 for details.

Mechanical Dimensions (mm)



Preliminary Information

Table 2. Output Voltage vs. Voltage Identification Code

VID4	VID3	VID2	VID1	VID0	Nominal Voltage to CPU (V_{CCCORE})
0	1	1	1	1	1.30V
0	1	1	1	0	1.35V
0	1	1	0	1	1.40V
0	1	1	0	0	1.45V
0	1	0	1	1	1.50V
0	1	0	1	0	1.55V
0	1	0	0	1	1.60V
0	1	0	0	0	1.65V
0	0	1	1	1	1.70V
0	0	1	1	0	1.75V
0	0	1	0	1	1.80V
0	0	1	0	0	1.85V
0	0	0	1	1	1.90V
0	0	0	1	0	1.95V
0	0	0	0	1	2.00V
0	0	0	0	0	2.05V

VID4	VID3	VID2	VID1	VID0	Nominal Voltage to CPU (V_{CCCORE})
1	1	1	1	1	2.0V
1	1	1	1	0	2.1V
1	1	1	0	1	2.2V
1	1	1	0	0	2.3V
1	1	0	1	1	2.4V
1	1	0	1	0	2.5V
1	1	0	0	1	2.6V
1	1	0	0	0	2.7V
1	0	1	1	1	2.8V
1	0	1	1	0	2.9V
1	0	1	0	1	3.0V
1	0	1	0	0	3.1V
1	0	0	1	1	3.2V
1	0	0	1	0	3.3V
1	0	0	0	1	3.4V
1	0	0	0	0	3.5V

Note:

1. "0" indicates processor pin is tied to 0V (V_{SS}), "1" indicates it is tied to 5V or is open.

Ordering Information

Part Number	Input	Output Current
RCB007	5V DC	15A

Preliminary Information

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RCB010

Voltage Regulator Module (VRM) for PowerPC™ Processors

Features

- 5-bit digital input selects output voltage
- Programmable 1.3V to 3.5V output from 5V supply
- Maximum output current 8A
- Efficiency > 80%
- Total output accuracy within ±3%
- Short circuit protection
- Excellent transient response
- Output voltage set by CPU or preset on VRM.

Applications

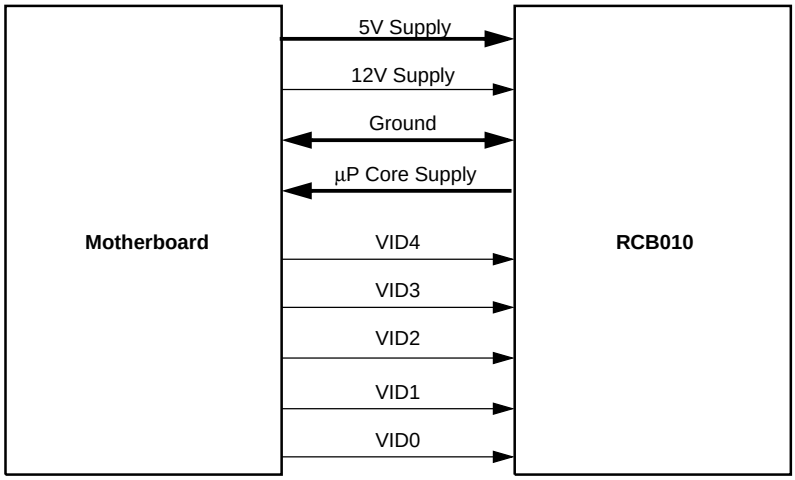
- VRM module for PowerPC motherboards
- Programmable power supply module

Description

The RCB010 is a programmable DC-DC Voltage Regulator Module designed to deliver the selectable processor core voltage required by the PowerPC microprocessors. This VRM offers flexibility to board designers to support PowerPC processors with a modular add-in power supply. The RCB010 takes full advantage of a proprietary Raytheon programmable DC-DC controller IC. This IC integrates a 5-bit DAC for automatic output programmability without the need for external precision resistors. The result is a VRM with a minimum number of components that achieves high reliability at a competitive cost.

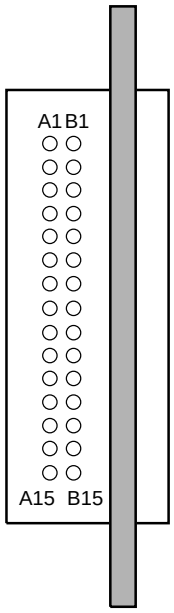
The RCB010 provides an extremely well regulated selectable output voltage from 1.3V to 3.5V. Output voltage selection is accomplished through a 5-bit interface between the processor and the module connector. Other features include high efficiency, short circuit protection, and low package weight.

Block Diagram



Pin Orientation — Top View

(Socket: AMPMOD2 532956-5 or equivalent)



RCB010 Pin Definitions

Pin #	Row A	Row B
1	GND	GND
2	GND	GND
3	3.3V[1]	3.3V[1]
4	3.3V[1]	3.3V[1]
5	5V	5V
6	5V	5V
7	VID4	VID2
8	VID3	VID1
9	VID0	12V
10	GND	GND
11	GND	GND
12	NC*	NC*
13	V_{OUT}	V_{OUT}
14	V_{OUT}	V_{OUT}
15	V_{OUT}	V_{OUT}

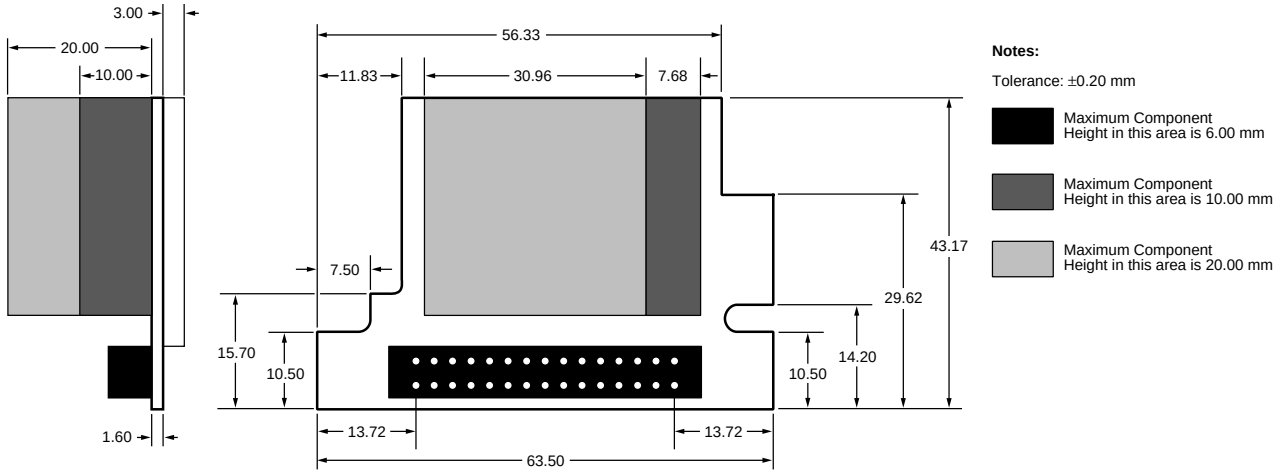
Note:

1. Not used on module; no current is drawn.

VRM Connector Pin Reference

Pin Description	Input/ Output	Function
5V	I	Supply voltage to support power to the CPU.
3.3V	I	Alternate supply voltage to support CPU. These pins are not used on this module, but are reserved for possible later use.
12V	I	Supply voltage for MOSFET drivers.
VID0 to VID4 (Voltage Identification) Open collector TTL inputs	I	These five signals are used to indicate the voltage required by the processor. The output can be programmed from 1.3V to 3.5V by setting the VID pins according to the Output Voltage Programming Codes table.
V_{OUT}	O	Module output voltage.
GND	I, O	Ground Reference.

Mechanical Dimensions (mm)



Electrical Specifications

(V_{IN} = +5V, T_A = 0°C to 60°C unless otherwise specified.)

Parameter	Test Conditions	Min.	Typ.	Max.	Units
Input Specifications					
Main supply voltage, 5V	Steady State	4.75	5	5.25	V
	100 msec maximum			6.5	
MOSFET supply voltage, 12V	Steady State	11.4	12	12.6	V
	100 msec maximum			18	
Output Specifications					
Output Voltage Range, V_{OUT}	See Output Programming Codes	1.3		3.5	V
DC Output Current, I_{OUT}		0	5	8	A
Set Point Accuracy[1]	I_{LOAD} = 2A, T_A = 25°C		±1.0		%
Load Regulation	I_{LOAD} = 0.5A to 7A		±30		mV
Line Regulation	V_{IN} = 5.0 ± 0.25 V		±3	±5	mV
Output Temperature Drift			20		ppm/°C
Load Transient (See Figure 1)[3]	I_{LOAD} = 0.5A to 6A, 20A/sec		10	20	mV
Step Recovery Time[3]	I_{LOAD} = 0.5A to 6A			100	µsec
Output Ripple[3]	I_{LOAD} = 6A		20	25	mV_{p-p}
Cumulative Accuracy[2]			±2	±3	%
Efficiency	I_{LOAD} = 8A, V_{OUT} = 1.8V	75	79		%
	I_{LOAD} = 8A, V_{OUT} = 2.8V	80	82		%
General Specifications					
Switching Frequency			300		KHz
Short Circuit Protection		8	9	13	A

Notes:

1. Set Point Accurcy is defined as the static accuracy of the output voltage at 2A.
2. Cumulative Accuracy includes Set Point Accuracy, Output Temperature Drift, Line and Load Regulation.
3. Test fixture includes 3 x 100µF Tantalum capacitors (ESR < 100mΩ) and 48 x 1µF from output to GND at the CPU socket.

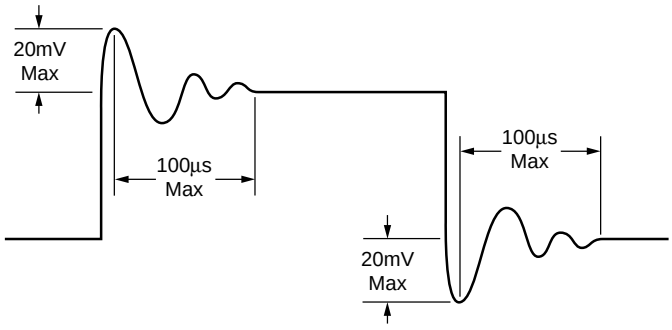


Figure 1. Load Transient

Output Voltage Programming Codes

VID4	VID3	VID2	VID1	VID0	Vout to CPU
0	1	1	1	1	1.30V
0	1	1	1	0	1.35V
0	1	1	0	1	1.40V
0	1	1	0	0	1.45V
0	1	0	1	1	1.50V
0	1	0	1	0	1.55V
0	1	0	0	1	1.60V
0	1	0	0	0	1.65V
0	0	1	1	1	1.70V
0	0	1	1	0	1.75V
0	0	1	0	1	1.80V
0	0	1	0	0	1.85V
0	0	0	1	1	1.90V
0	0	0	1	0	1.95V
0	0	0	0	1	2.00V
0	0	0	0	0	2.05V

VID4	VID3	VID2	VID1	VID0	Vout to CPU
1	1	1	1	1	2.0V
1	1	1	1	0	2.1V
1	1	1	0	1	2.2V
1	1	1	0	0	2.3V
1	1	0	1	1	2.4V
1	1	0	1	0	2.5V
1	1	0	0	1	2.6V
1	1	0	0	0	2.7V
1	0	1	1	1	2.8V
1	0	1	1	0	2.9V
1	0	1	0	1	3.0V
1	0	1	0	0	3.1V
1	0	0	1	1	3.2V
1	0	0	1	0	3.3V
1	0	0	0	1	3.4V
1	0	0	0	0	3.5V

Note:

1. 0 = processor pin is tied to GND
   1 = processor pin is open

Ordering Information

Part Number	Input	Output Current
RCB010	5V DC	8A

Fairchild Semiconductor Corporation
Americas
Customer Response Center
Tel:1-888-522-5372

Fairchild Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 8 141-35-0
English Tel: +44 (0) 1 793-85-68-56
Italy Tel: +39 (0) 2 57 5631

Fairchild Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Center, 5 Canto Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel:+852 2737-7200
Fax:+852 2314-0061

National Semiconductor Japan Ltd.
Tel:81-3-5620-6175
Fax:81-3-5620-6179

www.fairchildsemi.com

1/98 0.0m
Stock#DS3000B010

RCC611

100BaseTX Transceiver

Features

- 100 Mbps/125 Mbaud data rates
- Low power 0.6 micron CMOS technology
- PLL Clock and data recovery
- Clock synthesizer
- Auto-negotiation
- 4b/5b Encode/Decode
- FDDI TP/PMD scrambling/descrambling
- Management Interface for control/status
- Link Pulse Signalling
- Conforming to MII interface of IEEE 100baseTX Fast Ethernet Standard(P802.3u/D3)
- Low Power Dissipation—600 mW typical
- Single power supply: +5V
- PECL compatible serial data inputs/outputs
- Support for external 10 Mbps PHY
- 100 pin PQFP (20mm x 14mm x 2.7 mm)

Applications

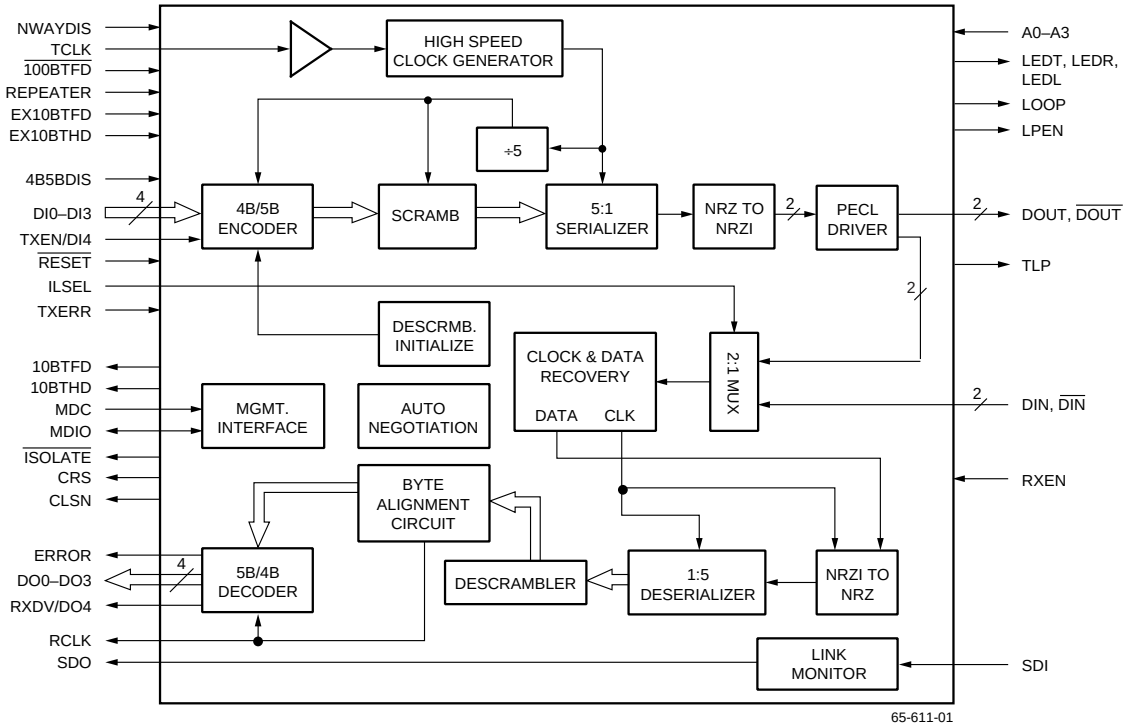
- Fast Ethernet Adapter/hub/switch
- FDDI Adapter/hub
- High Speed Point to Point Links
- Bus Extenders
- Multimedia
- High Resolution Graphic Displays
- Fast Ethernet test equipment
- FDDI Test Equipment

Description

The RCC611 is a monolithic 125 Megabaud CMOS transceiver chip. It integrates a complete phase-locked loop clock and data recovery, a phase locked loop clock synthesizer, a 5:1 Serializer, a 1:5 Deserializer, 4B/5B Encoder, 5B/4B Decoder, auto-negotiation and a management interface for link control and status. It also includes scrambler, descrambler for twisted pair copper applications in compliance with FDDI TP-PMD specifications. In conjunction with RCC613 twisted pair transceiver, the chipset can be used for driving with category 5 unshielded twisted pair cable and Type 1 shielded twisted pair cable. The chip meets the physical layer interface requirements of the 100 Base-X Fast Ethernet and FDDI standards. The RCC611 chip operates with a single, +5V power supply.

Advanced Information

Block Diagram



Rev. 0.5.0A

Advanced Information

Functional Description

Transmitter Section

The RCC611 transmitter section includes a phase locked loop synthesizer, 4B/5B encoder, scrambler and 5:1 serializer.

The RCC611 accepts a CMOS data nibble (DI0-DI3) and a control bit, TXEN. The data gets strobed on the positive transition of TCLK. The transmitter encodes the data, DI0-DI3 using 4b/5b coding (see Table 1). TXEN is used to denote the transmitter input being active or not. Whenever TXEN=0, IDLE symbol (11111) is encoded and transmitted. When TXEN transitions from 1 to 0, TR byte is sent before transmitting IDLE symbols. The order of transmission of the 4b/5b encoded output (E4..0)is that the most significant bit of the encoded symbol, E4 is transmitted first followed by E3,E2,E1 and E0.

When 4B5BDIS is HIGH, the 4b/5b encoder is bypassed. Under that case, TXEN is used as the fifth bit (DI4) of the encoded symbol. The order of transmission of the input when 4B5BDIS is HIGH is DI4 followed by DI3, DI2, DI1 and DI0.

The clock generator consists of a frequency multiplying Phase Locked Loop (PLL). The multiplying ratio is 5. The serial output goes through Non-Return-to-Zero (NRZ) to Non-Return-to-Zero Invert on Ones (NRZI) conversion. The NRZ to NRZI converter takes in the serial NRZ stream and puts out a transition for every 1 in the input stream. For zeros, there will be no transition. This will ensure that there is clocking information even when there is a long stream of 1s. The differential NRZI output is enabled to the output pins DOUT, $\overline{\text{DOUT}}$. The serial Data Stream (DOUT/ $\overline{\text{DOUT}}$) is transmitted at PECL levels (positive shifted ECL levels, Vth= +3.7 V). The input clock reference for the PLL Clock Generator, TCLK, typically comes from the CMOS protocol layer IC. TXERR=1 is used to force HALT symbol (00100) on the transmit output.

The encoded symbol is scrambled as per FDDI's TP-PMD standard. The scrambler used is a stream cipher scrambler. The scrambler polynomial is $1+x^{9}+x^{11}$.

Descrambler Initialization

The descrambler initialization timing is shown in the accompanying diagram. On powerup, TXEN=0. RCC611 automatically initializes the downstream descrambler by forcing IDLE symbols (11111) which gets scrambled and driven to the medium. Transmitting IDLE continues until TXEN=1.

The transmitter has the provision to loopback its output to the receiver input, when ILSEL=1. Under that case, a continuous logic LOW state is sent through the DOUT, $\overline{\text{DOUT}}$ pins.

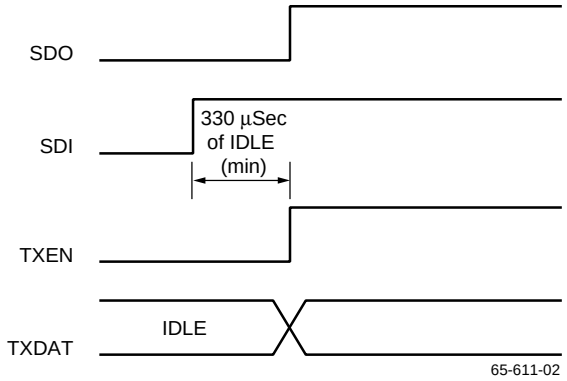


Figure 1.

There is also one more level of loopback provided through the external RCC613 chip. When control register Reg0 bit 14 is HIGH, LOOP output pin is HIGH and the the serial output, DOUT, $\overline{\text{DOUT}}$ goes through the RCC613 TXIP, TXIN inputs and loops back through the RXOP, RXON outputs back to the DIN, $\overline{\text{DIN}}$ of RCC611.

Table 1. 4B/5B Encoding

Symbol	TXEN	DI3–DI0	Encoded Output (E4-E0)
0	1	0000	11110
1	1	0001	01001
2	1	0010	10100
3	1	0011	10101
4	1	0100	01010
5	1	0101	01011
6	1	0110	01110
7	1	0111	01111
8	1	1000	10010
9	1	1001	10011
A	1	1010	10110
B	1	1011	10111
C	1	1100	11010
D	1	1101	11011
E	1	1110	11100
F	1	1111	11101
T	0	xxxx	01101
R	0	xxxx	00111
J	1	xxxx	11000
K	1	xxxx	10001
I (IDLE)	0	xxxx	11111
H (HALT)	1	xxxx	00100

Note:

1. All the symbols are encoded as per the state diagram provided in Chapter 28 of IEEE802.3.

Table 2. 5B/4B Decoding

Symbol	Encoded Output	DO3–0	ERROR
0	11110	0000	0
1	01001	0001	0
2	10100	0010	0
3	10101	0011	0
4	01010	0100	0
5	01011	0101	0
6	01110	0110	0
7	01111	0111	0
8	10010	1000	0
9	10011	1001	0
A	10110	1010	0
B	10111	1011	0
C	11010	1100	0
D	11011	1101	0
E	11100	1110	0
F	11101	1111	0
T	01101	xxxx	0
R	00111	xxxx	0
J	11000	xxxx	0
K	10001	xxxx	0
I	11111	xxxx	0
H	00100	xxxx	1
V	00000	xxxx	1
V	00001	xxxx	1
V	00010	xxxx	1
V	00011	xxxx	1
V	00101	xxxx	1
V	00110	xxxx	1
V	01000	xxxx	1
V	01100	xxxx	1
V	10000	xxxx	1
V	11011	xxxx	1

Note:

1. All the symbols are decoded as per the state diagram provided in Chapter 28 of IEEE802.3.

Receiver Section

The RCC611 Receiver section includes a 2 to 1 multiplexer, a complete phase-locked loop clock and data recovery, and decoder.

The 2 to 1 Mux is used to choose between the differential PECL receive input data (DIN, $\overline{\text{DIN}}$) or the transmit output for enabling to the clock and data recovery circuit. The choice of the inputs is made by the ILSEL pin. If ILSEL is HIGH, the transmit output is looped back to the input of the receiver. If ILSEL is LOW, the receive input is chosen.

The RCC611 recovers the clock and regenerates the encoded serial data. There is a PECL to CMOS converter for the SDI signal detect PECL input signal. If SDI goes LOW to HIGH, the SDO output goes HIGH after a minimum of 330 microseconds of continuous IDLE symbols to allow for the clock and data recovery and descrambler to synchronize.

The recovered encoded data is then converted to 5 parallel data lines via 1:5 De-Serializer.

The RCC611 contains a byte alignment circuitry. When the JK symbols are detected in the serial stream, the chip will automatically resynchronize the demultiplexer to byte align with the JK.

The data is then decoded into an 4-bit symbol via the 5b/4b decoder as per the 5b/4b Decoding table. The received data is checked during the 5b/4b decoding and violations are flagged by bringing the Error Flag (ERROR) to a level HIGH. The 5b/4b decoder is bypassed for FDDI.

The output from the 5b/4b decoder comes out as 4 bits of data, DO0–DO3 and one control bit output, RXDV. When 4B5BDIS is HIGH, the 5b/4b decoder is bypassed and the output come out as DO0-DO4 where DO4 replaces the RXDV signal.

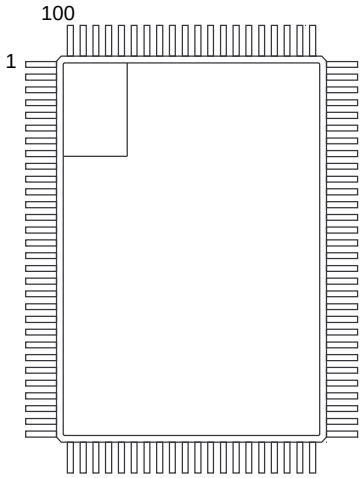
The demultiplexed data goes through a descrambler. The descrambler descrambles the data as per the polynomial discussed in the transmit section.

CLSN signal is flagged if the chip is transmitting and receiving data as per the IEEE802.3 transmit and receive state diagram in Chapter 24. CRS is flagged if either the chip is transmitting data or receiving data as per the IEEE802.3 transmit and receive state diagram in Chapter 24. Both CLSN and CRS are asynchronous signals.

Advanced Information

Advanced Information

Pin Assignments



Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	DGND	26	DVCC	51	LPEN	76	DVCC
2	DGND	27	$\overline{\text{RESET}}$	52	RXEN	77	NC
3	DVCC	28	LEDT	53	DGND	78	NC
4	DVCC	29	$\overline{\text{ISOLATE}}$	54	DGND	79	NC
5	NC	30	LEDR	55	DO3	80	NC
6	AGND	31	LEDL	56	DO2	81	DIN
7	DGND	32	DVCC	57	DO1	82	$\overline{\text{DIN}}$
8	4B5BDIS	33	DGND	58	DO0	83	NC
9	DI0	34	A0	59	DVCC	84	SDI
10	DI1	35	A1	60	DVCC	85	DGND
11	DI2	36	A2	61	RXDV/DO4	86	AGND
12	DI3	37	A3	62	ERROR	87	RXAVCC
13	TXEN/DI4	38	DGND	63	DGND	88	AGND
14	TXERR	39	DGND	64	RCLK	89	RXAVCC
15	DGND	40	10BTFD	65	SDO	90	TXAVCC
16	TCLK	41	10BTHD	66	AGND	91	AGND
17	DVCC	42	EX10BTHD	67	DGND	92	DGND
18	REPEATER	43	EX10BTFD	68	DVCC	93	DVCC
19	NC	44	CLSN	69	DGND	94	TXAVCC
20	MDC	45	CRS	70	DGND	95	TXAVCC
21	MDIO	46	$\overline{\text{100BTFD}}$	71	DVCC	96	AGND
22	LOOP	47	TLP	72	DVCC	97	AGND
23	NC	48	DVCC	73	DGND	98	ILSEL
24	NC	49	DVCC	74	DGND	99	$\overline{\text{DOUT}}$
25	DGND	50	NWAYDIS	75	DVCC	100	DOUT

Pin Descriptions

Pin Name	Pin Number	Type	Description
10BTFD	40	CMOS O/P	**10BaseT Full Duplex.**10BTFD is used to enable or disable a local 10BaseT Full duplex device.
10BTHD	41	CMOS O/P	**10BaseT Half Duplex.** 10BTHD is used to enable or disable a local 10BaseT half duplex physical layer device.
4B5BDIS	8	TTL I/P	**4b/5b disable.** This pin is used to disable the 4b/5b encoder and 5b/4b decoder.
A0–A3	34–37	TTL I/P	**Address 0–3.** A0–A3 pins are used to denote the physical address of the chip for writing or reading of the internal control/ status registers. During reset, if the PHY address are all zeroes (0000) then the MII interface will be tri-stated.
AGND	6, 66, 86, 88, 91, 96, 97		**Chip ground for Analog circuitry.** AGND pins should be connected to the printed circuit board's ground plane at the pins.
CLSN	44	CMOS O/P	**Collision.** This output is HIGH if the chip is receiving data and at the same time it is transmitting packet data. It is an asynchronous output. CLSN is LOW during Full duplex mode of operation.
CRS	45	CMOS O/P	**Carrier Sense.** This output is HIGH if the chip is either receiving data or transmitting packet data. It is an asynchronous output. CRS is determined by receive activity during Full duplex mode.
DGND	1, 2,7,15, 25, 33, 38, 39, 53, 54, 63, 67, 69, 70, 73, 74, 85, 92		**Chip ground for digital circuitry.** DGND should be connected to the printed circuit board's ground plane at the pins.

Pin Descriptions (continued)

Pin Name	Pin Number	Type	Description
DIN, $\overline{\text{DIN}}$	81, 82	PECL I/P	**Receiver differential input data.**
DO0–DO3	58-55	CMOS O/P	**Receiver output data.**
DOUT, $\overline{\text{DOUT}}$	100, 99	PECL O/P	**Transmit differential output data.**
DVCC	3, 4, 17, 26, 32, 48, 49, 59, 60, 68, 71, 72, 75, 76, 93		**Positive supply for Digital circuitry.** The nominal value is 5V ±5%. VCC should be bypassed to the ground plane with a 0.1µF chip capacitor placed as close to the pin as possible.
DI0–DI3	9-12	TTL I/P	**Transmitter Input data.**
ERROR	62	CMOS O/P	**Error Flag.** ERROR goes HIGH to flag 5B/4B decoding violations. It also indicates transition to idle condition from active without end of frame delimiters.
$\overline{\text{100BTFD}}$	46	CMOS O/P	**100BaseT Full Duplex.** $\overline{\text{100BTFD}}$ when low is used to activate a LED and indicates that the RCC611 is operating in the 100BaseT Full Duplex mode.
EX10BTFD	43	TTL I/P	**10BaseT Full Duplex.** When EX10BTFD is high, it indicates that there is available an external 10BaseT Physical layer device capable of full duplex operation. This input goes directly to Reg1 bit12.
EX10BTHD	42	TTL I/P	**10BaseT Half Duplex**. When EX10BTHD is high, it indicates that there is available an external 10BT physical layer device with half duplex capability. This input goes directly to Reg1 bit11.
$\overline{\text{ISOLATE}}$	29	CMOS O/P	**Isolate.** $\overline{\text{ISOLATE}}$ is used to indicate that the chip is in the isolate mode. When activated (low), all the MII interfaces will be tri-stated. Software can be used to override the the $\overline{\text{ISOLATE}}$ bit (Reg0 bit10). Note that the polarity of $\overline{\text{ISOLATE}}$ and Reg0 bit10 are the opposite to each other. See page 10 for more details.
LEDL	31	CMOS O/P	**LED Link OK.** It is used as an active LOW output to indicate that the link is OK as indicated by the FLG signal from the arbitration state machine.
LEDR	30	CMOS O/P	**LED Receive.** It is used as an active LOW output to indicate that the receive is active. It will be LOW if CRS = 1.
LEDT	28	CMOS O/P	**LED Transmit.** It is used as an active LOW output to indicate that the transmit is active. It will be LOW if TXEN = 1.
LOOP	22	CMOS O/P	**Loop.** LOOP is used to enable the loopback input of RCC613 chip. LOOP is active if the control register Reg0 bit 14 is HIGH .
LPEN	51	CMOS O/P	**Link Pulse Enable.** It provides an enable signal to the RCC613 for the transmit link pulse.
ILSEL	98	TTL I/P	**Loop Select.** ILSEL is used for differential loopback for “on-board” diagnostic of the device. When ILSEL is HIGH, the receiver accepts the serial output data from the transmitter section. Connect to GND or leave open when not used.
MDIO	21	TTL/CMOS I/O	**Management Data Input/Output.** MDIO is a bidirectional signal between RCC611 and the station management entity. It is used to transfer control and status information. All the read and write transactions are done synchronously with MDC.
MDC	20	TTL I/P	**Management Data Clock.** MDC is sourced by the station management entity to RCC611 as a timing reference for transfer of information on MDIO signal. MDC is an aperiodic signal whose minimum high and low times are 200 ns.

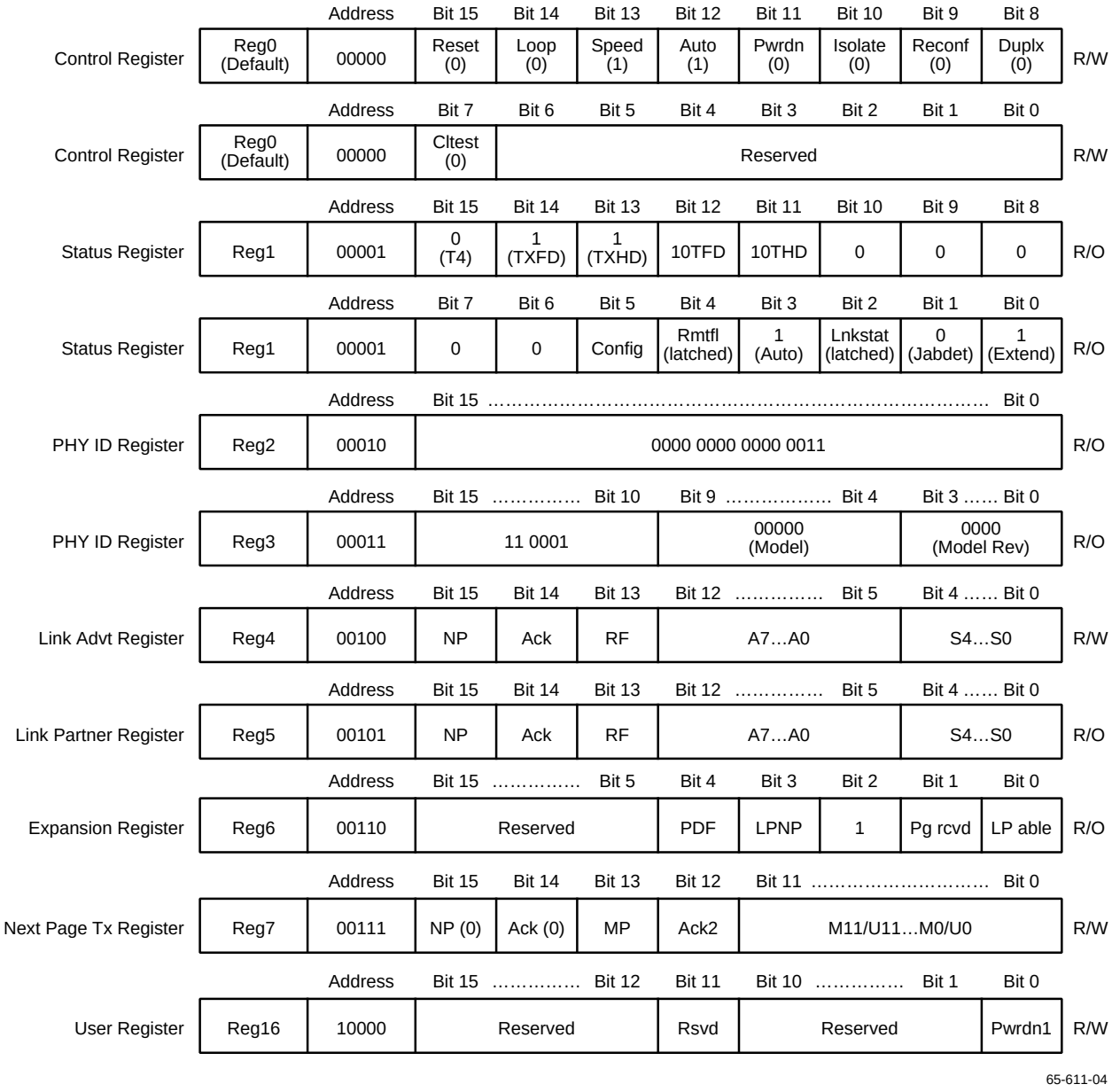
Advanced Information

Pin Descriptions (continued)

Pin Name	Pin Number	Type	Description
NWAYDIS	50	TTL I/P	**Nway Disable.** When NWAYDIS is high, the auto-negotiation state machines are disabled and AUTO bit (Reg0 bit12) is set to 0. Software can be used to override the AUTO bit. see page 10 for more details. For manual setting, see Table 3.
RCLK	64	CMOS O/P	**Receive Clock.** It is the recovered byte clock derived from the byte alignment circuitry. It provides timing to DO0–DO3, RXDV and ERROR.
REPEATER	18	TTL I/P	**Repeater/Node Mode.** When in the Repeater (high) mode as in the Full Duplex mode, CRS output is asserted due to activity from the receiver only. When in the Node (low) mode and not Full Duplex mode, CRS is asserted due to either receive or transmit activity.
$\overline{\text{RESET}}$	27	TTL I/P	**Reset.** RESET is an asynchronous input which when LOW is used to reset the state machines inside the chip. RESET needs to be LOW for at least one byte clock.
RXEN	52	TTL I/P	**Receive Enable.** When activated (high), it enables the outputs D0-D3, CRS, ERROR, RXDV, CLSN and RCLK. When low these outputs are tri-stated.
RXAVCC	87,89		**Positive Supply for Receive Analog Circuitry.** The nominal value is 5V±5%. RXAVCC should be bypassed to the ground plane with a 0.1µF chip capacitor placed as close to the pin as possible.
RXDV/DO4	61	CMOS O/P	**Receive Data Valid.** RXDV when HIGH indicates the receive output data being active. When 4B5BDIS is HIGH, this pin is used as DO4, the fifth data output.
SDI	84	PECL I/P	**Signal Detect Input.** It is converted to CMOS output level through a PECL to CMOS converter.
SDO	65	CMOS O/P	**Signal Detect Output.** SDO is the output from the PECL to CMOS converter for the signal detect signal. The signal is asserted 330 microseconds after SDIN goes HIGH. SDO output is made synchronous to RCLK and has the same timing as the DO0–3.
TCLK	16	TTL I/P	**Transmit Clock.** TCLK is the 25 MHz input reference for the internal high speed bit clock generator. It provides the timing for the input data, DI0..DI3, TXEN and TXERR.
TLP	47	CMOS O/P	**Transmit Link Pulse.** TLP is HIGH when a link pulse needs to be transmitted.
TXAVCC	90, 94, 95		**Positive supply for Transmit Analog circuity.** The nominal value is 5V ±5%. TXAVCC should be bypassed to the ground plane with a 0.1µF chip capacitor placed as close to the pin as possible.
TXEN/DI4	13	TTL I/P	**Transmit Enable .** WhenTXEN is HIGH, it indicates that the input data is active. When 4B5BDIS is HIGH, this pin is used as DI4, the fifth data input.
TXERR	14	TLL I/P	**Transmit Error.** TXERR is used to transmit VIOLATION symbols (00100) on the transmit output.

Advanced Information

Management Interface



65-611-04

Register Description

The management interface provides a simple, two wire, serial inteface (MDIO, MDC) to connect the station management entity to the PHY for control and status gathering. MDC is sourced by the station management entity to the PHY as a timing reference for transfer of information on the MDIO signal. MDC is an aperiodic signal with a minimum high and low times of 200 ns. MDIO is a bidirectional signal between PHY and the station management entity. Control information is driven by the station management entity synchronously to MDC and sampled synchronously by PHY. Status information is driven synchronously by PHY and sampled synchronously by the station management. As shown in the figure, there are a total of 9 sixteen bit registers: Reg0, Reg1, through Reg7 and Reg16. Their functions are detailed in the register definitions section. The default values for the registers where applicable are shown in parenthesis. All the status and control transistions occur synchronous to the local clock, TCLK.

Advanced Information

	Idle	SOF	OpCd	PHY Addr	Reg Addr	Fill	Data
Read:	Idle	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD
Write:	Idle	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD

Management Frame Structure

Management Frame Structure

The management frame structure is as shown in the figure. In between the frames is an Idle condition. The Idle condition on the two wire interface is a logic one through the internal pullup resistor. The open drain driver for MDIO will be disabled. Prior to initiating any transaction, the station management entity will send a sequence of 32 contiguous logic one bits on MDIO with 32 corresponding cycles on MDC to provide the chip with a pattern that it can use to establish synchronization.

The frame begins with an SOF field. SOF is indicated by a 01 pattern. The next field is Opcode. The Opcode for a read transaction is 10 and for a write transaction is 01. Next to Opcode is the PHY Address field. The PHY address is 5 bits. The first bit is the most significant bit of the PHY address. The chip will recognize 00000 as its own address. The next field is the register address. The register address is 5 bits. The register accessed at register address zero (00000) is the Register 0 (Reg0) and so on.

Next to the Register address is the Turnaround field. An idle bit time during which no device actively drives the MDIO signal is inserted between the Register address field and the Data field of the frame during a Read transaction in order to avoid contention. During a Read transaction, the chip will drive a zero bit onto MDIO for the bit time following the idle bit and preceding the Data field. During a write transaction, the station management entity will fill this idle time with a one bit followed by a zero bit. The data field is 16 bits. The first data bit transmitted and received is the MSB of the data payload.

Auto-Negotiation Signalling

The chip has the provision to advertise its mode of operation to the remote end of a link segment and detect corresponding operational modes that the other device may be advertising. The auto-negotiation algorithm is performed out of band using a modified 10baseT link integrity pulse sequence. The algorithm allows the devices at both ends of a link segment to request and acknowledge use of the commom modes of operation that both devices share and to reject the use of operational modes that are not shared by both devices. When more than one common mode exists between the two devices, a mechanism is provided to allow the devices to resolve to a single mode of operation using a predetermined priority resolution table.

The information is encapsulated within a burst of closely separated link integrity test pulses that meet 10baseT transmitter waveform for Link test pulses. This burst of pulses is referred to as a Fast Link Pulse (FLP) burst. The chip issues FLP bursts at powerup. The burst consists of alternating clock/data sequence.

To maintain interoperability with existing 10baseT devices, the alogrithm also supports the transmission of 10baseT compliant link integrity test pulses. 10baseT pulse is referred to as the Normal Link Pulse (NLP). A device which fails to respond to the FLP sequence and returns only the NLP indication is treated as a 10baseT compatible device.

Transmit Function

The FLP burst shall contain the Link Code Word (Reg4). FLP bursts consists of 33 pulse positions. The 17 odd numbered pulse positions are always present and represent clock information. The 16 even numbered positions represent data information. A link pulse present in an even numbered position represents a logic one and a link pulse absent from an even numbered pulse position represents a logic zero. The first pulse is a clock pulse. Clock pulses are evenly spaced apart by 125±30 microseconds. The data ONE pulse occurs 62.5±15 microseconds after the clock pulse. The first bit in consecutive FLP bursts shall occur at 16±8 msec interval. The pulses are sent through the TLP pin. A link pulse enable signal, LPEN, is also provided for convenience.

Receive Function

The receive function detects NLP sequence. In addition, the receive function shall detect FLP bursts and decode the information contained.

Arbitration Function

Arbitration function ensures proper sequencing of the autonegotiation algorithm through the transmit and receive function. The arbitration function enables the transmit function to advertise abilities and upon consistent and consecutive reception of the received link code word, advertises acknowledgement. Upon reception of 4 to 6 link code words with acknowledge bit set, the arbitration function determines the highest common denominator using the priority resolution table.

If SDO goes active before autonegotiation is complete, a test window timer will be started and at the expiration of the timer, the arbitration function shall indicate that a valid link has been established.

Table 3. Manual Setting for Non-Auto-Negotiation

Function	AUTO Bit (Reg0 Bit12)	Speed Bit (Reg0 Bit13)	Duplex Bit (Reg0 Bit8)
Auto-negotiation	1	X	X
100BaseT Full Duplex	0	1	1
100BaseT Half Duplex	0	1	0
10BaseT Full Duplex	0	0	1
10BaseT Half Duplex	0	0	0

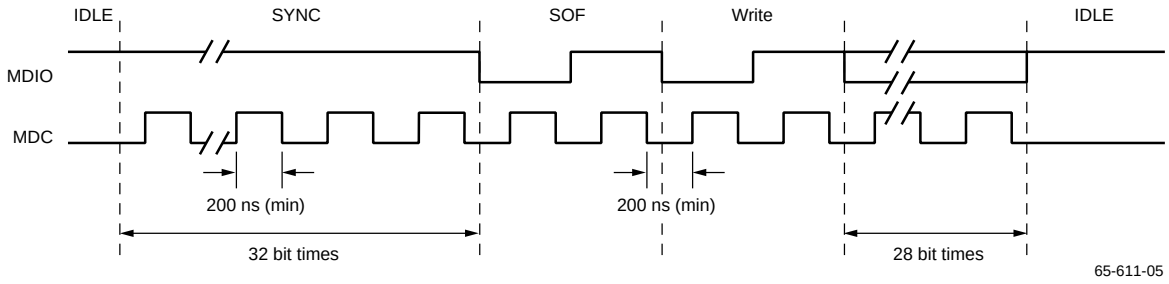


Figure 2. Management Interface Timing during Write to Registers

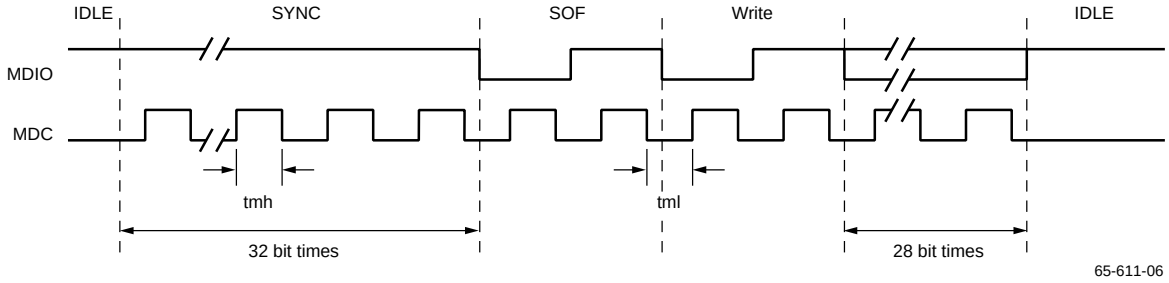


Figure 3. Management Interface Timing during Read from Registers

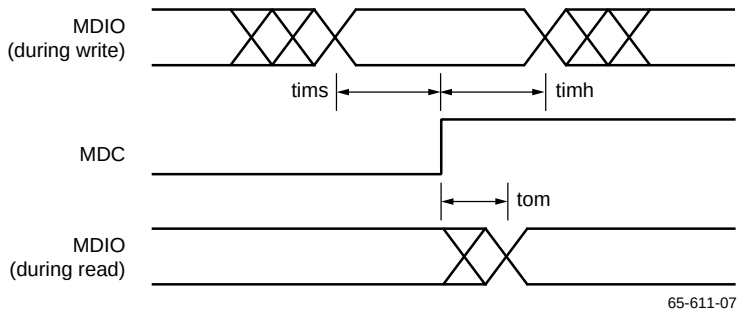


Figure 4.

Advanced Information

Register Definitions

Control Register (Read/Write) – Address 00000 (Register 0)

15	14	13	12	11	10	9	8
Reset	Loop	Speed	Auto	Pwrdn	Isolate	Reconfig	Duplex

7	6	5	4	3	2	1	0
Cltest	Reserved						

All of the control register bits (0 through 15) are read/write.

The functions within the Reg0 are as follows: speed, full/half duplex, Isolate, Automatic speed selection, Loopback, Collision test. The individual bit descriptions and the default values are as follows:

Reg	Bit	Name	Default	Description
0	15	Reset	O	Reset = 1 resets the PHY, i.e. all the control and status registers are reset to their default states. This function is self-clearing. The default value is zero. Writes to other bits of control register has no effect until the reset process is completed.
0	14	Loop	O	Loop = 1. This bit is used to enable the LOOP output pin HIGH and thereby enable the local loopback of the RCC611 through the RCC613. The default value is zero.
0	13	Speed	I	This bit is used to manually set the speed of operation. Speed=1 denotes 100 Mbps mode of operation. Speed=0 denotes 10 Mbps mode of operation. This bit is used to manually set the speed of operation. This bit is effective only if Auto (Reg0, bit 12)=0 (ie. manual speed selection). The default value is one. If bit12 (Auto) of Reg0=0, and Speed=0, 10Mbps operation is enabled and determined by Reg 1 bit 12 and bit 11. If bit12 (Auto) of Reg0=0 and Speed=1, 100 Mbps operation is enabled.
0	12	Auto	I	Auto = 1 denotes automatic speed selection. Auto=0 denotes manual speed selection. Auto speed selection enables PHY's auto selection algorithm. The default value = 1.
0	11	Pwrdn	O	Pwrdn = 1 shuts off the power to the chip except the portions involving the management transactions. The default value=0. Both Pwrdn & Pwrdn1 cannot be HIGH at the same time. If so, there will not be any power down.
0	10	Isolate	O	The chip isolates its data path from the parallel (MII) interface when Isolate=1. When Isolate=1, the chip will tristate the CMOS outputs: RXCLK, RXDV, ERROR, RXD3..RXD0, CLSN, & CRS. Also, the TTL inputs (DI0..DI3, TXEN, TXERR, TCLK) are ignored. The default value=0. If A(3..0)=0000, the default value=1. This bit is brought out as ISOLATE pin. This can be used to enable or disable an external additional PHY connected to the same controller.
0	9	Reconfig	O	Autolink configuration process will be initiated when Reconfig=1. This bit is self-clearing.
0	8	Duplex	O	When auto-configuration is disabled (Auto=0), Duplex=1 sets the chip for full duplex operation. In this mode, CRS signal is determined by receive activity. Duplex=0 sets the chip for half duplex operation. The default value of Duplex=0.
0	7	Cltest	O	When Cltest=1, CLSN is asserted in response to TXEN. The default value of Cltest=0.
0	6–0	Reserved	O	These bits are reserved for future definition. They are set equal to zero.

Register Definitions (continued)

Status Register (Read Only) – Address 00001 (Register 1)

15	14	13	12	11	10	9	8
0 (T4)	1 (TXFD)	1 (TXHD)	10TFD	10THD	0	0	0

7	6	5	4	3	2	1	0
0	0	Config	Rmtflt	1 (Auto)	Lnkstat	0 (Jabdet)	Extend

The status functions are as follows: information about all the modes of operation supported by the local PHY, the status of auto-negotiation, and if auto-negotiation is supported by the local PHY or not.

Reg	Bit	Name	Default	Description
1	15	T4	0	T4=1 indicates the mode is 100 base T4 capable. T4 is set to 0 for RCC611
1	14	TXFD	1	TXFD=1 indicates the mode is capable of full duplex transmission at 100 base TX. TXFD is set to 1 for RCC611
1	13	TXHD	1	TXHD=1 indicates the mode is capable of half duplex transmission at 100 base TX. TXHD is set to 1 for RCC611
1	12	10TFD	—	10TFD=1 indicates the local PHY has the ability to perform full duplex link transmission and reception using the 10baseT signalling specification. 10TFD=1 if the input pin EX10BTFD is equal to 1.
1	11	10THD	—	10THD=1 indicates the local PHY has the ability to perform half duplex link transmission and reception using the 100baseTX signalling specification. 10THD=1 if the input pin EX10BTHD is equal to 1.
1	10–6	Reserved	0	Bits10–6 are reserved for future definition. These bits are set to zero.
1	5	Config		When Config=1, it indicates that the auto link configuration has been completed and the Registers Reg4, Reg5 and Reg6 are valid. When Config=0, it indicates that the auto link configuration has not been completed. If control register bit 12 (Auto) =0, Config is set to zero.
1	4	Rmtflt		When Rmtflt=1, it indicates that a remote fault condition has been detected. This bit is set to 1 if Reg5 bit 13=1. This bit will remain set until read.
1	3	Auto	1	Auto=1 constitutes the ability of RCC611 to perform auto link detection and configuration. It is set to 1 to indicate that the local PHY has the ability to perform auto link detection and configuration.
1	2	Lnkstat		Lnkstat=1 indicates that the link is active. SDO going HIGH sets Lnkstat HIGH and SDO going HIGH to LOW causes Lnkstat to go HIGH to LOW. Lnkstat=0 indicates that the link is not valid. The occurance of a link failure condition will cause Lnkstat=0 and will remain equal to zero until read. It is set to 1 after read and remains set until the next occurence of SDO going HIGH to LOW.
1	1	Jabdet	0	This bit is set to 0 since jabber detect function is not supported.
1	0	Extend	1	Extend=1 indicates that the PHY provides extended set of capabilities which may be accessed through the extended register set, Reg2 through Reg6. The Extend bit is set to 1 for RCC611.

Register Definitions (continued)

PHY ID Register (Read Only) – Address 00010 (Register 2)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0000 0000 0000 0011															

PHY ID Register (Read Only) – Address 00011 (Register 3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
11 0001						00 0000 (Model)						0000 (Model Rev)			

Register 2 and Register 3 provide a 32-bit value which shall constitute a unique identifier for the PHY. Bits 15–0 of Register 2 and Bits 15–10 of Register 3 constitute the manufacturer ID (OUI). Bits 9–4 of Register 3 constitutes the vendor model and is set to zero. Bits 3–0 of Register 3 constitutes the vendor model version and is set to zero.

Link Advertisement Register (Read/Write) – Address 00100 (Register 4)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NP	Ack	RF	A7–A0								S4–S0				

Register 4 provides a 16-bit value used by the auto link configuration process. Bit 0 is the first bit to be transmitted followed by Bit 1, Bit 2–Bit 15.

Reg	Bit	Name	Default	Description
4	15	NP	0	Next Page (NP) bit is set to 1 to indicate that this node intends to advertise another Link code word. Otherwise, this bit is set to 0. This bit is set through the management interface. The default value is 0.
4	14	Ack	0	Acknowledge (ACK) field is used by the auto-negotiation algorithm to indicate that a station has successfully received its link partner's code word. If no next page (Reg4 bit15=0), this bit is set to 1 after the station has successfully received at least 3 consecutive and consistent Fast Link Pulse Bursts. If next page is to be sent as indicated by the NP bit, this bit is set to 1 after the node has successfully received at least 3 consecutive and consistent FLP bursts and read the current Link Code Word. When the ACK bit is set to 1, the Link Code Word shall be sent 6 times. Initially on powerup, before the auto-negotiation starts, ACK=0.
4	13	RF	0	Remote Fault (RF) is set to 1 to indicate to the link partner the presence of a fault. Otherwise, this bit shall be set to 0. This bit is set to 1 through the management interface. The default value is 0.
4	12–5	A7–A0	0	A7–A0 indicate the technological ability field. This field is used to indicate the supported technologies for each selector field value. The default value is 0. The bit assignments for various technologies are as follows: A0 10baseT A1 10baseT full-duplex A2 100baseTX A3 100baseTX full-duplex A4 100baseT4 A5–7 Reserved
4	4–0	S4–S0		S4–S0 is the selector field. It indicates the type of message that is being sent. For IEEE802.3, S4–S0=00001.

Register Definitions (continued)

Link Partner Register (Read Only) – Address 00101 (Register 5)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NP	Ack	RF	A7–A0								S4–S0				

Register 5 is the link partner's advertised capability register. The fields are same as those of Register 4. Upon successful completion of the auto-negotiation as indicated by Register 1/Bit 5 set to 1, Register 5 has valid information about the advertised ability of the link partner's PHY.

Expansion Register (Read Only) – Address 00110 (Register 6)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											PDF	LPNP	1	Pg Rcvd	LP Able

Reg	Bit	Name	Description
6	15–5	Reserved	Bits 5 through 15 of Register 6 are reserved for future expansion.
6	4	PDF	PDF = 1 indicates a fault has been detected via the Parallel Detection function. Default = 0.
6	3	LPNP	LPNP indicates that the link partner supports the Next Page function.
6	2	NP Able	NP Able indicates local device is Next Page able. It is set to 1.
6	1	Pg Rcvd	Pg rcvd bit is a status bit and indicates that 3 identical and consecutive link code words have been received. This bit is auto clear on read.
6	0	LP Able	LP Able indicates that the Link Partner is able to participate in the auto-negotiation algorithm.

Advanced Information

Register Definitions (continued)

Next Page Register (Read/Write) – Address 00111 (Register 7)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NP	Ack	MP	Ack2	M11/U11–M0/U0											

This next page register is a control register used to convey information beyond that of the base page. All the bits except Ack are written through the management interface.

Reg	Bit	Name	Description
7	15	NP	It is set to 1 to indicate that this node intends to advertise another next page. Otherwise, this bit is set to 0. The default value is 0.
7	14	Ack	Acknowledge (Ack) field is used by the auto-negotiation algorithm to indicate that a station has successfully received the link partner's next page. If no next page (Register 7, Bit 15=0), this bit is set to 1 after the station has successfully received at least 3 consecutive and consistent Fast Link Pulse Bursts. If next page is to be sent as indicated by the NP bit, this bit is set to 1 after the node has successfully received at least 3 consecutive and consistent FLP bursts and read the current Link Code Word. When the ACK bit is set to 1, the Link Code Word shall be sent 6 times. Initially on powerup, before the auto-negotiation starts, Ack=0.
7	13	MP	Message Page (MP). This field is used to differentiate the next page to be message page or the unformatted page. If MP=1, the next page is a message page. If MP=0, the message page is unformatted. Any unformatted page shall be preceded by a message page.
7	12	Ack2	Acknowledge2 (Ack2). If Ack2=1, the station has the ability to comply with the received next page. If Ack2=0, the station will not comply with the message.
7	11–0	M11/U11–M0/U0	This is the 12 bit encoded message or unformatted message depending on MP being 1 or 0 respectively.

User Control/Status Register (Read/Write) – Address 10000 (Register 16)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				Rsvd	Reserved										Pwrdn1

This register is used for additional control & status which are user specific. The additional functions are as follows:

Reg	Bit	Name	Description
16	15–12	Reserved	Bits 12 through 15 are reserved for future use.
16	11	Reserved	Flow Control Enable. This bit is used to enable flow control signalling mechanism inside the chip.
16	10–1	Reserved	Flow Control Symbols. This is a user-assigned symbol pair that is used to communicate the flow control information to the other communicating node. Do not write JK code combination (1100010001) into this set of bits.
16	0	Pwrdn1	In this mode, link signalling is enabled during powerdown.

Advanced Information

Absolute Maximum Ratings[1]

Parameter	Min	Max	Unit
Storage Temperature Range	-65	150	°C
Junction Temperature Range	-55	150	°C
Lead Temperature Range (soldering, 10 seconds)		300	°C
Positive Power Supply, VCC, ATXVCC, ARXVCC	0	6	V
Voltage applied to any TTL inputs	-1	6	V
Voltage applied to any PECL inputs	-1	6	V
Voltage applied to any CMOS outputs	-1	6	V
Voltage applied to any PECL outputs	-1	6	V
Current from any CMOS outputs	-50	50	mA
Current from any PECL outputs	-50	50	mA

Note:

1. "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. If the device is subjected to the limits in the absolute maximum ratings for extended periods, its reliability may be impaired. The tables of Electrical Characteristics provide conditions for actual device operation.

Operating Conditions

Parameter		Min	Typ	Max	Units
Ta	Ambient Operating Temperature	0		70	°C
VCC	Positive Supply Voltage (DVCC and AVCC)	4.75	5.0	5.25	V
RI	PECL Differential Load Resistance (Note 1)	80	100	120	Ω

Note:

1. Differential load resistance of 100 Ω equals 50 Ω to AC ground on each of DOUT, $\overline{\text{DOUT}}$.

Advanced Information

DC Electrical Characteristics

AVCC, DVCC = 5V±5%, GND=0V, unless otherwise indicated.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Transmitter Section						
Vihc	TTL input Voltage HIGH		2.0		VCC+0.5	V
Vilc	TTL input Voltage LOW		0		0.8	V
Iinc	TTL Input Current		-1		100	µA
Ci	Input Capacitance			4	10	pF
Vohp	PECL Output Voltage HIGH	Rdiff=100Ω, VCC=5V	3.5	3.8	4.2	V
Volp	PECL Output Voltage LOW	Rdiff=100Ω, VCC=5V	2.6	3.0	3.4	V
Vop	PECL Output Voltage amplitude	Vohp-Volp, VCC=5V	0.6	0.8	1.0	V
Iolp	PECL Output Current HIGH			8		mA
Receiver Section						
Vihc	TTL input Voltage HIGH		2.0		+5.5	V
Vilc	TTL input Voltage LOW		0		0.8	V
Iinc	TTL Input Current		-1		1	µA
Vcm	Com. Mode Range (DIN,$\overline{\text{DIN}}$)		2		5	V
Vdiff	Diff. Input Voltage (DIN, $\overline{\text{DIN}}$)		0.2		5.5	V
Iip	PECL Input Current		-1		1	µA
Vohc	Output Voltage HIGH		3.5		VCC	V
Volc	Output Voltage LOW		0		0.5	V
Iolc	Output Current LOW		4			mA
Iohc	Output Current HIGH		4			mA
ICC	Power Supply Current			120		mA
PD	Power Dissipation			600		mW

Advanced Information

AC Electrical Characteristics

AVCC, DVCC = 5V±5%, GND = 0V, unless otherwise indicated

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Transmitter Section						
Tt1	TCLK Period			40		ns
Tch	TCLK Pulse Width HIGH		15			ns
Tcl	TCLK Pulse Width LOW		15			ns
tids	DIN0–DIN7,TXEN,TXERR to TCLK ↑ setup time		4			ns
tidh	TCLK ↑ to DIN0–3, TXEN,TXERR hold time		4			ns
tr, tf	DOUT, $\overline{\text{DOUT}}$ rise and fall times	10% to 90% points			2	ns
ttj	DOUT, $\overline{\text{DOUT}}$ total pk-pk jitter				1.4	ns
tdj	DOUT, $\overline{\text{DOUT}}$ pk-pk duty cycle distortion				500	ps
Receiver Section						
fcc	Input Data Rate Variation				±1000	ppm
D	Input Data Transition Density to Acquire and Maintain Lock		0.1			ppm
n	Maximum run length of consective 1's or 0's before loss of lock		60			bits
tacq	Loop Acquisition Time for 10E-12 BER				1000	bits
tri, tfi	DIN, $\overline{\text{DIN}}$ input rise and fall time				1	ns
tj	DIN, $\overline{\text{DIN}}$ input peak to peak jitter tolerance				0.075T	ns
tod	RCLK ↓ to DO0–DO3, RXDV valid				10	ns
Tr1	RCLK period			40		ns
Trh	RCLK pulse width HIGH		0.35Tr1	0.4Tr1	0.45Tr1	ns
Management Section						
Tmh	MDC pulse width HIGH		200			ns
Tml	MDC pulse width LOW		200			ns
tims	MDIO to MDC ↑ setup		5			ns
timh	MDIO to MDC ↑ hold		5			ns
tom	MDC ↑ to MDIO				15	ns

Note:

1. Test conditions (unless otherwise indicated:) PECL Input rise and fall times ≤1ns, RL = 100Ω (differential), RL = 50Ω (single-ended). TTL Input rise and fall times ≤15ns. Transition density ≥ 0.1.

Advanced Information

TIming Diagrams

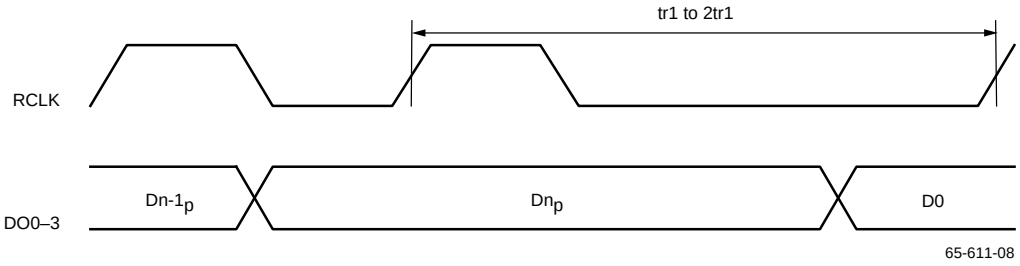


Figure 5. Receiver Timing—New Alignment

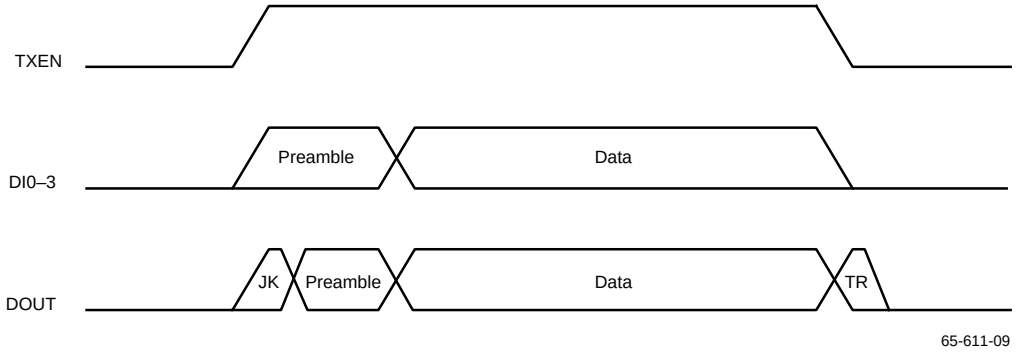


Figure 6. Frame Sequence—Transmit

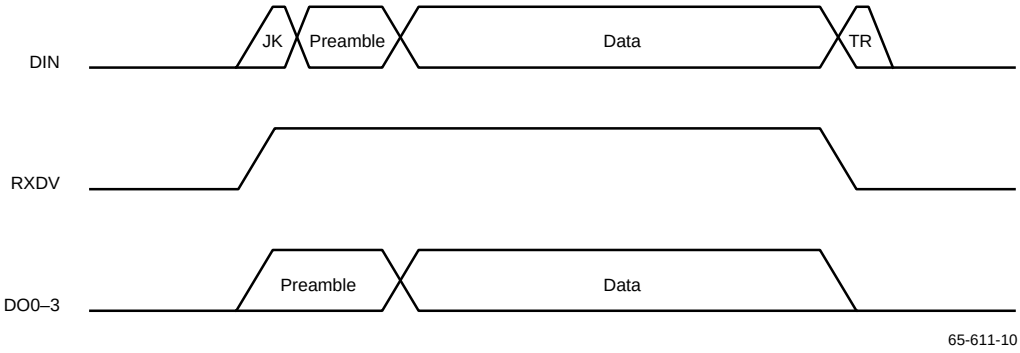


Figure 7. Frame Sequence—Receive

Advanced Information

Timing Diagrams (continued)

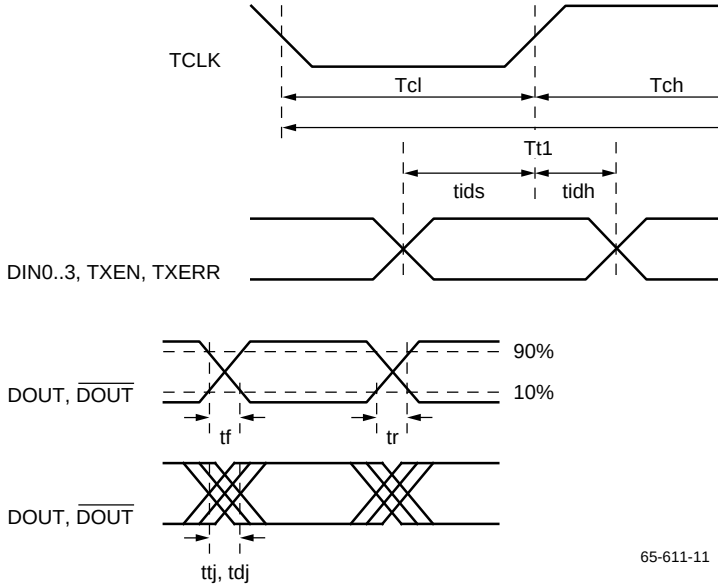


Figure 8. Transmitter Timing

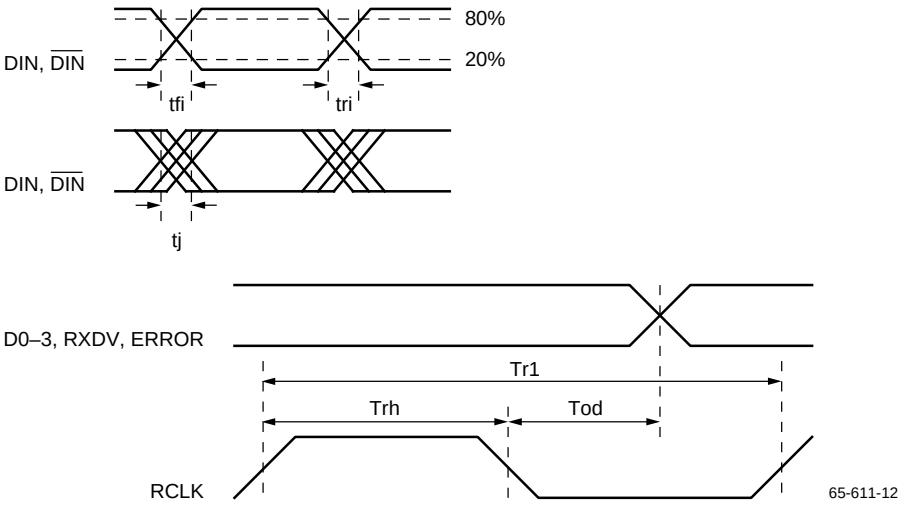


Figure 9. Receiver Timing

Advanced Information

Applications Discussion

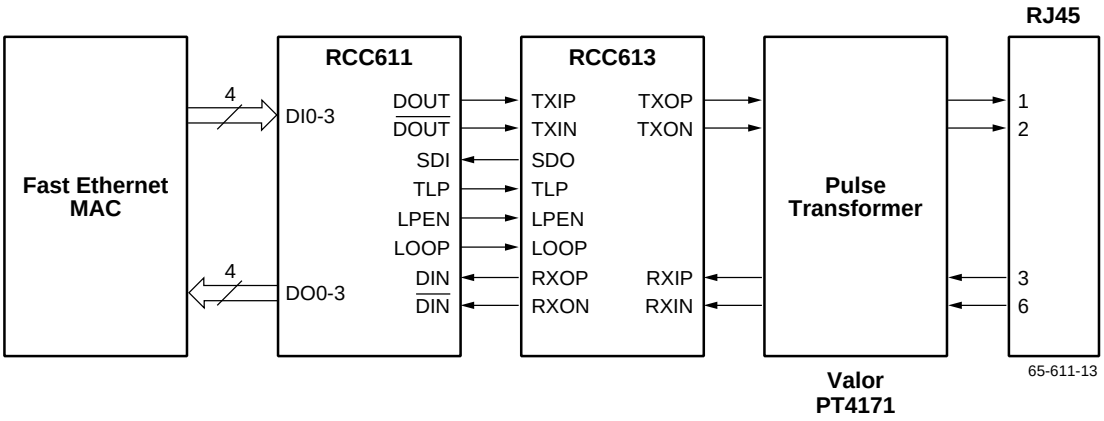


Figure 10. Typical Application

Advanced Information

Notes:

Notes:

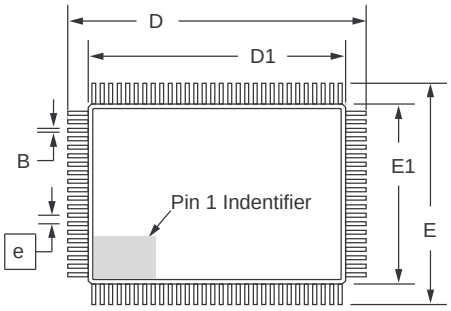
Mechanical Dimensions

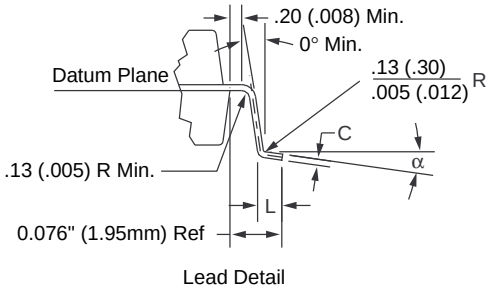
100 Lead MQFP 14x20mm Package—3.9mm Footprint

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.134	—	3.40	
A1	.010	—	.25	—	
A2	.100	.120	2.55	3.05	
B	.008	.015	.22	.38	3, 5
C	.005	.009	.13	.23	5
D	.922	.942	23.65	24.15	
D1	.783	.791	19.90	20.10	
E	.688	.708	17.65	18.15	
E1	.547	.555	13.90	14.10	
e	.0256 BSC		.65 BSC		
L	.028	.040	.73	1.03	4
N	100		100		
ND	30		30		
NE	20		20		
α	0°	7°	0°	7°	
ccc	—	.005	—	.12	

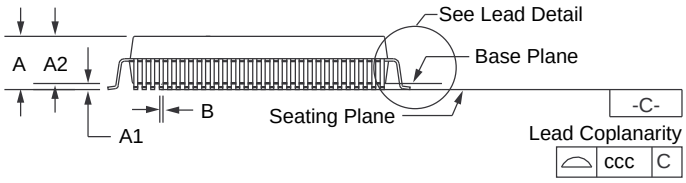
Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Controlling dimension is millimeters.
3. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be .08mm (.003in.) maximum in excess of the "B" dimension. Dambar cannot be located on the lower radius or the foot.
4. "L" is the length of terminal for soldering to a substrate.
5. "B" & "C" includes lead finish thickness.





Lead Detail



Advanced Information

Ordering Information

Product Number	Package
RCC611KR	100 Lead MQFP

Advanced Information

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RCC611

100BaseTX Transceiver

Features

- 100 Mbps/125 Mbaud data rates
- Low power 0.6 micron CMOS technology
- PLL Clock and data recovery
- Clock synthesizer
- Auto-negotiation
- 4b/5b Encode/Decode
- FDDI TP/PMD scrambling/descrambling
- Management Interface for control/status
- Link Pulse Signalling
- Conforming to MII interface of IEEE 100baseTX Fast Ethernet Standard(P802.3u/D3)
- Low Power Dissipation—600 mW typical
- Single power supply: +5V
- PECL compatible serial data inputs/outputs
- Support for external 10 Mbps PHY
- 100 pin PQFP (20mm x 14mm x 2.7 mm)

Applications

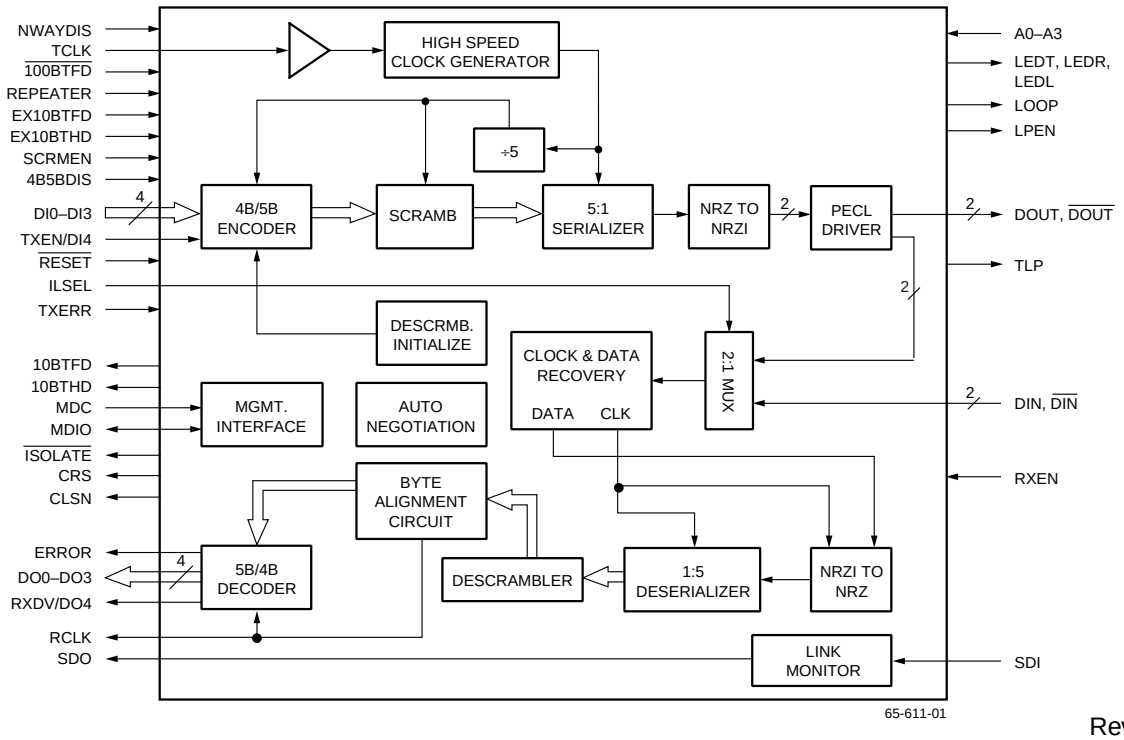
- Fast Ethernet Adapter/hub/switch
- FDDI Adapter/hub
- High Speed Point to Point Links
- Bus Extenders
- Multimedia
- High Resolution Graphic Displays
- Fast Ethernet test equipment
- FDDI Test Equipment

Description

The RCC611 is a monolithic 125 Megabaud CMOS transceiver chip. It integrates a complete phase-locked loop clock and data recovery, a phase locked loop clock synthesizer, a 5:1 Serializer, a 1:5 Deserializer, 4B/5B Encoder, 5B/4B Decoder, auto-negotiation and a management interface for link control and status. It also includes scrambler, descrambler for twisted pair copper applications in compliance with FDDI TP-PMD specifications. In conjunction with RCC613 twisted pair transceiver, the chipset can be used for driving with category 5 unshielded twisted pair cable and Type 1 shielded twisted pair cable. The chip also can be used to directly interface to fiber optic transceiver for FDDI and 100base-FX applications. The chip meets the physical layer interface requirements of the 100 Base-X Fast Ethernet and FDDI standards. The RCC611 chip operates with a single, +5V power supply.

Advanced Information

Block Diagram



Rev. 0.5.3

Advanced Information

Functional Description

Transmitter Section

The RCC611 transmitter section includes a phase locked loop synthesizer, 4B/5B encoder, scrambler and 5:1 serializer.

The RCC611 accepts a CMOS data nibble (DI0-DI3) and a control bit, TXEN. The data gets strobed on the positive transition of TCLK. The transmitter encodes the data, DI0-DI3 using 4b/5b coding (see Table 1). TXEN is used to denote the transmitter input being active or not. Whenever TXEN=0, IDLE symbol (11111) is encoded and transmitted. When TXEN transitions from 1 to 0, TR byte is sent before transmitting IDLE symbols. The order of transmission of the 4b/5b encoded output (E4..0)is that the most significant bit of the encoded symbol, E4 is transmitted first followed by E3,E2,E1 and E0.

When 4B5BDIS is HIGH, the 4b/5b encoder is bypassed. Under that case, TXEN is used as the fifth bit (DI4) of the encoded symbol. The order of transmission of the input when 4B5BDIS is HIGH is DI4 followed by DI3, DI2, DI1 and DI0.

The clock generator consists of a frequency multiplying Phase Locked Loop (PLL). The multiplying ratio is 5. The serial output goes through Non-Return-to-Zero (NRZ) to Non-Return-to-Zero Invert on Ones (NRZI) conversion. The NRZ to NRZI converter takes in the serial NRZ stream and puts out a transition for every 1 in the input stream. For zeros, there will be no transition. This will ensure that there is clocking information even when there is a long stream of 1s. The differential NRZI output is enabled to the output pins DOUT, $\overline{\text{DOUT}}$. The serial Data Stream (DOUT/ $\overline{\text{DOUT}}$) is transmitted at PECL levels (positive shifted ECL levels, Vth= +3.7 V). The input clock reference for the PLL Clock Generator, TCLK, typically comes from the CMOS protocol layer IC. TXERR=1 is used to force HALT symbol (00100) on the transmit output.

When SCRMEN is HIGH, the encoded symbol is scrambled as per FDDI's TP-PMD standard. The scrambler used is a stream cipher scrambler. The scrambler polynomial is $1+x^{9}+x^{11}$.

Descrambler Initialization

The descrambler initialization timing is shown in the accompanying diagram. On powerup, TXEN=0. RCC611 under that case, if SCRMEN=1, automatically initializes the downstream descrambler by forcing IDLE symbols (11111) which gets scrambled and driven to the medium. Transmitting IDLE continues until TXEN=1.

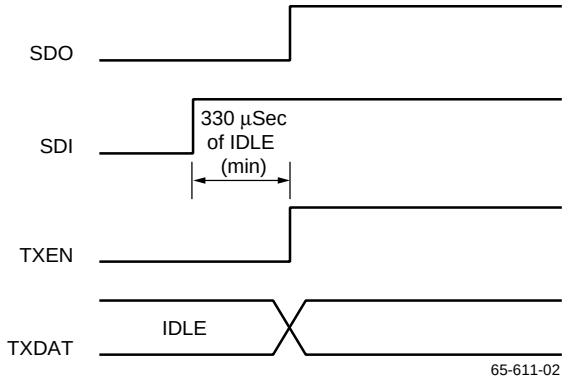


Figure 1.

The transmitter has the provision to loopback its output to the receiver input, when ILSEL=1. Under that case, a continuous logic LOW state is sent through the DOUT, $\overline{\text{DOUT}}$ pins.

There is also one more level of loopback provided through the external RCC613 chip. When control register Reg0 bit 14 is HIGH, LOOP output pin is HIGH and the the serial output, DOUT, $\overline{\text{DOUT}}$ goes through the RCC613 TXIP, TXIN inputs and loops back through the RXOP, RXON outputs back to the DIN, $\overline{\text{DIN}}$ of RCC611.

Table 1. 4B/5B Encoding

Symbol	TXEN	DI3–DI0	Encoded Output (E4-E0)
0	1	0000	11110
1	1	0001	01001
2	1	0010	10100
3	1	0011	10101
4	1	0100	01010
5	1	0101	01011
6	1	0110	01110
7	1	0111	01111
8	1	1000	10010
9	1	1001	10011
A	1	1010	10110
B	1	1011	10111
C	1	1100	11010
D	1	1101	11011
E	1	1110	11100
F	1	1111	11101
T	0	xxxx	01101
R	0	xxxx	00111
J	1	xxxx	11000
K	1	xxxx	10001

Table 1. 4B/5B Encoding (continued)

Symbol	TXEN	DI3–DI0	Encoded Output (E4-E0)
I (IDLE)	0	xxxx	11111
H (HALT)	1	xxxx	00100

Note:
1. All the symbols are encoded as per the state diagram provided in Chapter 28 of IEEE802.3.

Table 2. 5B/4B Decoding

Symbol	Encoded Output	DO3–0	ERROR
0	11110	0000	0
1	01001	0001	0
2	10100	0010	0
3	10101	0011	0
4	01010	0100	0
5	01011	0101	0
6	01110	0110	0
7	01111	0111	0
8	10010	1000	0
9	10011	1001	0
A	10110	1010	0
B	10111	1011	0
C	11010	1100	0
D	11011	1101	0
E	11100	1110	0
F	11101	1111	0
T	01101	xxxx	0
R	00111	xxxx	0
J	11000	xxxx	0
K	10001	xxxx	0
I	11111	xxxx	0
H	00100	xxxx	1
V	00000	xxxx	1
V	00001	xxxx	1
V	00010	xxxx	1
V	00011	xxxx	1
V	00101	xxxx	1
V	00110	xxxx	1
V	01000	xxxx	1
V	01100	xxxx	1

Table 2. 5B/4B Decoding (continued)

Symbol	Encoded Output	DO3–0	ERROR
V	10000	xxxx	1
V	11011	xxxx	1

Note:
1. All the symbols are decoded as per the state diagram provided in Chapter 28 of IEEE802.3.

Receiver Section

The RCC611 Receiver section includes a 2 to 1 multiplexer, a complete phase-locked loop clock and data recovery, and decoder. For twisted pair cable applications, the descrambler function is enabled when SCRMEN pin is HIGH.

The 2 to 1 Mux is used to choose between the differential PECL receive input data (DIN, $\overline{\text{DIN}}$) or the transmit output for enabling to the clock and data recovery circuit. The choice of the inputs is made by the ILSEL pin. If ILSEL is HIGH, the transmit output is looped back to the input of the receiver. If ILSEL is LOW, the receive input is chosen.

The RCC611 recovers the clock and regenerates the encoded serial data. There is a PECL to CMOS converter for the SDI signal detect PECL input signal. If SDI goes LOW to HIGH, the SDO output goes HIGH after a minimum of 330 microseconds of continuous IDLE symbols to allow for the clock and data recovery and descrambler to synchronize.

The recovered encoded data is then converted to 5 parallel data lines via 1:5 De-Serializer.

The RCC611 contains a byte alignment circuitry. When the JK symbols are detected in the serial stream, the chip will automatically resynchronize the demultiplexer to byte align with the JK.

The data is then decoded into an 4-bit symbol via the 5b/4b decoder as per the 5b/4b Decoding table. The received data is checked during the 5b/4b decoding and violations are flagged by bringing the Error Flag (ERROR) to a level HIGH. The 5b/4b decoder is bypassed for FDDI.

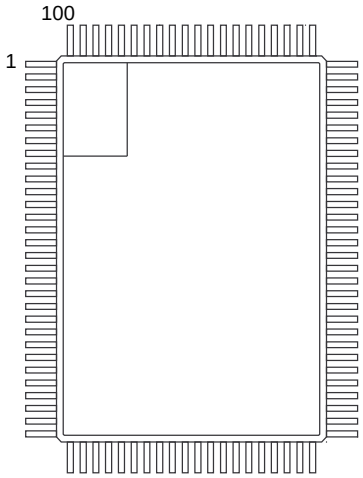
The output from the 5b/4b decoder comes out as 4 bits of data, DO0–DO3 and one control bit output, RXDV. When 4B5BDIS is HIGH, the 5b/4b decoder is bypassed and the output come out as DO0-DO4 where DO4 replaces the RXDV signal.

The demultiplexed data goes through a descrambler if SCRMEN=1. The descrambler descrambles the data as per the polynomial discussed in the transmit section.

CLSN signal is flagged if the chip is transmitting and receiving data as per the IEEE802.3 transmit and receive state diagram in Chapter 24. CRS is flagged if either the chip is transmitting data or receiving data as per the IEEE802.3 transmit and receive state diagram in Chapter 24. Both CLSN and CRS are asynchronous signals.

Advanced Information

Pin Assignments



Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	DGND	26	DVCC	51	LPEN	76	DVCC
2	DGND	27	$\overline{\text{RESET}}$	52	RXEN	77	NC
3	DVCC	28	LEDT	53	DGND	78	NC
4	DVCC	29	$\overline{\text{ISOLATE}}$	54	DGND	79	NC
5	NC	30	LEDR	55	DO3	80	NC
6	AGND	31	LEDL	56	DO2	81	DIN
7	DGND	32	DVCC	57	DO1	82	$\overline{\text{DIN}}$
8	4B5BDIS	33	DGND	58	DO0	83	NC
9	DI0	34	A0	59	DVCC	84	SDI
10	DI1	35	A1	60	DVCC	85	DGND
11	DI2	36	A2	61	RXDV/DO4	86	AGND
12	DI3	37	A3	62	ERROR	87	RXAVCC
13	TXEN/DI4	38	DGND	63	DGND	88	AGND
14	TXERR	39	DGND	64	RCLK	89	RXAVCC
15	DGND	40	10BTFD	65	SDO	90	TXAVCC
16	TCLK	41	10BTHD	66	AGND	91	AGND
17	DVCC	42	EX10BTHD	67	DGND	92	DGND
18	REPEATER	43	EX10BTFD	68	DVCC	93	DVCC
19	SCRMEN	44	CLSN	69	DGND	94	TXAVCC
20	MDC	45	CRS	70	DGND	95	TXAVCC
21	MDIO	46	$\overline{\text{100BTFD}}$	71	DVCC	96	AGND
22	LOOP	47	TLP	72	DVCC	97	AGND
23	NC	48	DVCC	73	DGND	98	ILSEL
24	NC	49	DVCC	74	DGND	99	$\overline{\text{DOUT}}$
25	DGND	50	NWAYDIS	75	DVCC	100	DOUT

Pin Descriptions

Pin Name	Pin Number	Type	Description
10BTFD	40	CMOS O/P	**10BaseT Full Duplex.**10BTFD is used to enable or disable a local 10BaseT Full duplex device.
10BTHD	41	CMOS O/P	**10BaseT Half Duplex.** 10BTHD is used to enable or disable a local 10BaseT half duplex physical layer device.
4B5BDIS	8	TTL I/P	**4b/5b disable.** This pin is used to disable the 4b/5b encoder and 5b/4b decoder.
A0–A3	34–37	TTL I/P	**Address 0–3.** A0–A3 pins are used to denote the physical address of the chip for writing or reading of the internal control/ status registers. During reset, if the PHY address are all zeroes (0000) then the MII interface will be tri-stated.
AGND	6, 66, 86, 88, 91, 96, 97		**Chip ground for Analog circuitry.** AGND pins should be connected to the printed circuit board's ground plane at the pins.
CLSN	44	CMOS O/P	**Collision.** This output is HIGH if the chip is receiving data and at the same time it is transmitting packet data. It is an asynchronous output. CLSN is LOW during Full duplex mode of operation.
CRS	45	CMOS O/P	**Carrier Sense.** This output is HIGH if the chip is either receiving data or transmitting packet data. It is an asynchronous output. CRS is determined by receive activity during Full duplex mode.
DGND	1, 2,7,15, 25, 33, 38, 39, 53, 54, 63, 67, 69, 70, 73, 74, 85, 92		**Chip ground for digital circuitry.** DGND should be connected to the printed circuit board's ground plane at the pins.

Advanced Information

Pin Descriptions (continued)

Pin Name	Pin Number	Type	Description
DIN, $\overline{\text{DIN}}$	81, 82	PECL I/P	**Receiver differential input data.**
DO0–DO3	58-55	CMOS O/P	**Receiver output data.**
DOUT, $\overline{\text{DOUT}}$	100, 99	PECL O/P	**Transmit differential output data.**
DVCC	3, 4, 17, 26, 32, 48, 49, 59, 60, 68, 71, 72, 75, 76, 93		**Positive supply for Digital circuitry.** The nominal value is 5V ±5%. VCC should be bypassed to the ground plane with a 0.1µF chip capacitor placed as close to the pin as possible.
DI0–DI3	9-12	TTL I/P	**Transmitter Input data.**
ERROR	62	CMOS O/P	**Error Flag.** ERROR goes HIGH to flag 5B/4B decoding violations. It also indicates transition to idle condition from active without end of frame delimiters.
$\overline{\text{100BTFD}}$	46	CMOS O/P	**100BaseT Full Duplex.** $\overline{\text{100BTFD}}$ when low is used to activate a LED and indicates that the RCC611 is operating in the 100BaseT Full Duplex mode.
EX10BTFD	43	TTL I/P	**10BaseT Full Duplex.** When EX10BTFD is high, it indicates that there is available an external 10BaseT Physical layer device capable of full duplex operation. This input goes directly to Reg1 bit12.
EX10BTHD	42	TTL I/P	**10BaseT Half Duplex**. When EX10BTHD is high, it indicates that there is available an external 10BT physical layer device with half duplex capability. This input goes directly to Reg1 bit11.
$\overline{\text{ISOLATE}}$	29	CMOS O/P	**Isolate.** $\overline{\text{ISOLATE}}$ is used to indicate that the chip is in the isolate mode. When activated (low), all the MII interfaces will be tri-stated. Software can be used to override the the $\overline{\text{ISOLATE}}$ bit (Reg0 bit10). Note that the polarity of $\overline{\text{ISOLATE}}$ and Reg0 bit10 are the opposite to each other. See page 10 for more details.
LEDL	31	CMOS O/P	**LED Link OK.** It is used as an active LOW output to indicate that the link is OK as indicated by the FLG signal from the arbitration state machine.
LEDR	30	CMOS O/P	**LED Receive.** It is used as an active LOW output to indicate that the receive is active. It will be LOW if CRS=1.
LEDT	28	CMOS O/P	**LED Transmit.** It is used as an active LOW output to indicate that the transmit is active. It will be LOW if TXEN=1.
LOOP	22	CMOS O/P	**Loop.** LOOP is used to enable the loopback input of RCC613 chip. LOOP is active if the control register Reg0 bit 14 is HIGH .
LPEN	51	CMOS O/P	**Link Pulse Enable.** It provides an enable signal to the RCC613 for the transmit link pulse.
ILSEL	98	TTL I/P	**Loop Select.** ILSEL is used for differential loopback for "on-board" diagnostic of the device. When ILSEL is HIGH, the receiver accepts the serial output data from the transmitter section. Connect to GND or leave open when not used.
MDIO	21	TTL/CMOS I/O	**Management Data Input/Output.** MDIO is a bidirectional signal between RCC611 and the station management entity. It is used to transfer control and status information. All the read and write transactions are done synchronously with MDC.
MDC	20	TTL I/P	**Management Data Clock.** MDC is sourced by the station management entity to RCC611 as a timing reference for transfer of information on MDIO signal. MDC is an aperiodic signal whose minimum high and low times are 200 ns.

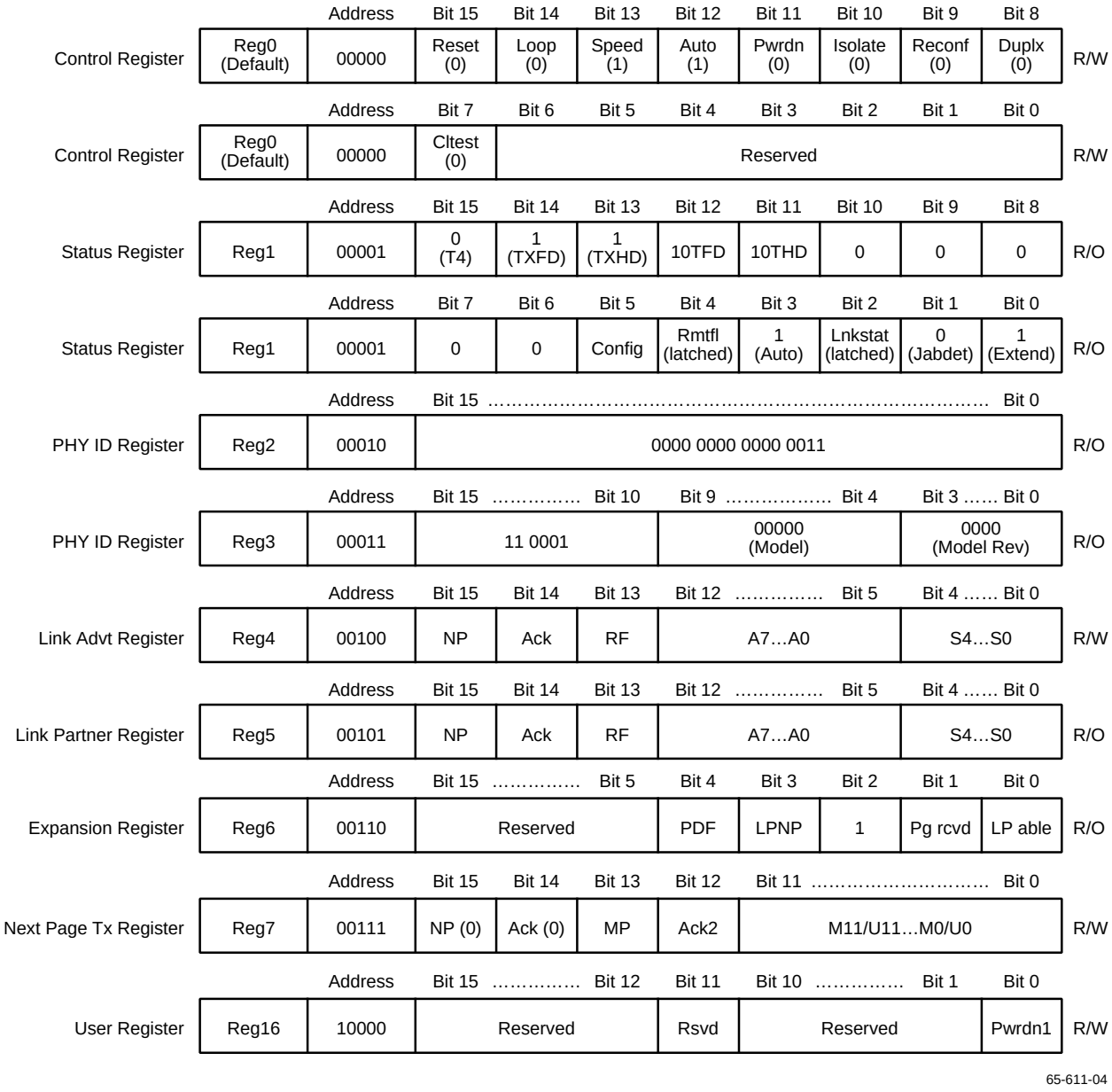
Advanced Information

Pin Descriptions (continued)

Pin Name	Pin Number	Type	Description
NWAYDIS	50	TTL I/P	**Nway Disable.** When NWAYDIS is high, the auto-negotiation state machines are disabled and AUTO bit (Reg0 bit12) is set to 0. Software can be used to override the AUTO bit. see page 10 for more details. For manual setting, see Table 3.
RCLK	64	CMOS O/P	**Receive Clock.** It is the recovered byte clock derived from the byte alignment circuitry. It provides timing to DO0–DO3, RXDV and ERROR.
REPEATER	18	TTL I/P	**Repeater/Node Mode.** When in the Repeater (high) mode as in the Full Duplex mode, CRS output is asserted due to activity from the receiver only. When in the Node (low) mode and not Full Duplex mode, CRS is asserted due to either receive or transmit activity.
$\overline{\text{RESET}}$	27	TTL I/P	**Reset.** RESET is an asynchronous input which when LOW is used to reset the state machines inside the chip. RESET needs to be LOW for at least one byte clock.
RXEN	52	TTL I/P	**Receive Enable.** When activated (high), it enables the outputs D0-D3, CRS, ERROR, RXDV, CLSN and RCLK. When low these outputs are tri-stated.
RXAVCC	87,89		**Positive Supply for Receive Analog Circuitry.** The nominal value is 5V±5%. RXAVCC should be bypassed to the ground plane with a 0.1µF chip capacitor placed as close to the pin as possible.
RXDV/DO4	61	CMOS O/P	**Receive Data Valid.** RXDV when HIGH indicates the receive output data being active. When 4B5BDIS is HIGH, this pin is used as DO4, the fifth data output.
SCRMEN	19	TTL I/P	**Scrambler Enable.** Scrmen when HIGH is used to enable the scrambler and descrambler.
SDI	84	PECL I/P	**Signal Detect Input.** It is converted to CMOS output level through a PECL to CMOS converter.
SDO	65	CMOS O/P	**Signal Detect Output.** SDO is the output from the PECL to CMOS converter for the signal detect signal. The signal is asserted 330 microseconds after SDIN goes HIGH. SDO output is made synchronous to RCLK and has the same timing as the DO0–3.
TCLK	16	TTL I/P	**Transmit Clock.** TCLK is the 25 MHz input reference for the internal high speed bit clock generator. It provides the timing for the input data, DI0..DI3, TXEN and TXERR.
TLP	47	CMOS O/P	**Transmit Link Pulse.** TLP is HIGH when a link pulse needs to be transmitted.
TXAVCC	90, 94, 95		**Positive supply for Transmit Analog circuitry.** The nominal value is 5V ±5%. TXAVCC should be bypassed to the ground plane with a 0.1µF chip capacitor placed as close to the pin as possible.
TXEN/DI4	13	TTL I/P	**Transmit Enable .** WhenTXEN is HIGH, it indicates that the input data is active. When 4B5BDIS is HIGH, this pin is used as DI4, the fifth data input.
TXERR	14	TLL I/P	**Transmit Error.** TXERR is used to transmit VIOLATION symbols (00100) on the transmit output.

Advanced Information

Management Interface



65-611-04

Register Description

The management interface provides a simple, two wire, serial inteface (MDIO, MDC) to connect the station management entity to the PHY for control and status gathering. MDC is sourced by the station management entity to the PHY as a timing reference for transfer of information on the MDIO signal. MDC is an aperiodic signal with a minimum high and low times of 200 ns. MDIO is a bidirectional signal between PHY and the station management entity. Control information is driven by the station management entity synchronously to MDC and sampled synchronously by PHY. Status information is driven synchronously by PHY and sampled synchronously by the station management. As shown in the figure, there are a total of 9 sixteen bit registers: Reg0, Reg1, through Reg7 and Reg16. Their functions are detailed in the register definitions section. The default values for the registers where applicable are shown in parenthesis. All the status and control transistions occur synchronous to the local clock, TCLK.

Advanced Information

	Idle	SOF	OpCd	PHY Addr	Reg Addr	Fill	Data
Read:	Idle	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD
Write:	Idle	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD

Management Frame Structure

Management Frame Structure

The management frame structure is as shown in the figure. In between the frames is an Idle condition. The Idle condition on the two wire interface is a logic one through the internal pullup resistor. The open drain driver for MDIO will be disabled. Prior to initiating any transaction, the station management entity will send a sequence of 32 contiguous logic one bits on MDIO with 32 corresponding cycles on MDC to provide the chip with a pattern that it can use to establish synchronization.

The frame begins with an SOF field. SOF is indicated by a 01 pattern. The next field is Opcode. The Opcode for a read transaction is 10 and for a write transaction is 01. Next to Opcode is the PHY Address field. The PHY address is 5 bits. The first bit is the most significant bit of the PHY address. The chip will recognize 00000 as its own address. The next field is the register address. The register address is 5 bits. The register accessed at register address zero (00000) is the Register 0 (Reg0) and so on.

Next to the Register address is the Turnaround field. An idle bit time during which no device actively drives the MDIO signal is inserted between the Register address field and the Data field of the frame during a Read transaction in order to avoid contention. During a Read transaction, the chip will drive a zero bit onto MDIO for the bit time following the idle bit and preceding the Data field. During a write transaction, the station management entity will fill this idle time with a one bit followed by a zero bit. The data field is 16 bits. The first data bit transmitted and received is the MSB of the data payload.

Auto-Negotiation Signalling

The chip has the provision to advertise its mode of operation to the remote end of a link segment and detect corresponding operational modes that the other device may be advertising. The auto-negotiation algorithm is performed out of band using a modified 10baseT link integrity pulse sequence. The algorithm allows the devices at both ends of a link segment to request and acknowledge use of the commom modes of operation that both devices share and to reject the use of operational modes that are not shared by both devices. When more than one common mode exists between the two devices, a mechanism is provided to allow the devices to resolve to a single mode of operation using a predetermined priority resolution table.

The information is encapsulated within a burst of closely separated link integrity test pulses that meet 10baseT transmitter waveform for Link test pulses. This burst of pulses is referred to as a Fast Link Pulse (FLP) burst. The chip issues FLP bursts at powerup. The burst consists of alternating clock/data sequence.

To maintain interoperability with existing 10baseT devices, the alogrithm also supports the transmission of 10baseT compliant link integrity test pulses. 10baseT pulse is referred to as the Normal Link Pulse (NLP). A device which fails to respond to the FLP sequence and returns only the NLP indication is treated as a 10baseT compatible device.

Transmit Function

The FLP burst shall contain the Link Code Word (Reg4). FLP bursts consists of 33 pulse positions. The 17 odd numbered pulse positions are always present and represent clock information. The 16 even numbered positions represent data information. A link pulse present in an even numbered position represents a logic one and a link pulse absent from an even numbered pulse position represents a logic zero. The first pulse is a clock pulse. Clock pulses are evenly spaced apart by 125±30 microseconds. The data ONE pulse occurs 62.5±15 microseconds after the clock pulse. The first bit in consecutive FLP bursts shall occur at 16±8 msec interval. The pulses are sent through the TLP pin. A link pulse enable signal, LPEN, is also provided for convenience.

Receive Function

The receive function detects NLP sequence. In addition, the receive function shall detect FLP bursts and decode the information contained.

Arbitration Function

Arbitration function ensures proper sequencing of the autonegotiation algorithm through the transmit and receive function. The arbitration function enables the transmit function to advertise abilities and upon consistent and consecutive reception of the received link code word, advertises acknowledgement. Upon reception of 4 to 6 link code words with acknowledge bit set, the arbitration function determines the highest common denominator using the priority resolution table.

If SDO goes active before autonegotiation is complete, a test window timer will be started and at the expiration of the timer, the arbitration function shall indicate that a valid link has been established.

Table 3. Manual Setting for Non-Auto-Negotiation

Function	AUTO Bit (Reg0 Bit12)	Speed Bit (Reg0 Bit13)	Duplex Bit (Reg0 Bit8)
Auto-negotiation	1	X	X
100BaseT Full Duplex	0	1	1
100BaseT Half Duplex	0	1	0
10BaseT Full Duplex	0	0	1
10BaseT Half Duplex	0	0	0

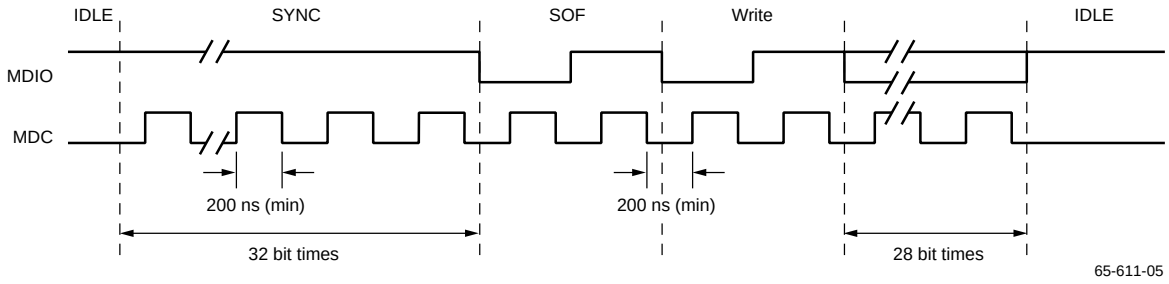


Figure 2. Management Interface Timing during Write to Registers

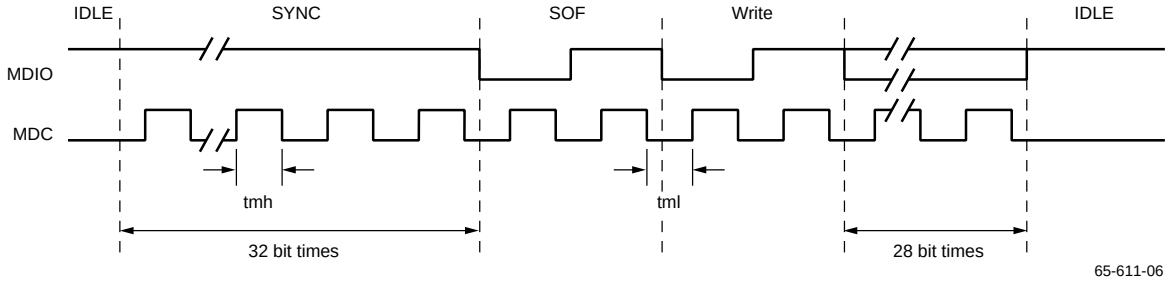


Figure 3. Management Interface Timing during Read from Registers

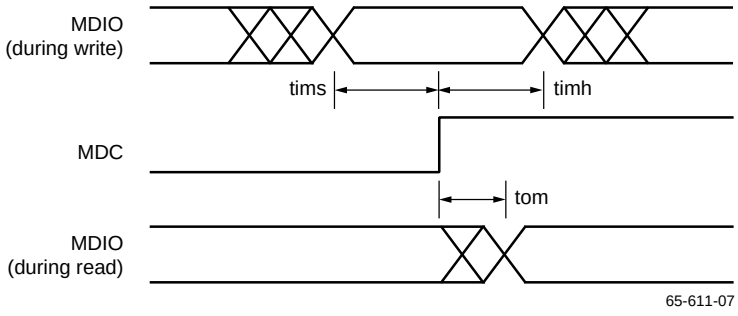


Figure 4.

Advanced Information

Register Definitions

Control Register (Read/Write) – Address 00000 (Register 0)

15	14	13	12	11	10	9	8
Reset	Loop	Speed	Auto	Pwrdn	Isolate	Reconfig	Duplex

7	6	5	4	3	2	1	0
Cltest	Reserved						

All of the control register bits (0 through 15) are read/write.

The functions within the Reg0 are as follows: speed, full/half duplex, Isolate, Automatic speed selection, Loopback, Collision test. The individual bit descriptions and the default values are as follows:

Reg	Bit	Name	Default	Description
0	15	Reset	O	Reset=1 resets the PHY, i.e. all the control and status registers are reset to their default states. This function is self-clearing. The default value is zero. Writes to other bits of control register has no effect until the reset process is completed.
0	14	Loop	O	Loop=1. This bit is used to enable the LOOP output pin HIGH and thereby enable the local loopback of the RCC611 through the RCC613. The default value is zero.
0	13	Speed	I	This bit is used to manually set the speed of operation. Speed=1 denotes 100 Mbps mode of operation. Speed=0 denotes 10 Mbps mode of operation. This bit is used to manually set the speed of operation. This bit is effective only if Auto (Reg0, bit 12)=0 (ie. manual speed selection). The default value is one. If bit12 (Auto) of Reg0=0, and Speed=0, 10Mbps operation is enabled and determined by Reg 1 bit 12 and bit 11. If bit12 (Auto) of Reg0=0 and Speed=1, 100 Mbps operation is enabled.
0	12	Auto	I	Auto=1 denotes automatic speed selection. Auto=0 denotes manual speed selection. Auto speed selection enables PHY's auto selection algorithm. The default value=1.
0	11	Pwrdn	O	Pwrdn=1 shuts off the power to the chip except the portions involving the management transactions. The default value=0. Both Pwrdn & Pwrdn1 cannot be HIGH at the same time. If so, there will not be any power down.
0	10	Isolate	O	The chip isolates its data path from the parallel (MII) interface when Isolate=1. When Isolate=1, the chip will tristate the CMOS outputs: RXCLK, RXDV, ERROR, RXD3..RXD0, CLSN, & CRS. Also, the TTL inputs (DI0..DI3, TXEN, TXERR, TCLK) are ignored. The default value=0. If A(3..0)=0000, the default value=1. This bit is brought out as ISOLATE pin. This can be used to enable or disable an external additional PHY connected to the same controller.
0	9	Reconfig	O	Autolink configuration process will be initiated when Reconfig=1. This bit is self-clearing.
0	8	Duplex	O	When auto-configuration is disabled (Auto=0), Duplex=1 sets the chip for full duplex operation. In this mode, CRS signal is determined by receive activity. Duplex=0 sets the chip for half duplex operation. The default value of Duplex=0.
0	7	Cltest	O	When Cltest=1, CLSN is asserted in response to TXEN. The default value of Cltest=0.
0	6–0	Reserved	O	These bits are reserved for future definition. They are set equal to zero.

Register Definitions (continued)

Status Register (Read Only) – Address 00001 (Register 1)

15	14	13	12	11	10	9	8
0 (T4)	1 (TXFD)	1 (TXHD)	10TFD	10THD	0	0	0

7	6	5	4	3	2	1	0
0	0	Config	Rmtflt	1 (Auto)	Lnkstat	0 (Jabdet)	Extend

The status functions are as follows: information about all the modes of operation supported by the local PHY, the status of auto-negotiation, and if auto-negotiation is supported by the local PHY or not.

Reg	Bit	Name	Default	Description
1	15	T4	0	T4=1 indicates the mode is 100 base T4 capable. T4 is set to 0 for RCC611
1	14	TXFD	1	TXFD=1 indicates the mode is capable of full duplex transmission at 100 base TX. TXFD is set to 1 for RCC611
1	13	TXHD	1	TXHD=1 indicates the mode is capable of half duplex transmission at 100 base TX. TXHD is set to 1 for RCC611
1	12	10TFD	—	10TFD=1 indicates the local PHY has the ability to perform full duplex link transmission and reception using the 10baseT signalling specification. 10TFD=1 if the input pin EX10BTFD is equal to 1.
1	11	10THD	—	10THD=1 indicates the local PHY has the ability to perform half duplex link transmission and reception using the 100baseTX signalling specification. 10THD=1 if the input pin EX10BTHD is equal to 1.
1	10–6	Reserved	0	Bits10–6 are reserved for future definition. These bits are set to zero.
1	5	Config		When Config=1, it indicates that the auto link configuration has been completed and the Registers Reg4, Reg5 and Reg6 are valid. When Config=0, it indicates that the auto link configuration has not been completed. If control register bit 12 (Auto) =0, Config is set to zero.
1	4	Rmtflt		When Rmtflt=1, it indicates that a remote fault condition has been detected. This bit is set to 1 if Reg5 bit 13=1. This bit will remain set until read.
1	3	Auto	1	Auto=1 constitutes the ability of RCC611 to perform auto link detection and configuration. It is set to 1 to indicate that the local PHY has the ability to perform auto link detection and configuration.
1	2	Lnkstat		Lnkstat=1 indicates that the link is active. SDO going HIGH sets Lnkstat HIGH and SDO going HIGH to LOW causes Lnkstat to go HIGH to LOW. Lnkstat=0 indicates that the link is not valid. The occurance of a link failure condition will cause Lnkstat=0 and will remain equal to zero until read. It is set to 1 after read and remains set until the next occurence of SDO going HIGH to LOW.
1	1	Jabdet	0	This bit is set to 0 since jabber detect function is not supported.
1	0	Extend	1	Extend=1 indicates that the PHY provides extended set of capabilities which may be accessed through the extended register set, Reg2 through Reg6. The Extend bit is set to 1 for RCC611.

Register Definitions (continued)

PHY ID Register (Read Only) – Address 00010 (Register 2)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0000 0000 0000 0011															

PHY ID Register (Read Only) – Address 00011 (Register 3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
11 0001						00 0000 (Model)						0000 (Model Rev)			

Register 2 and Register 3 provide a 32-bit value which shall constitute a unique identifier for the PHY. Bits 15–0 of Register 2 and Bits 15–10 of Register 3 constitute the manufacturer ID (OUI). Bits 9–4 of Register 3 constitutes the vendor model and is set to zero. Bits 3–0 of Register 3 constitutes the vendor model version and is set to zero.

Link Advertisement Register (Read/Write) – Address 00100 (Register 4)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NP	Ack	RF	A7–A0								S4–S0				

Register 4 provides a 16-bit value used by the auto link configuration process. Bit 0 is the first bit to be transmitted followed by Bit 1, Bit 2–Bit 15.

Reg	Bit	Name	Default	Description
4	15	NP	0	Next Page (NP) bit is set to 1 to indicate that this node intends to advertise another Link code word. Otherwise, this bit is set to 0. This bit is set through the management interface. The default value is 0.
4	14	Ack	0	Acknowledge (ACK) field is used by the auto-negotiation algorithm to indicate that a station has successfully received its link partner's code word. If no next page (Reg4 bit15=0), this bit is set to 1 after the station has successfully received at least 3 consecutive and consistent Fast Link Pulse Bursts. If next page is to be sent as indicated by the NP bit, this bit is set to 1 after the node has successfully received at least 3 consecutive and consistent FLP bursts and read the current Link Code Word. When the ACK bit is set to 1, the Link Code Word shall be sent 6 times. Initially on powerup, before the auto-negotiation starts, ACK=0.
4	13	RF	0	Remote Fault (RF) is set to 1 to indicate to the link partner the presence of a fault. Otherwise, this bit shall be set to 0. This bit is set to 1 through the management interface. The default value is 0.
4	12–5	A7–A0	0	A7–A0 indicate the technological ability field. This field is used to indicate the supported technologies for each selector field value. The default value is 0. The bit assignments for various technologies are as follows: A0 10baseT A1 10baseT full-duplex A2 100baseTX A3 100baseTX full-duplex A4 100baseT4 A5–7 Reserved
4	4–0	S4–S0		S4–S0 is the selector field. It indicates the type of message that is being sent. For IEEE802.3, S4–S0=00001.

Register Definitions (continued)

Link Partner Register (Read Only) – Address 00101 (Register 5)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NP	Ack	RF	A7–A0								S4–S0				

Register 5 is the link partner's advertised capability register. The fields are same as those of Register 4. Upon successful completion of the auto-negotiation as indicated by Register 1/Bit 5 set to 1, Register 5 has valid information about the advertised ability of the link partner's PHY.

Expansion Register (Read Only) – Address 00110 (Register 6)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											PDF	LPNP	1	Pg Rcvd	LP Able

Reg	Bit	Name	Description
6	15–5	Reserved	Bits 5 through 15 of Register 6 are reserved for future expansion.
6	4	PDF	PDF = 1 indicates a fault has been detected via the Parallel Detection function. Default = 0.
6	3	LPNP	LPNP indicates that the link partner supports the Next Page function.
6	2	NP Able	NP Able indicates local device is Next Page able. It is set to 1.
6	1	Pg Rcvd	Pg rcvd bit is a status bit and indicates that 3 identical and consecutive link code words have been received. This bit is auto clear on read.
6	0	LP Able	LP Able indicates that the Link Partner is able to participate in the auto-negotiation algorithm.

Advanced Information

Register Definitions (continued)

Next Page Register (Read/Write) – Address 00111 (Register 7)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NP	Ack	MP	Ack2	M11/U11–M0/U0											

This next page register is a control register used to convey information beyond that of the base page. All the bits except Ack are written through the management interface.

Reg	Bit	Name	Description
7	15	NP	It is set to 1 to indicate that this node intends to advertise another next page. Otherwise, this bit is set to 0. The default value is 0.
7	14	Ack	Acknowledge (Ack) field is used by the auto-negotiation algorithm to indicate that a station has successfully received the link partner's next page. If no next page (Register 7, Bit 15=0), this bit is set to 1 after the station has successfully received at least 3 consecutive and consistent Fast Link Pulse Bursts. If next page is to be sent as indicated by the NP bit, this bit is set to 1 after the node has successfully received at least 3 consecutive and consistent FLP bursts and read the current Link Code Word. When the ACK bit is set to 1, the Link Code Word shall be sent 6 times. Initially on powerup, before the auto-negotiation starts, Ack=0.
7	13	MP	Message Page (MP). This field is used to differentiate the next page to be message page or the unformatted page. If MP=1, the next page is a message page. If MP=0, the message page is unformatted. Any unformatted page shall be preceded by a message page.
7	12	Ack2	Acknowledge2 (Ack2). If Ack2=1, the station has the ability to comply with the received next page. If Ack2=0, the station will not comply with the message.
7	11–0	M11/U11–M0/U0	This is the 12 bit encoded message or unformatted message depending on MP being 1 or 0 respectively.

User Control/Status Register (Read/Write) – Address 10000 (Register 16)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				Rsvd	Reserved										Pwrdn1

This register is used for additional control & status which are user specific. The additional functions are as follows:

Reg	Bit	Name	Description
16	15–12	Reserved	Bits 12 through 15 are reserved for future use.
16	11	Reserved	Flow Control Enable. This bit is used to enable flow control signalling mechanism inside the chip.
16	10–1	Reserved	Flow Control Symbols. This is a user-assigned symbol pair that is used to communicate the flow control information to the other communicating node. Do not write JK code combination (1100010001) into this set of bits.
16	0	Pwrdn1	In this mode, link signalling is enabled during powerdown.

Advanced Information

Absolute Maximum Ratings[1]

Parameter	Min	Max	Unit
Storage Temperature Range	-65	150	°C
Junction Temperature Range	-55	150	°C
Lead Temperature Range (soldering, 10 seconds)		300	°C
Positive Power Supply, VCC, ATXVCC, ARXVCC	0	6	V
Voltage applied to any TTL inputs	-1	6	V
Voltage applied to any PECL inputs	-1	6	V
Voltage applied to any CMOS outputs	-1	6	V
Voltage applied to any PECL outputs	-1	6	V
Current from any CMOS outputs	-50	50	mA
Current from any PECL outputs	-50	50	mA

Note:

1. "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. If the device is subjected to the limits in the absolute maximum ratings for extended periods, its reliability may be impaired. The tables of Electrical Characteristics provide conditions for actual device operation.

Operating Conditions

Parameter		Min	Typ	Max	Units
Ta	Ambient Operating Temperature	0		70	°C
VCC	Positive Supply Voltage (DVCC and AVCC)	4.75	5.0	5.25	V
RI	PECL Differential Load Resistance (Note 1)	80	100	120	Ω

Note:

1. Differential load resistance of 100 Ω equals 50 Ω to AC ground on each of DOUT, $\overline{\text{DOUT}}$.

Advanced Information

DC Electrical Characteristics

AVCC, DVCC = 5V±5%, GND=0V, unless otherwise indicated.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Transmitter Section						
Vihc	TTL input Voltage HIGH		2.0		VCC+0.5	V
Vilc	TTL input Voltage LOW		0		0.8	V
Iinc	TTL Input Current		-1		100	µA
Ci	Input Capacitance			4	10	pF
Vohp	PECL Output Voltage HIGH	Rdiff=100Ω, VCC=5V	3.5	3.8	4.2	V
Volp	PECL Output Voltage LOW	Rdiff=100Ω, VCC=5V	2.6	3.0	3.4	V
Vop	PECL Output Voltage amplitude	Vohp-Volp, VCC=5V	0.6	0.8	1.0	V
Iolp	PECL Output Current HIGH			8		mA
Receiver Section						
Vihc	TTL input Voltage HIGH		2.0		+5.5	V
Vilc	TTL input Voltage LOW		0		0.8	V
Iinc	TTL Input Current		-1		1	µA
Vcm	Com. Mode Range (DIN,$\overline{\text{DIN}}$)		2		5	V
Vdiff	Diff. Input Voltage (DIN, $\overline{\text{DIN}}$)		0.2		5.5	V
Iip	PECL Input Current		-1		1	µA
Vohc	Output Voltage HIGH		3.5		VCC	V
Volc	Output Voltage LOW		0		0.5	V
Iolc	Output Current LOW		4			mA
Iohc	Output Current HIGH		4			mA
ICC	Power Supply Current			120		mA
PD	Power Dissipation			600		mW

Advanced Information

AC Electrical Characteristics

AVCC, DVCC = 5V±5%, GND = 0V, unless otherwise indicated

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Transmitter Section						
Tt1	TCLK Period			40		ns
Tch	TCLK Pulse Width HIGH		15			ns
Tcl	TCLK Pulse Width LOW		15			ns
tids	DIN0–DIN7,TXEN,TXERR to TCLK ↑ setup time		4			ns
tidh	TCLK ↑ to DIN0–3, TXEN,TXERR hold time		4			ns
tr, tf	DOUT, $\overline{\text{DOUT}}$ rise and fall times	10% to 90% points			2	ns
ttj	DOUT, $\overline{\text{DOUT}}$ total pk-pk jitter				1.4	ns
tdj	DOUT, $\overline{\text{DOUT}}$ pk-pk duty cycle distortion				500	ps
Receiver Section						
fcc	Input Data Rate Variation				±1000	ppm
D	Input Data Transition Density to Acquire and Maintain Lock		0.1			ppm
n	Maximum run length of consective 1's or 0's before loss of lock		60			bits
tacq	Loop Acquisition Time for 10E-12 BER				1000	bits
tri, tfi	DIN, $\overline{\text{DIN}}$ input rise and fall time				1	ns
tj	DIN, $\overline{\text{DIN}}$ input peak to peak jitter tolerance				0.075T	ns
tod	RCLK ↓ to DO0–DO3, RXDV valid				10	ns
Tr1	RCLK period			40		ns
Trh	RCLK pulse width HIGH		0.35Tr1	0.4Tr1	0.45Tr1	ns
Management Section						
Tmh	MDC pulse width HIGH		200			ns
Tml	MDC pulse width LOW		200			ns
tims	MDIO to MDC ↑ setup		5			ns
timh	MDIO to MDC ↑ hold		5			ns
tom	MDC ↑ to MDIO				15	ns

Note:

1. Test conditions (unless otherwise indicated:) PECL Input rise and fall times ≤1ns, RL = 100Ω (differential), RL = 50Ω (single-ended). TTL Input rise and fall times ≤15ns. Transition density ≥ 0.1.

Advanced Information

TIming Diagrams

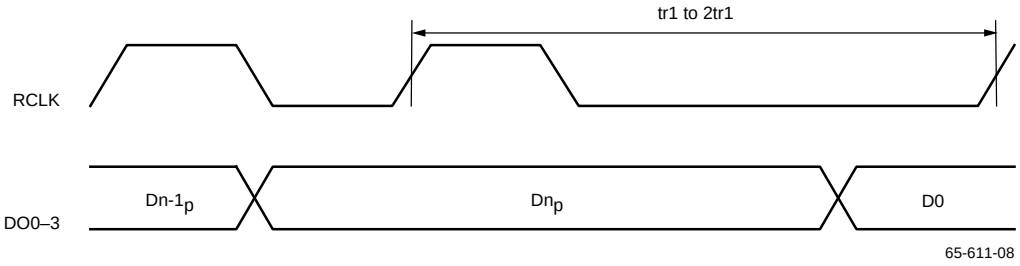


Figure 5. Receiver Timing—New Alignment

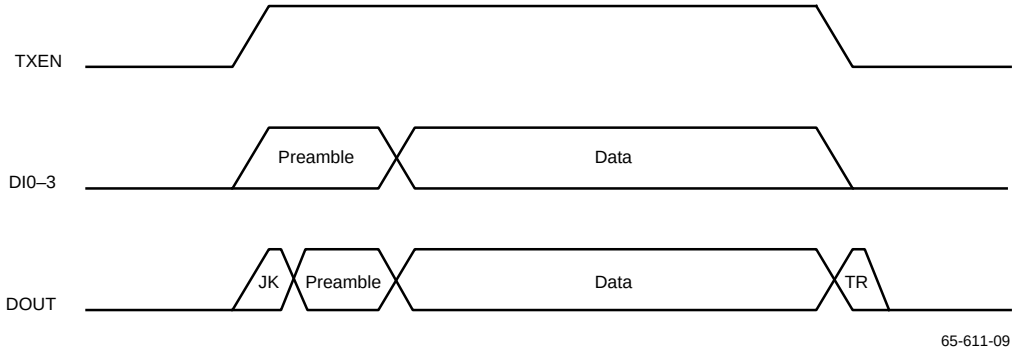


Figure 6. Frame Sequence—Transmit

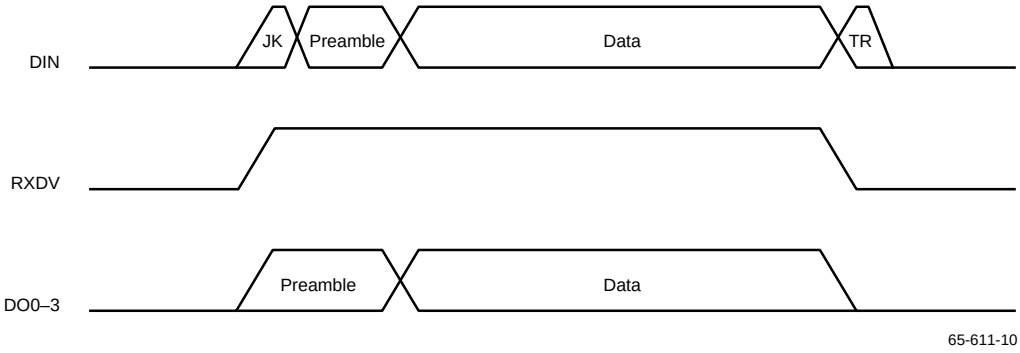


Figure 7. Frame Sequence—Receive

Advanced Information

Timing Diagrams (continued)

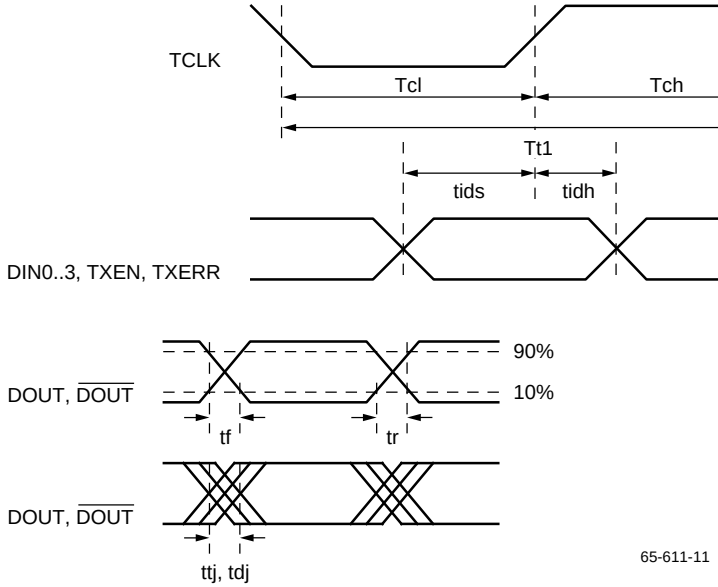


Figure 8. Transmitter Timing

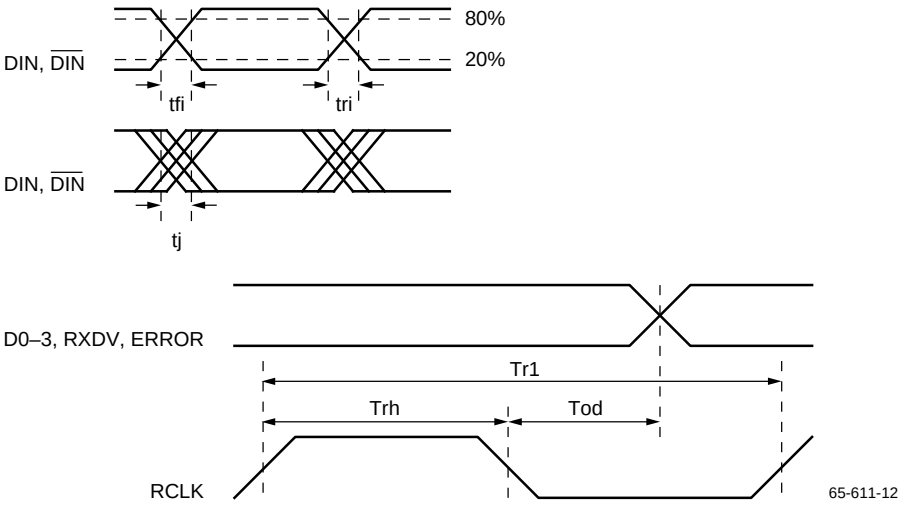


Figure 9. Receiver Timing

Advanced Information

Applications Discussion

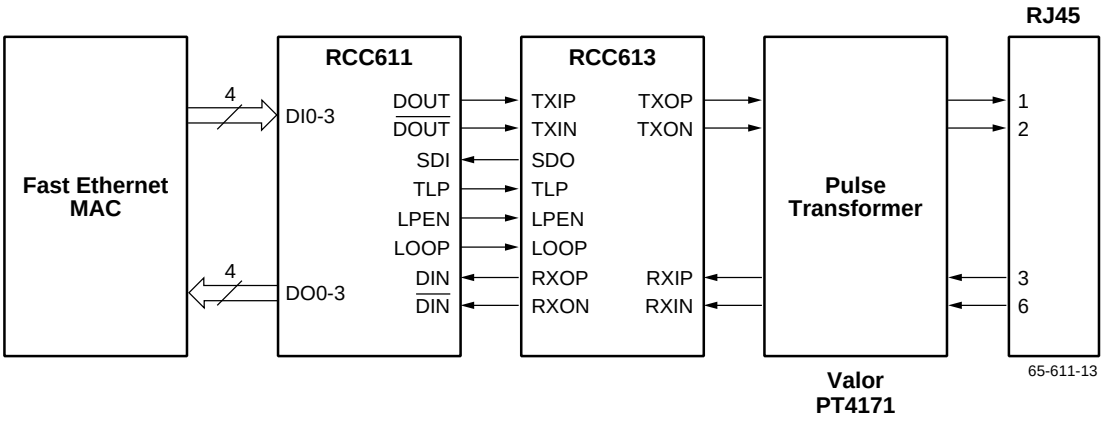


Figure 10. Typical Application

Advanced Information

Notes:

Notes:

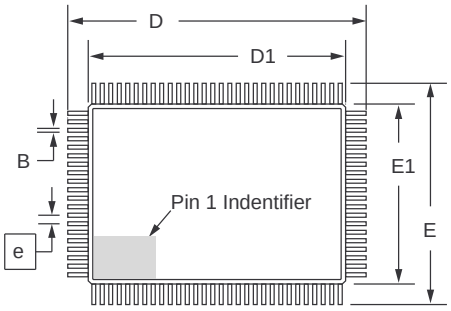
Mechanical Dimensions

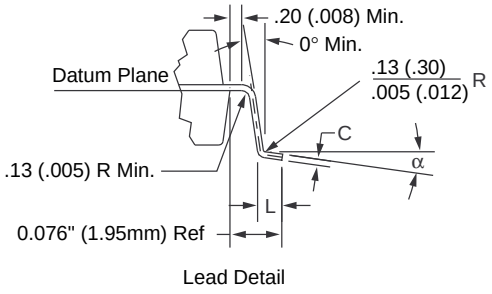
100 Lead MQFP 14x20mm Package—3.9mm Footprint

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.134	—	3.40	
A1	.010	—	.25	—	
A2	.100	.120	2.55	3.05	
B	.008	.015	.22	.38	3, 5
C	.005	.009	.13	.23	5
D	.922	.942	23.65	24.15	
D1	.783	.791	19.90	20.10	
E	.688	.708	17.65	18.15	
E1	.547	.555	13.90	14.10	
e	.0256 BSC		.65 BSC		
L	.028	.040	.73	1.03	4
N	100		100		
ND	30		30		
NE	20		20		
α	0°	7°	0°	7°	
ccc	—	.005	—	.12	

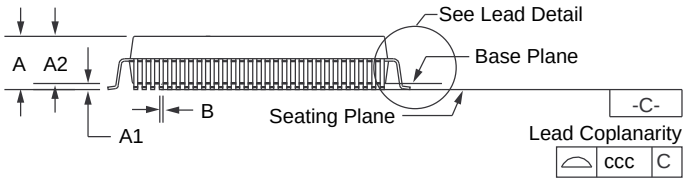
Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Controlling dimension is millimeters.
3. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be .08mm (.003in.) maximum in excess of the "B" dimension. Dambar cannot be located on the lower radius or the foot.
4. "L" is the length of terminal for soldering to a substrate.
5. "B" & "C" includes lead finish thickness.





Lead Detail



Advanced Information

Ordering Information

Product Number	Package
RCC611KR	100 Lead MQFP

Advanced Information

LIFE SUPPORT POLICY

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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2/98 0.0m
Stock#DS50000611

RCC613

125 Mbaud Twisted Pair Transceiver (TPT)

Features

- Designed for 100BaseTX Fast Ethernet PMD Standard
- Controlled symmetric transmit output rise/fall time
- Tristatable transmit output
- Adjustable transmit amplitude for longer cables
- DC restoration (Baseline wander compensation)
- No receive input attenuation required
- Adaptive line equalization
- Compatible with RCC611 Fast Ethernet PHY
- Fast link pulse driving
- 28 pin PLCC
- 525mW power dissipation

Applications

- 100Mbps Fast Ethernet
- Bus extenders
- Serial Video Communication
- Fast Ethernet test equipment

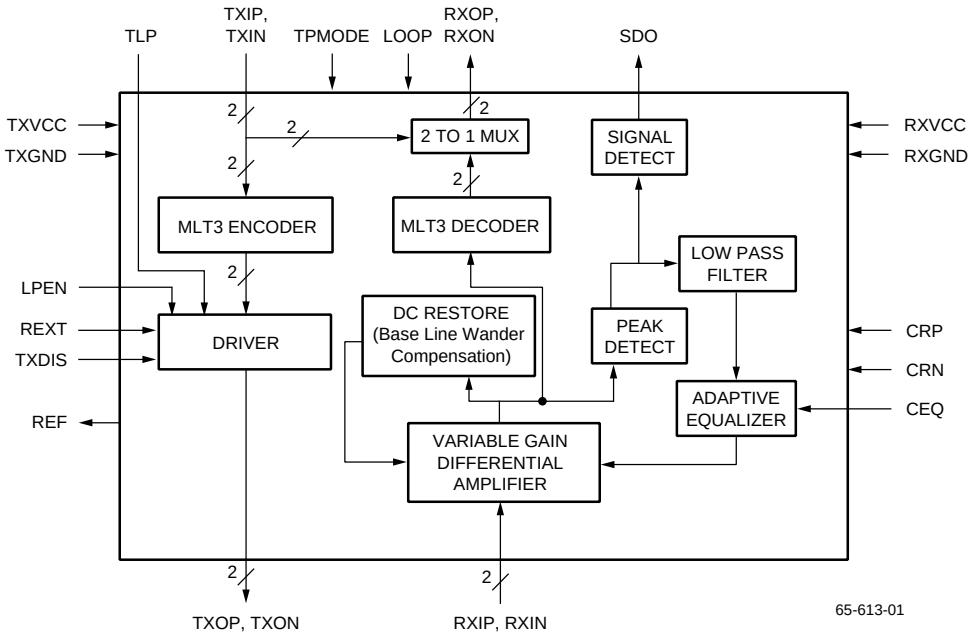
Description

The RCC613 is a monolithic 125 Megabaud twisted pair transceiver (TPT) designed for IEEE 802.3 Fast Ethernet applications. It implements the Physical Media Dependent (PMD) Layer requirements of the 100baseTX Fast Ethernet standard. It can be used with RCC611 Fast Ethernet PHY to perform the 100baseTX physical layer requirements.

The RCC613 Integrates MLT3 encoding, data driving and receiving, link pulse driving, adaptive equalization, base line wander compensation (DC restoration) and MLT3 decoding. It operates with a single +5V supply.

Preliminary Information

Block Diagram



Functional Description

Transmitter Section

The RCC613 transmitter section includes the MLT3 Encoder and Twisted pair driver. The transmitter drives either unshielded or shielded twisted pair cables to implement FDDI TP/PMD standard.

The differential PECL data from TXIP, TXIN goes through a MLT3 Encoder. The MLT3 encoder is enabled when the TPMODE pin is LOW. The data is encoded per the following rules: The encoded output takes on one of three possible levels: High, Middle, or Low. Whenever the input signal changes state, the output will also change state. If the output is in the middle state, the state to which it will change to is dependent on the previous state. If the previous state was high(low), then the output will change to a low(high) state from the middle state. If the output is at either a high or a low state, then the next transition will cause the output to change to the middle state. The encoder conforms to the diagram shown in Figure 1.

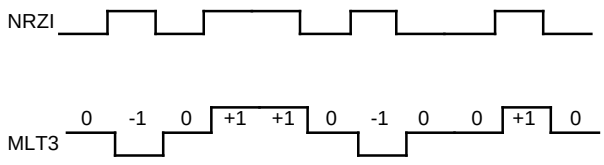


Figure 1. MLT3-NRZI Conversion Diagram

When TPMODE pin is HIGH, the MLT3 encoder is bypassed and the data directly goes to the current source driver. The driver output current is controlled by external resistor between REXT and REF pins.

The voltage at the output is a function of the load termination across the differential output. If R is the effective load termination and I is the current source, the peak to peak output voltage V = IR. I = 40/REXT(in kΩ) mA, where REXT is the resistor connected between the REXT and REF pins. The TP driver provides a differential 2 V peak to peak swing voltage output across TXOP, TXON through a 100Ω termination in parallel with two 50Ω pullup resistor, when REXT = 1KΩ.

TXOP,TXON are connected externally to a coupling transformer and then to the twisted pair cable medium. The driver can be tristated by means of a pin TXDIS. When TXDIS is HIGH, the output presents a high impedance. In 2-level mode (TPMODE = HIGH), the output amplitude is half that of 3-level mode.

The transition time of the output is closely matched and controlled to reduce radiated emissions and to comply with FCC class B regulations.

The transmitter section has a pin LPEN to enable fast link pulses for driving. When LPEN is HIGH and Transmit Link Pulse (TLP) input is HIGH, the outputs TXOP and TXON will be at HIGH of 3 volts.

Receiver Section

The signal from the transformer drives RXIP and RXIN and goes through a differential amplifier stage and then to a peak detect circuitry. The output of the peak detector goes to the signal detect comparator and to a low pass filter to remove the AC components. The low pass filter output then goes to an adaptive equalizer.

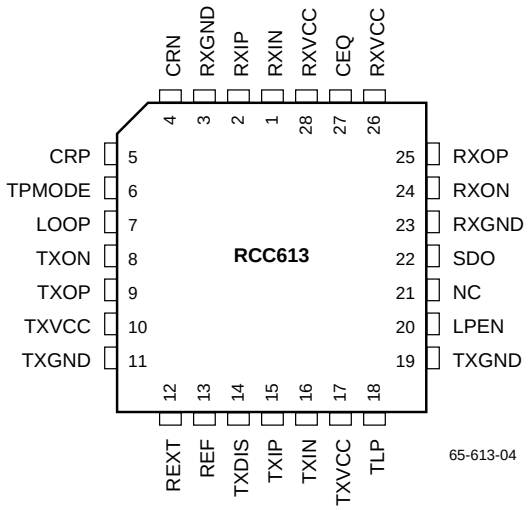
The equalizer output provides an adaptive gain control for the variable gain differential amplifier to compensate for the cable distortion. The gain depends on the measured peak value of the input. The equalizer filter characteristics can be adjusted by means of an external capacitor connected between CEQ and ground (1000pF is suggested).

The variable gain differential amplifier output also goes through the DC restoration and decode circuitry. The purpose of the DC restoration (baseline wander compensation) circuit is to provide DC restoration to the data stream on the occurrence of a long run-length. During those instances, the average DC tends to drift away from the decode circuit's threshold. The DC restoration circuit integrates the decoder output to provide a DC offset to the envelope to center it around the threshold of the decoder circuit. The MLT3 decoder also provides 3-level to 2-level conversion. The decoder conforms to the diagram shown in Figure 1.

The decoder output goes through a 2 to 1 multiplexer. The other input to the multiplexer comes from the transmitter inputs TXIP, TXIN. If LOOP signal is HIGH, the transmit input is looped back to RXOP, RXON through the multiplexer. Under this condition, the transmitter output (TXOP, TXON) presents a logic LOW voltage. If LOOP is LOW, the decoder output is enabled and routes the signal to RXOP, RXON.

The receive section also includes a signal detect logic. The signal detect logic filters the input signal and if the signal exceeds a specified level, the SDO output will go HIGH.

Pin Assignments



Pin Definitions

Pin Name	Pin Number	Pin Type	Description
TXVCC	10, 17	Power	**Transmit Positive Supply.** The nominal value is 5V±5%. TXVCC should be bypassed to TXGND with a 0.1µF chip capacitor placed as close to the pin as possible.
RXVCC	26, 28	Power	**Receive Positive Supply.** The nominal value is 5V±5%. RXVCC should be bypassed to RXGND with a 0.1µF chip capacitor placed as close to the pin as possible.
TXGND	11, 19	Power	**Transmit Ground.** Chip ground for transmit circuitry. TXGND should be connected to the printed circuit board's ground plane through a ferrite bead of value 0.2µH to 1µH.
RXGND	23,3	Power	**Receive Ground.** Chip ground for digital circuitry. RXGND should be connected to the printed circuit board's ground plane through a ferrite bead of value 0.2µH to 1µH.
TXIP, TXIN	15, 16	PECL DIFF I/P	**Transmit Input Positive, Transmit Input Negative.** Differential NRZI Transmit data from the PHY chip.
TPMODE	6	TTL I/P	**Twisted Pair Encode Mode.** When TPMODE is LOW, the transmit output is MLT3 encoded with three levels. When TPMODE is HIGH, the transmit output is NRZI with two levels.
TXOP,TXON	9,8	O/P	**Transmit Output Positive, Transmit Output Negative.** (MLT3 outputs if TPMODE = 0, NRZI outputs if TPMODE = 1). Transmit differential current driver data outputs.
REXT	12	Analog	**External Resistor.** It is connected between REXT and REF to adjust the amplitudes of TXOP,TXON. For MLT3 signals, the peak-to-peak differential voltage of 2V is generated across TXOP, TXON when the effective differential load is 50Ω and REXT = 1KΩ.
RXIP, RXIN	2,1	I/P	**Receive Input Positive, Receive Input Negative.** (MLT3 inputs if TPMODE = 0, NRZI inputs if TPMODE = 1). Receive differential data inputs.
CEQ	27	Analog	**Equalizer Capacitor.** A capacitor is connected between CEQ and RXGND to adjust the gain of the adaptive equalizer. 1000 pF is recommended.

Preliminary Information

Pin Definitions (continued)

Pin Name	Pin Number	Pin Type	Description
RXOP, RXON	25, 24	PECL DIFF O/P	**Receive Output Positive, Receive Output Negative.** Differential NRZI receive data to the PHY chip. Do not tie external termination lower than 510Ω to RXGND. For 50Ω applications, 50Ω from the outputs to 3V may be connected.
SDO	22	PECL O/P	**Signal Detect.** When SDO is HIGH, it indicates that the receive input is active. Do not tie any external termination resistor to SDO.
TLP	18	TTL I/P	**Transmit Link Pulse.** If TLP and LPEN are both HIGH, the transmitter generates a 3V differential across TXOP and TXON.
LPEN	20	TTL I/P	**Link Pulse Enable.** This pin, when HIGH, is used to enable the link pulse driving.
LOOP	7	TTL I/P	**Loop.** If LOOP is HIGH, it loops the transmit input data, TXIP, TXIN to the receiver output, RXOP, RXON. If LOOP is LOW, the normal operation occurs.
TXDIS	14	TTL I/P	**Transmit Disable.** If TXDIS is HIGH, the transmitter disables the TXOP, TXON output and presents a high impedance. If TXDIS is LOW, the transmitter enables normal data transmission through RCC613.
CRP, CRN	5, 4	Analog	**DC Restoration Capacitor Positive, DC Restoration Capacitor Negative.** A capacitor is connected at each of CRP, and CRN to RXGND to provide DC restoration. 1000 pF is recommended.
REF	13	Analog O/P	**Reference.** Provides the reference voltage to set the transmit output amplitude when an external resistor is connected between REF and REXT. It is nominally 2.5 Volts.

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Min.	Max.	Units
Positive power supply	0	6	V
Voltage applied to any PECL/MLT3 outputs	-0.5	V_{CC}	V
Voltage applied to any TTL inputs	-0.5	V_{CC}	V
Voltage applied to any PECL inputs	-0.5	V_{CC}	V
Current from any PECL/MLT3 outputs	-50	+50	mA
Operating Temperature	0	70	°C
Storage Temperature	-65	150	°C
Junction Temperature	-55	150	°C
Lead Soldering (10 seconds)		300	°C

Note:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter		Min.	Typ.	Max.	Units
Ta	Ambient Operating Temperature	0		70	°C
V_{CC}	Positive Supply Voltage (TXVCC and RXVCC)	4.75	5.00	5.25	V
R_{utp}	Unshielded Twisted Pair Differential Load Resistance	99.8	100	100.2	Ω
R_{stp}	Shielded Twisted Pair Differential Load Resistance	149.7	150	150.3	Ω

DC Electrical Characteristics

RXVCC, TXVCC = 5V ±5%, RXGND, TXGND = 0V, unless otherwise indicated

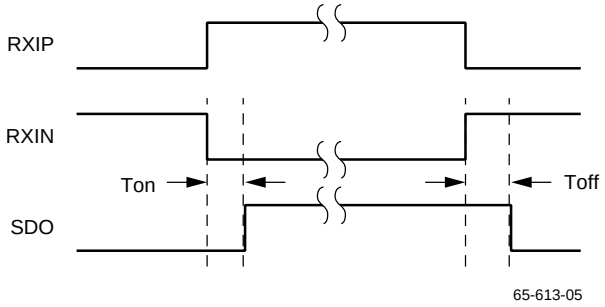
Parameter		Conditions	Min.	Typ.	Max.	Units
Transmitter Section						
Vihc	TTL input Voltage HIGH		2.0		V_{CC}	V
Vilc	TTL input Voltage LOW		0		0.8	V
Iinc	TTL Input Current				25	µA
C	Input Capacitance			3.0		pF
Vcm	Com. Mode Range (TXIP,TXIN)		3.3	3.7	4.1	V
Vdiff	Diff. Input Voltage (TXIP,TXIN)		0.4		2.0	Vpp
Iip	PECL Input Current		-20	0	20	µA
Vomh	MLT3 Positive Peak Voltage	Diff load R=100Ω ±0.2% and 50Ω on both TXOP, TXON to VCC		4.2		V
Voml	MLT3 Negative Peak Voltage			3.2		V
Vohs	NRZI Output Voltage HIGH			4.2		V
Vols	NRZI Output Voltage LOW			3.2		V
Volp	Link Pulse Output				3	V
Receiver Section						
Vdif	RXIP, RXIN Diff Input Voltage		0.4		2	V
Vcm	RXIP, RXIN Com. Mode Range			2.6		V
Vocm	RXOP, RXON Com. Mode Range	510Ω to GND on RXOP, RXON		V_{CC}–1.5		V
Vodiff	RXOP, RXON Diff Output Voltage			1.5		Vpp
Vohs	SDO Output HIGH		V_{CC}–1.1		V_{CC}–0.7	V
Vols	SDO Output LOW		V_{CC}–2		V_{CC}–1.4	V
Vonth	SDO Turnon threshold			350		mV
Vofth	SDO Turnoff threshold			260		mV
Power Section						
ICC	Power Supply Current			110		mA
PD	Power Dissipation			525		mW

Preliminary Information

Preliminary Information

AC Electrical Characteristics[1]

V_{CC} = 5V ±5%, GND = 0V, unless otherwise indicated.

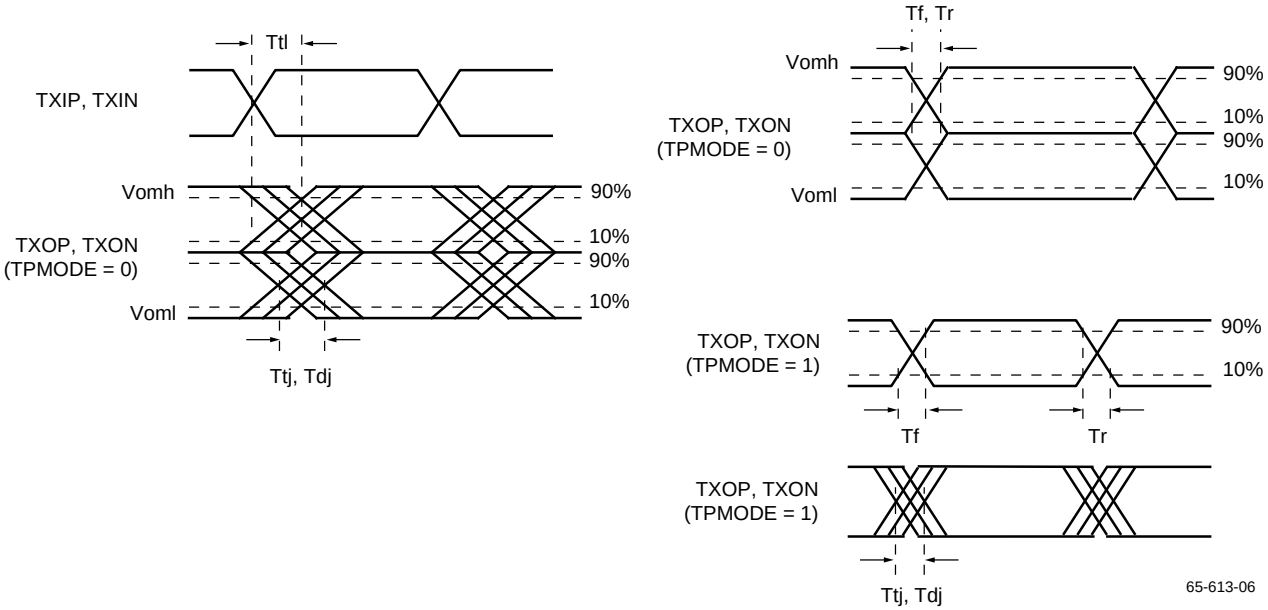


Parameter		Conditions	Min	Typ	Max	Units
Receiver Section						
Ton	SDO turnon delay @ CEQ = 1000pF	Diff I/P > 1V		1	1000	µs
Toff	SDO turnoff delay @ CEQ = 1000pF	Diff I/P < 0.2V		200	350	µs

Notes:

1. Test conditions (unless otherwise indicated:) PECL Input rise and fall times ≤ 2ns, R_L = 100Ω. TTL Input rise and fall times ≤ 15ns. Transition density ≥ 0.1.

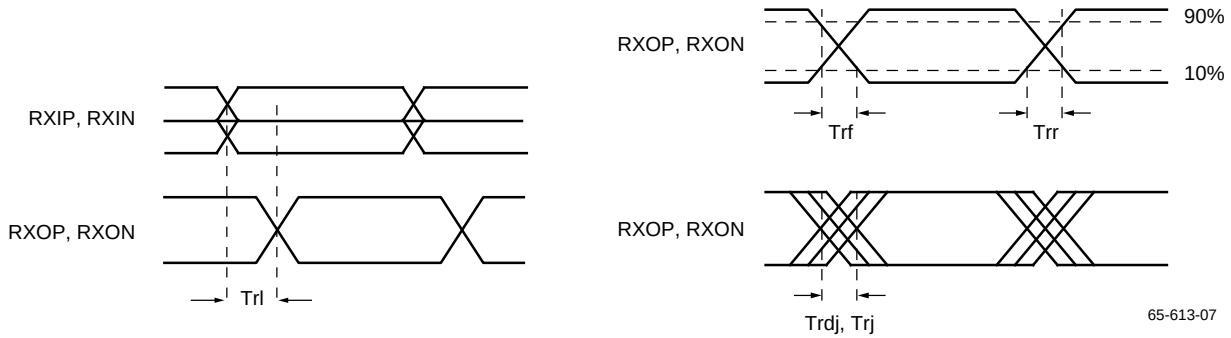
Timing Diagrams



Transmitter Timing

Parameter		Conditions	Min	Typ	Max	Units
Tr	TXOP, TXON rise time 10% to 90%	100Ω termination		2.7		ns
Tf	TXOP, TXON fall time 90% to 10%			2.7		ns
Tdj	TXOP, TXON duty cycle distortion (peak-to-peak)			0.3		ns
Ttj	Random jitter			300		ps
Ttl	Transmit latency			5.0		ns

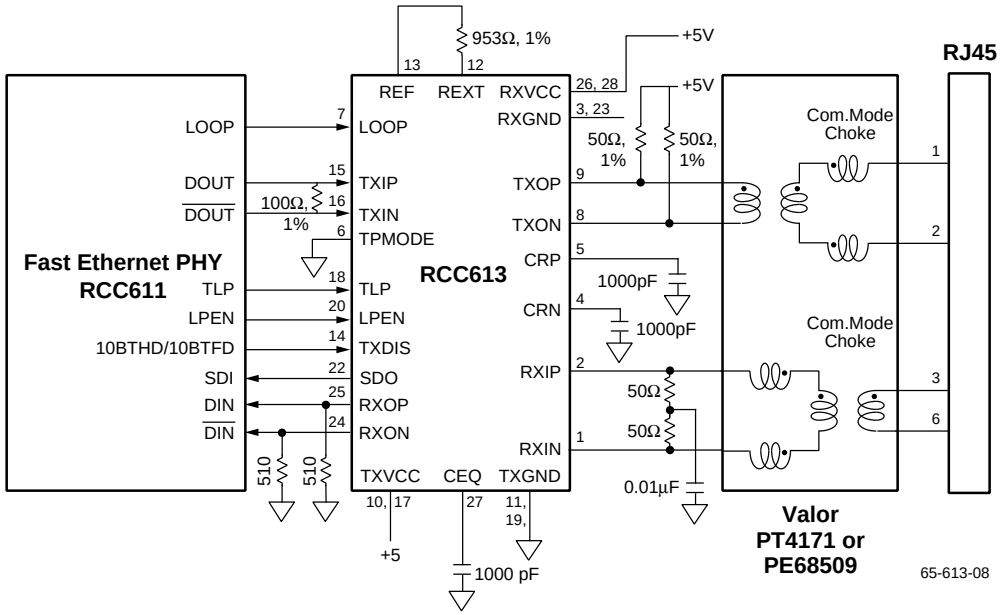
Timing Diagrams (continued)



Receiver Timing

Parameter		Conditions	Min	Typ	Max	Units
Trr	RXOP, RXON rise time 10% to 90%	510Ω to GND		1.5		ns
Tfr	RXOP, RXON fall time 90% to 10%			1.5		ns
Trdj	RXOP, RXON duty cycle distortion (peak-to-peak) @ 100m calbe (UTP)			0.5		ns
Trj	RXOP, RXON peak to peak jitter			400		ps
Trl	Receive latency	@ 100m UTP		5		ns

Applications Discussion



Notes:

1. For FDDI applications, the receive pins are 7 and 8 instead of 3 and 6 on the RJ45 connector.
2. TXVCC and RXVCC should be connected individually to circuit board's +5 volts through ferrite bead of value 0.2µH to 1µH (e.g. FAIR-RITE BEAD #274-3019-446).
3. TXGND and RXGND should be connected individually to circuit board's ground through ferrite bead of value 0.2µH to 1µH (e.g. FAIR-RITE BEAD #276-3019-446). The current handling capability should be 100mA.
4. For 50Ω applications, RXOP, RXON may be connected with 50Ω to 3V.

Preliminary Information

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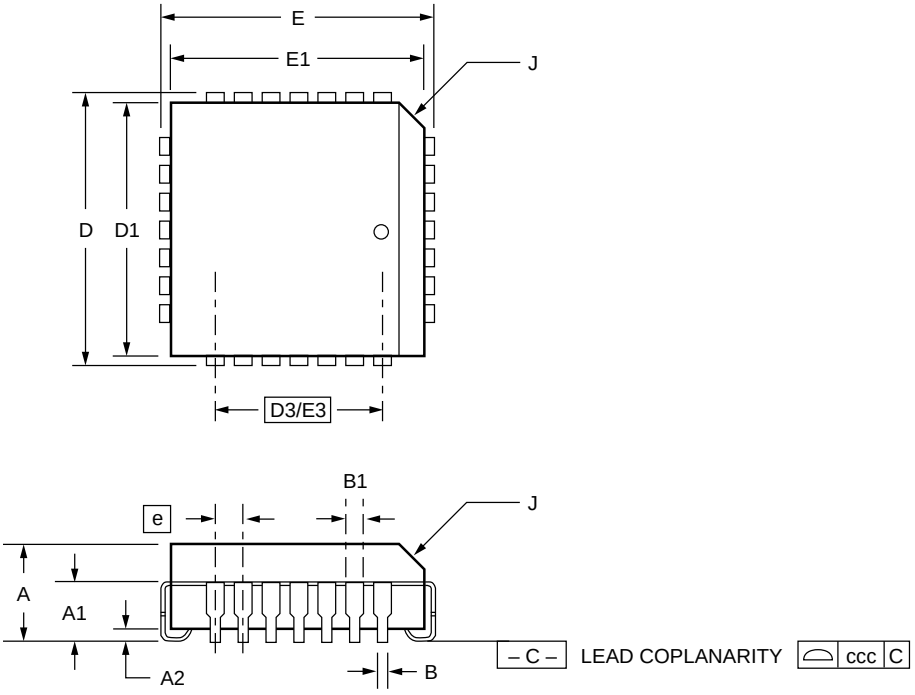
Mechanical Dimensions – 28 Lead PLCC (QA) Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.180	4.19	4.57	
A1	.090	.120	2.29	3.04	
A2	.020	—	.51	—	
B	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D/E	.485	.495	12.32	12.57	
D1/E1	.450	.456	11.43	11.58	
D3/E3	.300 BSC		7.62 BSC		
e	.050 BSC		1.27 BSC		
J	.042	.048	1.07	1.22	8
ND/NE	7		7		
N	28		28		
ccc		.004		0.10	

Notes:

1. Cavity mismatch = .004 (0.10mm)
2. Cavity frame offset = .002 (0.05mm) excluding leadframe tolerances.
3. Mold protrusions: Parting Line = .006 (0.15mm), Top or Bottom = .001 (0.025mm)
4. Variation in lead position = .005 (0.13mm)
5. Shoulder instrusions & protrusions: Intrusions = .002 (0.05mm), Protrusions = .003 (0.08mm)
6. Package warpage, WARP FACTOR = 2.5 = $\frac{\text{WARP (mils)}}{\text{Package Length (inches)}}$
7. Ejector pin depth = .010 (0.25mm) maximum.
8. Corner and edge chamfer = 45°C.



Preliminary Information

Ordering Information

Product Number	Package
RCC613V	28 PLCC

Preliminary Information

LIFE SUPPORT POLICY

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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RCC615

125 Mbaud Twisted Pair Transceiver (TPT)

Features

- Compliant with FDDI TP-PMD standards
- Controlled symmetric transmit output rise/fall time
- Tristatable transmit output
- Adjustable transmit amplitude for longer cables
- DC Restoration (Baseline wander compensation)
- No receive input attenuation required
- Adaptive line equalization
- Compatible with existing FDDI/Fast Ethernet Physical layer (PHY) chips
- 28 pin PLCC
- 525mW power dissipation

Applications

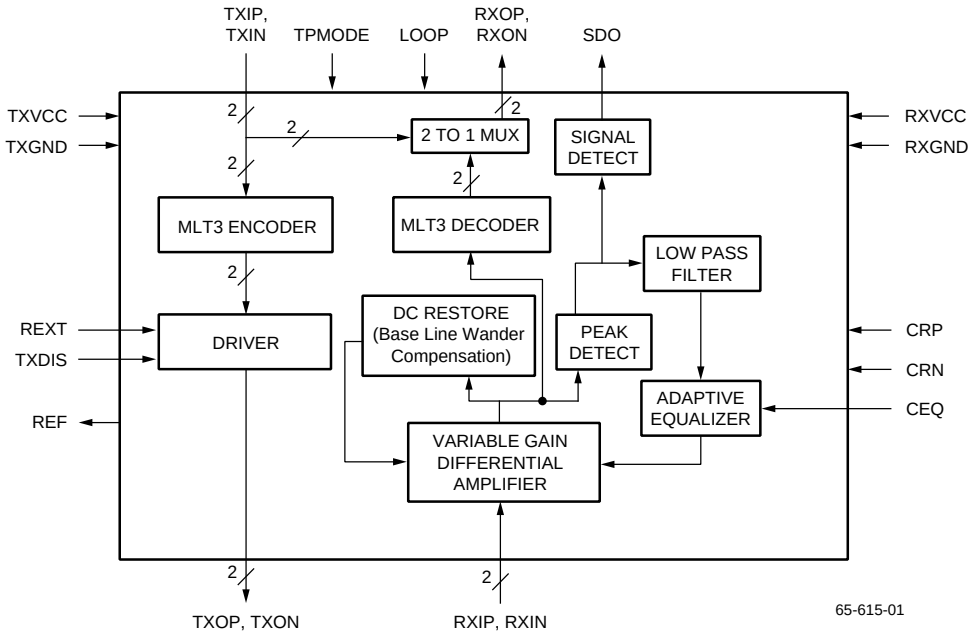
- FDDI
- 100 Mbps Fast Ethernet
- Bus Extenders
- Serial Video Communication
- Fast Ethernet/FDDI test equipment

Description

The RCC615 is a monolithic 125 Megabaud twisted pair transceiver (TPT) designed for IEEE 802.3 Fast Ethernet & American National Standard's (ANSI's) Fiber Distributed Data Interface (FDDI) applications. It implements the Physical Media Dependent Layer requirements of the FDDI (TP_PMD) standard. It can be used in a PHY layer solution for FDDI or 100base-TX Fast ethernet.

The RCC615 Integrates MLT3 encoding, driving, receiving, adaptive equalization, base line wander compensation (DC restoration) and MLT3 decoding. It operates with a single +5V supply.

Block Diagram



Rev. 0.9.6

Functional Description

Transmitter Section

The RCC615 transmitter section includes the MLT3 Encoder and Twisted pair driver. The transmittter drives either unshielded or shielded twisted pair cables to implement FDDI TP/PMD standard.

The differential PECL data from TXIP, TXIN goes through a MLT3 Encoder. The MLT3 encoder is enabled when the TPMODE pin is LOW. The data is encoded per the following rules: The encoded output takes on one of three possible levels: High, Middle, or Low. Whenever the input signal changes state, the output will also change state. If the output is in the middle state, the state to which it will change to is dependent on the previous state. If the previous state was high(low), then the output will change to a low(high) state from the middle state. If the output is at either a high or a low state, then the next transition will cause the output to change to the middle state. The encoder conforms to the diagram shown in Figure 1.

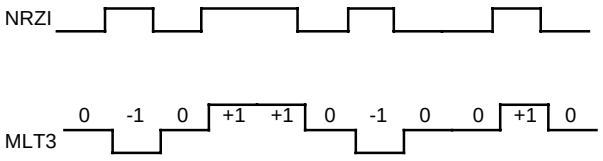


Figure 1. MLT3-NRZI Conversion Diagram

When TPMODE pin is high, the MLT3 encoder is bypassed and the data directly goes to the current source driver. The driver output current is controlled by external resistor between REXT and REF pins.

The voltage at the output is a function of the load termination across the differential output. If R is the effective load termination and I is the current source, the peak to peak output voltage V = IR. I = 40/REXT(in kΩ) mA, where REXT is the resistor connected between the REXT and REF pins. The TP driver provides a differential 2 V peak to peak swing voltage output across TXOP, TXON through a 100Ω termination in parallel with two 50Ω pullup resistor, when REXT = 1KΩ.

TXOP,TXON are connected externally to a coupling transformer and then to the twisted pair cable medium. The driver can be tristated by means of a pin TXDIS. When TXDIS is HIGH, the output presents a high impedance. In 2-level mode (TPMODE = HIGH), the output amplitude is half that of 3-level mode.

The transition time of the output is closely matched and controlled to reduce radiated emissions and to comply with FCC class B regulations.

Receiver Section

The signal from the transformer drives RXIP and RXIN and goes through a differential amplifier stage and then to a peak detect circuitry. The output of the peak detector goes to the signal detect comparator and to a low pass filter to remove the AC components. The low pass filter output then goes to an adaptive equalizer.

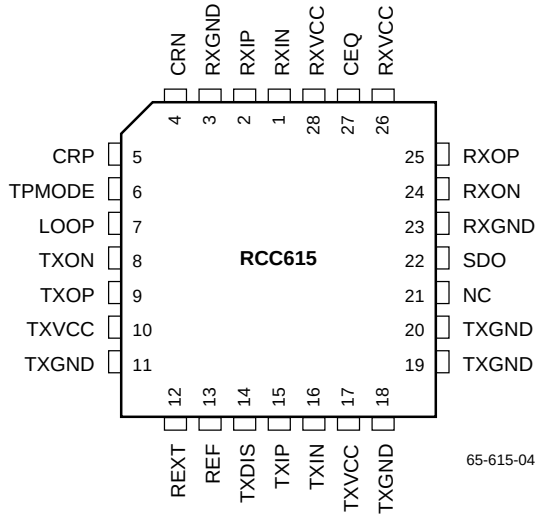
The equalizer output provides an adaptive gain control for the variable gain differential amplifier to compensate for the cable distortion. The gain depends on the measured peak value of the input. The equalizer filter characteristics can be adjusted by means of an external capacitor connected between CEQ and ground (1000pF is suggested).

The variable gain differential amplifier output also goes through the DC restoration and decode circuitry. The purpose of the DC restoration (baseline wander compensation) circuit is to provide DC restoration to the data stream on the occurrence of a long run-length. During those instances, the average DC tends to drift away from the decode circuit's threshold. The DC restoration circuit integrates the decoder output to provide a DC offset to the envelope to center it around the threshold of the decoder circuit. The MLT3 decoder also provides 3-level to 2-level conversion. The decoder conforms to the diagram shown in Figure 1.

The decoder output goes through a 2 to 1 multiplexer. The other input to the multiplexer comes from the transmitter inputs TXIP, TXIN. If LOOP signal is HIGH, the transmit input is looped back to RXOP, RXON through the multiplexer. Under this condition, the transmitter output (TXOP, TXON) presents a logic LOW voltage. If LOOP is LOW, the decoder output is enabled and routes the signal to RXOP, RXON.

The receive section also includes a signal detect logic. The signal detect logic filters the input signal and if the signal exceeds a specified level, the SDO output will go HIGH.

Pin Assignments



Pin Descriptions

Pin Name	Pin Number	Pin Type	Description
CEQ	27	Analog	**Equalizer Capacitor.** A capacitor is connected between CEQ and RXGND to adjust the gain of the adaptive equalizer. 1000 pF is recommended.
CRP, CRN	5, 4	Analog	**DC Restoration Capacitor Positive, DC Restoration Capacitor Negative.** A capacitor is connected at each of CRP, and CRN to RXGND to provide DC restoration. 1000 pF is recommended.
LOOP	7	TTL I/P	**Loop.** If LOOP is HIGH, it loops the transmit input data, TXIP,TXIN to the receiver output, RXOP,RXON. If LOOP is LOW, the normal operation occurs.
REF	13	Analog O/P	**Reference.** Provides the reference voltage to set the transmit output amplitude when an external resistor is connected between REF and REXT. It is nominally 2.5 Volts.
REXT	12	Analog	**External Resistor.** It is connected between REXT and REF to adjust the amplitudes of TXOP, TXON. For MLT3 signals, the peak-to-peak differential voltage of 2V is generated across TXOP, TXON when the effective differential load is 50Ω and REXT = 1KΩ.
RXGND	3, 23	Power	**Receive Ground.** Chip ground for receive circuity. RXGND should be connected to the printed circuit board's ground plane through a ferrite bead of value 0.2μH to 1μH.
RXIP, RXIN	2, 1	I/P	**Receive Input Positive, Receive Input Negative.** (MLT3 inputs if TPMODE = 0, NRZI inputs if TPMODE = 1). Receive differential data inputs.
RXOP, RXON	25, 24	PECL DIFF O/P	**Receive Output Positive, Receive Output Negative.** Differential NRZI receive data to the PHY chip. Do not tie external termination below 510Ω to RXGND. For 50Ω applications, 50Ω from the outputs to 3V may be connected.
RXVCC	26, 28	Power	**Receive Positive Supply.** The nominal value is 5V ±5%. RXVCC should be bypassed to RXGND with a 0.1μF chip capacitor placed as close to the pin as possible.

Preliminary Information

Pin Descriptions (continued)

Pin Name	Pin Number	Pin Type	Description
SDO	22	PECL O/P	**Signal Detect.** When SDO is HIGH, it indicates that the receive input is active. Do not tie any external termination resistor to SDO.
TXGND	11, 18, 19, 20	Power	**Transmit Ground.** Chip ground for transmit circuity. TXGND should be connected to the printed circuit board's ground plane through a ferrite bead of value 0.2μH to 1 μH.
TPMODE	6	TTL I/P	**Twisted Pair Encode Mode.** When TPMODE is LOW, the transmit output is MLT3 encoded with three levels. When TPMODE is HIGH, the transmit output is NRZI with two levels.
TXDIS	14	TTL I/P	**Transmit Disable.** If TXDIS is HIGH, the transmitter disables the TXOP, TXON output and presents a high impedance. If TXDIS is LOW, the transmitter enables normal data transmission through RCC615.
TXIP,TXIN	15,16	PECL DIFF I/P	**Transmit Input Positive, Transmit Input Negative.** Differential NRZI Transmit data from the PHY chip.
TXOP,TXON	9,8	O/P	**Transmit Output Positive, Transmit Output Negative.** (MLT3 outputs if TPMODE = 0, NRZI outputs if TPMODE = 1). Transmit differential current driver data outputs.
TXVCC	10,17	Power	**Transmit Positive Supply.** The nominal value is 5V ±5%. TXVCC should be bypassed to TXGND with a 0.1μF chip capacitor placed as close to the pin as possible.

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Min.	Max.	Units
Positive power supply	0	6	V
Voltage applied to any PECL/MLT3 outputs	-0.5	V_{CC}	V
Voltage applied to any TTL inputs	-0.5	V_{CC}	V
Voltage applied to any PECL inputs	-0.5	V_{CC}	V
Current from any PECL/MLT3 outputs	-50	+50	mA
Operating Temperature	0	70	°C
Storage Temperature	-65	150	°C
Junction Temperature	-55	150	°C
Lead Soldering (10 seconds)		300	°C

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter		Min.	Typ.	Max.	Units
Ta	Ambient Operating Temperature	0		70	°C
V_{CC}	Positive Supply Voltage (TXVCC and RXVCC)	4.75	5.00	5.25	V
R_{utp}	Unshielded Twisted Pair Differential Load Resistance	99.8	100	100.2	Ω
R_{stp}	Shielded Twisted Pair Differential Load Resistance	149.7	150	150.3	Ω

DC Electrical Characteristics

RXVCC, TXVCC = 5V ±5%, RXGND, TXGND = 0V, unless otherwise indicated

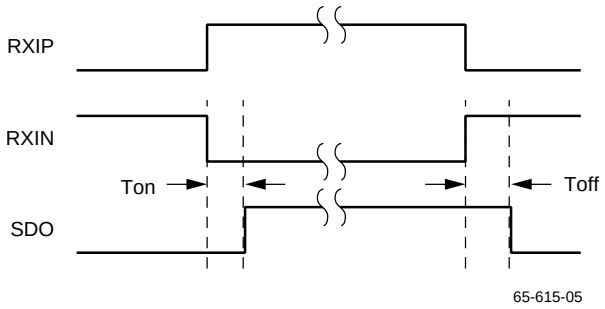
Parameter		Conditions	Min.	Typ.	Max.	Units
Transmitter Section						
Vihc	TTL input Voltage HIGH		2.0		V_{CC}	V
Vilc	TTL input Voltage LOW		0		0.8	V
Iinc	TTL Input Current				25	μA
C	Input Capacitance			3.0		pF
Vcm	Com. Mode Range (TXIP, TXIN)		3.3	3.7	4.1	V
Vdiff	Diff. Input Voltage (TXIP, TXIN)		0.4		2.0	Vpp
Iip	PECL Input Current		-20	0	20	μA
Vomh	MLT3 Positive Peak Voltage	Diff load R = 100Ω ±0.2% and 50Ω on both TXOP, TXON to VCC		4.2		V
Voml	MLT3 Negative Peak Voltage			3.2		V
Vohn	NRZI Output Voltage HIGH			4.2		V
Voln	NRZI Output Voltage LOW			3.2		V
Receiver Section						
Vdif	RXIP, RXIN Diff Input Voltage		0.4		2	V
Vcm	RXIP, RXIN Com. Mode Range			2.6		V
Vocm	RXOP, RXON Com. Mode Range	510Ω to GND on RXOP, RXON		V_{CC}–1.5		V
Vodiff	RXOP, RXON Diff Output Voltage			1.5		Vpp
Vohp	SDO Output HIGH		V_{CC}–1.1		V_{CC}–0.7	V
Volp	SDO Output LOW		V_{CC}–2		V_{CC}–1.4	V
Vonth	SDO Turnon threshold			350		mV
Vofth	SDO Turnoff threshold			260		mV
Power Section						
ICC	Power Supply Current			110		mA
PD	Power Dissipation			525		mW

Preliminary Information

Preliminary Information

AC Electrical Characteristics[1]

V_{CC} = 5V ±5%, GND = 0V, unless otherwise indicated

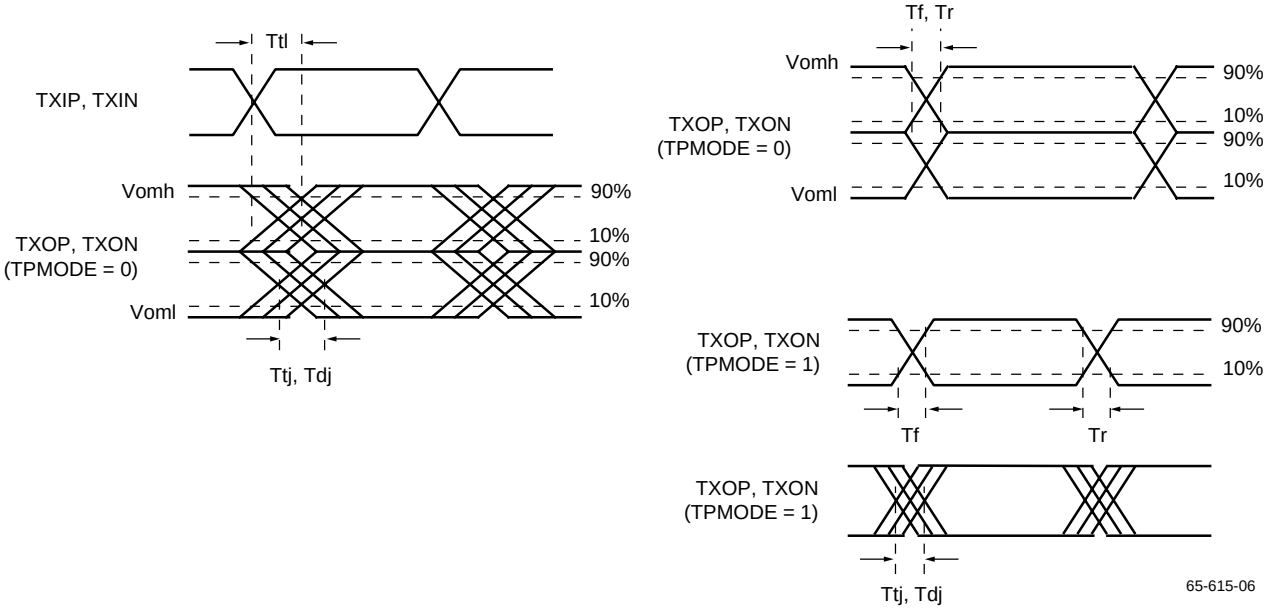


Parameter		Conditions	Min.	Typ.	Max.	Units
Receiver Section						
Ton	SDO turnon delay @ CEQ = 1000pF	Diff I/P > 1V		1	1000	µs
Toff	SDO turnoff delay @ CEQ = 1000pF	Diff I/P <0.2V		200	350	µs

Note:

1. Test conditions (unless otherwise indicated:) PECL Input rise and fall times ≤ 2ns, R_L = 100Ω. TTL Input rise and fall times ≤ 15ns. Transition density ≥ 0.1.

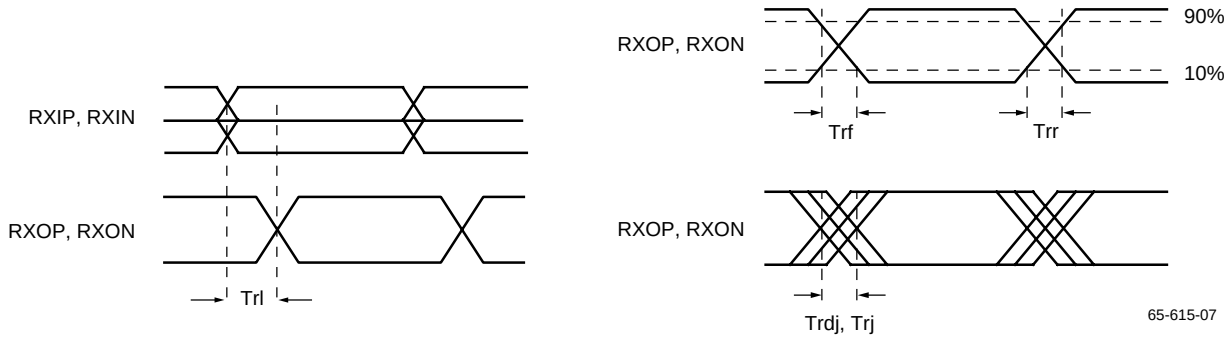
Timing Diagrams



Transmitter Timing

Parameter		Conditions	Min.	Typ.	Max.	Units
Tr	TXOP, TXON rise time 10% to 90%	100Ω termination		2.7		ns
Tf	TXOP, TXON fall time			2.7		ns
Tdj	TXOP, TXON duty cycle distortion (peak-to-peak)			0.3		ns
Ttj	Random jitter			300		ps
Ttl	Transmit latency			5.0		ns

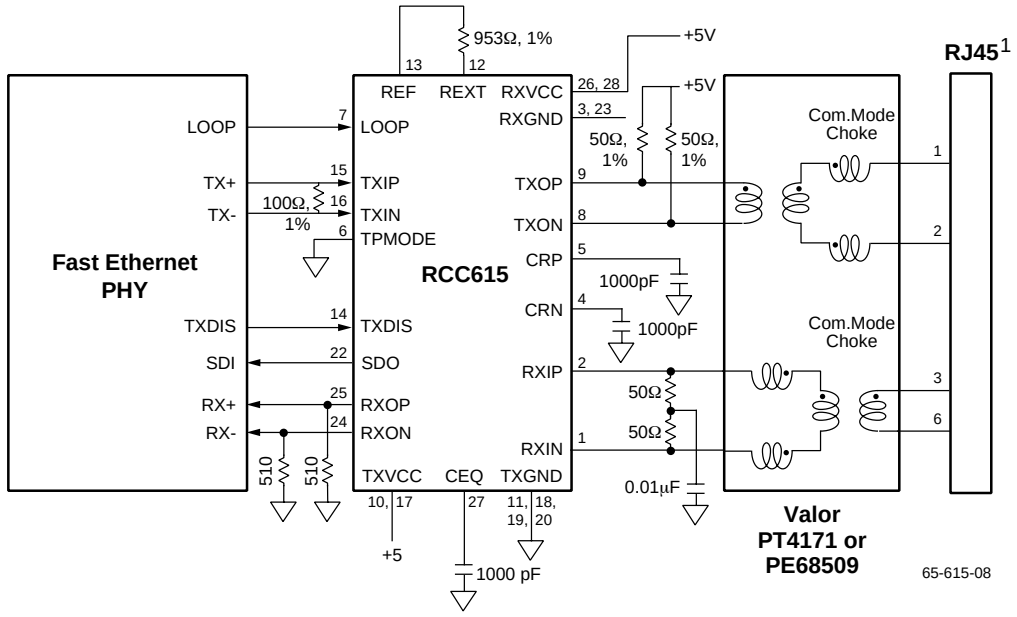
Timing Diagrams (continued)



Receiver Timing

Parameter		Conditions	Min.	Typ.	Max.	Units
Trr	RXOP, RXON rise time	10% to 90%		1.5		ns
Tfr	RXOP, RXON fall time	90% to 10%		1,5		ns
Trdj	RXOP, RXON duty cycle distortion (peak-to-peak) @ 100m calbe (UTP)			0.5		ns
Trj	RXOP,RXON peak to peak jitter			400		ps
Trl	Receive latency	@ 100m UTP		5		ns

Applications Discussion



Notes:

1. For FDDI applications, the receive pins are 7 and 8 instead of 3 and 6 on the RJ45 connector.
2. TXVCC and RXVCC should be connected individually to circuit board's +5 volts through ferrite bead of value 0.2μH to 1μH (e.g. FAIR-RITE BEAD #274-3019-446).
3. TXGND and RXGND should be connected individually to circuit board's ground through ferrite bead of value 0.2μH to 1μH (e.g. FAIR-RITE BEAD #276-3019-446). The current handling capability should be 100mA.
4. For 50Ω applications, RXOP, RXON may be connected with 50Ω to 3V.

Preliminary Information

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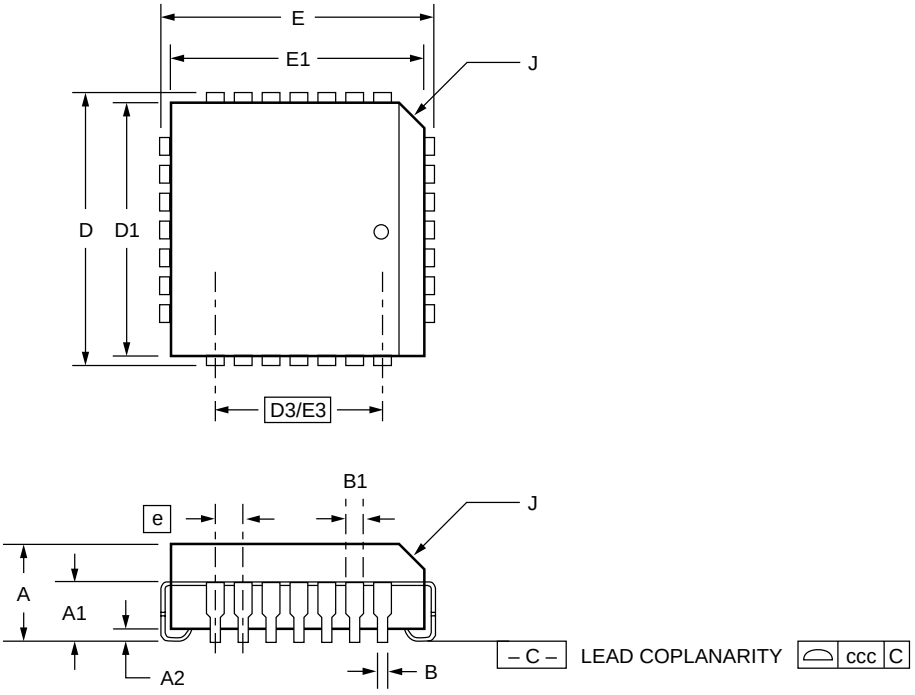
Mechanical Dimensions – 28 Lead PLCC (QA) Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.180	4.19	4.57	
A1	.090	.120	2.29	3.04	
A2	.020	—	.51	—	
B	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D/E	.485	.495	12.32	12.57	
D1/E1	.450	.456	11.43	11.58	
D3/E3	.300 BSC		7.62 BSC		
e	.050 BSC		1.27 BSC		
J	.042	.048	1.07	1.22	8
ND/NE	7		7		
N	28		28		
ccc		.004		0.10	

Notes:

1. Cavity mismatch = .004 (0.10mm)
2. Cavity frame offset = .002 (0.05mm) excluding leadframe tolerances.
3. Mold protrusions: Parting Line = .006 (0.15mm), Top or Bottom = .001 (0.025mm)
4. Variation in lead position = .005 (0.13mm)
5. Shoulder instrusions & protrusions: Intrusions = .002 (0.05mm), Protrusions = .003 (0.08mm)
6. Package warpage, WARP FACTOR = 2.5 = $\frac{\text{WARP (mils)}}{\text{Package Length (inches)}}$
7. Ejector pin depth = .010 (0.25mm) maximum.
8. Corner and edge chamfer = 45°C.



Preliminary Information

Ordering Information

Product Number	Package
RCC615V	28 PLCC

Preliminary Information

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

5/20/98 0.0m 001
Stock#DS50000615

RCC700A

Fibre Channel Transceiver

240 to 330 Megabaud

Features

- 240 to 330 Megabaud data rates
- Compliant with Fibre Channel standard
- Submicron CMOS technology
- PLL clock and data recovery
- Clock synthesizer
- Selectable 8 bit/10 bit encode, 10 bit/8 bit decode
- Parity generate/check
- Low power dissipation: 600 mW typ. at 250 Megabaud
- Byte sync on K28.1, K28.5 or K28.7
- Single power supply: +5V
- CMOS/TTL compatible parallel data inputs/outputs
- PECL compatible serial data inputs/outputs
- Available in 64-pin PQFP, 68 pin PLCC

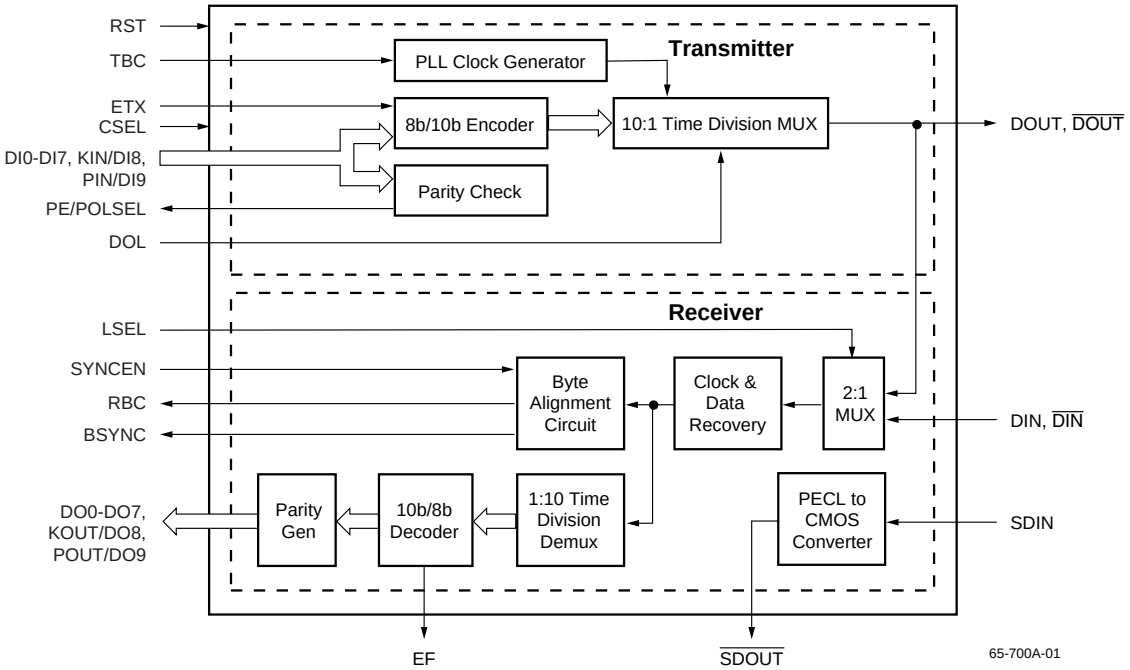
Applications

- Fibre Channel Transceiver
- High-speed Fiber Optics or Copper links
- High-resolution graphic display terminal
- LAN Switching
- Video data transmission

Description

The RCC700A is a monolithic transmitter/receiver IC integrating a complete phase-locked loop clock recovery and data retiming/regeneration subsystem, a phase-locked loop clock synthesizer, a 10:1 mux, a 1:10 demux, an 8-bit/10-bit encoder, and an 10-bit/8-bit decoder. It operates with a single +5V power supply. The RCC700A provides a complete physical interface in compliance with the Fibre Channel Physical Layer Standard (FC-PH) specifications at 265.625 Megabaud (Mbaud). 8 bit/10 bit encoder and 10 bit/8 bit decoder can be disabled through an external pin.

Block Diagram



Functional Description

Transmitter Section

The RCC700A transmitter section includes a phase-locked loop synthesizer, an 8-bit/10-bit encoder, an input parity checker and a 10:1 multiplexer. The RCC700A accepts a CMOS/TTL data byte (DI0-DI7) along with the K character indicator (KIN) and parity bit (PIN) for CSEL = 0. For CSEL = 1, KIN and PIN become DI8 and DI9, respectively.

The Parity Check circuitry calculates the odd parity of the input data byte and compares it with PIN. If the calculated parity differs from PIN, the transmitter flags the error by bringing the parity error bit, PE to a HIGH level. For example, for DI0-DI7=00000101, PIN should be 1. If PIN is not equal to 1, PE=1.

The RCC700A transmitter section encodes the CMOS/TTL input data bye (DI0-DI7) into a 10-bit word using IBM's 8-bit/10-bit coding (see Table 2). The encoder is disabled if CSEL = 1, and enabled if CSEL = 0. The encoded word is then converted to a serial high speed data stream (DOUT/$\overline{\text{DOUT}}$) at 240 to 330 Mbaud via a 10:1 time division mux. The serial data stream (DOUT/$\overline{\text{DOUT}}$) is transmitted at PECL levels (positive shifted ECL levels, Vth = +3.4V).

The RCC700A features a Data Output Low function (DOL) that can force the data output (DOUT, $\overline{\text{DOUT}}$) to logic LOW for protection of the fiber optic module transmitter diode. DOL is controlled by the Protocol IC or the fiber optic transmitter module. The RCC700A also incorporates an Error Transmit input (ETX). The RCC700A sends a violating code when ETX is brought to a logic HIGH. If ETX stays HIGH for more than one byte clock cycle, the transmitter will send error bytes of alternate running disparities in order to maintain the DC balance of the line (100111 1011 or 011000 0100).

The 240 to 330 MHz clock used for the serial stream is generated using a PLL clock generator which multiplies the input frequency, 24 to 33 MHz, by a factor of 10. The input clock reference for the PLL clock generator, Transmit Byte Clock (TBC), typically comes from a crystal oscillator or from the system.

Receiver Section

The RCC700A receiver section includes a complete phase-locked loop clock recovery and data retiming/regeneration subsystem, a byte alignment circuit, a 1:10 demultiplexer, an 10-bit/8-bit decoder, a disparity/code violation checker and a parity generator. The RCC700A accepts a differential data stream (DIN/$\overline{\text{DIN}}$) at 240 to 330 Mbaud, recovers the clock and regenerates the encoded serial data. The recovered encoded data is then converted to 10 parallel data lines via a 1:10 time division demultiplexer and decoded into an 8-bit byte via the 10-bit/8-bit decoder. The decoder is disabled if CSEL = 1, and enabled if CSEL = 0. K Command characters are also detected and indicated by bringing the KOUT pin to a HIGH level. The odd parity of the output 8-bit byte (DO0-DO7) is calculated and available at pin POUT. For example, for DO0-DO7=00000101, POUT should be 1. For CSEL = 1, KOUT and POUT become D08 and D09, respectively. The RCC700A also generates a Receive Byte Clock (RBC) for driving the CMOS protocol layer IC. All the outputs to the protocol layer IC are at CMOS levels.

Running disparity and coding is checked during the 10-bit/8-bit decoding and violations are flagged by bringing the Error Flag (EF) to a HIGH level. If consecutive bytes have more 1s or more 0s, or if running disparity is different from expected for the received code, or the transmission character is not part of Table 2, EF goes HIGH. If 100111 1011 or 011000 0100 is received, EF=1, KOUT=1, DO0-DO7=00000000.

The RCC700A contains a byte synchronization circuitry. When enabled (SYNCEN HIGH), the RCC700A will automatically resynchronize the demultiplexer to byte align with the leading seven bits (00111 11 or 11000 00) of the transmission character, corresponding to reception of K28.1, K28.5 or K28.7.

SYNCEN pin gives the protocol layer IC the flexibility to request the RCC700A to align only when required, e.g. at power up or after loss of byte synchronization. The RCC700A also incorporates a PECL to CMOS converter to translate the PECL output signal from an optical receiver module SDIN to a CMOS output signal. This allows for direct interfacing with the CMOS protocol layer circuit. SDIN is active HIGH. Therefore, $\overline{\text{SDOUT}}$ will be at a CMOS level LOW when an optical signal is present at the input of the fiber optics receiver module.

Loopback Test Mode

The RCC700A features an internal differential loopback for on-board diagnostic of the device. When loop select (LSEL) is HIGH, the receiver accepts the output data from the transmitter section (DOUT, $\overline{\text{DOUT}}$). When LSEL is LOW, i.e., tied to GND, the receiver accepts the incoming input data (DIN, $\overline{\text{DIN}}$).

Use of Table 2 for Encoding/ Decoding

The following information describes how Table 2 can be used for generating valid transmission characters (encoding) and checking the validity of received transmission characters (decoding).

The transmission character is labelled "abcdeifghj". The transmission order is a,b,c...j in that order. HGFEDCBA cor-

responds to the data inputs DI7...DI0 in that order. In the table, each valid data byte and special code byte has two columns corresponding to the current value of the running disparity (CURRENT RD- or CURRENT RD+). Running disparity is a binary parameter with either the value + or -.

The transmitter calculates the new running disparity based on the contents of the transmitted character. Similarly, the receiver calculates the new running disparity based on the contents of the received character.

The first six bits of the character, "abcdei," form one sub-block, and "fghj" forms another sub-block for computing running disparity. Running disparity (CURRENT RD+ or CURRENT RD-) at the beginning of the 6-bit sub-block is the running disparity at the end of the last transmission character. Running disparity at the beginning of the 4-bit sub-block is the running disparity at the end of the 6-bit sub-block. Running disparity at the end of the transmission character is the running disparity at the end of the 4-bit sub-block.

Running disparity for the sub-block is calculated as follows:

1. Running disparity at the end of any sub-block is positive if the sub-block contains more ones than zeros. It is also positive at the end of the six-bit sub-block if the six-bit sub-block is 000111, and it is positive at the end of the four-bit sub-block if the four-bit sub-block if 0011.

2. Running disparity at the end of any sub-block is negative if the sub-block contains more zeros than ones. It is also negative at the end of the six-bit sub-block if the six-bit sub-block is 111000, and it is negative at the end of the four-bit sub-block if the four-bit sub-block is 1100.

3. If neither of the above two conditions applies, running disparity at the end of the sub-block is the same as at the beginning of the sub-block.

CURRENT RD is used to select the transmission character for the data byte or special code.

While decoding the received character, the column corresponding to the current value of the receiver's running disparity shall be searched for the received transmission character. If the received transmission character is found in the proper column, the transmission character is considered valid and the associated data or special code byte decoded. Otherwise, the character is considered invalid and EF pin is held HIGH for that byte. Independent of the transmission character's validity, the received transmission character shall be used to calculate a new value of running disparity.

Detection of code violation (EF=HIGH) does not necessarily indicate that the transmission character in which the code violation was detected is in error. Code violation may occur due to the prior error which altered the running disparity of the bit stream but did not result in a detectable error at the transmission character in which it occurred. An example of an error scenario where the error is flagged after it happens is shown below (see Table 1).

Reset Function

For CSEL = 0, during normal operation, the reset input pin, RST, is LOW and is not used. Under total failure of receive PLL to acquire lock, this reset function can be used. When RST goes HIGH for at least 1 byte clock, the chip is reset, i.e. the receive PLL acquires lock to the bit clock derived from the TBC reference byte frequency and then to the incoming data.

For CSEL = 1, RST is normally HIGH and is LOW for at least 1 byte clock to reset.

Table 1. Example of Error Scenario

	RD	Character	RD	Character	RD	Character	RD
Transmitted character stream	-	D21.1	-	D10.2	-	D23.5	+
Transmitted bit stream	-	101010 1001	-	010101 0101	-	111010 1010	+
Bit stream after error	-	101010 1011	+	010101 0101	+	111010 1010	+
Decoded character stream	-	D21.0	+	D10.2	+	Error	+

Table 2. 8b/10b Encoding

DATA[3] BYTE NAME	BITS		CURRENT RD-		CURRENT RD+	
	HGF	EDCBA[1]	abcdei	fghj[2]	abcdei	fghj[2]
D0.0	000	00000	100111	0100	011000	1011
D1.0	000	00001	011101	0100	100010	1011
D2.0	000	00010	101101	0100	010010	1011
D3.0	000	00011	110001	1011	110001	0100
D4.0	000	00100	110101	0100	001010	1011
D5.0	000	00101	101001	1011	101001	0100
D6.0	000	00110	011001	1011	011001	0100
D7.0	000	00111	111000	1011	000111	0100
D8.0	000	01000	111001	0100	000110	1011
D9.0	000	01001	100101	1011	100101	0100
D10.0	000	01010	010101	1011	010101	0100
D11.0	000	01011	110100	1011	110100	0100
D12.0	000	01100	001101	1011	001101	0100
D13.0	000	01101	101100	1011	101100	0100
D14.0	000	01110	011100	1011	011100	0100
D15.0	000	01111	010111	0100	101000	1011
D16.0	000	10000	011011	0100	100100	1011
D17.0	000	10001	100011	1011	100011	0100
D18.0	000	10010	010011	1011	010011	0100
D19.0	000	10011	110010	1011	110010	0100
D20.0	000	10100	001011	1011	001011	0100
D21.0	000	10101	101010	1011	101010	0100
D22.0	000	10110	011010	1011	011010	0100
D23.0	000	10111	111010	0100	000101	1011
D24.0	000	11000	110011	0100	001100	1011
D25.0	000	11001	100110	1011	100110	0100
D26.0	000	11010	010110	1011	010110	0100
D27.0	000	11011	110110	0100	001001	1011
D28.0	000	11100	001110	1011	001110	0100
D29.0	000	11101	101110	0100	010001	1011
D30.0	000	11110	011110	0100	100001	1011
D31.0	000	11111	101011	0100	010100	1011
D0.1	001	00000	100111	1001	011000	1001
D1.1	001	00001	011101	1001	100010	1001
D2.1	001	00010	101101	1001	010010	1001
D3.1	001	00011	110001	1001	110001	1001
D4.1	001	00100	110101	1001	001010	1001
D5.1	001	00101	101001	1001	101001	1001
D6.1	001	00110	011001	1001	011001	1001
D7.1	001	00111	111000	1001	000111	1001
D8.1	001	01000	111001	1001	000110	1001
D9.1	001	01001	100101	1001	100101	1001
D10.1	001	01010	010101	1001	010101	1001
D11.1	001	01011	110100	1001	110100	1001
D12.1	001	01100	001101	1001	001101	1001
D13.1	001	01101	101100	1001	101100	1001
D14.1	001	01110	011100	1001	011100	1001
D15.1	001	01111	010111	1001	101000	1001

DATA[3] BYTE NAME	BITS		CURRENT RD-		CURRENT RD+	
	HGF	EDCBA[1]	abcdei	fghj[2]	abcdei	fghj[2]
D16.1	001	10000	011011	1001	100100	1001
D17.1	001	10001	100011	1001	100011	1001
D18.1	001	10010	010011	1001	010011	1001
D19.1	001	10011	110010	1001	110010	1001
D20.1	001	10100	001011	1001	001011	1001
D21.1	001	10101	101010	1001	101010	1001
D22.1	001	10110	011010	1001	011010	1001
D23.1	001	10111	111010	1001	000101	1001
D24.1	001	11000	110011	1001	001100	1001
D25.1	001	11001	100110	1001	100110	1001
D26.1	001	11010	010110	1001	010110	1001
D27.1	001	11011	110110	1001	001001	1001
D28.1	001	11100	001110	1001	001110	1001
D29.1	001	11101	101110	1001	010001	1001
D30.1	001	11110	011110	1001	100001	1001
D31.1	001	11111	101011	1001	010100	1001
D0.2	010	00000	100111	0101	011000	0101
D1.2	010	00001	011101	0101	100010	0101
D2.2	010	00010	101101	0101	010010	0101
D3.2	010	00011	110001	0101	110001	0101
D4.2	010	00100	110101	0101	001010	0101
D5.2	010	00101	101001	0101	101001	0101
D6.2	010	00110	011001	0101	011001	0101
D7.2	010	00111	111000	0101	000111	0101
D8.2	010	01000	111001	0101	000110	0101
D9.2	010	01001	100101	0101	100101	0101
D10.2	010	01010	010101	0101	010101	0101
D11.2	010	01011	110100	0101	110100	0101
D12.2	010	01100	001101	0101	001101	0101
D13.2	010	01101	101100	0101	101100	0101
D14.2	010	01110	011100	0101	011100	0101
D15.2	010	01111	010111	0101	101000	0101
D16.2	010	10000	011011	0101	100100	0101
D17.2	010	10001	100011	0101	100011	0101
D18.2	010	10010	010011	0101	010011	0101
D19.2	010	10011	110010	0101	110010	0101
D20.2	010	10100	001011	0101	001011	0101
D21.2	010	10101	101010	0101	101010	0101
D22.2	010	10110	011010	0101	011010	0101
D23.2	010	10111	111010	0101	000101	0101
D24.2	010	11000	110011	0101	001100	0101
D25.2	010	11001	100110	0101	100110	0101
D26.2	010	11010	010110	0101	010110	0101
D27.2	010	11011	110110	0101	001001	0101
D28.2	010	11100	001110	0101	001110	0101
D29.2	010	11101	101110	0101	010001	0101
D30.2	010	11110	011110	0101	100001	0101
D31.3	010	11111	101011	0101	010100	0101

Table 2. 8b/10b Encoding (continued)

DATA[3] BYTE NAME	BITS		CURRENT RD-		CURRENT RD+	
	HGF	EDCBA[1]	abcdei	fghj[2]	abcdei	fghj[2]
D0.3	011	00000	100111	0011	011000	1100
D1.3	011	00001	011101	0011	100010	1100
D2.3	011	00010	101101	0011	010010	1100
D3.3	011	00011	110001	1100	110001	0011
D4.3	011	00100	110101	0011	001010	1100
D5.3	011	00101	101001	1100	101001	0011
D6.3	011	00110	011001	1100	011001	0011
D7.3	011	00111	111000	1100	000111	0011
D8.3	011	01000	111001	0011	000110	1100
D9.3	011	01001	100101	1100	100101	0011
D10.3	011	01010	010101	1100	010101	0011
D11.3	011	01011	110100	1100	110100	0011
D12.3	011	01100	001101	1100	001101	0011
D13.3	011	01101	101100	1100	101100	0011
D14.3	011	01110	011100	1100	011100	0011
D15.3	011	01111	010111	0011	101000	1100
D16.3	011	10000	011011	0011	100100	1100
D17.3	011	10001	100011	1100	100011	0011
D18.3	011	10010	010011	1100	010011	0011
D19.3	011	10011	110010	1100	110010	0011
D20.3	011	10100	001011	1100	001011	0011
D21.3	011	10101	101010	1100	101010	0011
D22.3	011	10110	011010	1100	011010	0011
D23.3	011	10111	111010	0011	000101	1100
D24.3	011	11000	110011	0011	001100	1100
D25.3	011	11001	100110	1100	100110	0011
D26.3	011	11010	010110	1100	010110	0011
D27.3	011	11011	110110	0011	001001	1100
D28.3	011	11100	001110	1100	001110	0011
D29.3	011	11101	101110	0011	010001	1100
D30.3	011	11110	011110	0011	100001	1100
D31.3	011	11111	101011	0011	010100	1100
D0.4	100	00000	100111	0010	011000	1101
D1.4	100	00001	011101	0010	100010	1101
D2.4	100	00010	101101	0010	010010	1101
D3.4	100	00011	110001	1101	110001	0010
D4.4	100	00100	110101	0010	001010	1101
D5.4	100	00101	101001	1101	101001	0010
D6.5	100	00110	011001	1101	011001	0010
D7.5	100	00111	111000	1101	000111	0010
D8.5	100	01000	111001	0010	000110	1101
D9.5	100	01001	100101	1101	100101	0010
D10.4	100	01010	010101	1101	010101	0010
D11.4	100	01011	110100	1101	110100	0010
D12.4	100	01100	001101	1101	001101	0010
D13.4	100	01101	101100	1101	101100	0010
D14.4	100	01110	011100	1101	011100	0010
D15.4	100	01111	010111	0010	101000	1101

DATA[3] BYTE NAME	BITS		CURRENT RD-		CURRENT RD+	
	HGF	EDCBA[1]	abcdei	fghj[2]	abcdei	fghj[2]
D16.4	100	10000	011011	0010	100100	1101
D17.4	100	10001	100011	1101	100011	0010
D18.4	100	10010	010011	1101	010011	0010
D19.4	100	10011	110010	1101	110010	0010
D20.4	100	10100	001011	1101	001011	0010
D21.4	100	10101	101010	1101	101010	0010
D22.4	100	10110	011010	1101	011010	0010
D23.4	100	10111	111010	0010	000101	1101
D24.4	100	11000	110011	0010	001100	1101
D25.4	100	11001	100110	1101	100110	0010
D26.4	100	11010	010110	1101	010110	0010
D27.4	100	11011	110110	0010	001001	1101
D28.4	100	11100	001110	1101	001110	0010
D29.4	100	11101	101110	0010	010001	1101
D30.4	100	11110	011110	0010	100001	1101
D31.4	100	11111	101011	0010	010100	1101
D0.5	101	00000	100111	1010	011000	1010
D1.5	101	00001	011101	1010	100010	1010
D2.5	101	00010	101101	1010	010010	1010
D3.5	101	00011	110001	1010	110001	1010
D4.5	101	00100	110101	1010	001010	1010
D5.5	101	00101	101001	1010	101001	1010
D6.5	101	00110	011001	1010	011001	1010
D7.5	101	00111	111000	1010	000111	1010
D8.5	101	01000	111001	1010	000110	1010
D9.5	101	01001	100101	1010	100101	1010
D10.5	101	01010	010101	1010	010101	1010
D11.5	101	01011	110100	1010	110100	1010
D12.5	101	01100	001101	1010	001101	1010
D13.5	101	01101	101100	1010	101100	1010
D14.5	101	01110	011100	1010	011100	1010
D15.5	101	01111	010111	1010	101000	1010
D16.5	101	10000	011011	1010	100100	1010
D17.5	101	10001	100011	1010	100011	1010
D18.5	101	10010	010011	1010	010011	1010
D19.5	101	10011	110010	1010	110010	1010
D20.5	101	10100	001011	1010	001011	1010
D21.5	101	10101	101010	1010	101010	1010
D22.5	101	10110	011010	1010	011010	1010
D23.5	101	10111	111010	1010	000101	1010
D24.5	101	11000	110011	1010	001100	1010
D25.5	101	11001	100110	1010	100110	1010
D26.5	101	11010	010110	1010	010110	1010
D27.5	101	11011	110110	1010	001001	1010
D28.5	101	11100	001110	1010	001110	1010
D29.5	101	11101	101110	1010	010001	1010
D30.5	101	11110	011110	1010	100001	1010
D31.5	101	11111	101011	1010	010100	1010

Table 2. 8b/10b Encoding (continued)

DATA[3] BYTE NAME	BITS		CURRENT RD-		CURRENT RD+	
	HGF	EDCBA	abcdei	fghj[2]	abcdei	fghj[2]
D0.6	110	00000	100111	0110	011000	0110
D1.6	110	00001	011101	0110	100010	0110
D2.6	110	00010	101101	0110	010010	0110
D3.6	110	00011	110001	0110	110001	0110
D4.6	110	00100	110101	0110	001010	0110
D5.6	110	00101	101001	0110	101001	0110
D6.6	110	00110	011001	0110	011001	0110
D7.6	110	00111	111000	0110	000111	0110
D8.6	110	01000	111001	0110	000110	0110
D9.6	110	01001	100101	0110	100101	0110
D10.6	110	01010	010101	0110	010101	0110
D11.6	110	01011	110100	0110	110100	0110
D12.6	110	01100	001101	0110	001101	0110
D13.6	110	01101	101100	0110	101100	0110
D14.6	110	01110	011100	0110	011100	0110
D15.6	110	01111	010111	0110	101000	0110
D16.6	110	10000	011011	0110	100100	0110
D17.6	110	10001	100011	0110	100011	0110
D18.6	110	10010	010011	0110	010011	0110
D19.6	110	10011	110010	0110	110010	0110
D20.6	110	10100	001011	0110	001011	0110
D21.6	110	10101	101010	0110	101010	0110
D22.6	110	10110	011010	0110	011010	0110
D23.6	110	10111	111010	0110	000101	0110
D24.6	110	11000	110011	0110	001100	0110
D25.6	110	11001	100110	0110	100110	0110
D26.6	110	11010	010110	0110	010110	0110
D27.6	110	11011	110110	0110	001001	0110
D28.6	110	11100	001110	0110	001110	0110
D29.6	110	11101	101110	0110	010001	0110
D30.6	110	11110	011110	0110	100001	0110
D31.6	110	11111	101011	0110	010100	0110

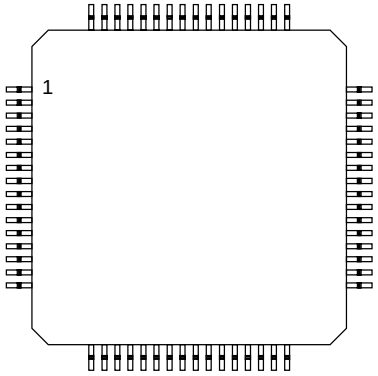
DATA[3] BYTE NAME	BITS		CURRENT RD-		CURRENT RD+	
	HGF	EDCBA	abcdei	fghj[2]	abcdei	fghj[2]
D0.7	111	00000	100111	0001	011000	1110
D1.7	111	00001	011101	0001	100010	1110
D2.7	111	00010	101101	0001	010010	1110
D3.7	111	00011	110001	1110	110001	0001
D4.7	111	00100	110101	0001	001010	1110
D5.7	111	00101	101001	1110	101001	0001
D6.7	111	00110	011001	1110	011001	0001
D7.7	111	00111	111000	1110	000111	0001
D8.7	111	01000	111001	0001	000110	1110
D9.7	111	01001	100101	1110	100101	0001
D10.7	111	01010	010101	1110	010101	0001
D11.7	111	01011	110100	1110	110100	1000
D12.7	111	01100	001101	1110	001101	0001
D13.7	111	01101	101100	1110	101100	1000
D14.7	111	01110	011100	1110	011100	1000
D15.7	111	01111	010111	0001	101000	1110
D16.7	111	10000	011011	0001	100100	1110
D17.7	111	10001	100011	0111	100011	0001
D18.7	111	10010	010011	0111	010011	0001
D19.7	111	10011	110010	1110	110010	0001
D20.7	111	10100	001011	0111	001011	0001
D21.7	111	10101	101010	1110	101010	0001
D22.7	111	10110	011010	1110	011010	0001
D23.7	111	10111	111010	0001	000101	1110
D24.7	111	11000	110011	0001	001100	1110
D25.7	111	11001	100110	1110	100110	0001
D26.7	111	11010	010110	1110	010110	0001
D27.7	111	11011	110110	0001	001001	1110
D28.7	111	11100	001110	1110	001110	0001
D29.7	111	11101	101110	0001	010001	1110
D30.7	111	11110	011110	0001	100001	1110
D31.7	111	11111	101011	0001	010100	1110

DATA[4] BYTE NAME	BITS		CURRENT RD-		CURRENT RD+	
	HGF	EDCBA[1]	abcdei	fghj[2]	abcdei	fghj[2]
K28.0	000	11100	001111	0100	110000	1011
K28.1	001	11100	001111	1001	110000	0110
K28.2	010	11100	001111	0101	110000	1010
K28.3	011	11100	001111	0011	110000	1100
K28.4	100	11100	001111	0010	110000	1101
K28.5	101	11100	001111	1010	110000	0101
K28.6	110	11100	001111	0110	110000	1001
K28.7	111	11100	001111	1000	110000	0111
K23.7	111	10111	111010	1000	000101	0111
K27.7	111	11011	110110	1000	001001	0111
K29.7	111	11101	101110	1000	010001	0111
K30.7	111	11110	011110	1000	100001	0111

Notes:

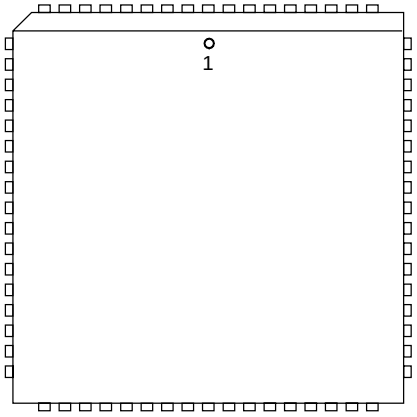
1. "HGF EDC BA" corresponds to DI7 ...0 in that order
2. a is to be transmitted first, followed by b, c, d ....j in that order
3. Kin=0
4. Kin=1

Pin Assignments



65-700A-02

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	DO2	17	DI7	33	DOUT	49	$\overline{\text{SDOUT}}$
2	DO1	18	DI6	34	$\overline{\text{DOUT}}$	50	CSEL
3	DO0	19	DI5	35	LSEL	51	SYNCEN
4	DVCC	20	DI4	36	AGND	52	BSYNC
5	DVCC	21	DI3	37	AVCC	53	DVCC
6	DGND	22	DI2	38	AVCC	54	DGND
7	DGND	23	DI1	39	AGND	55	DVCC
8	POUT/DO9	24	DI0	40	AGND	56	DGND
9	KOUT/DO8	25	DGND	41	AVCC	57	DVCC
10	EF	26	TBC	42	AVCC	58	DGND
11	RBC	27	DVCC	43	AGND	59	DO7
12	DGND	28	RST	44	AVCC	60	DO6
13	PE/POLSEL	29	DGND	45	AGND	61	DO5
14	PIN/DI9	30	DVCC	46	SDIN	62	DO4
15	KIN/DI8	31	DOL	47	$\overline{\text{DIN}}$	63	D03
16	ETX	32	DGND	48	DIN	64	DGND



65-700A-07

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	DGND	18	POUT/DO9	35	DI0	52	AGND
2	DVCC	19	KOUT/DO8	36	DGND	53	AVCC
3	DGND	20	EF	37	TBC	54	AVCC
4	DO7	21	RBC	38	DVCC	55	AGND
5	DO6	22	DGND	39	RST	56	AVCC
6	DO5	23	PE/POLSEL	40	DGND	57	AGND
7	DO4	24	PIN/DI9	41	DVCC	58	SDIN
8	DO3	25	KIN/DI8	42	DOL	59	$\overline{\text{DIN}}$
9	DGND	26	ETX	43	DGND	60	DIN
10	DGND	27	DGND	44	DOUT	61	DGND
11	DO2	28	DI7	45	$\overline{\text{DOUT}}$	62	$\overline{\text{SDOUT}}$
12	DO1	29	DI6	46	NC	63	CSEL
13	DO0	30	DI5	47	LSEL	64	SYNCEN
14	DVCC	31	DI4	48	AGND	65	BSYNC
15	DVCC	32	DI3	49	AVCC	66	DVCC
16	DGND	33	DI2	50	AVCC	67	DGND
17	DGND	34	DI1	51	AGND	68	DVCC

Pin Descriptions

Name	Pin Number		Function
	64-pin PQFP	68-pin PLCC	
DVCC	4, 5, 27, 30, 53, 55, 57	2, 14, 15, 38, 41, 66, 68	Positive supply for digital circuitry. The nominal value is 5V ±5%. VCC should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible.
AVCC	37, 38, 41, 42, 44	49, 50, 53, 54, 56	Positive supply for analog circuitry. The nominal value is 5V ±5%. VCC should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible.
DGND	6, 7, 12, 25, 29, 32, 54, 56, 58, 64	1, 3, 9, 10, 16, 17, 22, 27, 36, 40, 43, 61, 67	Chip ground for digital circuitry. DGND should be connected to the printed circuit board's ground plane at the pins.
AGND	36, 39, 40, 43, 45	48, 51, 52, 55, 57	Chip ground for analog circuitry. AGND should be connected to the printed circuit board's ground plane at the pins.
DI0-DI7	24, 23, 22, 21, 20, 19, 18, 17	35, 34, 33, 32, 31, 30, 29, 28	Transmitter input data (TTL levels).

Pin Descriptions (continued)

Name	Pin Number		Function
	64-pin PQFP	68-pin PLCC	
TBC	26	37	Transmit Byte Clock input (TTL level). Input reference frequency for the internal high speed clock generator: 24 to 33 MHz.
KIN/DI8	15	25	K character indicator input/Transmitter input data (TTL levels). If CSEL = 0, this pin in KIN. If CSEL = 1, this pin is DI8.
PIN/DI9	14	24	Odd parity input /Transmitter input data (TTL levels). If CSEL = 0, this pin in PIN. If CSEL = 1, this pin is DI9.
PE/ POLSEL	13	23	Parity Error indicator output/Polarity Select Input (CMOS/TTL levels). For CSEL = 0, This pin is PE. For CSEL = 1, This pin is POLSEL. PE will stay low when the on-chip calculated odd parity matches the incoming parity PIN. If there is a parity error, the PE flag is raised to a level HIGH. If POLSEL = 0, the receive data output timing specifications are with respect to the positive edge of RBC. If POLSEL = 1, the above specifications are with respect to the negative edge of RBC.
DOUT/ $\overline{\text{DOUT}}$	33,34	44,45	Transmitter differential output data (PECL levels). The output is a current mode driver with a nominal current driver of 8 mA. To generate a 0.8 V swing, use a 100Ω resistor across DOUT, $\overline{\text{DOUT}}$.
DOL	31	42	Data Output Low control input (TTL level). When HIGH, it forces the output to a logic low state (DOUT = LOW and $\overline{\text{DOUT}}$ = HIGH) to protect the fiber optic source. Connect to GND or leave open when not used.
LSEL	35	47	Loop Select input (TTL level). Internal differential loopback for "on-board" diagnostic of the device. When loop select (LSEL) is HIGH, the receiver accepts the output data from the transmitter section (DOUT/$\overline{\text{DOUT}}$). When LSEL is LOW, i.e. tied to GND, the receiver accepts the incoming input data (DIN/$\overline{\text{DIN}}$). Connect to GND or leave open when not used.
DIN/$\overline{\text{DIN}}$	48, 47	60, 59	Receiver differential input data (PECL levels).
SYNCEN	51	64	Byte Synchronization Enable input (TTL level). When SYNCEN is HIGH, the RCC700A will automatically resynchronize the demultiplexer to byte align with the received K28.1, K28.5 or K28.7 for both negative and positive running disparities (RD- and RD+). Connect to GND or leave open when not used.
BSYNC	52	65	Byte Synchronized output flag (CMOS levels). BSYNC goes to a HIGH level for one byte clock when SYNCEN is HIGH and the RCC700A detects and resynchronizes on K28.1, K28.5 or K28.7.
SDIN	46	58	Signal Detect input (PECL level). PECL input of the PECL to CMOS converter for the signal detect flag of the fiber optics receiver module. Leave open when not used.
$\overline{\text{SDOUT}}$	49	62	Signal Detect Output (CMOS level). CMOS output of the PECL to CMOS converter for the signal detect flag of the fiber optics receiver module. $\overline{\text{SDOUT}}$ is LOW when SDIN is HIGH.
DO0-DO7	3, 2, 1, 63, 62, 61, 60, 59	13, 12, 11, 8, 7, 6, 5, 4	Receiver output data/Receive output data (CMOS levels).
KOUT/DO8	9	19	K character indicator output / Receive Output Data (CMOS level). If CSEL = 0, this pin is KOUT. If CSEL = 1, this pin is DO8.
POUT/DO9	8	18	Odd parity output/Receive output data (CMOS level). If CSEL = 0, this pin is POUT. POUT is HIGH when the parity of the DO0...DO7 byte is even. If CSEL = 1, this pin is DO9.

Pin Descriptions (continued)

Name	Pin Number		Function
	64-pin PQFP	68-pin PLCC	
RBC	11	21	Receive Byte Clock output (CMOS level): 24 to 33 MHz.
EF	10	20	Error Flag output (CMOS level). EF goes HIGH to flag running disparity and coding violations detected during the 10b/8b decoding.
RST	28	39	Asynchronous reset input (TTL level). For CSEL = 0, this pin is normally LOW, and when HIGH for at least one byte clock, is used to reset all functions of the chip. This is a master reset. For CSEL = 1, this pin is normally HIGH, and when LOW for at least one byte clock, provides reset.
ETX	16	26	Error Transmit input (TTL level). This pin is only applicable of CSEL = 0 and is a No Connect for CSEL = 1. This pin is normally LOW. This pin, when HIGH, is used to force DC balanced alternating violation codes on its serial output.
CSEL	50	63	Select input (TTL level). This pin is normally low and enables the 8b/10b encoder/decoder circuitry. When high, the 8b/10b encoder/decoder is disabled and the following pins are affected: PIN/DI9, KIN/DI8, POUT/DO9, KOUT/DO8, PE/POLSEL, RST, and ETX.
NC	—	46	No connection.

Absolute Maximum Ratings[1]

Parameter	Min	Max	Unit
Storage temperature range	-65	150	°C
Junction temperature range	-55	150	°C
Lead temperature range (soldering, 10 seconds)		300	°C
Positive power supply, V_{CC}	0	6	V
Voltage applied to any TTL inputs	-1	6	V
Voltage applied to any CMOS inputs	-1	6	V
Voltage applied to any PECL inputs	-1	6	V
Voltage applied to any CMOS outputs	-1	6	V
Voltage applied to any PECL outputs	-1	6	V
Current from any CMOS outputs	-50	50	mA
Current from any PECL outputs	-50	50	mA

Note:

1. “Absolute maximum ratings” are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply the device should be operated at these limits. If the device is subjected to the limits in the absolute maximum ratings for extended periods, its reliability may be impaired. The tables of Electrical Characteristics provide conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameters	Min	Typ	Max	Units
T_A	Ambient operating temperature	0		70	°C
V_{CC}	Positive supply voltage (DVCC and AVCC)	4.75	5.0	5.25	V
R_I	PECL differential load resistance[1]	80	100	150	Ω

Note:

1. Differential load resistance of 100Ω equals connection of 50Ω to AC ground on each of DOUT, $\overline{DOUT}$.

DC Electrical Characteristics

V_{CC} = 5V ±5%, GND = 0V unless otherwise indicated.

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
Transmitter						
V_{IH}	TTL input voltage HIGH		2.0		V_{CC} +0.5	V
V_{IL}	TTL input voltage LOW				0.8	V
I_{IH}	TTL input HIGH current	V_{CC} = max, V_{IN} = 2.7V			100	µA
I_{IL}	TTL input LOW current	V_{CC} = max, V_{IN} = 0.4V	-1		100	µA
C_I	Input capacitance			4	10	pF
V_{OHP}	PECL output voltage HIGH	R_{DIFF} = 100Ω, V_{CC} = 5V	3.5	3.8	4.2	V
V_{OLP}	PECL ouput voltage LOW	R_{DIFF} = 100Ω, V_{CC} = 5V	2.6	3.0	3.4	V
V_{OP}	PECL output voltage amplitude	V_{OHP} - V_{OLP}, V_{CC} = 5V	0.6	0.8	1.0	V
I_O	PECL output current			8		mA
Receiver						
V_{IH}	TTL input voltage HIGH		2.0		V_{CC} +0.5	V
V_{IL}	TTL input voltage LOW		0		0.8	V
I_{IH}	TTL input HIGH current	V_{CC} = max, Vin = 2.7V			100	µA
I_{IL}	TTL input LOW current	V_{CC} = max, Vin = 0.4V			-100	µA
V_{CM}	Com. mode range (DIN, $\overline{DIN}$)		2.8		4.5	V
V_{DIFF}	Diff. input voltage (DIN, $\overline{DIN}$)		0.4			V
I_{IPH}	PECL input HIGH current	V_{IH} = V_{CC} -0.88V			100	µA
I_{IPL}	PECL input LOW current	V_{IL} = V_{CC} - 1.81V	-100			µA
V_{OHC}	CMOS output voltage HIGH	I_{OH}= -4.1mA (-8.1mA for RBC)	3.5		V_{CC}	V
V_{OLC}	CMOS output voltage LOW	I_{OL}= 4.1 mA (8.1 mA for RBC)	0		0.5	V
I_{OLC}	Output current (except RBC)	Forcing V_{OH}, V_{OL}	4			mA
I_{OLC}	Output current (RBC)	Forcing V_{OH}, V_{OL}	8			mA
I_{CC}	Supply Current (266 Mbaud)	V_{CC} = 5.25V		135	150	mA
PD	Power dissipation (266 Mbaud)	Based on I_{CC}		690		mW

Note:

1. Under both transmit and receive output switching conditions

AC Electrical Characteristics[1]

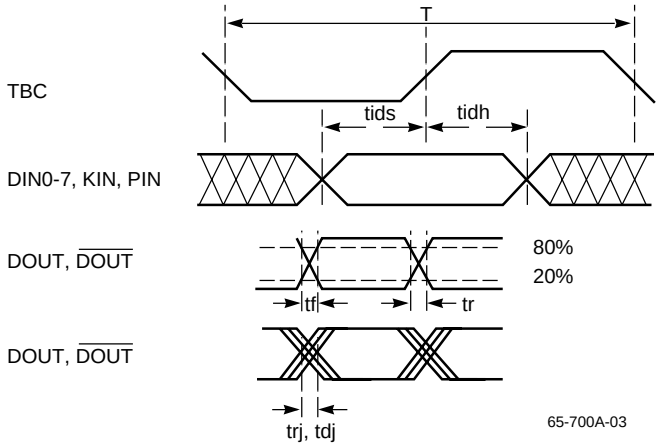
V_{CC} = 5V ±5%, GND = 0V unless otherwise indicated.

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
Transmitter						
T	TBC Period	266 Mbaud		37.7		ns
t_{acq}	Acquisition time	Note 2			1	ms
t_{ids}[6]	DIN0..7, KIN, PIN valid to TBC setup ↑		4			ns
t_{idh}[6]	TBC ↑ to DIN0..7, KIN, PIN invalid hold		4			ns
F_{out}	Output data rate		240		330	Mbaud
t_r, t_f	DOUT, $\overline{DOUT}$ rise and fall times	20% to 80% points			500	ps
t_{rj}	DOUT, $\overline{DOUT}$ pk-pk random jitter	Note 3		220		ps
t_{dj}	DOUT, $\overline{DOUT}$ pk-pk deterministic jitter	Note 4		125		ps
Receiver						
f_{cc}	Input data rate variation				±1000	ppm
D	Input data transition density to acquire and maintain lock		0.25			
t_{acq}	Loop acquisition time for 1E-12 BER				2500	bits
f_c	Loop capture range		±1000			ppm
t_j	DIN, $\overline{DIN}$ input peak to peak jitter	Note 5			0.07T	ns
t_h	RBC pulsewidth HIGH		0.4T	0.5T	0.6T	ns
t_{od}[6, 7]	RBC ↑ to DO0..7 KOUT, POUT, BSYNC delay (CSEL = 0, or CSEL = 1, POLSEL = 0)	266 Mbaud	15		25	ns
T	RBC period	266 Mbaud		37.7		ns

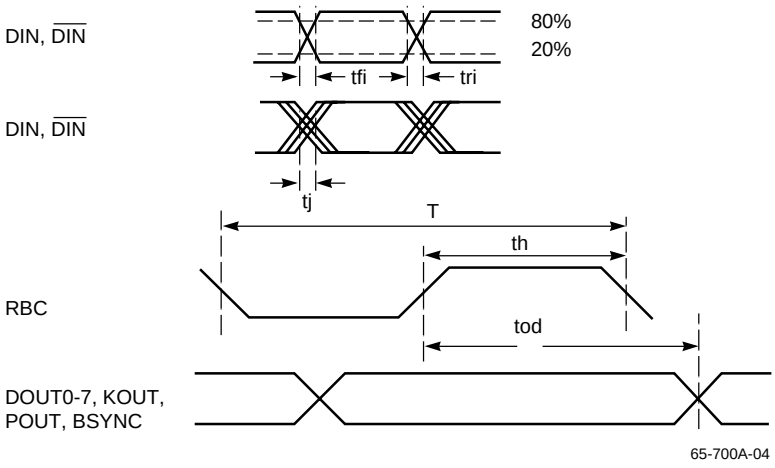
Notes:

1. Test conditions (unless otherwise indicated): PECL input rise and fall times, ≤2 ns, RLOAD = 100Ω across DOUT, $\overline{DOUT}$; TTL input rise and fall times ≤15 ns. Receiver input data rate = 265.625 Mbaud and ±1000 ppm; transition density ≥ 0.25.
2. Acquisition time is the time to establish lock once the device is powered up to the operating VCC range.
3. Input test pattern K28.7. Jitter measured at 50% amplitude, for a BER of 1E-12 with receiver running asynchronously.
4. Input test pattern K28.5. Jitter measured at 50% amplitude.
5. Guaranteed by design.
6. For CSEL = 0, the input pins are DI0..7, KIN and PIN, and the output pins are DO0..7, KOUT, and POUT. For CSEL = 1, the input pins are DI0..DI9, and the output pins are DO0..9.
7. For CSEL = 1 and POLSEL = 1, the timing specifications are with respect to the negative edge of RBC.

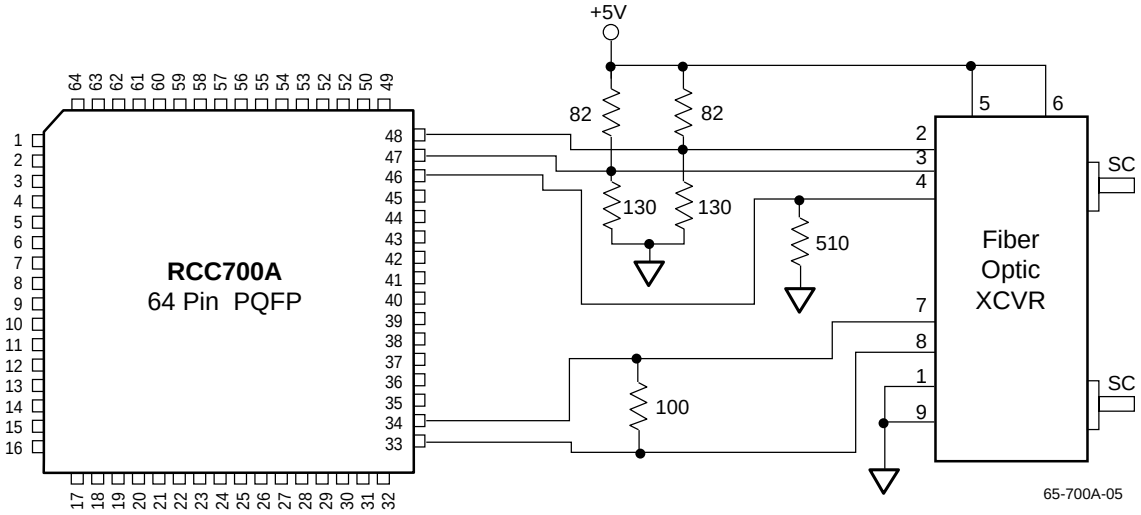
Transmitter Timing



Receiver Timing



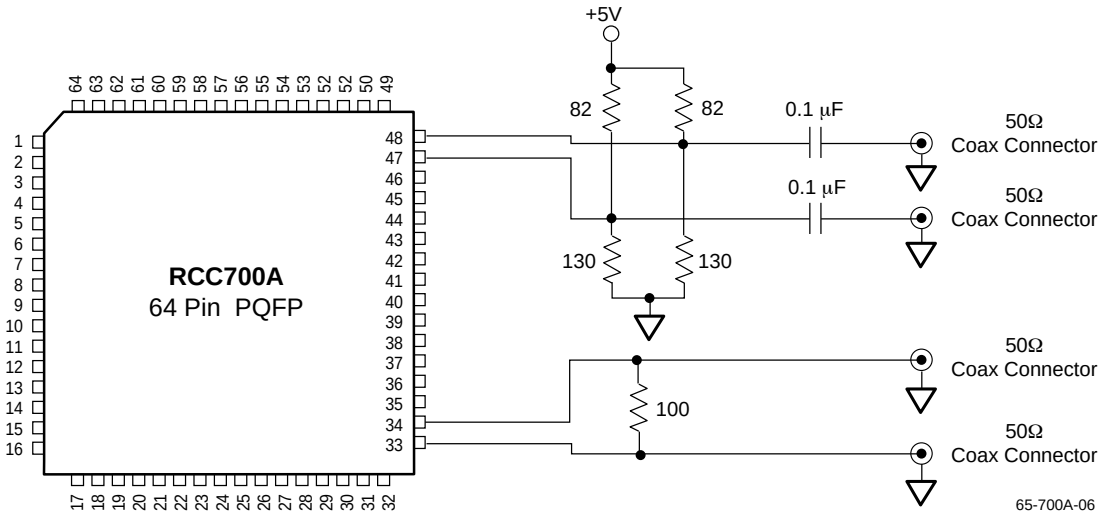
Applications Discussion



Interconnection of RCC700A to a Fiber Optic Transceiver

Recommended Fiber Optic Transceivers:

1. HP BR-5302
2. Siemens V23806-A7-C2



Interconnection of RCC700A to a Coax Cable

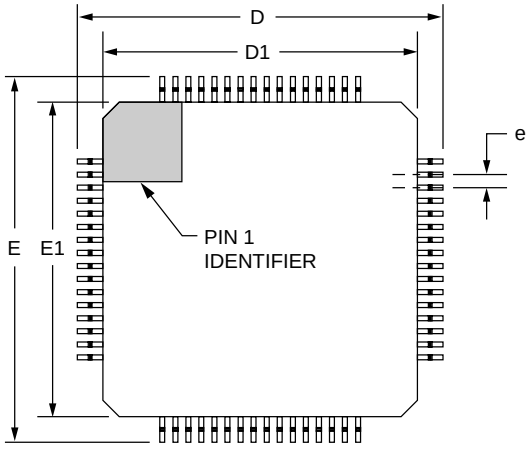
Mechanical Dimensions

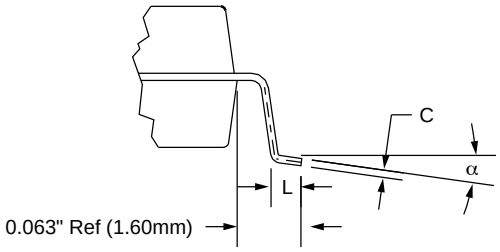
64-Lead MQFP Package

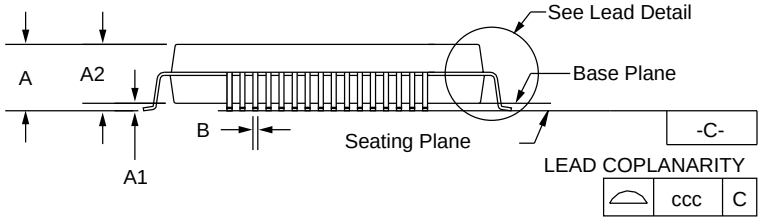
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.096	—	2.45	
A1	.010	—	.25	—	
A2	.077	.083	1.95	2.10	
B	.007	.011	.17	.27	7
D/E	.510	.530	12.95	13.45	
D1/E1	.390	.398	9.90	10.10	2
e	.020 BSC		.50 BSC		
L	.031	.040	.78	1.03	6
N	64		64		4
ND	16		16		5
α	0°	7°	0°	7°	
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Dimensions "D1" and "E1" do not include mold protrusion.
3. Pin 1 identifier is optional.
4. Dimension N: number of terminals.
5. Dimension ND: Number of terminals per package edge.
6. "L" is the length of terminal for soldering to a substrate.
7. "B" includes lead finish thickness.







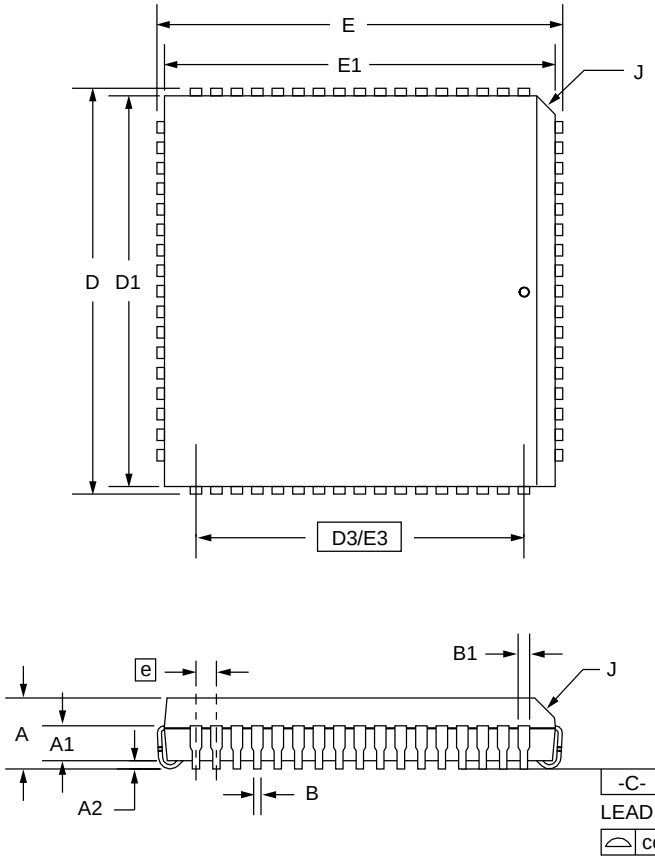
Mechanical Dimensions (continued)

68-Lead PLCC Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.200	4.19	5.08	
A1	.090	.130	2.29	3.30	
A2	.020	—	.51	—	
B	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D/E	.985	.995	25.02	25.27	
D1/E1	.950	.958	24.13	24.33	3
D3/E3	.800 BSC		20.32 BSC		
e	.050 BSC		1.27 BSC		
J	.042	.056	1.07	1.42	2
ND/NE	17		17		
N	68		68		
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982
2. Corner and edge chamfer (J) = 45°
3. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is .101" (.25mm)



Ordering Information

Part Number	Package
RCC700AKA	64 PQFP
RCC700AQD	68 PLCC

RCXXXX

Offline Battery Charger

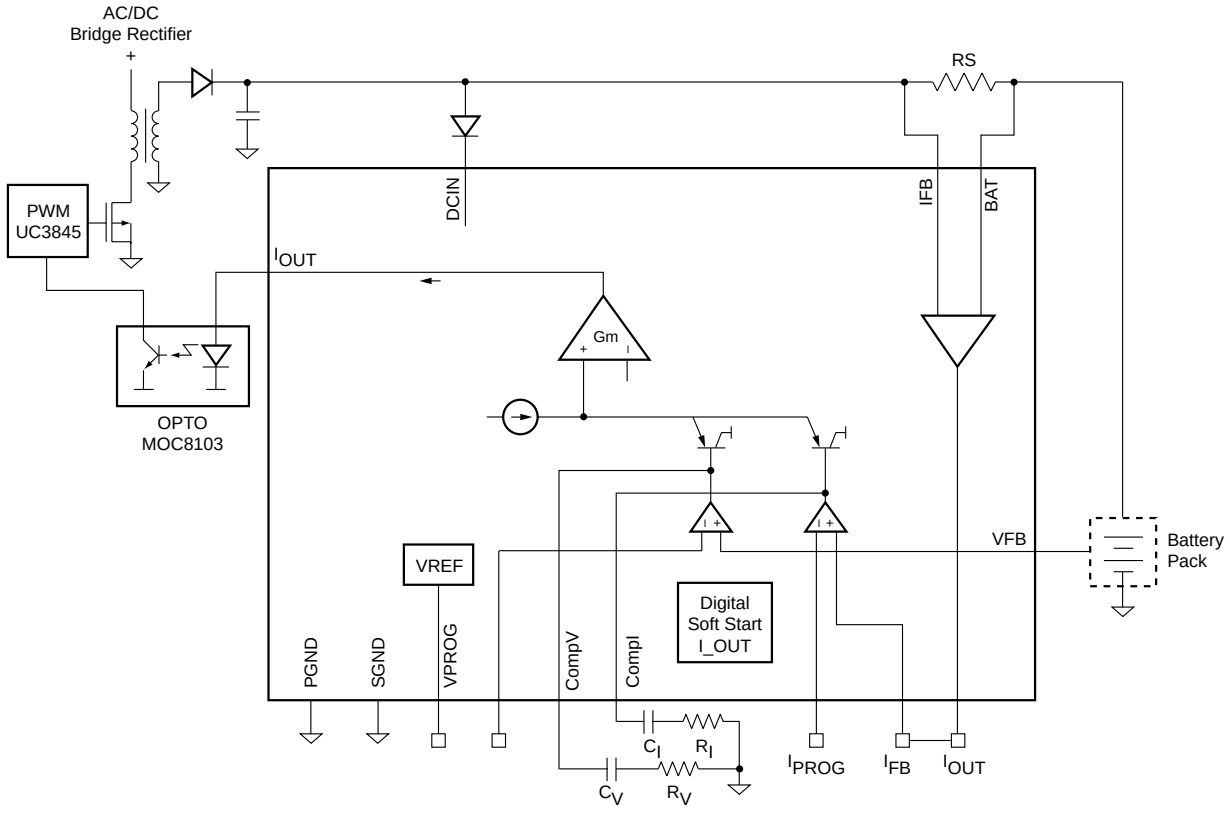
Features

- Very high precision
- Chemistry independent

Applications

- Offline applications
- Portable PCs
- PDAs
- Cellular telephones

Block Diagram



Target Specification