

Features

- Fast Read Access Time - 120 ns
- Automatic Page Write Operation
 - Internal Address and Data Latches for 128 Bytes
 - Internal Control Timer
- Fast Write Cycle Time
 - Page Write Cycle Time - 10 ms maximum
 - 1 to 128 Byte Page Write Operation
- Low Power Dissipation
 - 80 mA Active Current
 - 300 μ A CMOS Standby Current
- Hardware and Software Data Protection
- DATA Polling for End of Write Detection
- High Reliability CMOS Technology
 - Endurance: 10^4 or 10^5 Cycles
 - Data Retention: 10 years
- Single 5 V $\pm$ 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout
- Full Military, Commercial and Industrial Temperature Ranges

**1 Megabit
(128K x 8)
Paged
CMOS
E²PROM**

Description

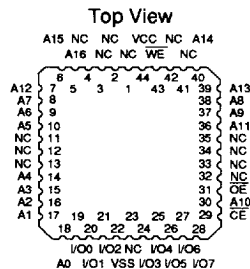
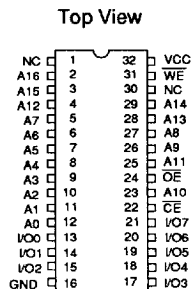
The AT28C010 is a high-performance Electrically Erasable and Programmable Read Only Memory. Its one megabit of memory is organized as 131,072 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 120 ns with power dissipation of just 440 mW. When the device is deselected, the CMOS standby current is less than 300 μ A.

The AT28C010 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 128-byte page register to allow writing of up to 128 bytes simultaneously. During a write cycle, the address and 1 to 128 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by DATA polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

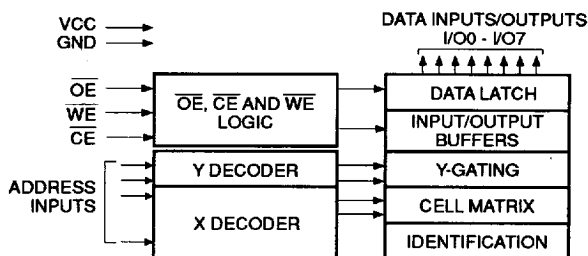
Atmel's 28C010 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 128 bytes of E²PROM for device identification or tracking.

Pin Configurations

Pin Name	Function
A0 - A16	Addresses
CE	Chip Enable
OE	Output Enable
WE	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect



Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6 V to +6.25 V
All Output Voltages with Respect to Ground	-0.6 V to V _{CC} + 0.6 V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6 V to +13.5 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28C010 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

BYTE WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion.

PAGE WRITE: The page write operation of the AT28C010 allows one to one hundred twenty-eight bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by one to one hundred twenty-seven additional bytes. Each successive byte must be written within 150 μ s (t_{BLC}) of the previous byte. If the

t_{BLC} limit is exceeded the AT28C010 will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A7-A16 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A7 - A16 must be the same.

The A0 to A6 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

DATA POLLING: The AT28C010 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{DATA}$ Polling may begin at anytime during the write cycle.

(continued on next page)

Device Operation (Continued)

TOGGLE BIT: In addition to $\overline{\text{DATA}}$ Polling the AT28C010 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION: Hardware features protect against inadvertent writes to the AT28C010 in the following ways: (a) VCC sense - if VCC is below 3.8 V (typical) the write function is inhibited; (b) VCC power-on delay - once VCC has reached 3.8 V the device will automatically time out 5 ms (typical) before allowing a write; (c) write inhibit - holding any one of OE low, $\overline{\text{CE}}$ high or $\overline{\text{WE}}$ high inhibits write cycles; (d) noise filter - pulses of less than 15 ns (typical) on the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature has been implemented on the AT28C010. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28C010 is shipped from Atmel with SDP disabled.

SDP is enabled by the host system issuing a series of three write commands; three specific bytes of data are written to three specific addresses (refer to Software Data Protection Algorithm). After writing the three byte command sequence and after two the entire AT28C010 will be protected against inadvertent write operations. It should be noted, that once protected the host may still perform a byte or page write to the AT28C010. This is done by preceding the data to be written by the same three byte command sequence used to enable SDP.

Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP and SDP will protect the AT28C010 during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not written to the device and the memory addresses used in the sequence may be written with data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the three byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of two, read operations will effectively be polling operations.

DEVICE IDENTIFICATION: An extra 128 bytes of E²PROM memory are available to the user for device identification. By raising A9 to 12 V $\pm$ 0.5 V and using address locations 1FF80H to 1FFFFH the bytes may be written to or read from in the same manner as the regular memory array.

Pin Capacitance (f = 1 MHz, T = 25°C) ⁽¹⁾

	Typ	Max	Units	Conditions
C _{IN}	4	10	pF	V _{IN} = 0 V
C _{OUT}	8	12	pF	V _{OUT} = 0 V

Note: 1. This parameter is characterized and is not 100% tested.



D.C. and A.C. Operating Range

		AT28C010-12	AT28C010-15	AT28C010-20	AT28C010-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
Vcc Power Supply		5 V ± 10%	5 V ± 10%	5 V ± 10%	5 V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V _{IL}	V _{IL}	V _{IH}	DOUT
Write ⁽²⁾	V _{IL}	V _{IH}	V _{IL}	DIN
Standby/Write Inhibit	V _{IH}	X ⁽¹⁾	X	High Z
Write Inhibit	X	X	V _{IH}	
Write Inhibit	X	V _{IL}	X	
Output Disable	X	V _{IH}	X	High Z

Notes: 1. X can be V_{IL} or V_{IH}.

2. Refer to A.C. Programming Waveforms.

D.C. Characteristics

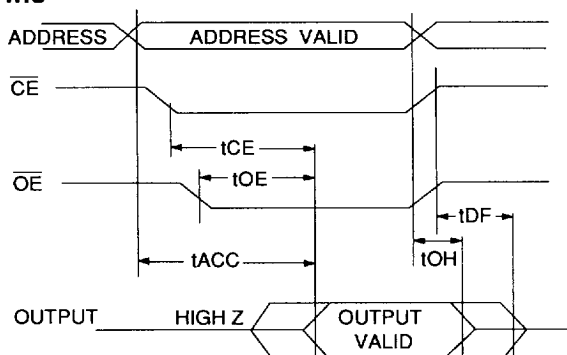
Symbol	Parameter	Condition	Min	Max	Units
I _{LI}	Input Load Current	V _{IN} = 0 V to V _{CC} + 1 V		10	μA
I _{LO}	Output Leakage Current	V _{IO} = 0 V to V _{CC}		10	μA
I _{SB1}	Vcc Standby Current CMOS	$\overline{CE}$ = V _{CC} - 0.3 V to V _{CC} + 1 V		300	μA
I _{SB2}	Vcc Standby Current TTL	$\overline{CE}$ = 2.0 V to V _{CC} + 1 V		3	mA
I _{CC}	Vcc Active Current	f = 5 MHz; I _{OUT} = 0 mA		80	mA
V _{IL}	Input Low Voltage			0.8	V
V _{IH}	Input High Voltage		2.0		V
V _{OL}	Output Low Voltage	I _{OL} = 2.1 mA		.45	V
V _{OH1}	Output High Voltage	I _{OH} = -400 μA	2.4		V
V _{OH2}	Output High Voltage CMOS	I _{OH} = -100 μA; V _{CC} = 4.5 V	4.2		V

A.C. Read Characteristics

Symbol	Parameter	AT28C010-12		AT28C010-15		AT28C010-20		AT28C010-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		120		150		200		250	ns
$t_{CE}^{(1)}$	$\overline{CE}$ to Output Delay		120		150		200		250	ns
$t_{OE}^{(2)}$	$\overline{OE}$ to Output Delay	0	50	0	55	0	55	0	55	ns
$t_{DF}^{(3,4)}$	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	50	0	55	0	55	0	55	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

2

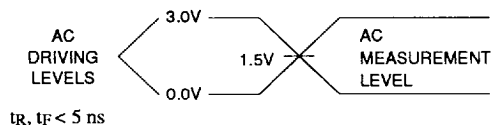
A.C. Read Waveforms



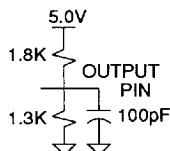
Notes:

- $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC} .
- $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC} .
- t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first ($C_L = 5pF$).
- This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



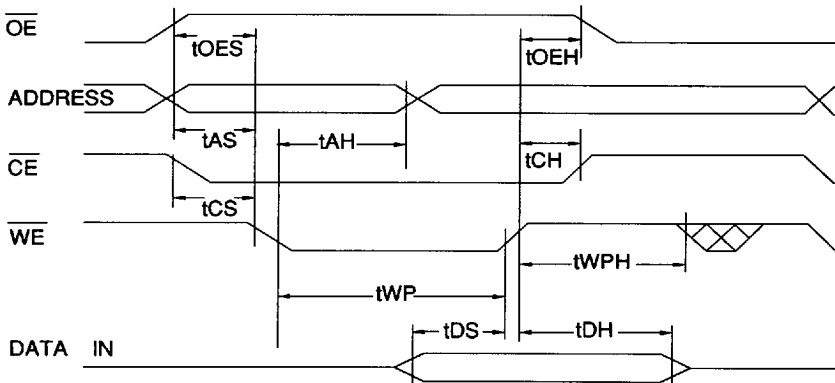
Output Test Load



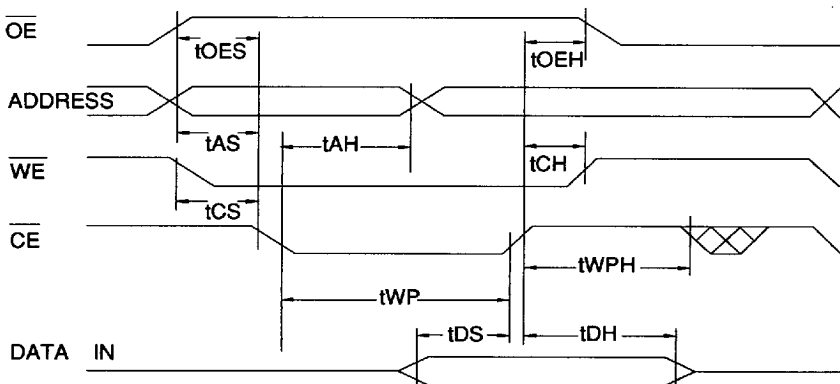
A.C. Write Characteristics

Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEh}	Data, $\overline{OE}$ Hold Time	0		ns
t_{WC}	Write Cycle Time		10	ms

A.C. Write Waveforms- $\overline{WE}$ Controlled



A.C. Write Waveforms- $\overline{CE}$ Controlled

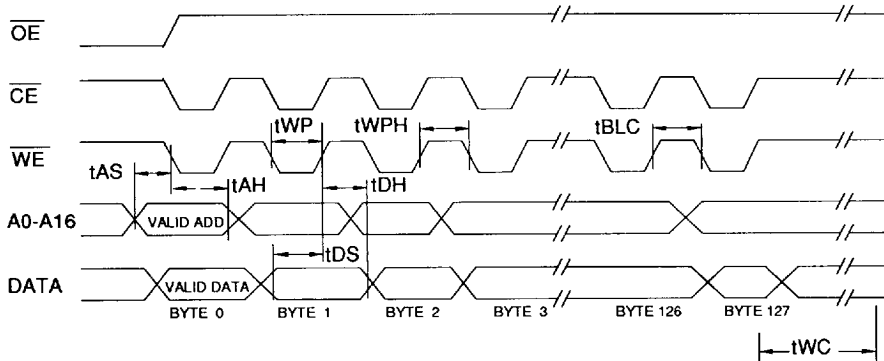


Page Mode Characteristics

Symbol	Parameter	Min	Max	Units
t _{WC}	Write Cycle Time		10	ms
t _{AS}	Address Set-up Time	0		ns
t _{AH}	Address Hold Time	50		ns
t _{DS}	Data Set-up Time	50		ns
t _{DH}	Data Hold Time	0		ns
t _{WP}	Write Pulse Width	100		ns
t _{BLC}	Byte Load Cycle Time		150	μs
t _{WPH}	Write Pulse Width High	50		ns

2

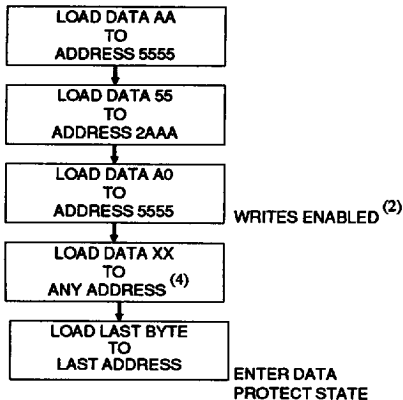
Page Mode Write Waveforms



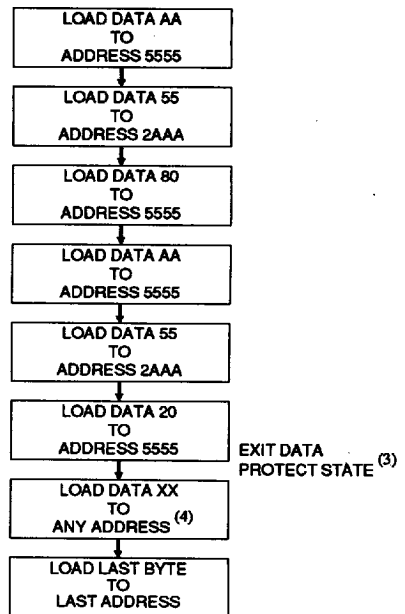
Notes: A7 through A16 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
 $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.



Software Data Protection Enable Algorithm ⁽¹⁾



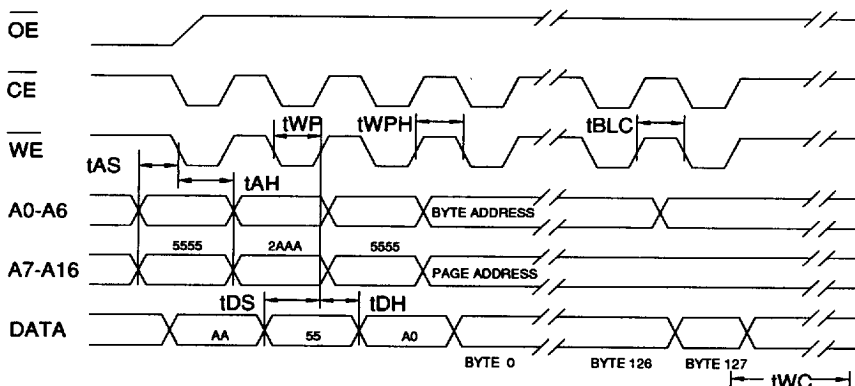
Software Data Protection Disable Algorithm ⁽¹⁾



Notes:

1. Data Format: I/O7 - I/O0 (Hex); Address Format: A14 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 128 bytes of data are loaded.

Software Protected Program Cycle Waveform



- Notes:
- A0-A14 must conform to the addressing sequence for the first three bytes as shown above.
 - After the command sequence has been issued and a page write operation follows, the page address inputs (A7-A16) must be the same for each high to low transition of WE (or CE).
 - OE must be high only when WE and CE are both low.

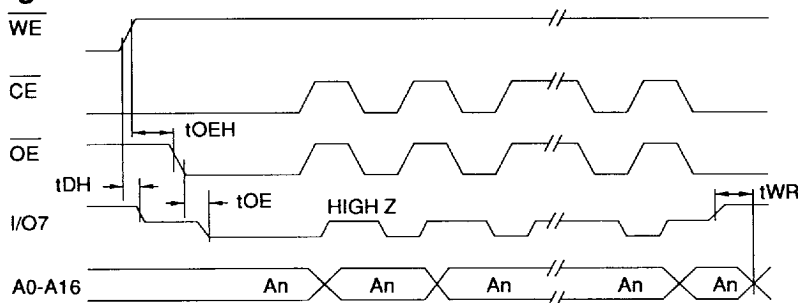
Data Polling Characteristics⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Units
t _{DH}	Data Hold Time	10			ns
t _{OE}	$\overline{OE}$ Hold Time	10			ns
t _{OE}	$\overline{OE}$ to Output Delay			100	ns
t _{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

2

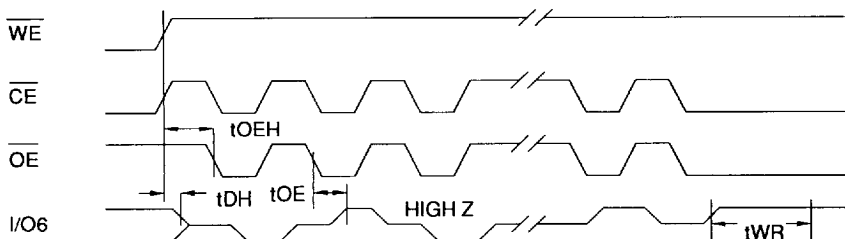
Data Polling Waveforms

Toggle Bit Characteristics⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Units
t _{DH}	Data Hold Time	10			ns
t _{OE}	$\overline{OE}$ Hold Time	10			ns
t _{OE}	$\overline{OE}$ to Output Delay			100	ns
t _{OEHP}	$\overline{OE}$ High Pulse	150			ns
t _{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

Toggle Bit Waveforms



Notes:

1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.



2-191

1074177 0005134 467

Ordering Information

t _{ACC} (ns)	I _{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	80	0.3	AT28C010-12BC (E)	32B	Commercial (0° to 70°C)
			AT28C010-12FC	32F	
			AT28C010-12LC (E)	44L	
			AT28C010-12BI (E)	32B	Industrial (-40° to 85°C)
			AT28C010-12FI	32F	
			AT28C010-12LI (E)	44L	Military (-55°C to 125°C)
			AT28C010-12BM (E)	32B	
			AT28C010-12FM	32F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			AT28C010-12LM (E)	44L	
150	80	0.3	AT28C010-12BM/883 (E)	32B	Commercial (0° to 70°C)
			AT28C010-12FM/883	32F	
			AT28C010-12LM/883 (E)	44L	
			AT28C010-15BC (E)	32B	Industrial (-40° to 85°C)
			AT28C010-15FC	32F	
			AT28C010-15LC (E)	44L	
			AT28C010-15UC	30U	
			AT28C010-15VC	V	Military (-55°C to 125°C)
			AT28C010-15BI (E)	32B	
			AT28C010-15FI	32F	
			AT28C010-15LI (E)	44L	
			AT28C010-15UI	30U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			AT28C010-15VI	V	
			AT28C010-15BM (E)	32B	
			AT28C010-15FM	32F	
200	80	0.3	AT28C010-15LM (E)	44L	Commercial (0° to 70°C)
			AT28C010-15UM	30U	
			AT28C010-15VM	V	
			AT28C010-15BM/883 (E)	32B	Industrial (-40° to 85°C)
			AT28C010-15FM/883	32F	
			AT28C010-15LM/883 (E)	44L	
			AT28C010-15UM/883	30U	
			AT28C010-20BC (E)	32B	Military (-55°C to 125°C)
			AT28C010-20FC	32F	
			AT28C010-20LC (E)	44L	
			AT28C010-20UC	30U	
			AT28C010-20VC	V	Commercial (0° to 70°C)
			AT28C010-20BI (E)	32B	
			AT28C010-20FI	32F	
			AT28C010-20LI (E)	44L	
			AT28C010-20UI	30U	Industrial (-40° to 85°C)
			AT28C010-20VI	V	
			AT28C010-20BM (E)	32B	
			AT28C010-20FM	32F	
			AT28C010-20LM (E)	44L	Military (-55°C to 125°C)
			AT28C010-20UM	30U	
			AT28C010-20VM	V	

Ordering Information

t _{ACC} (ns)	I _{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	80	0.3	AT28C010-20BM/883 (E) AT28C010-20FM/883 AT28C010-20LM/883 (E) AT28C010-20UM/883	32B 32F 44L 30U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	80	0.3	AT28C010-25BC (E) AT28C010-25FC AT28C010-25LC (E) AT28C010-25UC AT28C010-25VC AT28C010-W	32B 32F 44L 30U V DIE	Commercial (0° to 70°C)
			AT28C010-25BI (E) AT28C010-25FI AT28C010-25LI (E) AT28C010-25UI AT28C010-25VI	32B 32F 44L 30U V	Industrial (-40° to 85°C)
			AT28C010-25BM (E) AT28C010-25FM AT28C010-25LM (E) AT28C010-25UM AT28C010-25VM	32B 32F 44L 30U V	Military (-55°C to 125°C)
			AT28C010-25BM/883 (E) AT28C010-25FM/883 AT28C010-25LM/883 (E) AT28C010-25UM/883	32B 32F 44L 30U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	80	0.3	5962-38267 07M XX 5962-38267 07M YX 5962-38267 07M ZX	32B 44L 32F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	80	0.3	5962-38267 05M XX 5962-38267 05M YX 5962-38267 05M ZX	32B 44L 32F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	80	0.3	5962-38267 03M XX 5962-38267 03M YX 5962-38267 03M ZX	32B 44L 32F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	80	0.3	5962-38267 01M XX 5962-38267 01M YX 5962-38267 01M ZX	32B 44L 32F	Military/883C Class B, Fully Compliant (-55°C to 125°C)

2




Ordering Information

Package Type	
32B	32 Lead, 0.600" Wide, Ceramic Side Braze Dual Inline (Side Braze)
32F	32 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
44L	44 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
30U	30 Pin, Ceramic Pin Grid Array (PGA)
V	Tape Automated Bond (TAB) Carrier
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles