RC56CSM and RC56DDP
Downloadable Digital Central Site Modem Device Family

Introduction

The Rockwell RC56CSM and RC56DDP Digital Central Site Modem Device Family supports one or more channels of high speed PSTN data, ISDN data, and fax. Integrated modem controller, controller firmware and data pump functions are available in RC56CSM models supporting one or two channels. Also offered are data pump-only functions in RC56DDP models supporting one or four channels. (See Table 1 and Figure 1.) The downloadable RC56CSM and RC56DDP architecture allows upgrading of modem controller and data pump firmware from the central site controller.

Rockwell K56Plus technology allows data to be transmitted from a digitally connected, central site modem at speeds up to 56 kbps. Taking advantage of the PSTN, which is primarily digital except for the client modem to central office local loop, the RC56CSM modem is ideal for remote access applications such as Internet Server Provider, on-line service, or corporate site. Data can be received at speeds up to 33.6 kbps.

The RC56CSM achieves higher density in the central site modem application by eliminating the analog front end. The ability to directly interface to digital PCM data makes the RC56CSM ideal for central site modem equipment capable of supporting high capacity T1/E1/PRI connections. Compact form factors make the device set perfect for equipment designed with the goal of increasing channel count and improving modem density.

The RC56CSM is intended for use with a digital network connection, and can also interface to a separately available quad analog front end. In supporting both linear inputs from dial-up lines and PCM inputs from the digital connection, the chipset enables manufacturers to produce equipment which scales from dial-up lines to T1/E1/PRI lines using one RC56CSM chipset. Note: 56k bps and ISDN operation is not possible when the RC56CSM chipset is used with a separate analog front end.

A sleep mode with quick wake up reduces power consumption. Thermal vias in BGA packages further aid heat dissipation. These features, combined with a glueless interface to a T1/E1/PRI framer, provide maximum channel density in application designs.

Terminating both PSTN data and fax calls, as well as digital ISDN calls, the RC56CSM eliminates the need for equipment manufacturers and equipment users to supply dedicated ISDN channels and to pre-determine what percentage of channels should support ISDN. This increases system flexibility and allows the system to run at higher capacity.

The RC56CSM device set accepts a digital μ-law or A-law PCM data stream. This data stream is one channel of a T1/E1 or Primary Rate ISDN signal. The RC56CSM interprets the digital data stream to process the analog modulation for a remote analog source (analog modem or analog fax machine) or to provide HDLC control for a remote digital source (ISDN terminal adapter).

As a data modem, the RC56CSM operates at line speeds up to 56,000 bps downstream and up to 33,600 bps upstream with a PSTN remote modem. Error correction (V.42/MNP 2-4) and data compression (V.42 bis/MNP 5) maximize data transfer integrity and boost average data throughput by a factor of four. Non-error-correcting mode is also supported.

In ISDN B Channel call termination mode, the modem performs HDLC control, including HDLC Flag generation/detection, bit stuffing/extraction, and CRC generation/checking on a 64 kbps PCM data stream provided by a Primary Rate Interface line. Also supported are 56 kbps ISDN B channels. Call setup must be handled by the central site system controller (CSSC).

As a fax modem, the RC56CSM supports Group 3 send and receive rates up to 14,400 bps, T.30 protocol, and EIA/TIA 578 Class 1 and Class 2.

The RC56CSM device set supports one channel and consists of a modem controller (MCU) and a digital data pump (DDP), each packaged in an 80-pin PQFP. The RC56CSM/2 supports two channels and is packaged in a single 268-pin BGA. In each case, the OEM adds memory and discrete components to complete the modem. A SRAM loader executable in the MCU is available to download MCU firmware from the CSSC into MCU SRAM. DDP firmware downloaded by the MCU to the DDP during normal operation is transparent to the CSSC.

MCU firmware is available for customization. A PC-based "ConfigurACE" utility program allows the OEM to configure MCU firmware options to suit specific applications. Demonstration hardware is available.

Features

- Downloadable modem controller and data pump firmware
- Data modem modes
  - PSTN: K56Plus, upgradable to ITU-T 56 kbps 33.6 kbps, V.34, V.32 bis, V.32, V.22 bis, V.22A/B, V.23, and V.21; Bell 212A and 103
  - ISDN: 64 kbps ISDN Basic Rate Interface B Channel
- ISDN data line speeds up to 64 kbps (including 56 kbps ISDN B channels)
  - HDLC control
  - Data pass-through mode for HDLC processing elsewhere in the central site system
- Internal error correction and data compression (ECC)
  - V.42 LAPM, MNP 2-4, and MNP 10 error correction
  - V.42 bis and MNP 5 data compression
- MNP 10EC™ enhanced cellular performance
- Low-power sleep mode with quick wake.
- Glueless interface to T1/E1/PRI framer
- Optional interface to separately available analog front end
- Multi frequency tone support for legacy network equipment
- Fax modem send and receive rates up to 14400 bps
  - V.33, V.17, V.29, V.27 ter, and V.21 channel 2
  - Group 3, T.30 protocol and Class 1, 2 supported
- Parallel 16550A-compatible host interface
- SRAM loader available for host download to MCU
- Flow control and speed buffering
- Communications software compatible AT command sets
- NVRAM directory and stored profiles
- +5V operation

Table 1. RC56CSM Family Models and Supported Channels

Model	Channels Supported	No. of Devices	Controller Functions Provided	Packaging
RC56CSM/2 Integrated Modem	2	1	2	One 268-pin BGA providing two MCU functions and two RC56DDP functions
RC56CSM Integrated Modem	1	2	1	One 80-pin PQFP providing one MCU function and one 80-pin PQFP providing one RC56DDP function
RC56DDP/4 Digital Data Pump	4	1	None	One 268-pin BGA providing four RC56DDP functions
RC56DDP Digital Data Pump	1	1	None	One 80-pin PQFP providing one RC56DDP function

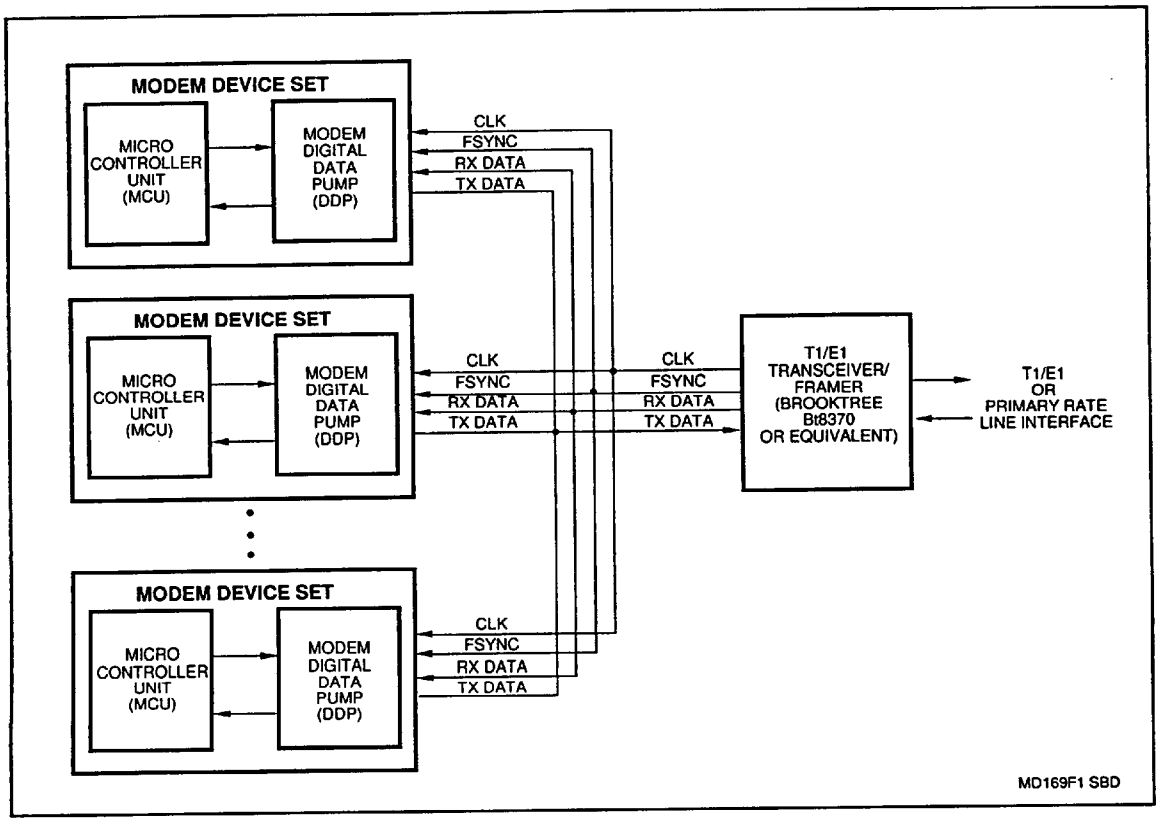

Figure 1. System Block Diagram

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Technical Specifications

General Description

The RC56CSM device set provides the processing core for one or more channels of a central site modem system supporting high speed T1/E1/PRI digital lines. The OEM adds an oscillator, discrete components, and digital interface circuitry to complete the modem channels.

A system block diagram is shown in Figure 1.

The modem is a full-featured, self-contained data modem/fax modem solution shown in Figure 2 and Figure 3. Data modem handshake, fax modem protocol, and ISDN data connection functions are supported and controlled through the AT command set.

Data pump only implementations are also available as illustrated in Figure 4 and Figure 5.

Modem Digital Data Pump (DDP)

The DDP is a Rockwell data pump supporting PSTN data/fax modem operation and ISDN B Channel call termination mode. The DDP executes internal firmware including downloadable modules.

Digital data transfers serially between the T1/E1 framer device and the DDP at a data rate up to 8.192 Mbps. The T1/E1 framing device provides a strobe signal so the DDP can detect where the data for the channel starts in the serial TDM data stream using a programmable counter. The DDP performs PCM μ-law or A-law conversion and synchronizes with an external clock.

The DDP can be configured to operate with a separately available Rockwell Quad Analog Front End.

Microcontroller (MCU)

The MCU performs the command processing and interfaces to the central site system controller via a parallel 16550A UART compatible host bus interface. The MCU may be supplied by Rockwell or by the OEM.

The MCU connects to the DDP via dedicated lines and the external bus. The MCU external bus also connects to OEM-supplied memory. A SRAM loader is available to support download from the central site system controller on startup if desired.

Modem Operation

In data modem modes, each modem channel can independently connect to PSTN data modems at rates up to 56 kbps or ISDN terminal adapters at rates up to 64 kbps.

For PSTN modems, complete handshake and data rate negotiations are performed. By optimizing the modem configuration for line conditions, the DDP can connect at the highest data rate that the channel can support from 56 kbps to 300 bps with automatic fallback. Automode operation in V.34 is provided in accordance with PN3320 and in V.32 bis in accordance with PN2330. All tone and pattern detection functions required by the applicable ITU or Bell standard are supported.

When the remote end is an ISDN terminal adapter, the RC56CSM provides HDLC control including HDLC Flag generation/detection, bit stuffing/extraction, and CRC generation/checking.

In fax modem mode, the RC56CSM supports Group 3 facsimile send and receive speeds of 14400, 12000, 9600, 7200, 4800, or 2400 bps. Fax modem modes support T.30 fax requirements. Fax data transmission and reception performed by the modem is controlled and monitored through the EIA-578 Class 1 and Class 2 command interface.

Both transmit and receive fax data are buffered within the modem. Data transfer to and from the central site modem system controller is flow controlled by XON/XOFF or RTS/CTS.

Modem Firmware

Modem firmware performs processing of general modem control, command sets, error correction and data compression, fax class 1 and class 2, and central site system controller interface functions.

The modem firmware is provided in object code form for the OEM to run out of external non-volatile memory or to download on startup to external volatile memory. The modem firmware may also be provided in source code form under a source code addendum license agreement.

Hardware Interface Signals

The RC56CSM/2 interface is illustrated in Figure 2.

The RC56CSM interface is illustrated in Figure 3.

The RC56DDP/4 interface is illustrated in Figure 4.

The RC56DDP interface is illustrated in Figure 5.

The 268-pin BGA package identifying pin locations for the RC56CSM/2 and the RC56DDP/4 is shown in Figure 6.

The RC56CSM/2 pin signals in the 268-pin BGA are listed by location in Table 2 and by signal in Table 3.

The RC56DDP/4 pin signals in the 268-pin BGA are listed by location in Table 4 and by signal in Table 5.

The MCU pin signals in the 80-pin PQFP are shown in Figure 7.

The RC56DDP pin signals in the 80-pin PQFP are shown in Figure 8.

Electrical and Environmental Specifications

The current and power requirements are listed in Table 6.

The absolute maximum ratings are listed in Table 7.

Additional Information

Additional information is described in the RC56CSM Modem Designer's Guide (Order No. 1127), the RC56DDP Modem Designer's Guide (Order No. 1126), and the AT Command Reference Manual (Order No. 1048).

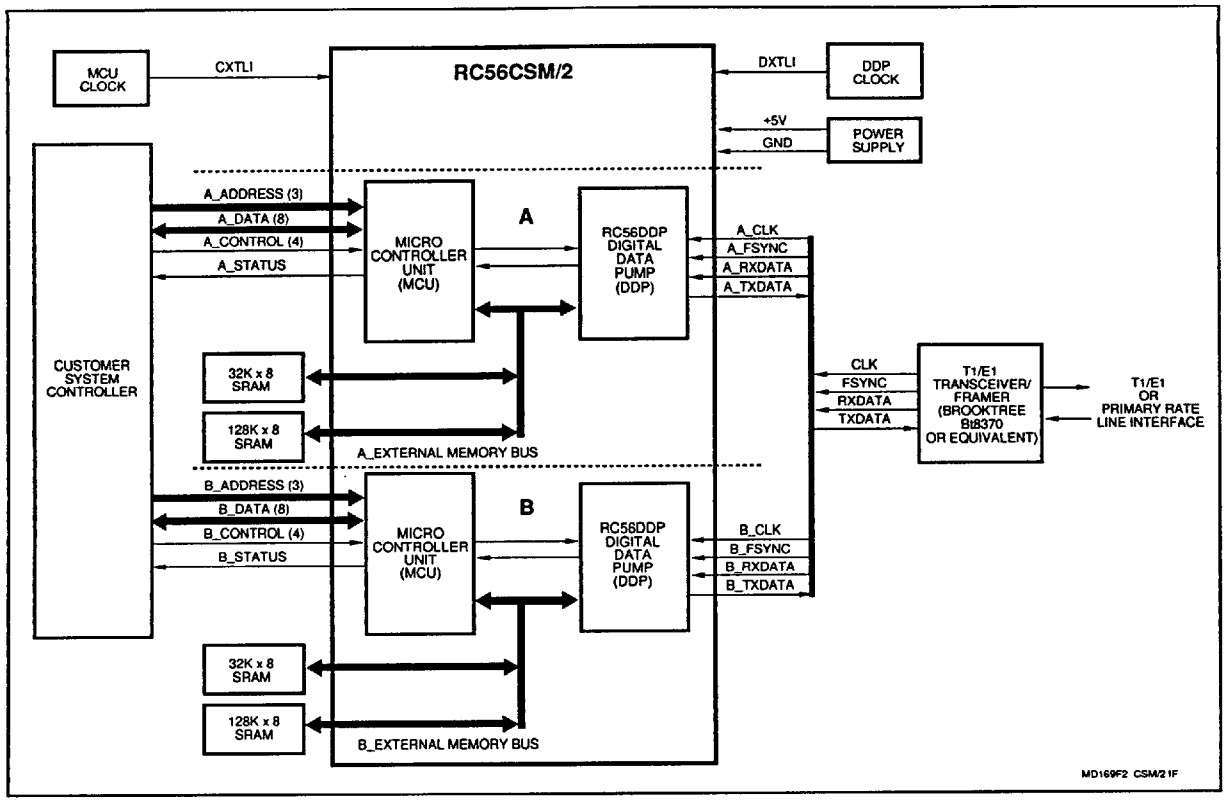


Figure 2. RC56CSM/2 Interface - 268-Pin BGA

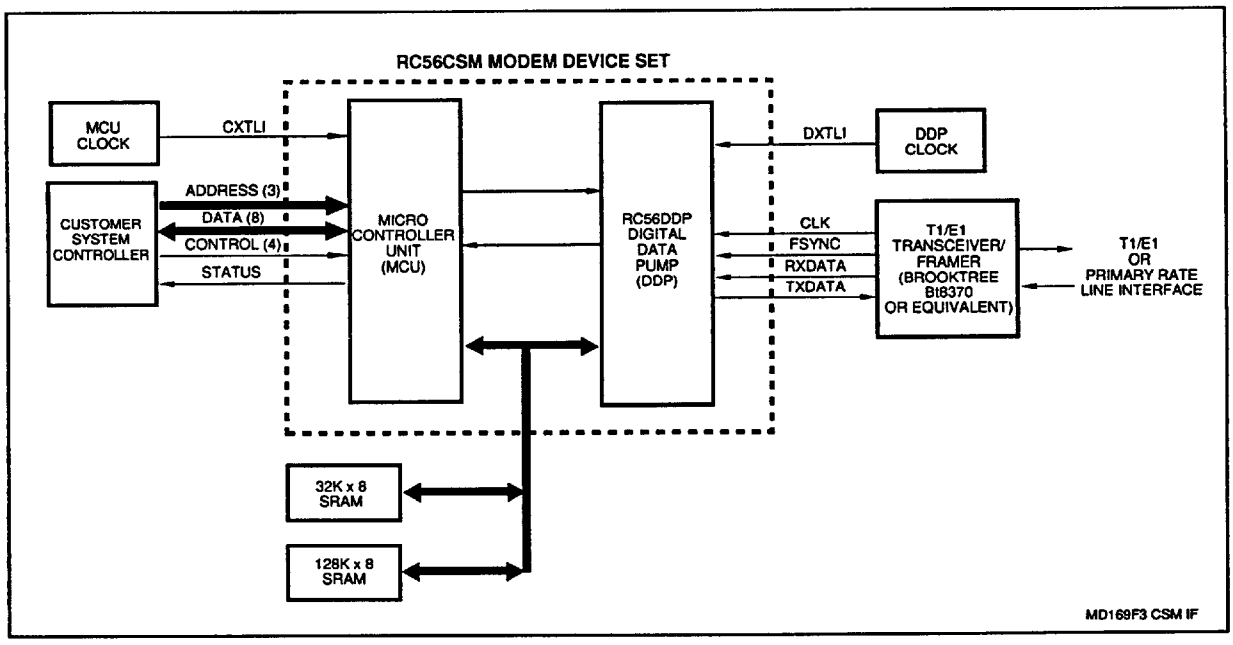


Figure 3. RC56CSM Device Set Interface - One MCU in 80-Pin PQFP and One RC56DDP in 80-Pin PQFP

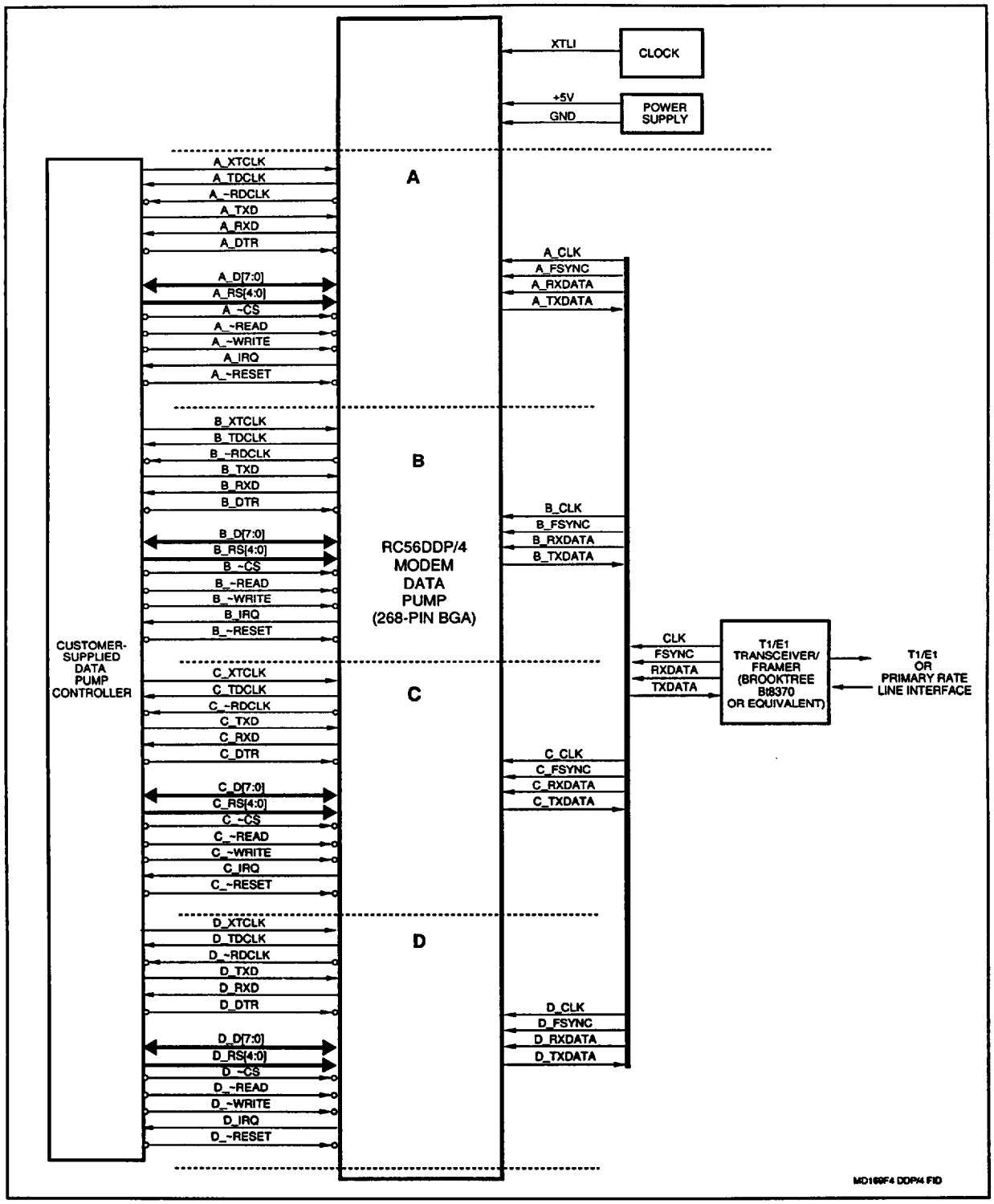


Figure 4. RC56DDP/4 Interface - 268-Pin BGA

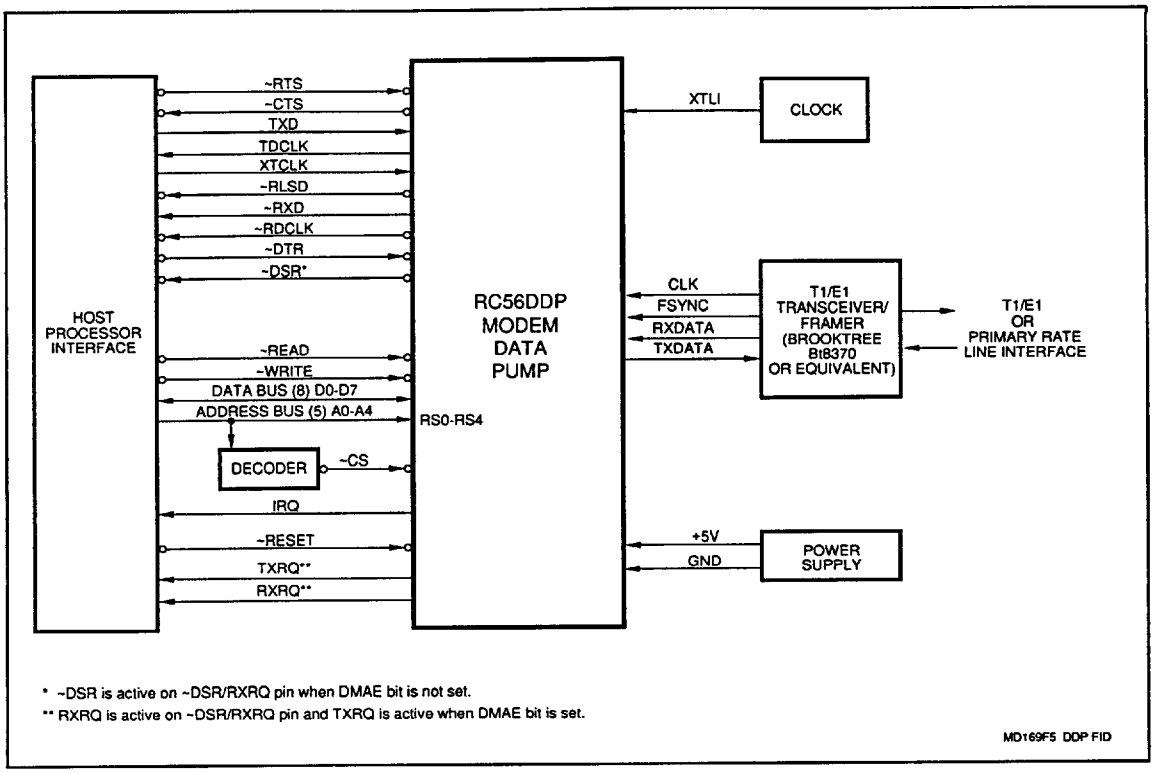


Figure 5. RC56DDP Interface - 80-Pin PQFP

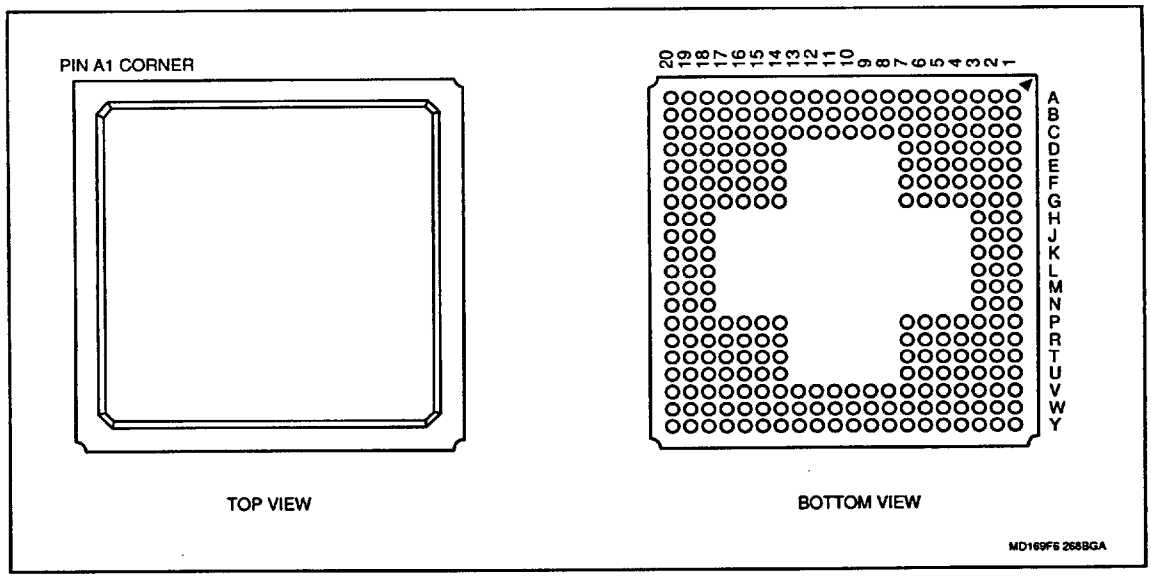


Figure 6. 268-Pin BGA Package for RC56CSM/2 and RC56DDP/4

Table 2. RC56CSM/2 Pin Signals by Pin Location - 268-Pin BGA

Location	Signal	Location	Signal	Location	Signal	Location	Signal	Location	Signal
A1	B_~DRES	C1	B_FSYNC	E1	B_A10	G1	B_A14	J1	GND
A2	GND	C2	B_RXDATA	E2	B_A9	G2	B_A13	J2	B_A16
A3	B_~DWR	C3	B_TMODE	E3	B_IA2CLK	G3	NC	J3	NC
A4	VDD	C4	B_IACLK	E4	GND	G4	GND		
A5	B_D1	C5	B_IASLEEP	E5	GND	G5	GND		
A6	B_D3	C6	B_SR2IO	E6	GND	G6	GND		
A7	B_D5	C7	B_SA2CLK	E7	GND	G7	GND		
A8	B_D7	C8	B_VTXD						
A9	B_A1	C9	NC						
A10	B_A3	C10	B_~DCS						
A11	B_A5	C11	B_PLLCAP						
A12	GND	C12	B_VRXD						
A13	~CTEST	C13	B_SR2CLK						
A14	B_NVMCLK	C14	B_SR3CLK	E14	GND	G14	GND		
A15	B_CRXD	C15	B_SA3CLK	E15	GND	G15	GND		
A16	B_~HRD	C16	B_YCLK	E16	GND	G16	GND		
A17	B_~HCS	C17	B_XCLK	E17	GND	G17	GND		
A18	B_HA2	C18	NC	E18	NC	G18	NC	J18	NC
A19	B_HA0	C19	B_HD4	E19	B_HD0	G19	B_~CRES	J19	B_~RAMSEL
A20	B_HD7	C20	B_HD3	E20	GND	G20	B_~READ	J20	B_HINT
B1	B_TXDATA	D1	B_SCLK	F1	B_A12	H1	VDD	K1	NC
B2	B_SYCLK	D2	B_A8	F2	B_A11	H2	B_A15	K2	B_PLLVDD
B3	B_~DRD	D3	GPTEST	F3	B_SR7OUT	H3	B_DIRQ	K3	NC
B4	B_PLLGND	D4	GND	F4	GND				
B5	B_D0	D5	GND	F5	GND				
B6	B_D2	D6	GND	F6	GND				
B7	B_D4	D7	GND	F7	GND				
B8	B_D6								
B9	B_A0								
B10	B_A2								
B11	B_A4								
B12	B_A6								
B13	B_A7								
B14	B_CTXD	D14	GND	F14	GND				
B15	B_NVMDATA	D15	GND	F15	GND				
B16	B_~HWR	D16	GND	F16	GND				
B17	B_HA3	D17	GND	F17	GND				
B18	B_HA1	D18	NC	F18	NC	H18	NC	K18	NC
B19	B_HD6	D19	B_HD2	F19	VDD	H19	B_NMI	K19	B_~ROMSEL
B20	B_HD5	D20	B_HD1	F20	VDD	H20	B_~WRITE	K20	CXTLI

Table 2. RC56CSM/2 Pin Signals by Pin Location - 268-Pin BGA (Cont'd)

Location	Signal	Location	Signal	Location	Signal	Location	Signal	Location	Signal
L1	VDD	N1	A_~DWR	R1	A_RXDATA	U1	VDD	W1	GND
L2	DXTLI	N2	A_~DRD	R2	A_SCLK	U2	A_D0	W2	A_D3
L3	A_SR7OUT	N3	A_XCLK	R3	NC	U3	A_SR3CLK	W3	A_D6
				R4	GND	U4	GND	W4	A_A7
				R5	GND	U5	GND	W5	A_A9
				R6	GND	U6	GND	W6	A_A11
				R7	GND	U7	GND	W7	A_A13
								W8	A_A15
								W9	A_PLLGND
								W10	A_A6
								W11	A_A4
								W12	A_A2
								W13	A_A0
				R14	GND	U14	GND	W14	A_~HRD
				R15	GND	U15	GND	W15	A_~HCS
				R16	GND	U16	GND	W16	A_HA3
				R17	GND	U17	GND	W17	A_HA1
L18	NC	N18	NC	R18	NC	U18	NC	W18	A_~ROMSEL
L19	A_HD6	N19	A_HD2	R19	A_~READ	U19	A_~CRES	W19	A_CTXD
L20	A_HD7	N20	A_HD3	R20	GND	U20	A_NMI	W20	A_CRXD
M1	GND	P1	A_~DRES	T1	A_FSYNC	V1	A_D1	Y1	A_D4
M2	A_SYCLK	P2	A_TXDATA	T2	~DTEST	V2	A_D2	Y2	A_D5
M3	XYCNT	P3	A_YCLK	T3	A_SA3CLK	V3	A_TMODE	Y3	A_D7
		P4	GND	T4	GND	V4	A_IACLK	Y4	A_A8
		P5	GND	T5	GND	V5	A_IASLEEP	Y5	A_A10
		P6	GND	T6	GND	V6	A_SR2IO	Y6	A_A12
		P7	GND	T7	GND	V7	A_SA2CLK	Y7	A_A14
						V8	A_VTXD	Y8	A_A16
						V9	A_PLLCAP	Y9	VDD
						V10	A_~DCS	Y10	A_A5
						V11	A_DIRQ	Y11	A_A3
						V12	A_VRXD	Y12	A_A1
						V13	A_SR2CLK	Y13	A_NVMDATA
		P14	GND	T14	GND	V14	A_IA2CLK	Y14	A_~HWR
		P15	GND	T15	GND	V15	NC	Y15	GND
		P16	GND	T16	GND	V16	NC	Y16	A_HA2
		P17	GND	T17	GND	V17	NC	Y17	A_HA0
M18	NC	P18	NC	T18	NC	V18	NC	Y18	A_PLLGND
M19	A_HD4	P19	A_HD0	T19	A_~WRITE	V19	A_NVMCLK	Y19	A_~RAMSEL
M20	A_HD5	P20	A_HD1	T20	VDD	V20	NC	Y20	A_HINT

Table 3. RC56CSM/2 Pin Signals by Signal - 268-Pin BGA

Channel Dependent			
Signal	Location	Signal	Location
A_~CRES	U19	B_~CRES	G19
A_~DCS	V10	B_~DCS	C10
A_~DRD	N2	B_~DRD	B3
A_~DRES	P1	B_~DRES	A1
A_~DWR	N1	B_~DWR	A3
A_~HCS	W15	B_~HCS	A17
A_~HRD	W14	B_~HRD	A16
A_~HWR	Y14	B_~HWR	B16
A_~RAMSEL	Y19	B_~RAMSEL	J19
A_~READ	R19	B_~READ	G20
A_~ROMSEL	W18	B_~ROMSEL	K19
A_~WRITE	T19	B_~WRITE	H20
A_A0	W13	B_A0	B9
A_A1	Y12	B_A1	A9
A_A2	W12	B_A2	B10
A_A3	Y11	B_A3	A10
A_A4	W11	B_A4	B11
A_A5	Y10	B_A5	A11
A_A6	W10	B_A6	B12
A_A7	W4	B_A7	B13
A_A8	Y4	B_A8	D2
A_A9	W5	B_A9	E2
A_A10	Y5	B_A10	E1
A_A11	W6	B_A11	F2
A_A12	Y6	B_A12	F1
A_A13	W7	B_A13	G2
A_A14	Y7	B_A14	G1
A_A15	W8	B_A15	H2
A_A16	Y8	B_A16	J2
A_CRXD	W20	B_CRXD	A15
A_CTXD	W19	B_CTXD	B14
A_D0	U2	B_D0	B5
A_D1	V1	B_D1	A5
A_D2	V2	B_D2	B6
A_D3	W2	B_D3	A6
A_D4	Y1	B_D4	B7
A_D5	Y2	B_D5	A7
A_D6	W3	B_D6	B8
A_D7	Y3	B_D7	A8
A_DIRQ	V11	B_DIRQ	H3

Table 3. RC56CSM/2 Pin Signals by Signal - 268-Pin BGA (Cont'd)

Channel Dependent			
A_HA0	Y17	B_HA0	A19
A_HA1	W17	B_HA1	B18
A_HA2	Y16	B_HA2	A18
A_HA3	W16	B_HA3	B17
A_HD0	P19	B_HD0	E19
A_HD1	P20	B_HD1	D20
A_HD2	N19	B_HD2	D19
A_HD3	N20	B_HD3	C20
A_HD4	M19	B_HD4	C19
A_HD5	M20	B_HD5	B20
A_HD6	L19	B_HD6	B19
A_HD7	L20	B_HD7	A20
A_HINT	Y20	B_HINT	J20
A_IA2CLK	V14	B_IA2CLK	E3
A_IACLK	V4	B_IACLK	C4
A_IASLEEP	V5	B_IASLEEP	C5
A_NMI	U20	B_NMI	H19
A_NVMCLK	V19	B_NVMCLK	A14
A_NVMDATA	Y13	B_NVMDATA	B15
A_PLLCAP	V9	B_PLLCAP	C11
A_PLLGND	W9	B_PLLGND	B4
A_PLLGND	Y18	B_PLLVDD	K2
A_RXDATA	R1	B_RXDATA	C2
A_SA2CLK	V7	B_SA2CLK	C7
A_SA3CLK	T3	B_SA3CLK	C15
A_SCLK	R2	B_SCLK	D1
A_SR2CLK	V13	B_SR2CLK	C13
A_SR2IO	V6	B_SR2IO	C6
A_SR3CLK	U3	B_SR3CLK	C14
A_SR7OUT	L3	B_SR7OUT	F3
A_SYCLK	M2	B_SYCLK	B2
A_FSYNC	T1	B_FSYNC	C1
A_TMODE	V3	B_TMODE	C3
A_TXDATA	P2	B_TXDATA	B1
A_VRXD	V12	B_VRXD	C12
A_VTXD	V8	B_VTXD	C8
A_XCLK	N3	B_XCLK	C17
A_YCLK	P3	B_YCLK	C16

Table 3. RC56CSM/2 Pin Signals by Signal - 268-Pin BGA (Cont'd)

Channel Independent	
Signal	**Location**
~CTEST	A13
~DTEST	T2
CXTLI	K20
DXTLI	L2
XYCNT	M3
GPTEST	D3
VDD	A4, F19, F20, H1, L1, T20, U1, Y9
GND	A2, A12, D4, D5, D6, D7, D14, D15, D16, D17, E4, E5, E6, E7, E14, E15, E16, E17, E20, F4, F5, F6, F7, F14, F15, F16, F17, G4, G5, G6, G7, G14, G15, G16, G17, J1, M1, P4, P5, P6, P7, P14, P15, P16, P17, R4, R5, R6, R7, R14, R15, R16, R17, R20, T4, T5, T6, T7, T14, T15, T16, T17, U4, U5, U6, U7, U14, U15, U16, U17, W1, Y15
NC	C9, C18, D18, E18, F18, G3, G18, H18, J3, J18, K1, K3, K18, L18, M18, N18, P18, R3, R18, T18, U18, V15, V16, V17, V18, V20

Table 4. RC56DDP/4 Pin Signals by Pin Location - 268-Pin BGA

Location	Signal	Location	Signal	Location	Signal	Location	Signal	Location	Signal
A1	A_SYCLK	C1	A_TXDATA	E1	A_FSYNC	G1	~TEST	J1	A_RXD
A2	GND	C2	A_D4	E2	A_D2	G2	A_D0	J2	GND
A3	A_TDCLK	C3	A_VTXD	E3	A_SA3CLK	G3	A_SA2CLK	J3	A_SR1IO
A4	VDD	C4	A_VRXD	E4	GND	G4	GND		
A5	A_~RDCLK	C5	A_SR2CLK	E5	GND	G5	GND		
A6	A_~WRITE	C6	NC	E6	GND	G6	GND		
A7	A_RS4	C7	A_SR7OUT	E7	GND	G7	GND		
A8	A_RS2	C8	A_PLLCAP						
A9	A_RS1	C9	A_PLLGND						
A10	B_RS1	C10	A_PLLVDD						
A11	B_RS0	C11	B_PLLCAP						
A12	A_YCLK	C12	B_PLLVDD						
A13	A_XCLK	C13	B_SR7OUT						
A14	GND	C14	B_PLLGND	E14	GND	G14	GND		
A15	B_IRQ	C15	NC	E15	GND	G15	GND		
A16	GND	C16	NC	E16	GND	G16	GND		
A17	B_~DTR	C17	B_IASLEEP	E17	GND	G17	GND		
A18	B_RXD	C18	B_SR1IO	E18	B_SA2CLK	G18	B_SA3CLK	J18	B_VTXD
A19	B_CLK	C19	B_TXDATA	E19	B_~RDCLK	G19	B_~WRITE	J19	B_XCLK
A20	B_FSYNC	C20	VDD	E20	B_TDCLK	G20	B_SYCLK	J20	B_RS3
B1	A_~RESET	D1	A_RXDATA	F1	A_CLK	H1	VDD	K1	A_IRQ
B2	A_TXD	D2	A_D3	F2	A_D1	H2	A_XTCLK	K2	A_~DTR
B3	A_D5	D3	IACLK1	F3	A_SR3CLK	H3	A_SR2IO	K3	A_IASLEEP
B4	A_D6	D4	GND	F4	GND				
B5	A_D7	D5	GND	F5	GND				
B6	A_~READ	D6	GND	F6	GND				
B7	A_~CS	D7	GND	F7	GND				
B8	A_RS3								
B9	A_RS0								
B10	XTLI								
B11	B_D7								
B12	B_D6								
B13	B_D5								
B14	B_D4	D14	GND	F14	GND				
B15	B_D3	D15	GND	F15	GND				
B16	B_D2	D16	GND	F16	GND				
B17	B_D1	D17	GND	F17	GND				
B18	B_D0	D18	B_SR2IO	F18	B_SR3CLK	H18	B_VRXD	K18	B_SA2CLK
B19	B_XTCLK	D19	B_YCLK	F19	B_TXD	H19	B_~CS	K19	B_RS2
B20	B_RXDATA	D20	B_~RESET	F20	B_~READ	H20	B_RS4	K20	VDD

Table 4. RC56DDP/4 Pin Signals by Pin Location - 268-Pin BGA (Cont'd)

Location	Signal	Location	Signal	Location	Signal	Location	Signal	Location	Signal
L1	VDD	N1	C_TDCLK	R1	C_~RESET	U1	C_RXDATA	W1	C_FSYNC
L2	C_SYCLK	N2	C_~READ	R2	C_RS4	U2	C_RS2	W2	C_YCLK
L3	C_SR2CLK	N3	C_VRXD	R3	C_SA3CLK	U3	C_SA2CLK	W3	C_D0
				R4	GND	U4	GND	W4	C_D1
				R5	GND	U5	GND	W5	C_D2
				R6	GND	U6	GND	W6	C_D3
				R7	GND	U7	GND	W7	C_D4
								W8	C_D5
								W9	C_D6
								W10	C_D7
								W11	D_YCLK
								W12	D_RS0
								W13	D_RS1
				R14	GND	U14	GND	W14	GND
				R15	GND	U15	GND	W15	D_~WRITE
				R16	GND	U16	GND	W16	D_D7
				R17	GND	U17	GND	W17	D_D6
L18	NC	N18	D_SR1IO	R18	D_SA2CLK	U18	D_SA3CLK	W18	D_D5
L19	D_~DTR	N19	D_XTCLK	R19	D_D1	U19	D_D3	W19	D_~RESET
L20	D_RXD	N20	VDD	R20	D_CLK	U20	D_RXDATA	W20	D_XCLK
M1	C_XCLK	P1	C_~WRITE	T1	C_TXDATA	V1	VDD	Y1	C_CLK
M2	C_TXD	P2	C_~CS	T2	C_RS3	V2	XYCNT	Y2	C_XTCLK
M3	C_VTXD	P3	IACLK2	T3	C_SR3CLK	V3	C_SR1IO	Y3	C_RXD
		P4	GND	T4	GND	V4	C_SR2IO	Y4	C_~DTR
		P5	GND	T5	GND	V5	C_IASLEEP	Y5	GND
		P6	GND	T6	GND	V6	NC	Y6	C_IRQ
		P7	GND	T7	GND	V7	C_PLLGND	Y7	GND
						V8	C_SR7OUT	Y8	C_~RDCLK
						V9	C_PLLCAP	Y9	C_RS0
						V10	C_PLLVDD	Y10	C_RS1
						V11	D_PLLVDD	Y11	D_RS2
						V12	D_PLLCAP	Y12	D_RS3
						V13	D_PLLGND	Y13	D_RS4
		P14	GND	T14	GND	V14	D_SR7OUT	Y14	D_~CS
		P15	GND	T15	GND	V15	NC	Y15	D_~READ
		P16	GND	T16	GND	V16	D_SR2CLK	Y16	D_~RDCLK
		P17	GND	T17	GND	V17	D_VTXD	Y17	D_TDCLK
M18	D_IASLEEP	P18	D_SR2IO	T18	D_SR3CLK	V18	D_VRXD	Y18	VDD
M19	D_IRQ	P19	D_D0	T19	D_D2	V19	D_D4	Y19	D_TXD
M20	GND	P20	GPTEST	T20	D_FSYNC	V20	D_TXDATA	Y20	D_SYCLK

Table 5. RC56DDP/4 Pin Signals by Signal - 268-Pin BGA

Channel Dependent							
Signal	Location	Signal	Location	Signal	Location	Signal	Location
A_~CS	B7	B_~CS	H19	C_~CS	P2	D_~CS	Y14
A_~DTR	K2	B_~DTR	A17	C_~DTR	Y4	D_~DTR	L19
A_~RDCLK	A5	B_~RDCLK	E19	C_~RDCLK	Y8	D_~RDCLK	Y16
A_~READ	B6	B_~READ	F20	C_~READ	N2	D_~READ	Y15
A_~RESET	B1	B_~RESET	D20	C_~RESET	R1	D_~RESET	W19
A_~WRITE	A6	B_~WRITE	G19	C_~WRITE	P1	D_~WRITE	W15
A_CLK	F1	B_CLK	A19	C_CLK	Y1	D_CLK	R20
A_D0	G2	B_D0	B18	C_D0	W3	D_D0	P19
A_D1	F2	B_D1	B17	C_D1	W4	D_D1	R19
A_D2	E2	B_D2	B16	C_D2	W5	D_D2	T19
A_D3	D2	B_D3	B15	C_D3	W6	D_D3	U19
A_D4	C2	B_D4	B14	C_D4	W7	D_D4	V19
A_D5	B3	B_D5	B13	C_D5	W8	D_D5	W18
A_D6	B4	B_D6	B12	C_D6	W9	D_D6	W17
A_D7	B5	B_D7	B11	C_D7	W10	D_D7	W16
A_IASLEEP	K3	B_IASLEEP	C17	C_IASLEEP	V5	D_IASLEEP	M18
A_IRQ	K1	B_IRQ	A15	C_IRQ	Y6	D_IRQ	M19
A_PLLCAP	C8	B_PLLCAP	C11	C_PLLCAP	V9	D_PLLCAP	V12
A_PLLGND	C9	B_PLLGND	C14	C_PLLGND	V7	D_PLLGND	V13
A_PLLVDD	C10	B_PLLVDD	C12	C_PLLVDD	V10	D_PLLVDD	V11
A_RS0	B9	B_RS0	A11	C_RS0	Y9	D_RS0	W12
A_RS1	A9	B_RS1	A10	C_RS1	Y10	D_RS1	W13
A_RS2	A8	B_RS2	K19	C_RS2	U2	D_RS2	Y11
A_RS3	B8	B_RS3	J20	C_RS3	T2	D_RS3	Y12
A_RS4	A7	B_RS4	H20	C_RS4	R2	D_RS4	Y13
A_RXD	J1	B_RXD	A18	C_RXD	Y3	D_RXD	L20
A_RXDATA	D1	B_RXDATA	B20	C_RXDATA	U1	D_RXDATA	U20
A_SA2CLK	G3	B_SA2CLK	E18	C_SA2CLK	U3	D_SA2CLK	R18
A_SA3CLK	E3	B_SA2CLK	K18	C_SA3CLK	R3	D_SA3CLK	U18
A_SR1IO	J3	B_SA3CLK	G18	C_SR1IO	V3	D_SR1IO	N18
A_SR2CLK	C5	B_SR1IO	C18	C_SR2CLK	L3	D_SR2CLK	V16
A_SR2IO	H3	B_SR2IO	D18	C_SR2IO	V4	D_SR2IO	P18
A_SR3CLK	F3	B_SR3CLK	F18	C_SR3CLK	T3	D_SR3CLK	T18
A_SR7OUT	C7	B_SR7OUT	C13	C_SR7OUT	V8	D_SR7OUT	V14
A_FSYNC	E1	B_FSYNC	A20	C_FSYNC	W1	D_FSYNC	T20
A_SYCLK	A1	B_SYCLK	G20	C_SYCLK	L2	D_SYCLK	Y20
A_TDCLK	A3	B_TDCLK	E20	C_TDCLK	N1	D_TDCLK	Y17
A_TXD	B2	B_TXD	F19	C_TXD	M2	D_TXD	Y19
A_TXDATA	C1	B_TXDATA	C19	C_TXDATA	T1	D_TXDATA	V20
A_VRXD	C4	B_VRXD	H18	C_VRXD	N3	D_VRXD	V18
A_VTXD	C3	B_VTXD	J18	C_VTXD	M3	D_VTXD	V17
A_XCLK	A13	B_XCLK	J19	C_XCLK	M1	D_XCLK	W20
A_XTCLK	H2	B_XTCLK	B19	C_XTCLK	Y2	D_XTCLK	N19
A_YCLK	A12	B_YCLK	D19	C_YCLK	W2	D_YCLK	W11

Table 5. RC56DDP/4 Pin Signals by Signal - 268-Pin BGA (Cont'd)

Channel Independent	
Signal	**Location**
~TEST	G1
GPTEST	P20
IACLK1	D3
IACLK2	P3
XTLI	B10
XYCNT	V2
VCC	A4, B10, C20, H1, K20, L1, N20, V1, V2, Y18
GND	A2, A14, A16, D4, D5, D6, D7, D14, D15, D16, D17, E4, E5, E6, E7, E14, E15, E16, E17, F4, F5, F6, F7, F14, F15, F16, F17, G4, G5, G6, G7, G14, G15, G16, G17, J2, M20, P4, P5, P6, P7, P14, P15, P16, P17, R4, R5, R6, R7, R14, R15, R16, R17, T4, T5, T6, T7, T14, T15, T16, T17, U4, U5, U6, U7, U14, U15, U16, U17, W14, Y5, Y7
NC	C6, C15, C16, L18, V6, V15

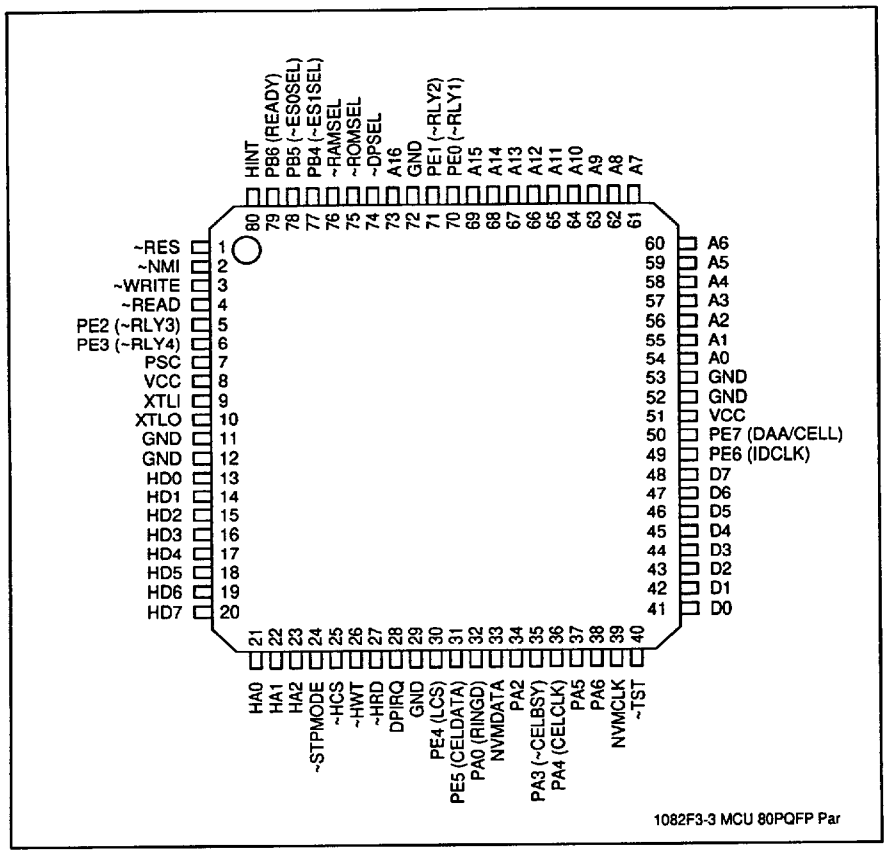


Figure 7. MCU Pin Signals - 80-Pin PQFP

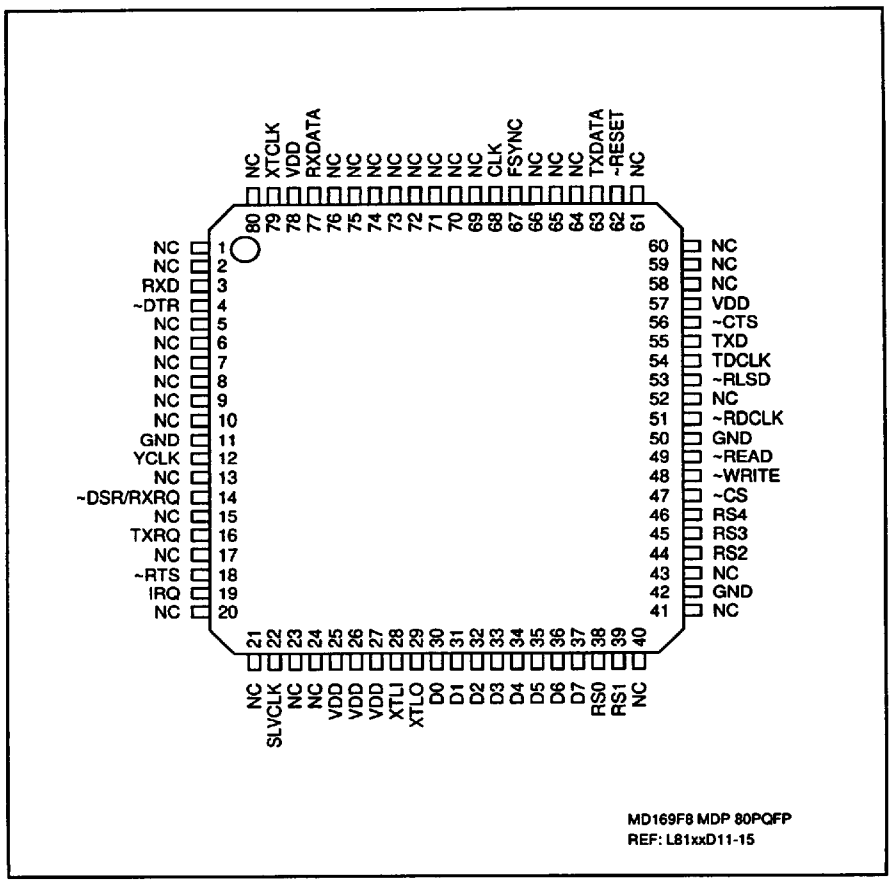


Figure 8. RC56DDP Pin Signals - 80-Pin PQFP

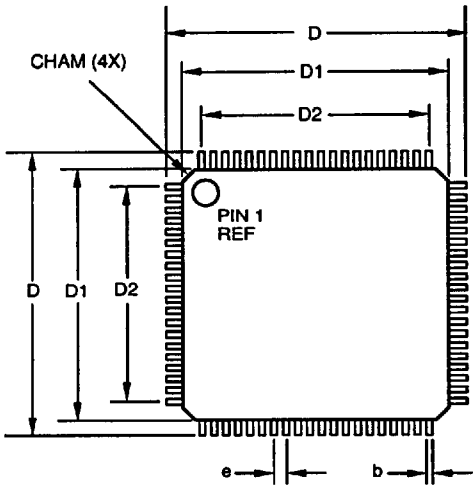
Table 6. Current and Power Requirements

Mode	Current (ID)		Power (PD)		Notes
	Typical Current (mA)	Maximum Current (mA)	Typical Power (mW)	Maximum Power (mW)	
MCU					f_{IN} = 28.224 MHz
Normal mode	40	45	200	235	
Sleep mode	2		10		
RC56DDP					f_{IN} = 56.448 MHz
Normal mode	125	135	625	710	
Sleep mode	2		10		
RC56CSM					
Normal mode	165	180	825	945	
Sleep mode	4		20		
RC56CSM/2					f_{IN} = 56.448 MHz
Normal mode	330	370	1650	1940	
Sleep mode	6		30		
RC56DDP/4					f_{IN} = 56.448 MHz
Normal mode	500	550	2500	2890	
Sleep mode	8		40		

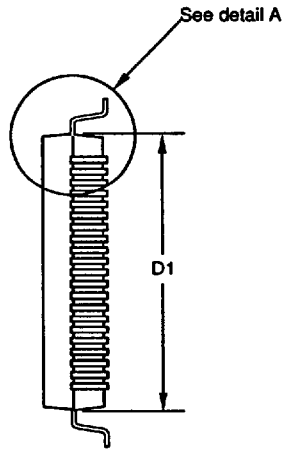
Notes:
Test conditions: VCC = 5.0 VDC for typical values; VCC = 5.25 VDC for maximum values.

Table 7. Absolute Maximum Ratings

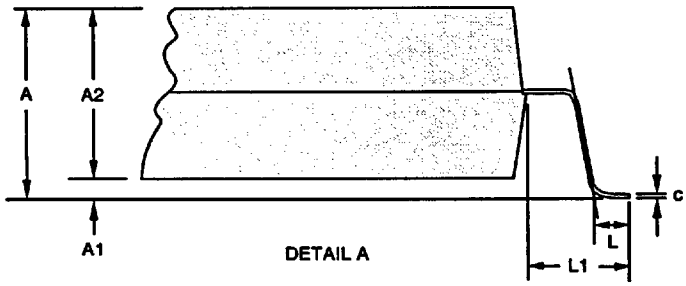
Parameter	Symbol	Limits	Units
Supply Voltage	V_{DD}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-0.5 to (+5VD +0.5)	V
Operating Temperature Range	T_A	-0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Analog Inputs	V_{IN}	-0.3 to (+5VA + 0.3)	V
Voltage Applied to Outputs in High Impedance (Off) State	V_{HZ}	-0.5 to (+5VD + 0.5)	V
DC Input Clamp Current	I_{IK}	±20	mA
DC Output Clamp Current	I_{OK}	±20	mA
Static Discharge Voltage (25°C)	V_{ESD}	±2500	V
Latch-up Current (25°C)	I_{TRIG}	±200	mA



TOP VIEW



SIDE VIEW

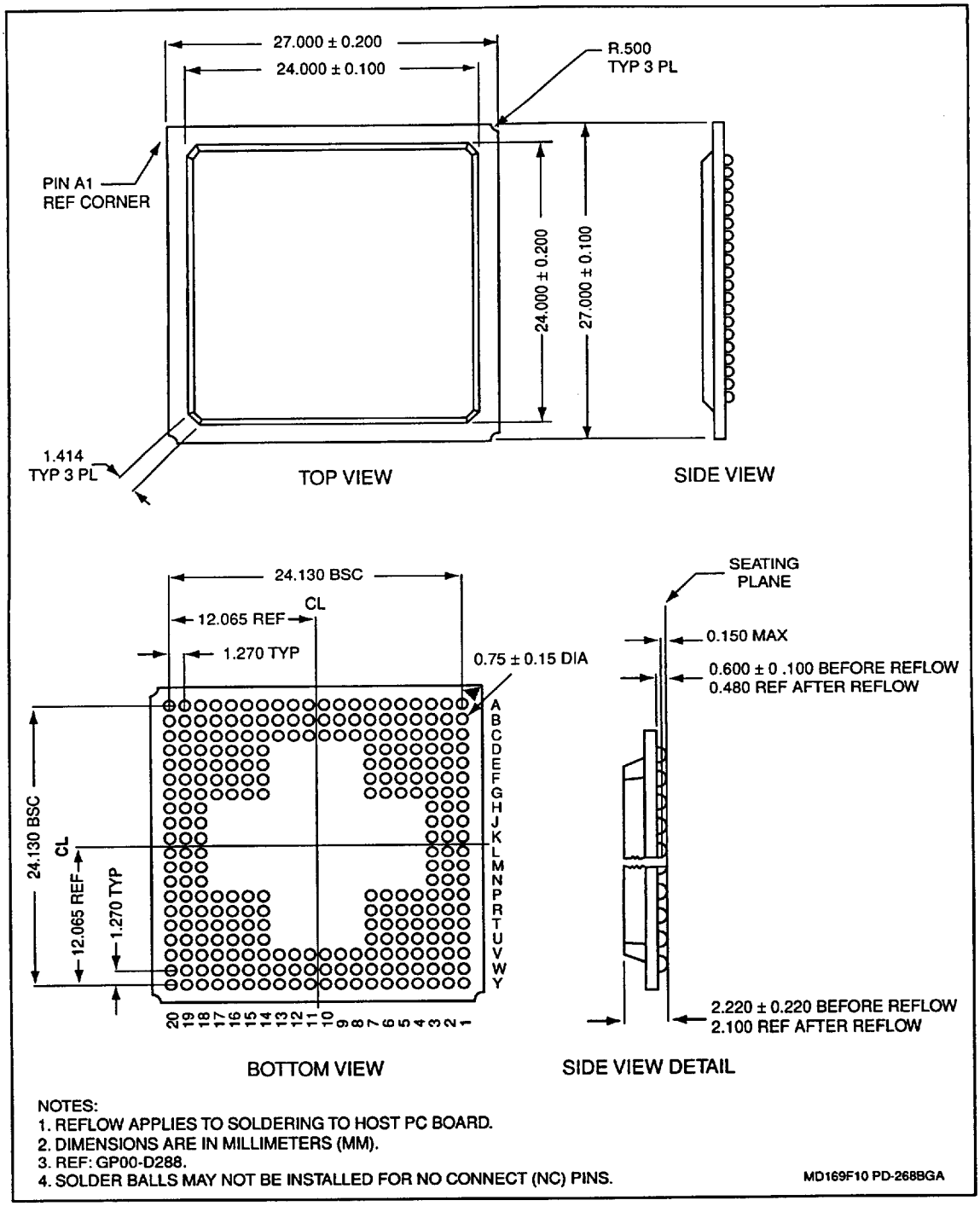


Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A		2.4 MAX		0.0945 MAX
A1	0.05	0.35	0.0020	0.0138
A2		2.0 REF		0.0787 REF
D	16.95	17.45	0.6673	0.6870
D1		14.0 REF		0.5512 REF
D2		12.35 REF		0.4862 REF
L	0.73	1.03	0.0287	0.0406
L1		1.6 REF		0.0630 REF
e		0.65 BSC		0.0256 BSC
b	0.25	0.45	0.0098	0.0177
c	0.13	0.19	0.0051	0.0075
Coplanarity		0.1 MAX		0.004 MAX
Ref: 80-PIN PQFP (GP00-D227)				

* Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may include round-off errors.

PD-PQFP-80 (040695)

Package Dimensions - 80-Pin PQFP



Package Dimensions - 268-Pin BGA

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