

# RC6303

## Triple Video Amplifier with Separate Enable Inputs

### Features

- Triple video amplifier
- Independently enabled amplifiers
- 90 MHz -3 dB Bandwidth ( $A_V = 2$ )
- 20 MHz  $\pm 0.1$  dB gain flatness
- Stable at  $A_V \geq 2$
- 0.06% differential gain ( $A_V = 2$ ,  $R_L = 150\Omega$ )
- 0.06° differential phase ( $A_V = 2$ ,  $R_L = 150\Omega$ )
- High CMRR (100dB), High PSRR (80 dB)
- Dual  $\pm 5V$  power supply
- Low offset 1.0 mV
- 16-pin narrow SO package
- 300 V/ $\mu$ s slew rate
- Fast settling time: 0.1% in 35 ns
- TTL or CMOS compatible enable inputs

### Applications

- RGB amplifier
- 3:1 crosspoint switch
- RGB switch
- Video instrumentation amplifier
- Selectable gain amplifier
- Active filter

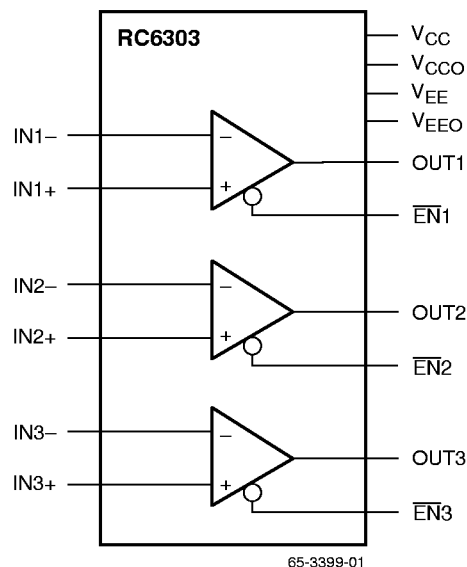
### Description

The RC6303 consists of three low power, wide band voltage feedback operational amplifiers. Each channel is capable of delivering a load current of at least 35mA. Each amplifier can be independently enabled or disabled with a TTL or CMOS signal. When disabled, the amplifier is in a high impedance output state, presenting a very high input to output isolation.

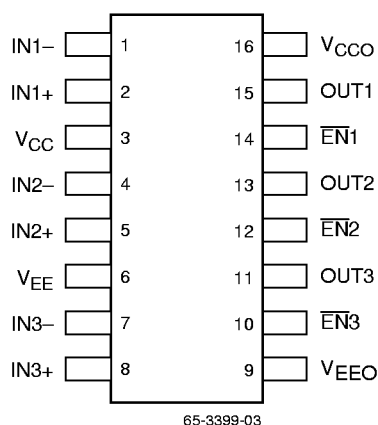
The amplifiers are optimized for video applications with gain  $\geq 2$  where low differential gain and low phase distortion are significant requirements.

The layout is optimized for minimal crosstalk between amplifiers.

### Block Diagram



## Pin Assignments



## Pin Definitions

| Pin Name | Pin Number | Pin Function Description          |
|----------|------------|-----------------------------------|
| EN1      | 14         | Enables amplifier 1 when low      |
| EN2      | 12         | Enables amplifier 2 when low      |
| EN3      | 10         | Enables amplifier 3 when low      |
| IN1-     | 1          | Amplifier 1 inverting input       |
| IN1+     | 2          | Amplifier 1 non-inverting input   |
| IN2-     | 4          | Amplifier 2 inverting input       |
| IN2+     | 5          | Amplifier 2 non-inverting input   |
| IN3-     | 7          | Amplifier 3 inverting input       |
| IN3+     | 8          | Amplifier 3 non-inverting input   |
| OUT1     | 15         | Amplifier 1 output                |
| OUT2     | 13         | Amplifier 2 output                |
| OUT3     | 11         | Amplifier 3 output                |
| VCC      | 3          | Analog positive supply            |
| VCCO     | 16         | Positive supply for output stages |
| VEE      | 6          | Analog negative supply            |
| VEEO     | 9          | Negative supply for output stages |

## Absolute Maximum Ratings

(beyond which the device may be damaged)<sup>1</sup>

| Parameter                                                                  | Min | Typ | Max  | Units |
|----------------------------------------------------------------------------|-----|-----|------|-------|
| Positive power supply, VCC                                                 |     |     | 7    | V     |
| Negative power supply, VEE                                                 |     |     | -7   | V     |
| Differential input voltage                                                 |     |     | 10   | V     |
| Operating Temperature                                                      | 0   |     | +70  | °C    |
| Storage Temperature                                                        | -40 |     | +125 | °C    |
| Junction Temperature                                                       |     |     | 150  | °C    |
| Lead Soldering Temperature (10 seconds)                                    |     |     | 300  | °C    |
| Short circuit tolerance: No more than one output can be shorted to ground. |     |     |      |       |

### Note:

- Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

## Operating Conditions

| Parameter |                         | Min   | Typ  | Max   | Units |
|-----------|-------------------------|-------|------|-------|-------|
| VCC       | Power Supply Voltage    | 4.75  | 5.0  | 5.25  | V     |
| VEE       | Negative Supply Voltage | -4.75 | -5.0 | -5.25 | V     |
| θJA       | SO16 thermal resistance |       | 105  |       | °C/W  |

## DC Characteristics

$V_{CC} = 5V$ ,  $V_{EE} = -5V$ ,  $A_V = 2$ ,  $R_{LOAD} = 150\Omega$ ,  $T_A = 0^\circ C$  to  $70^\circ C$ , unless otherwise specified. Open Loop.

| Parameter            |                                                | Conditions                     | Min  | Typ  | Max | Units |
|----------------------|------------------------------------------------|--------------------------------|------|------|-----|-------|
| V <sub>OS</sub>      | Input Offset Voltage                           | No Load                        |      | 1.0  | ±5  | mV    |
| ΔV <sub>OS</sub> /ΔT | Offset Voltage Drift <sup>1</sup>              |                                |      | 6.0  | ±50 | μV/°C |
| I <sub>B</sub>       | Input Bias Current                             |                                |      | ±1.0 | ±5  | μA    |
| ΔI <sub>B</sub> /ΔT  | Input Bias Current Drift <sup>1</sup>          |                                |      | ±8.0 | ±50 | nA/°C |
| R <sub>in</sub>      | Input Resistance <sup>1</sup>                  |                                | 1    |      |     | MΩ    |
| C <sub>in</sub>      | Input Capacitance <sup>1</sup>                 |                                |      | 0.5  | 2   | pF    |
| CMIR                 | Common Mode Input Range                        |                                | ±2.5 |      |     | V     |
| CMRR                 | Common Mode Rejection Ratio                    | No Load                        | 70   | 100  |     | dB    |
| PSRR                 | Power Supply Rejection Ratio                   | No Load                        | 60   | 80   |     | dB    |
| I <sub>s</sub>       | Quiescent Supply Current                       | No Load, Whole IC              |      | 25   | 33  | mA    |
| I <sub>sd</sub>      | Supply Current Disabled                        |                                |      | 3    | 4   | mA    |
| R <sub>OUT</sub>     | Output Impedance<br>(Closed Loop) <sup>1</sup> | Enabled, At DC                 |      | 0.2  |     | Ω     |
|                      |                                                | Disabled, V <sub>O</sub> = ±2V | 10   | 200  |     | kΩ    |
| C <sub>OUT</sub>     | Output Capacitance <sup>1</sup>                | Disabled                       |      | 0.5  | 2   | pF    |
| I <sub>OUT</sub>     | Output Current                                 |                                | 35   |      |     | mA    |
| V <sub>OUT</sub>     | Output Voltage Swing                           | No Load                        | ±2.5 | ±3.0 |     | V     |
|                      |                                                | R <sub>L</sub> = 150Ω          | ±2.5 | ±3.0 |     | V     |
| A <sub>VOL</sub>     | Open-loop Gain                                 |                                | 58   | 68   |     | dB    |
| V <sub>enh</sub>     | Enable High Voltage                            |                                | 2.4  |      |     | V     |
| V <sub>enl</sub>     | Enable Low Voltage                             |                                |      |      | 0.8 | V     |
| I <sub>en</sub>      | Enable Input Current                           |                                |      | 3    | 10  | μA    |
| t <sub>off</sub>     | Disable Time <sup>1</sup>                      |                                |      | 200  |     | ns    |
| t <sub>on</sub>      | Enable Time <sup>1</sup>                       | Settling to 1%                 |      | 160  |     | ns    |
| I <sub>so</sub>      | Off Isolation (Input to Output) <sup>1</sup>   | @ 5 MHz                        |      | 60   |     | dB    |

**Note:**

1. Guaranteed by design.

## AC Characteristics

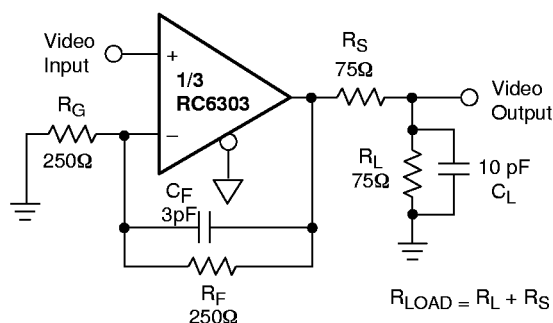
$V_{CC} = 5V$ ,  $V_{EE} = -5V$ ,  $A_V = 2$ ,  $T_A = 0$  to  $70^\circ C$ ,  $R_{LOAD} = 150\Omega$ ,  $R_G = R_F = 250\Omega$ ,  $C_L = 10$  pF,  $C_F = 3$  pF unless otherwise specified. Closed Loop. See Typical Test Circuit.

| Parameter              |                                              | Conditions                                      | Min | Typ  | Max | Units                  |
|------------------------|----------------------------------------------|-------------------------------------------------|-----|------|-----|------------------------|
| Frequency Response     |                                              |                                                 |     |      |     |                        |
| BW                     | -3 dB Bandwidth ( $A_V = 2$ ) <sup>1</sup>   | $V_{OUT} = 0.4\text{ V}_{pp}$                   |     | 90   |     | MHz                    |
|                        |                                              | $V_{OUT} = 0.8\text{ V}_{pp}$                   | 70  | 85   |     | MHz                    |
| Flat                   | $\pm 0.1\text{ dB}$ Bandwidth <sup>1</sup>   |                                                 | 15  | 20   |     | MHz                    |
| Peak                   | Maximum Small Signal AC Peaking <sup>1</sup> |                                                 |     | 0.3  |     | dB                     |
| XTALK                  | Crosstalk Isolation <sup>1</sup>             | @ 5 MHz                                         |     | 60   |     | dB                     |
| Time Domain Response   |                                              |                                                 |     |      |     |                        |
| $t_{r1}$ , $t_{f1}$    | Rise and Fall Time 10% to 90% <sup>1</sup>   | 2V Output Step                                  |     | 6    | 8   | ns                     |
| $t_s$                  | Settling Time to 0.1 % <sup>1</sup>          | 2V Output Step                                  |     | 35   |     | ns                     |
| OS                     | Overshoot <sup>1</sup>                       | 2V Output Step                                  |     | 13   |     | %                      |
| US                     | Undershoot <sup>1</sup>                      | 2V Output Step                                  |     | 4    |     | %                      |
| SR                     | Slew Rate <sup>1</sup>                       | $V_{OUT} = \pm 2.0\text{V}$                     | 200 | 300  |     | V/ $\mu\text{s}$       |
| Distortion             |                                              |                                                 |     |      |     |                        |
| HD <sub>2</sub>        | 2nd Harmonic Dist. @ 20 MHz <sup>1</sup>     | $V_{OUT} = 0.8\text{ V}_{pp}$                   |     | -50  |     | dB                     |
| HD <sub>3</sub>        | 3rd Harmonic Dist. @ 20 MHz <sup>1</sup>     | $V_{OUT} = 0.8\text{ V}_{pp}$                   |     | -50  |     | dB                     |
| Equivalent Input Noise |                                              |                                                 |     |      |     |                        |
| NF                     | Noise Floor > 100 KHz <sup>1</sup>           |                                                 |     | -140 |     | dBm                    |
| SND                    | Spectral Noise Density <sup>1</sup>          | 100 kHz to 200 MHz                              |     | 10   |     | nV/ $\sqrt{\text{Hz}}$ |
| Video Performance      |                                              |                                                 |     |      |     |                        |
| DG                     | Diff. Gain (p-p), NTSC & PAL <sup>1</sup>    | $R_L = 150\Omega$ , $V_{OUT} = \pm 1.5\text{V}$ |     | 0.06 |     | %                      |
| DP                     | Diff. Phase (p-p), NTSC & PAL <sup>1</sup>   | $R_L = 150\Omega$ , $V_{OUT} = \pm 1.5\text{V}$ |     | 0.06 |     | Deg.                   |

**Note:**

1. Guaranteed by design.

## Test Circuit



65-3399-02

## Applications Discussion

Each of the three sections of the RC6303 is provided with an Enable input, thus the part is useful for selecting and multiplexing. A three-channel video multiplexer can be built with just one RC6303 and a decoder, as shown in Figure 1.

Note that RC6303 enable time is shorter than its disable time, hence a make-before-break action is provided, minimizing switching transients on the signal output.

An RGB switch is shown in Figure 2.

### Capacitive Load

The RC6303 can drive a capacitive load from 10 to over 100 pF. In back terminated video applications, bandwidth will only be limited by the RC time constants of the external output components. A minimum 10 pF capacitive load is required. When driving a 75 $\Omega$  cable, place the 75 $\Omega$  source termination resistor as close to the amplifier output as possible.

### Enable/Disable

The enable pins (10, 12, 14), when pulled to a TTL or CMOS logic low or when tied to ground, activate each amplifier individually. When pulled to a TTL or CMOS logic high, the amplifier is tri-stated and presents a high impedance at its output. When disabled the amplifier's power consumption drops, and the non-inverting input signal is isolated from its respective output.

### DC Accuracy

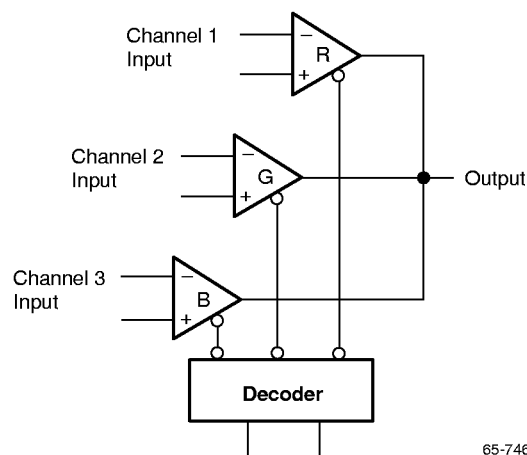
Since the RC6303 is a voltage-feedback amplifier, the inverting and non-inverting inputs have similar impedances and bias currents. To minimize offset voltage, match the source resistances seen by inverting and non-inverting inputs.

### Feedback Components

Because the RC6303 is a voltage-feedback amplifier, it facilitates using reactive (capacitive and inductive) feedback components for implementing filters, integrators, sample/hold circuits, etc. The feedback network and the parasitic capacitance at the inverting (summing junction) input create a pole and affect the transfer function of the circuit. For stable operation, minimize the parasitic capacitance and equivalent resistance of the components used in the feedback circuit.

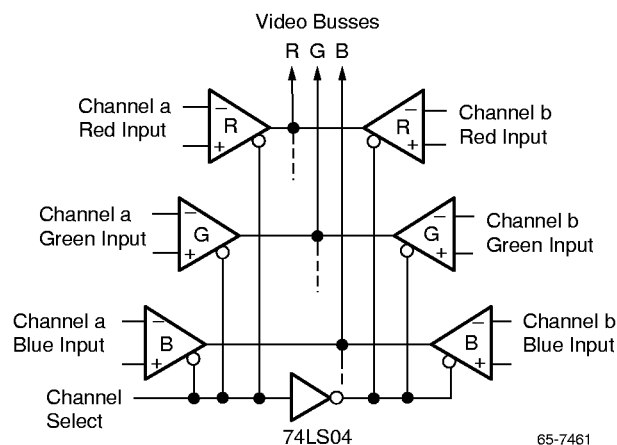
## Circuit Board

High-frequency applications require good grounding, power supply decoupling, low parasitic capacitance and inductance, and good isolation between the inputs to minimize their crosstalk. Avoid coupling from output to input to prevent positive feedback.



65-7460

Figure 1.



65-7461

Figure 2.

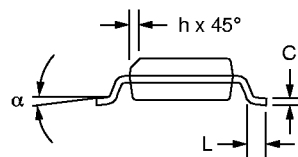
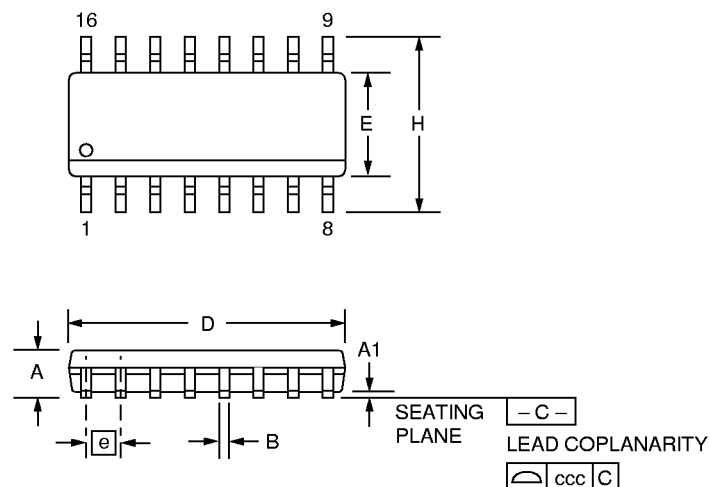
**Notes:**

## Mechanical Dimensions – 16-Lead SOIC Package

| Symbol   | Inches   |      | Millimeters |       | Notes |
|----------|----------|------|-------------|-------|-------|
|          | Min.     | Max. | Min.        | Max.  |       |
| A        | .053     | .069 | 1.35        | 1.75  |       |
| A1       | .004     | .010 | 0.10        | 0.25  |       |
| B        | .013     | .020 | 0.33        | 0.51  |       |
| C        | .008     | .010 | 0.19        | 0.25  | 5     |
| D        | .386     | .394 | 9.80        | 10.00 | 2     |
| E        | .150     | .158 | 3.81        | 4.00  | 2     |
| e        | .050 BSC |      | 1.27 BSC    |       |       |
| H        | .228     | .244 | 5.80        | 6.20  |       |
| h        | .010     | .020 | 0.25        | 0.50  |       |
| L        | .016     | .050 | 0.40        | 1.27  | 3     |
| N        | 16       |      | 16          |       | 6     |
| $\alpha$ | 0°       | 8°   | 0°          | 8°    |       |
| ccc      | —        | .004 | —           | 0.10  |       |

### Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.



## Ordering Information

| Product Number | Temperature Range | Screening  | Package            | Package Marking |
|----------------|-------------------|------------|--------------------|-----------------|
| RC6303M        | 0° to 70°C        | Commercial | 16 Pin Narrow SOIC | RC6303M         |

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