

RC6505

Differential IF Front-End

Features

- Integrated Analog IF Front-End
- Fully differential I/O
- IF flat bandwidth from 25 MHz to 55 MHz
- 48dB minimum gain at IF frequency
- Simple interface to SAW filter
- 9dB input noise figure
- Direct interface to A/D converter
- XTAL oscillator operating to 80MHz
- More than 50dB IMD3
- Industry standard 24-lead SOIC package

Applications

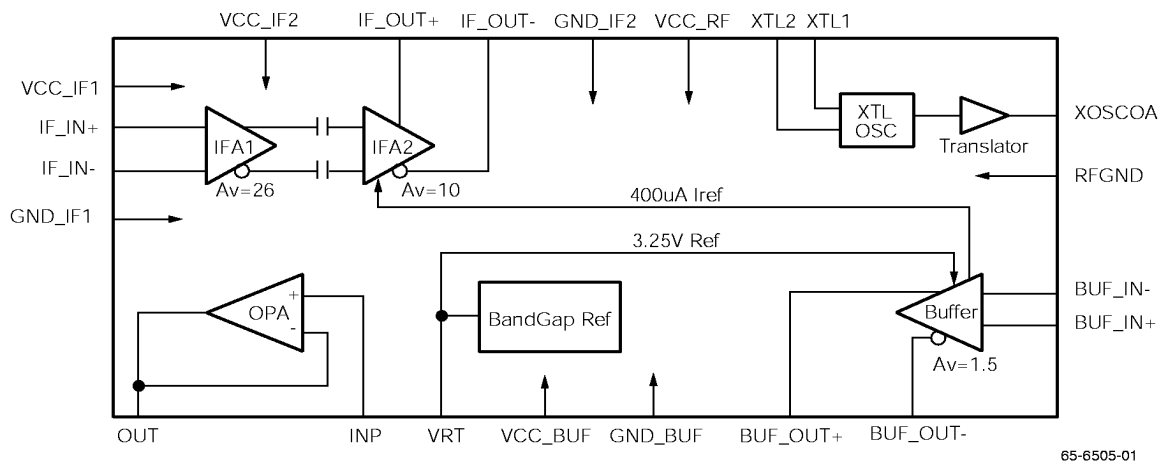
- IF sampling decoders
- QAM Receivers (up to 256 Constellations)
- Set-top receivers for digital cable
- Internet surf boards
- Cable modems
- Desktop video Conferencing

Description

The RC6505 incorporates IF gain stages, reference generators and a crystal oscillator on a single chip. The high input impedance enables direct interface to a SAW filter, while maintaining a low noise figure. The IF output can be further filtered externally and fed to the on-chip fully differential buffer/driver. This buffer is extremely useful when driving low impedance terminations like a differential input to an A/D. The RC6505 is specially suited in IF sampling applications for minimizing the parts count and thus achieving smaller board sizes and lower system costs.

The IF section works on a 12V supply voltage. The oscillator section runs on 5V supply. The RC6505 is available in a 24 Lead SOIC package.

Block Diagram



65-6505-01

Rev. 0.9.1

PRELIMINARY INFORMATION describes products that are not in full production at the time of printing. Specifications are based on design goals and limited characterization. They may change without notice. Contact Fairchild Semiconductor for current information.

Preliminary Information

Functional Description

The RC6505 as shown in the block diagram performs several analog signal processing typically required in modern wide-band digital receivers. These include:

- IF Sections
- Bias Voltage Generation
- Crystal Oscillator

IF Gain Section

The front end IF section provides greater than 48dB of stable gain at IF frequencies.

The input has high impedance while maintaining a low noise figure. The input and output sections are on different supplies to minimize parasitic couplings and prevent oscillations. The differential signal fed at IF_IN + /IF_IN- is available at IF_OUT+ /IF_OUT- after amplification.

This output can be filtered externally and fed back into the IC at pins BUF_IN+ & BUF_IN- to enhance the drive capability of the output and also to reduce any 'kick-back' from the A/D sampling.

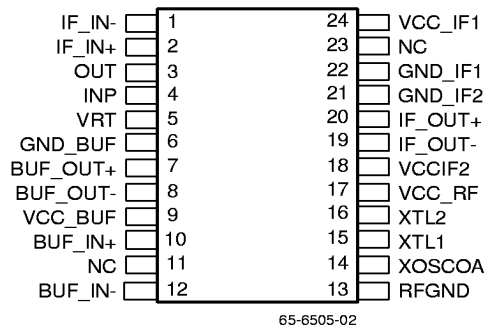
Bias Reference Voltage

The RC6505 has a built-in 3.25V references and an operational amplifier (OPA) with the ability to drive 10mA of load. The OPA will serve as a voltage follower to provide certain flexibility on application. Note that, the 3.25V reference has sourcing capability only.

Crystal Oscillator

This section has a crystal oscillator that can be used to generate timing signals like an A/D clock. The output level of Crystal Oscillator will be TTL compatible at the XOSCOA terminal.

Pin Assignments



Pin Descriptions

Pin Number	Pin Name	Description
1	IF_IN-	IF Input Complement.
2	IF_IN+	IF Input.
3	OUT	Output of OPA.
4	INP	Non-Inverting Input of OPA.
5	VRT	Output Reference Voltage for Top of A/D Input Range.
6	GND_BUF	Ground for Output Buffer.
7	BUF_OUT+	Differential Buffer/Driver Output.
8	BUF_OUT-	Differential Buffer/Driver Output Complement.
9	VCC_BUF	Supply Voltage for Output Buffer.
10	BUF_IN+	Differential Buffer/Driver Input.
11	NC	No Connect or Ground.
12	BUF_IN-	Differential Buffer/Driver Input Complement.
13	RFGND	Ground for High Frequency Crystal Oscillator.

Pin Descriptions (continued)

Pin Number	Pin Name	Description
14	XOSCOA	Crystal Oscillator Output (TTL compatible).
15	XTL1	Crystal Oscillator Frequency Select Circuit Connection.
16	XTL2	Crystal Oscillator Feedback Pin.
17	VCC_RF	Supply Voltage for High Frequency Crystal Oscillator.
18	VCCIF2	Supply Voltage for IF Output Sections.
19	IF_OUT-	IF Output Amplified, Complement.
20	IF_OUT+	IF Output Amplified.
21	GND_IF2	Ground for Amplified IF Output.
22	GND_IF1	Ground for IF Input Section.
23	NC	No Connect or Ground.
24	VCC_IF1	Supply Voltage for IF Input Section.

Absolute Maximum Ratings (Beyond which the device may be damaged)¹

Parameter	Description	Min.	Typ.	Max.	Units
V _{CC}	Supply Voltages ,VCC_IF1, VCC_IF2, VCC_BUF, VCC-RF			13.5	V
V _{in}	Input Voltages IF_IN+, IF_IN-, BUF_IN+, BUF_IN-, XTL1, XTL2	GND-0.3		VCC+0.3	V
I _{in}	Input Current (Power On or Off)			±10	mA
T _{stg}	Storage Temperature	-40		125	°C
T _j	Junction Temperature			150	°C
Θ _{JA}	SO24 Thermal Resistance		70		°C/W
Lead soldering	10 seconds			300	°C
Short Circuit Tolerance	No output can be shorted to ground				

Note:

- Functional Operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Units
VCC_IF1, VCC_IF2, VCC_BUF	Supply Voltages	8.5	12	13	V
VCC_RF	Supply Voltage	4.75	5	5.25	V
TA	Ambient Temperature	0	25	70	°C

DC Electrical Characteristics

VCC_RF = 5V; VCC_IF1, VCC_IF2, VCC_BUF = 12V; TA = 0 to 70°C, unless otherwise specified.

Parameter		Conditions	Min.	Typ.	Max.	Units
PW	Total Power Consumption			0.72	0.87	W
ICCIF1 + ICCIF2	IF Gain Stages total Supply Current	12V Supply		30	35	mA
ICCBUF	Buffer Supply Current (Including 10mA allocated for Band-gap Reference and OPA)	12V Supply		28	35	mA
ICCRF	XTL OSC Supply Current	5V Supply		12	15	mA
VRT	Top Reference Output Voltage	@ 5mA output	3.08	3.25	3.45	V
IOPA	Output Drive of OPA		-0.1		-15	mA
Vos	Output Offset of OPA	V _{OUT} = 2V	-8		+8	mV
I _{BIAS}	Input Bias Current of OPA	V _{INP} = 2V			-5	μA
PSRR	Power Rejection Ratio of OPA	VCC_BUF = 8.5 - 13.5V	55			dB
Avf	Gain of OPA (Voltage Follower)	V _{INP} = 2V	0.98	1.0	1.02	
V _{IOPA}	Input Range of OPA	I _O = 1mA	0.6		VCC_BUF - 3.0	V
IIF2O	Output Current Drive at IF_OUT+ and IF_OUT-				±15	mA
IBUFO	Output Current Drive at BUF_OUT+ and BUF_OUT-		±5		±15	mA
ΔVIFO	IFA DC Output Swing at IF_OUT+ and IF_OUT- (Differential)		4			V _{pp}
ΔVBUFO	Buffer DC Output Swing at BUF_OUT+ and BUF_OUT- (Differential)		4.0			V _{pp}
V _{OH}	High Level Output Voltage of XOSCOA		3.0			V
V _{OL}	Low Level Output Voltage of XOSCOA				0.5	V
I _{OH}	High Level Output Current of XOSCOA				-8	mA
I _{OL}	Low Level Output Current of XOSCOA		8			mA

Note:

1. All currents specified herein are quiescent current without loading on outputs.

AC Electrical Characteristics

VCC_RF = 5V; VCC_IF1, VCC_IF2, VCC_BUF = 12V; TA = 0 to 70°C, unless otherwise specified.

Parameter		Conditions	Min.	Typ.	Max.	Units
ZIFin	AC Input Impedance of IF Amplifier	@36MHz	2			KΩ
CIFin	AC Equivalent Input Cap	IF_IN+ & IF_IN-		6		pF
Vis	Input Sensitivity at Maximum Gain		50			dBμV
ZoIF2	AC Output Impedance of IF Amplifier	@36MHz			10	Ω
ZiBUF	AC Input Impedance of Buffer	@36MHz		7.5K Ω// 3.5pF		
ZoIF2	AC Output Impedance of Buffer	@36MHz			10	Ω
IMD3	Two Tone Intermodulation	Differential Output, BUF_OUT = +10dBm Differential AC Rload = 200Ω at IF_OUT+ & IF_OUT- f1/f2 = 35.5/36.5MHz	50			dBc
G	IF to Baseband Gain	Diff. Input and diff. Output	48		55	dB
NF	Noise Figure	@36MHz		9	12	dB
BW_IF	IF Bandwidth	±0.2dB for 10MHz bands	25	36	55	MHz
ΔBW	Bandwidth Roll-Off	31MHz-41MHz		0.1	0.15	dB
IΦ	Integrated Phase Noise	With TBD crystal@57.6MHz from 100Hz - 1MHz			0.5	deg r.m.s
ΦnXTL	XTAL OSC Phase Noise	@± 10KHz offset			-100	dBc/ Hz
dt/dv	Output Transition Rise or Fall Rate	XTL Oscillator Output, CL = 10pF			2.5	nS/V
dOSC	Duty Cycle of Output Pulse	XTL Oscillator Output, CL = 10pF	40		60	%

Performance Curves

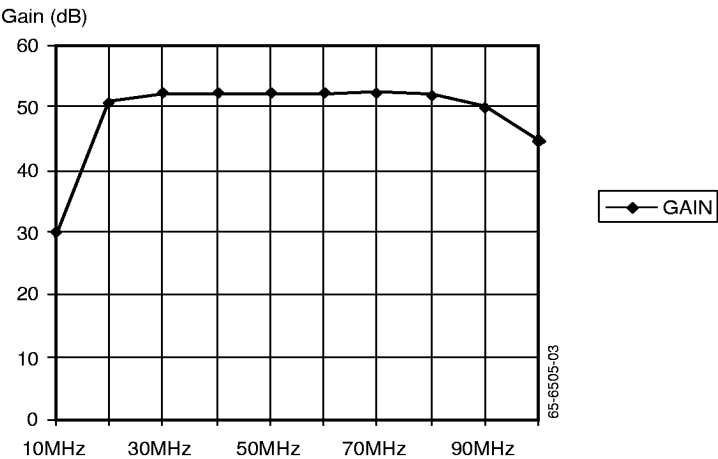


Figure 1. IF Input Bandwidth

Preliminary Information

using the crystal oscillator operating in the 3rd overtone mode at 57.6MHz and an external divided by 2 prescaler. The reference signals for A/D are the VRT and OUT outputs. The application is shown with the Fairchild Semiconductor Division's 10-bit ADC TMC1185. Other high performance A/Ds needing fully differential input can also be used. The A/D inputs are referenced to be in the mid-scale using the output from TMC1185. The filtered and buffered IF outputs can be a.c. coupled to the A/D inputs. In this application an external differential band-pass roofing filter is used to band-limit the signals before conversion.

Figure 3 shows details of circuits used to evaluate the performance of RC6505 with the TMC1185 A/D.

Figure 2. RC6505 Application in a Sub-sampling Digital Receiver for 256 QAM

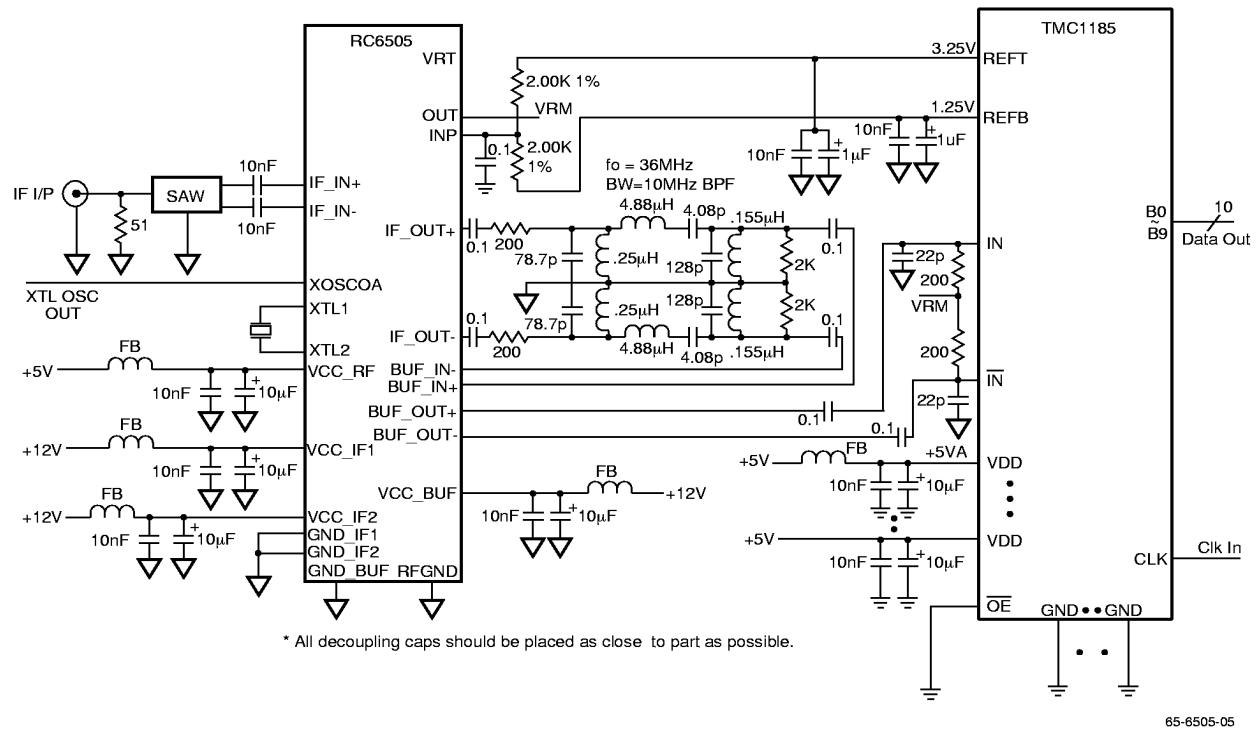
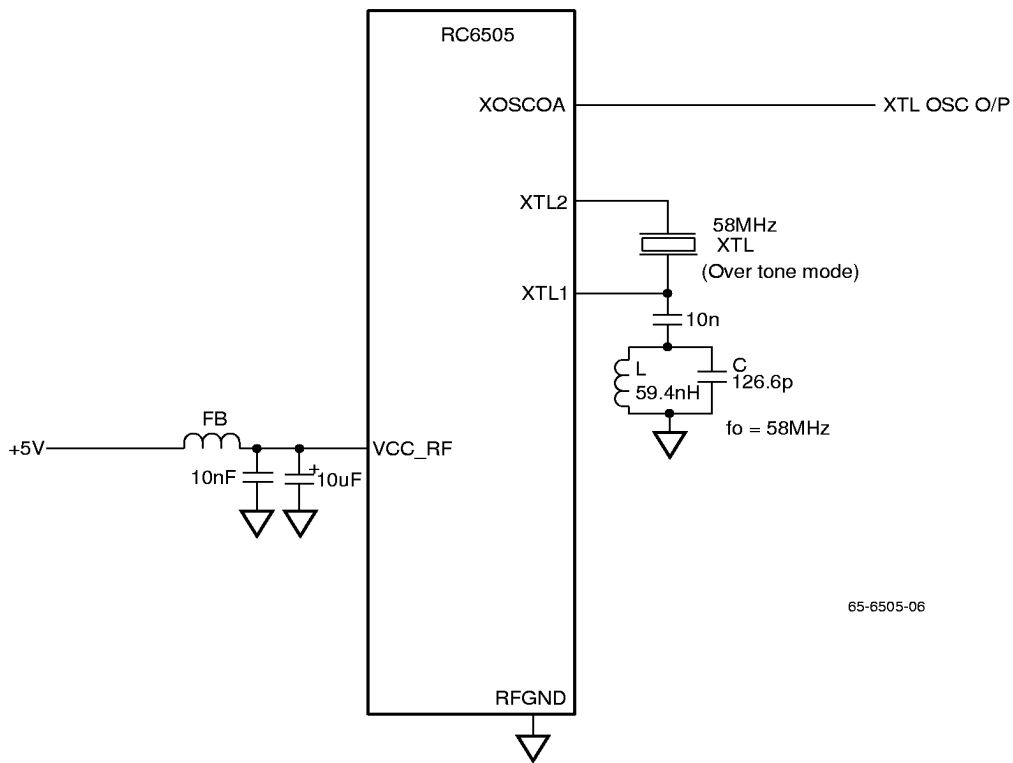


Figure 3. RC6505 interface with Fairchild Semiconductor Division's TMC1185 10-bit 40MSPS ADC (for reference only)

65-6505-05

Preliminary Information

Crystal Oscillator Operating in Over Tone Mode



Choose $Q = 12$ then using the following equations to calculate L and C . (Note that, $R_{in} = 260\ \Omega$ and f_O is given.)

$$2\pi f_O = (LC)^{-1/2}$$

$$Q = 2\pi f_O C R_{in}$$

Preliminary Information

Notes:

RC6505

PRODUCT SPECIFICATION

Notes:

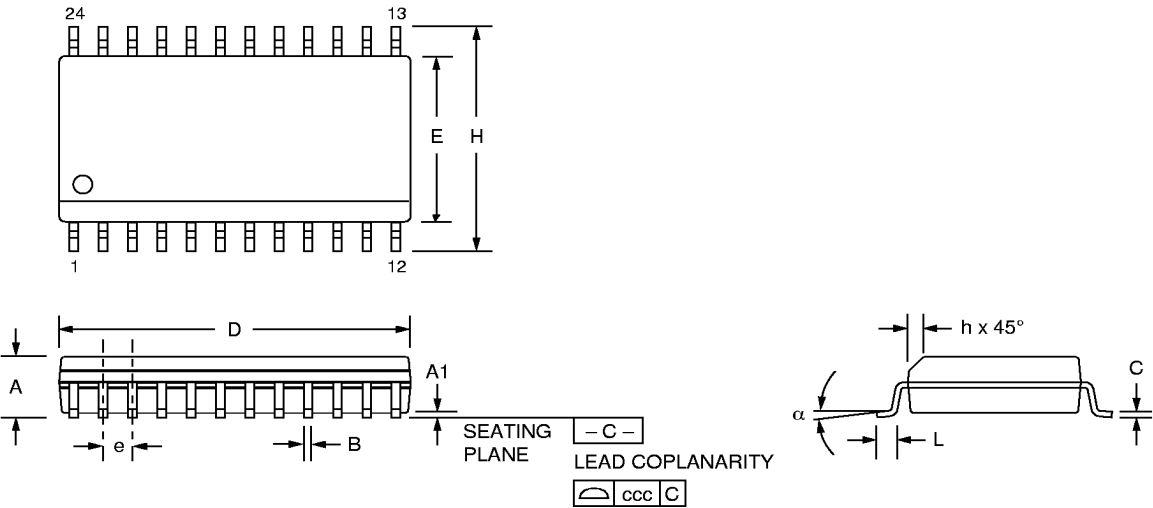
Preliminary Information

Mechanical Dimensions

24 Lead Small Outline IC (SOIC) – .300" Body Width

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.599	.614	15.20	15.60	2
E	.290	.299	7.36	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.020	0.25	0.51	
L	.016	.050	0.40	1.27	3
N	24		24		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

- Notes:
- 1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
 - 2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
 - 3. "L" is the length of terminal for soldering to a substrate.
 - 4. Terminal numbers are shown for reference only.
 - 5. "C" dimension does not include solder finish thickness.
 - 6. Symbol "N" is the maximum number of terminals.



Preliminary Information

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
RC6505M	0°C – 70°C	Commercial	24 Lead SOIC	RC6505M

Preliminary Information

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com