# RC9623DP Single Device Data/Fax Modem Data Pump

## INTRODUCTION

The Rockwell RC9623DP is a low power, V.22 bis 2400 bps data/fax modem data pump in a single VLSI package. The RC2324DPL is identical to the RC9623DP except fax modes are not provided. In this document, all references to the RC9623DP also apply to the RC2324DPL except for the fax modes and as otherwise noted.

The modem operates over the public switched telephone network (PSTN), as well as on point-to-point leased lines.

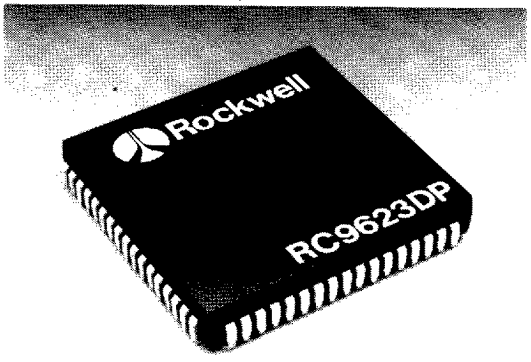
The modem supports data modes meeting the requirements specified in CCITT recommendations V.22 bis, V.22, V.23, and V.21, as well as Bell 212A and Bell 103.

The modem supports fax modes meeting the requirements specified in CCITT V.29, V.27 ter, and V.21 channel 2 synchronous.

Internal HDLC support eliminates the need for an external serial input/output (SIO) device or comparable functions in the host controller in products incorporating error correction and T.30 protocols.

The modem includes two CMOS VLSI functions—a digital signal processor (DSP) and an integrated analog function (IA). The RC9623DP integrates these functions into a single 68-pin plastic leaded chip carrier (PLCC).

Detailed hardware and software interface information is described in the RC9623DP and RC9624DP Designer's Guide (Order No. 822).




**RC9623DP Modem**

## FEATURES

- Single CMOS VLSI device
- Low power requirements
  - — Single voltage: + 5 Vdc ± 5%
  - —Operating: 300 mW (typical)
  - —Sleep: 15 mW (typical)
- 2-wire operation
  - —Full-duplex (FDX) for data modes
  - —Half-duplex (HDX) for fax modes
- Data configurations:
  - —V.22 bis, V.22, V.23, V.21
  - —Bell 212A, Bell 103
- Fax configurations (RC9623DP):
  - —V.29, V.27 ter, V.21 Channel 2
- Voice mode
- DTMF detection
- Receive dynamic range: –9 dBm to –43 dBm
- Transmit level: –10 dBm ±1 dB using internal hybrid circuit; attentuation selectable in 1 dB steps
- Multi-mode data/fax detection support
- V.22 bis fallback/fall-forward – 2400/1200 bps
- Serial data: synchronous and asynchronous
- Parallel data: synchronous (including HDLC) and asynchronous
- Programmable ring detect
- Programmable dialer
- Programmable tone detect bandpass filters
- Adjustable speaker output to monitor received signal
- Diagnostics
- Host bus interface memory for configuration, control, and parallel data; 8086 microprocessor bus compatible
- 5-pin serial data interface; TTL compatible
- Equalization
  - —Adaptive equalizer in receiver
  - —Selectable and programmable fixed compromise equalizers in both receiver and transmitter
- Loopback configurations
  - —Local analog, local digital, and remote digital
- Answer and originate handshake in data modes
- Training sequences for fax modes
- Leased line operation

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## TECHNICAL SPECIFICATIONS

### CONFIGURATIONS AND RATES

The selectable modem configurations, along with the corresponding signaling (baud) rates and data rates, are listed in Table 1 (CONF bits).

**Note:** Bit names refer to control or status bits in DSP interface memory which are set or reset by the host processor (see Figure 4 and Table 10).

### DATA ENCODING

The data encoding conforms to CCITT recommendations V.29, V.27 ter, V.22 bis, V.22, V.23, or V.21, or to Bell 212A or 103, depending on the selected configuration.

### TONE GENERATION

**Answer Tone:** A CCITT (2100 ± 15 Hz) or Bell (2225 ± 10 Hz) answer tone can be generated.

**Guard Tone:** A 1800 ± 20 Hz guard tone can be generated (enabled by the GTE bit).

**DTMF Tones:** Dual tone multi-frequency (DTMF) tones can be generated with a frequency accuracy of ±1.5% (Table 2).

**User Defined Tones:** A user-defined single or dual tone can be generated from 200 Hz to 3000 Hz ± 5 Hz.

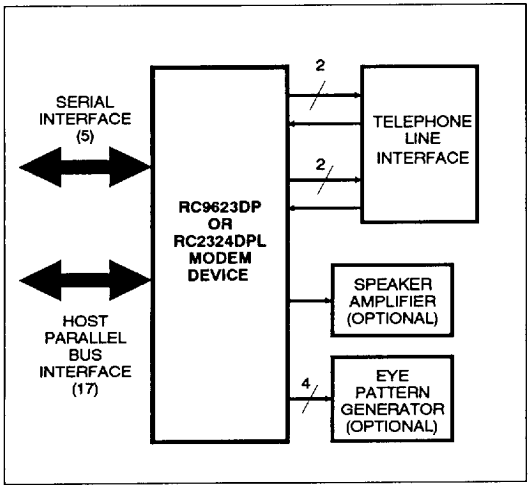


**Figure 1. RC9623DP or RC2324DPL Modem General**

### TONE DETECTION

**Answer Tone and Call Progress Tones:** Tones can be detected as follows:

Call progress frequency range: 340 ± 5 Hz to 640 ± 5 Hz

Answer tone frequency ranges: CCITT (2100 ± 15 Hz), Bell (2225 ± 10 Hz), or Bell FSK originate tone (1270 ± 10 Hz)

Detection range: –9 dBm to –43 dBm

Default detection threshold: –43 dBm

Response time: 75 ± 2 ms

The passband and tone detect threshold can be changed in DSP RAM.

**V.23 and V.21 Tones:** Tones can be detected as follows:

V.23 forward channel mark: 1300 ± 10 Hz

V.23 backward channel mark: 390 ± 10 Hz

V.21 high band mark (1650 ± 10 Hz) or low band mark (980 ± 10 Hz)

Detection range: –9 dBm to –43 dBm

Default detection threshold: –43 dBm

Response time: 25 ± 2 ms

The passbands and tone detect thresholds can also be changed in the DSP RAM.

### DTMF DETECTION

The modem can detect a valid DTMF tone pair (indicated by DTDET) and load a corresponding hexadecimal code into the modem interface memory (DTDIG).

### EQUALIZERS

Equalization functions are incorporated that improve performance when operating over low quality lines.

**Automatic Adaptive Equalizer.** An automatic adaptive equalizer in the receiver compensates for transmission line amplitude and group delay distortion. Updating of the taps can be enabled or disabled (EQFZ bit). The equalizer taps can also be reset (EQRES bit).

**Fixed Compromise Equalizers.** Fixed compromise equalizers are provided in the transmitter and receiver. The equalizers are programmable in DSP RAM.

### TRANSMIT LEVEL

The transmitter output level is –10 dBm ±1 dB using the internal hybrid circuit (see Figure 5). The attentuation is selectable from 0 dBm to –15 dBm in 1 dB steps (TLVL bits).

### TRANSMIT TIMING

Transmitter timing is selectable between internal (±0.01%), external , or loopback (TXCLK bits). When external clock is selected, the external clock rate must equal the desired data rate ±0.01% with a duty cycle of 50 ± 20%.

### SCRAMBLER/DESCRAMBLER

The modem incorporates a self-synchronizing scrambler/descrambler satisfying the applicable CCITT or Bell requirement. The scrambler and descrambler can be enabled or disabled (SDIS and DDIS bits, respectively).

### RECEIVE LEVEL

The receiver satisfies performance requirements for a received line signal from –9 dBm to –43 dBm. The default RLSD turn-on and RLSD turn-off thresholds are –43 dBm and –48 dBm, respectively. The RLSD threshold levels are programmable in DSP RAM.

### RECEIVER TIMING

The modem can track a frequency error up to ±0.03% in the associated transmit timing source.

### CARRIER RECOVERY

The modem can track a frequency offset up to ±7 Hz in the received carrier with less than a 0.2 dB degradation in bit error rate (BER).

**Table 2. Dial Digits/Tone Pairs**

| Dial Digit | Tone 1(Hz) | Tone 2 (Hz) |
|---|---|---|
| 1 | 697 | 1209 |
| 2 | 697 | 1336 |
| 3 | 697 | 1477 |
| 4 | 770 | 1209 |
| 5 | 770 | 1336 |
| 6 | 770 | 1477 |
| 7 | 852 | 1209 |
| 8 | 852 | 1336 |
| 9 | 852 | 1477 |
| 0 | 941 | 1336 |
| * | 941 | 1209 |
| # | 941 | 1477 |
| Spare (B) | 697 | 1633 |
| Spare (C) | 770 | 1633 |
| Spare (D) | 852 | 1633 |
| Spare (F) | 941 | 1633 |

**Table 1. Configurations, Signaling and Data Rates**

| Configuration | Modulation[1] | Transmitter Carrier Frequency (Hz) ±0.01% Answer[2] | Originate[2] | Data Rate (bps) ± 0.01% | Baud (Symbols/Sec.) | Bits Per Symbol | Constellation Points | Sample Rate (Samples/Sec.) |
|---|---|---|---|---|---|---|---|---|
| **Data Modes** | | | | | | | | |
| V.22 bis | QAM | 2400 | 1200 | 2400[3] | 600 | 4 | 16 | 7200 |
| V.22 | DPSK | 2400 | 1200 | 1200[3] | 600 | 2 | 4 | 7200 |
| | | 2400 | 1200 | 600[3] | 600 | 1 | 2 | 7200 |
| Bell 212A | DPSK | 2400 | 1200 | 1200[3] | 600 | 2 | 4 | 7200 |
| Bell 103 | FSK | 2225 M<br>2025 S | 1270 M<br>1070 S | 0-300[4] | 0-300[4] | 1 | 1 | 7200 |
| V.21 | FSK | 1650 M<br>1850 S | 980 M<br>1180 S | 0-300[4] | 0-300[4] | 1 | 1 | 7500 |
| V.23 Forward Channel[5] | FSK | 1300 M<br>2100 S | 1300 M<br>2100 S | 1200 | 1200 | 1 | 1 | 9600[7] |
| V.23 Backward Channel[5] | FSK | 390 M<br>450 S | 390 M<br>450 S | 75 | 75 | 1 | 1 | 7200 |
| **Fax Modes[6]** | | | | | | | | |
| V.29 | QAM | 1700 | 1700 | 9600 | 2400 | 4 | 16 | 9600 |
| | QAM | 1700 | 1700 | 7200 | 2400 | 3 | 8 | 7200 |
| | QAM | 1700 | 1700 | 4800 | 2400 | 2 | 4 | 9600 |
| V.27 ter | DPSK | 1800 | 1800 | 4800 | 1600 | 3 | 8 | 9600 |
| | DPSK | 1800 | 1800 | 2400 | 1200 | 2 | 4 | 9600 |
| V.21 channel 2 | FSK | 1650 M<br>1850 S | 1650 M<br>1850 S | 300 | 300 | 1 | 1 | 9600 |
| **Dial/Call Progress Mode** | | | | | 600 | | | 7200 |
| **Tone Generator/ Tone Detector Mode** | | | | | 600 | | | 7200 |

**Notes:**

1. Modulation legend: QAM Quadrature Amplitude Modulation; DPSK Differential Phase Shift Keying; FSK Frequency Shift Keying
2. M indicates a mark condition; S indicates a space condition.
3. Synchronous accuracy = ±0.01%; asynchronous accuracy = –2.5% to +1.0% (+2.3% if extended overspeed is selected).
4. Value is upper limit for serial (e.g., 0-300).
5. RC9623DP and RC2324DPL only.
6. RC9623DP and RC9624DP only.
7. 9600 samples per sec in V.23 FDX Tx75/Rx1200; 7200 samples per second in V.23 FDX Tx1200/Rx75.

### RTS-CTS Turn-On and Turn-Off Sequences

RTS ON to CTS ON and RTS OFF to CTS OFF response times are listed in Table 3.

In V.21, the transmitter turns off within 10 ms after RTS goes OFF.

For V.29, the turn-off sequence consists of approximately 5 ms of remaining data and scrambled ones followed by a 50 ms period of no transmitted energy.

For V.27 ter, the turn-off sequence consists of approximately 7 ms of remaining data and scrambled ones at 1200 baud or approximately 7.5 ms of data and scrambled ones at 1600 baud followed by a 20 ms period of no transmitted energy.

### SERIAL OR PARALLEL INTERFACE

The TPDM bit selects serial or parallel interface.

**Serial Interface.** The five hardware lines (RXD, TXD, TDCLK, RDCLK, and XTCLK) are supported by four control and status bits in the interface memory (CTS, DSR, RTS, and RLSD).

**Parallel Interface.** A 8086-compatible parallel microprocessor bus is supported.

### VOICE MODE

**Transmit Voice.** Transmit voice samples can be sent to the modem digital-to-analog converter (DAC) from the host through the transmit data buffer.

**Receive Voice.** Received voice samples from the modem analog-to-digital converter (ADC) can be read by the host from the receive data buffer.

### ASYNCHRONOUS CONVERSION

Asynchronous mode is selected by the ASYNC bit. The asynchronous character format is 1 start bit, 5 to 8 data bits (WDSZ bits), an optional parity bit (PARSL and PEN bits), and 1 or 2 stop bits (STB bit). Valid character size, including all bits, is 7, 8, 9, 10 or 11 bits per character.

**Table 3. RTS-CTS Response Times**

| Configuration | Turn On Time | Turn Off Time |
|---|---|---|
| **Data Modes** | | |
| V.22 bis, V.22, and Bell 212A (CC bit = 0) | ≤2 ms | ≤ 2 ms |
| V.22 bis, V.22, and Bell 212A (CC bit = 1) | 270 ms | ≤ 2 ms |
| V.21 and Bell 103 | 2-5 ms | 10 ms |
| V.23 | 11 ms | ≤ 2 ms |
| **Fax Modes (RC9623DP only)** | | |
| **Echo Protector Tone Disabled (NV25 = 1)** | | |
| V.29 (All speeds) | 253 ms | ≤ 2 ms |
| V.27 4800 | 898 ms | ≤ 2 ms |
| V.27 2400 | 1133 ms | 9 ms |
| V.21 | 20 ms | 4 ms |
| **Echo Protector Tone Enabled (NV25 = 0)** | | |
| V.29 (All speeds) | 253 ms | ≤ 2 ms |
| V.27 4800 | 1103 ms | ≤ 2 ms |
| V.27 2400 | 1338 ms | 9 ms |
| V.21 | 3095 ms | 4 ms |

**Signalling Rate Range.** Signalling rate range is selectable by the EXOS bit:

Basic range: +1% to −2.5%

Extended overspeed range: +2.3% to −2.5%

**Break.** Break is handled as described in V.22 bis.

### POWER AND ENVIRONMENTAL REQUIREMENTS

The power requirements are specified in Table 4. The environmental specifications are listed in Table 5.

## COMPATIBILITY

The modem is functionally backward compatible with the RC2324DP/1 with the following general enhancements and differences:

- —Addition of V.29, V.27 ter, and V.21 channel 2 fax modes (RC9623DP).
- —Addition of voice mode.
- —Addition of DTMF detection.
- —Inclusion of hybrid filtering components into the internal IA function thus reducing the need for external components.
- —Incorporation of speaker output control circuit in the IA function and a SPKR output signal.
- —Addition of a low-power sleep mode.
- —Addition of a second relay driver output control bit.
- —Deletion of −5VDC power supply requirement.
- —Different pin assignments.

**Table 4. Modem Power Requirements**

| Voltage | Mode | Current (Typ.) @ 25°C | Current (Max.) @ 0°C |
|---|---|---|---|
| 5 VDC ±5% | Operating | 60 mA | 90 mA |
| | Sleep | 3 mA | 4.5 mA |

**Note:** Input voltage ripple ≤ 0.1 volts peak-to-peak. The amplitude of any frequency between 20 kHz and 150 kHz must be less than 500 microvolts peak.

**Table 5. Modem Environmental Specifications**

| Parameter | Specification |
|---|---|
| Temperature | |
| Operating | 0°C to 70°C (32°F to 158°F) |
| Storage | −40°C to 80°C (−40°F to 176°F) |
| Relative Humidity | Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less. |
| Altitude | − 200 feet to +10,000 feet |

## HARDWARE INTERFACE

The modem functional hardware interface signals are shown in Figure 2. In this diagram, any point that is active low is represented by a small circle at the signal point.

Edge triggered inputs are denoted by a small triangle (e.g., TDCLK). Open-Collector (open-source or open-drain) outputs are denoted by a small half-circle (e.g., $\overline{IRQ}$). Active low signals are overscored (e.g., $\overline{POR}$).

A clock intended to activate logic on its rising edge (low-to-high transition) is called active low (e.g., $\overline{RDCLK}$), while a clock intended to activate logic on its falling edge (high-to-low transition) is called active high (e.g., TDCLK). When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

The modem pin assignments are shown in Figure 3. The pin assignments are listed by pin number in Table 6.

The hardware interface signal functions are summarized by major interface in Table 7.

The digital and analog interface characteristics are defined in Tables 8 and 9, respectively.

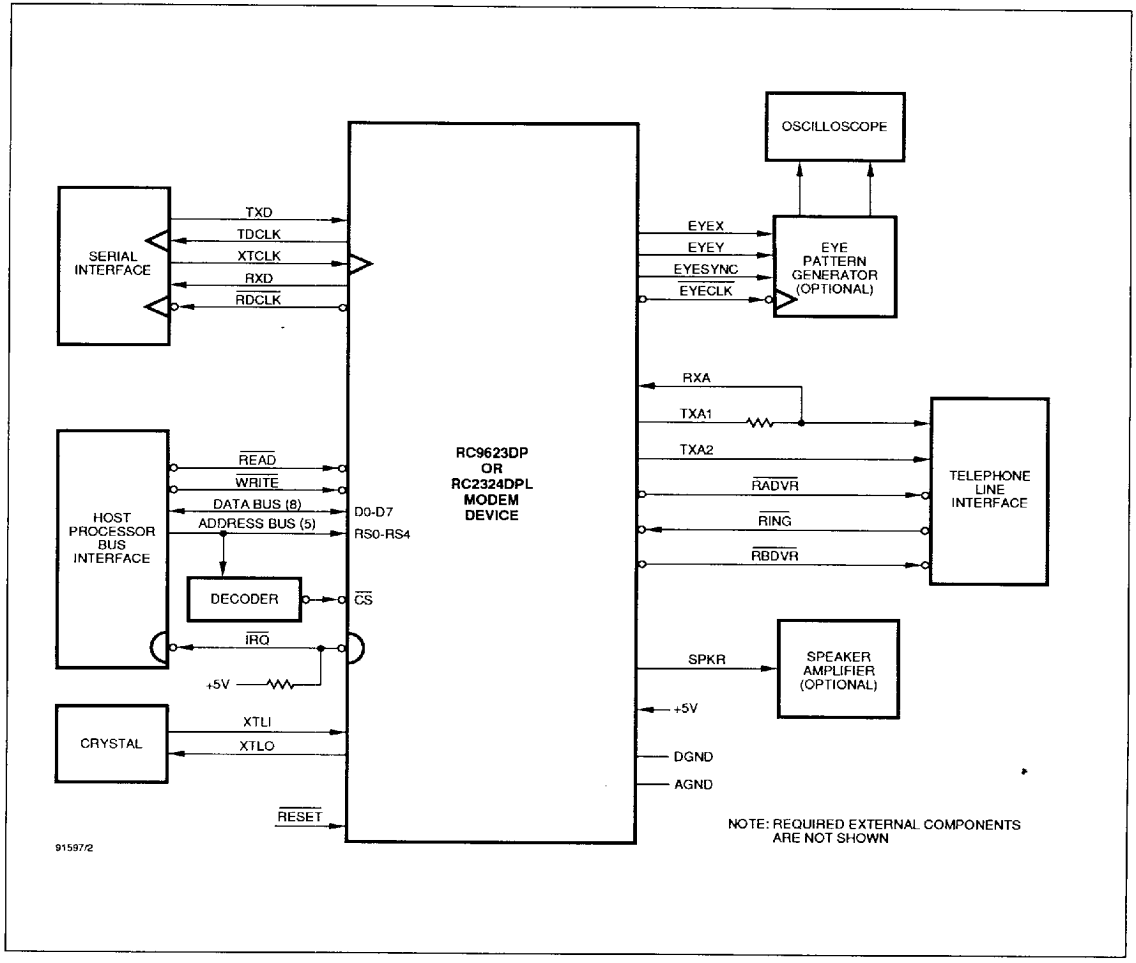


**Figure 2. RC9623DP Functional Interface Signals**

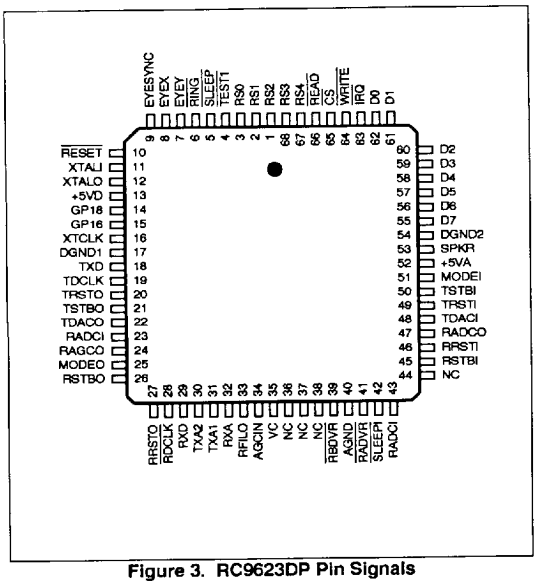


**Figure 3. RC9623DP Pin Signals**

**Table 6. RC9623DP Modem Device Pin Signals**

| Pin Number | Signal Name | I/O Type |
|---|---|---|
| 1 | RS2 | IA |
| 2 | RS1 | IA |
| 3 | RS0 | IA |
| 4 | TEST1 | |
| 5 | SLEEP | OA |
| 6 | RING | |
| 7 | EYEY | OB |
| 8 | EYEX | OB |
| 9 | EYESYNC | OB |
| 10 | RESET | ID |
| 11 | XTLI | IE |
| 12 | XTLO | OB |
| 13 | +5VD | |
| 14 | GP18 | OA |
| 15 | GP16 | OA |
| 16 | XTCLK | IA |
| 17 | DGND1 | |
| 18 | TXD | IA |
| 19 | TDCLK | OA |
| 20 | TRSTO | MI |
| 21 | TSTBO | MI |
| 22 | TDACO | MI |
| 23 | RADCI | MI |
| 24 | RAGCO | MI |
| 25 | MODEO | MI |
| 26 | RSTBO | MI |
| 27 | RRSTO | MI |
| 28 | RDCLK | OA |
| 29 | RXD | OA |
| 30 | TXA2 | O(DD) |
| 31 | TXA1 | O(DD) |
| 32 | RXA | I(DA) |
| 33 | RFILO | MI |
| 34 | AGCIN | MI |
| 35 | VC | |
| 36 | NC | |
| 37 | NC | |
| 38 | NC | |
| 39 | RBDVR | OD |
| 40 | AGND | |
| 41 | RADRV | OD |
| 42 | SLEEPI | IA |
| 43 | RAGCI | MI |
| 44 | NC | |
| 45 | RSTBI | MI |
| 46 | RRSTI | MI |
| 47 | RADCO | MI |
| 48 | TDACI | MI |
| 49 | TRSTI | MI |
| 50 | TSTBI | MI |
| 51 | MODEI | MI |
| 52 | +5VA | |
| 53 | SPKR | O(OF) |
| 54 | DGND2 | |
| 55 | D7 | IA/OB |
| 56 | D6 | IA/OB |
| 57 | D5 | IA/OB |
| 58 | D4 | IA/OB |
| 59 | D3 | IA/OB |
| 60 | D2 | IA/OB |
| 61 | D1 | IA/OB |
| 62 | D0 | IA/OB |
| 63 | IRQ | OC |
| 64 | WRITE | IA |
| 65 | CS | IA |
| 66 | READ | IA |
| 67 | RS4 | IA |
| 68 | RS3 | IA |

**Notes:**
1. MI = Modem Interconnection.
2. NC = No connection (may have internal connection; leave pin disconnected (open).
3. I/O types are described in Table 8 (digital signals) and Table 9 (analog signals).

**Table 7. Hardware Interface Signal Definitions**

| Label | I/O Type | Signal/Definition |
|---|---|---|
| | | **OVERHEAD SIGNALS** |
| XTLI<br>XTLO | IE<br>OB | **Crystal/Clock In and Crystal Out.** The DSP must be connected to an external crystal circuit consisting of a 24.00014 MHz crystal and two capacitors. Alternatively, XTLI, may be driven with a buffered clock (e.g., square wave generator) or a sine wave oscillator. |
| $\overline{\text{RESET}}$ | ID | **Reset.** The active low $\overline{\text{RESET}}$ input resets the internal modem logic. Upon transition of $\overline{\text{RESET}}$ from low-to-high, the DSP interface memory bits are set to the default values. |
| + 5VD | PWR | **+ 5V Digital Supply.** +5V ±5% is required. |
| + 5VA | PWR | **+ 5V Analog Supply.** +5V ±5% is required. |
| DGND | GND | **Digital Ground.** |
| AGND | GND | **Analog Ground.** |
| | | **SERIAL INTERFACE** |
| | | Five TTL-level hardware interface circuits implement a CCITT V.24-compatible serial data interface with control signals provided through the DSP interface memory. |
| $\overline{\text{RDCLK}}$ | OA | **Receive Data Clock.** In synchronous mode, the modem outputs a Receive Data Clock ($\overline{\text{RDCLK}}$) in the form of 50 ±1% duty cycle square wave. The low-to-high transitions of this output coincide with the center of received data bits. |
| TDCLK | OA | **Transmit Data Clock.** In synchronous mode, the modem outputs a Transmit Data Clock (TDCLK). The TDCLK clock frequency is data rate ±0.01% with a duty cycle of 50 ± 1%. |
| XTCLK | IA | **External Transmit Clock.** In synchronous mode, an external transmit data clock input (XTCLK) can be supplied. |
| RXD | OA | **Received Data.** The modem presents received serial data on the Received Data (RXD) output and to the interface memory Receive Data Register (RBUFFER) in both serial and parallel modes. |
| TXD | IA | **Transmitted Data.** The modem obtains serial data to be transmitted on the TXD input in serial mode, or from the interface memory Transmit Data Register (TBUFFER) in parallel mode. (See TPDM bit.) |
| | | **PARALLEL MICROPROCESSOR INTERFACE** |
| | | Address, data, control and interrupt hardware interface signals implement an 8086-compatible parallel microprocessor interface to a host processor. This parallel interface allows the host to change modem configuration, read or write channel and diagnostic data, and supervise modem operation by writing control bits and reading status bits. |
| D0–D7 | IA/OA | **Data Lines.** Eight bidirectional data lines (D0–D7) provide parallel transfer of data between the host and the modem. |
| $\overline{\text{CS}}$ | IA | **Chip Select.** The active low Chip Select ($\overline{\text{CS}}$) input enables parallel data transfer over the microprocessor bus. |
| RS0 - RS4 | IA | **Register Select Lines.** The five active high Register Select inputs (RS0 - RS4) address interface memory registers in the modem when $\overline{\text{CS}}$ is low. These lines are typically connected to address lines A0-A4 to address one of 32 8-bit internal interface memory registers (00-1F). The selected register can be read from, or written into, via the 8-bit parallel data bus (D0-D7). |
| $\overline{\text{READ}}$<br>$\overline{\text{WRITE}}$ | IA<br>IA | **Read Enable and Write Enable.** Reading or writing is controlled by the host pulsing either $\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ input low, respectively, during the microprocessor bus access cycle.<br>During a write cycle, data from the data bus is copied into the addressed DSP interface memory register, with high and low bus levels representing one and zero bit states, respectively. |
| $\overline{\text{IRQ}}$ | OA | **Interrupt Request.** The $\overline{\text{IRQ}}$ output structure is an open-drain field-effect-transistor (FET). The $\overline{\text{IRQ}}$ output can be enabled in the interface memory to allow immediate indication of change of conditions in the modem. The use of $\overline{\text{IRQ}}$ is optional depending upon modem application. |

**Table 7. Hardware Interface Signal Definitions (Cont'd)**

| Label | I/O Type | Signal/Definition |
|---|---|---|
| | | **HYBRID CIRCUIT** |
| TXA1<br>TXA2 | O(DF) | **Transmit Analog 1 and 2.** The TXA1 and TXA2 outputs are differential outputs 180 degrees out of phase with each other. |
| RXA | I(DA) | **Receive Analog.** RXA is a single-ended receive data input from the telephone line interface or an optional external hybrid circuit. |
| VC | OA | **Centerpoint Voltage.** VC is a +2.5 VDC centerpoint voltage which serves as the internal "analog ground" reference point. |
| | | **TELEPHONE LINE INTERFACE** |
| $\overline{\text{RADVR}}$ | OD | **Relay A Driver.** $\overline{\text{RADVR}}$ is an open drain output which can directly drive a relay with greater than 360 Ω coil resistance and having a "must operate" voltage of no greater than 4.0 VDC.<br><br>The $\overline{\text{RADVR}}$ output is controlled by the state of the RA bit, except in pulse dial mode. When RA is a 1, the $\overline{\text{RADVR}}$ output is active which applies current to the relay coil.<br><br>In a typical application, $\overline{\text{RADVR}}$ is connected to the normally open Off-Hook relay. In this case, $\overline{\text{RADVR}}$ active closes the Off-Hook relay to connect the modem to the telephone line. |
| $\overline{\text{RBDVR}}$ | OD | **Relay B Driver.** $\overline{\text{RBDVR}}$ is an open drain output which can directly drive a relay with greater than 360 Ω coil resistance and having a "must operate" voltage of no greater than 4.0 VDC.<br><br>$\overline{\text{RBDVR}}$ output is controlled by the state of the RB bit. When RB is a 1, the $\overline{\text{RBDVR}}$ output is active which applies current to the relay coil.<br><br>In a typical application, $\overline{\text{RBDVR}}$ is connected to the normally closed Talk/Data relay. In this case, $\overline{\text{RBDVR}}$ active opens the relay to disconnect the handset from the telephone line. |
| $\overline{\text{RING}}$ | IA | **Ring Frequency.** A low-going edge on the $\overline{\text{RING}}$ input initiates a ring frequency measurement. A valid ring detection is indicated by the RI bit. |
| | | **SPEAKER INTERFACE** |
| SPKR | O(DF) | **Speaker Analog Output.** The SPKR output reflects the received analog input signal. The SPKR on/off and three levels of attenuation are controlled by interface memory bits. When the speaker is turned off, the SPKR output is clamped to the voltage at the VC pin. The SPKR output can drive an impedance as low as 300 ohms. In a typical application, the SPKR output is an input to an external LM386 audio power amplifier. |
| | | **SLEEP MODE SIGNALS** |
| $\overline{\text{SLEEP}}$<br>$\overline{\text{SLEEPI}}$ | OA<br>IA | **Sleep Mode Output and Sleep Mode Input.** $\overline{\text{SLEEP}}$ output high indicates the DSP is operating in its normal mode. $\overline{\text{SLEEP}}$ low indicates that the DSP is in the sleep mode. This signal must be connected to the $\overline{\text{SLEEPI}}$ input to power down the IA in the sleep mode. $\overline{\text{SLEEP}}$ can also be used to control power to other devices (e.g., as a speaker enable). |
| | | **DIAGNOSTIC SIGNALS**<br><br>Four signals provide the timing and data necessary to create an oscilloscope quadrature eye pattern. The eye pattern is simply a display of the received baseband constellation. By observing this constellation, common line disturbances can usually be identified. |
| EYEX,<br>EYEY | OB | **Eye Pattern Data X and Eye Pattern Data Y.** The EYEX and EYEY outputs provide two serial bit streams containing data for display on the oscilloscope horizontal (X) axis and vertical (Y) axis, respectively. This serial digital data can be converted to analog form using two shift registers and two digital-to-analog converters (DACs). |
| $\overline{\text{EYECLK}}$<br>(RRSTO) | OA | **Eye Pattern Clock.** EYECLK is a clock for use by the serial-to-parallel converters. The $\overline{\text{EYECLK}}$ output is a 7200/9600 Hz clock. |
| EYESYNC | OB | **Eye Pattern Sync.** EYESYNC is a strobe for word synchronization. The falling edge of EYESYNC may be used to transfer the 8-bit word from the shift register to a holding register. Digital-to-analog conversion can then be performed for driving the X and Y inputs of an oscilloscope. |

**Table 7. Hardware Interface Signal Definitions (Cont'd)**

| Label | I/O Type | Signal/Definition |
|---|---|---|
| | | **MODEM INTERCONNECT** |
| RFILO | MI | **Receive Filter Output.** RFILO is the output of the internal receive analog filter which must be connected to AGCIN through a 0.1 µF, 20%, DC decoupling capacitor. |
| AGCIN | MI | **Receive AGC Gain Amplifier Input.** See RFILO. |
| MODEO (DSP), MODEI (IA) | MI | **Mode Control.** Serial IA mode control bits. Direct modem interconnect line. |
| TDACO (DSP), TDACI (IA) | MI | **Transmitter DAC Signal.** Transmitter serial digital DAC signal. Direct modem interconnect line. |
| TSTBO (DSP), TSTBI (IA) | MI | **Transmitter Strobe.** Transmitter 576 kHz digital timing reference. Direct modem interconnect line. |
| TRSTO (DSP), TRSTI (IA) | MI | **Transmitter Reset.** Transmitter 7200/9600 Hz digital timing reference. Direct modem interconnect line. |
| RADCI (DSP), RADCO (IA) | MI | **Receiver ADC Signal.** Receiver serial digital ADC signal. Direct modem interconnect line. |
| RAGCO (DSP), RAGCI (IA) | MI | **Receiver AGC Signal.** Receiver serial digital AGC signal. Direct modem interconnect line. |
| RSRBO (DSP), RSRBI (IA) | MI | **Receiver Strobe.** Receiver 576 kHz digital timing reference. Direct modem interconnect line. |
| RRSTO (DSP), RRSTI (IA) | MI | **Receiver Reset.** Receiver 7200/9600 Hz digital timing reference. Direct modem interconnect line. |

**Table 8. Digital Interface Characteristics**

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions[1] |
|---|---|---|---|---|---|---|
| Input High Voltage | $V_{IH}$ | | | | Vdc | |
| Type IA | | 2.0 | – | $V_{CC}$ | | |
| Type ID | | 0.8($V_{CC}$) | – | $V_{CC}$ | | |
| Input Low Voltage | $V_{IL}$ | –0.3 | – | 0.8 | Vdc | |
| Input Low Current | $I_{IL}$ | – | – | –400 | µA | $V_{CC}$ = 5.25V |
| Output High Voltage | $V_{OH}$ | | | | Vdc | |
| Types OA and OB | | 3.5 | – | – | | $I_{LOAD}$ = – 100 µA |
| Type OD | | – | – | $V_{CC}$ | | $I_{LOAD}$ = 0 mA |
| Output Low Voltage | $V_{OL}$ | | | | Vdc | |
| Types OA and OC | | – | – | 0.4 | | $I_{LOAD}$ = 1.6 mA |
| Type OB | | – | – | 0.4 | | $I_{LOAD}$ = 0.8 mA |
| Type OD | | – | | 0.75 | | $I_{LOAD}$ = 15 mA |
| Three–State Input Current (Off) | $I_{TSI}$ | – | – | ±10 | µA | $V_{IN}$ = 0.4 to $V_{CC}$ –1 |
| Power Dissipation | $P_D$ | | | | mW | |
| Operating | | – | 300 | 450 | | |
| Sleep | | – | 15 | 22.5 | | |

**Notes:**
1. Test Conditions: $V_{CC}$ = 5V ± 5%, $T_A$ = 0°C to 70°C (unless otherwise noted).

**Table 9. Analog Interface Characteristics**

| Name | Type | Characteristic |
|---|---|---|
| RXA | I (DA) | 1458 type op amp input |
| TXA1, TXA2 | O (DD) | 1458 type op amp output |
| SPKR | O (DF) | 1458 type op amp output |

## SOFTWARE INTERFACE

### INTERFACE MEMORY

The DSP communicates with the host by means of a dual-port, interface memory. The interface memory in the DSP contains thirty-two 8-bit registers, labeled register 00 through 1F. Each register can be read from, or written into, by both the host and the DSP. The host communicates with the DSP interface memory via the microprocessor bus.

The host can control modem operation by writing control bits to DSP interface memory and writing parameter values to DSP RAM through the interface memory. The host can monitor modem operation by reading status bits from DSP interface memory and reading parameter values from DSP RAM through interface memory.

### INTERFACE MEMORY MAP

A memory map of DSP interface memory identifying the contents of the 32 addressable registers is shown in Figure 4. These 8-bit registers may be read or written during any host read or write cycle. In order to operate on a single bit or group of bits in a register, the host must read a register then mask out unwanted data. When writing a single bit or group of bits in a register, the host must perform a read-modify-write operation. That is, the host must read the entire register, set or reset the necessary bits without altering the other register bits, then write the unaffected and modified bits back into the interface memory register.

### INTERFACE MEMORY BIT FUNCTIONS

Table 10 summarizes the functions of the individual bits in the interface memory. Bits in the interface memory are referred to using the format Z:Q. The register number is denoted by Z (00 through 1F) and the bit number is located by Q (0 through 7, where 0 = LSB).

| Register Function | Register Address (Hex) | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Interrupt Handling | 1F | NSIA | NCIA | — | NSIE | NEWS | NCIE | — | NEWC |
| | 1E | TDBIA | RDBIA | TDBIE | — | TDBE | RDBIE | — | RDBF |
| RAM Access, Control and Status | 1D | XACC | — | — | — | IOX | XCRD | XWT | XCR |
| | 1C | X RAM ADDRESS (XADD) | | | | | | | |
| | 1B | YACC | — | — | — | — | YCRD | YWT | YCR |
| | 1A | Y RAM ADDRESS (YADD) | | | | | | | |
| | 19 | X RAM DATA MSB (XDAM) | | | | | | | |
| | 18 | X RAM DATA LSB (XDAL) | | | | | | | |
| | 17 | Y RAM DATA MSB (YDAM) | | | | | | | |
| | 16 | Y RAM DATA LSB (YDAL) | | | | | | | |
| — | 15 | — | — | — | — | — | — | — | — |
| — | 14 | — | — | — | — | — | — | — | — |
| Control | 13 | TLVL | | | | VOL | | TXCLK | |
| | 12 | CONFIGURATION (CONF) | | | | | | | |
| Transmit Data Buffer | 11 | — | — | — | — | — | — | — | TXP |
| | 10 | TRANSMIT DATA BUFFER (TBUFFER) | | | | | | | |
| Status | 0F | RLSD | FED | CTS | DSR | RI | TM | SYNCD | FLAGS |
| | 0E | RTDET | BRKD | PE | FE | OE | SPEED | | |
| | 0D | — | PNDET | S1DET | SCR1 | U1DET | SADET | — | — |
| | 0C | EDET | — | — | — | DTDIG | | | |
| | 0B | TONEA | TONEB | TONEC | ATV25 | ATBELL | PNSUC | DTDET | BEL103 |
| | 0A | — | — | — | — | — | — | — | CRCS |
| Control | 09 | NV25 | CC | DTMF | ORG | LL | DATA | — | SLEEP |
| | 08 | ASYNC | TPDM | — | DDIS | TRFZ | — | RTRN | RTS |
| | 07 | RDLE | RDL | L2ACT | — | L3ACT | RB | RA | ABORT |
| | 06 | BRKS | EXOS | PARSL | | PEN | STB | WDSZ | |
| | 05 | — | — | — | TXSQ | CEQ | RCEQ | TXVOC | — |
| | 04 | EQRES | SWRES | — | — | EQFZ | IFIX | AGCFZ | CRFZ |
| | 03 | — | HDLC | SPLIT | — | ARC | SDIS | GTE | — |
| | 02 | — | — | — | — | — | — | — | — |
| Receive Data Buffer | 01 | — | — | — | — | — | — | — | RXP |
| | 00 | RECEIVE DATA BUFFER (RBUFFER) | | | | | | | |

NOTE: — In the "Bit" columns indicates reserved for modem use only.

**Figure 4. Interface Memory Map**

**Table 10. Interface Memory Bit Functions**

| Mnemonic | Memory Location | Name/Description |
|---|---|---|
| ABORT | 07:0 | **HDLC Abort.** Controls sending of continuous mark in HDLC mode. |
| AGCFZ. | 04:1 | **AGC Freeze.** Inhibits updating of the receiver AGC. |
| ARC | 03:3 | **Automatic Rate Change Enable.** Enables automatic on-line rate change sequence. |
| ASYNC | 08:7 | **Asynchronous/Synchronous.** Selects asynchronous or synchronous data mode. |
| ATBELL | 0B:3 | **Bell Answer Tone Detected.** Reports detection status of 2225 Hz answer tone. |
| ATV25 | 0B:4 | **V25 Answer Tone Detected.** Reports detection status of 2100 Hz answer tone. |
| BEL103 | 0B:0 | **Bell 103 Mark Frequency Detected.** Reports detection status of 1270 Hz Bell 103 mark. |
| BRKD | 0E:6 | **Break Detected.** Reports receipt status of continuous space. |
| BRKS | 06:7 | **Break Sequence.** Controls sending of continuous space in parallel asynchronous mode. |
| CC | 09:6 | **Controlled Carrier.** Selects controlled or constant carrier mode. |
| CEQ | 05:3 | **Compromise Equalizer Enable.** Enables the transmit passband digital compromise equalizer. |
| CONF | 12:0-7 | **Modem Configuration Select.** Selects the modem operating mode. |
| CRCS | 0A:0 | **CRC Sending.** Reports the sending status of the CRC (2 bytes) in HDLC mode. |
| CRFZ | 04:0 | **Carrier Recovery Freeze.** Disables update of the receiver's carrier recovery phase lock loop. |
| CTS | 0F:5 | **Clear to Send.** Reports that the training sequence has been completed (see TPDM). |
| DATA | 09:2 | **Data Mode.** Selects idle or data mode. |
| DDIS | 08:4 | **Descrambler Disable.** Disables the receiver's descrambler circuit. |
| DSR | 0F:4 | **Data Set Ready.** Reports the data transfer state. |
| DTDET | 0B:1 | **DTMF Digit Detected.** Reports that a valid DTFM digit has been detected. |
| DTDIG | 0C:0-3 | **Detected DTMF Digit.** Contains the hexadecimal code of the detected DTMF digit. |
| DTMF | 09:5 | **DTMF Dial Select.** Selects either DTMF or pulse dialing in the dial mode. |
| EDET | 0C:7 | **Early DTMF Detect.** Reports detection of the high group frequency of the DTMF tone pair. |
| EQFZ | 04:3 | **Equalizer Freeze.** Inhibits the update of the receiver's adaptive equalizer taps. |
| EQRES | 04:7 | **Equalizer Reset.** Resets the receiver adaptive equalizer taps to zero. |
| EXOS | 06:6 | **Extended Overspeed.** Selects extended overspeed mode in asynchronous mode. |
| FE | 0E:4 | **Framing Error.** Reports framing error detection or detection of an ABORT sequence. |
| FED | 0F:6 | **Fast Energy Detected.** Reports energy above the turn-on threshold is being detected. |
| FLAGS | 0F:0 | **Flag Sequence.** Reports transmission status of the Flag sequence in HDLC mode, or transmission of a constant mark in parallel asynchronous mode. |
| GTE | 03:1 | **Guard Tone Enable.** Enables transmission of the 1800 Hz guard tone (CCITT configuration only). |
| HDLC | 03:6 | **High Level Data Link Control.** Enables HDLC protocol support in parallel data mode. |
| IFIX | 04:2 | **Eye Fix.** Forces EYEX and EYEY serial data to be rotated equalizer output. |
| IOX | 1D:3 | **I/O Register Select.** Specifies that the X RAM ADDRESS (XADD) is an internal I/O register address. |
| L2ACT | 07:5 | **Loop 2 (Local Digital Loopback) Activate.** Selects connection of the receiver's digital output internally to the transmitter's digital input (locally activated digital loopback). |
| L3ACT | 07:3 | **Loop 3 (Local Analog Loopback) Activate.** Selects connection of the transmitter's analog output internally to the receiver's analog input (local analog loopback). |
| LL | 09:3 | **Leased Line.** Selects leased line data mode or handshake mode. |
| NCIA | 1F:6 | **NEWC Interrupt Active.** Reports that the cause of an interrupt request was completion of a configuration change. (See NEWC and NCIE.) |
| NCIE | 1F:2 | **NEWC Interrupt Enable.** Enables the assertion of $\overline{IRQ}$ and the setting of the NCIA bit. |
| NEWC | 1F:0 | **New Configuration.** Initiates a new configuration; cleared by the modem upon completion of configuration change. This bit can cause $\overline{IRQ}$ to be asserted. (See NCIE and NCIA.) |
| NEWS | 1F:3 | **New Status.** Reports the detection of a change in selected status bits. This bit can cause $\overline{IRQ}$ to be asserted. (See NSIE and NSIA.) |

Table 10. Interface Memory Bit Functions (Cont'd)

| Mnemonic | Memory Location | Name/Description |
|---|---|---|
| NSIA | 1F:7 | **NEWS Interrupt Active.** Reports that the cause of an interrupt request was a status bit change. (See NEWS and NSIE.) |
| NSIE | 1F:4 | **NEWS Interrupt Enable**. Enables the assertion of $\overline{IRQ}$ and the setting of the NSIA bit. (See NEWS.) |
| NV25 | 09:7 | **Disable V.25 Answer Sequence (Data Modes), Disable Echo Suppressor Tone (Fax Modes).** Disables the transmitting of the 2100 Hz CCITT answer tone when a handshake sequence is initiated in a data mode or disables sending of the echo suppressor tone in a fax mode. |
| OE | 0E:3 | **Overrun Error.** Reports overrun status of the Receiver Data Buffer (RBUFFER). |
| ORG | 09:4 | **Originate.** Selects originate or answer mode. |
| PE | 0E:5 | **Parity Error.** Reports parity error status or bad CRC |
| PNSUC | 0B:2 | **PN Success.** Indicates that the receiver has detected the PN portion of the training sequence. |
| RA | 07:1 | **Relay A Activate.** Activates the $\overline{RADRV}$ output. |
| PARSL | 06:4,5 | **Parity Select.** Selects stuff, space, even, or odd parity in the asynchronous parallel data mode. |
| RB | 07:2 | **Relay B Activate.** Activates the $\overline{RBDVR}$ output. |
| RBUFFER | 00:0-7 | **Receive Data Buffer.** Contains the received byte of data. |
| RDBF | 1E:0 | **Receiver Data Buffer Full.** Reports the status (full or not full) of the Receiver Data Buffer (RBUFFER). (See RDBIE and RDBIA.) |
| RDBIA | 1E:6 | **Receiver Data Buffer Interrupt Active.** Reports that the cause of an interrupt request is the Receiver Data Buffer (RBUFFER) full. (See RDBF and RDBIE.) |
| RDBIE | 1E:2 | **Receiver Data Buffer Interrupt Enable.** Enables the assertion of $\overline{IRQ}$ and the setting of the RDBIA bit when RBUFFER is full. (See RDBF and RDBIA.) |
| RDL | 07:6 | **Remote Digital Loopback Request.** Initiates a request for the remote modem to go into digital loopback. |
| RDLE | 07:7 | **Remote Digital Loopback Response Enable.** Enables the modem to respond to the remote modem's digital loopback request. |
| PEN | 06:3 | **Parity Enable.** Enables generation/checking of parity in asynchronous parallel data mode. |
| RCEQ | 05:2 | **Receiver Compromise Equalizer Enable.** Controls insertion of the receive passband digital compromise equalizer into the receive path. |
| RI | 0F:3 | **Ring Indicator.** Reports detection status of a valid ringing signal. |
| RTDET | 0E:7 | **Retrain Detected.** Reports detection status of a retrain request sequence. |
| RTRN | 08:1 | **Retrain.** Controls sending of the retrain request or automatic rate change to the remote modem. |
| RTS | 08:0 | **Request to Send.** Requests the transmitter to send data. |
| RLSD | 0F:7 | **Received Line Signal Detector.** Reports detection status of the carrier and the receipt of valid data. |
| RXP | 01:0 | **Received Parity bit.** This bit is the received parity bit (or ninth data bit). |
| S1DET | 0D:5 | **S1 Sequence Detected**. Reports detection status of the S1 sequence. |
| SADET | 0D:2 | **Scrambled Alternating Ones Sequence Detected.** Reports detection status of the Scrambled Alternating Ones sequence. |
| SCR1 | 0D:4 | **Scrambled Ones Sequence Detected.** Reports detection status of Scrambled Ones sequence. |
| SDIS | 03:2 | **Scrambler Disable.** Disables the transmitter scrambler. |
| SLEEP | 09:0 | **Sleep Mode.** Controls entry into the SLEEP mode. The modem requires a pulse on the $\overline{RESET}$ pin to return to normal operation. |
| SPEED | 0E:0-2 | **Speed Indication.** Reports the data rate at the completion of a connection. |
| SPLIT | 03:5 | **Extended Overspeed TX/RX Split.** Limits transmit data to the basic overspeed rate. |
| STB | 06:2 | **Stop Bit Number.** Selects the number of stop bits in asynchronous mode. |
| SWRES | 04:6 | **Software Reset.** Causes the modem to reinitialize to its power turn-on state. |
| TBUFFER | 10:0-7 | **Transmitter Data Buffer.** Contains the byte to be transmitted in the parallel mode. |
| TDBE | 1E:3 | **Transmitter Data Buffer Empty.** Reports the status (empty or not empty) of the Transmit Data Buffer (TBUFFER). (See TDBIE and TDBIA.) |

**Table 10. Interface Memory Bit Functions (Cont'd)**

| Mnemonic | Memory Location | Name/Description |
|---|---|---|
| TDBIA | 1E:7 | **Transmitter Data Buffer Interrupt Active.** Reports that the cause of an interrupt request is the Transmit Data Buffer (TBUFFER) empty. (See TDBE and TDBIE.) |
| TDBIE | 1E:5 | **Transmitter Data Buffer Interrupt Enable.** Enables assertion of $\overline{IRQ}$ and the setting of the TDBIA bit when the TBUFFER is empty. (See TDBE and TDBIA.) |
| TLVL | 13:4-7 | **Transmit Level Attenuation Select.** Selects the transmitter analog output level attenuation in 1 dB steps. The host can fine tune the transmit level to a value lying within a 1 dB step in DSP RAM. |
| TM | 0F:2 | **Test Mode.** Reports active status of the selected test mode. |
| TONEA | 0B:7 | **Tone Filter A Energy Detected.** Reports status of energy above the threshold detection by the Call Progress Monitor filter in the Dial Configuration or 1300 Hz FSK tone energy detection by the Tone A bandpass filter in the Tone Detector configuration. |
| TONEB | 0B:6 | **Tone Filter B Energy Detected.** Reports status of 390 Hz FSK tone energy detection by the Tone B bandpass filter in the Tone Detector configuration. |
| TONEC | 0B:5 | **Tone Filter C Energy Detected.** Reports status of 1650 Hz or 980 Hz (selected by the ORG bit) FSK tone energy detection by the Tone C bandpass filter in the Tone Detector configuration. |
| TPDM | 08:6 | **Transmitter Parallel Data Mode.** Selects transmitter parallel or serial mode. |
| TRFZ | 08:3 | **Timing Recovery Freeze.** Inhibits the update of the receiver's timing recovery algorithm. |
| TXCLK | 13:0,1 | **Transmit Clock Select.** Selects the transmitter data clock (internal, disable, slave, or external). |
| TXP | 11:0 | **Transmit Parity Bit (or 9th Data Bit).** This bit is the stuffed parity bit (or ninth data bit) for transmission. |
| TXSQ | 05:4 | **Transmitter Squelch.** Disables transmission of energy. |
| TXVOC | 05:1 | **Transmit Voice.** Enables the sending of voice samples. |
| U1DET | 0D:3 | **Unscrambled Ones Detected.** Reports detection status of the Unscrambled Ones sequence. |
| WDSZ | 06:0,1 | **Data Word Size.** Selects the number of data bits per character in asynchronous mode (5, 6, 7, or 8). |
| VOL | 13:2-3 | **Volume Control.** Two-bit encoded speaker volume selects volume off or one of three volume on levels. |
| XACC | 1D:7 | **X RAM Access Enable.** Controls DSP access of the X RAM associated with the address in XADD and the XCR bit. XWT determines if a read or write is performed. |
| XADD | 1C:0-7 | **X RAM Address.** Contains the X RAM address used to access the DSP's X Data RAM or X Coefficient RAM (selected by XCR) via the X RAM Data LSB and MSB registers). (See Table 11.) |
| XCR | 1D:0 | **X Coefficient RAM Select.** Controls XADD access to the DSP's X Coefficient RAM or the X Data RAM. |
| XCRD | 1D:2 | **X RAM Continuous Read.** Enables read of X RAM every sample from the location addressed by XADD independent of the XACC and XWT bits. |
| XDAL | 18:0-7 | **X RAM Data LSB.** The least significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in the DSP. |
| XDAM | 19:0-7 | **X RAM Data MSB.** The most significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in the DSP. |
| XWT | 1D:1 | **X RAM Write.** Controls the reading of data from, or the writing of data to, the X RAM Data registers (18 and 19) using the X RAM location addressed by XADD and XCR. |
| YACC | 1B:7 | **Y RAM Access Enable.** Controls DSP access of the Y RAM associated with the address in YADD and the YCR bit. YWT determines if a read or write is performed. |
| YADD | 1A:0-7 | **Y RAM Address.** Contains the Y RAM address used to access the DSP's Y Data RAM or Y Coefficient RAM (selected by YCR) via the Y RAM Data LSB and MSB registers. (See Table 11.) |
| YCR | 1B:0 | **Y Coefficient RAM Select.** Controls YADD access to the DSP's Y Coefficient RAM or the Y Data RAM. |
| YCRD | 1B:2 | **Y RAM Continuous Read.** Enables read of Y RAM every sample from the location addressed by YADD independent of the YACC and YWT bits. |
| YDAL | 16:0-7 | **Y RAM Data LSB.** The least significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in the DSP. |
| YDAM | 17:0-7 | **Y RAM Data MSB.** The most significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in the DSP. |
| YWT | 1B:1 | **Y RAM Write.** Controls the reading of data from, or the writing of data to, the Y RAM Data registers (16 and 17) using the Y RAM location addressed by YADD and YCR. |

### DSP RAM ACCESS

The DSP contains four sections of 16-bit wide random access memory (RAM). Because the DSP is optimized for performing complex arithmetic, the RAM is organized into real (X RAM) and imaginary (Y RAM) sections, as well as data and coefficient sections. The host processor can access (read or write) the X RAM only, the Y RAM only, or both the X RAM and the Y RAM simultaneously in either the data or coefficient section.

### INTERFACE MEMORY ACCESS TO DSP RAM

The DSP interface memory acts as an intermediary during host to DSP RAM or DSP RAM to host data exchanges. The addresses stored in modem interface memory RAM Address registers (i. e., XADD and YADD) by the host, in conjunction with the data or coefficient RAM bits (i. e., XCR and YCR) determine the DSP RAM addresses for data access.

### HOST PROGRAMMABLE DATA

The parameters available in DSP RAM are listed in Table 11 along with the X RAM or Y RAM address and corresponding XCR or YCR bit value. The scaling for the host programmable data is described in the RC9623DP and RC9624DP Modem Designer's Guide.

## MODEM INTERFACE CIRCUIT

The recommended modem interface circuit is shown in Figure 5.

**Table 11. DSP RAM Parameters**

| No. | XCR/ YCR* | X RAM Addr | Y RAM Addr | Parameter |
|---|---|---|---|---|
| 1 | 1 | 0-1E | | Adaptive Equalizer Coefficients, Real |
| | 1 | 0 | – | First Coefficient, Real (1) (Data/ Fax) |
| | 1 | 10 | – | Last Coefficient, Real (17) (Data) |
| | 1 | 1E | – | Last Coefficient, Real (31) (Fax) |
| 2 | 1 | | 0-1E | Adaptive Equalizer Coefficients, Imag. |
| | 1 | – | 0 | First Coefficient, Imag. (1) (Data/ Fax) |
| | 1 | – | 10 | Last Coefficient, Imag. (17) (Data) |
| | 1 | – | 1E | Last Coefficient, Imag. (31) (Fax) |
| 3 | 0 | 49 | – | Rotated Error, Real |
| 4 | 0 | – | 49 | Rotated Error, Imaginary |
| 5 | 0 | 3F | – | Max AGC Gain Word |
| 6 | 0 | 71 | – | Pulse Dial Interdigit Time |
| 7 | 0 | 7C | – | Tone Dial Interdigit Time |
| 8 | 0 | 72 | – | Pulse Dial Relay Make Time |
| 9 | 0 | 7D | – | Pulse Dial Relay Break Time |
| 10 | 0 | 7E | – | DTMF Duration |
| 11 | 0 | 6C | – | Tone 1 Angle Increment Per Sample (TXDPHI1) |
| 12 | 0 | 6D | – | Tone 2 Angle Increment Per Sample (TXDPHI2) |
| 13 | 0 | 6E | – | Tone 1 Amplitude (TXAMP1) |
| 14 | 0 | 6F | – | Tone 2 Amplitude (TXAMP2) |
| 15 | 0 | 73 | – | Max Samples Per Ring Frequency Period (RDMAXP) |
| 16 | 0 | 74 | – | Min Samples Per Ring Frequency Period (RDMINP) |
| 17 | 0 | 5E | – | Real Part of Error |
| 18 | 0 | – | 5E | Imaginary Part of Error |
| 19 | 0 | – | 3D | Rotation Angle for Carrier Recovery |
| 20 | 0 | 59 | – | Rotated Equalizer Output, Real |
| 21 | 0 | – | 59 | Rotated Equalizer Output, Imaginary |
| 22 | 0 | 3C | – | Lower Part of Phase Error |
| 23 | 0 | – | 3C | Upper Part of Phase Error |
| 24 | 1 | 3F | – | Upper Part of AGC Gain Word |
| 25 | 1 | 3E | – | Lower Part of AGC Gain Word |
| 26 | 1 | 2E | – | Average Power |
| 27 | 1 | 2D | – | Phase Error |
| 28 | 1 | 2F | – | Tone Power (TONEA) |
| 29 | 1 | 30 | – | Tone Power (ATBELL, BEL103, or TONEB) |

**Table 11. DSP RAM Parameters (Cont'd)**

| No. | XCR/ YCR* | X RAM Addr | Y RAM Addr | Parameter |
|---|---|---|---|---|
| 30 | 1 | 31 | – | Tone Power (TONEC, ATV25)[a] |
| 31 | 1 | 36 | – | Tone Detect Thresholdfor TONEA (THDA) |
| 32 | 1 | 37 | – | Tone Detect Threshold for ATBELL, BEL103, or TONEB (THDB) |
| 33 | 1 | 38 | – | Tone Detect Threshold for TONEC or ATV25 (THDC) |
| 34 | 1 | – | 6C | Biquad 1 Coefficient $\alpha 0$ |
| | 1 | – | 6D | Biquad 1 Coefficient $\alpha 1$ |
| | 1 | – | 6E | Biquad 1 Coefficient $\alpha 2$ |
| | 1 | – | 6F | Biquad 1 Coefficient $\beta 1$ |
| | 1 | – | 70 | Biquad 1 Coefficient $\beta 2$ |
| | 1 | – | 71–75 | Biquad 2 Coefficients $\alpha 0 - \beta 2$ |
| | 1 | – | 76–7A | Biquad 3 Coefficients $\alpha 0 - \beta 2$ |
| | 1 | – | 7B–7F | Biquad 4 Coefficients $\alpha 0 - \beta 2$ |
| | 1 | – | 62–66 | Biquad 5 Coefficients $\alpha 0 - \beta 2$ |
| | 1 | – | 67–6B | Biquad 6 Coefficients $\alpha 0 - \beta 2$ |
| 35 | 0 | 32 | – | Turn-on Threshold |
| 36 | 1 | 79 | – | Turn-off Threshold |
| 37 | 1 | – | 21 | RLSD Turn-off Time |
| 38 | 0 | 70 | – | Transmit Level Output Attenuation |
| 39 | 1 | 52 | – | Eye Quality Monitor (EQM) |

* XCR if an XRAM address is listed; YCR if a YRAM address is listed.

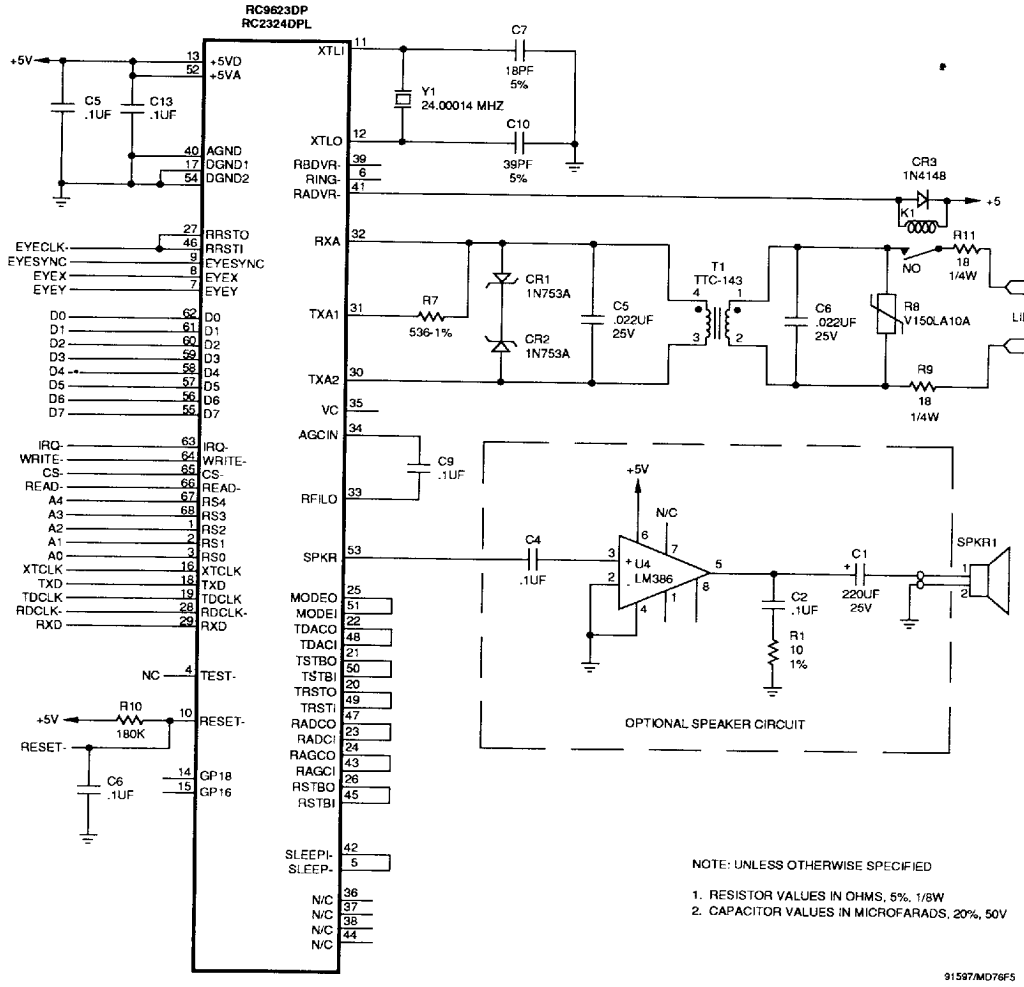


**Figure 5. Typical Modem Interface Circuit**