Device Description

The RD5108A is a 1024 sample bucket brigade device. It is pin-compatible with and similar to the RD5106A, but with four times the delay. The device contains internal clock drivers that can accept a TTL (or higher-level) single-phase input clock (f_C). Internal sample-and-hold provides a smooth stair step output over each sample period in normal operation. This device is manufactured using N-channel silicon-gate technology to fabricate a chain of MOS transistors and storage capacitors into a bucket-brigade charge-transfer device. The pinout configuration is shown in Figure 1, the functional equivalent circuit is shown in Figure 2, and the package dimensions are shown in Figure 9.

Key Features

- 1024 samples of delay
- On-chip driver requiring only single TTL-level clock input
- Clock-controlled delay: 2 msec to more than 4 sec
- N-channel silicon-gate bucket-brigade technology
- Sample-and-hold output circuit for maximum self-cancellation of clocking modulation
- Wide input signal frequency range: 0 to 170 kHz
- Wide clock frequency range: 500 Hz to 1 MHz
- Wide dynamic range: S/N >65 dB
- Low distortion: less than 1.2% (typical)
- Single power supply (7V to 13V range)
- 8-pin mini-DIP

Typical Applications

- Voice control of tape recorders
- Control of equalization filters
- Reverberation effects in stereo equipment
- Tremolo, vibrato, or chorus effects in electronic musical instruments
- Variable or fixed delay of analog signals
- Time compression of telephone conversations or other analog signals
- Voice scrambling systems
- Storage of multilevel digital signals

Drive and Voltage Considerations

The amplitude of the clock may be any positive pulse from +2V to V_{DD} and is best as a controlled rectangular pulse with rise and fall times less than 50 nsec. The positive duration of the clock should be greater than 200 nsec (preferably greater than 500 nsec) and the low-level duration not less than 300 nsec. When used, the sync input should be a positive pulse with amplitude $V_{DD}/2 < V_{SYNC} \leq V_{DD}$. This pulse should rise 100 nsec or later after a falling edge of the clock input, and fall at or before the next falling clock edge. Consult the waveform table in Figure 4. (If the sync input is not used, pin 7 should be connected to ground.)

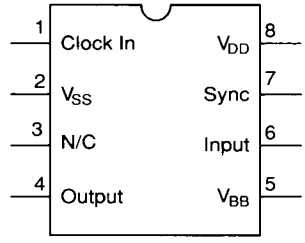

Figure 1. Pinout Configuration

Device Operation

For best performance, care should be given to layout and design as well as the filtering requirements. Ground planes are generally required on circuit boards to reduce crosstalk, and shielding of high-impedance circuits, such as the input circuit, is desirable.

It is very important to remember that the device is a sampled-data device, and as such has important requirements on filtering of the input and output signals and on the stability of the clock frequency.

The application equations for the RD5108A are as follows:

(1) The sampling frequency (f_S) is one-half the clock frequency: $f_S = f_C/2$

(2) The delay in seconds (d) is the number of samples in the delay line (N) divided by the sample frequency: $d = N/f_S$

(3) The delay line bandwidth (BW) is one-third of the sampling frequency: $BW = f_S/3$

Sampling waveforms, propagation delay, and internal dispersion limit f_C to 1 MHz ($f_{S(max)} = 500$ kHz). An example circuit is shown in Figure 3.

Signal inputs less than $1.0V_{rms}$ will have distortion of less than 1.2%. Figures 5 and 6 indicate performance considerations with respect to input level. Broadband dynamic range of better than 50 dB is available at moderate to high sample rates. However, dynamic ranges of greater than 65 dB may be obtained by using an A-weighting filter and a sample rate of at least 100 kHz. Signal input frequency too near the sampling frequency will generate modulation and other undesirable products. Limiting the input by low-pass filtering it to $f_S/3$ provides a "guard band" to permit adequate attenuation of those products.

The output is internally S/H, buffered by a source follower with load capability adequate to drive up to 200 pF with no further components. With 200 pF, the slew rate is approximately 0.5V/

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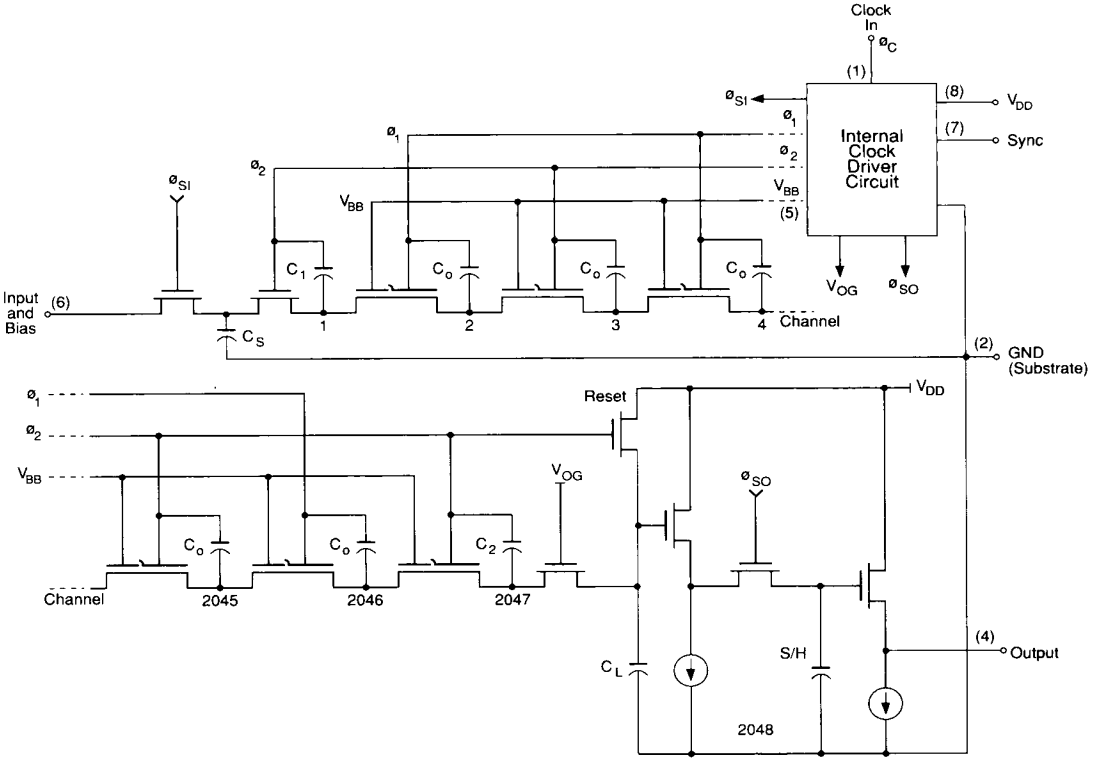

Figure 2. Equivalent Circuit

μsec and is inversely proportional to the capacitive load. AC-coupled loads are preferably 50KΩ or greater since the internal current driver is inadequate to drive a low AC-coupled resistance. Otherwise, an external buffer is recommended (Figure 8). Response attenuation relative to f_{in}/f_S (f_{in} is input signal frequency, f_S is sample frequency) is displayed in Figure 7. Note that, typically, there is less than 2 dB loss in the delay line itself.

Even after a sample-and-hold output, sampling steps (artifacts of the output sample-hold process) appear on the output waveform. The high state of the clock determines the duration of these sampling steps (see the S/H timing in Figure 4), whereas the low state of the clock controls the duration of the input track-and-hold process (see Figure 4 again). Making the positive clock state as short as possible (but not so short as to degrade the S/H output process) will minimize these steps. These sample-frequency steps can be further removed by a lowpass filter with a cutoff at approximately one quarter of the clock frequency ($f_C/4$) or less and a rolloff of not less than 36 dB/octave.

A sync input is included in the device and the waveform is shown in Figure 4. This input allows synchronized operation of multiple devices in either serial or parallel configuration when the same sync pulse is applied to each individual device. If the devices are used individually, the sync input (pin 7) should be grounded.

Evaluation Circuit, RC5106A

For evaluation, Reticon offers the RC5106A circuit card. This circuit provides variable sample frequencies to 200 kHz and utilizes a two-pole output filter with a cutoff frequency at 15 kHz. Antialiasing input filters should be externally provided to limit input bandwidth to less than $f_S/3$.

The bias should be set such that sine-wave signals large enough to show visible clipping are symmetrically clipped; the clipping should disappear as the signal level is reduced. A different device, or operation at different sample rates (particularly for changes between widely different sample rates) may require readjustment for optimum performance.

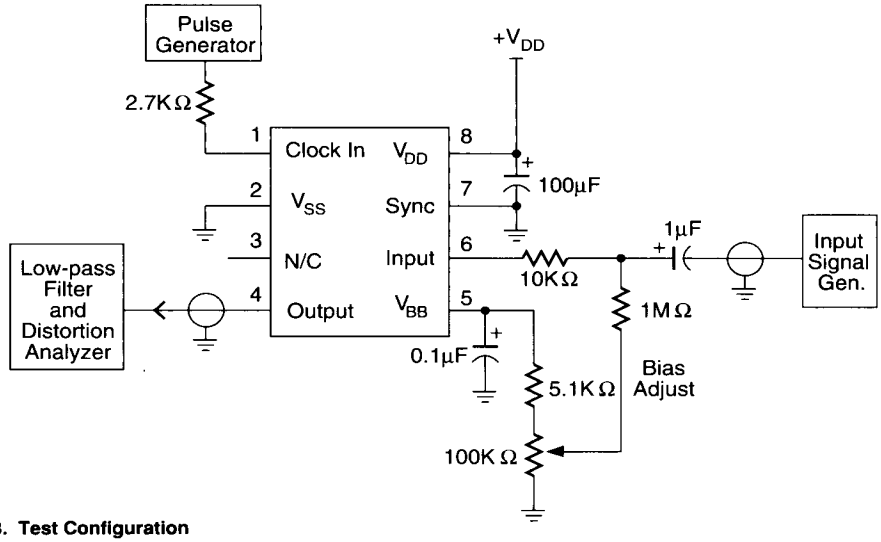

Figure 3. Test Configuration

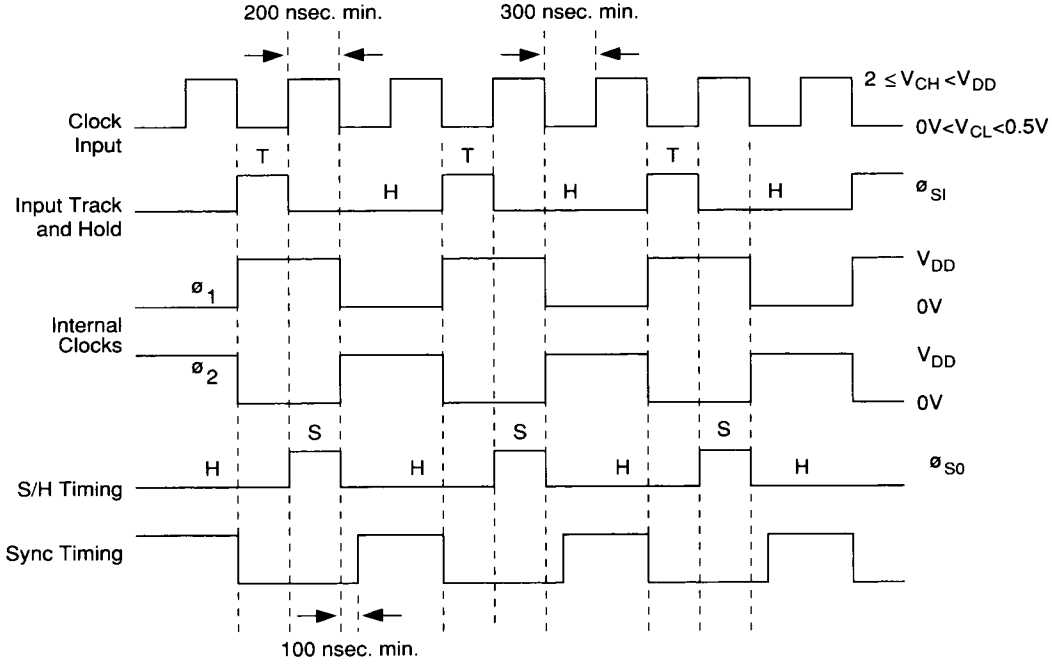

Figure 4. Timing Relations

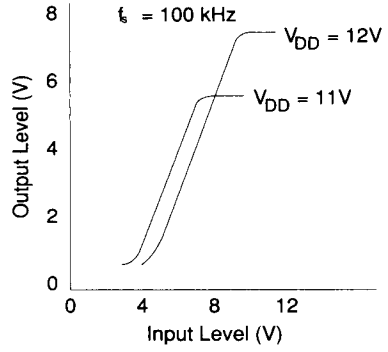

Figure 5. Typical DC Output vs. DC Input

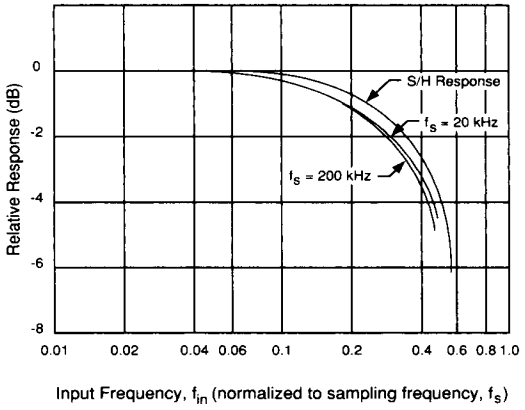

Figure 7. Typical Relative Responses vs. Input Frequency, f_{in}

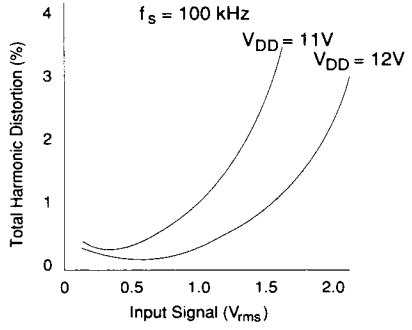

Figure 6. Typical Total Harmonic Distortion vs. Input Level

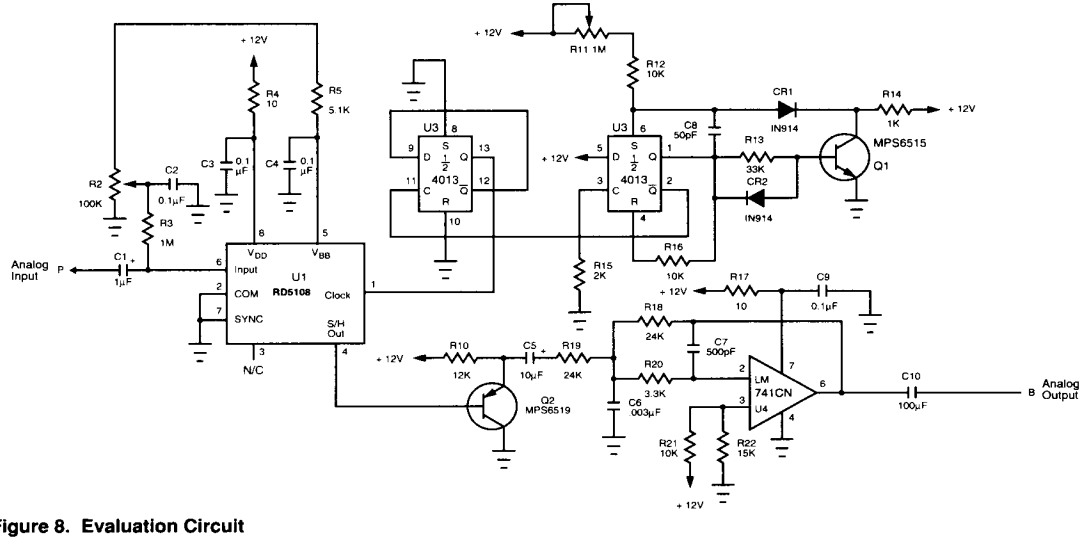

Figure 8. Evaluation Circuit

Table 1. Absolute Minimum/Maximum Ratings

	Min	Max	Units
Input voltage - any terminal with respect to substrate, pin 2 (V_{SS})	-0.4	21	V
Output short-circuit duration - any terminal	Indefinite		
Operating temperature	0	70	°C
Storage temperature	-55	125	°C
Lead temperature (soldering, 10 sec.)		300	°C

CAUTION: Observe MOS Handling and Operating Procedures

Note: This table shows stress ratings *exclusively*. Functional operation of this product under any conditions beyond those listed under standard operating conditions is not suggested by the table. Permanent damage may result if the device is subject to stresses beyond these absolute min/max values. Moreover, reliability may be diminished if the device is run for protracted periods at absolute maximum values.

Although devices are internally gate-protected to minimize the possibility of static damage, MOS handling precautions should be observed. Do not apply instantaneous supply voltages to the device or insert or remove device from socket while under power. Use decoupling networks to suppress power supply turn-off/ on switching transients and ripple. Applying AC signals or clock to device with power off may exceed negative limit.

Table 2. Device Characteristics and Operation Range Limits [4, 5]

Parameter	Conditions & Comments	Sym	Min	Typ	Max	Units
Supply voltage	Pin 8	V_{DD}	+7	+12	+13	V
Tetrode gate voltage [5]	Pin 5 (supplied internally)	V_{BB}	8.2	V_{DD}-2V		V
Substrate voltage	Pin 2	V_{SS}	GND	GND	GND	V
Clock frequency	$f_c = 2xf_s$	f_c	0.50	100-200	1000	kHz
Clock amplitude [1]		V_c	2	5	VDD	V
Clock pulse width		T_{cp}	200	$T_c/2$	T_c-300	nsec
Input signal bandwidth	3 dB point (Figure 7)				$f_s/3$	Hz
Input signal bias [3]	Initial estimate = 0.6 V_{DD}			7		V
Input signal amplitude [4]	(1.2% distortion)		1.0	1.5		V_{rms}
Sync pulse amplitude	Pin 7 (if required)	Sync	5		V_{DD}	V
Quiescent current [2]		I_Q			6	mA
Input capacitance		C_{in}			15	pF
Input shunt resistance	Measured @ f_s = 500 kHz	R_{in}	300			KΩ
Clock input capacitance		C_c		8	10	pF

Notes:
1 All voltages measured with respect to GND (Pin 2).
2 Increases 15% for operation to 0°C.
3 Voltage will vary with the amplitude of the clock.Voltage (and V_{DD}) may be adjusted for optimum linearity at maximum signal level. The value shown is nominal for 12V clocks.
4 With V_{DD} = 12V, f_s = 100 kHz, V_{in} = 1V_{rms} at 1 kHz.
5 T = 25°C

Table 3. Performance Characteristics [3]

Parameter	Conditions & Comments	Sym	Min	Typ	Max	Units
Gain RD5106A [1,2]			0	0.5	4	dB
Dynamic range		DR	50	60		dB
Total harmonic distortion [2]	Figure 6	THD			1.2	%
DC level (In-Out)	Figure 5					

Notes:
1 The value of gain depends on the output loading. Values given are for limited external loading.
2 With V_{DD} = 12V, f_s = 100 kHz, V_{in} = 1V_{rms} at 1 kHz.
3 T = 25°C

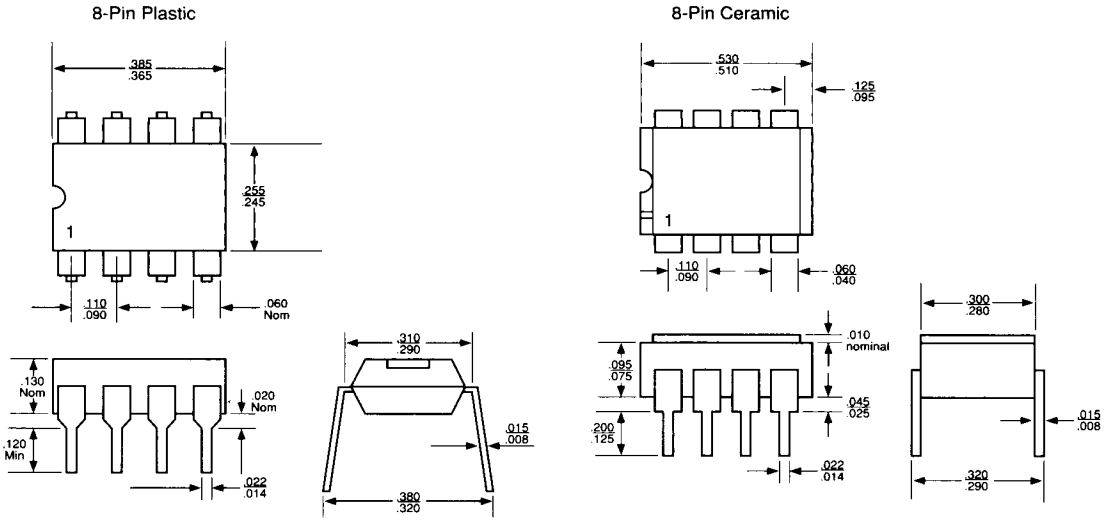

Figure 9. Package Dimensions

Ordering Information

Part Number	Description
RD5108ANP-011	1024-sample analog delay line, 8-pin plastic package