64K (8K x 8) High Speed CMOS E^2PROM

Features

- Fast Read Access Time - 55 ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 32 Bytes
  - Internal Control Timer
- Fast Write Cycle Times
  - Maximum Page Write Cycle Time: 2 ms
  - 1 to 32 Byte Page Write Operation
- Low Power Dissipation
  - 80 mA Active Current
  - 100 µA CMOS Standby Current (28HC64L)
- Direct Microprocessor Control
  - DATA Polling
- High Reliability CMOS Technology
  - Endurance: 10^4 or 10^5 Cycles
  - Data Retention: 10 years
- Single 5 V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout
- Full Military, Commercial, and Industrial Temperature Ranges

Description

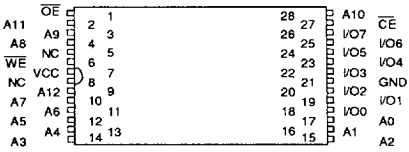
The AT28HC64/L is a high-speed, low-power Electrically Erasable and Programmable Read Only Memory. Its 64K of memory is organized as 8,192 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 55 ns with power dissipation of just 440mW. When the device is deselected the standby current is less than 100 µA.

The AT28HC64/L is accessed like a Static RAM for the read or write cycles without the need for external components. The device contains a 32-byte page register to allow writing of up to 32 bytes simultaneously. During a write cycle, the addresses and 1 to 32 bytes of data are

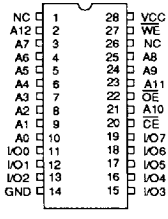
(continued on next page)

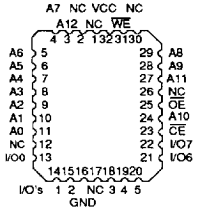
Pin Configurations

TSOP Top View



Pin Name	Function
A0 - A12	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect





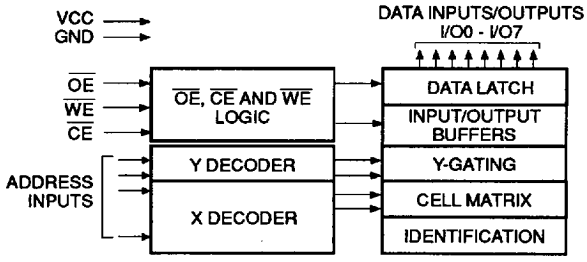
Note: PLCC package pins 1 and 17 are DON'T CONNECT.

Description (Continued)

internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{DATA}$ polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28HC64/L has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. The AT28HC64/L also includes an extra 32 bytes of E^2PROM for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6 V to +6.25 V
All Output Voltages with Respect to Ground	-0.6 V to V_{CC} +0.6 V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6 V to +13.5 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28HC64 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

BYTE WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion.

PAGE WRITE: The page write operation of the AT28HC64 allows one to thirty-two bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by one to thirty-one additional bytes. Each successive byte must be written within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded the AT28HC64 will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A5-A12 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A5 - A12 must be the same.

The A0 to A4 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28HC64 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{DATA}$ Polling may begin at anytime during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling the AT28HC64 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes to the AT28HC64 may occur during transitions of the host system power supply. Atmel has incorporated the following features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION: Hardware features protect against inadvertent writes to the AT28HC64 in the following ways: (a) V_{CC} sense - if V_{CC} is below 3.8 V (typical) the write function is inhibited; (b) V_{CC} power-on delay - once V_{CC} has reached 3.8 V the device will automatically time out 5 ms (typical) before allowing a write: (c) write inhibit - holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles; (d) noise filter - pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

CHIP CLEAR: The contents of the entire memory of the AT28HC64 may be set to the high state (erased) by the use of the CHIP CLEAR operation. By setting $\overline{CE}$ low and $\overline{OE}$ to 12 volts, the chip is cleared when a 10ms low pulse is applied to the $\overline{WE}$ pin.

DEVICE IDENTIFICATION: An extra 32 bytes of E^2PROM memory are available to the user for device identification. By raising A9 to 12 V ± 0.5 V and using address locations 1FE0H to 1FFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Note: 1. This parameter is characterized and is not 100% tested.

D.C. and A.C. Operating Range

		AT28HC64-55	AT28HC64L-70	AT28HC64-70	AT28HC64/L-90	AT28HC64/L-12
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.			-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%	5 V ± 10%	5 V ± 10%	5 V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H [3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. $V_H = 12.0\ V \pm 0.5\ V$.

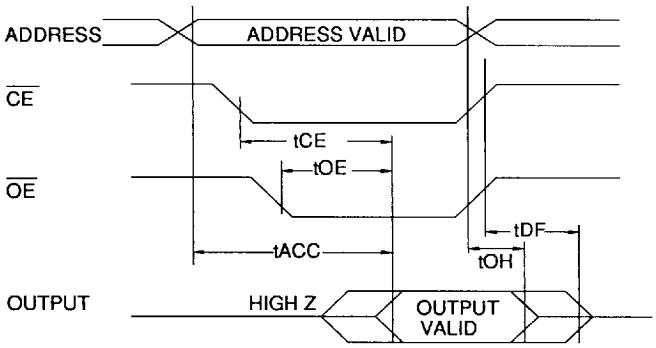
D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0 V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC}-0.3 V to V_{CC} + 1 V AT28HC64L	Com., Ind.		100	µA
			Mil.		200	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0 V to V_{CC} + 1 V	AT28HC64L		3	mA
			AT28HC64		60	mA
I_{CC}	V_{CC} Active Current	f = 10 MHz; I_{OUT} = 0 mA			80	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 4 mA			.4	V
V_{OH}	Output High Voltage	I_{OH} = -4.0 mA		2.4		V

A.C. Read Characteristics [1]

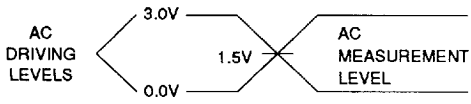
Symbol	Parameter	AT28HC64 -55		AT28HC64/L -70		AT28HC64/L -90		AT28HC64L -12		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		55		70		90		120	ns
t_{CE} [2]	$\overline{CE}$ to Output Delay		55		70		90		120	ns
t_{OE} [3]	$\overline{OE}$ to Output Delay	0	30	0	35	0	40	0	50	ns
t_{DF} [4,5]	$\overline{OE}$ to Output Float	0	30	0	35	0	40	0	50	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

A.C. Read Waveforms



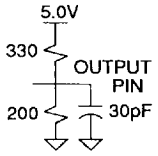
Notes:
1. C_L = 30 pF.
2. $\overline{CE}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
3. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
5. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

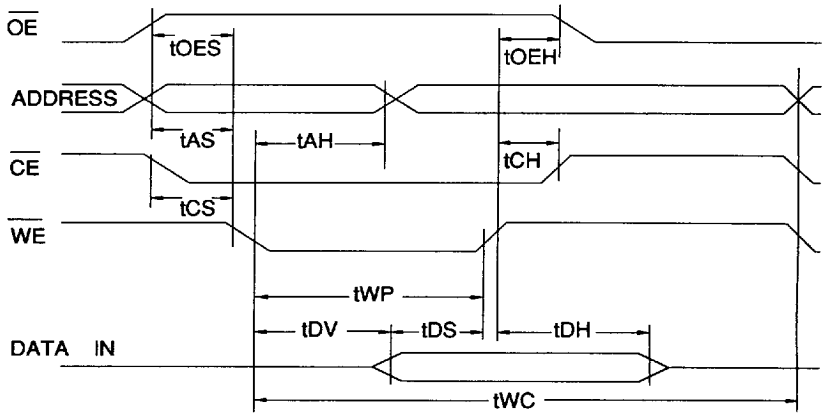
Output Test Load



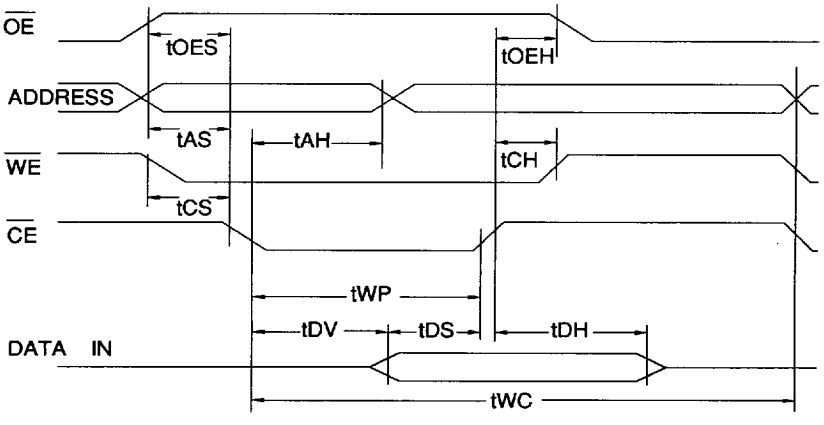
A.C. Write Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{CS}	Chip Select Set-up Time	0			ns
t_{CH}	Chip Select Hold Time	0			ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		1000	ns
t_{DS}	Data Set-up Time	50			ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	0			ns
t_{DV}	Time to Data Valid			1	µs
t_{WC}	Write Cycle Time		1.0	2.0	ms

A.C. Write Waveforms- $\overline{WE}$ Controlled



A.C. Write Waveforms- $\overline{CE}$ Controlled

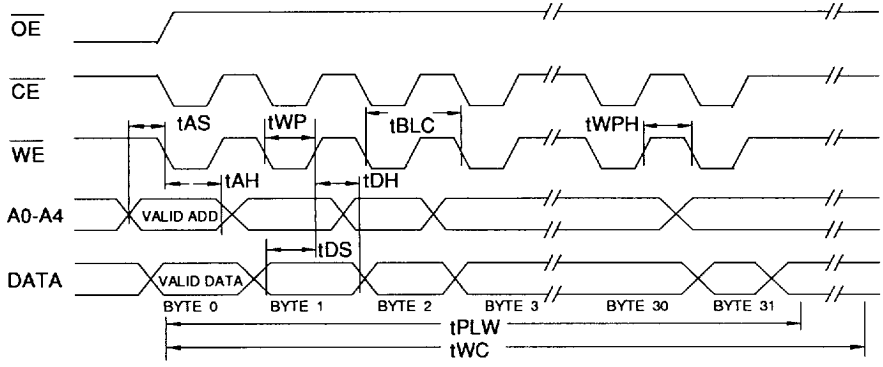


Page Mode Write Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{WC}	Write Cycle Time		1	2.0	ms
t_{AS}	Address Set-up Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{DS}	Data Set-up Time	50			ns
t_{DH}	Data Hold Time	0			ns
t_{WP}	Write Pulse Width	100		1000	ns
t_{BLC}	Byte Load Cycle Time	150			ns
t_{PLW}	Page Load Width			150	µs
t_{WPH}	Write Pulse Width High	50			ns

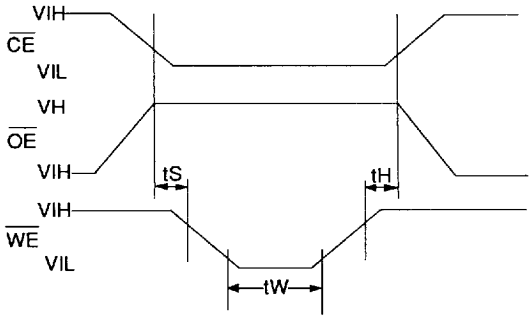
2

Page Mode Write Waveforms



Notes: A5 through A12 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Chip Erase Waveforms



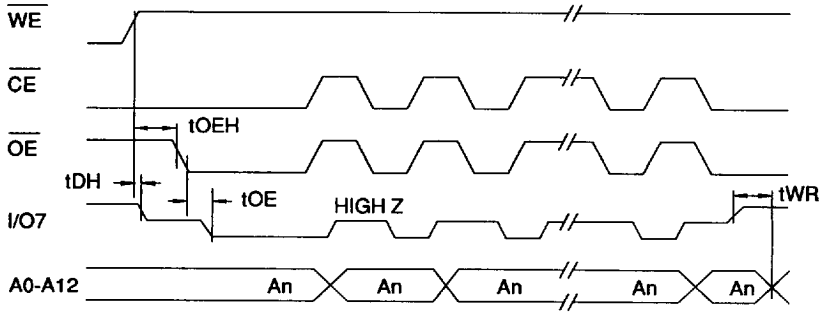
$t_S = t_H = 1$ µsec (min.)
$t_W = 10$ msec (min.)
$V_H = 12.0\ V \pm 0.5\ V$

$\overline{\text{Data}}$ Polling Characteristics[1]

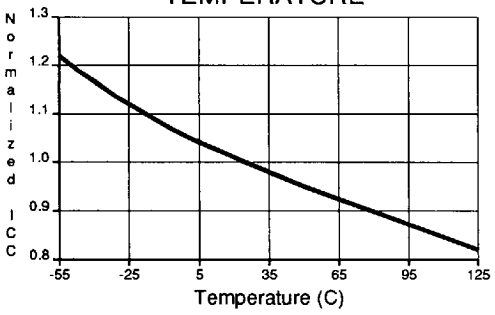
Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	0			ns
t_{OE}	$\overline{OE}$ to Output Delay			50	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

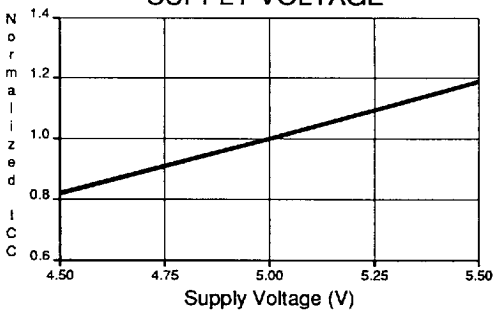
$\overline{\text{Data}}$ Polling Waveforms



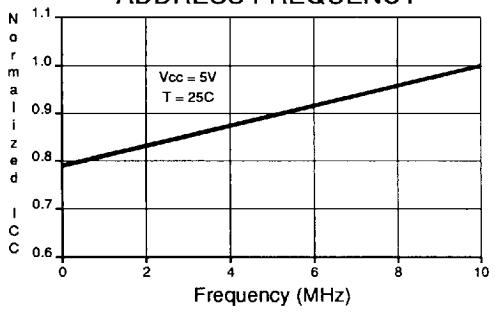
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
55	80	60	AT28HC64(E)-55DC AT28HC64(E)-55JC AT28HC64(E)-55PC	28D6 32J 28P6	Commercial (0°C to 70°C)
			AT28HC64(E)-55DI AT28HC64(E)-55JI AT28HC64(E)-55PI	28D6 32J 28P6	Industrial (-40°C to 85°C)
70	80	60	AT28HC64(E)-70DC AT28HC64(E)-70JC AT28HC64(E)-70PC	28D6 32J 28P6	Commercial (0°C to 70°C)
			AT28HC64(E)-70DI AT28HC64(E)-70JI AT28HC64(E)-70PI	28D6 32J 28P6	Industrial (-40°C to 85°C)
			AT28HC64(E)-70DM/883 AT28HC64(E)-70LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	80	60	AT28HC64(E)-90DC AT28HC64(E)-90JC AT28HC64(E)-90PC AT28HC64(E)-90TC	28D6 32J 28P6 28T	Commercial (0°C to 70°C)
			AT28HC64(E)-90DI AT28HC64(E)-90JI AT28HC64(E)-90PI AT28HC64(E)-90TI	28D6 32J 28P6 28T	Industrial (-40°C to 85°C)
			AT28HC64(E)-90DM/883 AT28HC64(E)-90LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	80	60	AT28HC64(E)-12DC AT28HC64(E)-12JC AT28HC64(E)-12PC	28D6 32J 28P6	Commercial (0°C to 70°C)
			AT28HC64(E)-12DI AT28HC64(E)-12JI AT28HC64(E)-12PI	28D6 32J 28P6	Industrial (-40°C to 85°C)
			AT28HC64(E)-12DM/883 AT28HC64(E)-12LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28T	28 Lead, Plastic Thin Small Outline Package (TSOP)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 2 ms
E	High Endurance Option: Endurance = 100K Write Cycles

Ordering Information

t_{ACC} (ns)	Icc (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	80	0.1	AT28HC64L(E)-70DC AT28HC64L(E)-70JC AT28HC64L(E)-70PC	28D6 32J 28P6	Commercial (0°C to 70°C)
			AT28HC64L(E)-70DI AT28HC64L(E)-70JI AT28HC64L(E)-70PI	28D6 32J 28P6	Industrial (-40°C to 85°C)
90	80	0.1	AT28HC64L(E)-90DC AT28HC64L(E)-90JC AT28HC64L(E)-90PC	28D6 32J 28P6	Commercial (0°C to 70°C)
			AT28HC64L(E)-90DI AT28HC64L(E)-90JI AT28HC64L(E)-90PI	28D6 32J 28P6	Industrial (-40°C to 85°C)
90	80	0.2	AT28HC64L(E)-90DM/883 AT28HC64L(E)-90LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	80	0.1	AT28HC64L(E)-12DC AT28HC64L(E)-12JC AT28HC64L(E)-12PC AT28HC64L-W	28D6 32J 28P6 DIE	Commercial (0°C to 70°C)
			AT28HC64L(E)-12DI AT28HC64L(E)-12JI AT28HC64L(E)-12PI	28D6 32J 28P6	Industrial (-40°C to 85°C)
120	80	0.2	AT28HC64L(E)-12DM/883 AT28HC64L(E)-12LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
70	80	0.2	5962-87514 12 XX 5962-87514 12 YX	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	80	0.2	5962-87514 11 XX 5962-87514 11 YX	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	80	0.2	5962-87514 10 XX 5962-87514 10 YX	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 2 ms
E	High Endurance Option: Endurance = 100K Write Cycles