# Virtex-E Extended Memory Electrical Characteristics

## Definition of Terms

Electrical and switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

**Advance**: These speed files are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

**Preliminary**: These speed files are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

**Production**: These speed files are released once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications. Contact the factory for design considerations requiring more detailed information.

Table 1 correlates the current status of each Virtex-E Extended Memory device with a corresponding speed file designation.

*Table 1:* **Virtex-E Extended Memory Device Speed Grade Designations**

| Device | Speed Grade Designations | | |
|---|---|---|---|
| | Advance | Preliminary | Production |
| XCV405E | | –8, –7, –6 | |
| XCV812E | | –8, –7, –6 | |

All specifications are subject to change without notice.

# DC Characteristics

## Absolute Maximum Ratings

| Symbol | Description(1) | | | Units |
|---|---|---|---|---|
| $V_{CCINT}$ | Internal Supply voltage relative to GND(2) | | –0.5 to 2.0 | V |
| $V_{CCO}$ | Supply voltage relative to GND | | –0.5 to 4.0 | V |
| $V_{REF}$ | Input Reference Voltage | | –0.5 to 4.0 | V |
| $V_{IN}$ | Input voltage relative to GND | | –0.5 to 4.0 | V |
| $V_{TS}$ | Voltage applied to 3-state output | | –0.5 to 4.0 | V |
| $V_{CC}$ | Longest Supply Voltage Rise Time from 0 V – 1.71 V | | 50 | ms |
| $T_{STG}$ | Storage temperature (ambient) | | –65 to +150 | °C |
| $T_J$ | Junction temperature(3) | Plastic packages | +125 | °C |

**Notes:**

1. Stresses beyond those listed under Absolute Maximum Ratings can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time can affect device reliability.
2. Xilinx recommends that all device power supplies ($V_{CCINT}$ , $V_{CCO}$) be powered up simultaneously. Other power supply sequence options might result in higher than typical power-up currents.
3. For soldering guidelines and thermal considerations, see the **Device Packaging** infomation on the Xilinx website.

## Recommended Operating Conditions

| Symbol | Description | | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Internal Supply voltage relative to GND, $T_J$ = 0 °C to +85°C | Commercial | 1.8 – 5% | 1.8 + 5% | V |
| | Internal Supply voltage relative to GND, $T_J$ = –40°C to +100°C | Industrial | 1.8 – 5% | 1.8 + 5% | V |
| $V_{CCO}$ | Supply voltage relative to GND, $T_J$ = 0 °C to +85°C | Commercial | 1.2 | 3.6 | V |
| | Supply voltage relative to GND, $T_J$ = –40°C to +100°C | Industrial | 1.2 | 3.6 | V |
| $T_{IN}$ | Input signal transition time | | | 250 | ns |

## DC Characteristics Over Recommended Operating Conditions

| Symbol | Description[1] | | Device | Min | Max | Units |
|---|---|---|---|---|---|---|
| $V_{DRINT}$ | Data Retention $V_{CCINT}$ Voltage (below which configuration data might be lost) | | All | 1.5 | | V |
| $V_{DRIO}$ | Data Retention $V_{CCO}$ Voltage (below which configuration data might be lost) | | All | 1.2 | | V |
| $I_{CCINTQ}$ | Quiescent $V_{CCINT}$ supply current[1] | | XCV405E | | 400 | mA |
| | | | XCV812E | | 500 | mA |
| $I_{CCOQ}$ | Quiescent $V_{CCO}$ supply current[1] | | XCV405E | | 2 | mA |
| | | | XCV812E | | 2 | mA |
| $I_L$ | Input or output leakage current | | All | –10 | +10 | µA |
| $C_{IN}$ | Input capacitance (sample tested) | BGA, PQ, HQ, packages | All | | 8 | pF |
| $I_{RPU}$ | Pad pull-up (when selected) @ $V_{in}$ = 0 V, $V_{CCO}$ = 3.3 V (sample tested) | | All | Note 2 | 0.25 | mA |
| $I_{RPD}$ | Pad pull-down (when selected) @ $V_{in}$ = 3.6 V (sample tested) | | | Note 2 | 0.25 | mA |

**Notes:**
1. With no output current loads, no active input pull-up resistors, all I/O pins 3-stated and floating.
2. Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits.

## Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device operation. The actual current consumed depends on the power-on ramp rate of the power supply. This is the time required to reach the nominal power supply voltage of the device[1] from 0 V. The fastest suggested ramp rate is 0 V to nominal voltage in 2 ms and the slowest allowed ramp rate is 0 V to nominal voltage in 50 ms.

| Product (Commercial Grade) | Description[2] | Current Requirement[3] |
|---|---|---|
| XCV50E - XCV600E | Minimum required current supply | 500 mA |
| XCV812E - XCV2000E | Minimum required current supply | 1 A |
| XCV2600E - XCV3200E | Minimum required current supply | 1.2 A |
| Virtex-E Family, Industrial Grade | Minimum required current supply | 2 A |

**Notes:**
1. Ramp rate used for this specification is from 0 - 1.8 V DC. Peak current occurs on or near the internal power-on reset threshold and lasts for less than 3 ms.
2. Devices are guaranteed to initialize properly with the minimum current available from the power supply as noted above.
3. Larger currents might result if ramp rates are forced to be faster.

## DC Input and Output Levels

Values for $V_{IL}$ and $V_{IH}$ are recommended input voltages. Values for $I_{OL}$ and $I_{OH}$ are guaranteed over the recommended operating conditions at the $V_{OL}$ and $V_{OH}$ test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum $V_{CCO}$ with the respective $V_{OL}$ and $V_{OH}$ voltage levels shown. Other standards are sample tested.

| Input/Output Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|
| | V, min | V, max | V, min | V, max | V, Max | V, Min | mA | mA |
| LVTTL(1) | – 0.5 | 0.8 | 2.0 | 3.6 | 0.4 | 2.4 | 24 | – 24 |
| LVCMOS2 | – 0.5 | 0.7 | 1.7 | 2.7 | 0.4 | 1.9 | 12 | – 12 |
| LVCMOS18 | – 0.5 | 20% $V_{CCO}$ | 70% $V_{CCO}$ | 1.95 | 0.4 | $V_{CCO}$ – 0.4 | 8 | – 8 |
| PCI, 3.3 V | – 0.5 | 30% $V_{CCO}$ | 50% $V_{CCO}$ | $V_{CCO}$ + 0.5 | 10% $V_{CCO}$ | 90% $V_{CCO}$ | Note 2 | Note 2 |
| GTL | – 0.5 | $V_{REF}$ – 0.05 | $V_{REF}$ + 0.05 | 3.6 | 0.4 | n/a | 40 | n/a |
| GTL+ | – 0.5 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 3.6 | 0.6 | n/a | 36 | n/a |
| HSTL I(3) | – 0.5 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 3.6 | 0.4 | $V_{CCO}$ – 0.4 | 8 | –8 |
| HSTL III | – 0.5 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 3.6 | 0.4 | $V_{CCO}$ – 0.4 | 24 | –8 |
| HSTL IV | – 0.5 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 3.6 | 0.4 | $V_{CCO}$ – 0.4 | 48 | –8 |
| SSTL3 I | – 0.5 | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 3.6 | $V_{REF}$ – 0.6 | $V_{REF}$ + 0.6 | 8 | –8 |
| SSTL3 II | – 0.5 | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 3.6 | $V_{REF}$ – 0.8 | $V_{REF}$ + 0.8 | 16 | –16 |
| SSTL2 I | – 0.5 | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 3.6 | $V_{REF}$ – 0.61 | $V_{REF}$ + 0.61 | 7.6 | –7.6 |
| SSTL2 II | – 0.5 | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 3.6 | $V_{REF}$ – 0.80 | $V_{REF}$ + 0.80 | 15.2 | –15.2 |
| CTT | – 0.5 | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 3.6 | $V_{REF}$ – 0.4 | $V_{REF}$ + 0.4 | 8 | –8 |
| AGP | – 0.5 | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 3.6 | 10% $V_{CCO}$ | 90% $V_{CCO}$ | Note 2 | Note 2 |

**Notes:**
1. $V_{OL}$ and $V_{OH}$ for lower drive currents are sample tested.
2. Tested according to the relevant specifications.
3. DC input and output levels for HSTL18 (HSTL I/O standard with $V_{CCO}$ of 1.8 V) are provided in an **HSTL white paper** on the Xilinx website.

## LVDS DC Specifications

| DC Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CCO}$ | | 2.375 | 2.5 | 2.625 | V |
| Output High Voltage for Q and $\overline{Q}$ | $V_{OH}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 1.25 | 1.425 | 1.6 | V |
| Output Low Voltage for Q and $\overline{Q}$ | $V_{OL}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 0.9 | 1.075 | 1.25 | V |
| Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High | $V_{ODIFF}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 250 | 350 | 450 | mV |
| Output Common-Mode Voltage | $V_{OCM}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 1.125 | 1.25 | 1.375 | V |
| Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High | $V_{IDIFF}$ | Common-mode input voltage = 1.25 V | 100 | 350 | NA | mV |
| Input Common-Mode Voltage | $V_{ICM}$ | Differential input voltage = ±350 mV | 0.2 | 1.25 | 2.2 | V |

**Notes:**
1. Refer to the Design Consideration section for termination schematics.

## LVPECL DC Specifications

These values are valid at the output of the source termination pack shown under LVPECL, with a 100 Ω differential load only. The $V_{OH}$ levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. The following table summarizes the DC output specifications of LVPECL.

| DC Parameter | Min | Max | Min | Max | Min | Max | Units |
|---|---|---|---|---|---|---|---|
| **$V_{CCO}$** | **3.0** | | **3.3** | | **3.6** | | **V** |
| $V_{OH}$ | 1.8 | 2.11 | 1.92 | 2.28 | 2.13 | 2.41 | V |
| $V_{OL}$ | 0.96 | 1.27 | 1.06 | 1.43 | 1.30 | 1.57 | V |
| $V_{IH}$ | 1.49 | 2.72 | 1.49 | 2.72 | 1.49 | 2.72 | V |
| $V_{IL}$ | 0.86 | 2.125 | 0.86 | 2.125 | 0.86 | 2.125 | V |
| **Differential Input Voltage** | 0.3 | - | 0.3 | - | 0.3 | - | V |

# Virtex-E Switching Characteristics

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation net list. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Virtex-E devices unless otherwise noted.

## IOB Input Switching Characteristics

Input delays associated with the pad are specified for LVTTL levels. For other standards, adjust the delays with the values shown in "IOB Input Switching Characteristics Standard Adjustments" on page 6.

| | | | Speed Grade[2] | | | | |
|---|---|---|---|---|---|---|---|
| **Description[1]** | **Symbol** | **Device** | **Min[3]** | **-8** | **-7** | **-6** | **Units** |
| **Propagation Delays** | | | | | | | |
| Pad to I output, no delay | $T_{IOPI}$ | All | 0.43 | 0.8 | 0.8 | 0.8 | ns, max |
| Pad to I output, with delay | $T_{IOPID}$ | XCV405E | 0.51 | 1.0 | 1.0 | 1.0 | ns, max |
| | | XCV812E | 0.55 | 1.1 | 1.1 | 1.1 | ns, max |
| **Propagation Delays** | | | | | | | |
| Pad to output IQ via transparent latch, no delay | $T_{IOPLI}$ | All | 0.75 | 1.4 | 1.5 | 1.6 | ns, max |
| Pad to output IQ via transparent latch, with delay | $T_{IOPLID}$ | XCV405E | 1.55 | 3.5 | 3.6 | 3.7 | ns, max |
| | | XCV812E | 1.55 | 3.5 | 3.6 | 3.7 | ns, max |
| Clock CLK to output IQ | $T_{IOCKIQ}$ | All | 0.18 | 0.4 | 0.7 | 0.7 | ns, max |
| **Setup and Hold Times with respect to Clock at IOB Input Register** | | | | | | | |
| Pad, no delay | $T_{IOPICK}$ / $T_{IOICKP}$ | All | 0.69 / 0 | 1.3 / 0 | 1.4 / 0 | 1.5 / 0 | ns, min |
| Pad, with delay | $T_{IOPICKD}$ / $T_{IOICKPD}$ | XCV405E | 1.49 / 0 | 3.4 / 0 | 3.5 / 0 | 3.5 / 0 | ns, min |
| | | XCV812E | 1.49 / 0 | 3.4 / 0 | 3.5 / 0 | 3.5 / 0 | ns, min |
| ICE input | $T_{IOICECK}$ / $T_{IOCKICE}$ | All | 0.28 / 0.0 | 0.55 / 0.01 | 0.7 / 0.01 | 0.7 / 0.01 | ns, min |
| SR input (IFF, synchronous) | $T_{IOSRCKI}$ | All | 0.38 | 0.8 | 0.9 | 1.0 | ns, min |
| **Set/Reset Delays** | | | | | | | |
| SR input to IQ (asynchronous) | $T_{IOSRIQ}$ | All | 0.54 | 1.1 | 1.2 | 1.4 | ns, max |
| GSR to output IQ | $T_{GSRQ}$ | All | 3.88 | 7.6 | 8.5 | 9.7 | ns, max |

**Notes:**

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. Input timing i for LVTTL is measured at 1.4 V. For other I/O standards, see Table 3.
3. The numbers for Min are **Advance** product specification numbers.

## IOB Input Switching Characteristics Standard Adjustments

| Description | Symbol | Standard | Speed Grade[1] | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min[2] | -8 | -7 | -6 | |
| **Data Input Delay Adjustments** | | | | | | | |
| Standard-specific data input delay adjustments | $T_{ILVTTL}$ | LVTTL | 0.0 | 0.0 | 0.0 | 0.0 | ns |
| | $T_{ILVCMOS2}$ | LVCMOS2 | –0.02 | 0.0 | 0.0 | 0.0 | ns |
| | $T_{ILVCMOS18}$ | LVCMOS18 | –0.02 | +0.20 | +0.20 | +0.20 | ns |
| | $T_{ILVDS}$ | LVDS | 0.00 | +0.15 | +0.15 | +0.15 | ns |
| | $T_{ILVPECL}$ | LVPECL | 0.00 | +0.15 | +0.15 | +0.15 | ns |
| | $T_{IPCI33\_3}$ | PCI, 33 MHz, 3.3 V | –0.05 | +0.08 | +0.08 | +0.08 | ns |
| | $T_{IPCI66\_3}$ | PCI, 66 MHz, 3.3 V | –0.05 | –0.11 | –0.11 | –0.11 | ns |
| | $T_{IGTL}$ | GTL | +0.10 | +0.14 | +0.14 | +0.14 | ns |
| | $T_{IGTLPLUS}$ | GTL+ | +0.06 | +0.14 | +0.14 | +0.14 | ns |
| | $T_{IHSTL}$ | HSTL | +0.02 | +0.04 | +0.04 | +0.04 | ns |
| | $T_{ISSTL2}$ | SSTL2 | –0.04 | +0.04 | +0.04 | +0.04 | ns |
| | $T_{ISSTL3}$ | SSTL3 | –0.02 | +0.04 | +0.04 | +0.04 | ns |
| | $T_{ICTT}$ | CTT | +0.01 | +0.10 | +0.10 | +0.10 | ns |
| | $T_{IAGP}$ | AGP | –0.03 | +0.04 | +0.04 | +0.04 | ns |

**Notes:**
1. Input timing i for LVTTL is measured at 1.4 V. For other I/O standards, see Table 3.
2. The numbers for Min are **Advance** product specification numbers.

I

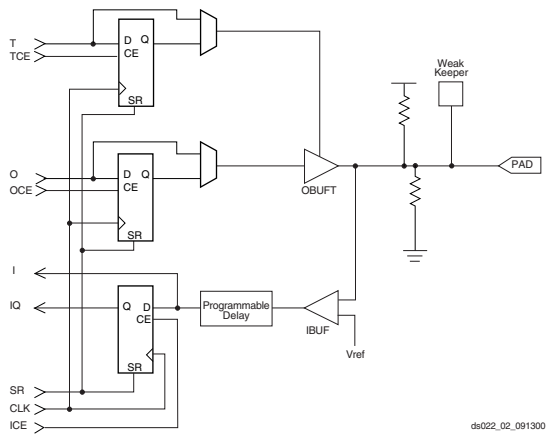



*Figure 1:* **Virtex-E Input/Output Block (IOB)**

## IOB Output Switching Characteristics, Figure 1

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in "IOB Output Switching Characteristics Standard Adjustments" on page 8..

| Description[1] | Symbol | Speed Grade[2] | | | | Units |
|---|---|---|---|---|---|---|
| | | Min[3] | -8 | -7 | -6 | |
| **Propagation Delays** | | | | | | |
| O input to Pad | $T_{IOOP}$ | 1.04 | 2.5 | 2.7 | 2.9 | ns, max |
| O input to Pad via transparent latch | $T_{IOOLP}$ | 1.24 | 2.9 | 3.1 | 3.4 | ns, max |
| **3-State Delays** | | | | | | |
| T input to Pad high-impedance (Note 2) | $T_{IOTHZ}$ | 0.73 | 1.5 | 1.7 | 1.9 | ns, max |
| T input to valid data on Pad | $T_{IOTON}$ | 1.13 | 2.7 | 2.9 | 3.1 | ns, max |
| T input to Pad high-impedance via transparent latch (Note 2) | $T_{IOTLPHZ}$ | 0.86 | 1.8 | 2.0 | 2.2 | ns, max |
| T input to valid data on Pad via transparent latch | $T_{IOTLPON}$ | 1.26 | 3.0 | 3.2 | 3.4 | ns, max |
| GTS to Pad high impedance (Note 2) | $T_{GTS}$ | 1.94 | 4.1 | 4.6 | 4.9 | ns, max |
| **Sequential Delays** | | | | | | |
| Clock CLK to Pad | $T_{IOCKP}$ | 0.97 | 2.4 | 2.8 | 2.9 | ns, max |
| Clock CLK to Pad high-impedance (synchronous) (Note 2) | $T_{IOCKHZ}$ | 0.77 | 1.6 | 2.0 | 2.2 | ns, max |
| Clock CLK to valid data on Pad (synchronous) | $T_{IOCKON}$ | 1.17 | 2.8 | 3.2 | 3.4 | ns, max |
| **Setup and Hold Times before/after Clock CLK** | | | | | | |
| O input | $T_{IOOCK}$ / $T_{IOCKO}$ | 0.43 / 0 | 0.9 / 0 | 1.0 / 0 | 1.1 / 0 | ns, min |
| OCE input | $T_{IOOCECK}$ / $T_{IOCKOCE}$ | 0.28 / 0 | 0.55 / 0.01 | 0.7 / 0 | 0.7 / 0 | ns, min |
| SR input (OFF) | $T_{IOSRCKO}$ / $T_{IOCKOSR}$ | 0.40 / 0 | 0.8 / 0 | 0.9 / 0 | 1.0 / 0 | ns, min |
| **3-State Setup Times, T input** | $T_{IOTCK}$ / $T_{IOCKT}$ | 0.26 / 0 | 0.51 / 0 | 0.6 / 0 | 0.7 / 0 | ns, min |
| **3-State Setup Times, TCE input** | $T_{IOTCECK}$ / $T_{IOCKTCE}$ | 0.30 / 0 | 0.6 / 0 | 0.7 / 0 | 0.8 / 0 | ns, min |
| **3-State Setup Times, SR input (TFF)** | $T_{IOSRCKT}$ / $T_{IOCKTSR}$ | 0.38 / 0 | 0.8 / 0 | 0.9 / 0 | 1.0 / 0 | ns, min |
| **Set/Reset Delays** | | | | | | |
| SR input to Pad (asynchronous) | $T_{IOSRP}$ | 1.30 | 3.1 | 3.3 | 3.5 | ns, max |
| SR input to Pad high-impedance (asynchronous) (Note 2) | $T_{IOSRHZ}$ | 1.08 | 2.2 | 2.4 | 2.7 | ns, max |
| SR input to valid data on Pad (asynchronous) | $T_{IOSRON}$ | 1.48 | 3.4 | 3.7 | 3.9 | ns, max |
| GSR to Pad | $T_{IOGSRQ}$ | 3.88 | 7.6 | 8.5 | 9.7 | ns, max |

**Notes:**

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. 3-state turn-off delays should not be adjusted.
3. The numbers for Min are **Advance** product specification numbers.

## IOB Output Switching Characteristics Standard Adjustments

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

| | | | Speed Grade | | | | |
|---|---|---|---|---|---|---|---|
| **Description** | **Symbol** | **Standard** | **Min[1]** | **-8** | **-7** | **-6** | **Units** |
| **Output Delay Adjustments** | | | | | | | |
| Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, Csl) | $T_{OLVTTL\_S2}$ | LVTTL, Slow, 2 mA | 4.2 | +14.7 | +14.7 | +14.7 | ns |
| | $T_{OLVTTL\_S4}$ | 4 mA | 2.5 | +7.5 | +7.5 | +7.5 | ns |
| | $T_{OLVTTL\_S6}$ | 6 mA | 1.8 | +4.8 | +4.8 | +4.8 | ns |
| | $T_{OLVTTL\_S8}$ | 8 mA | 1.2 | +3.0 | +3.0 | +3.0 | ns |
| | $T_{OLVTTL\_S12}$ | 12 mA | 1.0 | +1.9 | +1.9 | +1.9 | ns |
| | $T_{OLVTTL\_S16}$ | 16 mA | 0.9 | +1.7 | +1.7 | +1.7 | ns |
| | $T_{OLVTTL\_S24}$ | 24 mA | 0.8 | +1.3 | +1.3 | +1.3 | ns |
| | $T_{OLVTTL\_F2}$ | LVTTL, Fast, 2 mA | 1.9 | +13.1 | +13.1 | +13.1 | ns |
| | $T_{OLVTTL\_F4}$ | 4 mA | 0.7 | +5.3 | +5.3 | +5.3 | ns |
| | $T_{OLVTTL\_F6}$ | 6 mA | 0.20 | +3.1 | +3.1 | +3.1 | ns |
| | $T_{OLVTTL\_F8}$ | 8 mA | 0.10 | +1.0 | +1.0 | +1.0 | ns |
| | $T_{OLVTTL\_F12}$ | 12 mA | 0.0 | 0.0 | 0.0 | 0.0 | ns |
| | $T_{OLVTTL\_F16}$ | 16 mA | –0.10 | –0.05 | –0.05 | –0.05 | ns |
| | $T_{OLVTTL\_F24}$ | 24 mA | –0.10 | –0.20 | –0.20 | –0.20 | ns |
| | $T_{OLVCMOS\_2}$ | LVCMOS2 | 0.10 | +0.09 | +0.09 | +0.09 | ns |
| | $T_{OLVCMOS\_18}$ | LVCMOS18 | 0.10 | +0.7 | +0.7 | +0.7 | ns |
| | $T_{OLVDS}$ | LVDS | –0.39 | –1.2 | –1.2 | –1.2 | ns |
| | $T_{OLVPECL}$ | LVPECL | –0.20 | –0.41 | –0.41 | –0.41 | ns |
| | $T_{OPCI33\_3}$ | PCI, 33 MHz, 3.3 V | 0.50 | +2.3 | +2.3 | +2.3 | ns |
| | $T_{OPCI66\_3}$ | PCI, 66 MHz, 3.3 V | 0.10 | –0.41 | –0.41 | –0.41 | ns |
| | $T_{OGTL}$ | GTL | 0.6 | +0.49 | +0.49 | +0.49 | ns |
| | $T_{OGTLP}$ | GTL+ | 0.7 | +0.8 | +0.8 | +0.8 | ns |
| | $T_{OHSTL\_I}$ | HSTL I | 0.10 | –0.51 | –0.51 | –0.51 | ns |
| | $T_{OHSTL\_IIII}$ | HSTL III | –0.10 | –0.91 | –0.91 | –0.91 | ns |
| | $T_{OHSTL\_IV}$ | HSTL IV | –0.20 | –1.01 | –1.01 | –1.01 | ns |
| | $T_{OSSTL2\_I}$ | SSTL2 I | –0.10 | –0.51 | –0.51 | –0.51 | ns |
| | $T_{OSSTL2\_II}$ | SSTL2 II | –0.20 | –0.91 | –0.91 | –0.91 | ns |
| | $T_{OSSTL3\_I}$ | SSTL3 I | –0.20 | –0.51 | –0.51 | –0.51 | ns |
| | $T_{OSSTL3\_II}$ | SSTL3 II | –0.30 | –1.01 | –1.01 | –1.01 | ns |
| | $T_{OCTT}$ | CTT | 0.0 | –0.61 | –0.61 | –0.61 | ns |
| | $T_{OAGP}$ | AGP | –0.1 | –0.91 | –0.91 | –0.91 | ns |

**Notes:**
1. The numbers for Min are **Advance** product specification numbers.

## Calculation of $T_{ioop}$ as a Function of Capacitance

$T_{ioop}$ is the propagation delay from the O Input of the IOB to the pad. The values for $T_{ioop}$ are based on the standard capacitive load (Csl) for each I/O standard as listed in Table 2.

*Table 2:* **Constants for Use in Calculation of $T_{ioop}$**

| Standard | Csl (pF) | fl (ns/pF) |
|---|---|---|
| LVTTL Fast Slew Rate, 2mA drive | 35 | 0.41 |
| LVTTL Fast Slew Rate, 4mA drive | 35 | 0.20 |
| LVTTL Fast Slew Rate, 6mA drive | 35 | 0.13 |
| LVTTL Fast Slew Rate, 8mA drive | 35 | 0.079 |
| LVTTL Fast Slew Rate, 12mA drive | 35 | 0.044 |
| LVTTL Fast Slew Rate, 16mA drive | 35 | 0.043 |
| LVTTL Fast Slew Rate, 24mA drive | 35 | 0.033 |
| LVTTL Slow Slew Rate, 2mA drive | 35 | 0.41 |
| LVTTL Slow Slew Rate, 4mA drive | 35 | 0.20 |
| LVTTL Slow Slew Rate, 6mA drive | 35 | 0.10 |
| LVTTL Slow Slew Rate, 8mA drive | 35 | 0.086 |
| LVTTL Slow Slew Rate, 12mA drive | 35 | 0.058 |
| LVTTL Slow Slew Rate, 16mA drive | 35 | 0.050 |
| LVTTL Slow Slew Rate, 24mA drive | 35 | 0.048 |
| LVCMOS2 | 35 | 0.041 |
| LVCMOS18 | 35 | 0.050 |
| PCI 33 MHZ 3.3 V | 10 | 0.050 |
| PCI 66 MHz 3.3 V | 10 | 0.033 |
| GTL | 0 | 0.014 |
| GTL+ | 0 | 0.017 |
| HSTL Class I | 20 | 0.022 |
| HSTL Class III | 20 | 0.016 |
| HSTL Class IV | 20 | 0.014 |
| SSTL2 Class I | 30 | 0.028 |
| SSTL2 Class II | 30 | 0.016 |
| SSTL3 Class I | 30 | 0.029 |
| SSTL3 Class II | 30 | 0.016 |
| CTT | 20 | 0.035 |
| AGP | 10 | 0.037 |

**Notes:**
1. I/O parameter measurements are made with the capacitance values shown above. See the Application Examples for appropriate terminations.
2. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

For other capacitive loads, use the formulas below to calculate the corresponding $T_{ioop}$.

$$T_{ioop} = T_{ioop} + T_{opadjust} + (C_{load} - C_{sl}) * fl$$

where:

$T_{opadjust}$ is reported above in the Output Delay Adjustment section.

$C_{load}$ is the capacitive load for the design.

*Table 3:* **Delay Measurement Methodology**

| Standard | $V_L$[1] | $V_H$[1] | Meas. Point | $V_{REF}$ (Typ)[2] |
|---|---|---|---|---|
| LVTTL | 0 | 3 | 1.4 | - |
| LVCMOS2 | 0 | 2.5 | 1.125 | - |
| PCI33_3 | Per PCI Spec | | | - |
| PCI66_3 | Per PCI Spec | | | - |
| GTL | $V_{REF}$ –0.2 | $V_{REF}$ +0.2 | $V_{REF}$ | 0.80 |
| GTL+ | $V_{REF}$ –0.2 | $V_{REF}$ +0.2 | $V_{REF}$ | 1.0 |
| HSTL Class I | $V_{REF}$ –0.5 | $V_{REF}$ +0.5 | $V_{REF}$ | 0.75 |
| HSTL Class III | $V_{REF}$ –0.5 | $V_{REF}$ +0.5 | $V_{REF}$ | 0.90 |
| HSTL Class IV | $V_{REF}$ –0.5 | $V_{REF}$ +0.5 | $V_{REF}$ | 0.90 |
| SSTL3 I & II | $V_{REF}$ –1.0 | $V_{REF}$ +1.0 | $V_{REF}$ | 1.5 |
| SSTL2 I & II | $V_{REF}$ –0.75 | $V_{REF}$ +0.75 | $V_{REF}$ | 1.25 |
| CTT | $V_{REF}$ –0.2 | $V_{REF}$ +0.2 | $V_{REF}$ | 1.5 |
| AGP | $V_{REF}$ – (0.2x$V_{CCO}$) | $V_{REF}$ + (0.2x$V_{CCO}$) | $V_{REF}$ | Per AGP Spec |
| LVDS | 1.2 – 0.125 | 1.2 + 0.125 | 1.2 | |
| LVPECL | 1.6 – 0.3 | 1.6 + 0.3 | 1.6 | |

**Notes:**
1. Input waveform switches between $V_L$ and $V_H$.
2. Measurements are made at $V_{REF}$ (Typ), Maximum, and Minimum. Worst-case values are reported.

   I/O parameter measurements are made with the capacitance values shown in Table 2. See the Application Examples for appropriate terminations.

   I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

## Clock Distribution Switching Characteristics

| Description | Symbol | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | Min[1] | -8 | -7 | -6 | |
| **GCLK IOB and Buffer** | | | | | | |
| Global Clock PAD to output. | $T_{GPIO}$ | 0.38 | 0.7 | 0.7 | 0.7 | ns, max |
| Global Clock Buffer I input to O output | $T_{GIO}$ | 0.11 | 0.19 | 0.45 | 0.50 | ns, max |

**Notes:**
1. The numbers for Min are **Advance** product specification numbers.

## I/O Standard Global Clock Input Adjustments

| Description[1] | Symbol | Standard | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min[2] | -8 | -7 | -6 | |
| **Data Input Delay Adjustments** | | | | | | | |
| Standard-specific global clock input delay adjustments | $T_{GPLVTTL}$ | LVTTL | 0.0 | 0.0 | 0.0 | 0.0 | ns, max |
| | $T_{GPLVCMOS2}$ | LVCMOS2 | –0.02 | 0.0 | 0.0 | 0.0 | ns, max |
| | $T_{GPLVCMOS18}$ | LVCMOS2 | 0.12 | 0.20 | 0.20 | 0.20 | ns, max |
| | $T_{GLVDS}$ | LVDS | 0.23 | 0.38 | 0.38 | 0.38 | ns, max |
| | $T_{GLVPECL}$ | LVPECL | 0.23 | 0.38 | 0.38 | 0.38 | ns, max |
| | $T_{GPPCI33\_3}$ | PCI, 33 MHz, 3.3 V | –0.05 | 0.08 | 0.08 | 0.08 | ns, max |
| | $T_{GPPCI66\_3}$ | PCI, 66 MHz, 3.3 V | –0.05 | –0.11 | –0.11 | –0.11 | ns, max |
| | $T_{GPGTL}$ | GTL | 0.20 | 0.37 | 0.37 | 0.37 | ns, max |
| | $T_{GPGTLP}$ | GTL+ | 0.20 | 0.37 | 0.37 | 0.37 | ns, max |
| | $T_{GPHSTL}$ | HSTL | 0.18 | 0.27 | 0.27 | 0.27 | ns, max |
| | $T_{GPSSTL2}$ | SSTL2 | 0.21 | 0.27 | 0.27 | 0.27 | ns, max |
| | $T_{GPSSTL3}$ | SSTL3 | 0.18 | 0.27 | 0.27 | 0.27 | ns, max |
| | $T_{GPCTT}$ | CTT | 0.22 | 0.33 | 0.33 | 0.33 | ns, max |
| | $T_{GPAGP}$ | AGP | 0.21 | 0.27 | 0.27 | 0.27 | ns, max |

**Notes:**
1. Input timing for GPLVTTL is measured at 1.4 V. For other I/O standards, see Table 3.
2. The numbers for Min are **Advance** product specification numbers.

## CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used, see Figure 2. The values listed below are worst-case. Precise values are provided by the timing analyzer.

| Description[1] | Symbol | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | Min[2] | -8 | -7 | -6 | |
| **Combinatorial Delays** | | | | | | |
| 4-input function: F/G inputs to X/Y outputs | $T_{ILO}$ | 0.19 | 0.40 | 0.42 | 0.47 | ns, max |
| 5-input function: F/G inputs to F5 output | $T_{IF5}$ | 0.36 | 0.76 | 0.8 | 0.9 | ns, max |
| 5-input function: F/G inputs to X output | $T_{IF5X}$ | 0.35 | 0.74 | 0.8 | 0.9 | ns, max |
| 6-input function: F/G inputs to Y output via F6 MUX | $T_{IF6Y}$ | 0.35 | 0.74 | 0.9 | 1.0 | ns, max |
| 6-input function: F5IN input to Y output | $T_{F5INY}$ | 0.04 | 0.11 | 0.20 | 0.22 | ns, max |
| Incremental delay routing through transparent latch to XQ/YQ outputs | $T_{IFNCTL}$ | 0.27 | 0.63 | 0.7 | 0.8 | ns, max |
| BY input to YB output | $T_{BYYB}$ | 0.19 | 0.38 | 0.46 | 0.51 | ns, max |
| **Sequential Delays** | | | | | | |
| FF Clock CLK to XQ/YQ outputs | $T_{CKO}$ | 0.34 | 0.87 | 0.9 | 1.0 | ns, max |
| Latch Clock CLK to XQ/YQ outputs | $T_{CKLO}$ | 0.40 | 0.87 | 0.9 | 1.0 | ns, max |
| **Setup and Hold Times before/after Clock CLK** | | | | | | |
| 4-input function: F/G Inputs | $T_{ICK}$ / $T_{CKI}$ | 0.39 / 0 | 0.9 / 0 | 1.0 / 0 | 1.1 / 0 | ns, min |
| 5-input function: F/G inputs | $T_{IF5CK}$ / $T_{CKIF5}$ | 0.55 / 0 | 1.3 / 0 | 1.4 / 0 | 1.5 / 0 | ns, min |
| 6-input function: F5IN input | $T_{F5INCK}$ / $T_{CKF5IN}$ | 0.27 / 0 | 0.6 / 0 | 0.8 / 0 | 0.8 / 0 | ns, min |
| 6-input function: F/G inputs via F6 MUX | $T_{IF6CK}$ / $T_{CKIF6}$ | 0.58 / 0 | 1.3 / 0 | 1.5 / 0 | 1.6 / 0 | ns, min |
| BX/BY inputs | $T_{DICK}$ / $T_{CKDI}$ | 0.25 / 0 | 0.6 / 0 | 0.7 / 0 | 0.8 / 0 | ns, min |
| CE input | $T_{CECK}$ / $T_{CKCE}$ | 0.28 / 0 | 0.55 / 0 | 0.7 / 0 | 0.7 / 0 | ns, min |
| SR/BY inputs (synchronous) | $T_{RCK}$ / $T_{CKR}$ | 0.24 / 0 | 0.46 / 0 | 0.52 / 0 | 0.6 / 0 | ns, min |
| **Clock CLK** | | | | | | |
| Minimum Pulse Width, High | $T_{CH}$ | 0.56 | 1.2 | 1.3 | 1.4 | ns, min |
| Minimum Pulse Width, Low | $T_{CL}$ | 0.56 | 1.2 | 1.3 | 1.4 | ns, min |
| **Set/Reset** | | | | | | |
| Minimum Pulse Width, SR/BY inputs | $T_{RPW}$ | 0.94 | 1.9 | 2.1 | 2.4 | ns, min |
| Delay from SR/BY inputs to XQ/YQ outputs (asynchronous) | $T_{RQ}$ | 0.39 | 0.8 | 0.9 | 1.0 | ns, max |
| Toggle Frequency (MHz) (for export control) | $F_{TOG}$ | - | 416 | 400 | 357.2 | MHz |

**Notes:**

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. The numbers for Min are **Advance** product specification numbers.

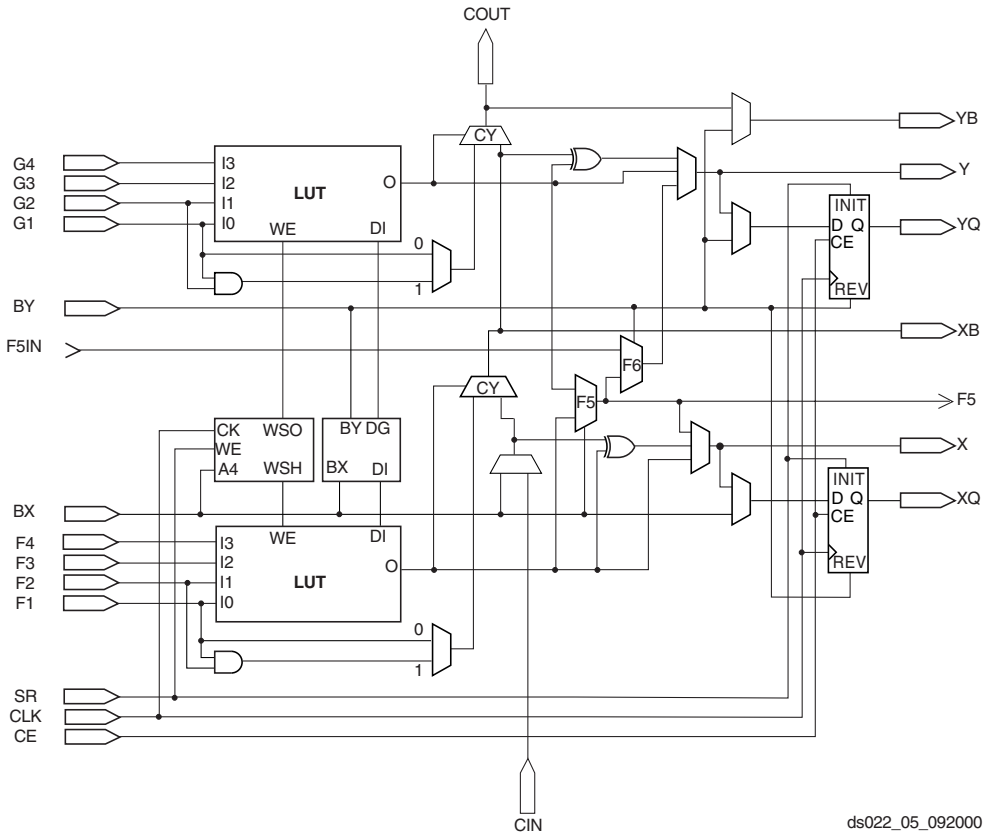



*Figure 2:* **Detailed View of Virtex-E Slice**

## CLB Arithmetic Switching Characteristics

Setup times not listed explicitly can be approximated by decreasing the combinatorial delays by the setup time adjustment listed. Precise values are provided by the timing analyzer.

| Description[1] | Symbol | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | Min[2] | -8 | -7 | -6 | |
| **Combinatorial Delays** | | | | | | |
| F operand inputs to X via XOR | $T_{OPX}$ | 0.32 | 0.68 | 0.8 | 0.8 | ns, max |
| F operand input to XB output | $T_{OPXB}$ | 0.35 | 0.65 | 0.8 | 0.9 | ns, max |
| F operand input to Y via XOR | $T_{OPY}$ | 0.59 | 1.06 | 1.4 | 1.5 | ns, max |
| F operand input to YB output | $T_{OPYB}$ | 0.48 | 0.89 | 1.1 | 1.3 | ns, max |
| F operand input to COUT output | $T_{OPCYF}$ | 0.37 | 0.71 | 0.9 | 1.0 | ns, max |
| G operand inputs to Y via XOR | $T_{OPGY}$ | 0.34 | 0.72 | 0.8 | 0.9 | ns, max |
| G operand input to YB output | $T_{OPGYB}$ | 0.47 | 0.78 | 1.2 | 1.3 | ns, max |
| G operand input to COUT output | $T_{OPCYG}$ | 0.36 | 0.60 | 0.9 | 1.0 | ns, max |
| BX initialization input to COUT | $T_{BXCY}$ | 0.19 | 0.36 | 0.51 | 0.57 | ns, max |
| CIN input to X output via XOR | $T_{CINX}$ | 0.27 | 0.50 | 0.6 | 0.7 | ns, max |
| CIN input to XB | $T_{CINXB}$ | 0.02 | 0.03 | 0.07 | 0.08 | ns, max |
| CIN input to Y via XOR | $T_{CINY}$ | 0.26 | 0.45 | 0.7 | 0.7 | ns, max |
| CIN input to YB | $T_{CINYB}$ | 0.16 | 0.28 | 0.38 | 0.43 | ns, max |
| CIN input to COUT output | $T_{BYP}$ | 0.05 | 0.10 | 0.14 | 0.15 | ns, max |
| **Multiplier Operation** | | | | | | |
| F1/2 operand inputs to XB output via AND | $T_{FANDXB}$ | 0.10 | 0.30 | 0.35 | 0.39 | ns, max |
| F1/2 operand inputs to YB output via AND | $T_{FANDYB}$ | 0.28 | 0.56 | 0.7 | 0.8 | ns, max |
| F1/2 operand inputs to COUT output via AND | $T_{FANDCY}$ | 0.17 | 0.38 | 0.46 | 0.51 | ns, max |
| G1/2 operand inputs to YB output via AND | $T_{GANDYB}$ | 0.20 | 0.46 | 0.55 | 0.7 | ns, max |
| G1/2 operand inputs to COUT output via AND | $T_{GANDCY}$ | 0.09 | 0.28 | 0.30 | 0.34 | ns, max |
| **Setup and Hold Times before/after Clock CLK** | | | | | | |
| CIN input to FFX | $T_{CCKX}/T_{CKCX}$ | 0.47 / 0 | 1.0 / 0 | 1.2 / 0 | 1.3 / 0 | ns, min |
| CIN input to FFY | $T_{CCKY}/T_{CKCY}$ | 0.49 / 0 | 0.92 / 0 | 1.2 / 0 | 1.3 / 0 | ns, min |

**Notes:**

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. The numbers for Min are **Advance** product specification numbers.

## CLB Distributed RAM Switching Characteristics

| Description[1] | Symbol | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | Min[2] | -8 | -7 | -6 | |
| **Sequential Delays** | | | | | | |
| Clock CLK to X/Y outputs (WE active) 16 x 1 mode | $T_{SHCKO16}$ | 0.67 | 1.48 | 1.5 | 1.7 | ns, max |
| Clock CLK to X/Y outputs (WE active) 32 x 1 mode | $T_{SHCKO32}$ | 0.84 | 1.76 | 1.9 | 2.1 | ns, max |
| **Shift-Register Mode** Clock CLK to X/Y outputs | $T_{REG}$ | 1.25 | 2.49 | 2.9 | 3.2 | ns, max |
| **Setup and Hold Times before/after Clock CLK** | | | | | | |
| F/G address inputs | $T_{AS}/T_{AH}$ | 0.19 / 0 | 0.38 / 0 | 0.42 / 0 | 0.47 / 0 | ns, min |
| BX/BY data inputs (DIN) | $T_{DS}/T_{DH}$ | 0.24 / 0 | 0.47 / 0 | 0.53 / 0 | 0.6 / 0 | ns, min |
| CE input (WE) | $T_{WS}/T_{WH}$ | 0.29 / 0 | 0.57 / 0 | 0.7 / 0 | 0.8 / 0 | ns, min |
| **Shift-Register Mode** | | | | | | |
| BX/BY data inputs (DIN) | $T_{SHDICK}$ | 0.24 / 0 | 0.47 / 0 | 0.53 / 0 | 0.6 / 0 | ns, min |
| CE input (WS) | $T_{SHCECK}$ | 0.29 / 0 | 0.57 / 0 | 0.7 / 0 | 0.8 / 0 | ns, min |
| **Clock CLK** | | | | | | |
| Minimum Pulse Width, High | $T_{WPH}$ | 0.96 | 1.9 | 2.1 | 2.4 | ns, min |
| Minimum Pulse Width, Low | $T_{WPL}$ | 0.96 | 1.9 | 2.1 | 2.4 | ns, min |
| Minimum clock period to meet address write cycle time | $T_{WC}$ | 1.92 | 3.8 | 4.2 | 4.8 | ns, min |
| **Shift-Register Mode** | | | | | | |
| Minimum Pulse Width, High | $T_{SRPH}$ | 1.0 | 1.9 | 2.1 | 2.4 | ns, min |
| Minimum Pulse Width, Low | $T_{SRPL}$ | 1.0 | 1.9 | 2.1 | 2.4 | ns, min |

**Notes:**
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. The numbers for Min are **Advance** product specification numbers.

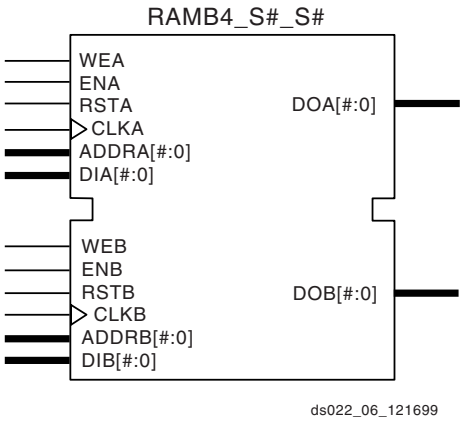



*Figure 3:* **Dual-Port Block SelectRAM**

## Block RAM Switching Characteristics

| Description[1] | Symbol | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | Min[2] | -8 | -7 | -6 | |
| **Sequential Delays** | | | | | | |
| Clock CLK to DOUT output | $T_{BCKO}$ | 0.63 | 2.46 | 3.1 | 3.5 | ns, max |
| **Setup and Hold Times before Clock CLK** | | | | | | |
| ADDR inputs | $T_{BACK}/T_{BCKA}$ | 0.42 / 0 | 0.9 / 0 | 1.0 / 0 | 1.1 / 0 | ns, min |
| DIN inputs | $T_{BDCK}/T_{BCKD}$ | 0.42 / 0 | 0.9 / 0 | 1.0 / 0 | 1.1 / 0 | ns, min |
| EN input | $T_{BECK}/T_{BCKE}$ | 0.97 / 0 | 2.0 / 0 | 2.2 / 0 | 2.5 / 0 | ns, min |
| RST input | $T_{BRCK}/T_{BCKR}$ | 0.9 / 0 | 1.8 / 0 | 2.1 / 0 | 2.3 / 0 | ns, min |
| WEN input | $T_{BWCK}/T_{BCKW}$ | 0.86 / 0 | 1.7 / 0 | 2.0 / 0 | 2.2 / 0 | ns, min |
| **Clock CLK** | | | | | | |
| Minimum Pulse Width, High | $T_{BPWH}$ | 0.6 | 1.2 | 1.35 | 1.5 | ns, min |
| Minimum Pulse Width, Low | $T_{BPWL}$ | 0.6 | 1.2 | 1.35 | 1.5 | ns, min |
| CLKA -> CLKB setup time for different ports | $T_{BCCS}$ | 1.2 | 2.4 | 2.7 | 3.0 | ns, min |

**Notes:**
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. The numbers for Min are **Advance** product specification numbers.

## TBUF Switching Characteristics

| Description | Symbol | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | Min[1] | -8 | -7 | -6 | |
| **Combinatorial Delays** | | | | | | |
| IN input to OUT output | $T_{IO}$ | 0.0 | 0.0 | 0.0 | 0 .0 | ns, max |
| TRI input to OUT output high-impedance | $T_{OFF}$ | 0.05 | 0.092 | 0.10 | 0.11 | ns, max |
| TRI input to valid data on OUT output | $T_{ON}$ | 0.05 | 0.092 | 0.10 | 0.11 | ns, max |

**Notes:**
1. The numbers for Min are **Advance** product specification numbers.

## JTAG Test Access Port Switching Characteristics

| Description | Symbol | Value | Units |
|---|---|---|---|
| TMS and TDI Setup times before TCK | $T_{TAPTK}$ | 4.0 | ns, min |
| TMS and TDI Hold times after TCK | $T_{TCKTAP}$ | 2.0 | ns, min |
| Output delay from clock TCK to output TDO | $T_{TCKTDO}$ | 11.0 | ns, max |
| Maximum TCK clock frequency | $F_{TCK}$ | 33 | MHz, max |

# Virtex-E Pin-to-Pin Output Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

## Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *with* DLL

| Description[1] | Symbol | Device[3] | Speed Grade[2] | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min[4] | -8 | -7 | -6 | |
| LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *with* DLL.<br>For data *output* with different standards, adjust the delays with the values shown in "IOB Output Switching Characteristics Standard Adjustments" on page 8. | $T_{ICKOFDLL}$ | XCV405E | 1.0 | 3.1 | 3.1 | 3.1 | ns |
| | | XCV812E | 1.0 | 3.1 | 3.1 | 3.1 | ns |

**Notes:**
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% $V_{CC}$ threshold with 35 pF external capacitive load. For other I/O standards and different loads, see Table 2 and Table 3.
3. DLL output jitter is already included in the timing calculation.
4. The numbers for Min are **Advance** product specification numbers.

## Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *without* DLL

| Description[1] | Symbol | Device | Speed Grade[2] | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min[3] | -8 | -7 | -6 | |
| LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *without* DLL.<br>For data *output* with different standards, adjust the delays with the values shown in "IOB Output Switching Characteristics Standard Adjustments" on page 8. | $T_{ICKOF}$ | XCV405E | 1.6 | 4.5 | 4.7 | 4.9 | ns |
| | | XCV812E | 1.8 | 4.8 | 5.0 | 5.2 | ns |

**Notes:**
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% $V_{CC}$ threshold with 35 pF external capacitive load. For other I/O standards and different loads, see Table 2 and Table 3.
3. The numbers for Min are **Advance** product specification numbers.

# Virtex-E Pin-to-Pin Input Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

## Global Clock Set-Up and Hold for LVTTL Standard, *with* DLL

| Description[1] | Symbol | Device[3] | Speed Grade[2] | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min[4] | -8 | -7 | -6 | |
| Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard.<br>For data input with different standards, adjust the setup time delay by the values shown in "IOB Input Switching Characteristics Standard Adjustments" on page 6. | | | | | | | |
| No Delay | $T_{PSDLL}/T_{PHDLL}$ | XCV405E | 1.5 / –0.4 | 1.5 / –0.4 | 1.6 / –0.4 | 1.7 / –0.4 | ns |
| Global Clock and IFF, with DLL | | XCV812E | 1.5 / –0.4 | 1.5 / –0.4 | 1.6 / –0.4 | 1.7 / –0.4 | ns |

**Notes:**
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. DLL output jitter is already included in the timing calculation.
4. The numbers for Min are **Advance** product specification numbers.

## Global Clock Set-Up and Hold for LVTTL Standard, *without* DLL

| Description[1] | Symbol | Device[3] | Speed Grade[2] | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min[4] | -8 | -7 | -6 | |
| Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard.<br>For data input with different standards, adjust the setup time delay by the values shown in "IOB Input Switching Characteristics Standard Adjustments" on page 6. | | | | | | | |
| Full Delay | $T_{PSFD}/T_{PHFD}$ | XCV405E | 2.3 / 0 | 2.3 / 0 | 2.3 / 0 | 2.3 / 0 | ns |
| Global Clock and IFF, without DLL | | XCV812E | 2.5 / 0 | 2.5 / 0 | 2.5 / 0 | 2.5 / 0 | ns |

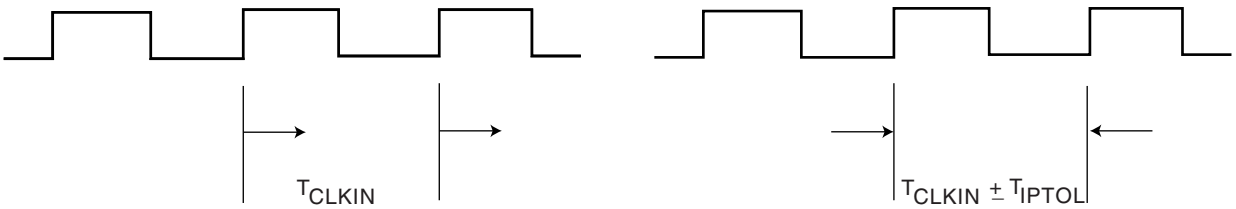
**Notes:**
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
4. The numbers for Min are **Advance** product specification numbers.

## DLL Timing Parameters

Switching parameters testing is modeled after testing methods specified by MIL-M-38510/605; all devices are 100 percent functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions.

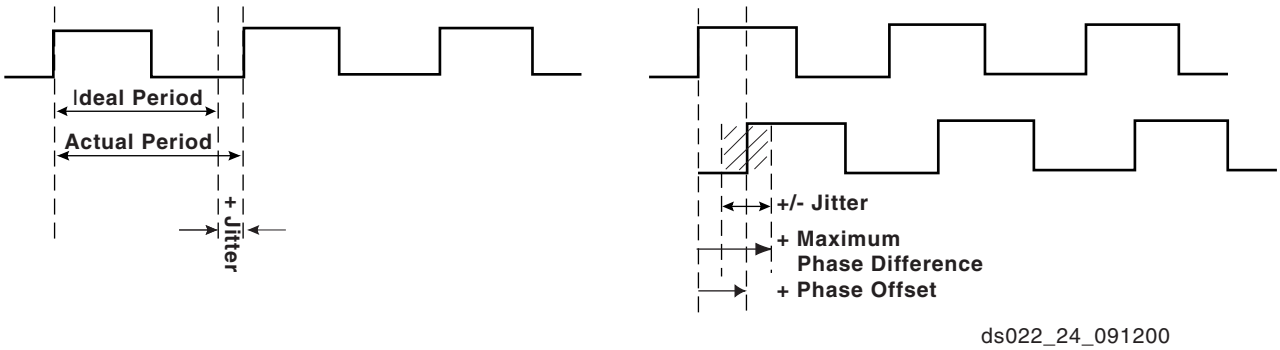
| Description | Symbol | $F_{CLKIN}$ | Speed Grade[1] | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | -8 | | -7 | | -6 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| Input Clock Frequency (CLKDLLHF) | FCLKINHF | | 60 | 320 | 60 | 320 | 60 | 260 | MHz |
| Input Clock Frequency (CLKDLL) | FCLKINLF | | 25 | 160 | 25 | 160 | 25 | 135 | MHz |
| Input Clock Low/High Pulse Width | $T_{DLLPW}$ | ≥25 MHz | 5.0 | | 5.0 | | 5.0 | | ns |
| | | ≥50 MHz | 3.0 | | 3.0 | | 3.0 | | ns |
| | | ≥100 MHz | 2.4 | | 2.4 | | 2.4 | | ns |
| | | ≥150 MHz | 2.0 | | 2.0 | | 2.0 | | ns |
| | | ≥200 MHz | 1.8 | | 1.8 | | 1.8 | | ns |
| | | ≥250 MHz | 1.5 | | 1.5 | | 1.5 | | ns |
| | | ≥300 MHz | 1.3 | | 1.3 | | NA | | ns |

***Period Tolerance:*** the allowed input clock period change in nanoseconds.




***Output Jitter:*** the difference between an ideal reference clock edge and the actual design.

***Phase Offset and Maximum Phase Difference***




ds022_24_091200

*Figure 4:* **DLL Timing Waveforms**

## DLL Clock Tolerance, Jitter, and Phase Information

All DLL output jitter and phase specifications determined through statistical measurement at the package pins using a clock mirror configuration and matched drivers.

| | | | CLKDLLHF | | CLKDLL | | |
|---|---|---|---|---|---|---|---|
| **Description** | **Symbol** | **$F_{CLKIN}$** | **Min** | **Max** | **Min** | **Max** | **Units** |
| Input Clock Period Tolerance | $T_{IPTOL}$ | | - | 1.0 | - | 1.0 | ns |
| Input Clock Jitter Tolerance (Cycle to Cycle) | $T_{IJITCC}$ | | - | ± 150 | - | ± 300 | ps |
| Time Required for DLL to Acquire Lock(6) | $T_{LOCK}$ | > 60 MHz | - | 20 | - | 20 | µs |
| | | 50 - 60 MHz | - | - | - | 25 | µs |
| | | 40 - 50 MHz | - | - | - | 50 | µs |
| | | 30 - 40 MHz | - | - | - | 90 | µs |
| | | 25 - 30 MHz | - | - | - | 120 | µs |
| Output Jitter (cycle-to-cycle) for any DLL Clock Output(1) | $T_{OJITCC}$ | | | ± 60 | | ± 60 | ps |
| Phase Offset between CLKIN and CLKO(2) | $T_{PHIO}$ | | | ± 100 | | ± 100 | ps |
| Phase Offset between Clock Outputs on the DLL(3) | $T_{PHOO}$ | | | ± 140 | | ± 140 | ps |
| Maximum Phase Difference between CLKIN and CLKO(4) | $T_{PHIOM}$ | | | ± 160 | | ± 160 | ps |
| Maximum Phase Difference between Clock Outputs on the DLL(5) | $T_{PHOOM}$ | | | ± 200 | | ± 200 | ps |

**Notes:**

1. **Output Jitter** is cycle-to-cycle jitter measured on the DLL output clock and is based on a maximum tap delay resolution, *excluding* input clock jitter.
2. **Phase Offset between CLKIN and CLKO** is the worst-case fixed time difference between rising edges of CLKIN and CLKO, *excluding* Output Jitter and input clock jitter.
3. **Phase Offset between Clock Outputs on the DLL** is the worst-case fixed time difference between rising edges of any two DLL outputs, *excluding* Output Jitter and input clock jitter.
4. **Maximum Phase Difference between CLKIN an CLKO** is the sum of Output Jitter and Phase Offset between CLKIN and CLKO, or the greatest difference between CLKIN and CLKO rising edges due to DLL alone (*excluding* input clock jitter).
5. **Maximum Phase DIfference between Clock Outputs on the DLL** is the sum of Output JItter and Phase Offset between any DLL clock outputs, or the greatest difference between any two DLL output rising edges sue to DLL alone (*excluding* input clock jitter).
6. Add 30% to the value for Industrial grade parts.

## Revision History

The following table shows the revision history for this document.

| Date | Version | Revision |
|---|---|---|
| 03/23/00 | 1.0 | Initial Xilinx release. |
| 08/01/00 | 1.1 | Accumulated edits and fixes. Upgrade to Preliminary. Preview -8 numbers added. Reformatted to adhere to corporate documentation style guidelines. Minor changes in BG560 pin-out table. |
| 09/19/00 | 1.2 | • In Table 3 (Module 4), **FG676 Fine-Pitch BGA — XCV405E**, the following pins are no longer labeled as VREF: B7, G16, G26, W26, AF20, AF8, Y1, H1.<br>• Min values added to **Virtex-E Electrical Characteristics** tables. |
| 11/20/00 | 1.3 | • Updated speed grade -8 numbers in **Virtex-E Electrical Characteristics** tables (Module 3).<br>• Updated minimums in Table 11 (Module 2), and added notes to Table 12 (Module 2).<br>• Added to note 2 of **Absolute Maximum Ratings** (Module 3).<br>• Changed all minimum hold times to –0.4 for **Global Clock Set-Up and Hold for LVTTL Standard, with DLL** (Module 3).<br>• Revised maximum $T_{DLLPW}$ in -6 speed grade for **DLL Timing Parameters** (Module 3). |
| 04/02/01 | 1.4 | • In Table 4, **FG676 Fine-Pitch BGA — XCV405E**, pin B19 is no longer labeled as VREF, and pin G16 is now labeled as VREF.<br>• Updated values in Virtex-E Switching Characteristics tables.<br>• Converted data sheet to modularized format. See the Virtex-E Extended Memory Data Sheet section. |
| 04/19/01 | 1.5 | • Updated values in Virtex-E Switching Characteristics tables. |
| 07/23/01 | 1.6 | • Under Absolute Maximum Ratings, changed ($T_{SOL}$) to 220 °C .<br>• Changes made to SSTL symbol names in IOB Input Switching Characteristics Standard Adjustments table. |
| 07/26/01 | 1.7 | • Removed $T_{SOL}$ parameter and added footnote to Absolute Maximum Ratings table. |
| 09/18/01 | 1.8 | • Reworded power supplies footnote to Absolute Maximum Ratings table. |
| 10/25/01 | 1.9 | • Updated the speed grade designations used in data sheets, and added Table 1, which shows the current speed grade designation for each device.<br>• Updated Power-On Power Supply Requirements table. |
| 11/09/01 | 2.0 | • Updated the XCV405E device speed grade designation to Preliminary in Table 1.<br>• Updated Power-On Power Supply Requirements table. |
| 02/01/02 | 2.1 | • Updated footnotes to the DC Input and Output Levels and DLL Clock Tolerance, Jitter, and Phase Information tables. |

## Virtex-E Extended Memory Data Sheet

The Virtex-E Extended Memory Data Sheet contains the following modules:

- DS025-1, Virtex-E 1.8V Extended Memory FPGAs: **Introduction and Ordering Information (Module 1)**
- DS025-2, Virtex-E 1.8V Extended Memory FPGAs: **Functional Description (Module 2)**
- DS025-3, Virtex-E 1.8V Extended Memory FPGAs: **DC and Switching Characteristics (Module 3)**
- DS025-4, Virtex-E 1.8V Extended Memory FPGAs: **Pinout Tables (Module 4)**