RF2412

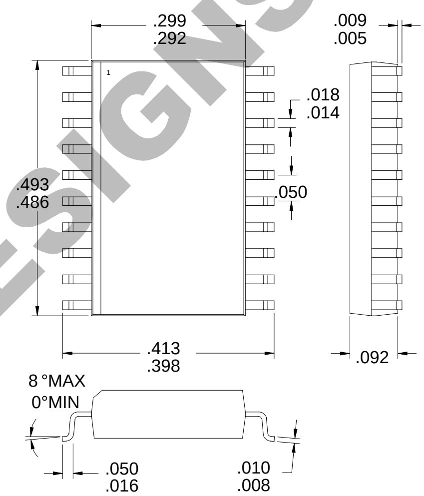
BROADBAND DUAL-CONVERSION QUADRATURE MODULATOR

Typical Applications

- Digital and Spread-Spectrum Systems
- Analog Communication Systems
- UHF Digital and Analog Transmitters
- GMSK, QPSK, DQPSK, QAM
- Portable Battery-Powered Equipment
- Commercial and Consumer Systems

Product Description

The RF2412 is a monolithic integrated transmitter universal modulation IC capable of generating modulated AM, PM, or compound carriers in the VHF/UHF frequency range. The modulation is performed at VHF, then the resulting spectrum is upconverted to a frequency range between 100MHz to 1000MHz. The IC contains all of the required components to implement the modulation function including differential amplifiers for the baseband inputs, a LO 90° hybrid phase splitter, limiting LO amplifiers, two balanced mixers, a combining differential amplifier, a second upconvert balanced mixer, and an output RF amplifier which will drive a 50Ω load. Since the modulation is performed at a low frequency, excellent amplitude balance and phase accuracy are obtained.



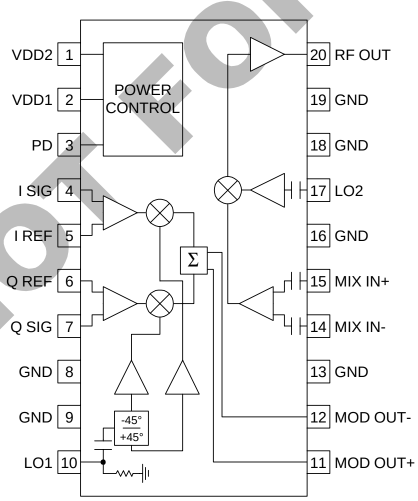
Package Style: SOP-20

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☑ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Features

- Single 3V to 6V Power Supply
- Digitally-Controlled Power Down Mode
- Dual Conversion
- DC to 50MHz Modulation Frequency
- 50MHz to 150MHz IF Frequency
- 100MHz to 1000MHz RF Frequency



Functional Block Diagram

Ordering Information

RF2412	Broadband Dual-Conversion Quadrature Modulator
RF2412 PCBA	Fully Assembled Evaluation Board

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to 7.5	V_{DC}
PD Voltage	V_{DD}+0.4	V_{DC}
Input LO and RF Levels	+6	dBm
Ambient Operating Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

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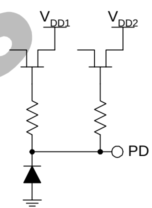
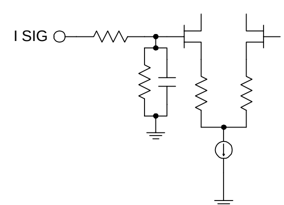
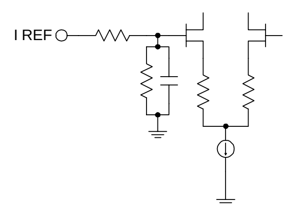
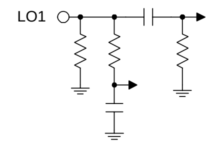
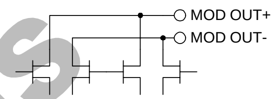
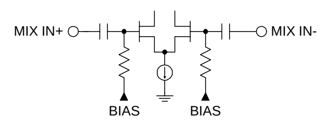
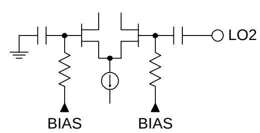
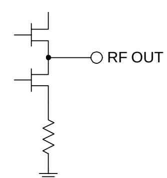
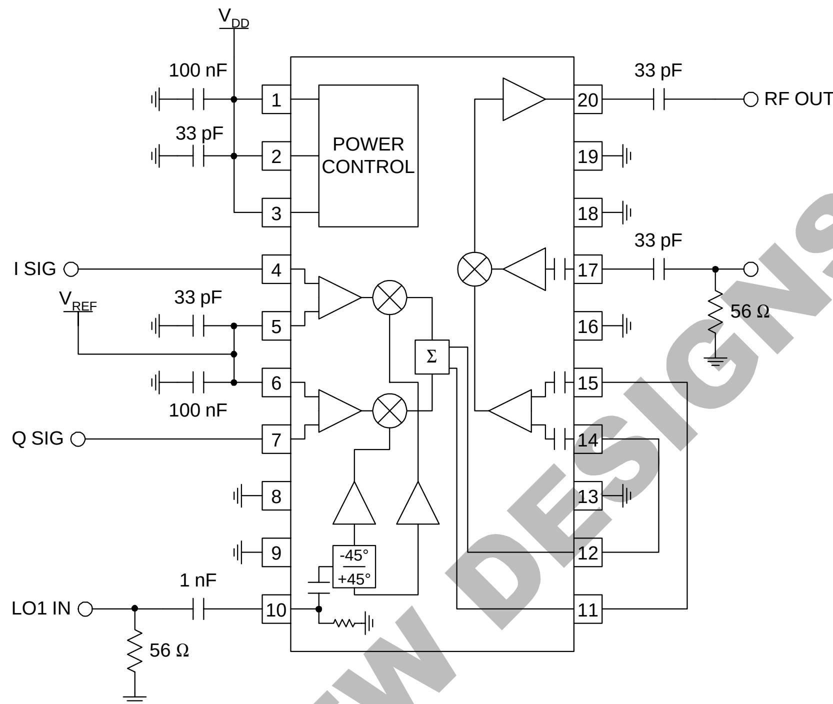
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Modulation Signals (I&Q)					T=25°C, V_{DD}=5V, V_{REF}=2.5V, BB=100kHz, LO1=70MHz, LO2=700MHz, V_{MOD}=3.0V_{PP} SSB, unless indicated otherwise.
Frequency Range		DC to 50		MHz	
Signal Level		2.2		V_{PP}	For 1dB compression
Reference Voltage (V_{REF})		2.0 to 3.0		V	
Input Impedance to GND		3		kΩ	
Amplitude Balance		0.1		dB	
Quadrature Phase Error		1		°	
First LO Input					
Frequency Range		50 to 150		MHz	For 30dB sideband suppression
		30 to 225		MHz	For 20dB sideband suppression
Power Level		-5 to +6		dBm	
Input Impedance		750-j400		Ω	Without external 50Ω termination
Second LO Input					
Frequency Range		100 to 1000		MHz	
Power Level		-5 to +6		dBm	
Input Impedance		600-j700		Ω	Without external 50Ω termination
RF Output					
Output Power					V_{DD}=5V, LO1,2 level=0dBm, SSB
		+4		dBm	Freq=200MHz to 500MHz
		0		dBm	Freq=500MHz to 800MHz
		-4		dBm	Freq=800MHz to 1000MHz
Output Power					V_{DD}=6V, LO1,2 power=0dBm, SSB
		+6		dBm	Freq=200MHz to 500MHz
		+3		dBm	Freq=500MHz to 800MHz
		-1		dBm	Freq=800MHz to 1000MHz
Nominal Output Impedance		50		Ω	
Output VSWR		1.5:1			Freq<600MHz
		3:1			600MHz<Freq<1000MHz
Output Broadband Noise Power		-155		dBm/Hz	
Spurious					Single sideband modulation
Sideband Suppression		35		dBc	
Carrier Suppression		25		dBc	Unadjusted. Modulation DC offset may be externally adjusted for maximum suppression. See Pin Descriptions.
First LO Harmonics		-20		dBc	Odd unfiltered IF
		-30		dBc	Even unfiltered IF
Power Supply					
Voltage		3 to 6.5		V	Operating limits
Current Consumption		31	35	mA	V_{CC}=5.0V

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Power Down					
Turn On/Off Time		<100		ns	
PD Input Resistance		>50		kΩ	
Power Down "ON"		V_{CC}		V	Threshold voltage
Power Down "OFF"		0		V	Threshold voltage

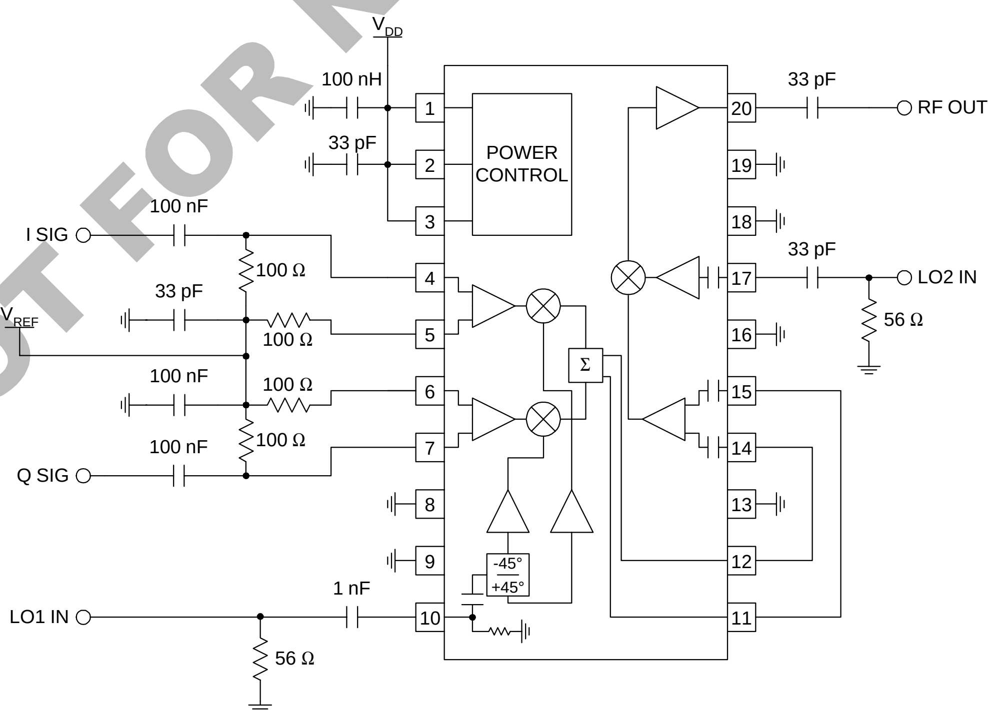
Pin	Function	Description	Interface Schematic
1	**VDD2**	Supply Voltage for the RF Output Stage only. A 33pF external bypass capacitor is required, and an optional 0.1µF will be required if no other low frequency bypass capacitors are nearby. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane. Though the part is designed to run from a 5V supply, it will also work at 4V. Gain and available output power will be reduced by 5dB to 10dB. Pins 1 and 2 may share a common bypass capacitor.	
2	**VDD1**	Supply Voltage for all circuits but the RF Output Stage. The same comments as for VDD2 apply to this pin. Pins 1 and 2 may share a common bypass capacitor.	
3	**PD**	Power Down control. When this pin is 0V all circuits are turned off, and when connected to V_{DD}, all circuits are operational. This is a high impedance input, internally connected to the parallel gates of two switching FETs. To minimize current consumption in power down mode, this pin should be as close to 0V as possible. Turn-on voltage of some parts of the circuit may be as low as 0.1V. In order to maximize output power, the voltage on this pin should be as close to V_{DD} as possible during normal operation. A 33pF capacitor is recommended for bypassing. If this pin is not used for power down control, it may be tied to pins 1 and 2, and all three pins may share one 33pF capacitor, provided that the associated trace lengths are minimized.	
4	**I SIG**	Baseband input to the I mixer. This pin is DC coupled. Maximum output power is obtained when the input signal has a peak to peak amplitude of 5V. A DC reference of approximately $V_{DD}/2$ must be supplied to this pin. The input impedance of this pin is about 3kΩ. The SIG and REF inputs are inputs of a differential amplifier. Therefore, the REF and SIG inputs are interchangeable. If swapping the I SIG and I REF pins, the Q SIG and Q REF pins also need to be swapped to maintain the correct phase. The SIG and REF pins may be driven differentially to increase conversion gain.	
5	**I REF**	Reference voltage for the I mixer. This voltage should be the same as the DC voltage supplied to the I SIG pin. To obtain a carrier suppression of better than 25dB it may be tuned ± 0.15V (relative to the I SIG DC voltage). Without tuning, the carrier suppression will typically be better than 25dB. The input impedance of this pin is about 3kΩ.	
6	**Q REF**	Reference voltage for the Q mixer. This voltage should be the same as the DC voltage supplied to the Q SIG pin. To obtain a carrier suppression of better than 25dB it may be tuned ±0.15V (relative to the Q SIG DC voltage). Without tuning, the carrier suppression will typically be better than 25dB. The input impedance of this pin is about 3 kΩ.	Same as pin 5.
7	**Q SIG**	Baseband input to the Q mixer. This pin is DC coupled. Maximum output power is obtained when the input signal has a peak to peak amplitude of 5V. A DC reference of approximately $V_{DD}/2$ must be supplied to this pin. The input impedance of this pin is about 3 kΩ. Therefore, the REF and SIG inputs are interchangeable. If swapping the I SIG and I REF pins, the Q SIG and Q REF also need to be swapped to maintain the correct phase. The SIG and REF pins may be driven differentially to increase conversion gain.	Same as pin 4.
8	**GND**	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
9	**GND**	Same as pin 8.	

Pin	Function	Description	Interface Schematic
10	LO1	High impedance modulator LO input. If approximately 0dBm of LO power is available, a shunt 56Ω resistor may be used for matching. If the available LO power is approximately -6dBm, then a reactive match may be required. There is an internal blocking capacitor between this pin and the LO circuitry, but not between the pin and an internal resistor to ground (see the functional block diagram). An external blocking capacitor should be provided if the pin is connected to a device with DC present. A DC path to ground (an inductor or resistor to ground) is, however, acceptable at this pin. If a blocking capacitor is required, a value of 1nF is recommended.	
11	MOD OUT+	Balanced IF output port. If no filtering is required this pin can be connected directly to the MIX IN+ pin. This pin is NOT DC blocked and carries DC. A blocking capacitor of 1nF is needed when this pin is connected to a DC path. An appropriate matching network may be needed if an IF filter is used.	
12	MOD OUT-	Same as pin 11, except complementary output.	See pin 11.
13	GND	Same as pin 8.	
14	MIX IN-	High impedance balanced input to the IF stage. This pin has an internal DC blocking capacitor. If no IF filter is needed this pin may be connected directly to MOD OUT-. If an IF filter is used, an external shunt resistor to ground may be needed to provide correct matching for the filter.	
15	MIX IN+	Same as pin 14, except complementary input.	See pin 14.
16	GND	Same as pin 8.	
17	LO2	Mixer LO Input port. A shunt 56Ω resistor can be used for matching. This pin has internal DC blocking.	
18	GND	Same as pin 8.	
19	GND	Same as pin 8.	
20	RF OUT	50Ω output. This pin is not internally DC blocked, and an external blocking capacitor of 33pF is required.	

Application Schematic
915 MHz Operation, DC Coupled I and Q Inputs



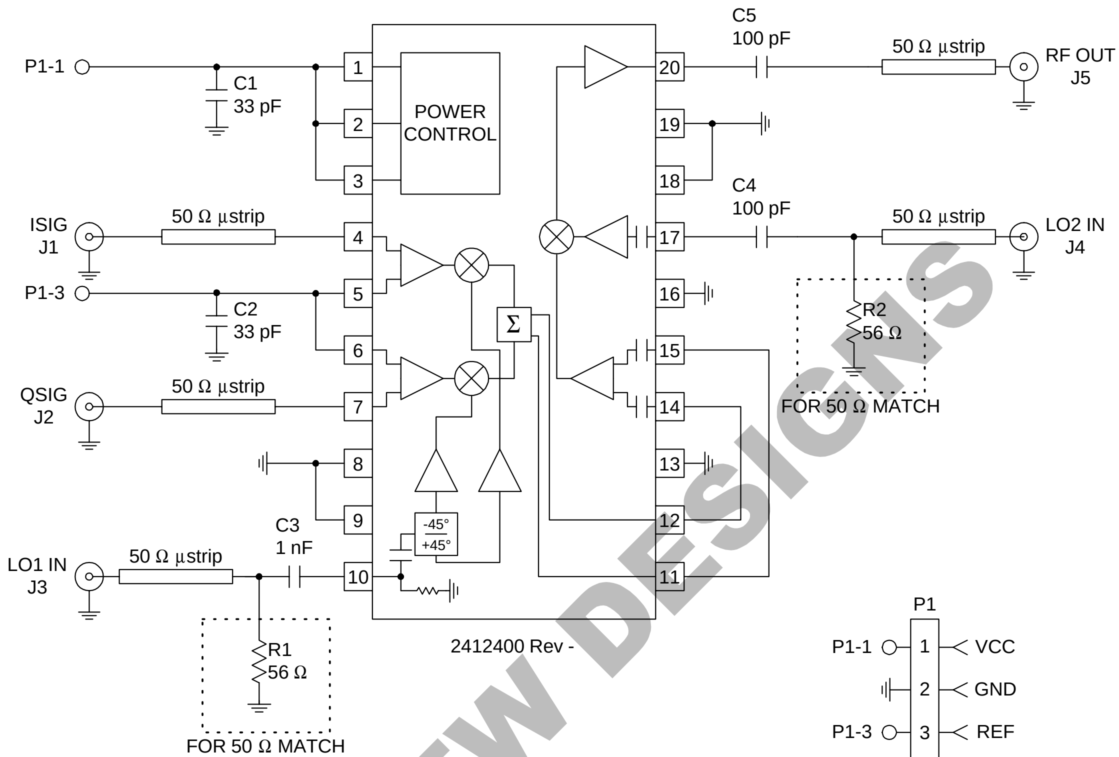
Application Schematic
915 MHz Operation, AC Coupled I and Q Inputs



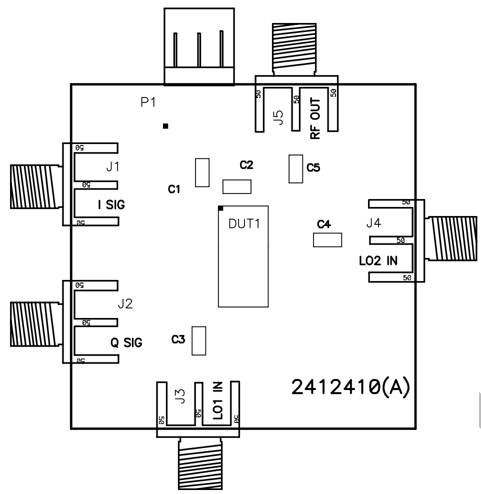
5
MODULATORS AND UPCONVERTERS

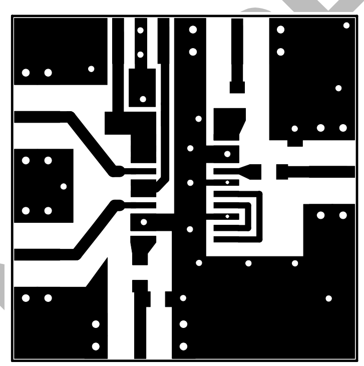
Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)

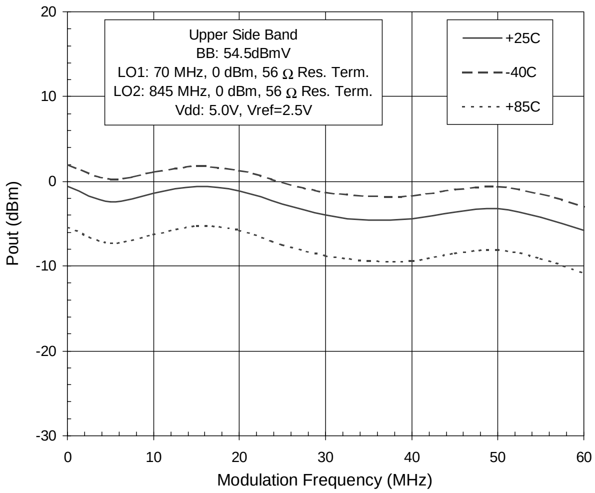


Evaluation Board Layout
1.52” x 1.52”

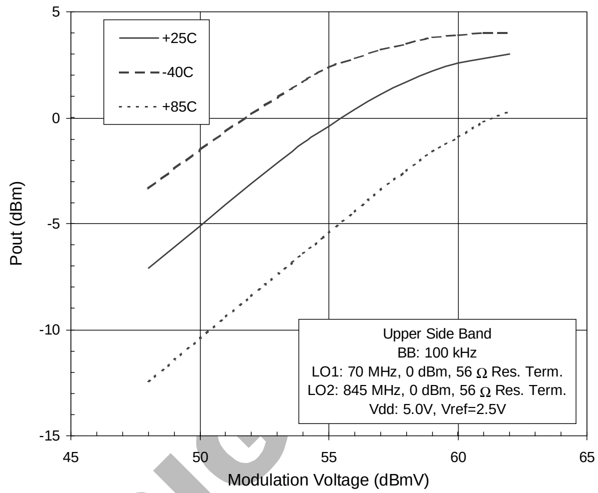




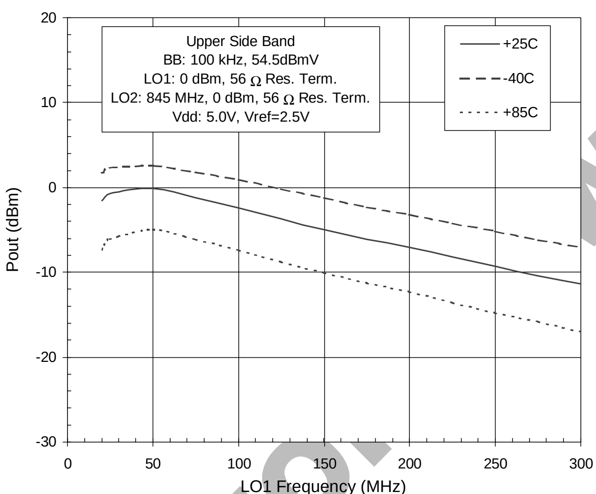
Pout vs. Baseband Modulation Frequency



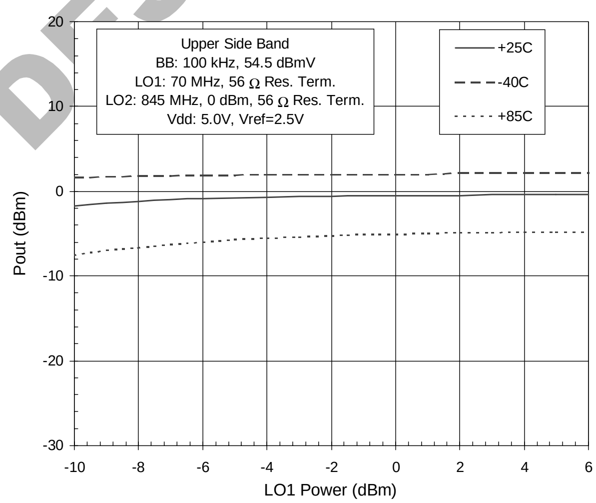
Pout vs. Baseband Modulation Voltage



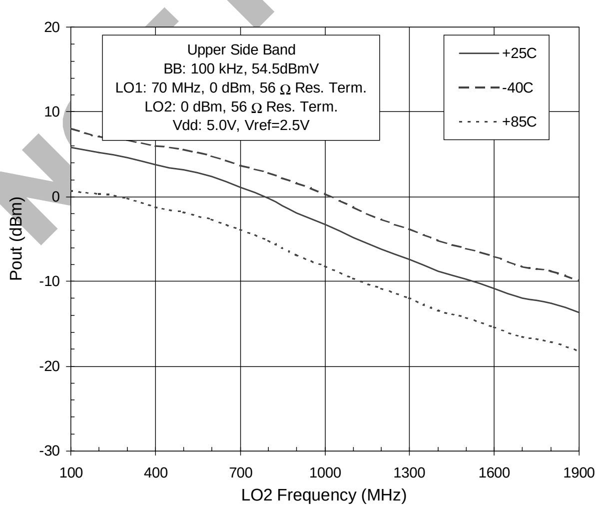
Pout vs. LO1 Frequency



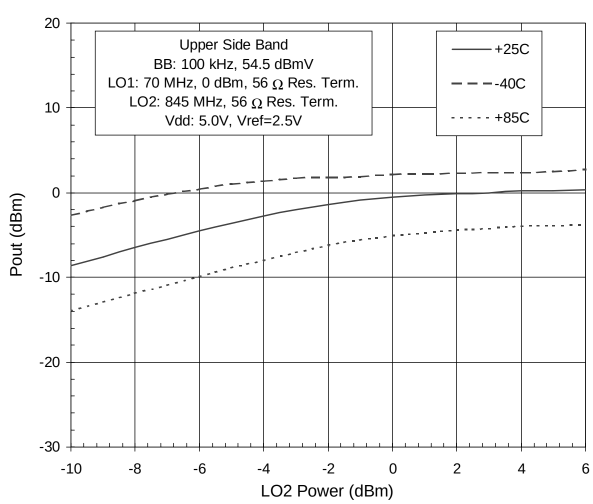
Pout vs. LO1 Power



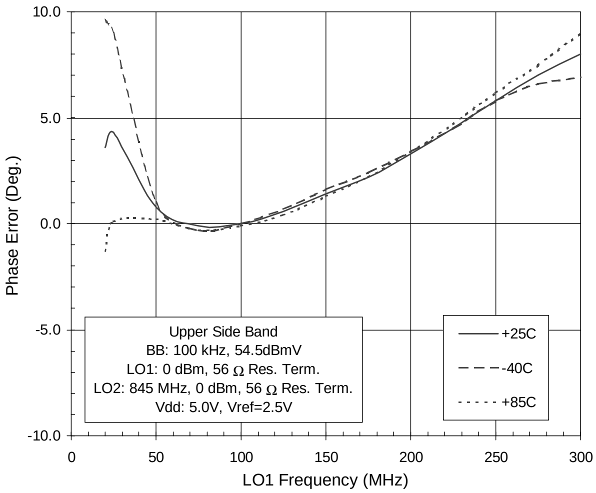
Pout vs. LO2 Frequency



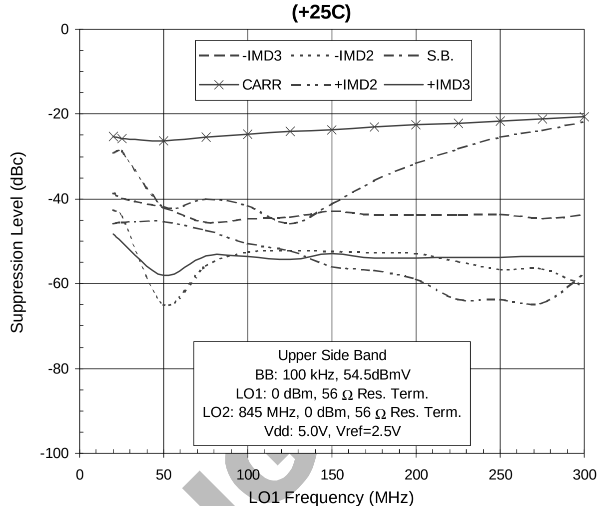
Pout vs. LO2 Power



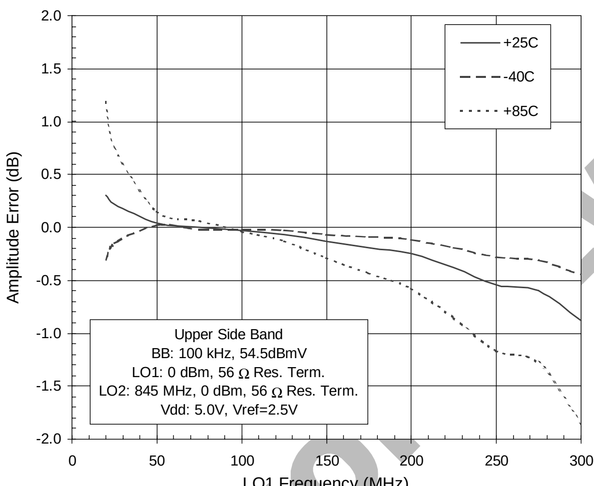
Phase Error vs. LO1 Frequency



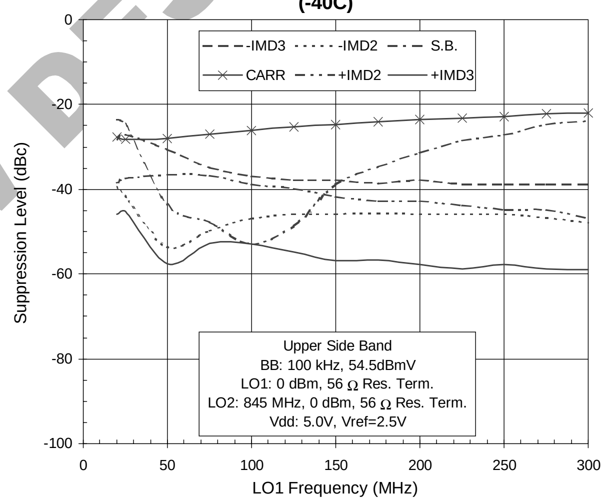
Suppression Levels vs. LO1 Frequency (+25C)



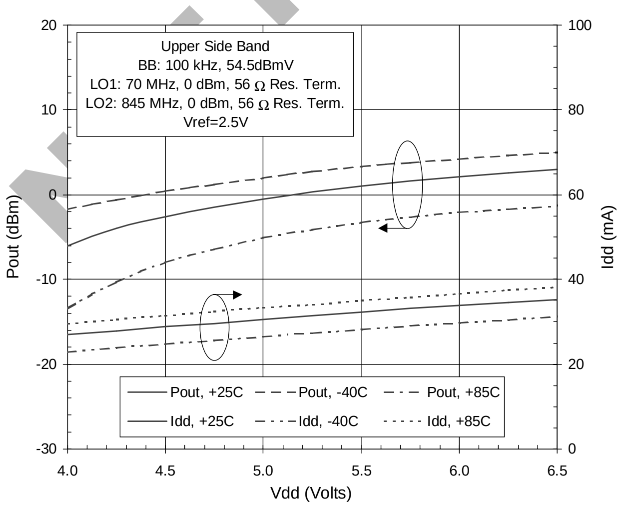
Amplitude Error vs. LO1 Frequency



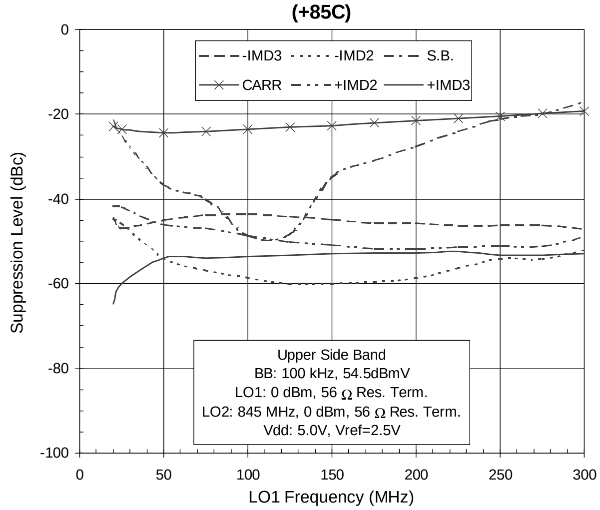
Suppression Levels vs. LO1 Frequency (-40C)



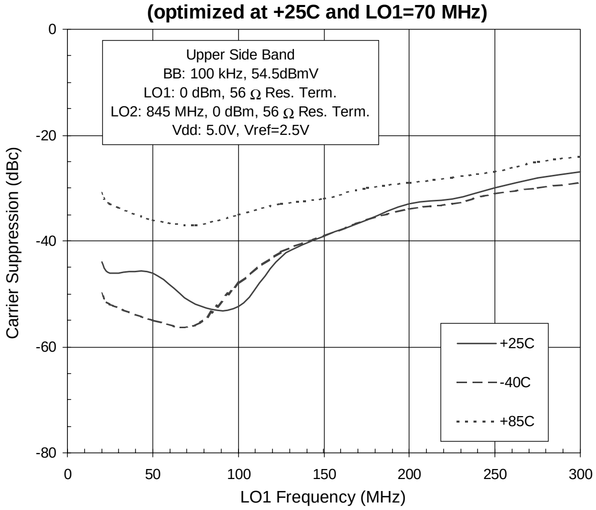
Pout and Idd vs. Vdd



Suppression Levels vs. LO1 Frequency (+85C)



Optimized Carrier Suppression vs. LO1 Frequency (optimized at +25C and LO1=70 MHz)



Optimized Sideband Suppression vs. LO1 Frequency (optimized at +25C and LO1=70 MHz)