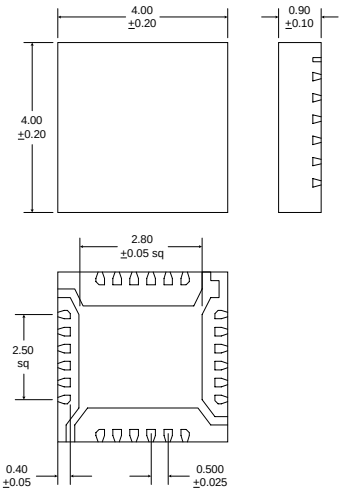
W-CDMA RECEIVE AGC AND DEMODULATOR

Typical Applications

- W-CDMA Systems

Product Description

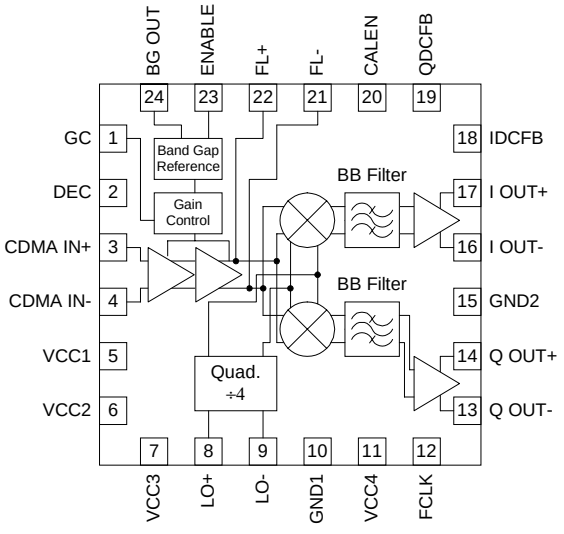
The RF2679 is an integrated complete IF AGC amplifier and Quadrature Demodulator designed for the receive section of W-CDMA applications. It is designed to amplify received IF signals, while providing 60dB of gain control range, a total of 90dB gain, and demodulate to baseband I and Q signals. This circuit is designed as part of RFMD's single-mode W-CDMA Chipset, which also includes the RF2678 W-CDMA Transmit Modulator and IF AGC. The IC is manufactured on an advanced 25GHz F_T Silicon Bi-CMOS process, and is packaged in a 4mmx4mm LPCC-24.



Package Style: LPCC-24

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☑ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Digitally Controlled Power Down Mode
- 2.7V to 3.3V Operation
- Digital LO Quadrature Divide-by-4
- IF AGC Amp with 70dB Gain Control
- 85dB Maximum Voltage Gain

Ordering Information

RF2679	W-CDMA Receive AGC and Demodulator
RF2679 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA

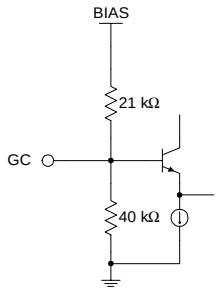
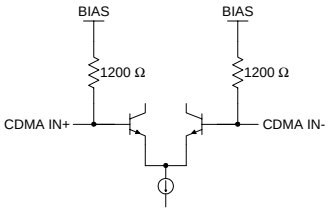
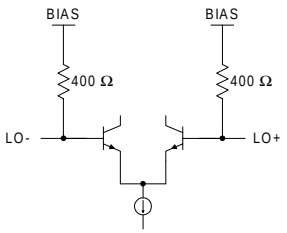
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

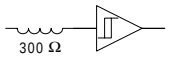
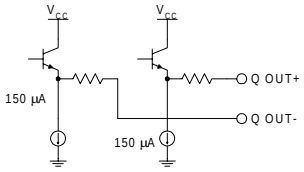
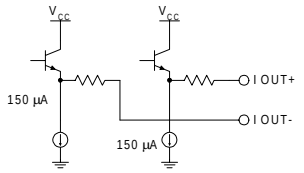
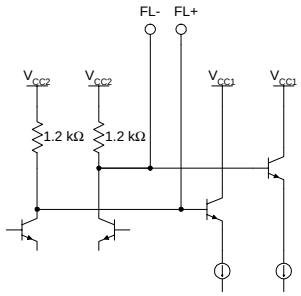
Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +5	V_{DC}
Power Down Voltage (V_{PD})	-0.5 to V_{CC}+0.7	V_{DC}
Input RF Power	+3	dBm
Ambient Operating Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

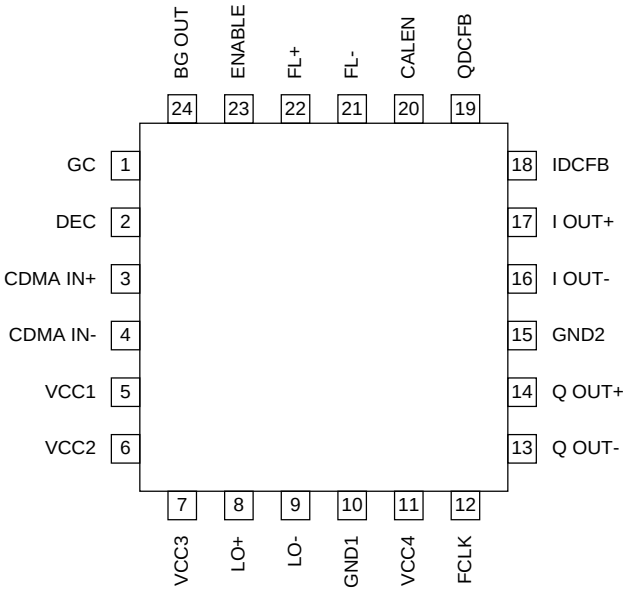
Caution! ESD sensitive device.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall (Cascaded)					T=25°C, V_{CC}=3.0V, Z_{LOAD}≅60kΩ, LO=760MHz @400mV$_{PP}$, IF Freq=191MHz, Z_S=500Ω
Maximum Gain		+85		dB	V_{GC}=2.4V, Balanced
Minimum Gain		+15		dB	V_{GC}=0.3V, Balanced
Gain Variation vs. V_{CC} and T	-3		+3	dB	V_{CC}=2.7V to 3.3V and T=-30°C to +85°C
Input IP3		-50		dBm	Maximum Gain
		-4		dBm	Minimum Gain
Noise Figure		5		dB	Maximum Gain
		45		dB	Minimum Gain
IF Input Frequency Range		190		MHz	
IF Input Impedance	2040	2400	2760	Ω	W-CDMA, Balanced
	1020	1200	1380	Ω	W-CDMA, Single Ended
I/Q Frequency Range		2.5		MHz	
I/Q Amplitude Balance		0.2		dB	
I/Q Phase Balance		1	5	deg	
Max I/Q Output Voltage	1			V_{PP}	Balanced, maximum output level, Z_{LOAD}≅60kΩ
I/Q DC Output		V_{CC}-1.3		V_{DC}	Common Mode
I/Q DC Offset		5	20	mV$_{DC}$	I OUT+ to I OUT-; QOUT+ to Q OUT-
Filter		f_C=2.5MHz± -250kHz			3rd order Butterworth after autocal FCLK=19.2MHz@100mVrms
LO Input Frequency Range		760		MHz	
LO Input Level		60 to 600		mV$_{PP}$	Balanced
LO Input Impedance	680	800	920	Ω	Balanced
	340	400	460	Ω	Single Ended
Power Supply					
Supply Voltage	2.7	3.0	3.3	V_{DC}	
Current Consumption		14.5		mA	
			10	µA	Sleep Mode (ENABLE≤0.5V)

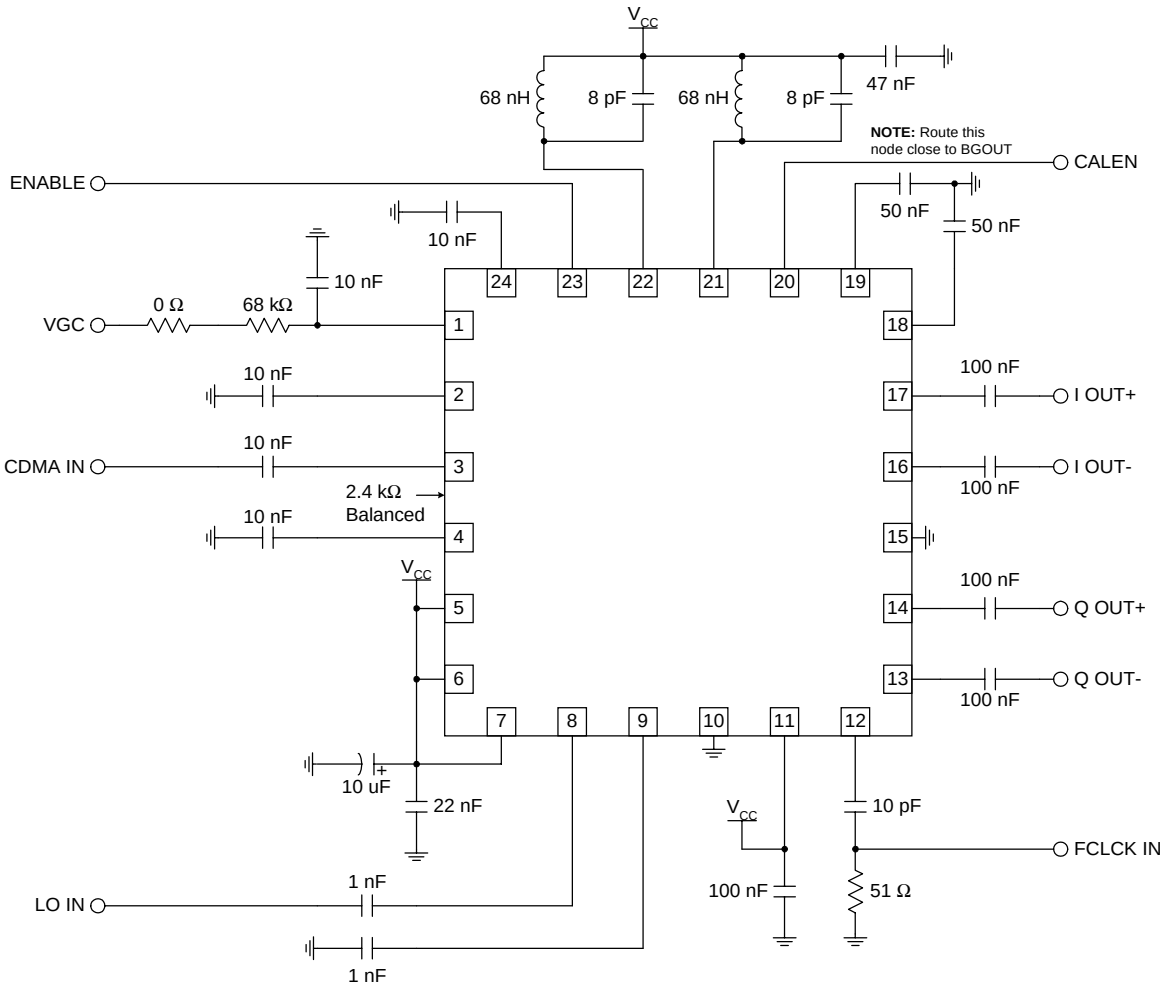
Pin	Function	Description	Interface Schematic
1	GC	Analog Gain Control for AGC Amplifiers. The valid control range is from 0.3 to 2.4V_{DC}. These voltages are valid for ONLY a 68kΩ source impedance. The gain range for the AGC is 60dB.	
2	DEC	AGC decoupling pin. An external bypass capacitor of 10nF capacitor is required. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane.	
3	WCDMA IN+	W-CDMA Balanced Input pin. This pin is internally DC biased and should be DC blocked if connected to a device with a DC level present. For single-ended input operation, one pin is used as an input and the other W-CDMA input is AC coupled to ground. The balanced input impedance is 2.4kΩ, while the single-ended input impedance is 1.2kΩ.	
4	WCDMA IN-	Same as pin 4, except complimentary input.	See pin 3.
5	VCC1	Supply voltage for the AGC input stage, band gap and gain control bias circuitry. This pin may be connected in parallel with pins 6 and 7. It should be bypassed by a 22nF capacitor. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane. The part is designed to work from a 2.7V to 3.3V supply.	
6	VCC2	Supply voltage for the bandgap, gain control bias circuitry, and AGC stages 2 and 3. This pin may be connected in parallel with pins 5 and 7. It should be bypassed by a 22nF capacitor. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane. The part is designed to work from a 2.7V to 3.3V supply.	
7	VCC3	Supply voltage for the LO divider and limiting amp. This pin may be connected in parallel with pins 5 and 6. It should be bypassed by a 22nF capacitor. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane. The part is designed to work from a 2.7V to 3.3V supply.	
8	LO+	Same as pin 12, except complementary input.	See pin 9.
9	LO-	LO Balanced Input pin. This pin is internally DC biased and should be DC blocked if connected to a device with DC present. For single-ended input operation, one pin is used as an input and the other LO input is AC coupled to ground. The frequency of the signal applied to these pins is internally divided by a factor of 4, hence the carrier frequency for the modulator becomes one fourth of the applied frequency. The single-ended input impedance is 400Ω (balanced is 800Ω). The LO input may be driven single-ended but balanced provides optimum gain and phase balance.	
10	GND1	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
11	VCC4	Supply voltage for the baseband stage. This pin should be bypassed by a 100nF capacitor.	

Pin	Function	Description	Interface Schematic
12	FCLK	Reference clock for base band filters.	
13	Q OUT-	Balanced Baseband Output of Q Mixer. This pin is internally DC biased and should be DC blocked externally. The output can be used in a single-ended configuration by leaving one of the two pins unconnected, however half the output voltage will be lost.	
14	Q OUT+	Same as pin 13, except complementary output.	See pin 13.
15	GND2	Ground connection for the baseband stage.	
16	I OUT-	Same as pin 17, except complementary output.	See pin 17.
17	I OUT+	Balanced Baseband Output of I Mixer. This pin is internally DC biased and should be DC blocked externally. The output can be used in a single-ended configuration by leaving one of the two pins unconnected, however half the output voltage will be lost.	
18	IDCFB	DC feedback capacitor for in-phase channel.	
19	QDCFB	DC feedback capacitor for quadrature channel.	
20	CALEN	Calibration enable for BB filters. Calibration is performed when CALEN goes high. The calibration takes approximately 100µs, consumes 0.5mA, and is totally independent of the ENABLE pin. Once calibration is complete, the calibration word is stored and the calibration circuit is disabled. If the CALEN pin goes low of V_{CC} is disabled, then the calibration word is lost and the IC needs recalibration.	
21	FL-	Balanced AGC Output/Demod Input. This balanced node is pinned out to allow shunt filtering of the AGC output signal as it enters the demodulator. The basic configuration of the filter should consist of a shunt inductor and shunt capacitor, both connected to the power supply, as the internal circuitry requires this power supply connection through the inductor to operate.	
22	FL+	Same as pin 21, except complementary.	See pin 21.
23	ENABLE	Power Down Control. When logic “high” (≥V_{CC}-0.3V), all circuits are operating; when logic “low” (≤0.5V), all circuits are turned off.	
24	BG OUT	Bandgap Voltage Reference. This voltage, constant over temperature and supply variation, is used to bias internal circuits. A 10nF external bypass capacitor is required. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane.	

Pin-Out


BG OUT
ENABLE
FL+
FL-
CALEN
QDCFB
24
23
22
21
20
19
GC 1
DEC 2
CDMA IN+ 3
CDMA IN- 4
VCC1 5
VCC2 6
18 IDCFB
17 I OUT+
16 I OUT-
15 GND2
14 Q OUT+
13 Q OUT-
7
8
9
10
11
12
VCC3
LO+
LO-
GND1
VCC4
FCLK

Application Schematic



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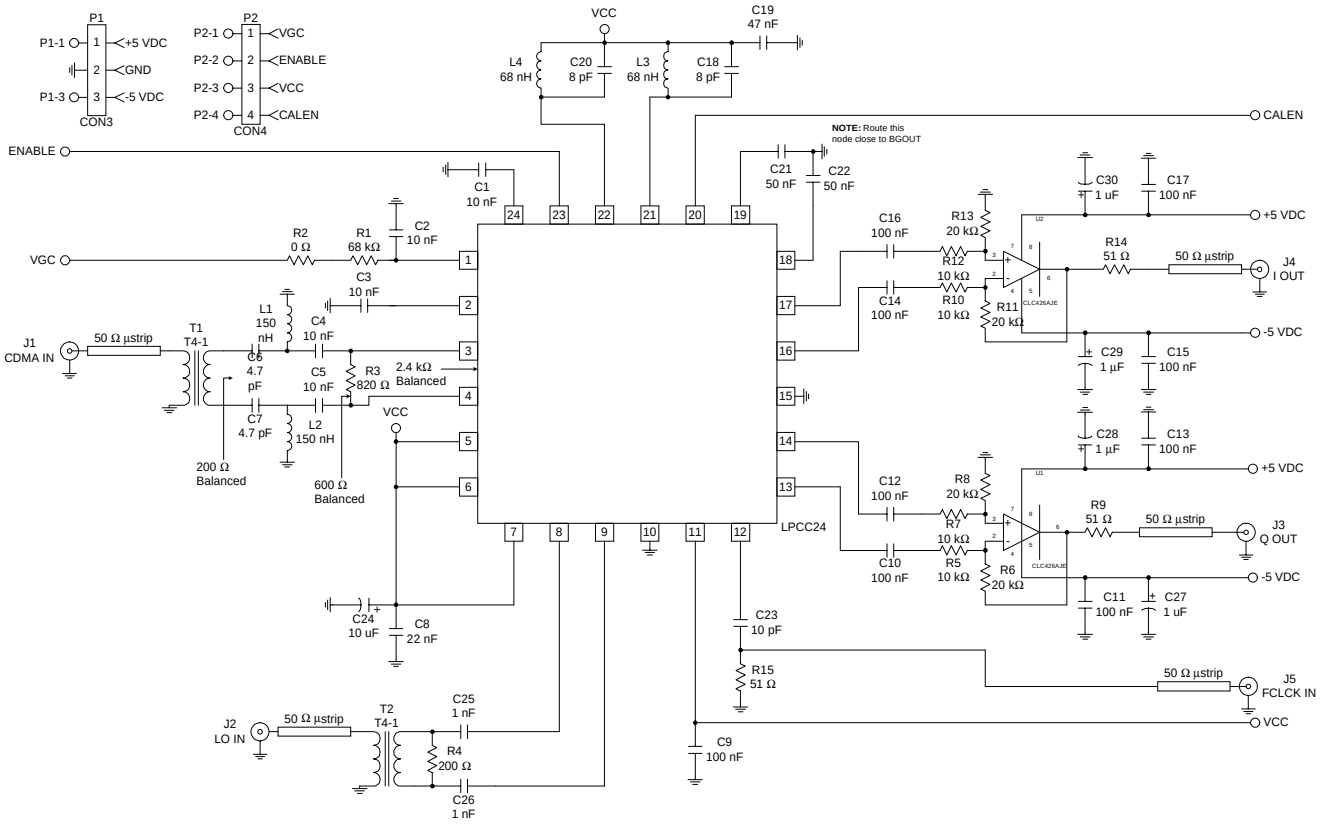
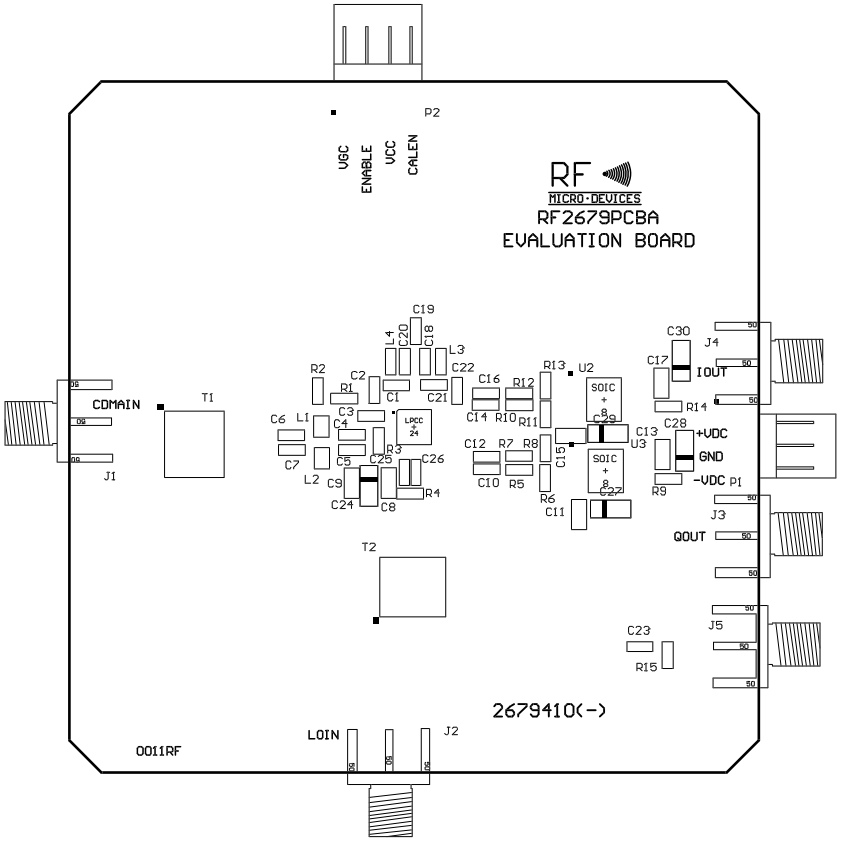
QUADRATURE DEMODULATORS

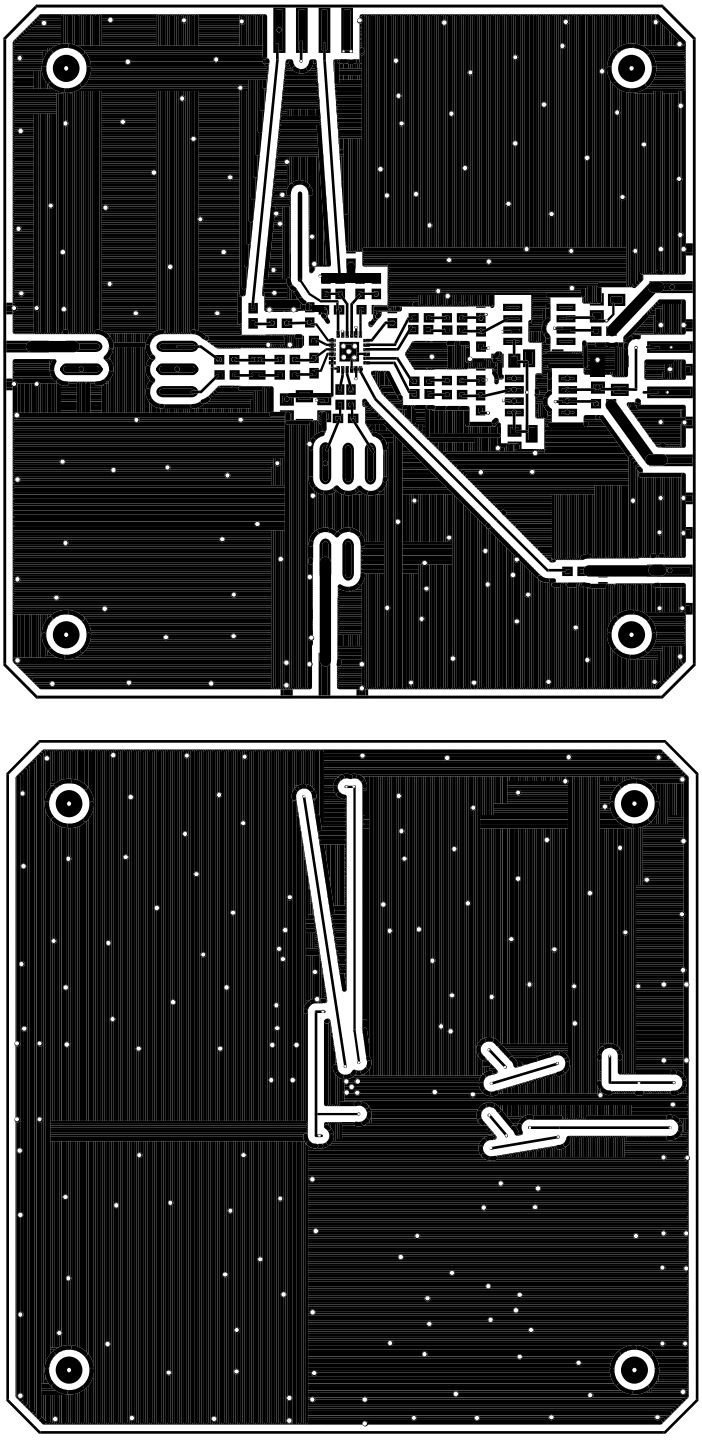
Evaluation Board Schematic

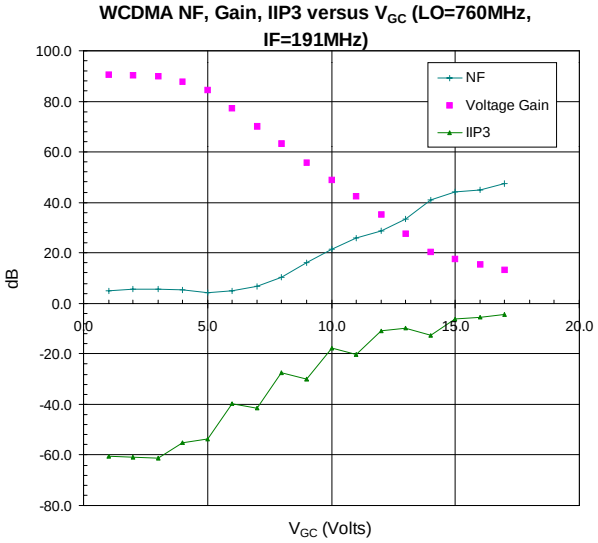
(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
Board Size 3.050” x 3.050”
Board Thickness 0.031”, Board Material FR-4






WCDMA NF, Gain, IIP3 versus V_{GC} (LO=760MHz, IF=191MHz)
NF
Voltage Gain
IIP3
dB
100.0
80.0
60.0
40.0
20.0
0.0
-20.0
-40.0
-60.0
-80.0
0.0
5.0
10.0
15.0
20.0
V_{GC} (Volts)