

12A, 60V, 0.150 Ohm, N-Channel Power MOSFETs

These are N-Channel enhancement mode silicon gate power field effect transistors. They are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA49082.

Ordering Information

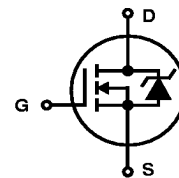
PART NUMBER	PACKAGE	BRAND
RFD3055	TO-251AA	FD3055
RFD3055SM	TO-252AA	FD3055
RFP3055	TO-220AB	FP3055

NOTE: When ordering, use the entire part number. Add the suffix 9A, to obtain the TO-252AA variant in tape and reel, i.e. RFD3055SM9A.

Features

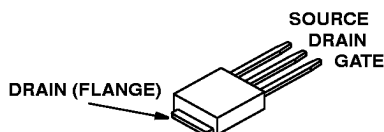
- 12A, 60V
- $r_{DS(ON)} = 0.150\Omega$
- Temperature Compensating PSPICE® Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- 175°C Operating Temperature
- Related Literature
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol

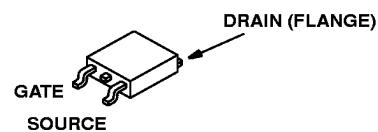


Packaging

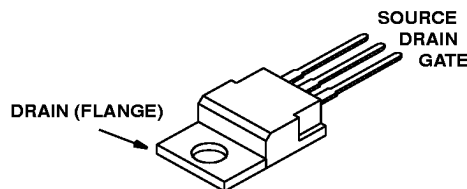
JEDEC TO-251AA



JEDEC TO-252AA



JEDEC TO-220AB



Absolute Maximum Ratings $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

	RFD3055, RFD3055SM, RFP3055	UNITS
Drain to Source Voltage (Note 1)	V_{DSS} 60	V
Drain to Gate Voltage ($R_{GS} = 20\text{K}\Omega$) (Note 1)	V_{DGR} 60	V
Gate to Source Voltage	V_{GS} ± 20	V
Continuous Drain Current	I_D 12	A
Pulsed Drain Current (Note 3)	I_{DM} Refer to Peak Current Curve	A
Single Pulse Avalanche Rating (Figures 14, 15)	I_{AS} Refer to UIS Curve	
Power Dissipation	P_D 53	W
Linear Derating Factor	0.357	W/ $^{\circ}\text{C}$
Operating and Storage Temperature	T_J, T_{STG} -55 to 175	$^{\circ}\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s.	T_L 300	$^{\circ}\text{C}$
Package Body for 10s, See Techbrief 334	T_{pkg} 260	$^{\circ}\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^{\circ}\text{C}$ to 150°C .

Electrical Specifications $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0V (Figure 11)		60	-	-	V
Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250μA (Figure 10)		2	-	4	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = Rated BV _{DSS} , V _{GS} = 0V		-	-	1	μA
		T _C = 125°C, V _{DS} = 0.8 x Rated BV _{DSS}		-	-	25	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20V		-	-	100	nA
Drain to Source On Resistance	r _{DS(ON)}	I _D = 12A, V _{GS} = 10V (Figure 9) (Note 2)		-	-	0.150	Ω
Turn-On Time	t _{ON}	V _{DD} = 30V, I _D = 12A R _L = 2.5Ω, V _{GS} = +10V R _G = 10Ω (Figure 13)		-	-	40	ns
Turn-On Delay Time	t _{d(ON)}			-	7	-	ns
Rise Time	t _r			-	21	-	ns
Turn-Off Delay Time	t _{d(OFF)}			-	16	-	ns
Fall Time	t _f			-	10	-	ns
Turn-Off Time	t _{OFF}			-	-	40	ns
Total Gate Charge	Q _{g(TOT)}	V _{GS} = 0 to 20V	V _{DD} = 48V, I _D = 12A, R _L = 4Ω, I _{g(REF)} = 0.24mA (Figure 13)	-	19	23	nC
Gate Charge at 10V	Q _{g(10)}	V _{GS} = 0 to 10V		-	10	12	nC
Threshold Gate Charge	Q _{g(TH)}	V _{GS} = 0 to 2V		-	0.6	0.8	nC
Input Capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz (Figure 12)		-	300	-	pF
Output Capacitance	C _{OSS}			-	100	-	pF
Reverse Transfer Capacitance	C _{RSS}			-	30	-	pF
Thermal Resistance Junction to Case	R _{θJC}			-	-	2.8	°C/W
Thermal Resistance Junction to Ambient	R _{θJA}	TO-251 and TO-252		-	-	100	°C/W
		TO-220		-	-	62.5	°C/W

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 12\text{A}$	-	-	1.5	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 12\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	100	ns

NOTES:

2. Pulse Test: Pulse Width $\leq 300\text{ms}$, Duty Cycle $\leq 2\%$.
3. Repetitive Rating: Pulse Width limited by max junction temperature. See Transient Thermal Impedance Curve (Figure 3) and Peak Current Capability Curve (Figure 5).

Typical Performance Curves Unless Otherwise Specified

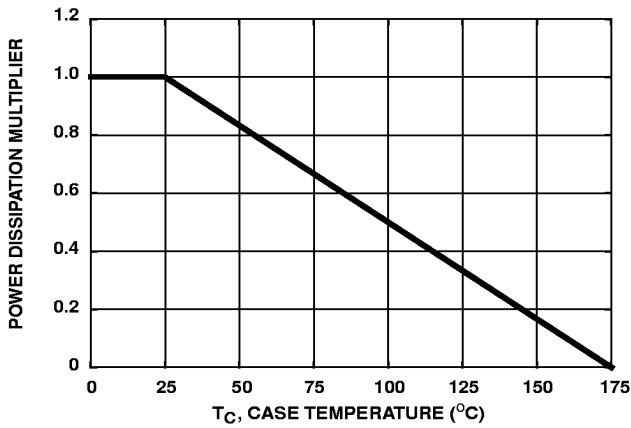


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

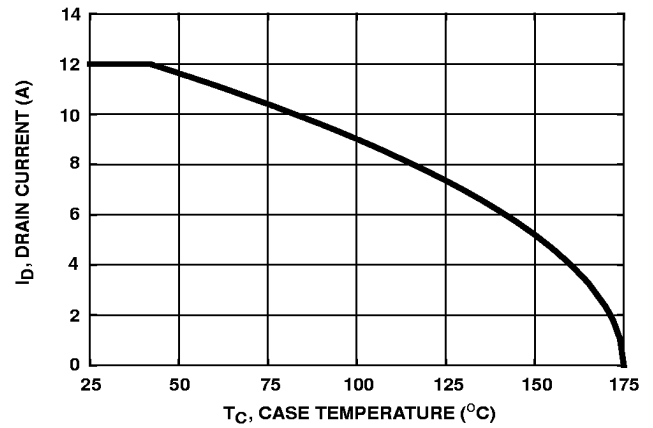


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

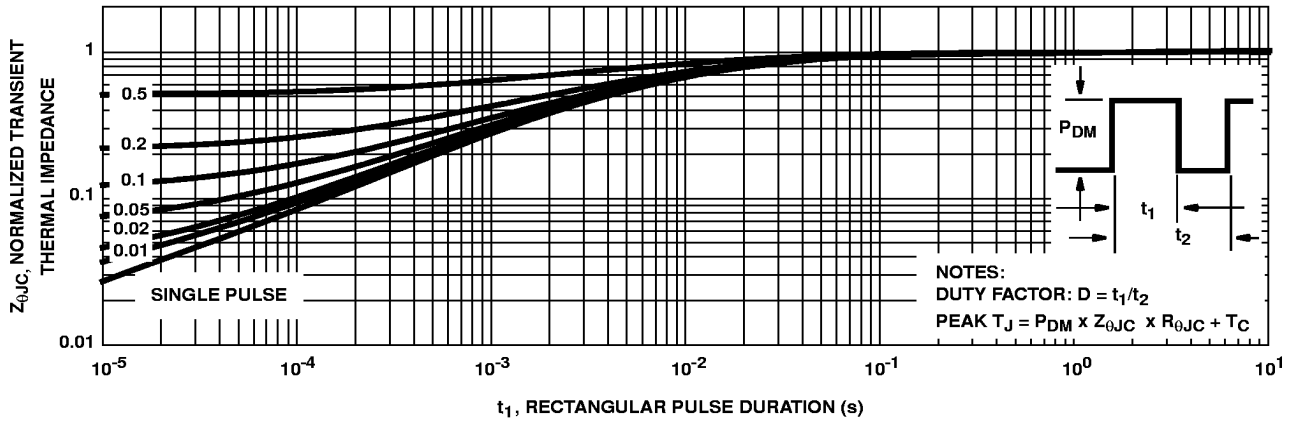


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

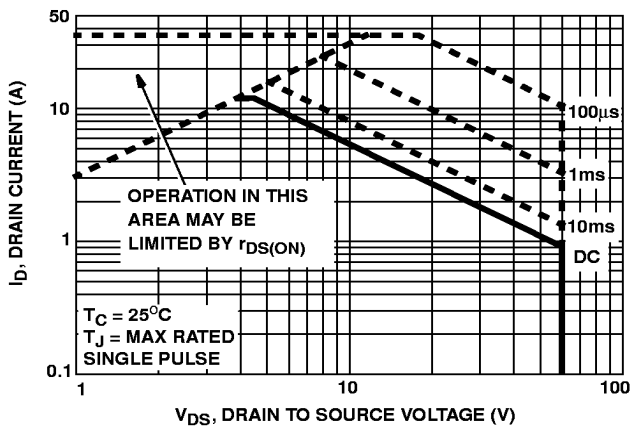


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

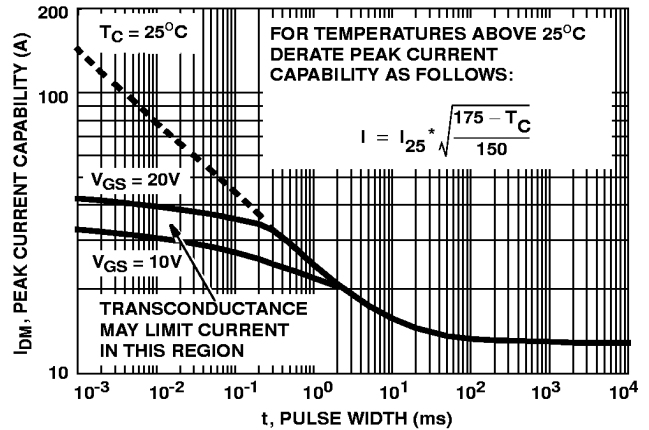


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves Unless Otherwise Specified (Continued)

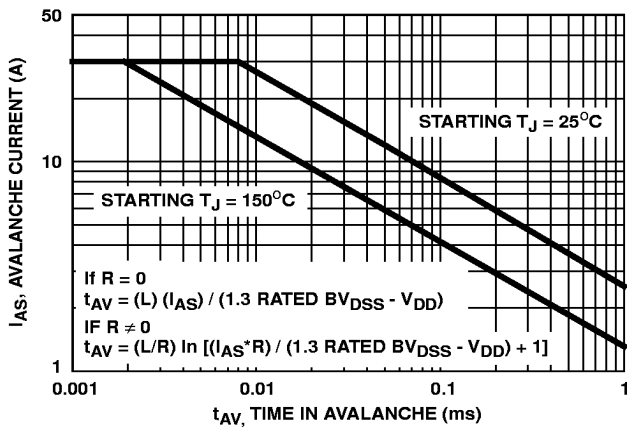


FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING

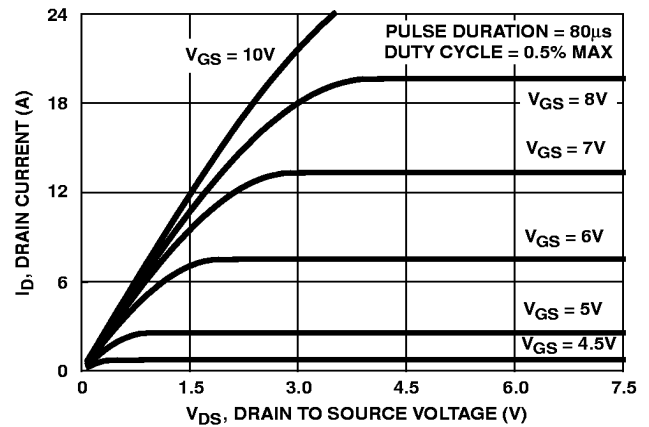


FIGURE 7. SATURATION CHARACTERISTICS

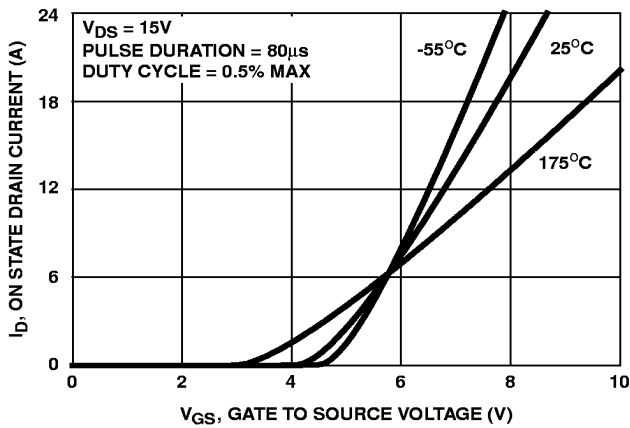


FIGURE 8. TRANSFER CHARACTERISTICS

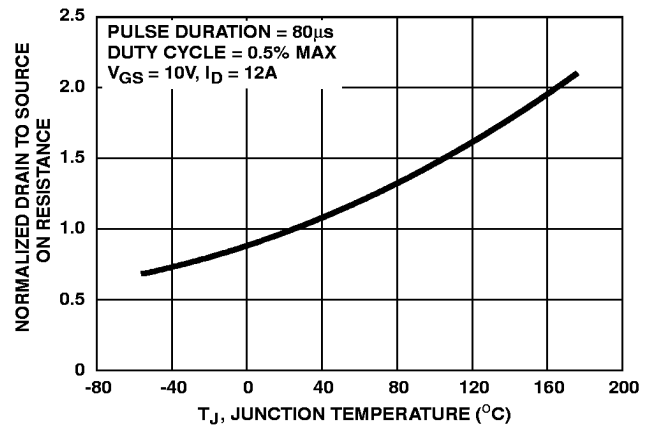


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

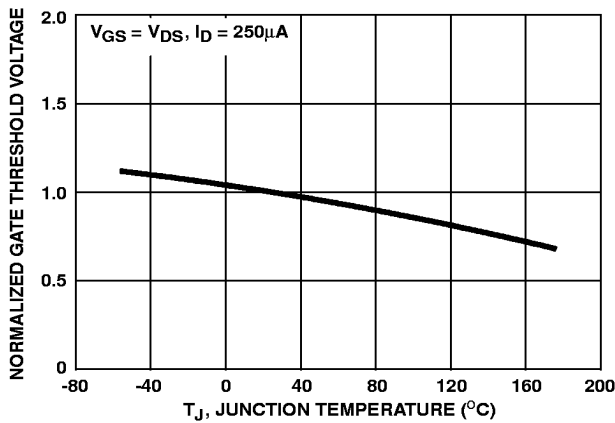


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

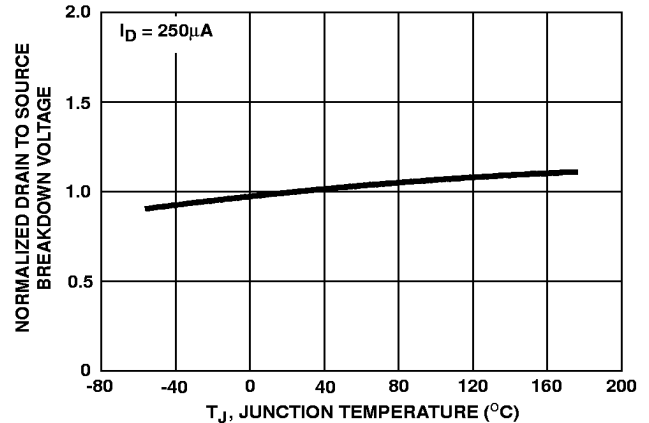


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

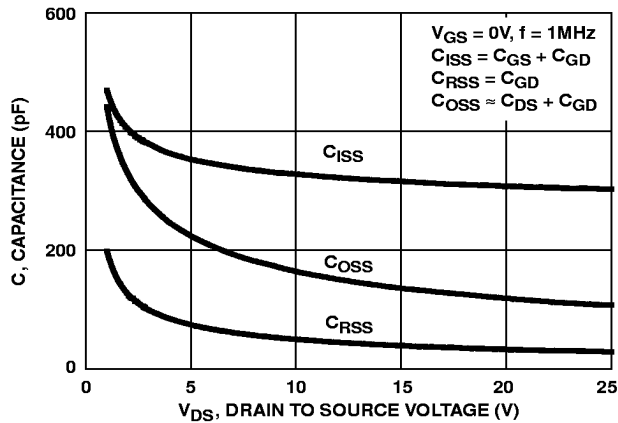
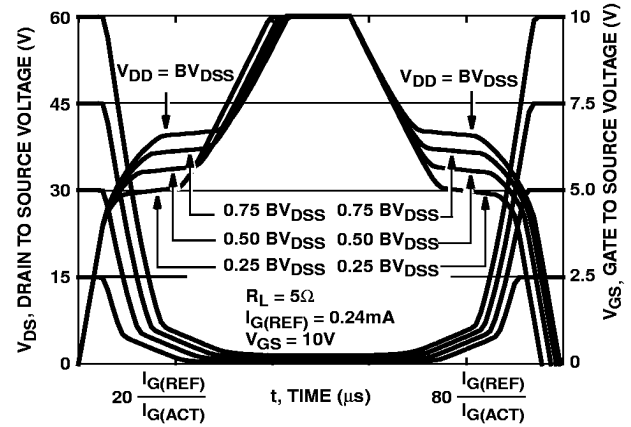


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Harris Application Notes AN7254 and AN7260.

FIGURE 13. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

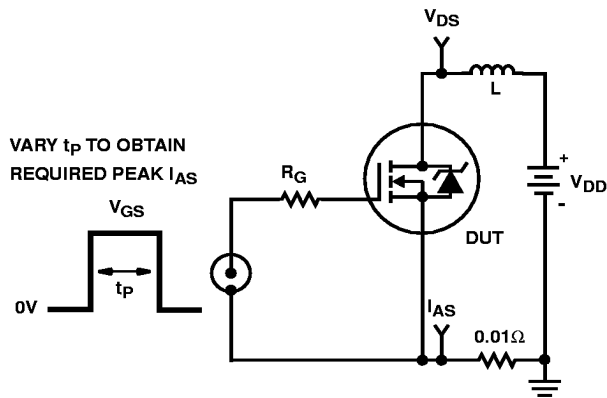


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

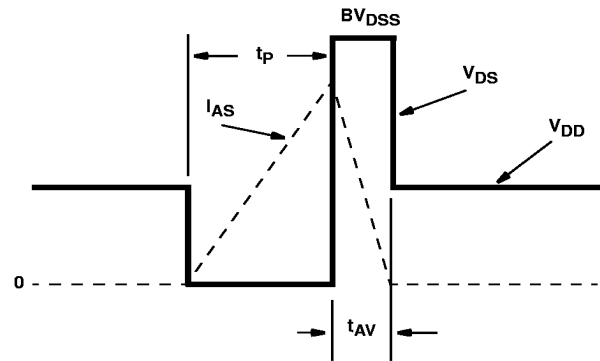


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

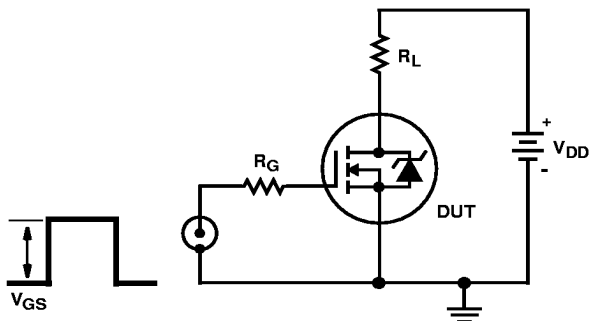


FIGURE 16. SWITCHING TIME TEST CIRCUIT

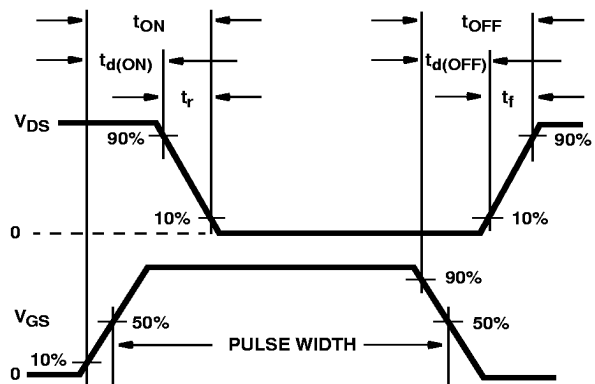


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Test Circuits and Waveforms (Continued)

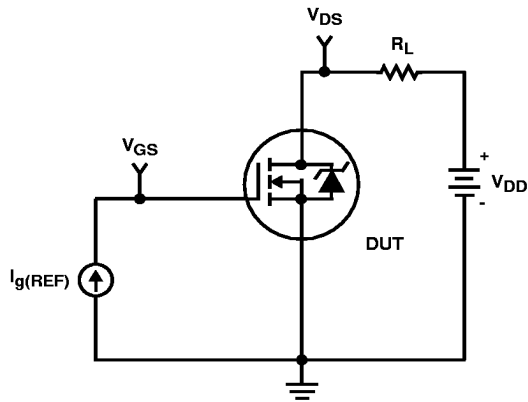


FIGURE 18. GATE CHARGE TEST CIRCUIT

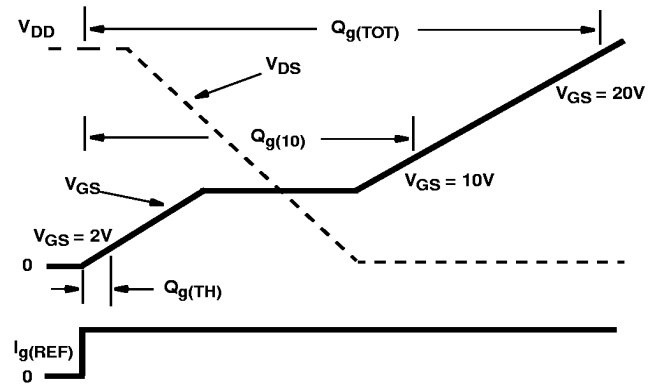


FIGURE 19. GATE CHARGE WAVEFORMS

PSPICE Electrical Model

.SUBCKT RFP3055 2 1 3; rev 10/26/93

CA 12 8 0.540e-9

CB 15 14 0.540e-9

CIN 6 8 0.300e-9

DBODY 7 5 DBDMOD

DBREAK 5 11 DBKMOD

DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 67.9

EDS 14 8 5 8 1

EGS 13 8 6 8 1

ESG 6 10 6 8 1

EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1e-9

LGATE 1 9 4.61e-9

LSOURCE 3 7 4.61e-9

MOS1 16 6 8 8 MOSMOD M=0.99

MOS2 16 21 8 8 MOSMOD M=0.01

RBREAK 17 18 RBKMOD 1

RDRAIN 50 16 RDSMOD 1e-4

RGATE 9 20 7.23

RIN 6 8 1e9

RSCL1 5 51 RSLVCMOD 1e-6

RSCL2 5 50 1e3

RSOURCE 8 7 RDSMOD 108e-3

RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD

S1B 13 12 13 8 S1BMOD

S2A 6 15 14 13 S2AMOD

S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1

VTO 21 6 0.5

ESCL 51 50 VALUE={ (V(5,51)/ABS(V(5,51))) * (PWR(V(5,51)) * 1e6 / 30,6.5) }

.MODEL DBDMOD D (IS=4.33e-14 RS=2.78e-2 TRS1=1.10e-3 TRS2=5.19e-6 CJO=3.94e-10 TT=7.63e-8)

.MODEL DBKMOD D (RS=0.676 TRS1=1.94e-3 TRS2=-1.09e-6)

.MODEL DPLCAPMOD D (CJO=0.238e-9 IS=1e-30 N=10)

.MODEL MOSMOD NMOS (VTO=4.078 KP=12 IS=1e-30 N=10 TOX=1 L=1u W=1u)

.MODEL RBKMOD RES (TC1=1.06e-3 TC2=-1.92e-6)

.MODEL RDSMOD RES (TC1=5.03e-3 TC2=1.53e-5)

.MODEL RSLVCMOD RES (TC1=2.2e-3 TC2=-5e-6)

.MODEL RVTOMOD RES (TC1=-5.02e-3 TC2=-9.16e-6)

.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-6.5 VOFF=-3.5)

.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-3.5 VOFF=-6.5)

.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2.50 VOFF=2.50)

.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=2.50 VOFF=-2.50)

.ENDS

NOTE: For further discussion of the PSPICE model consult **A New PSPICE Sub-Circuit for the Power MOSFet Featuring Global Temperature Options**; authored by William J. Hepp and C. Frank Wheatley.

