Unifying RISC and DSP

Greater microprocessor versatility with a wide variety of built-in functions

Sophisticated RISC/DSP- technologies lower costs and increase performance.
The Hyperstone E1-32X represents a new class of microprocessors: The combination of a high performance RISC processor with an additional powerful DSP instruction set and on-chip micro-controller functions. The high throughput is not achieved by raw clock speed, but is due to a sophisticated architecture, which combines the advantages of RISC and DSP technology. It offers a powerful set of variable length instructions. Programs for the Hyperstone E1-32X require less than half the memory size of most RISC µPs. Most instructions execute within one clock cycle. The fast multiply unit at high clock frequency makes it one of the fastest CPUs on the market with regard to DSP functionality. For many applications, the Hyperstone E1-32X makes the use of additional DSP chips obsolete.

Load-Store Architecture

The Hyperstone RISC technology is based on a load-store architecture. It is register-oriented and built around a 32-bit wide register stack that holds general-purpose local registers and 26 global registers. Load and store instructions are pipelined to a depth of 2 stages at the memory bus.

Global Registers

The global registers include a Program Counter, Status Register, Stack Pointer, Upper Stack Bound, Bus Control registers, Timer registers and 14 general-purpose global registers.

Local Registers

The local registers are organized into a 64-word, circular register stack to hold function/subroutine stack frames. The stack crosses the register-memory boundary. Organized into stack frames of up to 16 words, the current frames are kept on-chip and are automatically pushed down to off-chip memory as the register stack fills up. Likewise, as the frames are popped off the stack, stack frames from memory are automatically passed to the on-chip stack.

Register Stack with Overlapping Frames

The current stack frame can overlap with the previous stack frame at a variable range to allow fast parameter passing. The overflow and underflow of the register stack is managed automatically, relieving the programmer of this task.

Variable-length instructions make program codes more compact.

The basic size of a Hyperstone instruction is a 16-bit halfword, however, the variable-length instructions can have up to three 16-bit halfwords. As a result, 32-bit constants and 32-bit native addresses are provided, thus making pre-instructions for generating longer addresses or constants obsolete.
These variable-length instructions provide a program code that is more compact compared to other RISC and CISC architectures.

Integrated Timers

The Hyperstone E1-32X has two hardware timers integrated with a common time base and a resolution of 1 µs.
The system timer is a general-purpose timer, which is strongly supported by Hyperstone's real-time operating system hyRTK. In combination with hyRTK, the Hyperstone E1-32X provides up to 31 virtual timers in stack-level tasks and up to 254 virtual timers in interrupt-level tasks. Depending on the work load of the CPU, the latency of these virtual timers is in the range of 1..5 µs. Programming of these timers is very easy because only the delay has to be defined. Very important is that none of these timers generates any overhead CPU cycles for pending time events. A processing overhead of approximately 1 µs is required only when a timer event occurs.
The other timer can be directly controlled by the user. The signals of this timer are directly accessible at one of the chip's I/O pins without any latency. It is synchronized to the clock. Among others, this timer is ideally suited for measuring pulse widths or generation of pulse sequences.

Interrupts

Interrupts can be caused by external interrupt signals, by the general-purpose timer interrupt, or by an I/O Control Mode. Interrupts do not require a task switch. An interrupt causes an interrupt-level task to be entered. This interrupt-level task runs on the stack of the current task executing, just a new stack frame is created. Therefore, a full context switch is avoided. The interrupt latency time is 0.1..0.2 µs when no other interrupt is presently being served.
Up to 7 priority-controlled external interrupt signals can be connected directly.

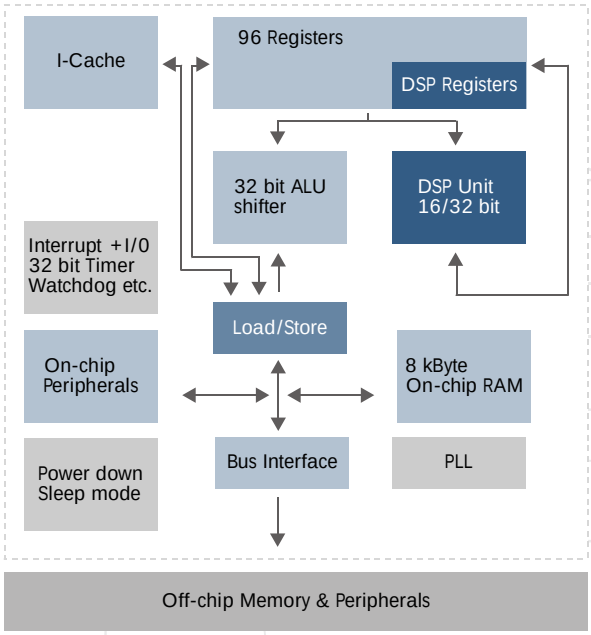
Shallow pipeline to accelerate branches plus an innovative instruction cache.
The Hyperstone's shallow, two-stage pipeline accelerates standard and delayed branches.
The innovative instruction cache provides automatic prefetch of instructions. This mechanism already loads the next instructions from memory into the cache, thus achieving the same high hit-rate as larger caches of other architectures.

Memory and I/O Address Spaces
The Hyperstone architecture provides separate memory and I/O address spaces.
The memory address space of 4 GByte in total is divided into four memory areas with separate bus timing and bus width. A DRAM controller is integrated for the first memory area. It uses the fast page mode of the DRAMs, thereby producing burst cycles automatically. Hence, no external logic is required to connect DRAMs or EDO RAMs. All memory areas can also be assigned to SRAM, (Flash-)EPROM or other memory devices, each with its own bus timing - and all without external logic.
Consequently, all memory devices can be directly connected pin-by-pin to Hyperstone microprocessors.
A portion of the memory address space is also used by a single-cycle 4-8 kByte on-chip RAM.
Hyperstone single-core RISC/DSP: ALU, DSP unit and load/store unit can work in parallel I/O devices are assigned to a separate I/O address space. Each I/O address has its own bus timing and virtually all peripheral components available on the market can be connected without external timing control logic.

A comprehensive on-chip bus interface.
The comprehensive on-chip bus interface includes memory control (refresh, RAS-CAS multiplexer, parity) as well as chip-select and R/W-signals. This makes system design with Hyperstone microprocessors very simple because no interface logic is required to connect memory or I/O.

On-chip DSP-features for demanding multimedia/telecom applications.
Up to now, separate DSPs and CPUs have been necessary for a number of applications, in particular for multimedia and telecom designs. Such applications can finally be realized through just one Hyperstone microprocessor because a DSP unit is already integrated into the architecture.

The DSP unit operates on the register set of the architecture in parallel to the ALU and load/store unit. It is executing a dedicated DSP instruction set. Like the other instructions, the DSP instructions are strictly following RISC-principles. During the latency cycles of DSP instructions the ALU and load/store unit can execute other instructions.
Thus, a much higher flexibility is achieved compared to conventional DSP implementations. Additionally, up to three operations per clock cycle can be executed. Therefore, a peak performance of up to 300 MOPS at 100 MHz can be achieved. The DSP unit gives support for 16-bit and 32-bit data types. In order to achieve highest data throughput the DSP unit provides dedicated result registers and a 32-bit hardware accumulator as well as a 64-bit hardware accumulator.
Among the dedicated DSP-type instructions are:
16-bit data format:
· multiply (single-cycle, pipelined)
· multiply-accumulate (single-cycle, pipelined)
· complex multiply
· complex multiply-accumulate
· addsub
· fixed-point shift
32-bit data format:
· multiply
· multiply-accumulate
· multiply-subtract

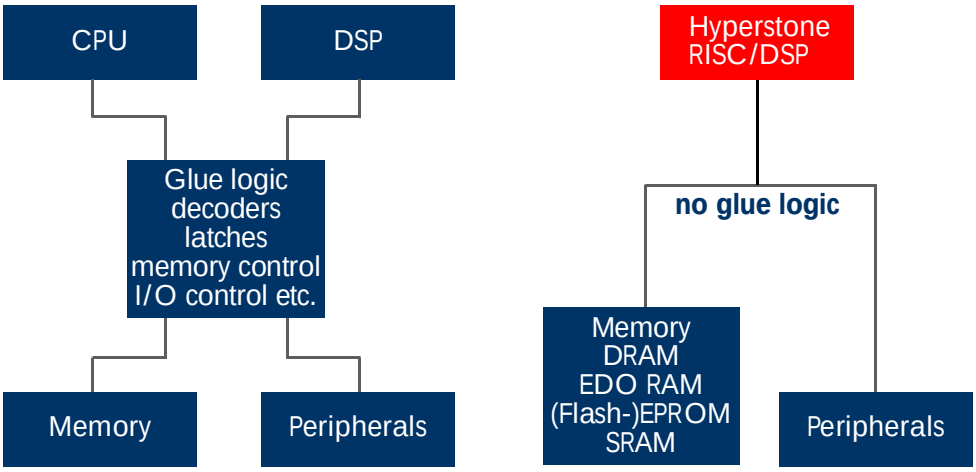


Hyperstone Architecture

Compact architecture and high performance give you a solid base for meeting or exceeding your project requirements Hyperstone E1-32X/E1-16X RISC/DSP

Compact design and low power consumption.
The Hyperstone's minimum transistor count results in a low power consumption of about 80 mW at 50 MHz (2.7 V) for the complete chip. An automatic power-down reduces power consumption even further in many applications. Due to the on-chip bus interface, total power consumption depends on the external load connected to the chip. The low power consumption makes very small packages possible.

Various Types
The Hyperstone E1-32X RISC/DSP family is available in various types. The external data bus-width is 32 bit and 16 bit for the E1-32X and E1-16 series, respectively. The package types for the E1-32X series are 144-pin TQFP (20 x 20 x 1.4mm) and 160-pin PQFP (28 x 28 x 3.4mm), whereas the E1-16X series comes in a very compact (14 x 14 x 1.4mm) 100-pin TQFP package. Each type has 8 kByte on-chip RAM and maximum clock rates of up to 80 MHz.



Hyperstone E1-32X/E1-16X RISC/DSP

- 32-bit RISC/DSP processor
- Parallelism of ALU, DSP unit and Load/Store unit
- 16, 32, 48-bit instructions
- 64 local, 26 global registers
- Local regs organized in circular register stack with stack frames
- 4 GByte memory address space
- Separate I/O address space
- 8 kByte RAM on-chip (1 cycle)
- On-chip instruction cache
- Separate address and data bus
- 32-bit timer and watchdog timer
- Comprehensive DRAM controller
- Programmable bus timing for all memory and I/O devices
- Clock frequency up to 80 MHz
- On-chip PLL (4:1)
- Static design
- 80 MIPS, up to 240 MOPS
- Up to 700 MIPS/Watt
- 1 k complex FFT in less than 0.5 ms
- 1 cycle MPY (16 x 16 bit)
- 4 cycle MPY (32 x 32 bit)
- 1 cycle multiply-add (pipelined)
- 1 cycle MOV, ADD, CMP, SHIFT
- 1 cycle DRAM read or write (pipelined)
- Glue-less memory- and I/O-connection
- 80 mW @ 50 MHz power dissipation
- Fully automatic power-down mode
- Clock-off function
- Operating Voltage: 2.4V...5V

Software and Hardware Development Tools

Whether starting a new project or looking for a more cost-effective solution to embedded systems problems, the hyperstone development tools meet all your needs. The development environment consists of both software and hardware. It provides all necessary components to develop an application.
They have been optimized over a number of years, resulting in a reliable set of tools. The major components are:
Programming Tools: C compiler, macro-assembler, linker with EPROM formatter, library manager, DSP Library.
Debugging Tools: Source-level debugger with profiler.
ANSI C Library: Full ANSI C run-time library.
Operating System: Multitasking real-time operating system.
Hardware: PC-based development boards and StarterKits are available.

System Requirements

To run the development tools, all what required is a PC with a full size-bit AT-bus slot and/or an RS232 serial interface (COM port) on the host PC.

C Compiler hyC

The optimizing C compiler hyC was specifically designed for use in embedded systems applications and accepts programs written in ANSI C and K&R C. The compiler performs optimizations related to Hyperstone microprocessors as well as all standard machine-independent optimizations. It also generates debugging information used by the hyDEBUG source-level debugger, thus providing true source- and system-level debugging and profiling.

Macro-Assembler hyMASM

The hyMASM Macro-Assembler is a two-pass assembler, which converts manually-generated assembler code or the code produced by the hyC compiler into relocatable object modules. These modules are then processed by the hyLINK Linker.

hyLINK Linker

hyLINK is an easy-to-use tool to create an executable file by combining a collection of object files and optionally one or more libraries. The resulting output file can either be loaded to a Hyperstone system or used to program EPROMs using the EPROM formatter. A sophisticated link control language provides flexibility in locating segments and in defining public symbols using C-like expressions and linker-specific functions.

hyLIB Librarian

The hyLIB librarian is used to manage a collection of object modules as a single library. It accelerates the linking process and helps to manage a large number of object modules. You can also add, delete, replace or extract object modules from a library.

hyDEBUG Source-Level Debugger

hyDEBUG allows complete source-level debugging of programs compiled by the hyC C compiler or the hyMASM macro-assembler. The window-oriented user-interface with pull-down menus, dialog-boxes and full mouse support simplifies debugging. hyDEBUG supports both machine-level and high-level debugging - including optimized C programs.

Complete hyperstone development tools help you accelerate your design tasks

Other features are single-step execution, complex conditional breakpoints, examination of machine registers and memory locations, plus examination of high-level data structures such as arrays, structures and bit fields.

Multitasking Debugging

In combination with the real-time operating system hyRTK, debugging of multiple tasks is supported by hyDEBUG.

Real-Time Debugging

Special breakpoints, called "active breakpoints" do not stop the program or task, but record "snapshots" of selected variables. When the program has been terminated, these snapshots are loaded to the host system that is running hyDEBUG. By taking advantage of these active break-points, you can trace your program close to real-time speed without expensive in-circuit emulators (ICE).

Software Profiler

The built-in software profiler is a performance analysis tool that locates heavily used sections of code. It helps you focus your attention on these particular areas so you can improve the performance of your application.

hyDSP Software Library

hyDSP is a collection of powerful DSP subprograms with ANSI C interfaces, optimally supported by the hyC ANSI C Compiler. The hyDSP Software Library offers programmers fast prototyping of DSP software and algorithms for the Hyperstone RISC/DSP processors.
hyDSP provides subroutines for the most important algorithms needed by DSP applications:

- Digital FIR Filtering
- Digital Adaptive FIR Filtering
- Digital IIR Filtering
- Fast Fourier Transformation
- Discrete Cosine Transformation
- Multidimensional Arithmetic
- Standard Functions
- Utility Functions

hyDSP offers a user-friendly, modular programming style without compromising performance. Software designers can do all programming in ANSI C, simply using the routines provided instead of time-consuming subroutines. hyDSP is constantly updated to provide programmers with the latest advances in DSP programming.

ANSI C Library

The C compiler hyC is equipped with a full ANSI C library with source code written in ANSI C and in assembler. Time-critical library functions are written in assembler and have been fine-tuned to match the capabilities of the Hyperstone architecture.

hyRTK Real-Time Operating System

The hyRTK real-time operating system is a multitasking operating system with pre-emptive task scheduling. It is specifically designed for use by Hyperstone microprocessors in embedded systems or board-level applications. Since hyRTK has been fine-tuned for the Hyperstone architecture, interrupt response times of approx. 0.1..0.2 µs can be achieved with a 80 MHz Hyperstone system. The complete operating system is less than 32 KB in size, including an integrated debug monitor and a floating-point library.
The debug monitor handles the commands of hyDEBUG running on the host PC.
hyRTK offers all the features of an up-to-date multitasking real-time system providing a wealth of functions including time management, task management, synchronization and interrupt services as well as message passing.

The main features of hyRTK are:

- Pre-emptive: Lower-priority tasks are preempted automatically by the highest-priority scheduled task
- Fast task context switching (ca. 2..3 µs)
- Low latency time for interrupts without context switch (0.1..0.2 µs)
- Precise timing functions with a resolution of 1 µs
- Fast execution of kernel functions (1..2 µs)
- Complete set of kernel functions on the finest granularity level provides extendibility via utilities for specific requirements
- User-friendly through novel, easy-to-handle task synchronization
- Static declaration of hyRTK resources guarantees deterministic behavior
- Automatic power-down mode without user program intervention
- Fully integrated debugging of programs running in real time

Development Board

In combination with the software tools, the Hyperstone development board provides the ideal hardware for developing Hyperstone applications. With this board you can evaluate Hyperstone microprocessors and start developing an own application on a real Hyperstone system.
The executable code of a program can either be downloaded to the board or directly programmed into the on-board Flash-EPROM. The application program is then executed on the development board under control of a debug monitor, following the commands of the hyDEBUG source-level debugger. Your own prototype hardware can easily be adapted using the I/O expansion connectors on the board.
The development board can either be operated via the AT-bus for rapid data transfer, or outside the PC, linked to the serial interface of the host PC using the hyICE Interface Control Extender.
The development board is equipped with up to 8 MB DRAM or EDO RAM, up to 512 KB fast SRAM and up to 512 KB Flash-EPROM containing the debug monitor firmware. In many cases, you can design your special application just as a subsystem of our development board.

Count on Hyperstone's fast and expert design support.
Our design support teams are standing by to help you achieve optimum performance for your hyperstone-based application. No matter where you are in your project, our support team can assist you at any stage in hardware as well as in software.
Our goal is your goal: an optimized combination of hardware and software in all cases.

Complete design services

Hyperstone is able to provide you with a complete design service for your projects. This includes ASICs and ASSPs tailored exactly for your requirements, board design, and complete system design according to your specifications. We are also standing by in defining how to complete your projects using our RISC/DSP technology.

Third-party Software

You will find a variety of software from third parties optimized for Hyperstone RISC/DSP processors, such as JPEG, TCP/IP, operating systems, web browsers, speech compression / decompression, communication software, and many more. Just ask us what kind of software you need. We are continuously extending our network of third-party software suppliers.

You will find Hyperstone partners throughout the world.

We are constantly working with our partner companies, licensees, second-source suppliers, distributors in all corners of the world to advance our technology and its applications. As a result, you can depend on receiving state-of-the-art microprocessors in any quantity you require, along with the responsive design support you need.

The Future

You can count on our continuous development of new compatible Hyperstone microprocessors, which are all based on the same basic hyperstone RISC/DSP architecture.
The next Hyperstone RISC/DSP, the Hyperstone E1-32XS, will be available in Q4/2000. It has an increased on-chip memory of 16 kByte and an complete design service on the ASIC-, board-, and system level plus responsive technical assistance all over the world - now and in the future.

Integrated interface to directly connect synchronous DRAMs (SDRAM IF).
According to market trends and technological developments, our chips will continue to be at the forefront of embedded RISC/DSP microprocessors. This gives you the option to easily upgrade your products with next-generation hyperstone RISC/DSP processors according to market demands.

Hyperstone AG, Am Seerhein 8, D-78467 Konstanz, Germany
Phone: +49 (07531) 98030 Fax: +49 (07531) 51725 Email: info@hyperstone.de
www.hyperstone-ag.com