EG&G RETICON

DE Series
Charge Coupled Linear Array

Introduction

The DE Series is a linear CCD sensor designed specifically for ease of system integration, wide spectral response applications, and ease of use. Its combination of single output with two or one and one-half phase operation make it ideal for high quality, cost effective image acquisition.

The imager configuration has a linear imaging array running parallel to a single readout register. This configuration allows the array to image one scene while reading out the previously imaged scene. Two-phase or one and one-half phase clocks are needed to drive the serial shift registers.

Note: While the DE Series has been designed to be resistant to electro-static discharge, ESD, damage, it still can be damaged from such discharges. Standard electronic ESD precautions should be observed when handling and storing this device.

Key Features

- Single high speed output
- 13 µm square pixels
- 3 poly buried channel process
- Data rates up to 20 MHz
- 700 Ke^- full well
- Sample and hold video output
- Wide spectral response (200 - 1000 nm)

General Description

The DE series features a linear Charge Coupled Device (CCD) with lengths of either 256, 512,1024, or 2048 picture elements (pixels). The DE Series offers a single output capable of data rates as high as 20 MHz. The readout register is located on one side of the imaging array and is optically shielded. All of the image data is simultaneously transferred from the imaging array to the readout register to be clocked out of the device. Immediately preceding the device output is an on-chip amplifier. A simplified schematic is shown in Figure 3. This design allows for accumulation of charge on a new line while the previous line is being readout.

Functional Description

Imaging Area

The imaging area is a linear array of 256, 512, 1024, or 2048 pixels. The pixel size is 13 µm x 13 µm. The total imaging area is shown in Figure 6. A special design in the imaging area stretches the wavelength absorption from the standard 400 - 1000 nm to 200 - 1000 nm. Typical spectral response as a function of wavelength is shown in Figure 2.

When the transfer gate is turned off, held low, and the pixel bias voltage of the sensing elements is held constant, an image

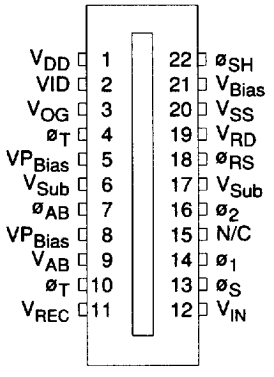

Figure 1. Pinout Configuration

impinged on the sensing area will create an electrical signal of the scene in the pixel potential wells.

The transfer gate øTG is provided at the interface of the imaging and readout registers for controlling charge flow. Charge flow is from each pixel of the imaging register into each ø1 gate of the readout register. The control function is performed by pulsing the transfer gate either high to permit or low to prevent the charge flow from the imaging register into the readout register for readout.

Horizontal Registers

There is a single horizontal readout shift register which is driven by two-phase clocks (ø1, ø2). The readout register receives charge from the imaging register and transfers the charge to the on-chip amplifier one pixel at a time. Immediately after this transfer a new integration period may begin.

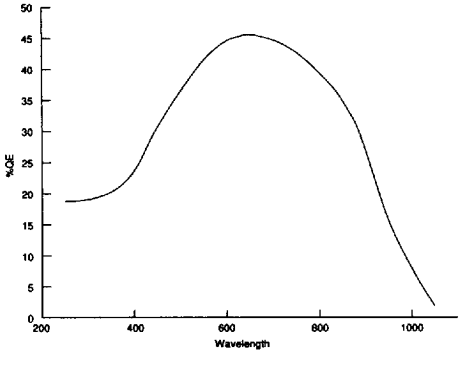

Figure 2. Typical Spectral Response at 1 MHz, 25°C

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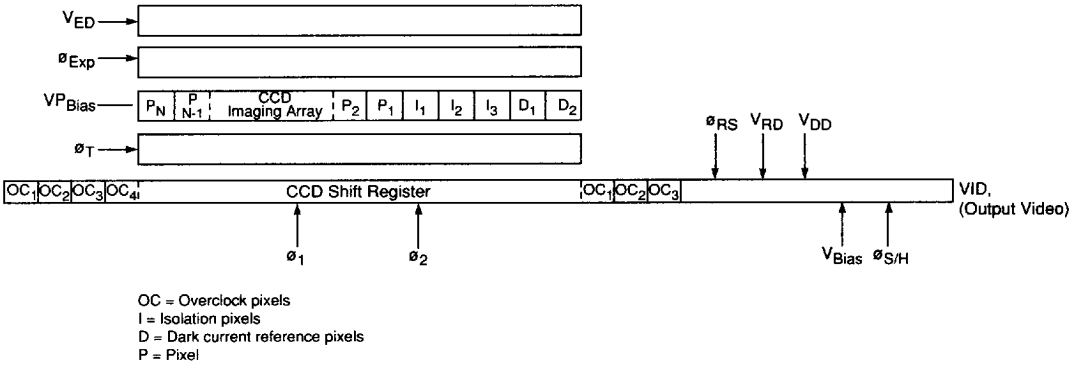


Figure 3. Simplified Schematic of the DE Series Linear Array

Output Amplifier

There is an on-chip amplifier associated with the output port. The video output amplifier has an output data rate of 20 MHz. Accordingly, the bandwidth is 60 MHz (-3 dB), referenced to a 10 pF load capacitance. The configuration is a cascade of two source followers with a combination of enhancement and depletion mode transistors. Non-linearity in these amplifiers is less than .1%. Full bandwidth operation can be achieved with a 12V biasing. At this bias value, the DC current is approximately 3 mA, resulting in a quiescent power dissipation of 36 mW.

A sample and hold circuit has been provided in the design, with provisions for optional use. This consists of a single depletion mode MOSFET between the two amplifier stages. Suppression of clocking feedthrough from the sample/hold clock is provided by an adjacent DC quiet gate. The sample and hold circuit is disabled by tying the sample clock to the high potential (VDD).

Antiblooming/Exposure Control

Under extremely high contrast conditions blooming control can be implemented. In this mode of operation, a bias voltage is required on the exposure/antiblooming drain. By adjusting the bias level on the exposure/antiblooming gate, excess charge present in a pixel is shunted to the exposure/antiblooming drain. Table 2 shows typical operating conditions of this bias. Another capability, when using this option, is as exposure control. The exposure is controlled by holding the exposure/antiblooming drain bias to the maximum level and clock the exposure/antiblooming gate. When this gate is on, the charge will be completely dumped out to the drain, and the integration will start when it is brought back to the off state (see Figure 4). The off level can be adjusted for antiblooming control.

Timing Requirements

The DE Series can be run using either standard two-phase clocks, or one and one-half phase clocks. For one-and-one-half phase clocking, $ø_2$ is held to a constant DC bias while $ø_1$ is clocked rail to rail. Both clocking schemes are shown in Figure 4.

Figure 4 also shows the timing of the reset, antiblooming/exposure control clock and transfer clocks. To achieve high transfer efficiency and high full well capacity in two-phase clocking, the serial clocks must overlap by more than 50%. In addition, the rise and fall times of the two-phase clocks should be more than 10 ns to prevent possible injection of spurious charge into the CCD channel.

The output amplifier is a gated charge integrator. In this output scheme, the output node (node A in Figure 5) is reset to the DC voltage (V_{RD}) which is applied to the drain of the reset transistor when the reset gate clock ($ø_{RS}$) is pulsed high to turn on the reset transistor.

When $ø_{RS}$ is low, the reset transistor is off and the signal charge is dumped to the capacitance of node A when ø1 goes low. The signal charge at node A is then measured as a voltage at the output of the three-stage amplifier which is operated in the source-follower configuration with an external resistance load. The signal is then sampled and the sensing node reset. The video output signal is also shown in Figure 4.

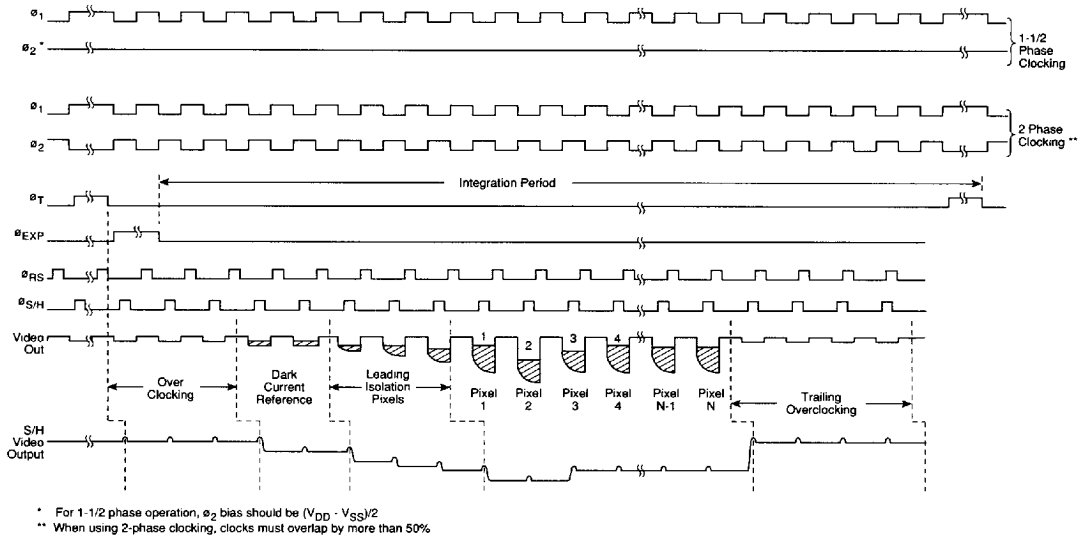
This timing is repeated the length of the array plus 12 (or more) times to allow the readout of one complete line of the image.

Electrical Input

It is recommended that the electrical input capability be disabled. In order to disable the electrical input, V_{IN} should be biased to V_{DD} and $ø_S$ and V_{REC} should be biased to V_{SS}.

Array Cooling

Both the dark current and the noise performance of the array can be improved by cooling. The dark current will be reduced 50% for every 7°C reduction in array temperature. The noise floor of the output amplifier is proportional to $(kTC)^{1/2}$ where k is Boltzmann's Constant, T is the array temperature in degrees Kelvin, and C is the output node capacitance of approximately .045 pF. Cooling can be achieved via a thermo-electric, Joule Thomson cooler, or liquid nitrogen dewar.



* For 1-1/2 phase operation, $ø_2$ bias should be $(V_{DD} - V_{SS})/2$
** When using 2-phase clocking, clocks must overlap by more than 50%

Figure 4. Timing Diagram

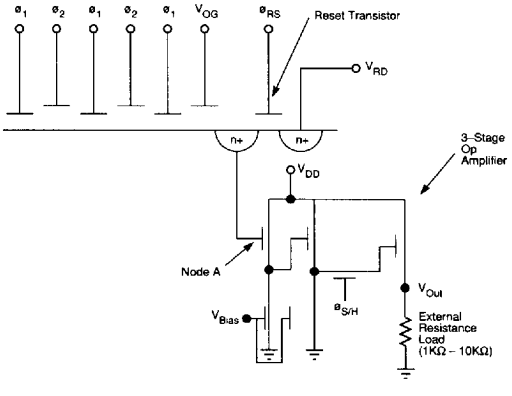


Figure 5. Output Charge Detection Circuitry (3-stage amp)

Specifications

Table 1 gives the pinout locations, Table 2 gives recommended operating conditions and Table 3 gives typical device specifications.

Table 1. Pinout Configuration

Pin #	Sym	Function
1	V_{DD}	Amplifier supply
2	VID	Output
3	V_{OG}	Output gate
4, 10	$ø_T$	Transfer gate
5	VP_{Bias}	Pixel bias
6, 17	V_{Sub}	Substrate
7	$ø_{AB}$	Exp/AB gate
8	VP_{Bias}	Pixel bias
9	V_{AB}	Exp/AB drain
11	N/C	No connection
12	N/C	No connection
13	N/C	No connection
14	$ø_1$	Phase 1 clock
15	N/C	No connection
16	$ø_2$	Phase 2 clock
18	$ø_{RS}$	Reset gate
19	V_{RD}	Reset drain
20	V_{SS}	Amplifier ground
21	V_{Bias}	Amplifier bias
22	$ø_{S/H}$	Sample and hold

Table 2. Operating Conditions

Parameter		Sym	Low	Typ	High	Units
Two-Phase Clocking						
Amplifier supply		V_{DD}	10	12	15	V DC
Amplifier ground		V_{SS}		0		
Amplifier bias		V_{Bias}	1.5	2.5	3.5	V DC
Output gate bias		VOG	3	5	6	V DC
Reset drain bias		V_{RD}		V_{DD}		V DC
Substrate bias		V_{Sub}	-2	0		V DC
Pixel bias		V_{PBias}	5	6	7	V DC
Readout clocks	High	$ø_{1H}$ - $ø_{2H}$		V_{DD}		V
	Low	$ø_{1L}$ - $ø_{2L}$		V_{SS}		V
Row transfer clocks	High	$ø_T$		V_{DD}		V
	Low			V_{SS}		V
Reset gate clock	High	$ø_{RG}$		V_{DD}		V
	Low			V_{SS}		V
Exp/AB gate clock	High	$ø_{AB}$		V_{DD}		V
	Low			V_{SS}		V
One and One-Half Phase Clocking						
Amplifier supply		V_{DD}	10	12	15	V DC
Amplifier ground		V_{SS}		0		
Amplifier bias		V_{Bias}	1.5	2.5	3.5	V DC
Output gate bias		V_{OG}	3	5	6	V DC
Reset drain bias		V_{RD}		V_{DD}		V DC
Substrate bias		V_{Sub}	-2	0		V DC
Pixel Bias		V_{PBias}	5	6	7	V DC
Readout clocks	High	$ø_{1H}$		V_{DD}		V
	Low	$ø_{1L}$		V_{SS}		V
	High	$ø_{2H}$		$(V_{DD}-V_{SS})/2$		V DC
	Low	$ø_{2L}$		$(V_{DD}-V_{SS})/2$		V DC
Row transfer clocks	High	$ø_T$		V_{DD}		V
	Low			V_{SS}		V
Reset gate clock	High	$ø_{RG}$		V_{DD}		V
	Low			V_{SS}		V
Exp/AB gate clock	High	$ø_{AB}$		V_{DD}		V
	Low			V_{SS}		V

Table 3. Device Specifications

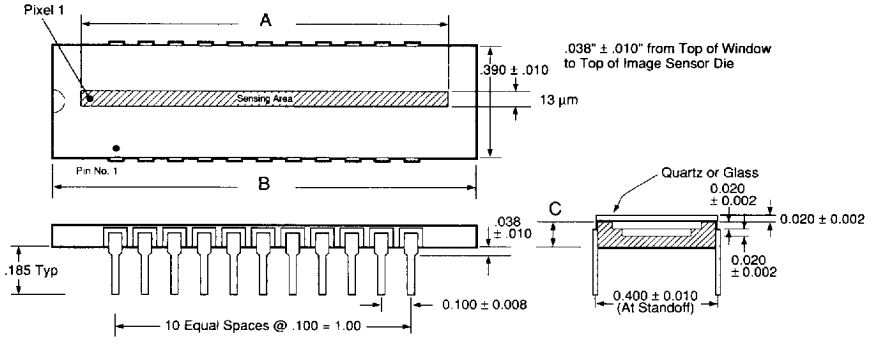
Conditions: (unless otherwise specified)
T_a = 25°C, f_{data} = 400 kHz, t_{int} = 10 ms, R_L (at video output) = 3KΩ, V_{AB} = 2V, Light Source = 2870°K + Fish Schurman HA-11, 1 mm filter. All other operating voltages are nominal, as specified in Array Electrical Characteristics for 2-phase clocking
First and last pixels of each video output are ignored

Parameter	Sym	Min	Typ	Max	Units
Center to center spacing			13		µm
Aperature width			13		µm
Operating frequency	fclock			20	MHz
Dynamic range	DR		5000:1		
Full well			700		Ke-
Saturation voltage	Vsat		1.5		V
Dark current	DL		2		nA/cm^2
Saturation exposure	Esat		0.2		$µj/cm^2$
Responsivity	R		5.4		V/µj/cm2
Charge transfer efficiency	CTE	.99995	.99999		
Photo response nonuniformity	PRNU		5		± %
Dark signal nonuniformity	DSNU		5		± %
Noise equivalent exposure p-p	NEE		0.2		nJ/cm^2
DC power dissipation	D_{dc}		36		mW
Read noise			140		e^- rms
Output amplifier sensitivity			2.2		$µV/e^-$
Noise, p-p			1.5		mV

Table 4. Absolute Maximum Ratings

Above which Useful Life May Be Impaired

	Min	Max	Units
Storage temperature	-25	+85	°C
Operating temperature	-25	+55	°C
Voltages: on any pin with respect to substrate	-0.3	+15	V



Device	A inches	A mm	B inches	C inches
RL0256DE	.131	3.328	1.080 ±0.011	0.090 ±0.009
RL0512DE	.262	6.656	1.080 ±0.011	0.080 ±0.008
RL1024DE	.524	13.312	1.080 ±0.011	0.080 ±0.008
RL2048DE	1.048	26.624	1.600 ±0.016	0.080 ±0.008

Figure 6. Package Dimensions

Ordering Information

Part Number	Evaluation Board
Quartz Window	
RL0256DEQ-011	RC0735LNN-011
RL0512DEQ-011	RC0735LNN-011
RL1024DEQ-011	RC0735LNN-011
RL2048DEQ-011	RC0735LNN-011
Glass Window	
RL0256DEG-011	RC0735LNN-011
RL0512DEG-011	RC0735LNN-011
RL1024DEG-011	RC0735LNN-011
RL2048DEG-011	RC0735LNN-011