RICOH

DIGITAL VIDEO ENCODER

R×5C292 SERIES

NO. EK-083-9609

OUTLINE

The R×5C292 Series is a video encoder IC that converts digital video signals (RGB/YCbCr signal) into composite video signals for NTSC or PAL systems. With its digital algorithm for color conversion, filtering or modulation, it is capable of outputting high precision characteristics enabling video reproduction with minimum cross color. Packages include 64pin QFP (RF5C292) and 64pin LQFP (RL5C292). Each of these has two versions of -001 and-002: RL5C292-001 is capable of outputting analog Y/C video signals and composite video signals simultaneously, with its digital section operating at 3.3V±0.3V. RF/RL5C292-002 outputs only analog composite video signals and operates at 3.3V±0.3V or at 5V±10% in digital section.

FEATURES

- All digital video encoding
- 24bit RGB or 16bit ITU-R-601 YCbCr pixel input formats
- External or internal synchronization through HSYNCB and VSYNCB signals
- 13.5MHz pixel rate (Single external clock required 13.5MHz)
- CD-G's 4fsc pixel rate compatible [will be released soon]
- M/NTSC or B,D,G,H/PAL Composite Video Output
- 27MHz convert by interpolation (on chip PLL)
- Cross color reduction (on trapfilter)
- 8colors On Screen Display (OSD) feature
- Sleep feature
- CMOS process
- Packages ·····64pin LQFP (RF5C292-002)
  64pin QFP (RL5C292-001, RL5C292-002)

RL5C292-001

- Simultaneous Composite and Y/C Video Output
- Three channels 8bit DACs on chip (37.5MΩ load drive, on chip V_{REF})
- Power Supply·····Digital block : 3.3V±0.3V, Analog block : 5V±10%

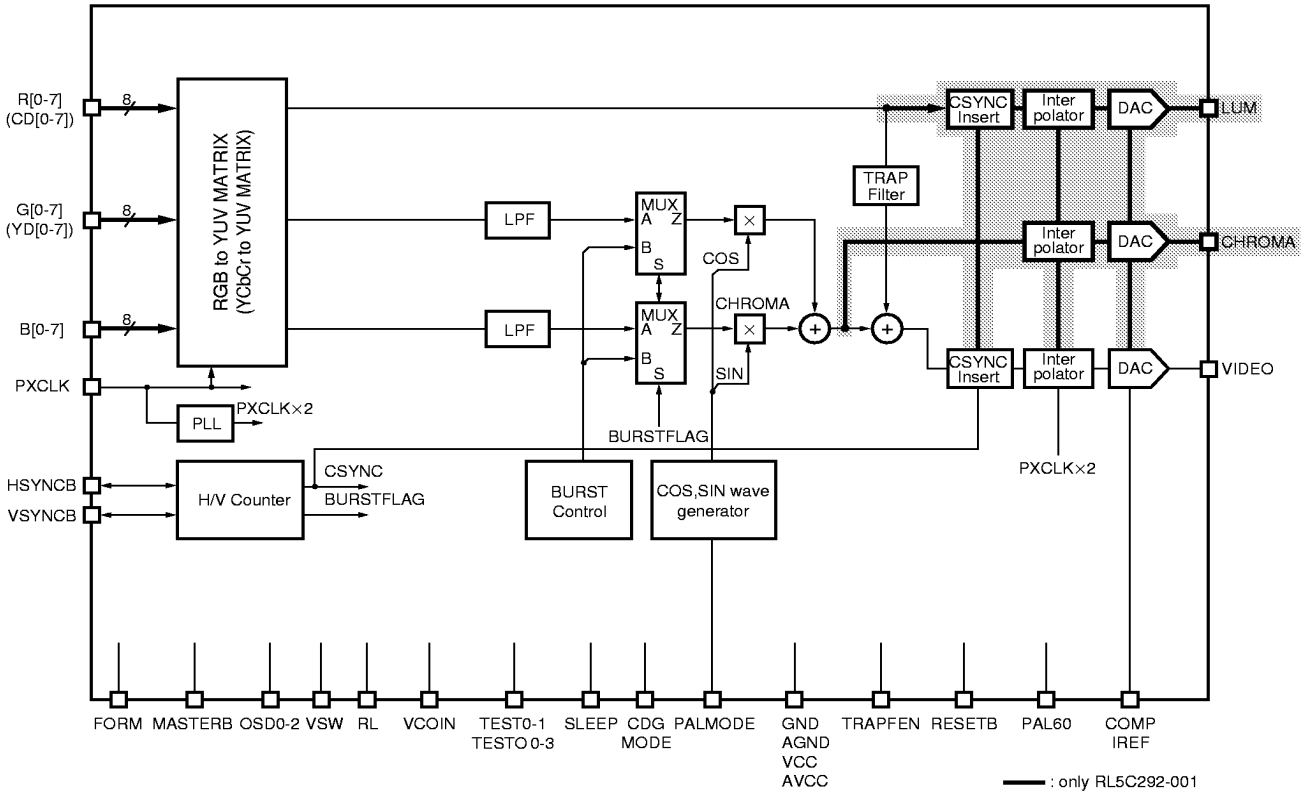
RF/RL5C292-002

- Composite Video Output
- One channel 8bit DAC on chip (37.5MΩ load drive, on chip V_{REF})
- Power Supply·····Digital block : 3.3V±0.3V or 5V±10%, Analog block : 5V±10%

APPLICATIONS

- Video CD player
- MPEG Reproduction Card
- Karaoke device
- TV games
- Set top box for cable TV or satellite broadcasting
- Internet supporting personal computers
- Video conference system

BLOCK DIAGRAM



SELECTION GUIDE

R×5C292 offers various packages or versions that may be selected according to a specific application. Selection may be done by using a device part number as shown in the example below :

R×5C292 – ××× ← Part Number
↑ a ↑ b

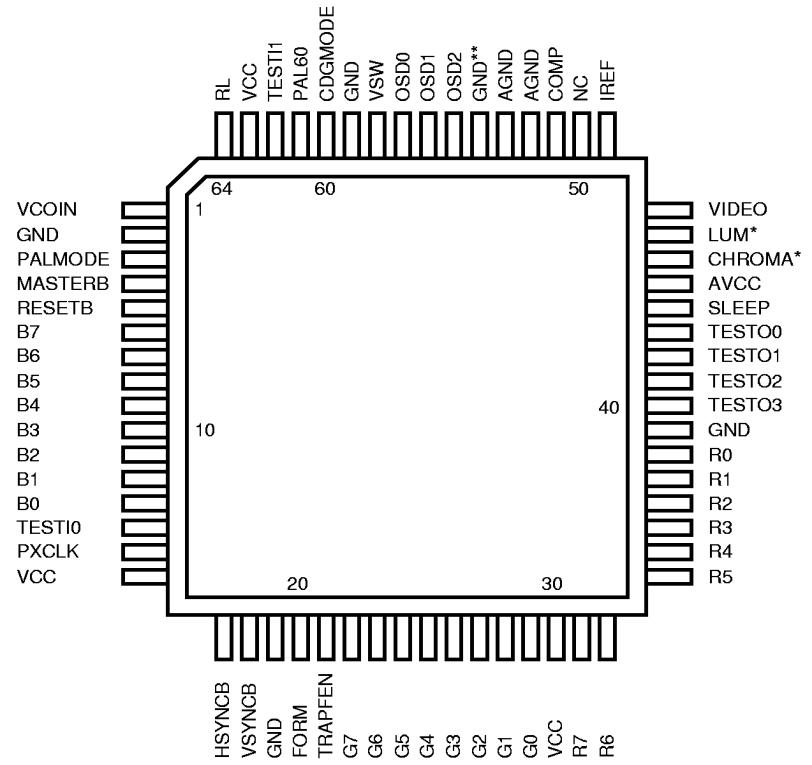
No.	Contents
a	Used for selecting a package. F : 64pin QFP (pin pitch : 0.8 mm , t=3.05mm (MAX.)) L : 64pin LQFP (pin pitch : 0.5mm , t=1.7mm (MAX.))
b	Used for specifying a version. 001 : Outputs analog Y/C signal and analog composite signal simultaneously. 3channel DAC incorporated (37.5Ω load drive, VREF incorporated); Supply voltage (digital block)3.3V±0.3V 002 : Outputs analog composite signal 1channel DAC incorporated (37.5Ω load drive, VREF incorporated); Supply voltage (digital block) 3.3V±0.3V or 5V±10%

For 64pin LQFP package of version 001, the model number will be RL5C292-001.

Note

Please note that RF5C292-001 is not available due to limitation of allowable loss of package.

PIN CONFIGURATION



*) only RL5C292-001
**) GND : RL5C292-001
VCC : RF/RL5C292-002

PIN DESCRIPTION

Built-in pull-up (PU) and pull-down (PD) resistors

Pin No.	Name	I/O	Function
15	PXCLK	I	13.5MHz or 4fsc pixel clock input (LVTTL compatible), whose frequency precision determines that of video signal subcarrier. (Refer to the CDGMODE of the PIN DESCRIPTION)
20	FORM	IPU	Input format select input (LVTTL compatible). Setting the FORM pin to "0" or "1" selects input of the CCIR-601 YCbCr (4:2:2 Format) or RGB signals, respectively. (This pin is equipped with a built-in pull-up resistor.)
38-31	R0 to 7	I	Input pins (LVTTL compatible) for R or CbCr data, whose valid input range is 16 to 235 and 16 to 240, respectively.
29-22	G0 to 7	I	Input pins (LVTTL compatible) for G or Y data, whose valid input range is 16 to 235 alike.
13-6	B0 to 7	I	Input pins (LVTTL compatible) for B data, whose valid input range is 16 to 235. Connect this pin to the GND pin when the FORM pin is set to "0".
4	MASTERB*	IPU	Synchronous mode switching control pin (LVTTL compatible). Setting the MASTERB pin to "0" or "1" selects the internal or external synchronous mode, respectively. (This pin is equipped with a built-in pull-up resistor.)
17	HSYNCB*	I/O	Horizontal synchronizing signal input/output pin (LVTTL compatible). In the external synchronous mode, this pin inputs the HSYNCB signal, which is detected only at its falling edge through sampling at the falling edge of the PXCLK signal. THe HSYNCB signal has a standard frequency of 858 clocks in the NTSC mode or 864 clocks in the PAL mode.
18	VSYNCB*	I/O	Vertical synchronizing signal input/output pin (LVTTL compatible). In the external synchronous mode, this pin inputs the VSYNCB signal, which is detected only at its falling edge through sampling at the falling edge of the PXCLK signal. Any watch between the falling edges of the HSYNCB and VSYNCB signals is recognized as the beginning of the ODD field. Conversely, any mismatch between their falling edge is recognized as the beginning of the EVEN field.
3	PALMODE	I	Video mode switching control pin (LVTTL compatible). Setting the PALMODE pin to "1" or "0" selects the PAL or NTSC mode, respectively.
5	RESETB*	I	Reset signal input pin (LVTTL compatible). This pin is active-low.
21	TRAPFEN	IPU	Enable control pin (LVTTL compatible) for the built-in Trap filter. Setting the TRAPFEN pin to "1" or "0" enables or disables the Trap filter. (This pin is equipped with a built-in pull-up resistor.)
44	SLEEP	I	Sleep mode switching control pin (LVTTL compatible). Setting the SLEEP pin to "1" or "0" selects the sleep or operational mode, respectively.
58	VSW	I	OSD/video switching control pin (LVTTL compatible), whose input is sampled at the falling edge of the PXCLK signal. Setting the VSW pin to "1" or "0" displays data input from the OSD0-2 and RGB pins, respectively.

*) "××××B" means active low

Built-in pull-up (PU) and pull-down (PD) resistors

Pin No.	Name	I/O	Function
57-55	OSD0 to 2	I	OSD color designation pins (LVTTL compatible), whose inputs are sampled at the falling edge of the PXCLK signal. Data input from the OSD 0-2 pins are encoded instead of those from the RGB pin when the VSW pin is set to "1".
48	VIDEO	O	An output pin for the analog VIDEO signal. (This pin is equipped with a 37.5Ω drive.)
47	LUM*	O	An output pin for the analog Y signal. (This pin is equipped with a 37.5Ω drive.). In case of RF5C292, keep this pin open without fail.
46	CHROMA*	O	An output pin for the analog C signal. (This pin is equipped with a 37.5Ω drive.). In case of RF5C292, keep this pin open without fail.
51	COMP	—	Compensation pin. Connect a 0.1µF capacitor from COMP to AVCC.
49	IREF	—	Resistor connected from this pin to AGND is used to setting full-scale output current value of the video signal.
61	NC	—	Reserved pin. Keep this pin open without fail.
1	VCOIN	I/O	Charge pump output/VCO input pin. Connect this pin to capacitor for the loop filter.
64	RL	—	VCO bias pin. Connect this pin to the AGND pin as standard.
16,30,63	VCC	—	Digital power supply pin. +3.3V (RL5C292-001) +3.3V or +5V (RF/RL5C292-002)
2,19,39, 59	GND	—	Digital ground pin.
54	GND/VCC	—	Digital ground pin upon RL5C292-001. Digital power supply pin upon RF/RL5C292-002.
45	AVCC	—	Analog power supply (+5V) pin.
52,53	AGND	—	Analog ground pin.
14,62	TESTI0 to 1	IPD	Test signal input pin. Keep this pin open.
43-40	TESTO0 to 3	O	Test signal output pin. Keep this pin open.
60	CDGMODE	IPD	CD-G pixel rate selection pin. When CDGMODE=1, clock signal (NTSC: 14.31818MHZ, PAL:17.734475MHz) can be input to the PXCLK pin. When CDGMODE=0, input clock signal of 13.5MHz to the PXCLK pin.
61	PAL60	IPD	PAL60 mode selection pin (LVTTL). When PAL=1 and PALMODE=1, H/V SYNC and internal modulation system can be set to NTSC and PAL respectively. Set PAL60=0 in the PAL normal mode. However, don't set PAL60=1 in the NTSC mode (PALMODE=0).

*) only RL5C292-001.

RL5C292-001 CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Conditions	Ratings	Unit
Vcc	Digital supply voltage	GND pin reference	–0.3 to +7.0	V
AVcc	Analog supply voltage	GND pin reference	–0.3 to +7.0	V
VTE	Pin voltage	—	–0.3 to Vcc+0.3	V
VATE	Analog pin voltage*	—	–0.3 to AVcc +0.3	V
Topr	Ambient operating temperature	—	0 to +70	°C
Tstg	Storage temperature	—	–55 to +125	°C
Pd	Total Power Dissipation	Tj=125°C	900	mW

*) The analog pin voltage rating applies to the VIDEO, LUM, CHROMA, IREF, and COMP pins.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum ratings are threshold limit values that must not be exceeded even for an instant under any conditions. Moreover, such values for any two items must not be reached simultaneously. Operation above these absolute maximum ratings may cause degradation or permanent damage to the device. These are stress ratings only and do not necessarily imply functional operation below these limits.

RECOMMENDED OPERATING CONDITION

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
Vcc	Supply voltage		3.0	3.3	3.6	V
AVcc	Supply voltage		4.5	5.0	5.5	V
Ta	Ambient operating temperature		0	25	70	°C

DC CHARACTERISTICS

(Vcc=3.3V±0.3V, AVcc=5.0V±0.5V, Ta=0 to 70°C)

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
V_{IH}	"H" input voltage		2.0		Vcc+0.3	V
V_{IL}	"L" input voltage		–0.3		0.8	V
I_{LI}	Input leakage current	V_I=0 to Vcc	–0.3		3.0	µA
I_{IL1}	Pull-up "L" input current	V_I=0V	–130	–45	–10	µA
I_{IH2}	Pull-down "H" input current	V_I=Vcc	10	45	130	µA
V_{OH}	"H" output voltage	I_{OH}=–50µA	Vcc × 0.8			V
V_{OL}	"L" output voltage	I_{OL}=4mA			0.4	V
I_{OZ}	Off-state output leakage current	V_O=0 to Vcc	–3.0		3.0	µA
I_{DCC2}	Digital supply current (Operating)	fpxclk=13.5MHz		—	50	mA
I_{DCC1}	Digital supply current (Stand-by)	SLEEP=Vcc		—	30	µA
I_{ACC2}	Analog supply current (Operating)	fpxclk=13.5MHz, R_{SET}=280Ω,		120		mA
		fpxclk=13.5MHz, R_{SET}=300Ω		110		mA
I_{ACC1}	Analog supply current (Stand-by)	SLEEP=Vcc		—	30	µA

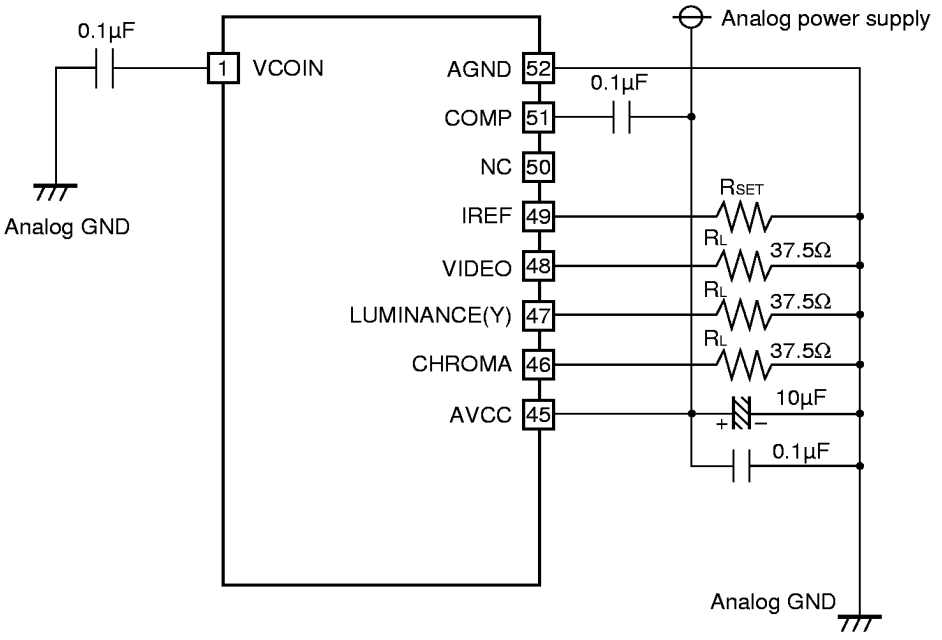
ELECTRIC CHARACTERISTICS OF D/A CONVERTER AND

AVcc=5V±0.5V

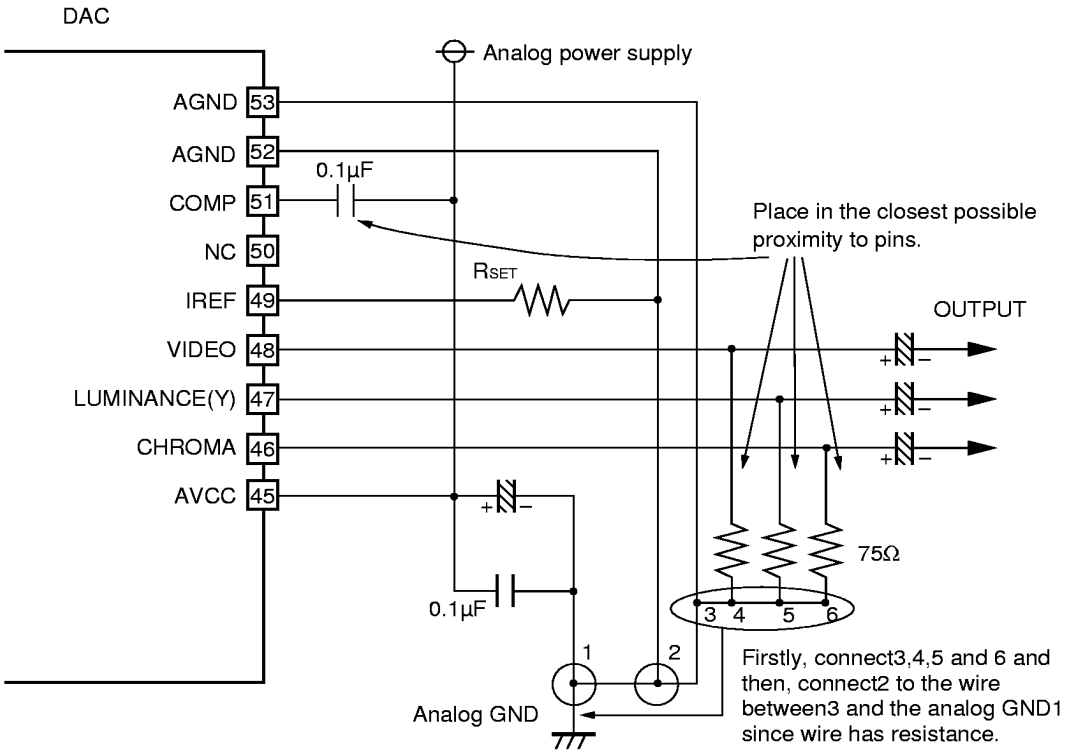
Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
VFOUT	Full-scale voltage	RSET=280Ω	1.2	1.3	1.4	V
		RSET=300Ω	1.13	1.23	1.33	V
VCO	Output compliance voltage	RSET=280Ω			1.5	V
		RSET=300Ω			1.4	V
fIN	Clock input frequency			27		MHz
TSET	Settling time*			33		ns
ENL	Linearity error			±1		LSB
ICCA	Analog supply current (5V)	RSET=280Ω		120		mA
		RSET=300Ω		110		mA
TLUT	PLL lock-up time				1	ms

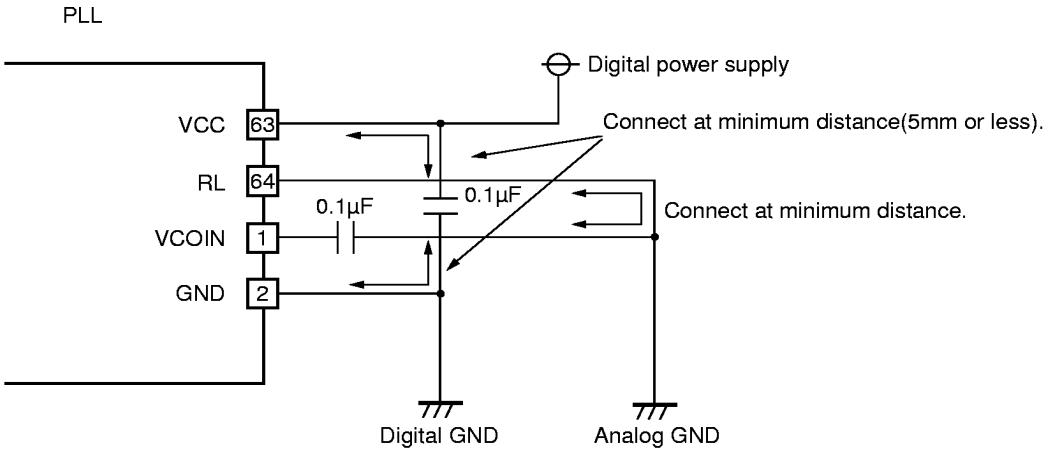
*) Time interval from when the D/A converter input rises to when the D/A converter output falls within ±2LSB of their final value (input code changes include changes from 00h to FFh and from FFh to 00h).

• Measuring Circuit



Notes on connecting analog terminals





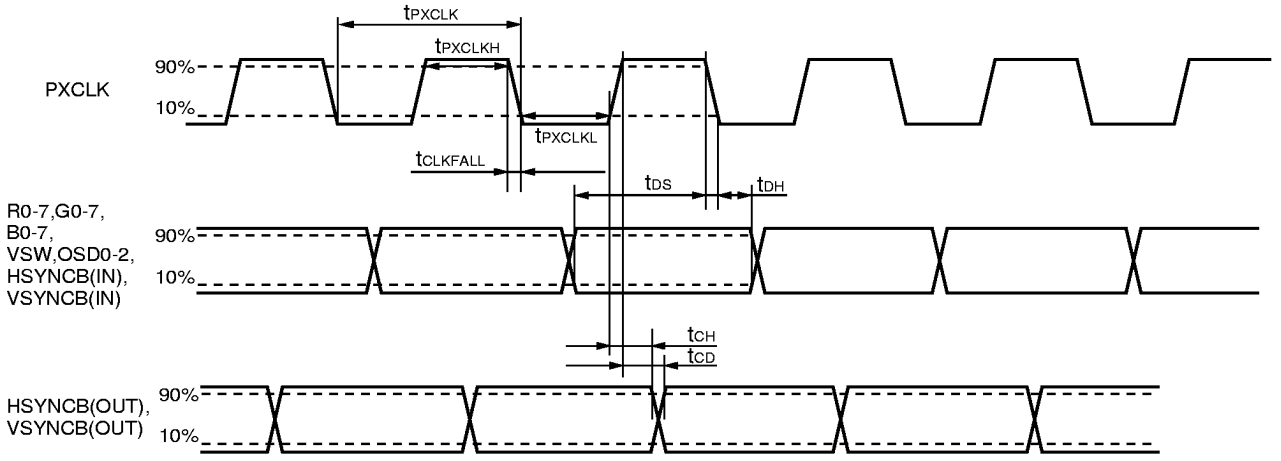
For each digital power terminal (pin No.16, 30 and 63) place a bypass condenser (0.1µF) between the ground as close to the device as possible.

AC ELECTRIC CHARACTERISTICS

Symbol	Item	MIN.	TYP.	MAX.	Unit
f_{PXCLK}	Clock frequency		13.5*		MHz
t_{PXCLK}	Clock cycle		74		ns
t_{PXCLKH}	"H" clock interval	30			ns
t_{PXCLKL}	"L" clock interval	30			ns
t_{DS}	Data/Control setup time	15			ns
t_{DH}	Data/control hold time	20			ns
t_{CD}	Video synchronizing output signal delay time			55	ns
t_{CH}	Video synchronizing output signal hold time	0			ns
$t_{CLKFALL}$	Clock fall time			5	ns

*) When CDGMODE=1, NTSC : 14.31818MHz and PAL : 17.734475MHz.

• Video Input/Output Timing



RF5C292-002 CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Conditions	Ratings	Unit
Vcc	Digital supply voltage	GND pin reference	–0.3 to +7.0	V
AVcc	Analog supply voltage	GND pin reference	–0.3 to +7.0	V
VTE	Pin voltage	—	–0.3 to Vcc+0.3	V
VATE	Analog pin voltage*	—	–0.3 to AVcc +0.3	V
Topr	Ambient operating temperature	—	0 to +70	°C
Tstg	Storage temperature	—	–55 to +125	°C
Pd	Total Power Dissipation	Tj=125°C	850	mW

*) The analog pin voltage rating applies to the VIDEO, IREF, and COMP pins.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum ratings are threshold limit values that must not be exceeded even for an instant under any conditions. Moreover, such values for any two items must not be reached simultaneously. Operation above these absolute maximum ratings may cause degradation or permanent damage to the device. These are stress ratings only and do not necessarily imply functional operation below these limits.

RECOMMENDED OPERATING CONDITION

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
Vcc	Supply voltage		3.0	3.3	3.6	V
			4.5	5.0	5.5	V
AVcc	Supply voltage		4.5	5.0	5.5	V
Ta	Ambient operating temperature		0	25	70	°C

DC CHARACTERISTICS (1)

(Vcc=3.3V±0.3V, AVcc=5.0V±0.5V, Ta=0 to 70°C)

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
V_{IH}	"H" input voltage		2.0		Vcc+0.3	V
V_{IL}	"L" input voltage		–0.3		0.8	V
I_{LI}	Input leakage current	V_I=0 to Vcc	–0.3		3.0	µA
I_{IL1}	Pull-up "L" input current	V_I=0V	–130	–45	–10	µA
I_{IH2}	Pull-down "H" input current	V_I=Vcc	10	45	130	µA
V_{OH}	"H" output voltage	I_{OH}=–50µA	Vcc × 0.8			V
V_{OL}	"L" output voltage	I_{OL}=4mA			0.4	V
I_{OZ}	Off-state output leakage current	V_O=0 to Vcc	–3.0		3.0	µA
I_{DCC2}	Digital supply current (Operating)	fpxclk=13.5MHz		—	50	mA
I_{DCC1}	Digital supply current (Stand-by)	SLEEP=Vcc		—	30	µA
I_{ACC2}	Analog supply current (Operating)	fpxclk=13.5MHz, R_{SET}=280Ω,		45		mA
		fpxclk=13.5MHz, R_{SET}=300Ω		40		mA
I_{ACC1}	Analog supply current (Stand-by)	SLEEP=Vcc		—	30	µA

DC CHARACTERISTICS (2)

(Vcc=5.0V±0.5V, AVcc=5.0V±0.5V, Ta=0 to 70°C)

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
V_{IH}	"H" input voltage		3.0		Vcc+0.3	V
V_{IL}	"L" input voltage		–0.3		Vcc × 0.3	V
I_{LI}	Input leakage current	V_I=0 to Vcc	–10		10	µA
I_{IL1}	Pull-up "L" input current	V_I=0V	–400	–100	–30	µA
I_{IH2}	Pull-down "H" input current	V_I=Vcc	30	100	400	µA
V_{OH}	"H" output voltage	I_{OH}=–50µA	Vcc × 0.8			V
V_{OL}	"L" output voltage	I_{OL}=4mA			0.4	V
I_{OZ}	Off-state output leakage current	V_O=0 to Vcc	–10		10	µA
I_{DCC2}	Digital supply current (Operating)	fpxclk=13.5MHz		—	90	mA
I_{DCC1}	Digital supply current (Stand-by)	SLEEP=Vcc		—	60	µA
I_{ACC2}	Analog supply current (Operating)	fpxclk=13.5MHz, R_{SET}=280Ω,		45		mA
		fpxclk=13.5MHz, R_{SET}=300Ω		40		mA
I_{ACC1}	Analog supply current (Stand-by)	SLEEP=Vcc		—	30	µA

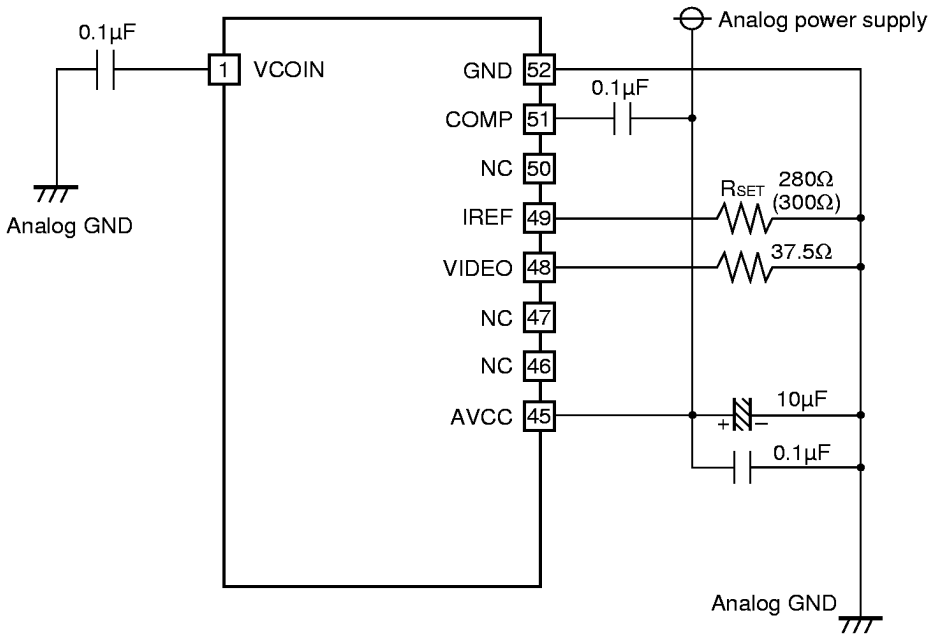
ELECTRIC CHARACTERISTICS OF D/A CONVERTER AND

(AVcc=5V±0.5V)

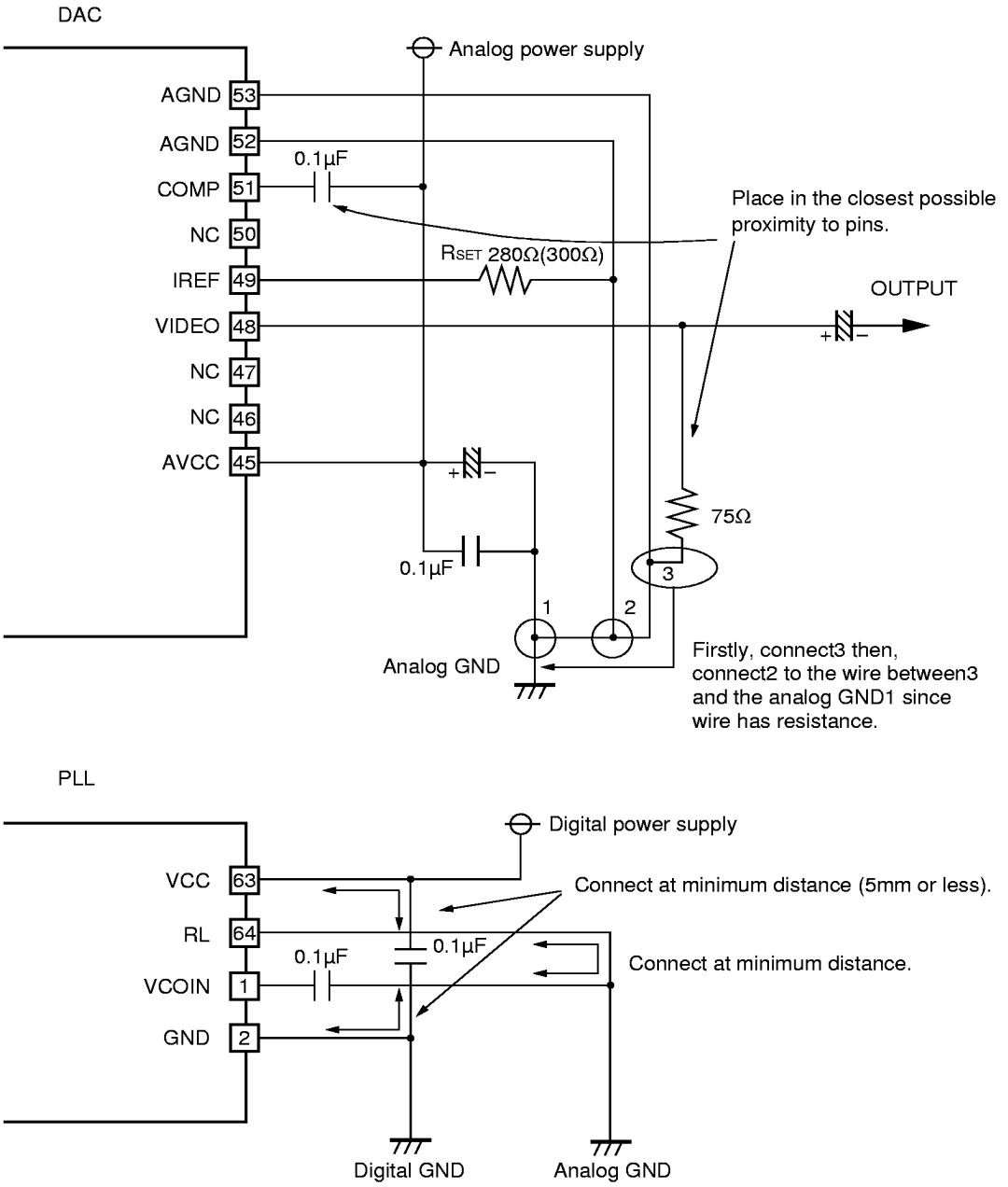
Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
VFOUT	Full-scale voltage	RSET=280Ω	1.2	1.3	1.4	V
		RSET=300Ω	1.13	1.23	1.33	V
VCO	Output compliance voltage	RSET=280Ω			1.5	V
		RSET=300Ω			1.4	V
fIN	Clock input frequency			27		MHz
TSET	Settling time*			33		ns
ENL	Linearity error			±1		LSB
ICCA	Analog supply current (5V)	RSET=280Ω		45		mA
		RSET=300Ω		40		mA
TLUT	PLL lock-up time				1	ms

*) Time interval from when the D/A converter input rises to when the D/A converter output falls within ±2LSB of their final value (input code changes include changes from 00h to FFh and from FFh to 00h).

• Measuring Circuit



Analog Pin Connection Diagram



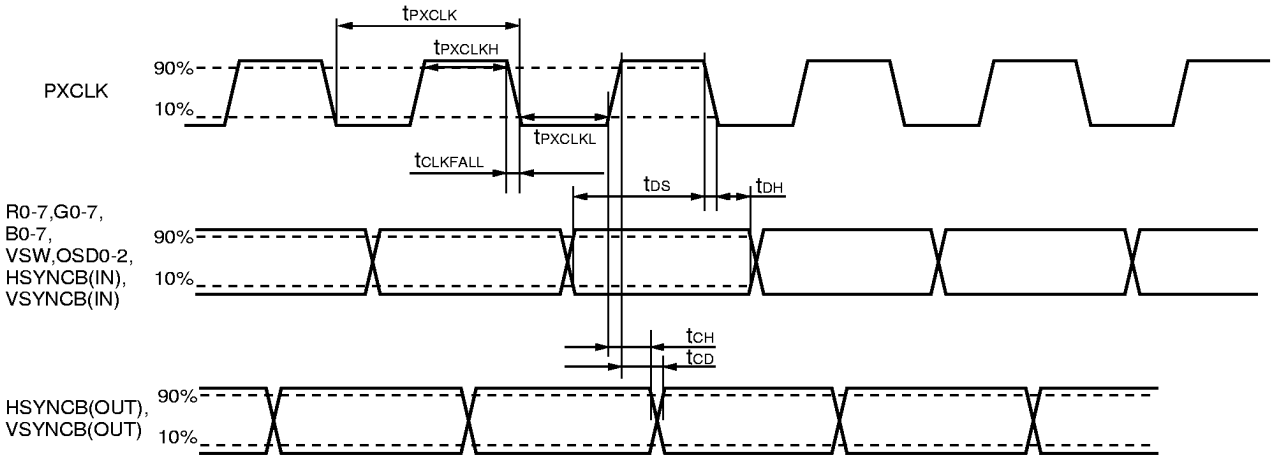
For each digital power terminal (pin No.16, 30 and 63) place a bypass condenser (0.1µF) between the ground as close to the device as possible.

AC ELECTRIC CHARACTERISTICS

Symbol	Item	MIN.	TYP.	MAX.	Unit
f_{PXCLK}	Clock frequency		13.5*		MHz
t_{PXCLK}	Clock cycle		74		ns
t_{PXCLKH}	High-level clock interval	30			ns
t_{PXCLKL}	Low-level clock interval	30			ns
t_{DS}	Data/Control setup time	15			ns
t_{DH}	Data/control hold time	20			ns
t_{CD}	Video synchronizing output signal delay time			55	ns
t_{CH}	Video synchronizing output signal hold time	0			ns
$t_{CLKFALL}$	Clock fall time			5	ns

*) When CDGMODE=1, NTSC : 14.31818MHz and PAL : 17.734475MHz.

• **Video Input/Output Timing**



RL5C292-002 CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Conditions	Ratings	Unit
Vcc	Digital supply voltage	GND pin reference	–0.3 to +7.0	V
AVcc	Analog supply voltage	GND pin reference	–0.3 to +7.0	V
VTE	Pin voltage	—	–0.3 to Vcc+0.3	V
VATE	Analog pin voltage*	—	–0.3 to AVcc +0.3	V
Topr	Ambient operating temperature	—	0 to +70	°C
Tstg	Storage temperature	—	–55 to +125	°C
Pd	Total Power Dissipation	Tj=125°C	850	mW

*) The analog pin voltage rating applies to the VIDEO, IREF, and COMP pins.

ABSOLUTE MAXIMUM RATINGS

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RECOMMENDED OPERATING CONDITION

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
Vcc	Supply voltage		3.0	3.3	3.6	V
			4.5	5.0	5.5	V
AVcc	Supply voltage		4.5	5.0	5.5	V
Ta	Ambient operating temperature		0	25	70	°C

DC CHARACTERISTICS (1)

(Vcc=3.3V±0.3V, AVcc=5.0V±0.5V, Ta=0 to 70°C)

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
V_{IH}	"H" input voltage		2.0		Vcc+0.3	V
V_{IL}	"L" input voltage		–0.3		0.8	V
I_{LI}	Input leakage current	V_I=0 to Vcc	–0.3		3.0	µA
I_{IL1}	Pull-up "L" input current	V_I=0V	–130	–45	–10	µA
I_{IH2}	Pull-down "H" input current	V_I=Vcc	10	45	130	µA
V_{OH}	"H" output voltage	I_{OH}=–50µA	Vcc × 0.8			V
V_{OL}	"L" output voltage	I_{OL}=4mA			0.4	V
I_{OZ}	Off-state output leakage current	V_O=0 to Vcc	–3.0		3.0	µA
I_{DCC2}	Digital supply current (Operating)	fpxclk=13.5MHz		—	50	mA
I_{DCC1}	Digital supply current (Stand-by)	SLEEP=Vcc		—	30	µA
I_{ACC2}	Analog supply current (Operating)	fpxclk=13.5MHz, R_{SET}=280Ω,		45		mA
		fpxclk=13.5MHz, R_{SET}=300Ω		40		mA
I_{ACC1}	Analog supply current (Stand-by)	SLEEP=Vcc		—	30	µA

DC CHARACTERISTICS (2)

(Vcc=5.0V±0.5V, AVcc=5.0V±0.5V, Ta=0 to 70°C)

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
V_{IH}	"H" input voltage		3.0		Vcc+0.3	V
V_{IL}	"L" input voltage		–0.3		Vcc × 0.3	V
I_{LI}	Input leakage current	V_I=0 to Vcc	–10		10	µA
I_{IL1}	Pull-up "L" input current	V_I=0V	–400	–100	–30	µA
I_{IH2}	Pull-down "H" input current	V_I=Vcc	30	100	400	µA
V_{OH}	"H" output voltage	I_{OH}=–50µA	Vcc × 0.8			V
V_{OL}	"L" output voltage	I_{OL}=4mA			0.4	V
I_{OZ}	Off-state output leakage current	V_O=0 to Vcc	–10		10	µA
I_{DCC2}	Digital supply current (Operating)	fpxclk=13.5MHz		—	90	mA
I_{DCC1}	Digital supply current (Stand-by)	SLEEP=Vcc		—	60	µA
I_{ACC2}	Analog supply current (Operating)	fpxclk=13.5MHz, R_{SET}=280Ω,		45		mA
		fpxclk=13.5MHz, R_{SET}=300Ω		40		mA
I_{ACC1}	Analog supply current (Stand-by)	SLEEP=Vcc		—	30	µA

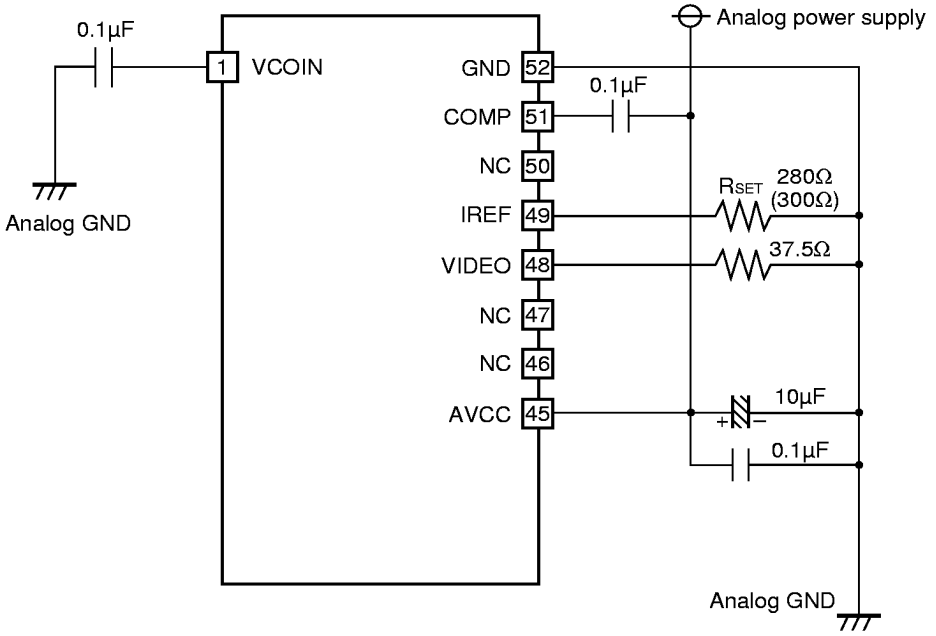
ELECTRIC CHARACTERISTICS OF D/A CONVERTER AND

(AVcc=5V±0.5V)

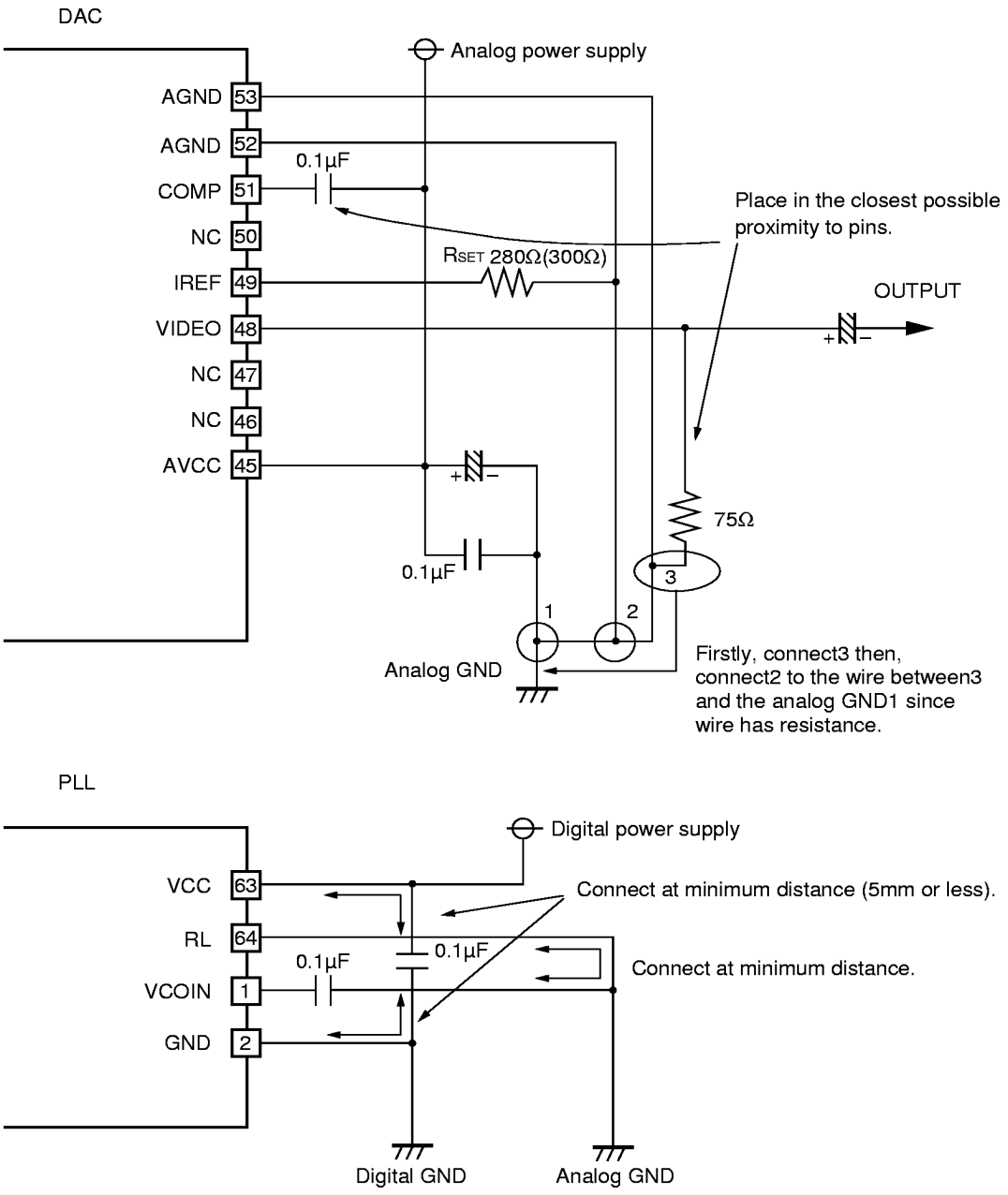
Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
VFOUT	Full-scale voltage	RSET=280Ω	1.2	1.3	1.4	V
		RSET=300Ω	1.13	1.23	1.33	V
VCO	Output compliance voltage	RSET=280Ω			1.5	V
		RSET=300Ω			1.4	V
fIN	Clock input frequency			27		MHz
TSET	Settling time*			33		ns
ENL	Linearity error			±1		LSB
ICCA	Analog supply current (5V)	RSET=280Ω		45		mA
		RSET=300Ω		40		mA
TLUT	PLL lock-up time				1	ms

*) Time interval from when the D/A converter input rises to when the D/A converter output falls within ±2LSB of their final value (input code changes include changes from 00h to FFh and from FFh to 00h).

• Measuring Circuit



Analog Pin Connection Diagram



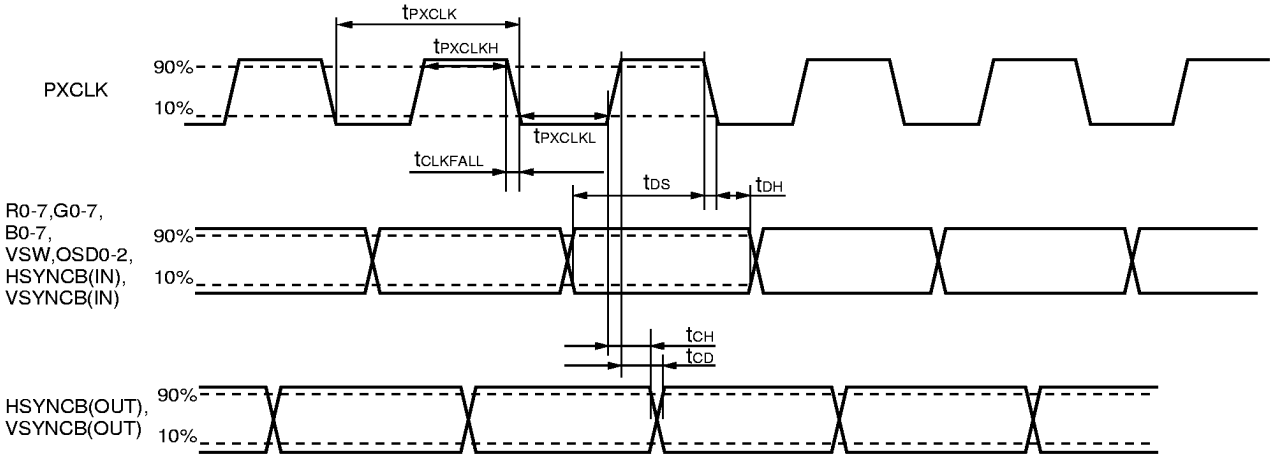
For each digital power terminal (pin No.16, 30 and 63) place a bypass condenser (0.1µF) between the ground as close to the device as possible.

AC ELECTRIC CHARACTERISTICS

Symbol	Item	MIN.	TYP.	MAX.	Unit
f_{PXCLK}	Clock frequency		13.5*		MHz
t_{PXCLK}	Clock cycle		74		ns
t_{PXCLKH}	"H" clock interval	30			ns
t_{PXCLKL}	"L" clock interval	30			ns
t_{DS}	Data/Control setup time	15			ns
t_{DH}	Data/control hold time	20			ns
t_{CD}	Video synchronizing output signal delay time			55	ns
t_{CH}	Video synchronizing output signal hold time	0			ns
$t_{CLKFALL}$	Clock fall time			5	ns

*) When CDGMODE=1, NTSC : 14.31818MHz and PAL : 17.734475MHz.

• Video Input/Output Timing



FUNCTIONAL DESCRIPTION

1. Pixel Input Format

1.1 24bit RGB Mode

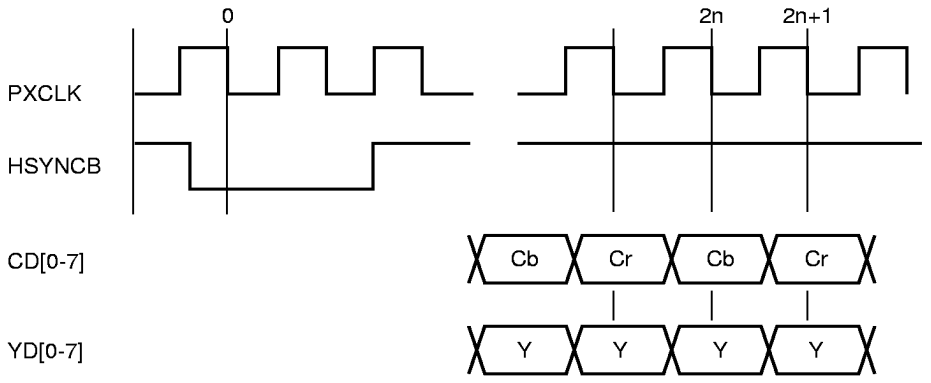
- The 24bit RGB mode is selected by setting the FORM pin (an input format selection pin) to "1". In this mode, 8bit RGB data can be input from the R0-7, G0-7, and B0-7 pins with the R0, G0, and B0 pin inputs as the least significant bits (LSBs).
- RGB data thus input are sampled at the falling edge of the PXCLK signal for input to the RGB-to-YUV matrix.
- RGB data have a valid input range of 16 to 235, beyond which they are clipped to these lower and upper limits.

1.2 16bit ITU-R-601 YCbCr Mode (4:2:2 Format)

- The 16bit YCbCr mode is selected by setting the FORM pin (an input format selection pin) to "0". In this mode, multiplexed CbCr data or Y data can be input from the R0-7 or G0-7 pins, respectively, with the Cb0, Cr0, and Y0 pin inputs as the least significant bits (LSBs). The B0-7 pins are unused in this mode and should be connected to the GND pin.
- CbCr and Y data thus input are sampled at the falling edge of the PXCLK signal for demultiplexing and interpolation and then input to the YCbCr-to-YUV matrix.
- Y data have a valid input range of 16 to 235, beyond which they are clipped to these lower and upper limits.
- CbCr data have a valid input range of 16 to 240, beyond which they are clipped to these lower and upper limits. Further, CbCr data have an offset binary input format in which 80h represents zero.

2. Formatting and Matrixes

- CbCr data should be input in an alternating sequence in which Cb and Cr data are input at odd and even timings, respectively, as counted from the falling edge of the PXCLK signal following that of the HSYNCB signal. This sequence is also followed in demultiplexing CbCr data.



Input Timings for YCbCr Data

- Demultiplexed YCbCr data are converted from the 4:2:2 Format to the 4:4:4 Format through linear interpolation.
- RGB-to-YUV color space conversion is performed by using the following equations:

  Y = 0.299R + 0.587G + 0.114B
  U = 0.493 (B–Y)
  V = 0.877 (R–Y)

- Input YCbCr data are converted into the YUV level as signals renormalized in compliance with the CCIR Standard No.601.
- A set-up of 7.5% is not supported in the NTSC mode.

3. OSD (On Screen Display)

- The VSW pin can be used to switch between colors designated by the OSD0-2 pins and data input from the RGB pins for display in units of pixels. The VSW signal is sampled at the falling edge of the PXCLK signal.
- Setting the VSW pin to "0" or "1" displays data input from the RGB and OSD0-2 pins, respectively.
- A saturation level should be set to 80% for each color.
- Data input from the OSD0-2 pins are sampled at the falling edge of the PXCLK signal, thus retaining synchronism with data input from the RGB pins.
- The OSD0-2 pins can be used to designate the colors listed in the table below.

TABLE 1 : OSD color Settings

color	OSD2	OSD1	OSD0
white	L	L	L
yellow	L	L	H
cyan	L	H	L
green	L	H	H
magenta	H	L	L
red	H	L	H
blue	H	H	L
black	H	H	H

4. PLL

- The PLL is housed to generate the PXCLK × 2 (27MHz*1) for comparison with the PXCLK (13.5MHz*2).
- The PLL consists of the VCO, the phase comparator, the divide-by-two circuit, and the charge pump. It incorporates the resistor for the loop filter and requires one capacitor to be connected as an external component to the VCOIN pin.
- When the chip is reset or the PXCLK signal is stopped, the PLL sets "unlock" and any input video data is invalid until the PLL sets "lock" again.
- When the AGND pattern is to be installed on the dual-layer board, the RL pin and the capacitor coupled with the VCOIN pin should be connected to the AGND pin at the shortest possible distance.

*1) When CDGMODE=1, NTSC : 14.31818MHz and PAL : 17.734475MHz.
*2) When CDGMODE=1, NTSC : 28.63636MHz and PAL : 35.46895MHz.

5. HV Counter and Decoding

- The HV counter is housed to generate signals required for such video signals as the Csync signal. It is synchronized with external components by the HSYNCB and VSYNCB signals.
- A total of 525 (60Hz) or 625 (50Hz) interlaced scanning lines are allowed in the NTSC or PAL mode, respectively.
- The HSYNCB signal has a cycle equivalent to the 858 or 864 PXCLK signals and displays maximum of 711 or 704 valid pixels in the NTSC or PAL mode, respectively.
- The synchronizing pulse of the video signal is generated through internal calculation of its width, serration pulses, equalizing pulses, duration of subcarrier burst, blanking of chrominance subcarrier, and blanking interval.
- The video signal is generated through no control over its build-up time of the edges of the line-blanking pulse and line-synchronizing pulses, and burst envelope.
- There are 4 or 8 color fields in the NTSC or PAL mode, respectively.

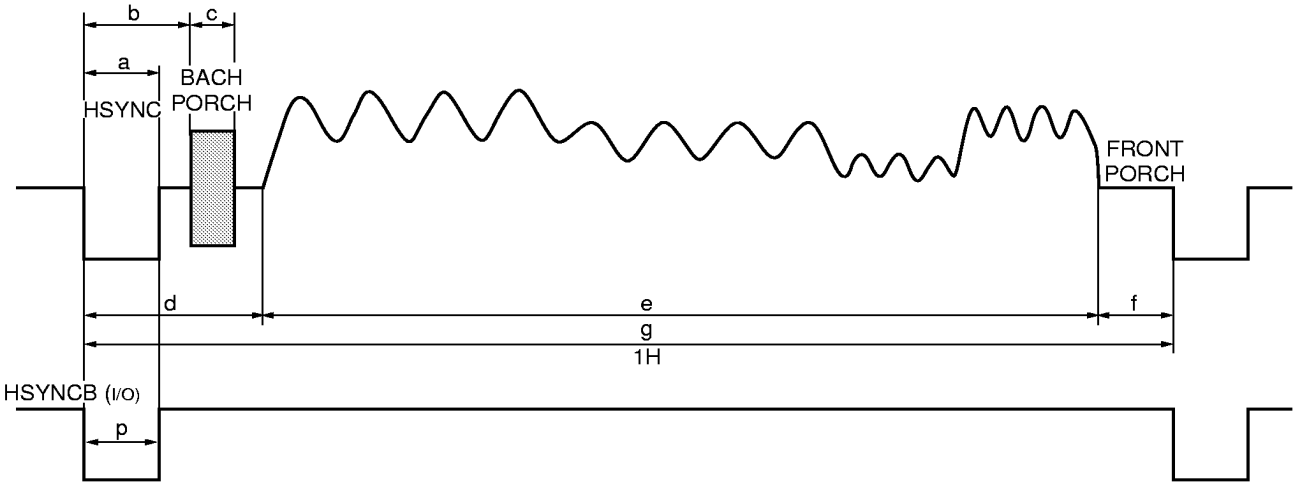
5.1 Internal Synchronous Mode

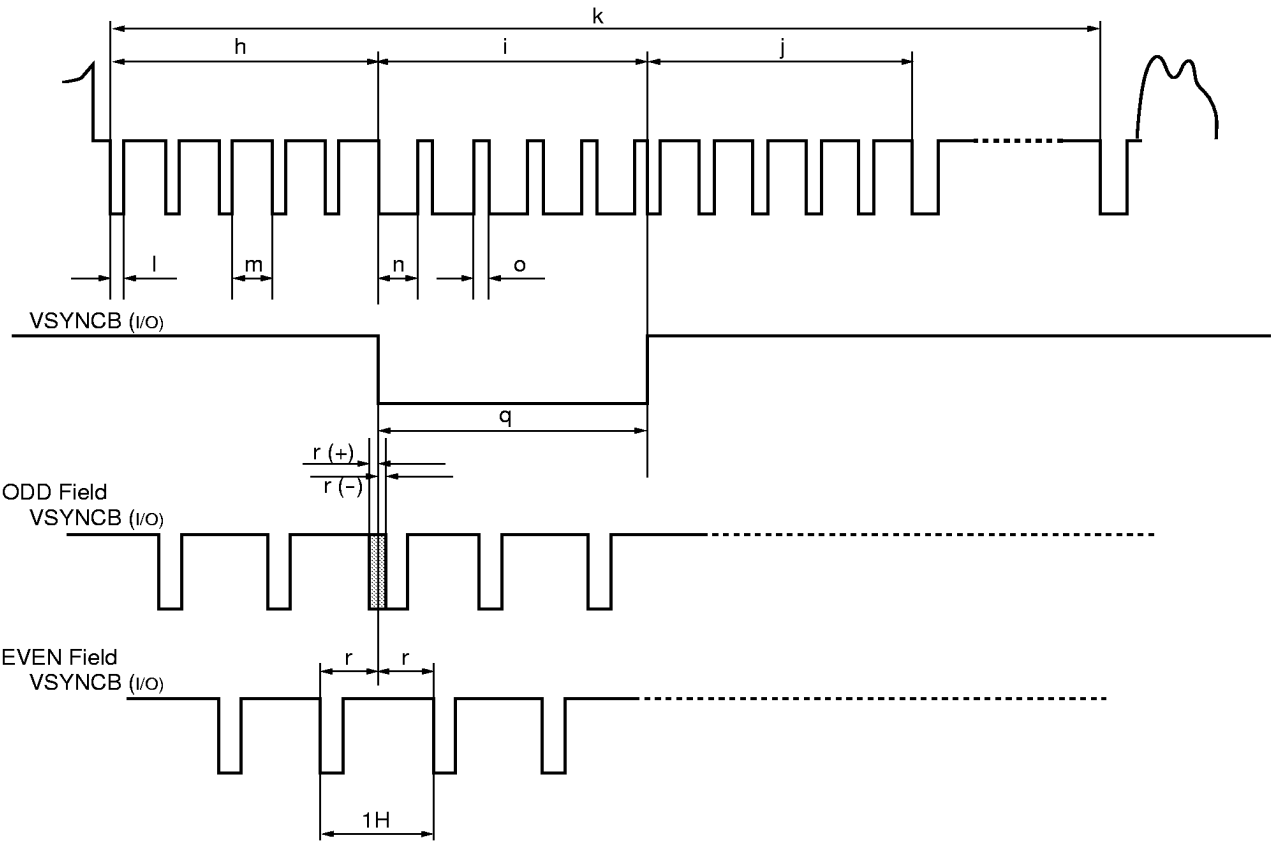
- The internal synchronous mode is selected by setting the MASTERB (a synchronous mode switching control pin) to "0". In this mode, the HSYNCB and VSYNCB pins function as output pins, from which the HSYNCB and VSYNCB signals are output in synchronization with the rising edge of the PXCLK signal with the built-in HV counter self-operated. To synchronize with external components, use the falling edge of the PXCLK signal.
- Any match between the falling edges of the HSYNCB and VSYNCB signals is recognized as the beginning of the ODD field. Meanwhile, any match between the high level of the HSYNCB signal and the falling edge of the VSYNCB signal is recognized as the beginning of the EVEN field.

5.2 External Synchronous Mode

- The external synchronous mode is selected by setting the MASTERB (a synchronous mode switching control pin) to "1". In this mode, the HSYNCB and VSYNCB pins function as input pins, to which the HSYNCB and VSYNCB signals are input for sampling at the falling edge of the PXCLK signal, allowing pixel data to retain synchronism with the falling edge of the HSYNCB signal.
- Any match between the falling edges of the HSYNCB and VSYNCB signals is recognized as the beginning of the ODD field. Meanwhile, any match between the nearly intermediate cycle of the HSYNCB signal and the falling edge of the VSYNCB signal is recognized as the beginning of the EVEN field.
- The HSYNCB and VSYNCB signals are detected only at their falling edge. Consequently, neither of these signals requires any pulse width equivalent to the Hsync or Vsync of the video signal. Nor should the VSYNCB signal be included with any serration pulses or equalizing pulses.
- In the external synchronous mode, a total of 262 non-interlaced scanning lines should be allowed in one field.

5.3 Datailed Diagram Showing Synchronized Waveform of Output Video Signal



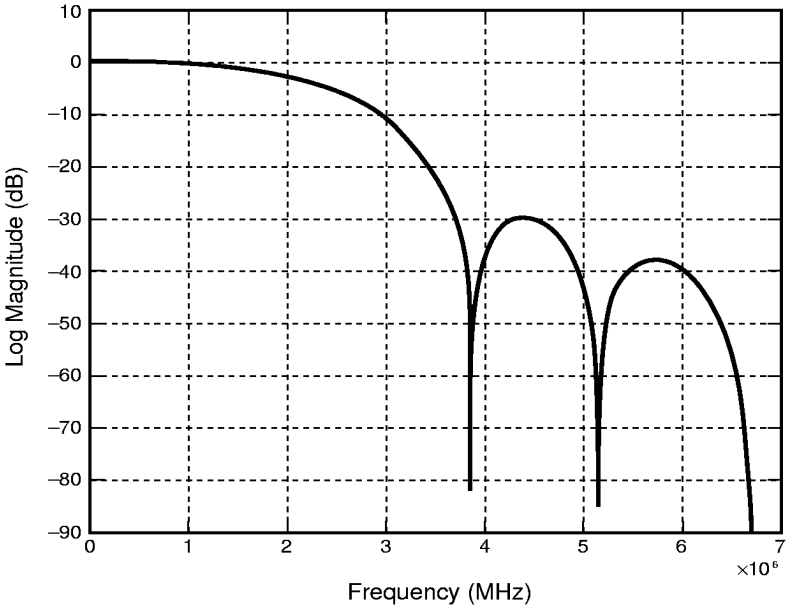


	Internal synchronous mode		External synchronous mode		Unit
	NTSC	PAL	NTSC	PAL	
a	64	64	64	64	PXCLK
b	72	76	72	76	PXCLK
c	34	31	34	31	PXCLK
d	127	141	127	141	PXCLK
e	711	704	711	704	PXCLK
f	20	19*1	(Externally dependent)*2	(Externally dependent)*2	PXCLK
g	858	864	(Externally dependent)	(Externally dependent)	PXCLK
h	3	2.5	(Externally dependent)	(Externally dependent)	H
i	3	2.5	3	2.5	H
j	3	2.5	3	2.5	H
k	20	25	(Externally dependent)	(Externally dependent)	H
l	31	31	31	31	PXCLK
m	398	401	398	401	PXCLK
n	365	368	365	368	PXCLK
o	64	64	64	64	PXCLK
p	64	64	2(MIN.)	2(MIN.)	PXCLK
q	3	2.5			H
			2(MIN.)	2(MIN.)	PXCLK
r(oddfield)	0	0	–5 to +5	–5 to +5	PXCLK
r (evenfield)	1/2	1/2			H
			10(MIN.)*3	10(MIN.)*3	PXCLK

*1) Include are items not conforming to the I/PAL standard, etc.
*2) Regardless of video inputs, an interval following (711+127) clocks (in the NTSC mode) or (704+141) clocks (in the PAL mode) after the falling edge of the HSYNCB signal becomes a blanking interval.
*3) The VSYNCB signal should preferably fall with the timing of 1/2 H (equivalent to a line midpoint)

6. Low-pass Filter

- The digital low-pass filter is housed to restrict the band of the UV color-difference signal.
- A linear-phase FIR filter functions as the low-pass filter and ensures a constant group delay.
- The low-pass filter has the filtering characteristics shown in the diagram below.



Filtering Characteristics of Digital Low-pass Filter

7. Wave Generator

- In the NTSC mode, the wave generator samples the fsc signal (3.579545MHz) at a pixel rate of 13.5MHz*1 to generate sine and cosine waves.
- In the PAL mode, the wave generator samples the fsc signal (4.43361875MHz) at a pixel rate of 13.5MHz*2 to generate sine and cosine waves in such a manner as to accommodate 25Hz compensation of color subcarriers.

*1) When CDGMODE=1, 14.31818MHz.
*2) When CDGMODE=1, 17.734475MHz.

8. Trap Filter

- The trap filter is housed to reduce cross color caused by the frequency components of subcarriers contained in luminance signals in composite video signals. It can be enabled or disabled by the TRAPFEN pin.
- Setting the TRAPFEN pin to high level enables the trap filter to filter luminance signals. Conversely, setting the TRAPFEN pin to low level bypasses the trap filter.
- Trade-off exists between cross color reduction and sharpness deterioration as follow:
  Cross color Large ⇔ Small
  Sharpness High ⇔ Low
- The TRAPFEN pin does not affect the LUM pin, from which luminance signals converted by the matrix circuit are output without any change. (only RL5C292-001)

9. Interpolator

- The interpolator converts luminance signal, chroma signal (only RL5C292-001), and composite video signal input to the D/A converter into twice their original pixel rate.
- Such sampling frequency conversion serves to facilitate the process of designing the analog post filter at the rear row of the D/A converter and reduce the aperture distortion by the D/A converter.

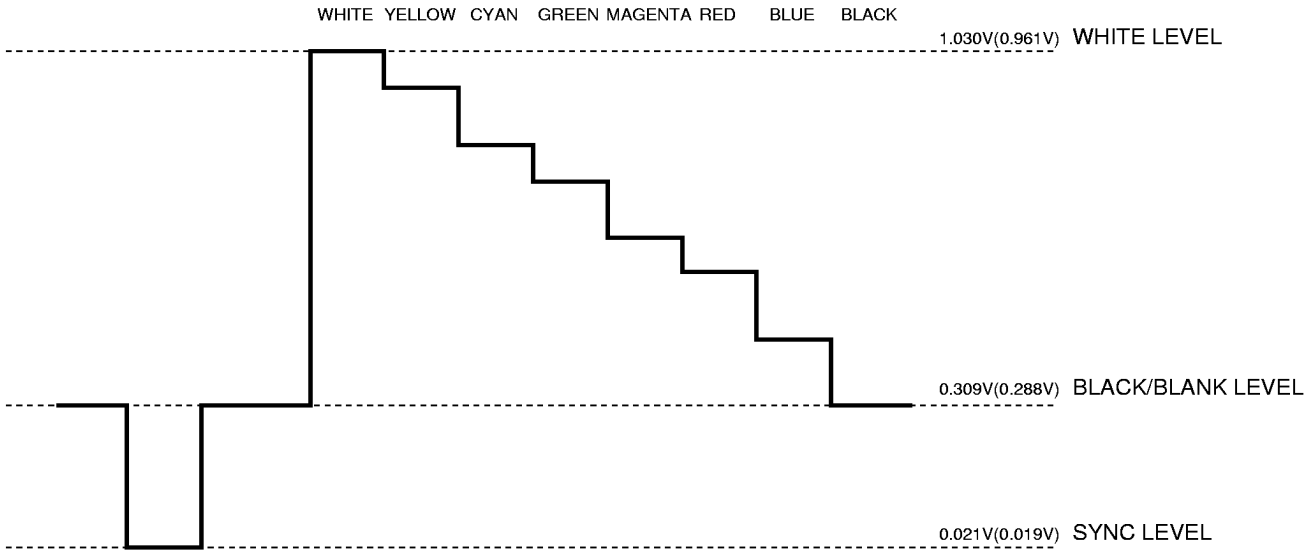
10. D/A Converter

- The 3-channel 8bit D/A converter is housed to convert luminance signal, chroma signal, and composite video signal. (Only RL5C292-001. Upon RF5C292-002, 1channel 8bit D/A converter is housed for composite video signal.)
- The D/A converter has a conversion rate of 27MHz. (two times the rate of PXCLK)
- The D/A converter allows direct driving under a load of 37.5Ω.
- Because the analog output pin for the D/A converter has high output impedance, the RL pull-down resistor (75Ω) to be connected to the output pin should be placed in the closest possible proximity to the pin.
- The phase compensation decoupling capacitor to be connected to the COMP pin for the D/A converter should also be placed in the closest possible proximity to the pin by means of a ceramic capacitor (0.1μF).
- When the dual-layer is to be used, the IREF pin and the AGND pin (pin 52) should be connected between the original AGND lines given one-point connection between the AGND pin (pin 53) and the RL pull-down resistor (75Ω) connected to the AGND pins. (refer to "Analog Pin Connection Diagram")
- The voltage reference supply is housed.

11. Detailed Diagram Showing Synchronized Waveform of Output Video Signal (Only composite video signal upon RF/RL5C292-002)

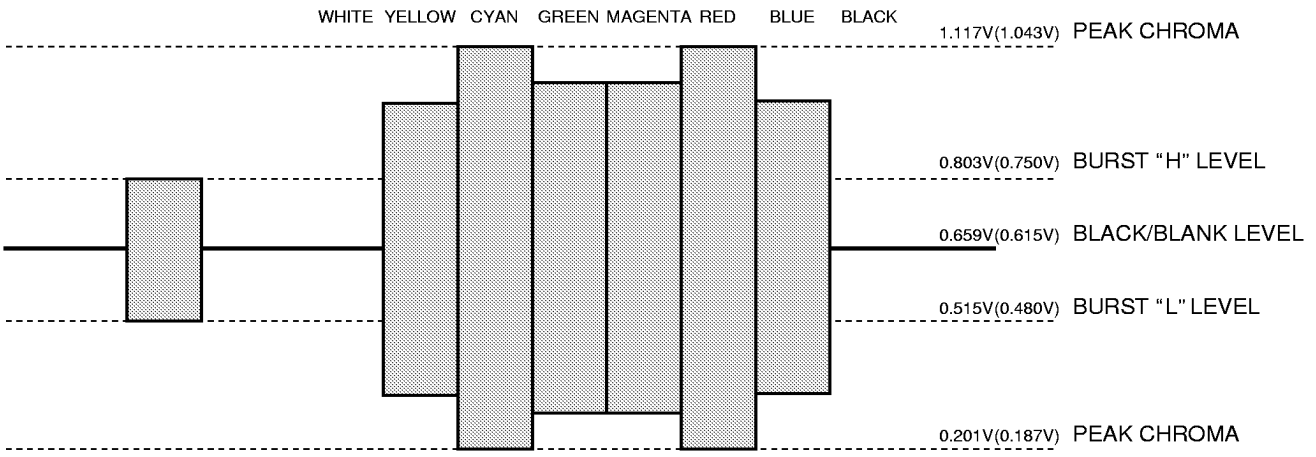
11.1 Output Waveform of Luminance Signal in NTSC Mode (Typical Condition)

Load=37.5Ω, VREF=1.23V, RSET=300Ω, AVcc=5V, 100/0/100/0 colorbar, Setup=0%
( ) : calculated as RSET=300Ω



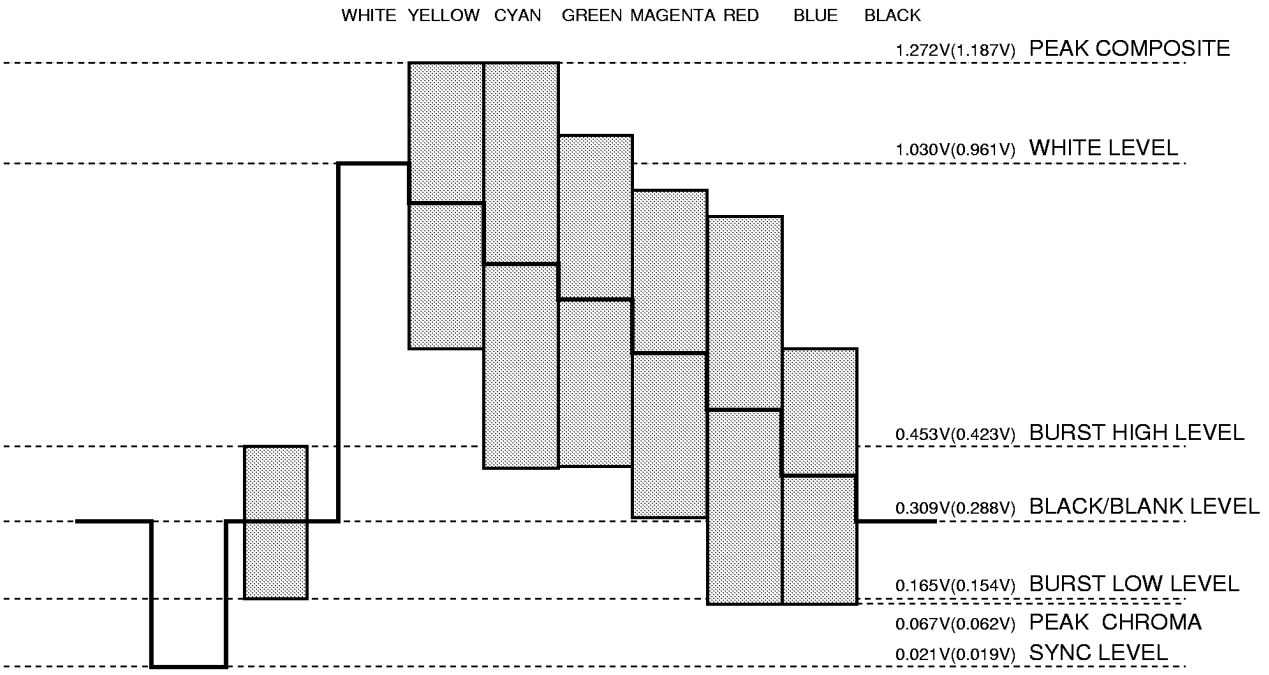
11.2 Output Waveforms of Chroma Signal in NTSC Mode (Typical Condition)

Load=37.5Ω, VREF=1.23V, RSET=300Ω, AVcc=5V, 100/0/100/0 colorbar, Setup=0%
( ) : calculated as RSET=300Ω



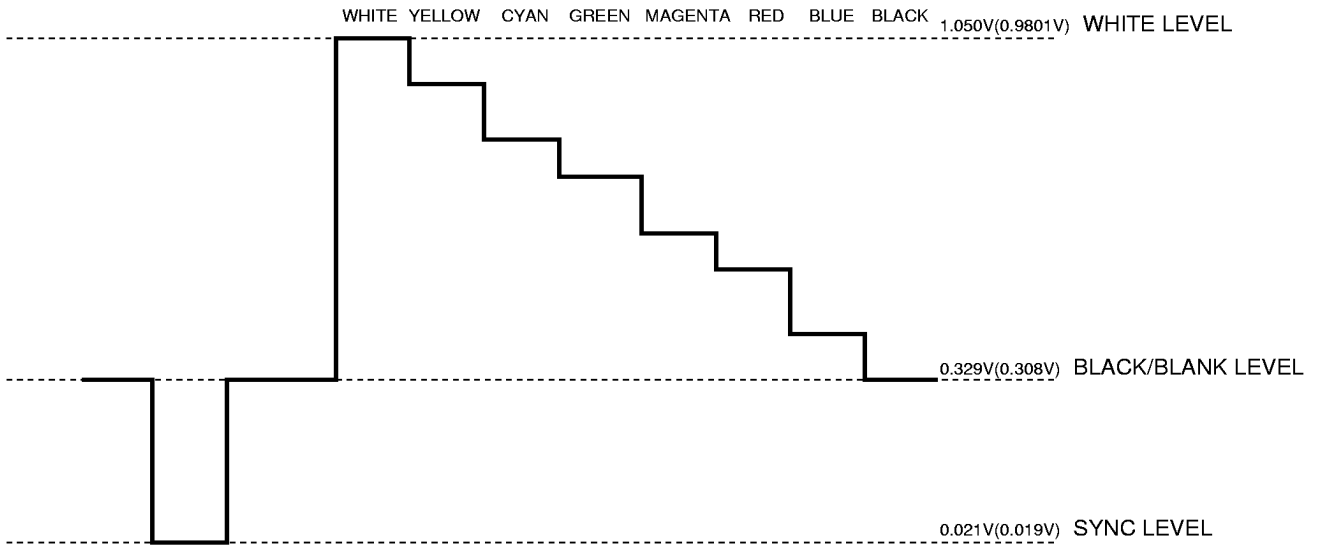
11.3 Output Waveforms of Composite Signal in NTSC Mode (Typical Condition) (only RL5C292-001)

Load=37.5Ω, V_{REF}=1.23V, R_{SET}=300Ω, AVcc=5V, 100/0/100/0 colorbar, Setup=0%
( ) : calculated as R_{SET}=300Ω



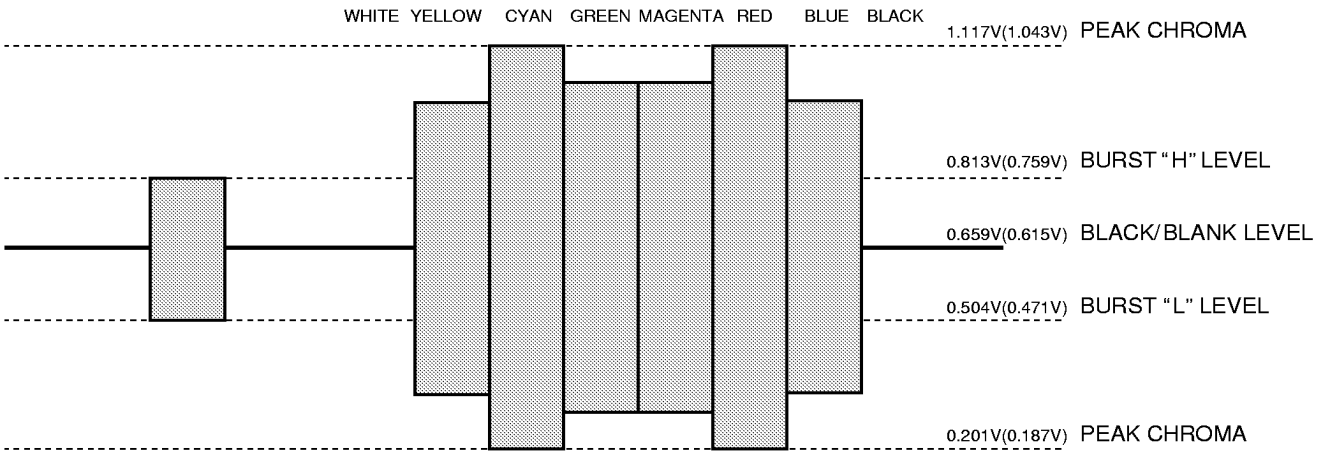
11.4 Output Waveform of Luminance Signal in PAL Mode (Typical Condition) (only RL5C292-001)

Load=37.5Ω, VREF=1.23V, RSET=300Ω, AVcc=5V, 100/0/100/0 colorbar, Setup=0%
( ) : calculated as RSET=300Ω



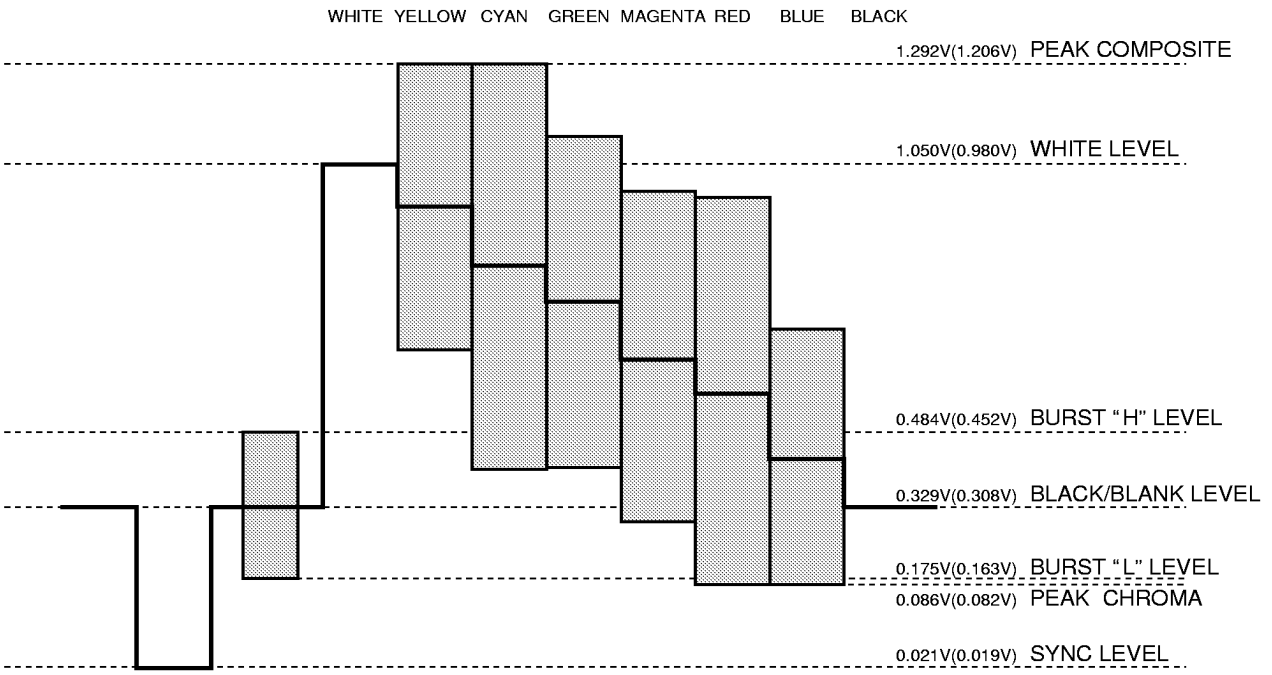
11.5 Output Waveform of Chroma Signal in PAL Mode (Typical Condition) (only RL5C292-001)

Load=37.5Ω, VREF=1.23V, RSET=300Ω, AVcc=5V, 100/0/100/0 colorbar, Setup=0%
( ) : calculated as RSET=300Ω



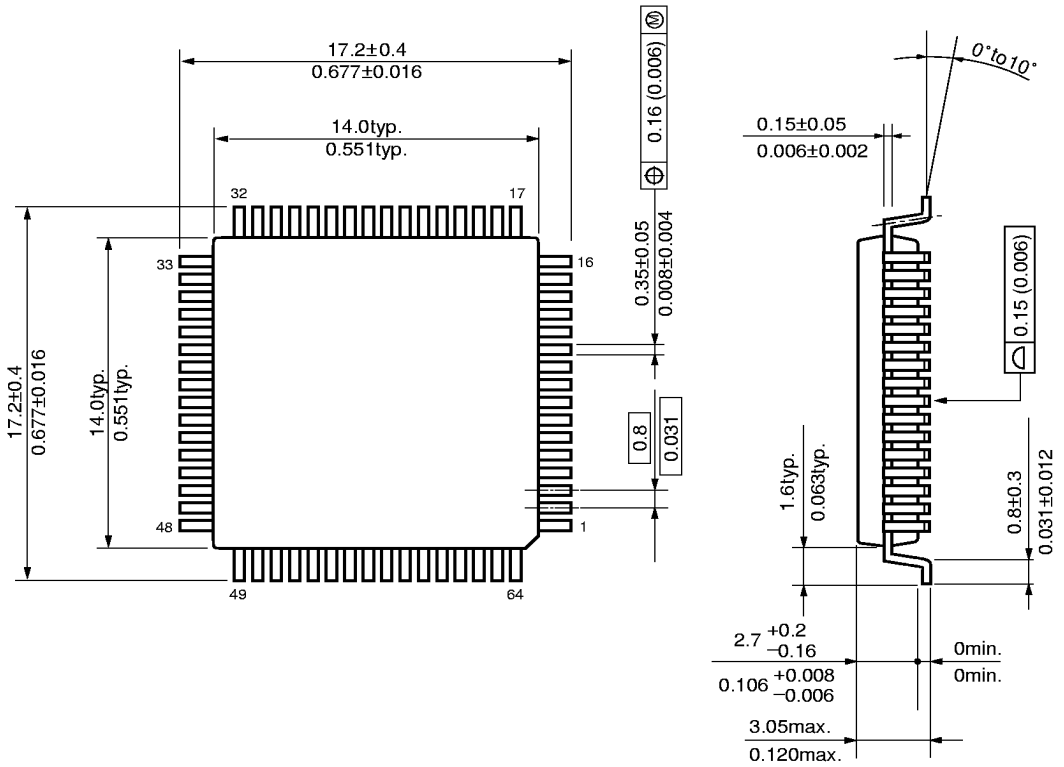
11.6 Output Waveform of Composite Video Signal in PAL Mode (Typical Condition) (only RL5C292-001)

Load=37.5Ω, V_{REF}=1.23V, R_{SET}=300Ω, AVcc=5V, 100/0/100/0 colorbar, Setup=0%
( ) : calculated as R_{SET}=300Ω



PACKAGE DIMENSIONS (Unit: mm/(inch))

• 64pin QFP



• 64pin LQFP