



REL-LABS INC. RL417
Hybrid Microelectronic Manufacturing

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ACTIVE TTL DIGITAL DELAY LINES

Industry standard delay lines are offered ranging from 25ns to 500ns. Other combinations or package style are available. Rel Labs Inc. engineering stands ready to solve your custom Delay Line Applications.

DIGITAL DELAY LINES FEATURE:

- 1) TTL Driven Inputs
- 2) TTL Buffered Outputs
- 3) Internal Terminations
- 4) Low Profile Packages (.240")
- 5) 14-Pin, DIP-IC Compatible
- 6) Output Rise Time 4.0ns max. (0.75v to 2.40v)

RECOMMENDED OPERATING CONDITIONS

(Vcc) Supply Voltage 5.00 $\pm$ 0.25VDC
(Icc) Supply Current 60ma (typ.)
(TRin) Input Rise Time 3ns.
(TWin) Input Pulse Width 40% of Delay
(Ein) Input Pulse Voltage 3.20VDC
Operating Temperature 0°C to 70°C
Storage Temperature -55°C to +125°C

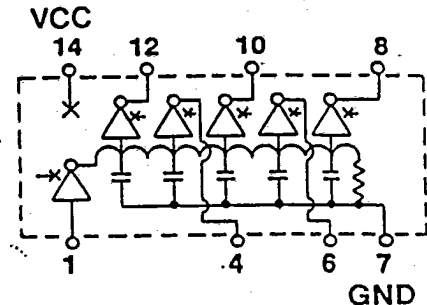
ELECTRICAL CHARACTERISTICS

PART NUMBER	TOTAL DELAY (NS) (1) (2)	TAP DELAY (NS) (1) (2)	INPUT PULSE WIDTH (NS MINIMUM)
RL- DDL-25	25	5	10
RL- DDL-30	30	6	12
RL- DDL-35	35	7	14
RL- DDL-40	40	8	16
RL- DDL-45	45	9	18
RL- DDL-50	50	10	20
RL- DDL-75	75	15	30
RL- DDL-100	100	20	40
RL- DDL-125	125	25	50
RL- DDL-150	150	30	60
RL- DDL-175	175	35	70
RL- DDL-200	200	40	80
RL- DDL-250	250	50	100
RL- DDL-300	300	60	120
RL- DDL-350	350	70	140
RL- DDL-400	400	80	160
RL- DDL-450	450	90	180
RL- DDL-500	500	100	200

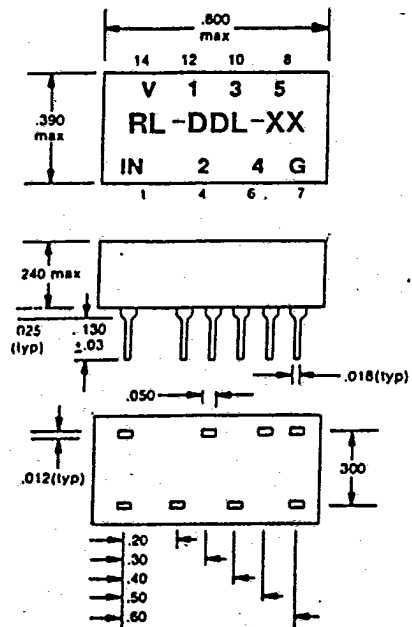
(1) Measured at 1.5V level leading edge; Vcc = 5.00VDC; No loads; at +25°C.

(2) Nominal delay, ± 2 NS or $\pm 5\%$, whichever is greater; reference to input.

SCHEMATIC / PINOUTS



PHYSICAL DIMENSIONS



ELECTRICAL CHARACTERISTICS

(VIH) High-Level Input Voltage 2.0 to 5.0V
(IIH) High-Level Input Current 50ua Max.
(VIL) Low-Level Input Voltage 0.8V Max.
(IIL) Low-Level Input Current -2ma Max.
(VOH) High-Level Output Voltage 2.4V Min.
(VOL) Low-Level Output Voltage 0.4V Max.
High-Level Output Drives 20 TTL Loads/Unit Max
Low-Level Output Drives 10 TTL Loads/Tap Max
20 TTL Loads/Unit Max