Features

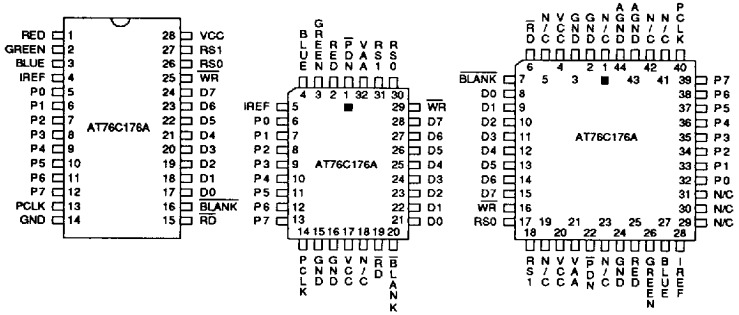
- Personal System/2*, 8514/A, and VGA* Compatible
- High Pixel Rates to 135 MHz
- Supports High Resolution 1280 x 1280 Pixels Color Graphics Displays
- Low Standby Current Less than 1 mA (Typical)
- Anti-Sparkle Circuitry
- Triple 6-Bit DACs Display 256K Possible Colors
- Pixel Word Mask and Composite Blank on All Three Channels
- 18-Bit Wide Color Palette Stores 256 Colors
- High Reliability CMOS Technology
  - 2000 V ESD Protection
  - 200 mA Latchup Immunity
- Available in Standard 28-Pin DIP, 32-Pin LCC, and 32- and 44-Pin Plastic LCC
- Full Military, Commercial and Industrial Temperature Ranges

Description

The AT76C176A is a second generation color palette DAC which provides direct drives for high resolution RGB color displays with resolutions up to 1280 x 1280 pixels. The AT76C176A integrates three high performance six-bit video DACs (Digital-to-Analog Converters), an advanced 256 x 18 Color Palette (Color Look-up Table) and a versatile microprocessor interface on a monolithic substrate.

The AT76C176A supports the RS170 video standard and graphics controllers compatible with the VGA and extended VGA standards. This device allows 256 colors to be displayed out of a total of 262,144 colors. The AT76C176A provides composite blank outputs on all three channels. Additional advanced features include on-chip anti-sparkle circuitry and pixel mask logic which allows displayed colors to be modified in a single write cycle rather than by altering the contents of the color palette. For lap-top computers and other battery powered applications, the AT76C176A provides a low power standby mode of operation.

Pin Configurations



Pin Name	Function
RED GREEN BLUE	Analog Video Outputs for R,G,B Guns
IREF	Reference Current Input
P0-P7	Pixel Address Inputs
PCLK	Pixel Clock Input
AGND	Analog Ground
GND	Ground
$\overline{RD}$	Read Enable Input

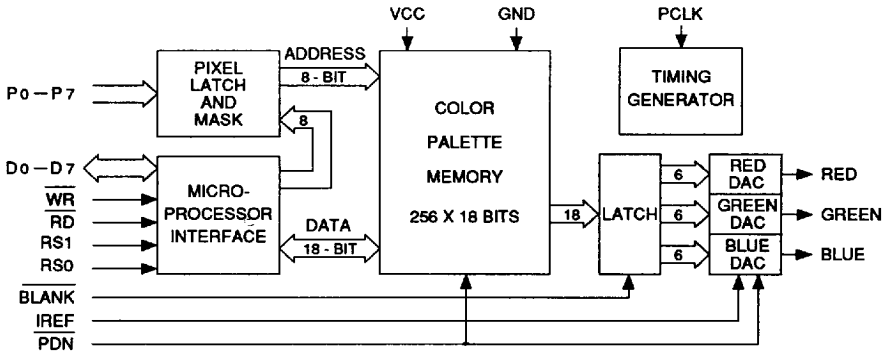
$\overline{BLANK}$	Video Blanking Input
D0-D7	Program Data I/O
$\overline{WR}$	Write Enable Input
RS0,RS1	Register Select Inputs
$\overline{PDN}$	Power-Down Input
VCC	+5 Volts Supply Input
VAA	+5 Volts Analog Supply Input
N/C	No Connect

* Personal System/2 and VGA are registered trademarks of IBM Corporation.

135 MHz Monolithic CMOS Hi-Res Video Color Palette

11

Block Diagram



Pin Definitions

	Symbol	Functional Descriptions
Video Interface	RED GREEN BLUE	Analog Video Outputs. These are the outputs of the triple video DACs. The 18-bit wide color palette output and the $\overline{\text{BLANK}}$ input drive the DAC inputs.
	IREF	Reference Current Input. The Reference Current sets the full scale current sourced by each DAC.
	P0-P7	Pixel Address Inputs. The 8-bit Pixel Address is logically AND'ed with the Pixel Mask value before it is used to select a stored 18-bit color value from the palette.
	PCLK	Pixel (or Dot) Clock Input. The rising edge of PCLK samples the Pixel Address and $\overline{\text{BLANK}}$ inputs. PCLK is the system clock for the palette DAC pipeline.
	$\overline{\text{BLANK}}$	Blanking Input. A logic "0" at $\overline{\text{BLANK}}$ input overrides the current color value and forces the Analog Video Outputs to the zero (or Blank) level. The Color Palette can be updated while Blanking is active.
Power Supply	AGND GND	Ground. Both AGND and GND should be connected to a solid ground plane in the system.
	VCC	Digital Supply. Nominal 5 Volts. VCC should be bypassed to GND with a high-frequency capacitor.
	VAA	Analog Supply. Nominal 5 Volts. VAA should be connected to a filtered system supply.
Microprocessor Interface	$\overline{\text{RD}}$	Read Enable Input. $\overline{\text{RD}}$ controls the timing of microprocessor Read operations.
	$\overline{\text{WR}}$	Write Enable Input. $\overline{\text{WR}}$ controls the timing of microprocessor Write operations. $\overline{\text{RD}}$ and $\overline{\text{WR}}$ should not be active (low) at the same time.
	D0-D7	Program Data I/O Ports (Bidirectional). The rising edge of $\overline{\text{WR}}$ latches Program Data at D7-D0 into the selected internal register. The falling edge of $\overline{\text{RD}}$ enables D7-D0 as outputs and the rising edge of $\overline{\text{RD}}$ returns D7-D0 to a high impedance state.
	RS0, RS1	Register Select Inputs. Control the selection of internal registers. (See description on Internal Registers.) The falling edge of $\overline{\text{RD}}$ or $\overline{\text{WR}}$ latches in the value at RS1, RSO.
	$\overline{\text{PDN}}$	Power-Down Input. A logic "0" at $\overline{\text{PDN}}$ input powers down the video DAC and Color Palette circuits for low power standby mode operation. The Color Palette can still be read or updated if PCLK is active. $\overline{\text{PDN}}$ should be held at logic "1" for normal operation.

Internal Registers

RS1	RS0	Bits	Register Name	Functional Description
0	0	8	Pixel Address (Write Mode)	The Pixel Address Register is accessed via Register Address (0,0) or (1,1). Reading the Pixel Address value from (0,0) is the same as reading from (1,1). A pixel address value is normally written to Pixel Address Register at (0,0) before one or more color values are written to the Color Palette. A pixel address value is normally written to Pixel Address Register at (1,1) before one or more color values are read from the Color Palette.
1	1	8	Pixel Address (Read Mode)	
0	1	18	Color Value	The Color Value Register acts as a buffer between the 18-bit wide Color Palette and the 8-bit microprocessor interface. Each READ and WRITE at (0,1) consists of three byte transfers in the order of RED first, GREEN second and BLUE last. Only the LSBs D5-D0 of each byte are used, the two MSBs are set to "0" when a color value is read. The Pixel Address Register automatically increments after each 18-bit color value READ or WRITE operation. Each color value READ or WRITE operation overrides the pixel stream for one PCLK period.
1	0	8	Pixel Mask	The Pixel Mask value is bitwise AND'ed with the Pixel Address value at P7-P0. A "1" in a position of the Pixel Mask will not change the corresponding bit in the Pixel Address, while a "0" sets that bit to "0". Pixel Address supplied via the microprocessor interface is not affected by the Pixel Mask.

Device Operation

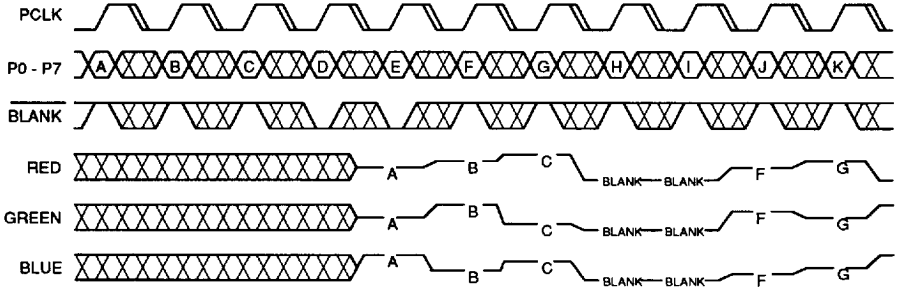
COLOR PALETTE: The AT76C176A provides an 18-bit wide by 256-word deep color palette static RAM array for storing the desired color intensity values. Each word is divided into three fields for the RED, GREEN and BLUE video DACs respectively. The eight-bit wide Pixel Address is decoded and used to select a particular location in the RAM array. The color value retrieved from that location is then used as inputs to the three video DACs which convert the digital color code into analog color intensity values.

The AT76C176A achieves low power, high speed operation by using an advanced pipelined palette DAC architecture. Delay from Pixel Address to color intensity value out is three PCLK periods.

MPU INTERFACE: The AT76C176A provides a standard microprocessor interface which allows the host display controller to access the Color Palette RAM and all internal registers of the AT76C176A. MPU READ and WRITE operations are internally synchronized with the video pipeline and therefore can take place asynchronously from the normal pixel mapping operation. An on-chip address counter allows the MPU to READ or WRITE the Color Palette in a Block Mode.

11

Video Pipeline Timing Diagram



COLOR PALETTE READ AND WRITE: Four MPU operations are required to write (i.e. store a Color Value) to a specific location in the Color Palette RAM. The desired RAM address is first written into the internal Pixel Address register by executing a WRITE operation at register address (0,0). A new Color Value is next written into the internal Color Value register at register address (0,1) by three consecutive WRITE operations, with the RED color first, GREEN second and BLUE last. Only LSBs D5-D0 of each byte transferred are used. The new Color Value is then automatically written into the designated address in the Color Palette RAM.

Similarly, four MPU operations are required to read a Color Value from a specific location in the Color Palette RAM. The RAM address is written into the internal Pixel Address register by executing a WRITE operation at register address (1,1). The Color Value stored in that particular RAM location is automatically transferred to the internal Color Value Register. Three consecutive READ operations are then required to read the retrieved Color Value in three bytes, with the RED color first, GREEN second and BLUE last. Only the last six LSBs D5-D0 contain valid data, the two MSBs are set to "0".

BLOCK READ AND WRITE MODE: The on-chip Pixel Address Register automatically increments by one after each complete Color Value READ or WRITE operation. This useful feature allows an entire block of the Color Palette RAM to be accessed by simply writing the starting address into the Pixel Address register at the appropriate register address. Subsequent READ or WRITE operations require only three-byte transfers at D7-D0.

ANTI-SPARKLE CIRCUITRY: The outputs of the Color Palette RAM drive the inputs of the video DACs via an 18-bit anti-sparkle register. Whenever a Read or Write is performed on the Color Palette through the MPU interface, the anti-sparkle register substitutes the latest pixel Color Value with the previous pixel Color value. Since the Color Value may be corrupted when the Color Palette is accessed during active display, this feature minimizes and often eliminates any visible sparkles on the video display. The anti-sparkle circuitry makes unrestricted access to the Color Palette RAM viable.

TRIPLE VIDEO DAC: Each of the three video DACs on the AT76C176A consists of an array of current sources tied to a common output. The current sources use an advanced current steering scheme to minimize glitch energy. The number of current sources in each DAC steered to the output during any PCLK period equals the value represented by the Color Value selected from the Color Palette. The rest of the current sources are steered to ground.

The input Reference Current (IREF) determines the current in each current source. Each DAC is designed to produce 0.7-volt peak white level when driving a doubly terminated 75-ohm load with IREF = -8.88 mA. The relationship between the peak white level and IREF is given by the equation:

$V_{Peak\ White} = 2.1 \times IREF \times R_{Load}$

BLANKING: The AT76C176A supports composite blanking at all three RED, GREEN and BLUE video outputs. The $\overline{BLANK}$ input is latched on the rising edge of PCLK and affects the analog video outputs after three PCLK periods. An internal pipelined delay circuit is used to synchronize the $\overline{BLANK}$ input with the normal pixel pipeline. A logic "0" at $\overline{BLANK}$ input overrides the current color value and forces the analog video outputs to the zero (or Blank) level. The $\overline{BLANK}$ circuit has no effect on the MPU interface and the Color Palette remains accessible via READ and WRITE.

PIXEL MASK: The AT76C176A features an advanced on-chip Pixel Mask which is very useful for cursor control, flashing objects, and animation. The Pixel Mask value stored in internal register (1,0) is bitwise AND'ed with the input Pixel Address value at P7-P0 to form the actual RAM address for the Color Palette. A "1" in a position of the Pixel Mask will not change the corresponding bit in the Pixel Address, while a "0" sets that bit to "0". Pixel Addresses supplied via the MPU interface are not affected by the Pixel Mask.

POWER-DOWN MODE: In PLCC packages, the AT76C176A provides an on-chip power-down feature for use in lap-top computers and other battery-powered applications. During normal operation, pin $\overline{PDN}$ should be held as logic "1." A logic "0" at $\overline{PDN}$ powers down the video DAC and Color Palette circuits.

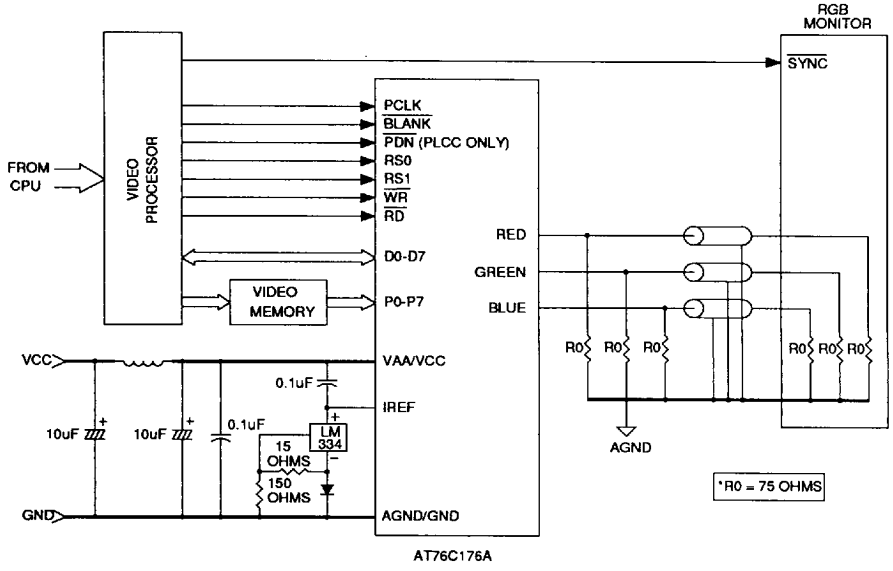
Absolute Maximum Ratings*

Temperature Under Bias	-55°C to 125°C
Storage Temperature	-65°C to 150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to 7.0 V(1)
Power Dissipation	1.5 W
Reference Current	-15 mA
Analog Output Current	45 mA
DC Digital Output Current	25 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum voltage is -0.6 V DC which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is VCC+0.75 V DC which may overshoot to 7.0 V for pulses of less than 20 ns.

Sample Connection for Typical Application



System Implementation Considerations

POWER SUPPLY DECOUPLING AND GROUNDING: To obtain the cleanest possible analog outputs from the AT76C176A, digital noise coupling into the analog signal paths needs to be minimized. The video data paths, power supply lines and ground planes on the circuit board should be laid out carefully to reduce noise coupling. As illustrated in the diagram above (Sample Connection for Typical Application), a separate VAA line decoupled to AGND with an electrolytic capacitor in parallel with a smaller ceramic chip capacitor should be used for the analog circuits on the AT76C176A. Similarly, a separate analog ground return, AGND, which is connected to the lowest impedance point in the system ground plane, should be used.

For best results, four-layer PC boards with separate ground and power supply planes are recommended. The AGND plane should be laid out as an island or tub underneath the AT76C176A. All video frequency signal traces should be kept as short as possible to minimize radiation and all decoupling capacitors should be placed as close to the AT76C176A as the layout rules permit.

Noise and transients on the power and ground lines can be coupled or aliased into the video circuits by the switching action of the AT76C176A. For applications at 66 MHz and above, it may be necessary to isolate both VAA and AGND from the system supplies with inductors of appropriate values.

CURRENT REFERENCE: The maximum full scale output of the video DACs is determined by the reference current supplied externally at pin IREF. An adjustable current source such as the LM334 is recommended to set the reference current at 8.88 mA for a full scale output of 0.7 volt when driving a 37.5-ohm load. The video DACs employ current sources which are referenced to the positive supply voltage. A high quality 0.1-µF chip capacitor may be required to decouple IREF to VAA or VCC.

VIDEO INTERFACE: The RED, GREEN and BLUE video outputs are designed to drive doubly terminated 75-ohm lines. To minimize ringing due to impedance mismatch, 75-ohm ± 1% thin film resistors should be placed close to the AT76C176A on the PC board.

To comply with FCC RF emission regulations, ferrite beads can be inserted at the video outputs to limit the amount of high frequency emission. The AT76C176A is designed to produce very little high frequency digital feedthrough.

SYSTEM TIMING: The pixel clock, PCLK, controls the timing of the Color Palette and the Video DACs. To obtain the highest quality display possible with the AT76C176A, Setup and Hold time requirements with respect to PCLK should be strictly adhered to. The duty cycle limits of PCLK should also be met over the entire display.

DIGITAL INTERFACE: When the high impedance digital inputs of the CMOS AT76C176A are driven by low impedance sources, considerable ringing can occur, which may degrade high video rate operation. Impedance matching resistors of the order of 50 ohms can be inserted in series at the inputs to the Pixel Address and Blanking inputs to reduce ringing. This also minimizes the amount of high frequency emission due to excessively high slew rates at the video data inputs.

D.C. and A.C. Operating Range

		AT76C176A-13 AT76C176A-11	AT76C176A-80	AT76C176A-66 AT76C176A-50	VCC/VAA Power Supplies
Operating Temperature Range(Case)	Com.	0° C - 70° C			5 V ± 5%
			0° C - 70° C	0° C - 70° C	5 V ± 10%
	Ind.		-40° C - 85° C	-40° C - 85° C	5 V ± 10%
	Mil.			-55° C -125° C	5 V ± 5%

D.C. Characteristics

Symbol	Parameter	Conditions	All Min	50 MHz Max	66 MHz Max	80 MHz Max	110 MHz Max	135 MHz Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+0.1 V		10	10	10	10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC} + 0.1 V		10	10	10	10	10	µA
I_{CC}	Power Supply Current	IO = 21 mA, $\overline{PDN}$ = V_{IH} Digital Outputs Open		170	190	210	240	265	mA
I_{SB}	Standby Supply Current	$\overline{PDN}$ = V_{IL} Digital Inputs = V_{IH} / V_{IL}			10	10	10	10	mA
I_{ILP}	Current Sourced by Pin PDN	$\overline{PDN}$ = V_{IL}			20	20	20	20	µA
I_{REF}	Reference Current		-7	-10	-10	-10	-10	-10	mA
V_{IL}	Input Low Voltage		-0.5	0.8	0.8	0.8	0.8	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}+0.5	V_{CC}+0.5	V_{CC}+0.5	V_{CC}+0.5	V_{CC}+0.5	V
V_{OL}	Output Low Voltage	IO = 5 mA		0.4	0.4	0.4	0.4	0.4	V
V_{OH}	Output High Voltage	IO = -5 mA	2.4						V
V_{REF}	Voltage at IREF Input		V_{CC}-3	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V

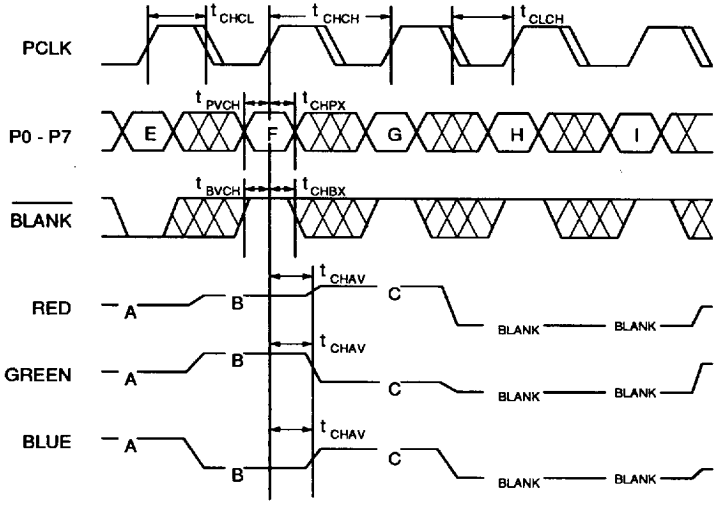
Video DAC Characteristics

Symbol	Parameter	Conditions	All Min	All Typ	50 MHz Max	66 MHz Max	80 MHz Max	110 MHz Max	135 MHz Max	Units
RES	Resolution		6							bits
ILE	Integral Linearity Error	Note A			±0.5	±0.5	±0.5	±0.5	±0.5	LSB
COR	DAC to DAC Correlation	Note B			±2	±2	±2	±2	±2	%
FSE	Full Scale Error	Note C			±5	±5	±5	±5	±5	%
DVT	Glitch Energy	Notes D, E		75						pVsec
IO	Output Current	VO < 1 V		18.6	21	21	21	21	21	mA
VO	Output Voltage	IO < 21 mA		0.7	1.5	1.5	1.5	1.5	1.5	V
t_{DR}	Rise Time (10% to 90%)	Notes D, E			8	6	6	5	4	ns

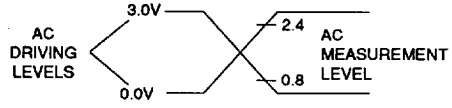
Video Timing Characteristics

Symbol	Parameter	Conditions	All Max	50 MHz Min	66 MHz Min	80 MHz Min	110 MHz Min	135 MHz Min	Units
t_{CHCH}	PCLK Period (τ)	Normal	10000	20	15	12.5	9	7.4	ns
Δt_{CHCH}	PCLK Jitter	$t_{CHCH} = \tau$	±2.5						%
t_{CLCH}	PCLK Low Width	Normal	10000	6	5	5	4	3.2	ns
t_{CHCL}	PCLK High Width	Normal	10000	6	5	5	4	3.2	ns
t_{PVCH}	Pixel Word Setup Time			4	3	3	3	2.5	ns
t_{CHPX}	Pixel Word Hold Time			4	3	3	2	2	ns
t_{BVCH}	$\overline{\text{BLANK}}$ Setup Time			4	3	3	3	2.5	ns
t_{CHBX}	$\overline{\text{BLANK}}$ Hold Time			4	3	3	2	2	ns
t_{CHAV}	PCLK to DAC Output Valid	Note G	30	5	5	5	5	5	ns
Δt_{CHAV}	Differential Output Delay	Note H	2						ns
t_{CC}	Pixel Clock Transition Time		50						ns

Video Timing Waveforms Diagram

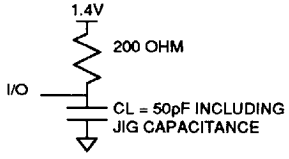


Input Test Waveforms



Notes: 1. t_R, t_F <3 ns (10% to 90%).
2. Input timing reference is at 1.5 V.

Digital Input/Output Load



MPU Interface Timing Characteristics

Symbol	Parameter	Conditions	All Max	66/50 MHz Min	80 MHz Min	110 MHz Min	135 MHz Min	Units
tWLWH	$\overline{WR}$ Pulse Width Low			50	50	50	50	ns
tRLRH	$\overline{RD}$ Pulse Width Low			50	50	50	50	ns
tSVWL	Register Select Setup Time	WRITE Operations		10	10	10	10	ns
tSVRL	Register Select Setup Time	READ Operations		10	10	10	10	ns
tWLSX	Register Select Hold Time	WRITE Operations		10	10	10	10	ns
tRLSX	Register Select Hold Time	READ Operations		10	10	10	10	ns
tDVWH	Write Data Setup Time			10	10	10	10	ns
tWHDX	Write Data Hold Time			10	10	10	10	ns
tRLQX	Output Turn-on Delay			5	5	5	5	ns
tRLQV	Read Enable Access Time		40					ns
tRHQX	Output Hold Time			5	5	5	5	ns
tRHQZ	Output Turn-off Delay	Note I	20					ns
tWHWL1	Successive Write Interval	τ = PCLK Period		4τ	4τ	4τ	4τ + 5	ns
tWHRL1	Write Followed by Read Interval	τ = PCLK Period		4τ	4τ	4τ	4τ + 5	ns
tRHRL1	Successive Read Interval	τ = PCLK Period		4τ	4τ	4τ	4τ + 5	ns
tRHWL1	Read Followed by Write Interval	τ = PCLK Period		4τ	4τ	4τ	4τ + 5	ns
tWHWL2	Write After Color Write	τ = PCLK Period		4τ	4τ	4τ	4τ + 5	ns
tWHRL2	Read After Color Write	τ = PCLK Period		4τ	4τ	4τ	4τ + 5	ns
tRHRL2	Read After Color Read	τ = PCLK Period		7τ	7τ	7τ	4τ + 5	ns
tRHWL2	Write After Color Read	τ = PCLK Period		7τ	7τ	7τ	4τ + 5	ns
tWHRL3	Read After Read Address Write	τ = PCLK Period		7τ	7τ	7τ	4τ + 5	ns

Notes

Note A: Measured from best fit line through DAC transfer curve.

Note B: Measured from the mid point of the distribution of the three DAC transfer curves.

Note C: $FSE = \left[\frac{VO - 2.1 \times IREF \times R_{Load}}{2.1 \times IREF \times R_{Load}}\right] \times 100\%$

Note D: Z_{Load} = 37.5 ohm + 30 pF, IREF = -8.88 mA

Note E: This parameter is sampled and not 100% tested.

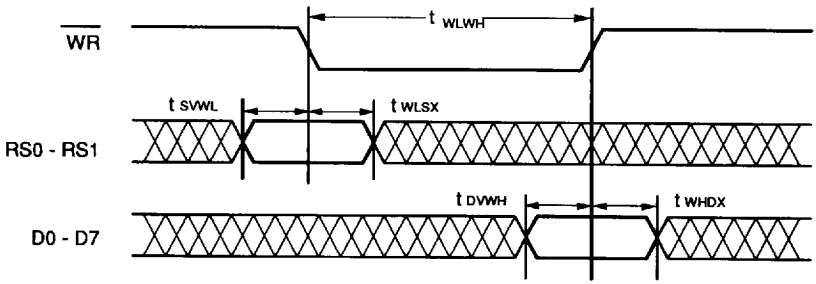
Note F: Measured from a 2% change in the DAC output voltage to within 2% of the final value.

Note G: Measured between the 50% point of the rising edge of PCLK and at the analog output halfway between successive output values.

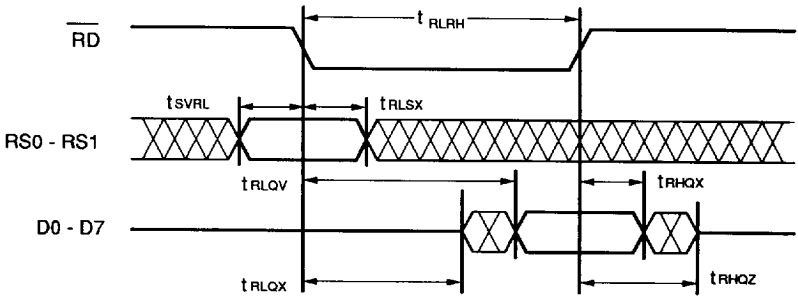
Note H: Measured between different analog outputs on the same device.

Note I: Measured at ±200 mV from steady state output values.

Write Operations Waveforms

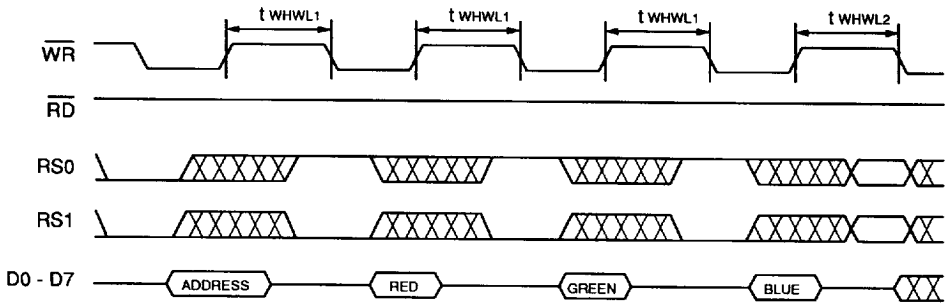


Read Operations Waveforms

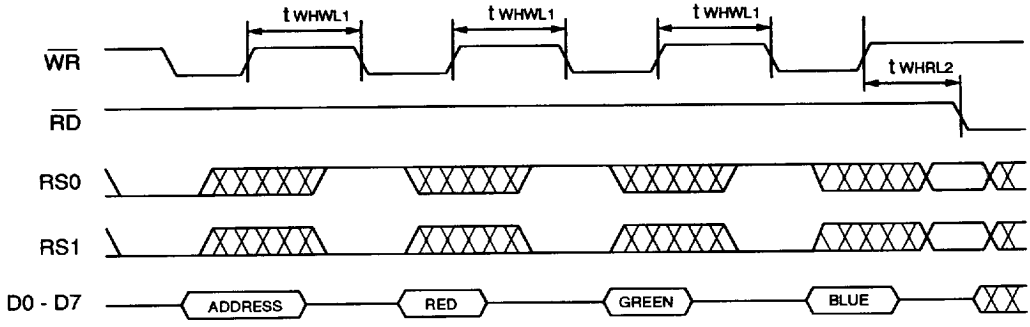


11

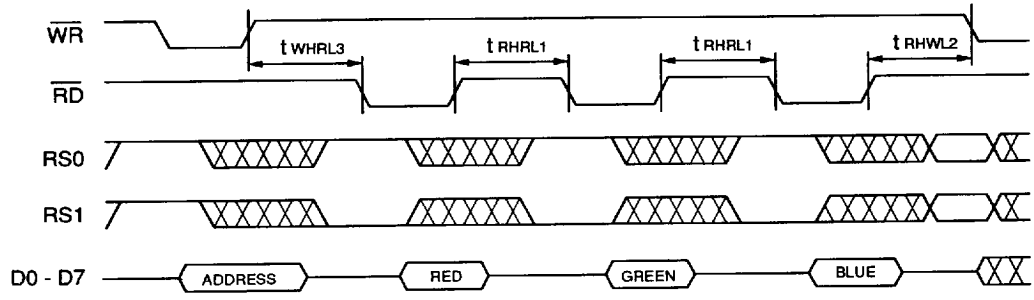
A.C. Waveforms for Color Value Write Followed by Any Write



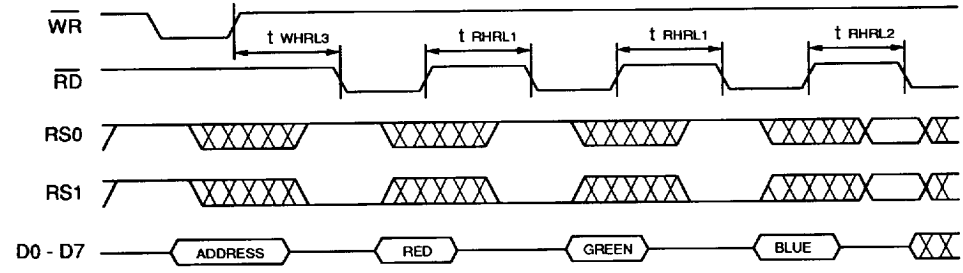
A.C. Waveforms for Color Value Write Followed by Any Read



A.C. Waveforms for Color Value Read Followed by Any Write

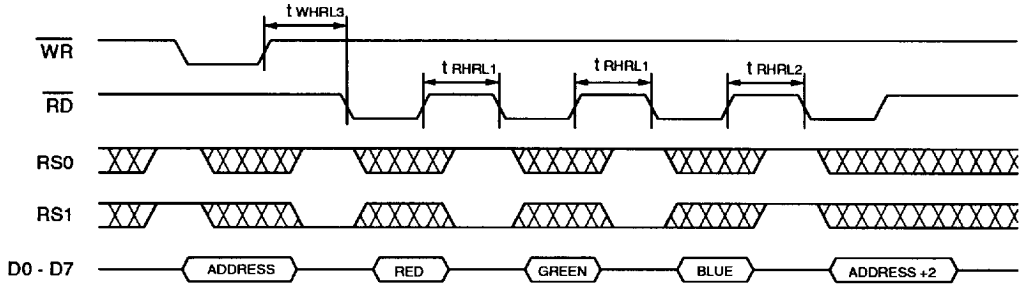


A.C. Waveforms for Color Value Read Followed by Any Read

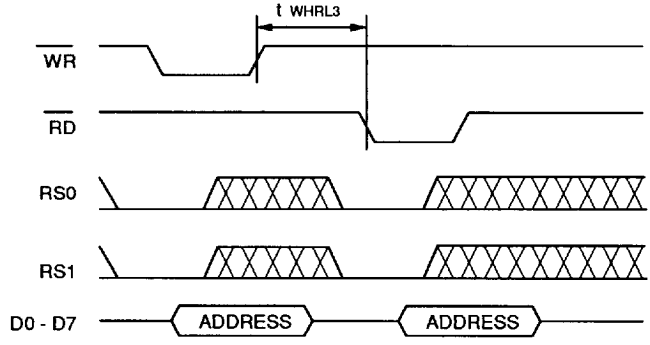


A.C. Waveforms for Color Value Read

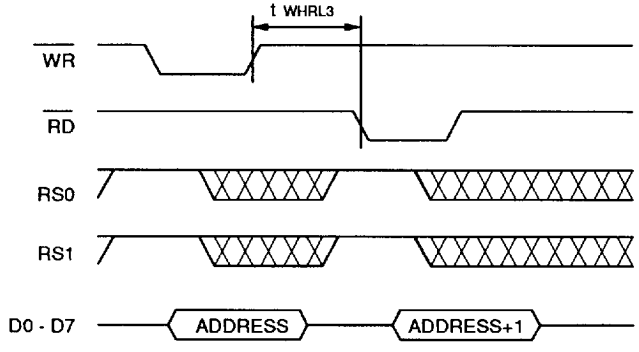
Followed by Pixel Address (Read Mode) Read



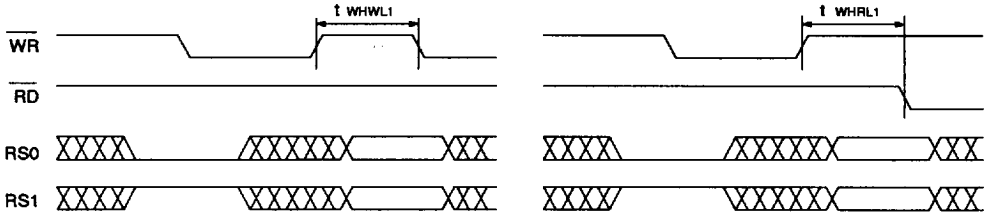
A.C. Waveforms for Pixel Address (Write Mode) Write and Read Back



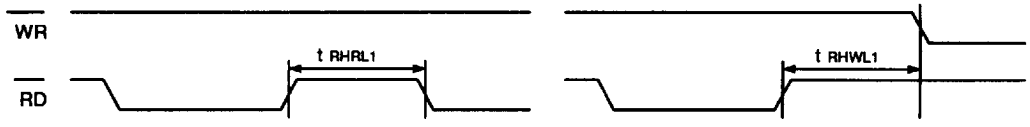
A.C. Waveforms for Pixel Address (Read Mode) Write and Read Back



A.C Waveforms for Pixel Mask Write Followed by Any Write or Read



A.C. Waveforms for Pixel Mask or Pixel Address Read Followed by Any Read or Write



Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
50	±10%	AT76C176A-50PC AT76C176A1-50JC AT76C176A2-50JC	28P6 32J 44J	Commercial (0°C to 70°C)
		AT76C176A-50PI AT76C176A1-50JI AT76C176A2-50JI	28P6 32J 44J	Industrial (-40°C to 85°C)
50	±5%	AT76C176A-50DMB AT76C176A-50LMB	28D6 32L	Military (-55°C to 125°C)
66	±10%	AT76C176A-66PC AT76C176A1-66JC AT76C176A2-66JC	28P6 32J 44J	Commercial (0°C to 70°C)
		AT76C176A-66PI AT76C176A1-66JI AT76C176A2-66JI	28P6 32J 44J	Industrial (-40°C to 85°C)
66	±5%	AT76C176A-66DMB AT76C176A-66LMB	28D6 32L	Military (-55°C to 125°C)
80	±10%	AT76C176A-80PC AT76C176A1-80JC AT76C176A2-80JC	28P6 32J 44J	Commercial (0°C to 70°C)
		AT76C176A-80PI AT76C176A1-80JI AT76C176A2-80JI	28P6 32J 44J	Industrial (-40°C to 85°C)
110	±5%	AT76C176A-11PC AT76C176A1-11JC AT76C176A2-11JC	28P6 32J 44J	Commercial (0°C to 70°C)

11

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
44J	44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)