80C51 MCUs

AT83C51RB2
AT83C51RC2
AT83C51IC2
AT80C51ID2
Errata Sheet

Active Errata List

- **During UART Reception, Clearing REN May Generate Unexpected IT**
- **SPI Interface - Transmission on Master Mode**
- **SPI Interface - SPI SS pin Limitation on Master/Slave**
- **SPI - SPI Slave Responding in a Multislave Configuration When Not Selected by the Master and its SPDAT Register Loaded**
- **SPI - SPI Slave Not Responding When Selected and Not Loaded**
- **ALE Disabled Toggles During Internal MOVX**
- **Timer 2 - Baud Rate Generator - No IT When TF2 is Set by Software**
- **Timer 2 - Baud Rate Generator - Long Start Time**
- **SPI Slave Mode/Data Corrupted**
- **32 kHz Oscillator for AT83C51IC2/T80C51ID2 Needs External Feed Back Resistor**
- **RB8 Lost With JBC on SCON**
- **C51 Core – Bad Exit of Power-down in X2 Mode**

Errata History

Rev	Lot Number	1st Prod.	Trouble List
A	above 00395	Nov 2001	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11

Errata Descriptions

1. During UART Reception, Clearing REN May Generate Unexpected IT

During UART reception, if the REN bit is cleared between a start bit detection and the end of reception, the UART will not discard the data (RI is set).

Workaround

Test REN at the beginning of Interrupt routine just after CLR RI, and run the Interrupt routine code only if REN is set.

2. SPI Interface - Transmission on Master Mode

A 9th bit is transmitted by the interface when the clock rate is set on divide by 2 mode and a positive polarity is selected; the SPR2, SPR1, SPR0 bits are cleared (000) and CPOL = 1 on the SPCON register.

Workaround

Set the clock rate divide by 4 and X2 mode.

3. SPI Interface - SPI SS pin Limitation on Master/Slave

The SS pin of the SPI does not return to an I/O when a One-to-One Master/Slave intercommunication is performed.

Workaround

No

4. SPI - SPI Slave Responding in a Multislave Configuration When Not Selected by the Master and its SPDAT Register Loaded

In a multislave configuration, if the master is sending the Sck and the Tx data to all the slaves, and only one slave is selected, the non-selected slaves respond and generate the end of the transmission interruption (SPIF) if their SPDAT registers are loaded before the transmission.

Workaround

No

4242A–8051–07/03

5. SPI - SPI Slave Not Responding When Selected and Not Loaded

SPI Slave does not respond when selected by a Master and no Data is loaded to be transmitted. No Rx data is registered and no SPIF interruption is generated at the end of the Transmission.

Workaround

No

6. ALE Disabled Toggles During Internal MOVX

When ALE is disabled, internal MOVX instruction shows toggle of ALE.

Workaround

No

7. Timer 2 - Baud Rate Generator - No IT When TF2 is Set by Software

When timer 2 is used in baud rate generator mode, setting TF2 by software doesn't generate an interrupt.

Workaround

Use timer 1 instead of timer 2 to generate baud rate and interrupt.

8. Timer 2 - Baud Rate Generator - Long Start Time

When timer 2 is used as baud rate generator, TH2 is not loaded with RCAP2H at the beginning, then UART is not operational before 10000 machine cycles.

Workaround

Add the initialisation of TH2 and TL2 in the initialisation of timer 2.

9. SPI Slave Mode/Data Corrupted

When SPI macro is configured in slave reception mode, the SPI block does not handle the good data on the SPI bus.

Workaround

No

10. 32 kHz Oscillator for AT83C51IC2/T80C51ID2 Needs External Feed Back Resistor

Internal feed back resistor is not connected, thus to start up, the 32 kHz Oscillator an external resistor is required.

Workaround

Connect between XTALB1 and XTALB2 a 2 MΩ resistor

11. RB8 Lost With JBC on SCON

On C51 when using JBC instruction on any bit of SCON register, if RB8 bit changes from "1" to "0" during JBC the "0" is lost and RB8 keeps "1".

Workaround

The workaround is to clear RB8.

In a polling algorithm you must clear RB8 at the beginning of the code and after each time it goes to "1".

Interrupt RB8 must be cleared at the beginning of the code and after each time it goes to "1".

12. C51 Core – Bad Exit of Power-down in X2 Mode

When exiting power-down mode by interrupt while CPU is in X2 mode, it leads to bad execution of the first instruction run when CPU restarts.

Workaround

Set the CPU in X1 mode directly before entering power-down mode.

Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/ High Speed Converters/RF Datacom
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

Printed on recycled paper.

4242A–8051–07/03 /xM