RM912

Power Amplifier Module, 3–4 Volts, for CDMA/AMPS (824–849 MHz)

The RM912 dual-mode Code Division Multiple Access (CDMA)/Advanced Mobile Phone Service (AMPS) Power Amplifier is a fully matched 6-pin surface mount module designed for mobile units operating in the 824-849 MHz cellular bandwidth. This device meets stringent IS95 CDMA linearity requirements to beyond 28 dBm output power and can be driven to power output levels beyond 31 dBm for high efficiency FM mode operation. A single GaAs Microwave Monolithic Integrated Circuit (MMIC) contains all active circuitry in the module. The MMIC contains on-board bias circuitry, as well as input and interstage matching circuits. The output match is realized off-chip within the module package to optimize efficiency and power performance into a 50 Ω load. This device is manufactured with Conexant's Gallium Arsenide (GaAs) heterojunction bipolar transistor (HBT) process that provides for all positive voltage DC supply operation while maintaining high efficiency and good linearity. Primary bias to the RM912 can be supplied directly from a three cell nickel-cadmium, single cell lithium-ion, or other suitable battery with an output in the 3-4 volt range. Power down is accomplished by setting the voltage on the low current reference pin to zero volts. No external supply side switch is needed as typical "off" leakage is a few microamperes with full primary voltage supplied from the battery.

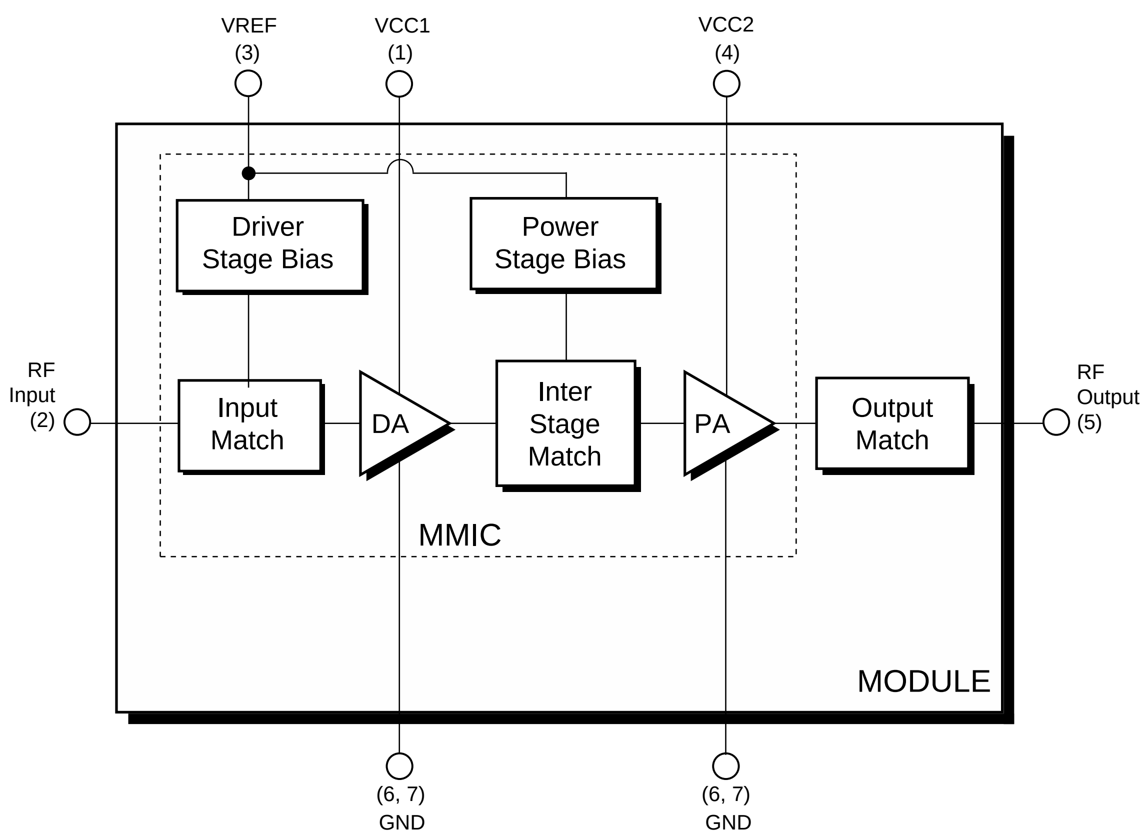
Distinguishing Features

- Low voltage positive bias supply
- Good linearity
- High efficiency
- Dual mode operation
- Large dynamic range
- 6-pin package (6 x 6 x 1.5 mm)
- Power down control

Applications

- Digital cellular (CDMA)
- Analog cellular (AMPS)
- Wireless local loop

Functional Block Diagram



Electrical Specifications

The following tables list the electrical characteristics of the RM912 Power Amplifier. Table 1 lists the absolute maximum ratings for continuous operation. Table 2 lists the recommended operating conditions for achieving the electrical performance listed in Table 3. Table 3 lists the electrical performance of the RM912 Power Amplifier over the recommended operating conditions.

Table 1. Absolute Maximum Ratings[(1)]

Parameter	Symbol	Minimum	Nominal	Maximum	Unit
RF Input Power	Pin	—	3.0	6.0	dBm
Supply Voltage	Vcc	—	3.4	6.0	Volts
Reference Voltage	Vref	—	3.0	3.3	Volts
Case Operating Temperature	Tc	–30	25	+110	°C
Storage Temperature	Tstg	–55	—	+125	°C

NOTE(S):
(1) No damage assuming only one parameter is set at limit at a time with all other parameters set at or below nominal value.

Table 2. Recommended Operating Conditions

Parameter	Symbol	Minimum	Nominal	Maximum	Unit
Supply Voltage	Vcc	3.2	3.4	4.2	Volts
Reference Voltage	Vref	2.9	3.0	3.1	Volts
Operating Frequency	Fo	824.0	836.5	849.0	MHz
Operating Temperature	To	–30	+25	+85	°C

Table 3. Electrical Specifications for CDMA / AMPS Nominal Operating Conditions[(1)]

Characteristics	Condition	Symbol	Minimum	Typical	Maximum	Unit
Quiescent current	Vref = 3.0 V Vref = 2.9 V	I_q I_q	— —	100.0 80.0	— —	mA mA
Leakage current	Vref = 0 V Vcc = 3.4 V	I_{lk}	—	—	4.0	µA
Gain–Digital	Po = 0 dBm Po = 28 dBm	G G_p	26.0 26.0	28.0 29.0	31.0 32.5	dB dB
Gain–Analog	Po = 31 dBm	Gp	26.0	28.0	31.9	dB
Power Added Efficiency Analog Mode Digital Mode	 Po = 31 dBm Po = 28 dBm	 PAEa PAEd	 42.0 31.0	 45.0 34.0	 — —	 % %
Adjacent Channel Power[(2)] 885 kHz Offset 1980 kHz Offset	 Po ≤ 28 dBm Po ≤ 28 dBm	 ACP1 ACP2	 — —	 –50.0 –58.0	 –47.0 –58.0	 dBc dBc
Harmonic Suppression Second Third	 Po ≤ 31 dBm Po ≤ 31 dBm	 AFo2 AFo3	 — —	 –42.0 –45.0	 –33.0 –35.0	 dBc dBc
Noise Power in RX Band 869-894 MHz	Po ≤ 28 dBm	RxBN	—	–134.0	–133.0	dBm/Hz
Noise Figure	—	NF	—	6.0	—	dB
Input Voltage Standing Wave Ratio	—	VSWR	—	1.4:1	1.9:1	—
Stability (Spurious output)	5:1 VSWR All phases	S	—	—	–60.0	dBc
Ruggedness—No damage	Po ≤ 31 dBm	Ru	10:1	—	—	VSWR

NOTE(S):

(1) Vcc = +3.4 V, Vref = +3.0 V, Freq = 836.5 MHz, Tc = 25 °C, unless otherwise specified.

(2) ACP is specified per IS95 as the ratio of the total in-band power (1.23 MHz BW) to adjacent power in a 30 kHz BW.

Table 4. Electrical Specifications Limits for CDMA / AMPS Recommended Operating Conditions[(1)]

Characteristics	Condition	Symbol	Minimum	Maximum	Unit
Quiescent current	Vref = 3.0 V	Iq	—	140.0	mA
Gain–Digital	Po = 0 dBm Po = 28 dBm	G G_p	25.0 24.0	31.5 34.0	dB dB
Gain—Analog	Po = 31dBm	Gp	23.0	33.4	dB
Power Added Efficiency Analog Mode Digital Mode	 Po = 31 dBm Po = 28 dBm	 PAEa PAEd	 40.0 30.0	 — —	 % %
Adjacent Channel Power[(2)] 885 kHz Offset 1980 kHz Offset	 Po ≤ 28 dBm Po ≤ 28 dBm	 ACP1 ACP2	 — —	 –44.0 –56.0	 dBc dBc
Harmonic Suppression Second Third	 Po ≤ 31 dBm Po ≤ 31 dBm	 AFo2 AFo3	 — —	 –30.0 –30.0	 dBc dBc
Noise Power in RX Band 869—894 MHz	Po ≤ 28 dBm	RxBN	—	–131.0	dBm/Hz
Input Voltage Standing Wave Ratio	—	VSWR	—	2:1	—

NOTE(S):
(1) Per Table 2.
(2) ACP is specified per IS95 as the ratio of the total in-band power (1.23 MHz BW) to adjacent power in a 30 kHz BW.

Characterization Data

The following charts illustrate the characteristics of a typical RM912 Power Amplifier tested in the evaluation board described in the following section. The amplifier was selected by characterizing a group of devices and choosing a part with average electrical performance at both nominal and worst case (limit) conditions. Figures 1 through 4 illustrate the digital signal characteristics and Figures 5 through 8 illustrate the analog characteristics of the RM912

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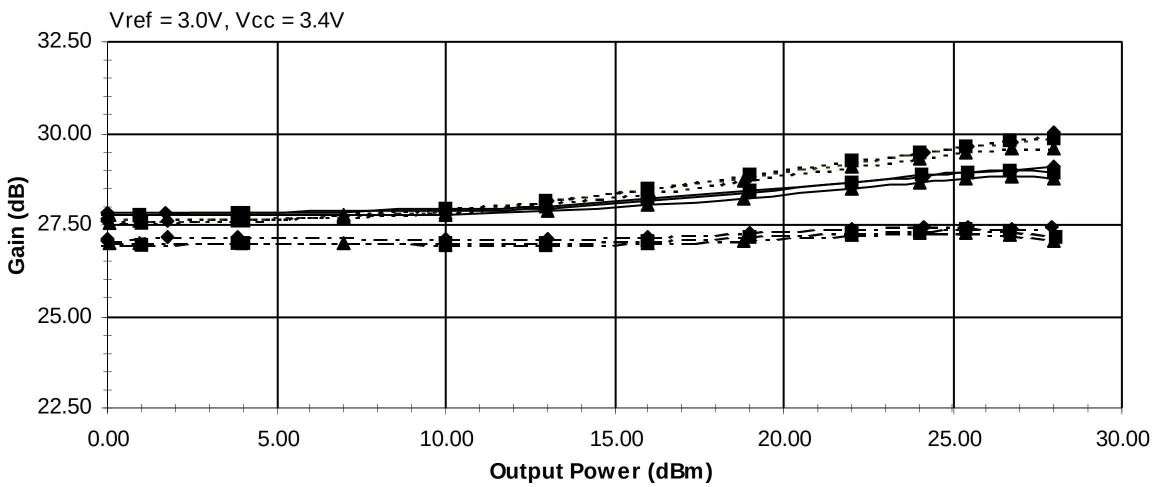
Figure 1. Digital Gain vs. Output Power



Legend

---◆---	824 MHz @ –30 °C	——◆——	824 MHz @ +25 °C	-·-◆-·-	824 MHz @ +85 °C
---■---	837 MHz @ –30 °C	——■——	837 MHz @ +25 °C	-·-■-·-	837 MHz @ +85 °C
---▲---	849 MHz @ –30 °C	——▲——	849 MHz @ +25 °C	-·-▲-·-	849 MHz @ +85 °C

Figure 2. Digital Adjacent Channel Power (ACP1) vs. Output Power

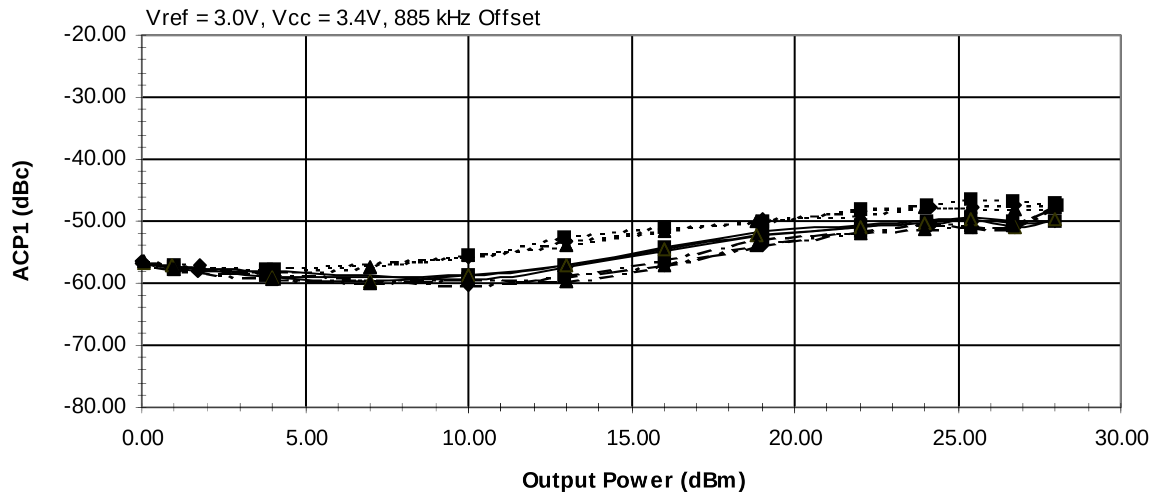
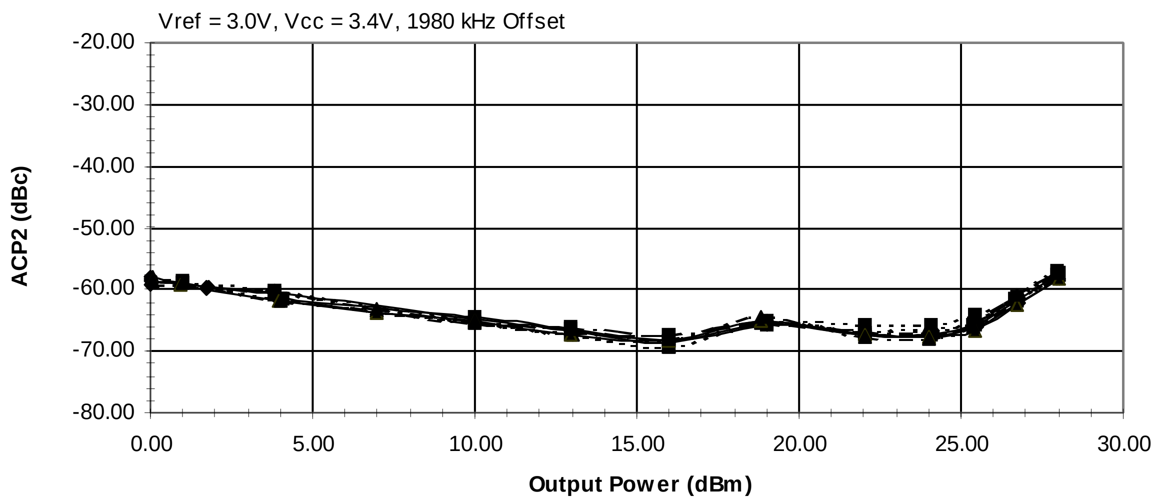


Figure 3. Digital Adjacent Channel Power (ACP2) vs. Output Power



Legend

- - -◆- - -	824 MHz @ –30 °C	——◆——	824 MHz @ +25 °C	- · -◆- · -	824 MHz @ +85 °C
- - -■- - -	837 MHz @ –30 °C	——■——	837 MHz @ +25 °C	- · -■- · -	837 MHz @ +85 °C
- - -▲- - -	849 MHz @ –30 °C	——▲——	849 MHz @ +25 °C	- · -▲- · -	849 MHz @ +85 °C

Figure 4. Digital Power Added Efficiency vs. Output Power

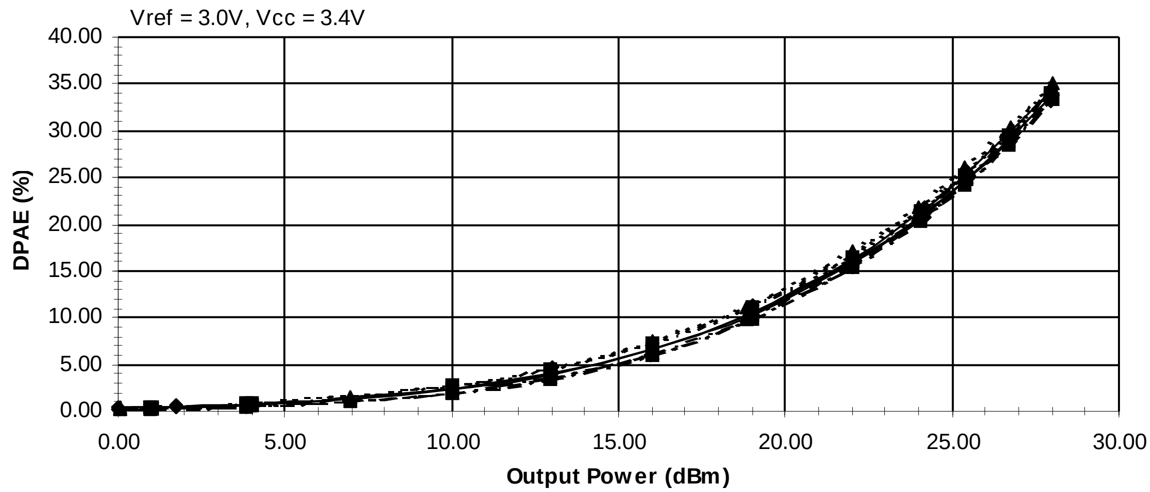
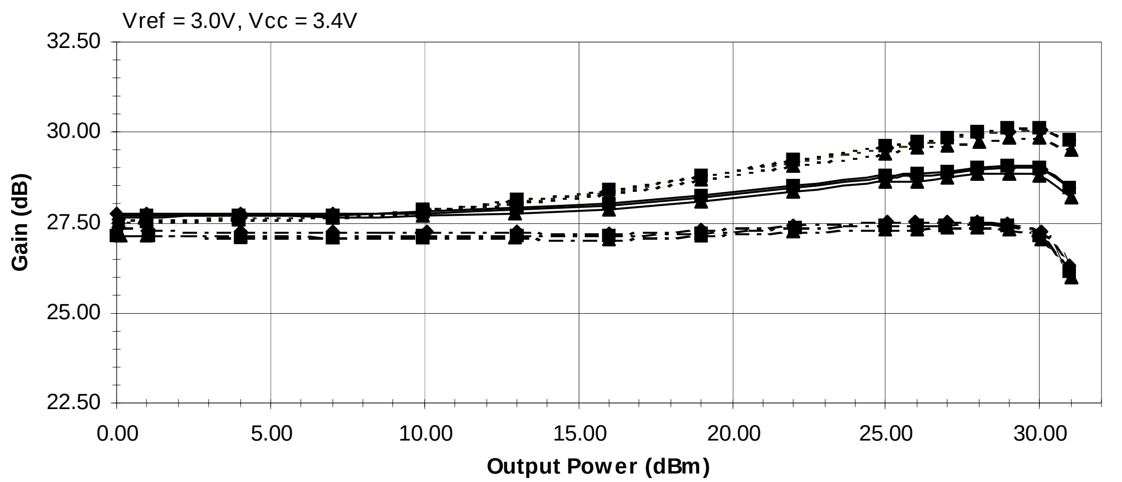


Figure 5. Analog Gain vs. Output Power



Legend

824 MHz @ –30 °C	824 MHz @ +25 °C	824 MHz @ +85 °C
837 MHz @ –30 °C	837 MHz @ +25 °C	837 MHz @ +85 °C
849 MHz @ –30 °C	849 MHz @ +25 °C	849 MHz @ +85 °C

Figure 6. Analog Power Added Efficiency vs. Output Power

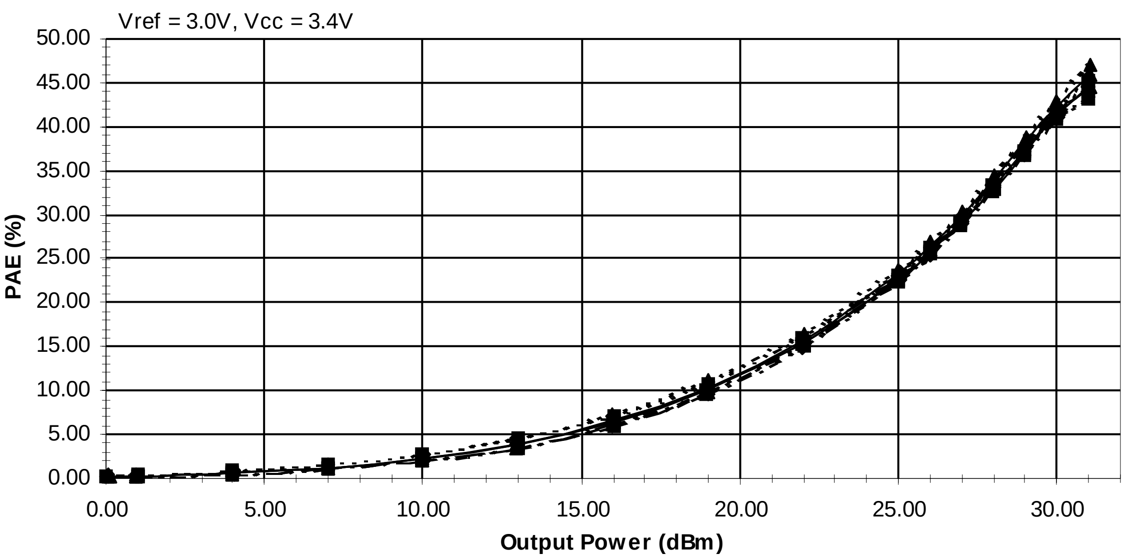
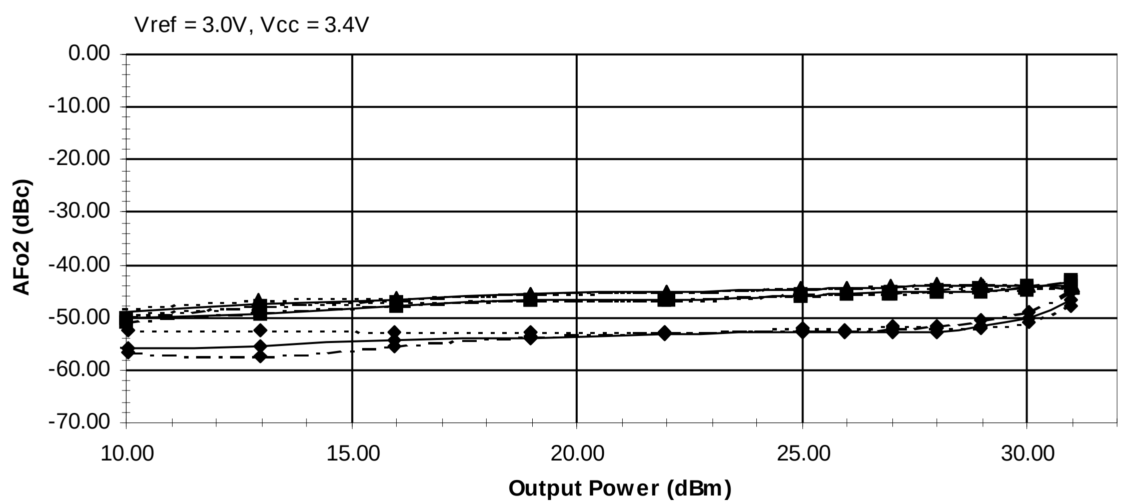


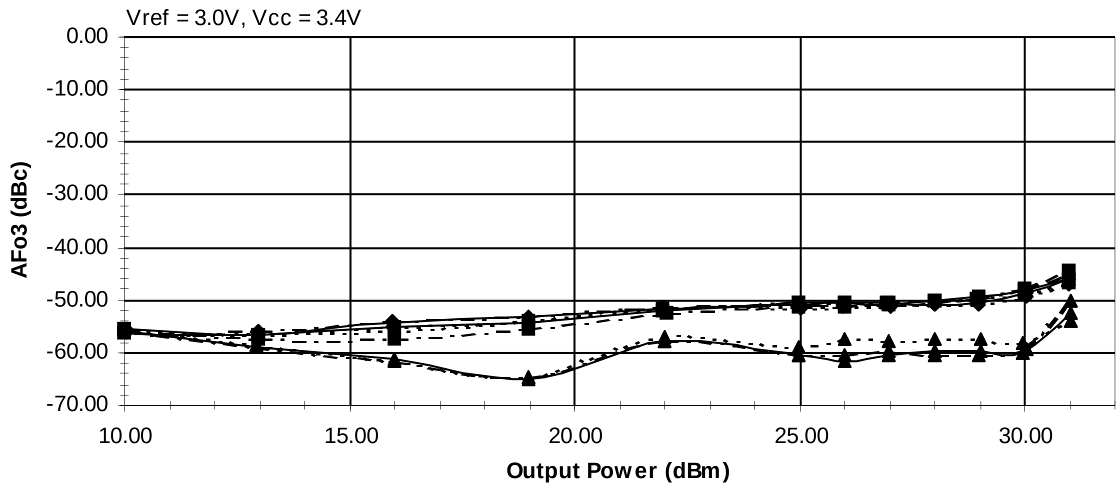
Figure 7. Analog Second Order Harmonic Suppression



Legend

---◆---	824 MHz @ –30 °C	——◆——	824 MHz @ +25 °C	-·-◆-·-	824 MHz @ +85 °C
---■---	837 MHz @ –30 °C	——■——	837 MHz @ +25 °C	-·-■-·-	837 MHz @ +85 °C
---▲---	849 MHz @ –30 °C	——▲——	849 MHz @ +25 °C	-·-▲-·-	849 MHz @ +85 °C

Figure 8. Analog Third Order Harmonic Suppression



Legend

---◆---	824 MHz @ –30 °C	——◆——	824 MHz @ +25 °C	--·◆·--	824 MHz @ +85 °C
---■---	837 MHz @ –30 °C	——■——	837 MHz @ +25 °C	--·■·--	837 MHz @ +85 °C
---▲---	849 MHz @ –30 °C	——▲——	849 MHz @ +25 °C	--·▲·--	849 MHz @ +85 °C

Figure 9. Digital Gain vs. Output Power

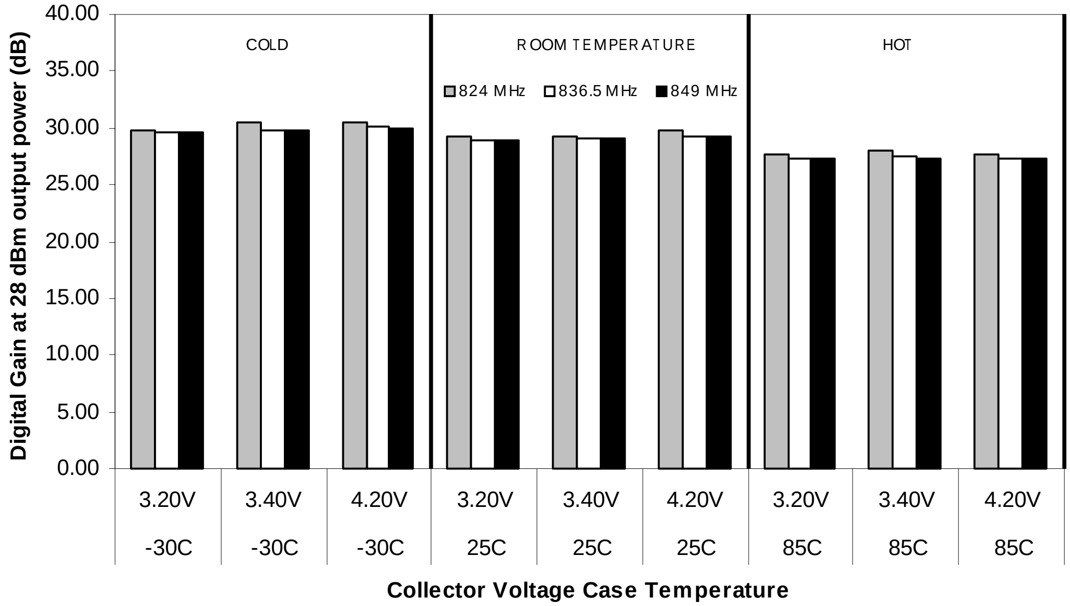


Figure 10. Digital Adjacent Channel Power (ACP1) vs. Output Power

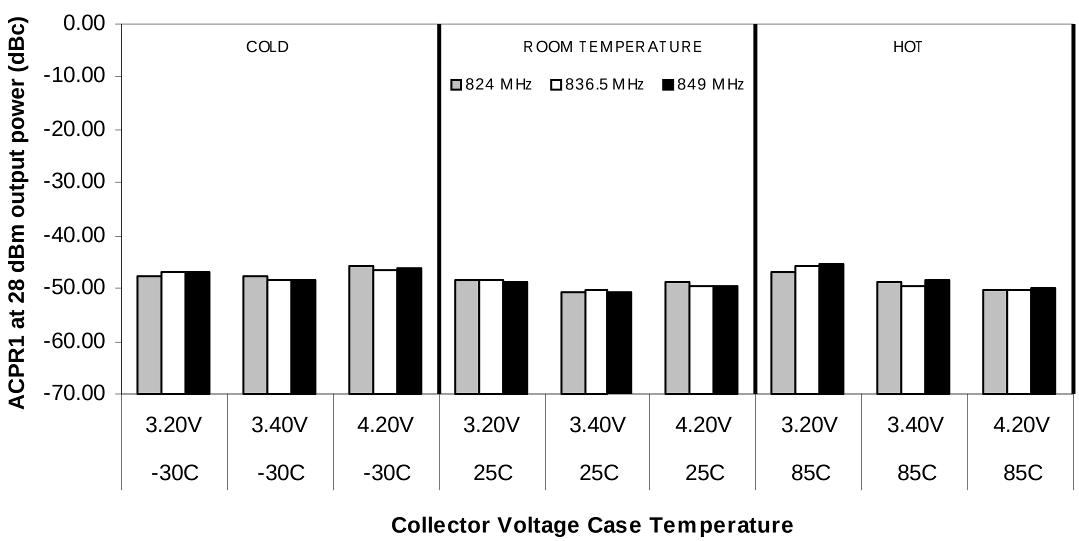


Figure 11. Digital Adjacent Channel Power (ACP2) vs. Output Power

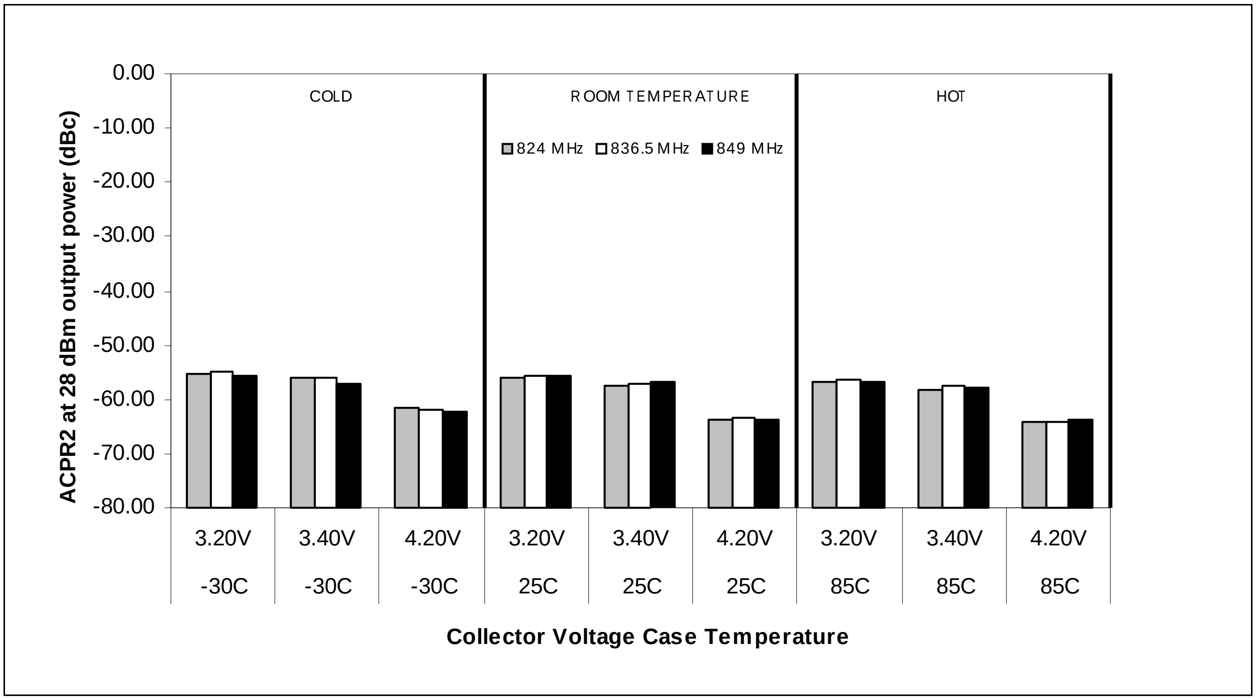


Figure 12. Analog Gain vs. Output Power

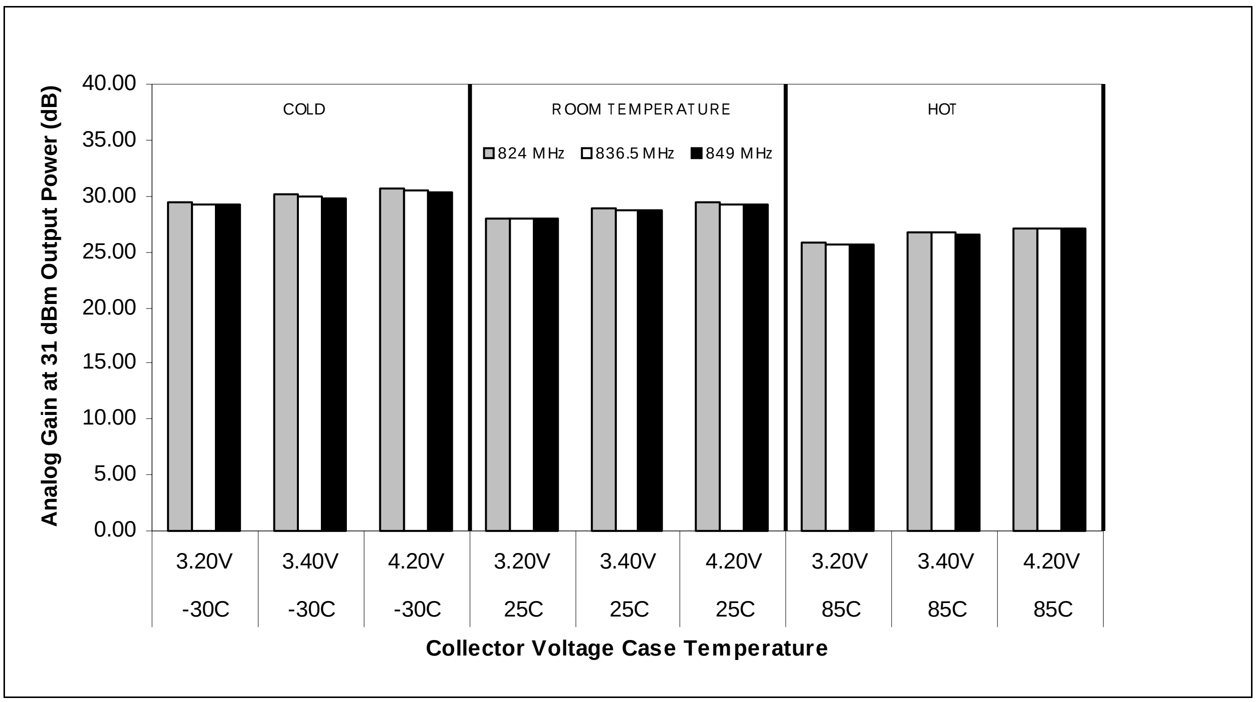


Figure 13. Analog Second Order Harmonic Suppression

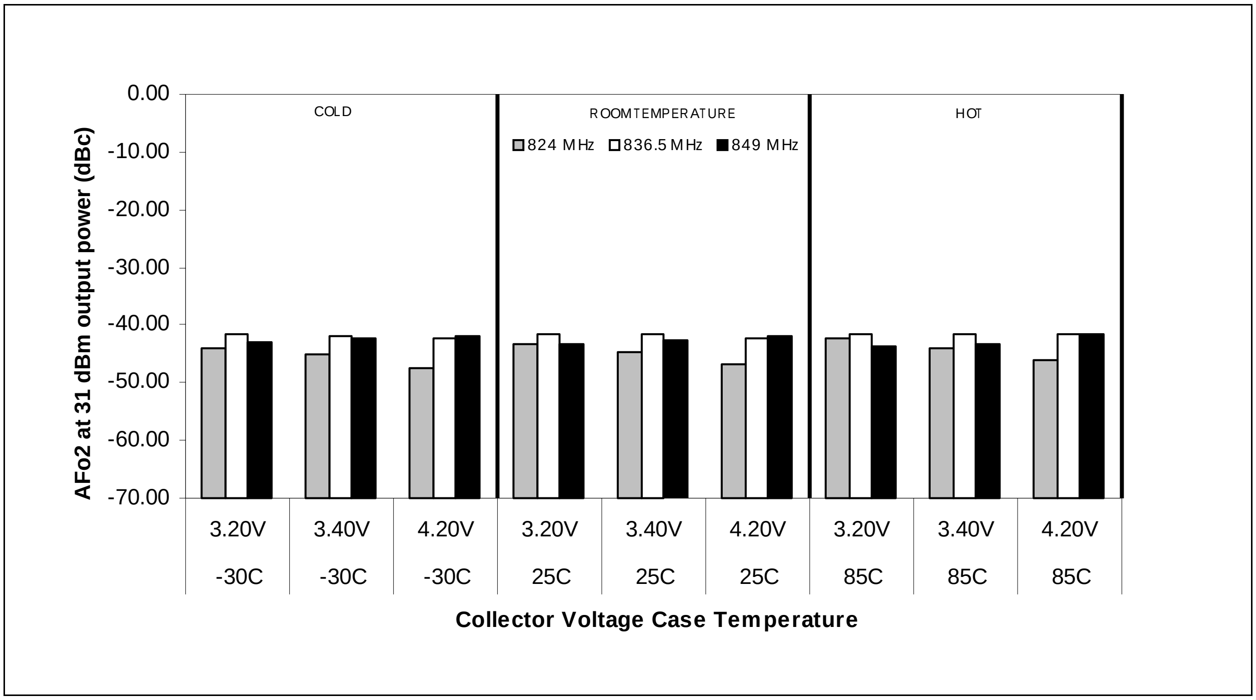


Figure 14. Analog Third Order Harmonic Suppression

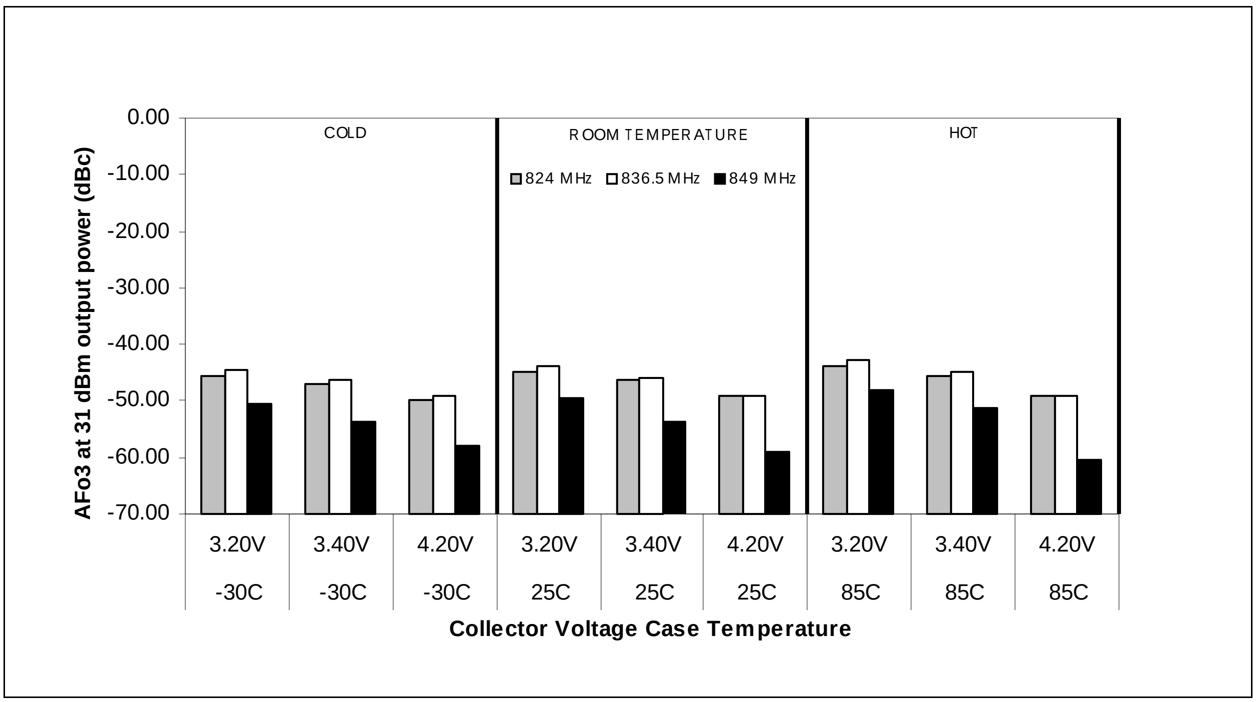


Figure 15. Noise Figure Variation Over Recommended Operating Conditions

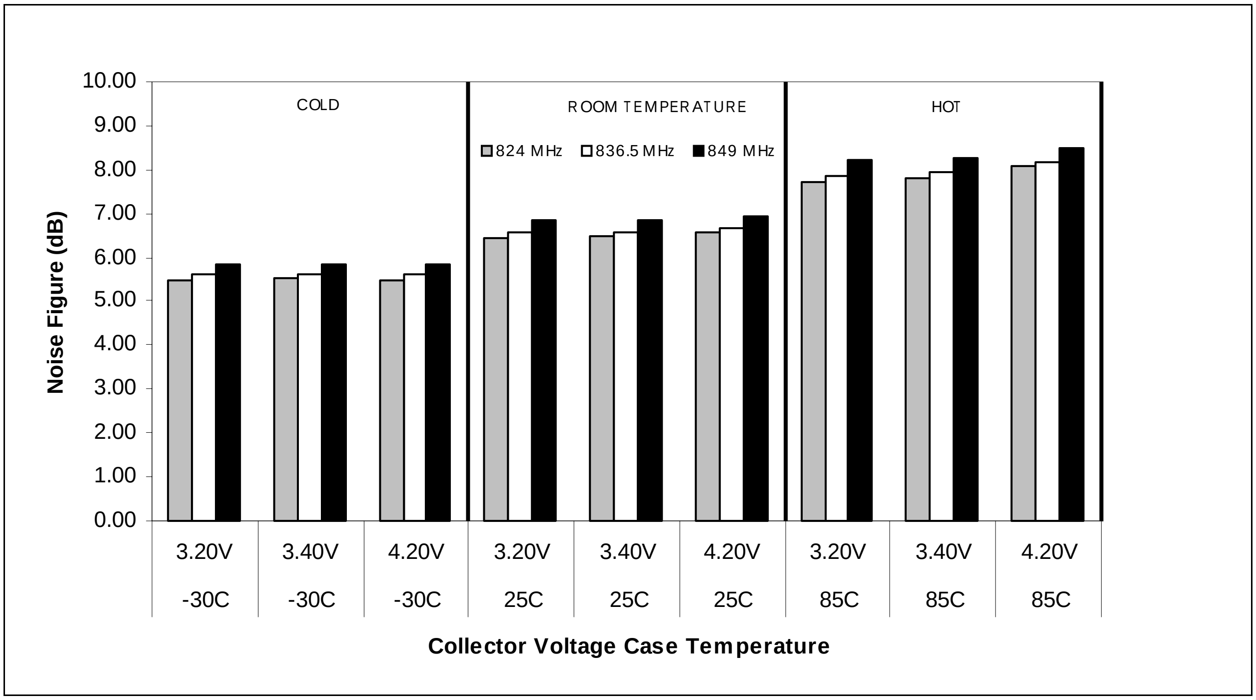
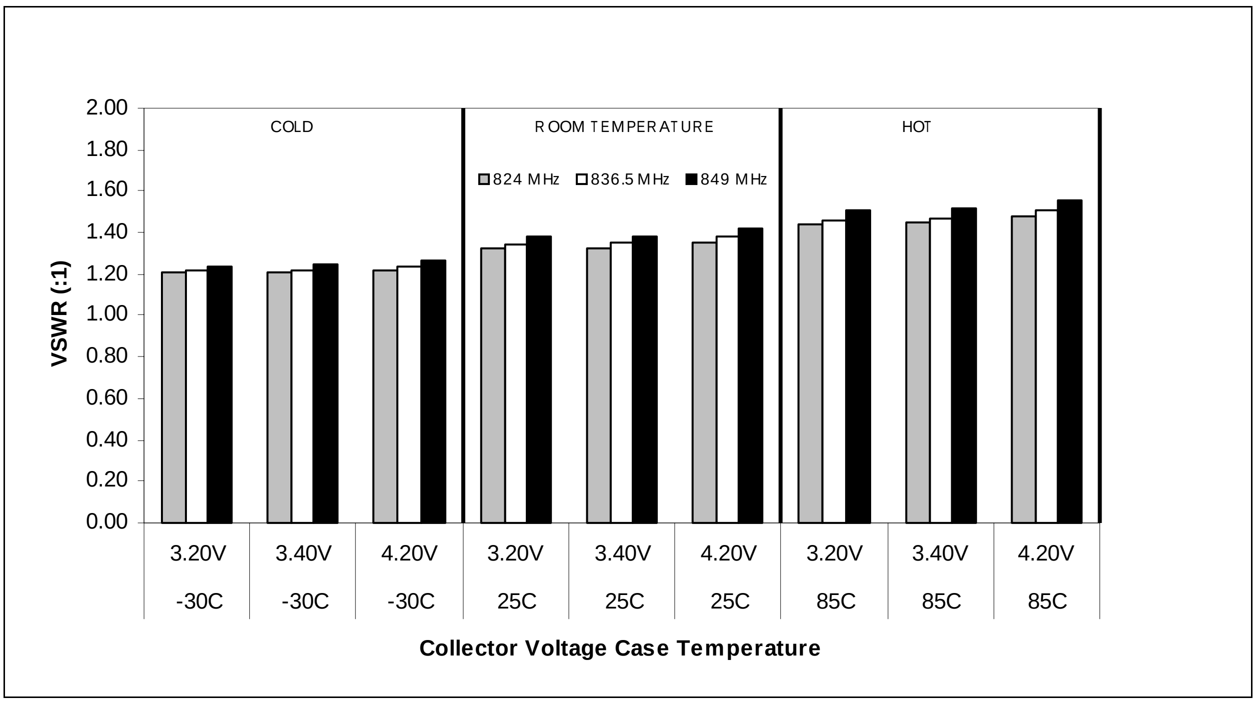


Figure 16. Voltage Standing Wave Ratio Variation Over Recommended Operating Conditions



Evaluation Board Description

The evaluation board is a platform for testing and interfacing design circuitry. To accommodate the interface testing of the RM912, the evaluation board schematic and diagrams are included for preliminary analysis and design. Figure 17 shows the basic schematic of the board for the 824 MHz to 849 MHz range. Figure 18 illustrates the board layout.

Figure 17. Evaluation Board Schematic

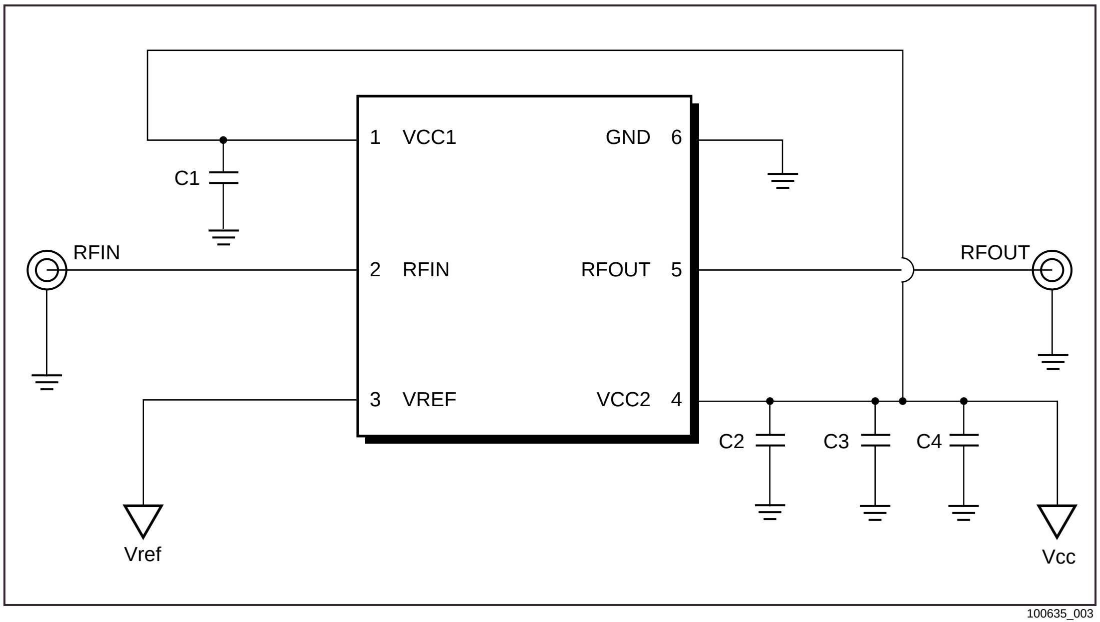
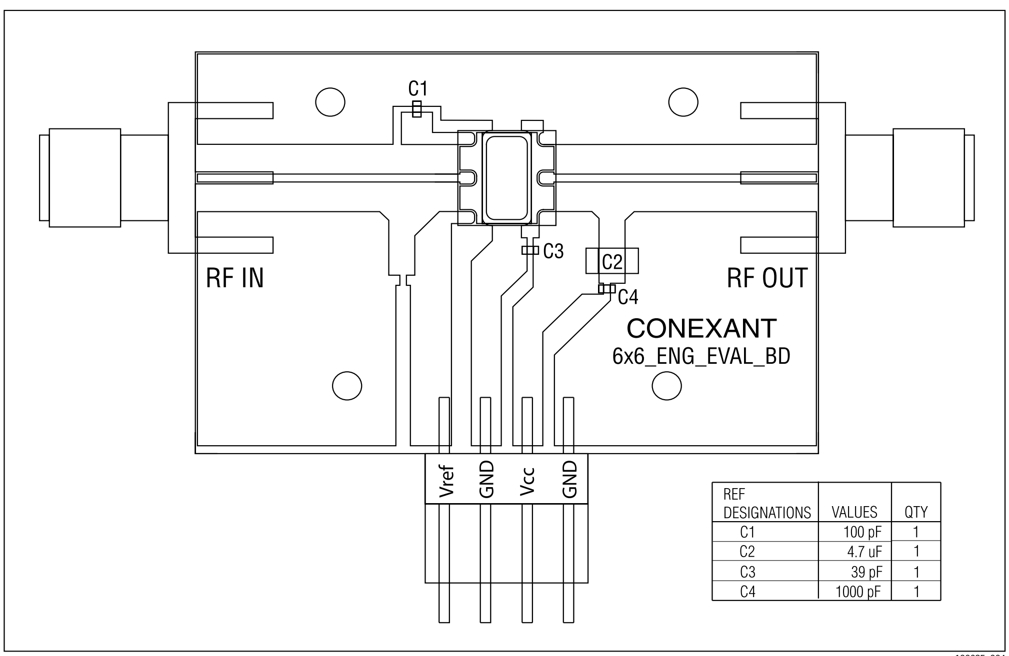


Figure 18. Evaluation Board Assembly Diagram



REF DESIGNATIONS	VALUES	QTY
C1	100 pF	1
C2	4.7 uF	1
C3	39 pF	1
C4	1000 pF	1

Package Dimensions and Pin Descriptions

The RM912 is a multi-layer laminate base, overmold encapsulated modular package designed for surface mount solder attachment to a printed circuit board.

Figure 19. RM912 Package Drawing

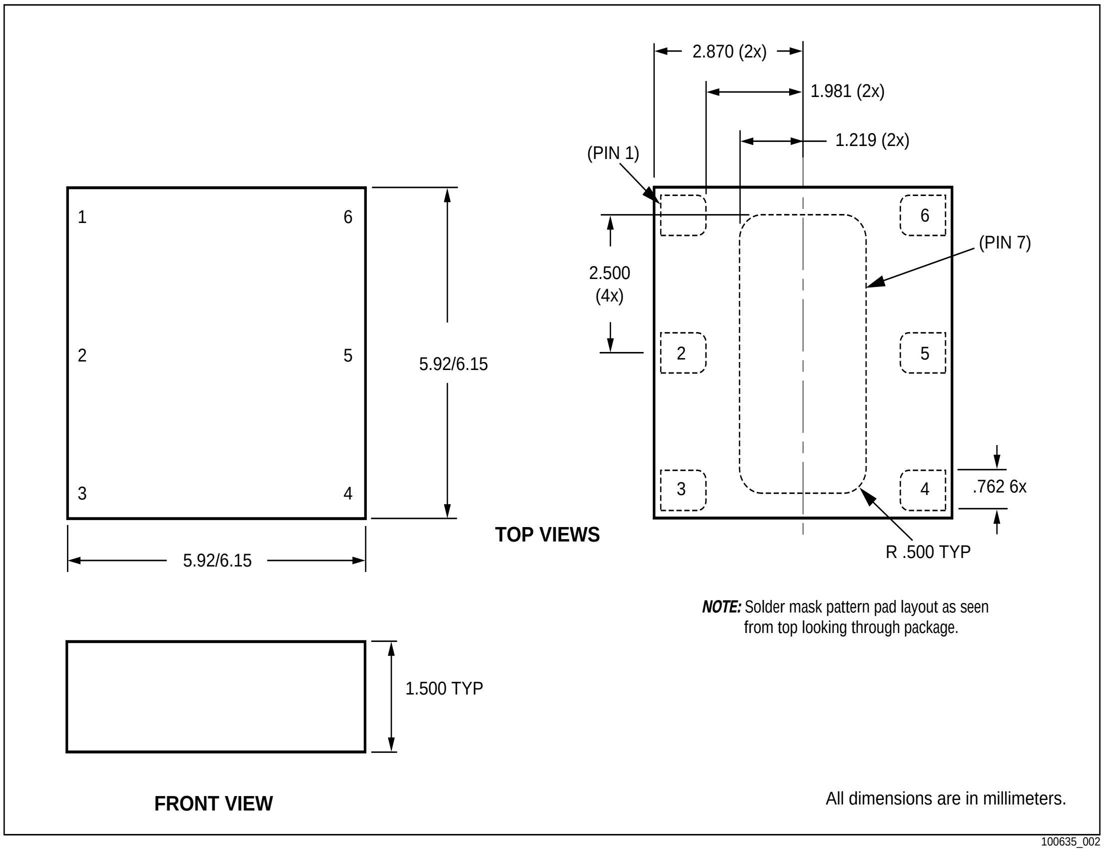


Table 5. Pin Description

Pin #	Function
1	VCC1[(1)]
2	RF Input
3	VREF
4	VCC2[(1)]
5	RF Output
6	GND
GND PAD	GND[(2)]

NOTE(S):
(1) All supply pins may be connected together at the supply.
(2) Package underside is GND.

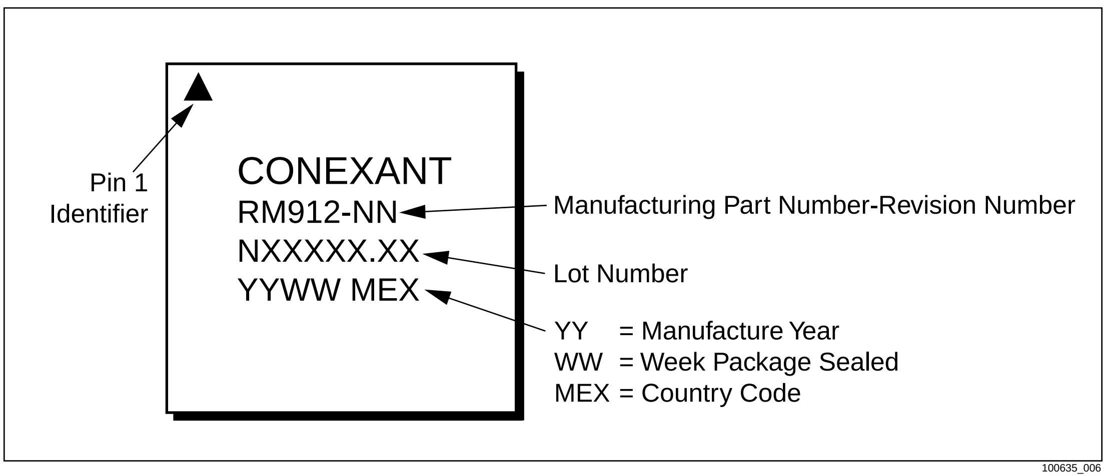
Package and Handling Information

Because this device package is sensitive to moisture absorption, it is baked and vacuum packed prior to shipment. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly. If the part is attached in a reflow oven, the temperature ramp rate should not exceed 5 °C per second. Maximum temperature should not exceed 225 °C and the time spent at a temperature exceeding 210 °C should be limited to less than 10 seconds. If the part is manually attached, precaution should be taken to insure that the part is not subjected to a temperature exceeding 300 °C for more than 10 seconds.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. For additional details on both attachment techniques, precautions, and handling procedures recommended by Conexant, please refer to *Application Note: Solder Reflow, Document Number 101536*.

Production quantities of this product are shipped in the standard tape-and-reel format. For packaging details, refer to *Application Note: Tape and Reel, Document Number 101568.*

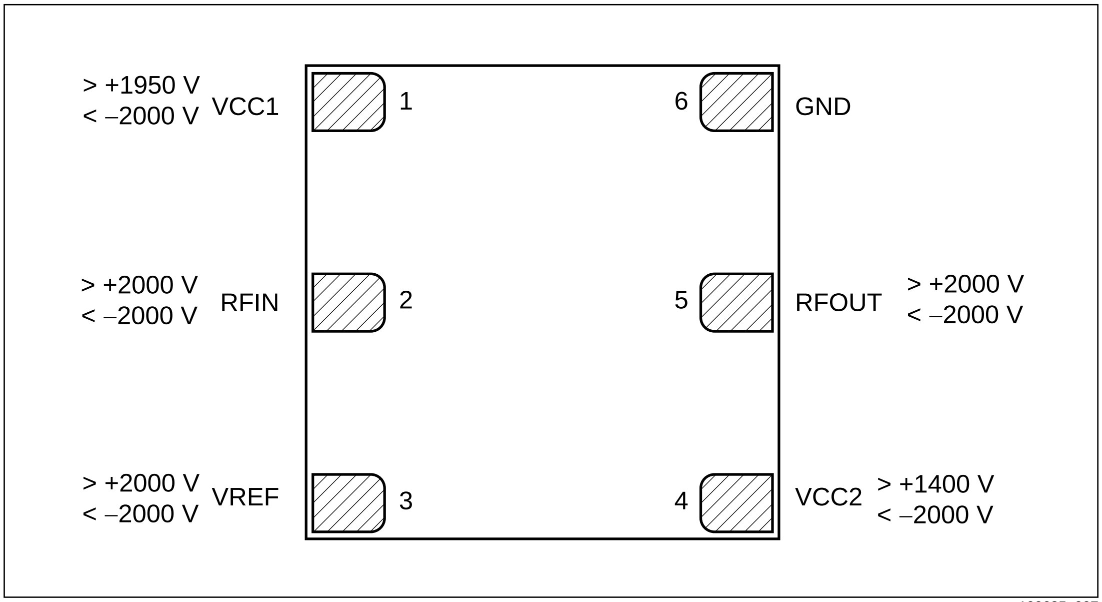
Figure 20. Typical Case Markings



Electrostatic Discharge Sensitivity

The RM912 is a Class I device. Figure 21 lists the Electrostatic Discharge (ESD) immunity level for each pin of the RM912 product. The numbers in Figure 21 specify the ESD threshold level for each pin where the I-V curve between the pin and ground starts to show degradation. The ESD testing was performed in compliance with MIL-STD-883E Method 3015.7 using the Human Body Model. Since 2000 volts represents the maximum measurement limit of the test equipment used, pins marked > 2000 V pass 2000V ESD stress.

Figure 21. ESD Sensitivity Areas



Various failure criteria can be utilized when performing ESD testing. Many vendors employ relaxed ESD failure standards which fail devices only after “the pin fails the electrical specification limits” or “the pin becomes completely non-functional”. Conexant employs most stringent criteria, fails devices as soon as the pin begins to show any degradation on a curve tracer.

To avoid ESD damage, latent or visible, it is very important the Class-1 ESD handling precautions listed in Table 6 be used in the product assembly and test areas follow.

Table 6. Precautions for GaAs ICs with ESD Thresholds Greater Than 200V But Less Than 2000V

Personnel Grounding Wrist Straps Conductive Smocks, Gloves and Finger Cots Antistatic ID Badges	**Facility** Relative Humidity Control and Air Ionizers Dissipative Floors (less than 10^9 Ω to GND)
Protective Workstation Dissipative Table Tops Protective Test Equipment (Properly Grounded) Grounded Tip Soldering Irons Conductive Solder Suckers Static Sensors	**Protective Packaging & Transportation** Bags and Pouches (Faraday Shield) Protective Tote Boxes (Conductive Static Shielding) Protective Trays Grounded Carts Protective Work Order Holders

Ordering Information

Model Number	Manufacturing Part Number	Product Revision	Package	Operating Temperature
RM912	RM912–15	15	6x6LM–6	–30 °C to +85 °C

Revision History

Revision	Level	Date	Description
A		March 2000	Preliminary Information
B		March 2000	Updated Preliminary Information
C		June 2000	Added Characterization Data, Released
D		July 2000	Updated ESD Data
E		July 2000	Preprint Update
F		August 2000	Web Site Update
G		August 2000	Web Format Corrections
H		December 2000	Add: Solder Reflow, Temp. Guidelines; Revise: Figure 21; Revise Ordering Information
I		March 2001	Revise: Table 3, graphs
J		October 2001	Revise: Tables 3, 4; Figures 18, 20, 21

References:

1. Application Note: Solder Reflow, Document Number 101536
2. Application Note: Tape and Reel, Document Number 101568

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