

## Features

- Compatible with MCS-51™ Products
- 8 Kbytes of In-System Reprogrammable Flash Memory  
Endurance: 1,000 Write/Erase Cycles
- Fully Static Operation: 0 Hz to 12 MHz
- Three-Level Program Memory Lock
- 256 x 8-Bit Internal RAM
- 32 Programmable I/O Lines
- Three 16-Bit Timer/Counters
- Eight Interrupt Sources
- Programmable Serial Channel
- Low Power Idle and Power Down Modes
- 2.7 V to 6 V Operating Range

## Description

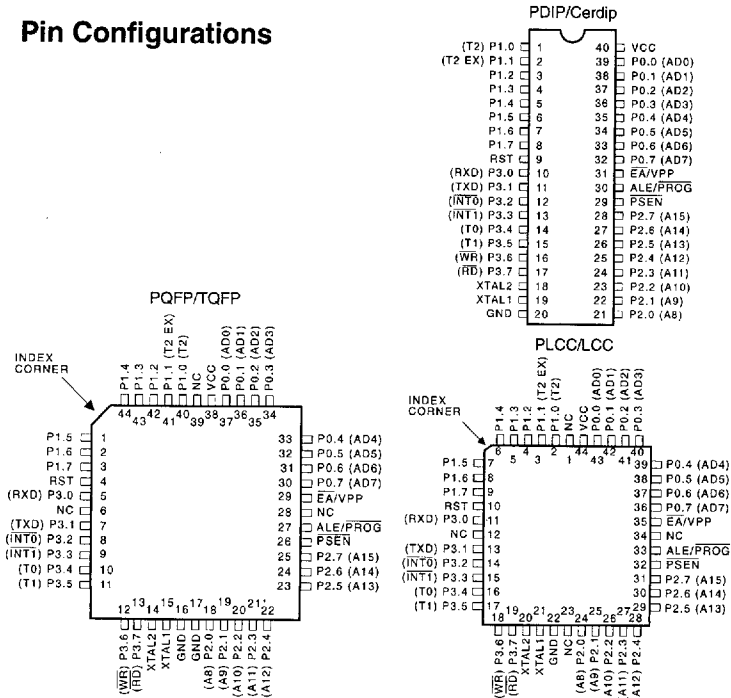
The AT89LV52 is a low-voltage, high-performance CMOS 8-bit microcomputer with 8 Kbytes of Flash programmable and crasable read only memory (PEROM). The device is manufactured using Atmel's high density nonvolatile memory technology and is compatible with the industry standard 80C51 and 80C52 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89LV52 is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications. The AT89LV52 operates at 2.7 volts up to 6.0 volts.

The AT89LV52 provides the following standard features: 8 Kbytes of Flash, 256 bytes of RAM, 32 I/O lines, three 16-bit timer/counters, a six-vector two-level interrupt architecture, a

## 8-Bit Microcontroller with 8 Kbytes Flash

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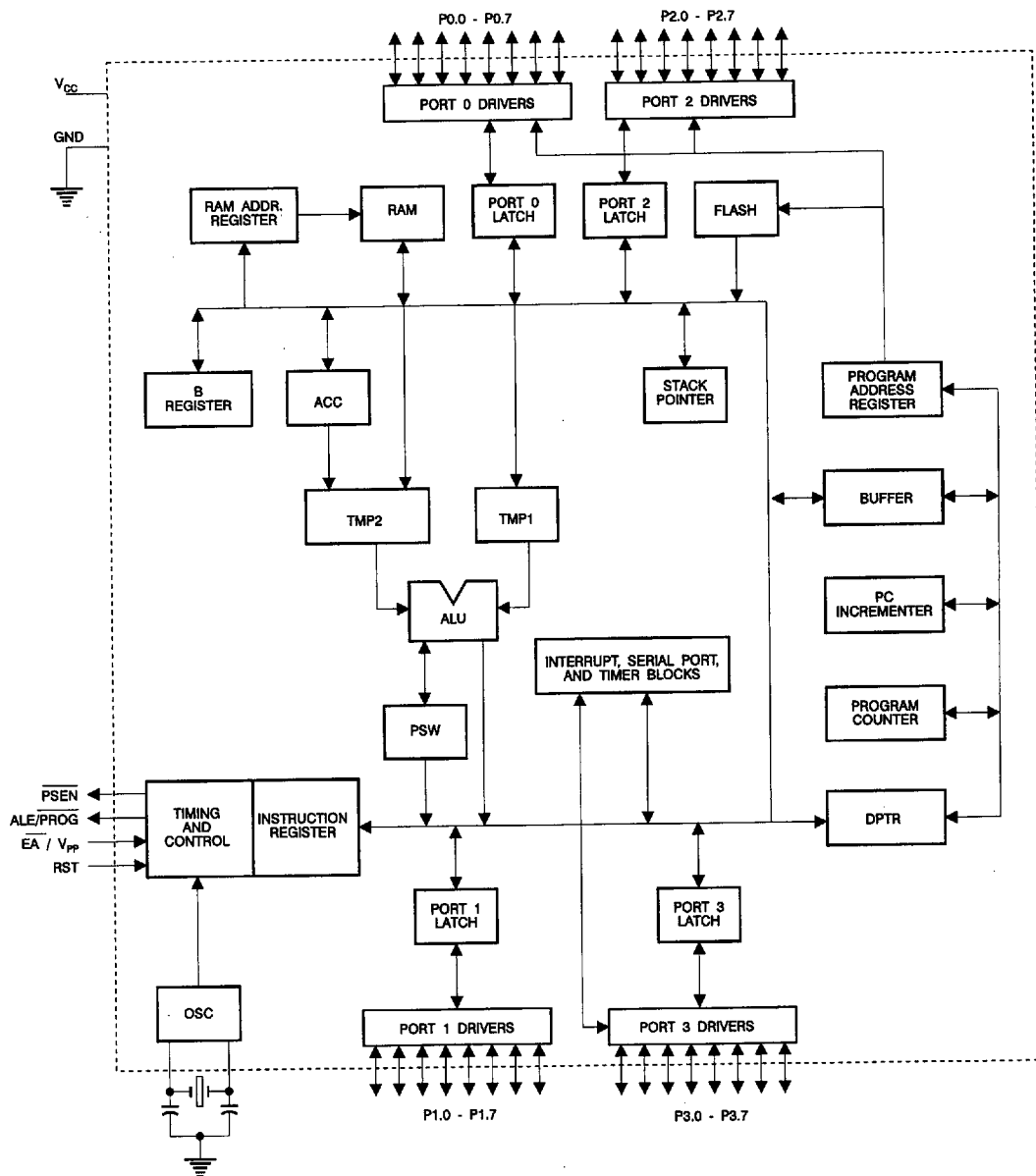
## Pin Configurations



0375B



# Block Diagram



## Description (Continued)

full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89LV52 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power Down Mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next hardware reset.

## Pin Description

Vcc

Supply voltage.

GND

Ground.

Port 0

Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pullups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1

Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current ( $I_{IL}$ ) because of the internal pullups.

In addition, P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively, as shown in the following table.

Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2), clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)

Port 1 also receives the low-order address bytes during Flash programming and program verification.

Port 2

Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current ( $I_{IL}$ ) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data

memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current ( $I_{IL}$ ) because of the pullups.

Port 3 also serves the functions of various special features of the AT89LV51, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	INT0 (external interrupt 0)
P3.3	INT1 (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	WR (external data memory write strobe)
P3.7	RD (external data memory read strobe)

Port 3 also receives some control signals for Flash programming and programming verification.

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/PROG

Address Latch Enable is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

PSEN

Program Store Enable is the read strobe to external program memory.

When the AT89LV52 is executing code from external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory.

(continued)



## Pin Description (Continued)

### $\overline{EA}/V_{PP}$

External Access Enable.  $\overline{EA}$  must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed,  $\overline{EA}$  will be internally latched on reset.

$\overline{EA}$  should be strapped to VCC for internal program executions. This pin also receives the 12-volt programming enable voltage ( $V_{PP}$ ) during Flash programming when 12-volt programming is selected.

### XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

### XTAL2

Output from the inverting oscillator amplifier.

## Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

**Timer 2 Registers** Control and status bits are contained in registers T2CON (shown in Table 2) and T2MOD (shown in Table 4) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16-bit capture mode or 16-bit auto-reload mode.

(continued)

**Table 1.** AT89LV52 SFR Map and Reset Values

0F8H								0FFH
0F0H	B 00000000							0F7H
0E8H								0EFH
0E0H	ACC 00000000							0E7H
0D8H								0DFH
0D0H	PSW 00000000							0D7H
0C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000		0CFH
0C0H								0C7H
0B8H	IP XX000000							0BFH
0B0H	P3 11111111							0B7H
0A8H	IE 0X000000							0AFH
0A0H	P2 11111111							0A7H
98H	SCON 00000000	SBUF XXXXXXXX						9FH
90H	P1 11111111							97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000		8FH
80H	P0 11111111	SP 00000111	DPL 00000000	DPH 00000000			PCON 0XXX0000	87H

**Table 2.** T2CON—Timer/Counter 2 Control Register

T2CON Address = 0C8H

Reset Value = 0000 0000B

Bit Addressable

	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/ $\overline{\text{T2}}$	CP/ $\overline{\text{RL2}}$
Bit	7	6	5	4	3	2	1	0

Symbol	Function
TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
TCLK	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
C/ $\overline{\text{T2}}$	Timer or counter select for Timer 2. C/ $\overline{\text{T2}}$ = 0 for timer function. C/ $\overline{\text{T2}}$ = 1 for external event counter (falling edge triggered).
CP/ $\overline{\text{RL2}}$	Capture/Reload select. CP/ $\overline{\text{RL2}}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/ $\overline{\text{RL2}}$ = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

**3**

## Special Function Registers (Continued)

**Interrupt Registers** The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the six interrupt sources in the IP register.

## Data Memory

The AT89LV52 implements 256 bytes of on-chip RAM. The upper 128 bytes occupy a parallel address space to the Special Function Registers. That means the upper 128 bytes have the same addresses as the SFR space but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions that use direct addressing access SFR space.

For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2).

```
MOV 0A0H, #data
```

Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

```
MOV @R0, #data
```

Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.



## Timer 0 and 1

Timer 0 and Timer 1 in the AT89LV52 operate the same way as Timer 0 and Timer 1 in the AT89LV51.

## Timer 2

Timer 2 is a 16-bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit  $C/\overline{T}2$  in the SFR T2CON (shown in Table 2). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in Table 3.

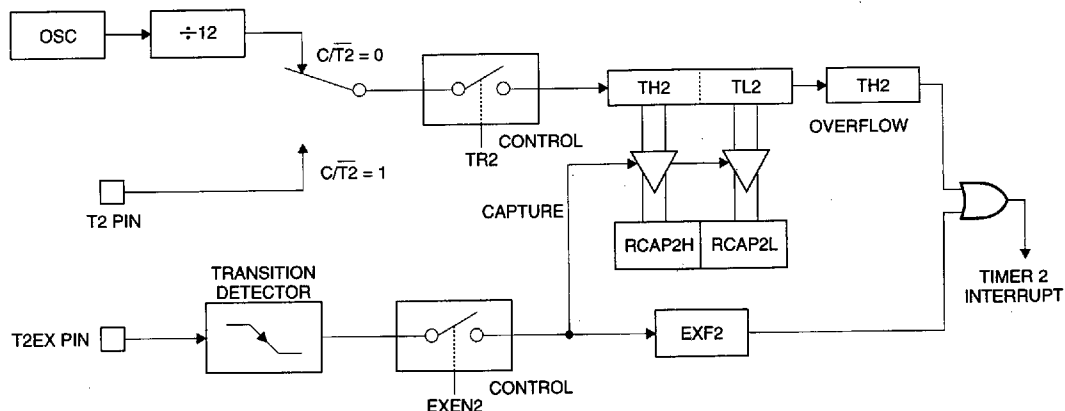
Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since two machine cycles (24 oscillator periods) are required to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, the level should be held for at least one full machine cycle.

**Table 3.** Timer 2 Operating Modes

RCLK + TCLK	CP/RL2	TR2	MODE
0	0	1	16-Bit Auto-Reload
0	1	1	16-Bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

**Figure 1.** Timer 2 in Capture Mode



## Capture Mode

In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 1.

## Auto-Reload (Up or Down Counter)

Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 4). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

Figure 2 shows Timer 2 automatically counting up when DCEN = 0. In this mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to 0xFFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in RCAP2H and RCAP2L. The values in RCAP2H and RCAP2L are preset by software. If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled.

Setting the DCEN bit enables Timer 2 to count up or down, as shown in Figure 3. In this mode, the T2EX pin controls the direction of the count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0xFFFFH and set the TF2 bit. This overflow also causes the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

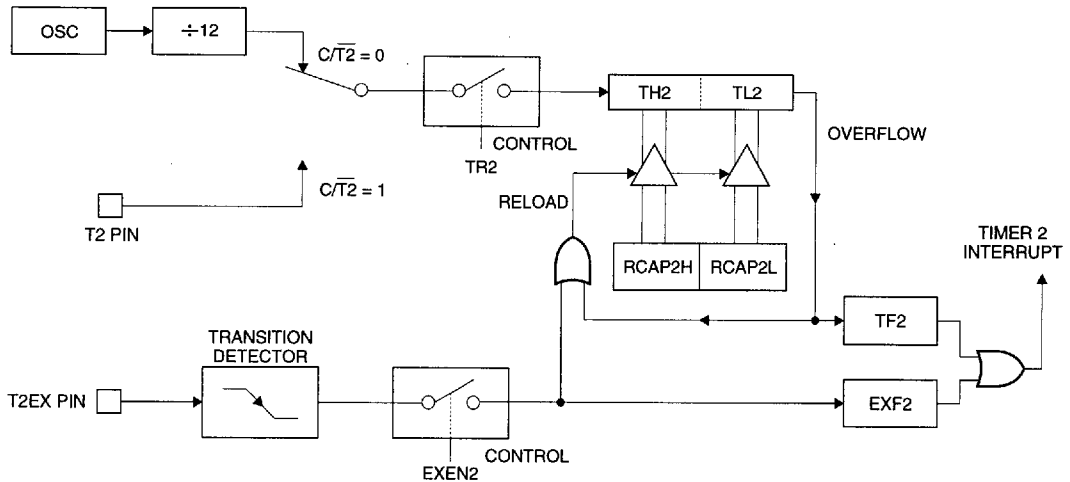
(continued)

### Auto-Reload (Up or Down Counter) (Continued)

A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

**Figure 2.** Timer 2 Auto Reload Mode (DCEN = 0)

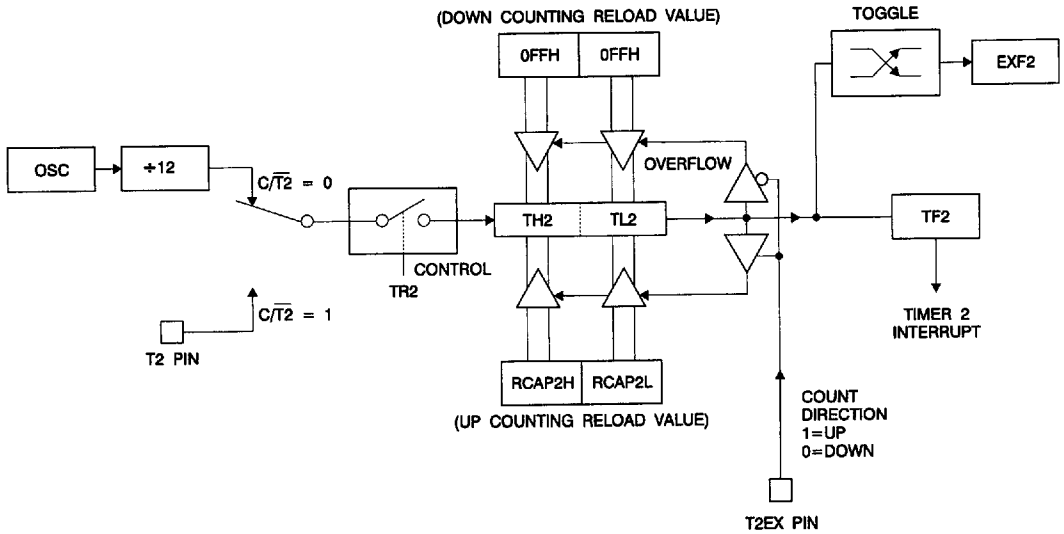


**Table 4.** T2MOD—Timer 2 Mode Control Register

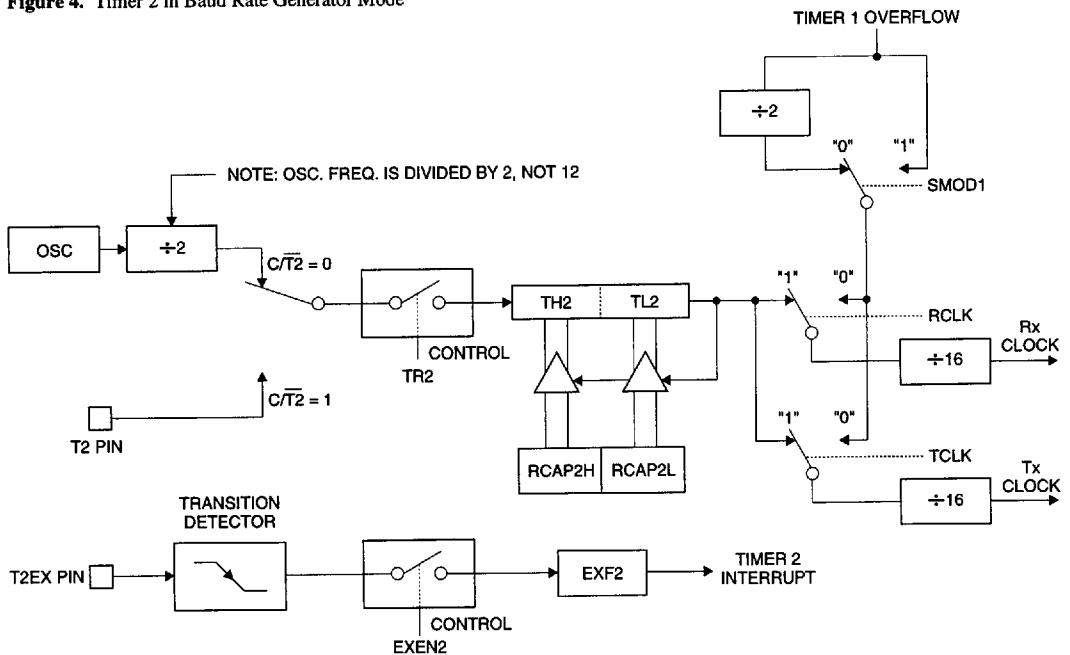
T2MOD Address = 0C9H						Reset Value = XXXX XX00B		
Not Bit Addressable								
	—	—	—	—	—	T2OE	DCEN	
Bit	7	6	5	4	3	2	1	0

Symbol	Function
—	Not implemented, reserved for future use.
T2OE	Timer 2 Output Enable bit.
DCEN	When set, this bit allows Timer 2 to be configured as an up/down counter.

**Figure 3.** Timer 2 Auto Reload Mode (DCEN = 1)



**Figure 4.** Timer 2 in Baud Rate Generator Mode





## Baud Rate Generator

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Table 2). Note that the baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 1 is used for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 4.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation.

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer can be configured for either timer or counter operation. In most applications, it is configured for timer operation ( $CP/T2 = 0$ ). The timer operation is different for Timer 2 when it is used as a baud rate generator. Normally, as a timer, it increments every machine cycle (at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (at

1/2 the oscillator frequency). The baud rate formula is given below.

$$\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - (\text{RCAP2H}, \text{RCAP2L})]}$$

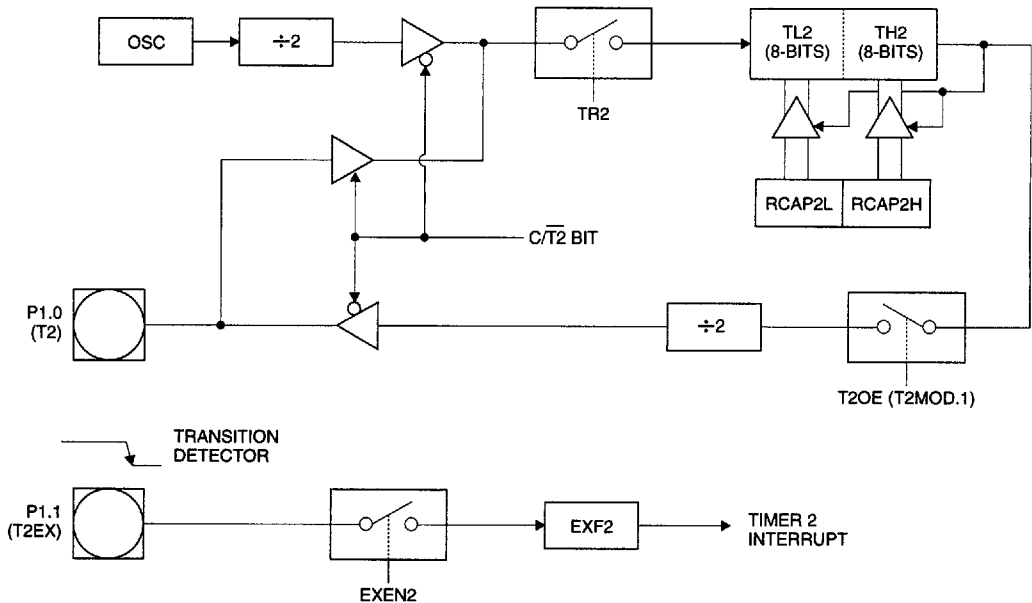
where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 4. This figure is valid only if RCLK or TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2 and will not generate an interrupt. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXP2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

Note that when Timer 2 is running ( $TR2 = 1$ ) as a timer in the baud rate generator mode, TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

3

Figure 5. Timer 2 in Clock-Out Mode



## Programmable Clock Out

A 50% duty cycle clock can be programmed to come out on P1.0, as shown in Figure 5. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed to input the external clock for Timer/Counter 2 or to output a 50% duty cycle clock ranging from 61 Hz to 3 MHz at a 12 MHz operating frequency.

To configure the Timer/Counter 2 as a clock generator, bit  $\overline{C/T2}$  (T2CON.1) must be cleared and bit T2OE (T2MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer.

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L), as shown in the following equation.

$$\text{Clock-Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times [65536 - (\text{RCAP2H}, \text{RCAP2L})]}$$

In the clock-out mode, Timer 2 roll-overs will not generate an interrupt. This behavior is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies cannot be determined independently from one another since they both use RCAP2H and RCAP2L.

## UART

The UART in the AT89LV52 operates the same way as the UART in the AT89LV51.

## Interrupts

The AT89LV52 has a total of six interrupt vectors: two external interrupts (INT0 and INT1), three timer interrupts (Timers 0, 1, and 2), and the serial port interrupt. These interrupts are all shown in Figure 6.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 5 shows that bit position IE.6 is unimplemented. In the AT89LV51, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S2P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the same cycle in which the timer overflows.

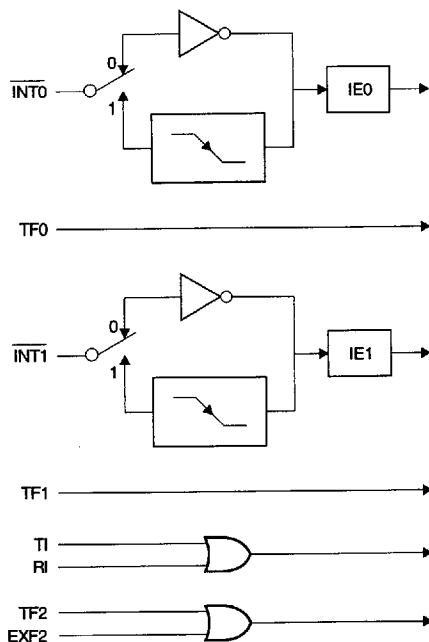
**Table 5.** Interrupt Enable (IE) Register

(MSB)				(LSB)			
EA	—	ET2	ES	ET1	EX1	ET0	EX0
Enable Bit = 1 enables the interrupt.							
Enable Bit = 0 disables the interrupt.							

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
—	IE.6	Reserved.
ET2	IE.5	Timer 2 interrupt enable bit.
ES	IE.4	Serial Port interrupt enable bit.
ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.

User software should never write 1s to unimplemented bits, because they may be used in future AT89 products.



**Figure 6.** Interrupt Sources

## Oscillator Characteristics

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 7. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 8. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

## Idle Mode

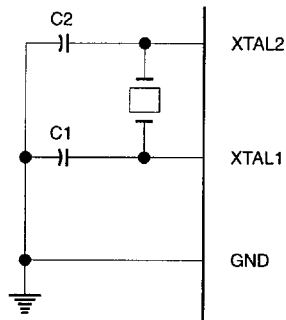
In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

## Power Down Mode

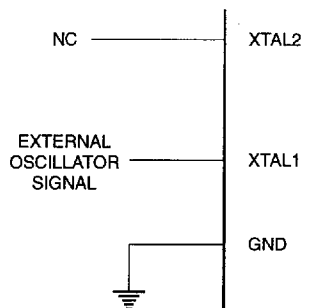
In the power down mode, the oscillator is stopped, and the instruction that invokes power down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power down mode is terminated. The only exit from power down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before  $V_{CC}$  is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

### Figure 7. Oscillator Connections



Notes: C1, C2 = 30 pF  $\pm$  10 pF for Crystals  
= 40 pF  $\pm$  10 pF for Ceramic Resonators

**Figure 8. External Clock Drive Configuration**



## Status of External Pins During Idle and Power Down

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

## Program Memory Lock Bits

The AT89LV52 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

When lock bit 1 is programmed, the logic level at the  $\overline{EA}$  pin is sampled and latched during reset. If the device is powered up

without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of  $\overline{EA}$  must agree with the current logic level at that pin in order for the device to function properly.

## Lock Bit Protection Modes

Program Lock Bits				Protection Type
	LB1	LB2	LB3	
1	U	U	U	No program lock features.
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash memory is disabled.
3	P	P	U	Same as mode 2, but verify is also disabled.
4	P	P	P	Same as mode 3, but external execution is also disabled.

## Programming the Flash

The AT89LV52 is normally shipped with the on-chip Flash memory array in the erased state (that is, contents = FFH) and ready to be programmed. The programming interface accepts either a high-voltage (12-volt) or a low-voltage ( $V_{CC}$ ) program enable signal. The low voltage programming mode provides a convenient way to program the AT89LV52 inside the user's system, while the high-voltage programming mode is compatible with conventional third party Flash or EPROM programmers.

The AT89LV52 is shipped with either the high-voltage or low-voltage programming mode enabled. The respective top-side marking and device signature codes are listed in the following table.

	$V_{PP} = 12\text{ V}$	$V_{PP} = 5\text{ V}$
Top-Side Mark	AT89LV52 xxxx yyww	AT89LV52 xxxx-5 yyww
Signature	(030H)=1EH (031H)=62H (032H)=FFH	(030H)=1EH (031H)=62H (032H)=05H

The AT89LV52 code memory array is programmed byte-by-byte in either programming mode. *To program any non-blank byte in the on-chip Flash Memory, the entire memory must be erased using the Chip Erase Mode.*

**Programming Algorithm:** Before programming the AT89LV52, the address, data and control signals should be set up according to the Flash programming mode table and Figures 9 and 10. To program the AT89LV52, take the following steps.

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.

3. Activate the correct combination of control signals.
4. Raise  $\overline{EA}/V_{PP}$  to 12 V for the high-voltage programming mode.
5. Pulse  $\overline{ALE}/\overline{PROG}$  once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 1.5 ms. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

**Data Polling:** The AT89LV52 features Data Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on PO.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. Data Polling may begin any time after a write cycle has been initiated.

**Ready/Busy:** The progress of byte programming can also be monitored by the RDY/ $\overline{BSY}$  output signal. P3.4 is pulled low after  $\overline{ALE}$  goes high during programming to indicate  $\overline{BSY}$ . P3.4 is pulled high again when programming is done to indicate READY.

**Program Verify:** If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

**Chip Erase:** The entire Flash array is erased electrically by using the proper combination of control signals and by holding  $\overline{ALE}/\overline{PROG}$  low for 10 ms. The code array is written with all 1s. The chip erase operation must be executed before the code memory can be reprogrammed.

**Reading the Signature Bytes:** The signature bytes are read by the same procedure as a normal verification of locations 030H,

(continued)

## Programming the Flash (Continued)

031H, and 032H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.






- (030H) = 1EH indicates manufactured by Atmel
- (031H) = 52H indicates 89LV52
- (032H) = FFH indicates 12 V programming
- (032H) = 05H indicates 5 V programming

## Programming Interface

Every code byte in the Flash array can be written, and the entire array can be erased, by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

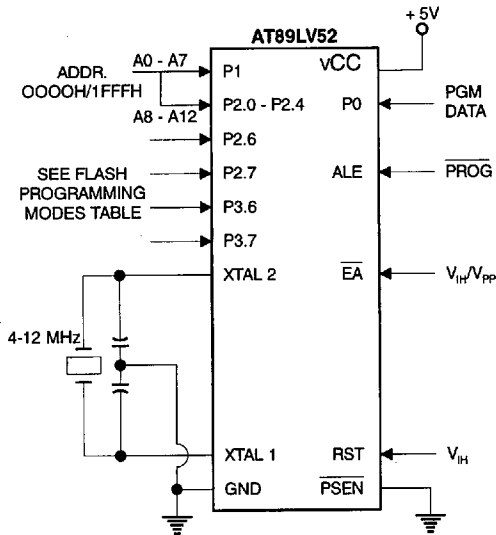
## Flash Programming Modes

Mode		RST	$\overline{\text{PSEN}}$	ALE/ PROG	EA/ V <sub>PP</sub>	P2.6	P2.7	P3.6	P3.7
Write Code Data		H	L		H/12V <sup>(1)</sup>	L	H	H	H
Read Code Data		H	L	H	H	L	L	H	H
Write Lock	Bit - 1	H	L		H/12V	H	H	H	H
	Bit - 2	H	L	 <sup>(2)</sup>	H/12V	H	H	L	L
	Bit - 3	H	L		H/12V	H	L	H	L
Chip Erase		H	L		H/12V	H	L	L	L
Read Signature Byte		H	L	H	H	L	L	L	L

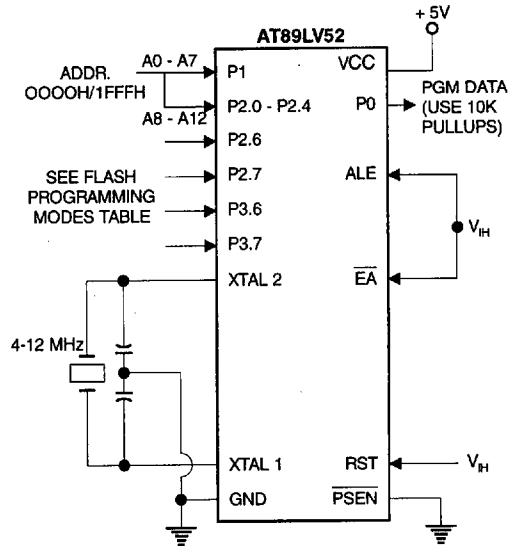
Notes: 1. The signature byte at location 032H designates whether V<sub>PP</sub> = 12 V or V<sub>PP</sub> = 5 V should be used to enable programming.

2. Chip Erase requires a 10 ms  $\overline{\text{PROG}}$  pulse.

**Figure 9. Programming the Flash Memory**



**Figure 10. Verifying the Flash Memory**



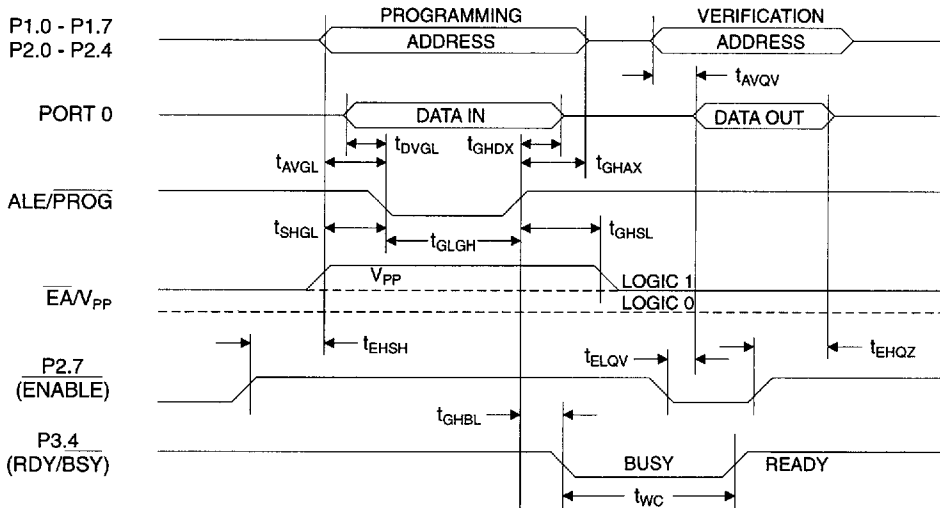
## Flash Programming and Verification Characteristics

$T_A = 21^\circ\text{C}$  to  $27^\circ\text{C}$ ,  $V_{CC} = 5.0 \pm 10\%$

Symbol	Parameter	Min	Max	Units
$V_{PP}^{(1)}$	Programming Enable Voltage	11.5	12.5	V
$I_{PP}^{(1)}$	Programming Enable Current		25	$\mu\text{A}$
$1/t_{CLCL}$	Oscillator Frequency	4	12	MHz
$t_{AVGL}$	Address Setup to $\overline{\text{PROG}}$ Low	$48t_{CLCL}$		
$t_{GHAX}$	Address Hold After $\overline{\text{PROG}}$	$48t_{CLCL}$		
$t_{DVGL}$	Data Setup to $\overline{\text{PROG}}$ Low	$48t_{CLCL}$		
$t_{GHDX}$	Data Hold After $\overline{\text{PROG}}$	$48t_{CLCL}$		
$t_{EHS}$	P2.7 ( $\overline{\text{ENABLE}}$ ) High to $V_{PP}$	$48t_{CLCL}$		
$t_{SHGL}$	$V_{PP}$ Setup to $\overline{\text{PROG}}$ Low	10		$\mu\text{s}$
$t_{GHSL}^{(1)}$	$V_{PP}$ Hold After $\overline{\text{PROG}}$	10		$\mu\text{s}$
$t_{GLGH}$	$\overline{\text{PROG}}$ Width	1	110	$\mu\text{s}$
$t_{AVQV}$	Address to Data Valid		$48t_{CLCL}$	
$t_{ELQV}$	$\overline{\text{ENABLE}}$ Low to Data Valid		$48t_{CLCL}$	
$t_{EHQV}$	Data Float After $\overline{\text{ENABLE}}$	0	$48t_{CLCL}$	
$t_{GHBL}$	$\overline{\text{PROG}}$ High to $\overline{\text{BUSY}}$ Low		1.0	$\mu\text{s}$
$t_{WC}$	Byte Write Cycle Time		2.0	ms

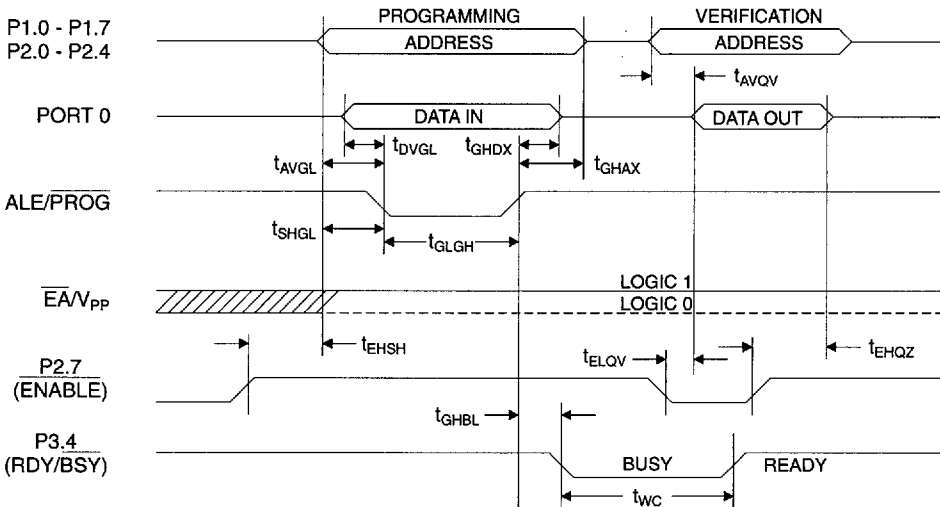
Note: 1. Only used in 12-volt programming mode.

### Flash Programming and Verification Waveforms - High Voltage Mode



3

### Flash Programming and Verification Waveforms - Low Voltage Mode





## Absolute Maximum Ratings\*

Operating Temperature.....	-55°C to +125°C
Storage Temperature.....	-65°C to +150°C
Voltage on Any Pin with Respect to Ground .....	-1.0 V to +7.0 V
Maximum Operating Voltage .....	6.6 V
DC Output Current .....	15.0 mA

\*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## D.C. Characteristics

The values shown in this table are valid for  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 5.0\text{ V} \pm 20\%$ , unless otherwise noted.

Symbol	Parameter	Condition	Min	Max	Units
$V_{IL}$	Input Low Voltage	(Except EA)	-0.5	$0.2 V_{CC} - 0.1$	V
$V_{IL1}$	Input Low Voltage (EA)		-0.5	$0.2 V_{CC} - 0.3$	V
$V_{IH}$	Input High Voltage	(Except XTAL1, RST)	$0.2 V_{CC} + 0.9$	$V_{CC} + 0.5$	V
$V_{IH1}$	Input High Voltage	(XTAL1, RST)	$0.7 V_{CC}$	$V_{CC} + 0.5$	V
$V_{OL}$	Output Low Voltage <sup>(1)</sup> (Ports 1,2,3)	$I_{OL} = 1.6\text{ mA}$		0.45	V
$V_{OL1}$	Output Low Voltage <sup>(1)</sup> (Port 0, ALE, PSEN)	$I_{OL} = 3.2\text{ mA}$		0.45	V
$V_{OH}$	Output High Voltage (Ports 1,2,3, ALE, PSEN)	$I_{OH} = -60\text{ }\mu\text{A}$ , $V_{CC} = 5\text{ V} \pm 10\%$	2.4		V
		$I_{OH} = -25\text{ }\mu\text{A}$	$0.75 V_{CC}$		V
		$I_{OH} = -10\text{ }\mu\text{A}$	$0.9 V_{CC}$		V
$V_{OH1}$	Output High Voltage (Port 0 in External Bus Mode)	$I_{OH} = -800\text{ }\mu\text{A}$ , $V_{CC} = 5\text{ V} \pm 10\%$	2.4		V
		$I_{OH} = -300\text{ }\mu\text{A}$	$0.75 V_{CC}$		V
		$I_{OH} = -80\text{ }\mu\text{A}$	$0.9 V_{CC}$		V
$I_{IL}$	Logical 0 Input Current (Ports 1,2,3)	$V_{IN} = 0.45\text{ V}$		-50	$\mu\text{A}$
$I_{TL}$	Logical 1 to 0 Transition Current (Ports 1,2,3)	$V_{IN} = 2\text{ V}$		-650	$\mu\text{A}$
$I_{LI}$	Input Leakage Current (Port 0, EA)	$0.45 < V_{IN} < V_{CC}$		$\pm 10$	$\mu\text{A}$
RRST	Reset Pulldown Resistor		50	300	$\text{K}\Omega$
$C_{IO}$	Pin Capacitance	Test Freq. = 1 MHz, $T_A = 25^\circ\text{C}$		10	pF
$I_{CC}$	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power Down Mode <sup>(2)</sup>	$V_{CC} = 6\text{ V}$		100	$\mu\text{A}$
		$V_{CC} = 3\text{ V}$		40	$\mu\text{A}$

Notes: 1. Under steady state (non-transient) conditions,  $I_{OL}$  must be externally limited as follows:  
Maximum  $I_{OL}$  per port pin: 10 mA  
Maximum  $I_{OL}$  per 8-bit port:  
Port 0: 26 mA  
Ports 1, 2, 3: 15 mA  
Maximum total  $I_{OL}$  for all output pins: 71 mA

If  $I_{OL}$  exceeds the test condition,  $V_{OL}$  may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.  
2. Minimum  $V_{CC}$  for Power Down is 2 V.



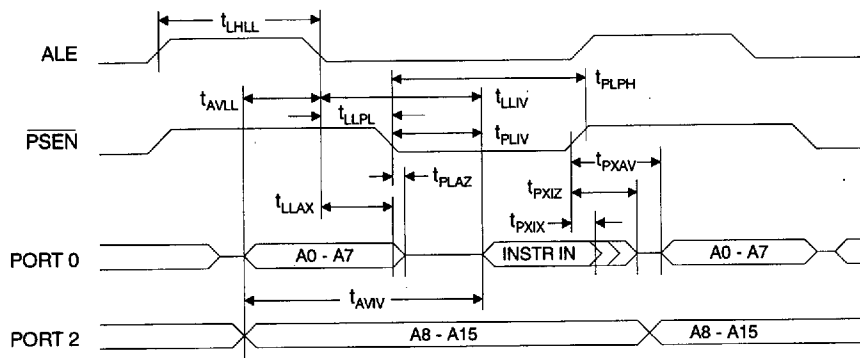
## A.C. Characteristics

Under operating conditions, load capacitance for Port 0, ALE/ $\overline{\text{PROG}}$ , and  $\overline{\text{PSEN}}$  = 100 pF; load capacitance for all other outputs = 80 pF.

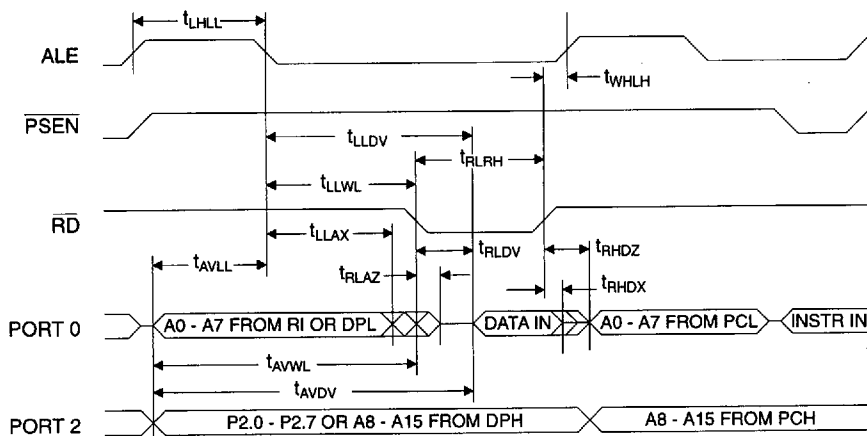
### External Program and Data Memory Characteristics

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
1/t <sub>CLCL</sub>	Oscillator Frequency			0	12	MHz
t <sub>LHLL</sub>	ALE Pulse Width	127		2t <sub>CLCL</sub> -40		ns
t <sub>AVLL</sub>	Address Valid to ALE Low	28		t <sub>CLCL</sub> -25		ns
t <sub>LLAX</sub>	Address Hold After ALE Low	48		t <sub>CLCL</sub> -25		ns
t <sub>LLIV</sub>	ALE Low to Valid Instruction In		233		4t <sub>CLCL</sub> -65	ns
t <sub>LLPL</sub>	ALE Low to $\overline{\text{PSEN}}$ Low	43		t <sub>CLCL</sub> -25		ns
t <sub>PLPH</sub>	$\overline{\text{PSEN}}$ Pulse Width	205		3t <sub>CLCL</sub> -45		ns
t <sub>PLIV</sub>	$\overline{\text{PSEN}}$ Low to Valid Instruction In		145		3t <sub>CLCL</sub> -60	ns
t <sub>PIXI</sub>	Input Instruction Hold After $\overline{\text{PSEN}}$	0		0		ns
t <sub>PIXZ</sub>	Input Instruction Float After $\overline{\text{PSEN}}$		59		t <sub>CLCL</sub> -25	ns
t <sub>PXAV</sub>	$\overline{\text{PSEN}}$ to Address Valid	75		t <sub>CLCL</sub> -8		ns
t <sub>AVIV</sub>	Address to Valid Instruction In		312		5t <sub>CLCL</sub> -80	ns
t <sub>PLAZ</sub>	$\overline{\text{PSEN}}$ Low to Address Float		10		10	ns
t <sub>RLRH</sub>	$\overline{\text{RD}}$ Pulse Width	400		6t <sub>CLCL</sub> -100		ns
t <sub>WLWH</sub>	$\overline{\text{WR}}$ Pulse Width	400		6t <sub>CLCL</sub> -100		ns
t <sub>RLDV</sub>	$\overline{\text{RD}}$ Low to Valid Data In		252		5t <sub>CLCL</sub> -90	ns
t <sub>RHDX</sub>	Data Hold After $\overline{\text{RD}}$	0		0		ns
t <sub>RHDZ</sub>	Data Float After $\overline{\text{RD}}$		97		2t <sub>CLCL</sub> -28	ns
t <sub>LLDV</sub>	ALE Low to Valid Data In		517		8t <sub>CLCL</sub> -150	ns
t <sub>AVDV</sub>	Address to Valid Data In		585		9t <sub>CLCL</sub> -165	ns
t <sub>LLWL</sub>	ALE Low to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Low	200	300	3t <sub>CLCL</sub> -50	3t <sub>CLCL</sub> +50	ns
t <sub>AVWL</sub>	Address to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Low	203		4t <sub>CLCL</sub> -75		ns
t <sub>QVWX</sub>	Data Valid to $\overline{\text{WR}}$ Transition	23		t <sub>CLCL</sub> -30		ns
t <sub>QVWH</sub>	Data Valid to $\overline{\text{WR}}$ High	433		7t <sub>CLCL</sub> -120		ns
t <sub>WHQX</sub>	Data Hold After $\overline{\text{WR}}$	33		t <sub>CLCL</sub> -25		ns
t <sub>RLAZ</sub>	$\overline{\text{RD}}$ Low to Address Float		0		0	ns
t <sub>WHLH</sub>	$\overline{\text{RD}}$ or $\overline{\text{WR}}$ High to ALE High	43	123	t <sub>CLCL</sub> -25	t <sub>CLCL</sub> +25	ns

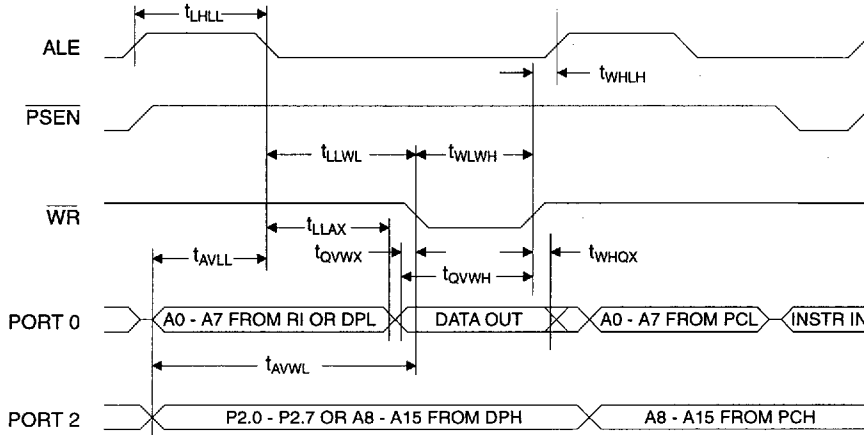
## External Program Memory Read Cycle



## External Data Memory Read Cycle

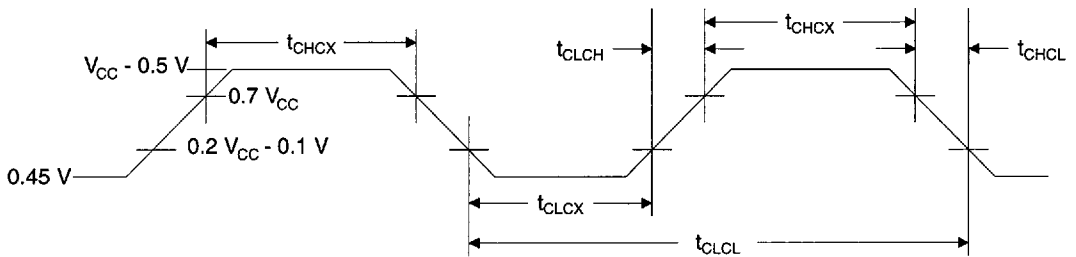


## External Data Memory Cycle



3

## External Clock Drive Waveforms



## External Clock Drive

Symbol	Parameter	Min	Max	Units
1/t <sub>CLCL</sub>	Oscillator Frequency	0	12	MHz
t <sub>CLCL</sub>	Clock Period	83.3		ns
t <sub>CHCX</sub>	High Time	20		ns
t <sub>CLCX</sub>	Low Time	20		ns
t <sub>CLCH</sub>	Rise Time		20	ns
t <sub>CHCL</sub>	Fall Time		20	ns

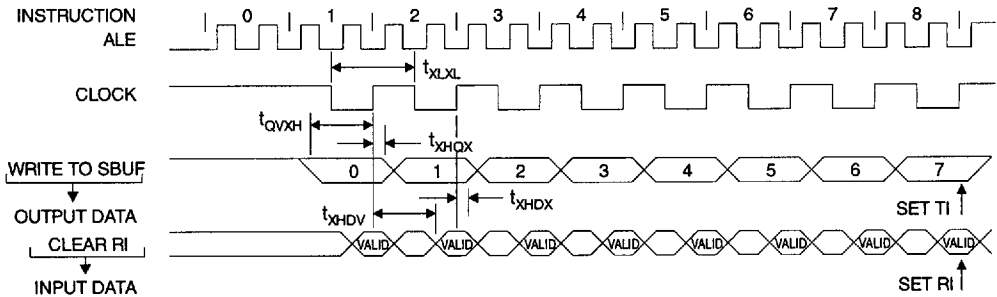


## Serial Port Timing: Shift Register Mode Test Conditions

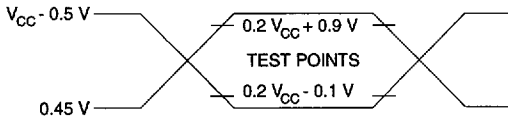
The values in this table are valid for  $V_{CC} = 5.0 \text{ V} \pm 20\%$  and Load Capacitance = 80 pF.

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
$t_{XLXL}$	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		$\mu\text{s}$
$t_{QVXH}$	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}-133$		ns
$t_{XHGX}$	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}-33$		ns
$t_{XHDX}$	Input Data Hold After Clock Rising Edge	0		0		ns
$t_{XHDV}$	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}-133$	ns

## Shift Register Mode Timing Waveforms

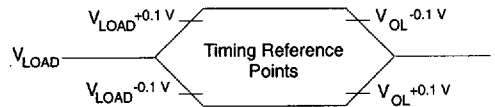


## AC Testing Input/Output Waveforms <sup>(1)</sup>



Note: 1. AC Inputs during testing are driven at  $V_{CC} - 0.5 \text{ V}$  for a logic 1 and  $0.45 \text{ V}$  for a logic 0. Timing measurements are made at  $V_{IH} \text{ min.}$  for a logic 1 and  $V_{IL} \text{ max.}$  for a logic 0.

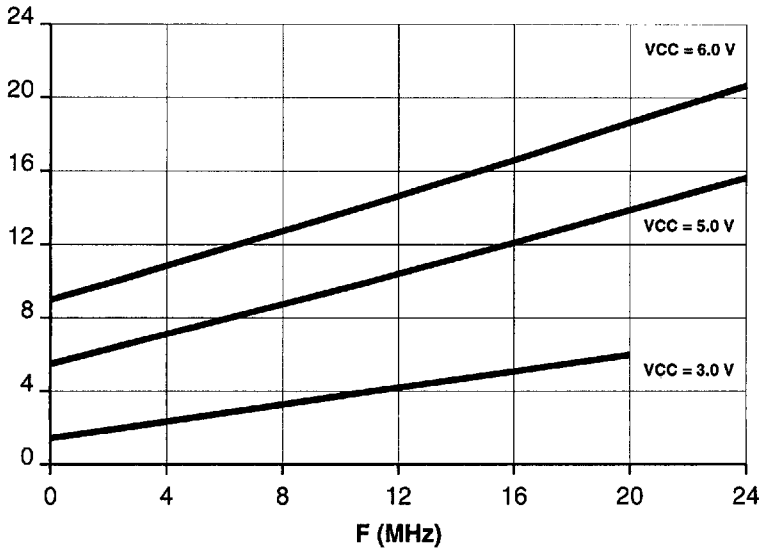
## Float Waveforms <sup>(1)</sup>



Note: 1. For timing purposes, a port pin is no longer floating when a 100-mV change from load voltage occurs. A port pin begins to float when a 100-mV change from the loaded  $V_{OH}/V_{OL}$  level occurs.

# AT89LV52

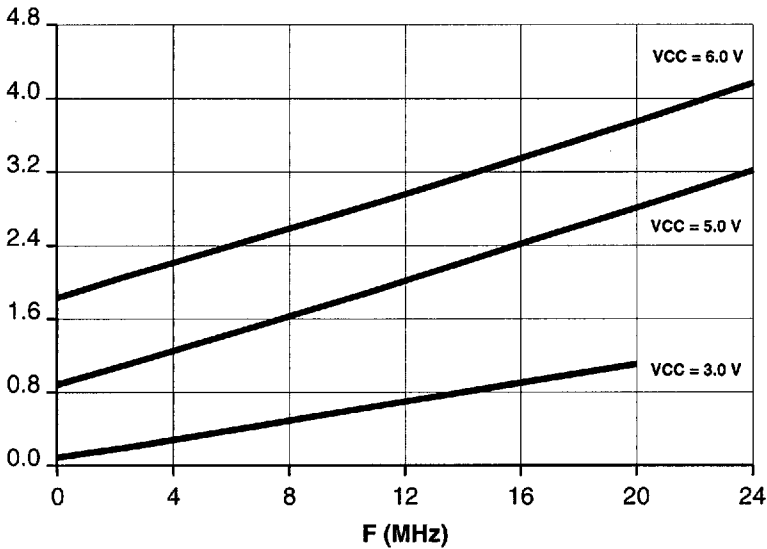
ICC (mA) TYPICAL ICC (ACTIVE) at 25°C



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# AT89LV52

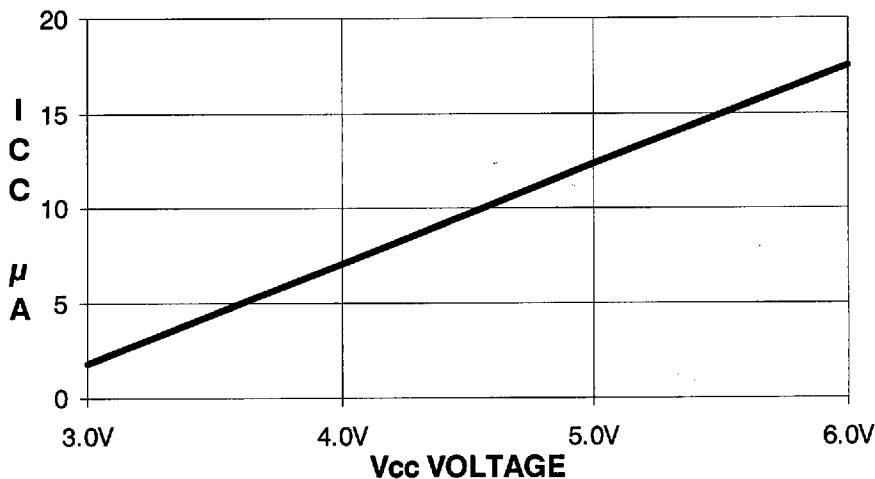
ICC (mA) TYPICAL ICC (IDLE) at 25°C





## AT89LV52

TYPICAL ICC vs. VOLTAGE - POWER DOWN (85°C)



### Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
12	2.7 V to 6 V	AT89LV52-12AC AT89LV52-12JC AT89LV52-12PC AT89LV52-12QC	44A 44J 40P6 44Q	Commercial (0°C to 70°C)

Package Type	
44A	44 Lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
40D6	40 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
44J	44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
44L	44 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
40P6	40 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
44Q	44 Lead, Plastic Gull Wing Quad Flatpack (PQFP)

Each Atmel data sheet includes an Ordering Information Section which specifies the package types available. This section provides size specifications and outlines for all package types.<sup>(1)</sup>

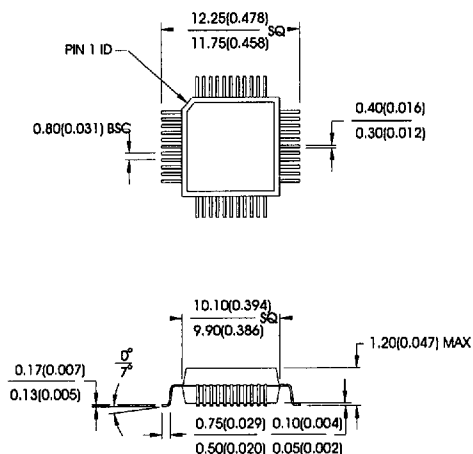
Package	Description	See Page
44A	44 Lead, Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (TQFP) .....	7-4
40D6	40 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip).....	7-4
44J	44 Lead, Plastic J-Leaded Chip Carrier (PLCC) .....	7-4
44L	44 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC) .....	7-4
40P6	40 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP).....	7-5
20P3	20 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP).....	7-5
44Q	44 Lead, Plastic Gull Wing Quad Flat Package (PQFP) .....	7-5
20S	20 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC).....	7-5

Package Drawings

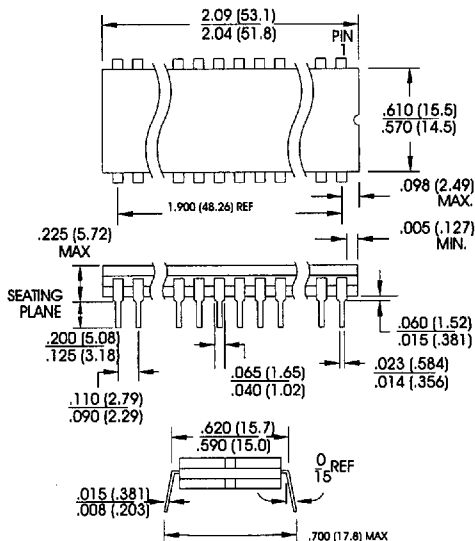
Note: 1. Dimensions shown do not include lead plating or mold flash.



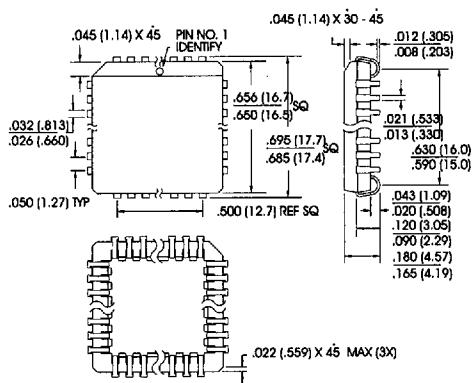
**44A, 44 Lead, Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (TQFP)**  
Dimensions in Inches and (Millimeters)



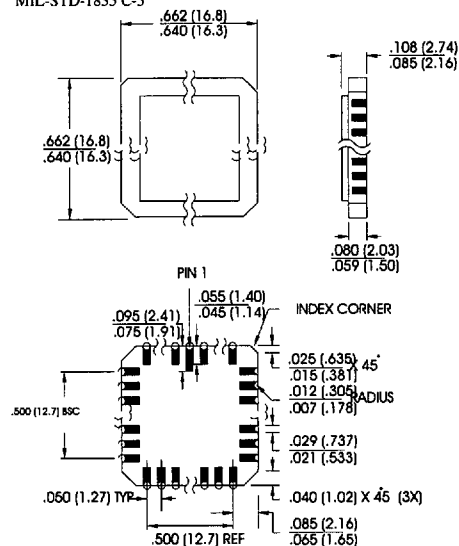
**40D6, 40 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)**  
Dimensions in Inches and (Millimeters)  
MIL-STD-1835 D-5 CONFIG A



**44J, 44 Lead, Plastic J-Leaded Chip Carrier (PLCC)**  
Dimensions in Inches and (Millimeters)  
JEDEC OUTLINE MO-047 AC



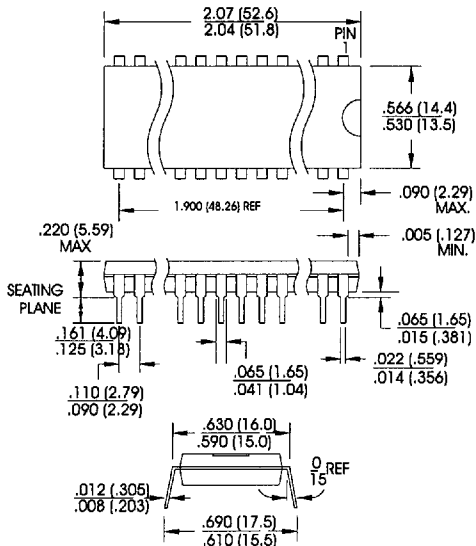
**44L, 44 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)**  
Dimensions in Inches and (Millimeters)\*  
MIL-STD-1835 C-5



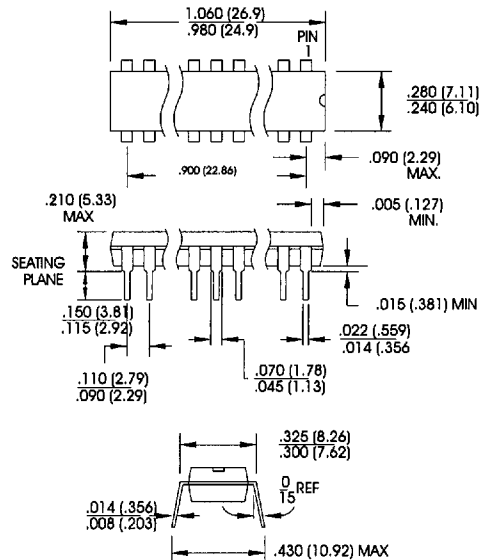
\*Ceramic lid standard unless specified.



**40P6, 40 Lead, 0.600" Wide,  
Plastic Dual Inline Package (PDIP)  
Dimensions in Inches and (Millimeters)**

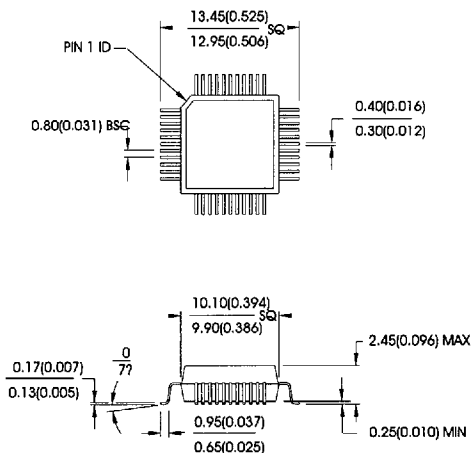


**20P3, 20 Lead, 0.300" Wide,  
Plastic Dual Inline Package (PDIP)  
Dimensions in Inches and (Millimeters)**



\*Controlling dimension: millimeters

**44Q, 44 Lead, Plastic Gull Wing Quad Flat Package (PQFP)**  
Dimensions in Inches and (Millimeters)



**20S, 20 Lead, 0.300" Wide,  
Plastic Gull Wing Small Outline (SOIC)  
Dimensions in Inches and (Millimeters)**

