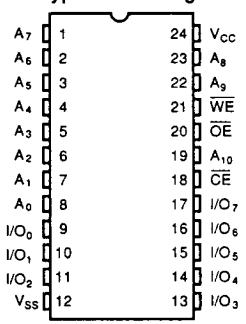
2K X 8 CMOS Electrically Erasable PROM

FEATURES

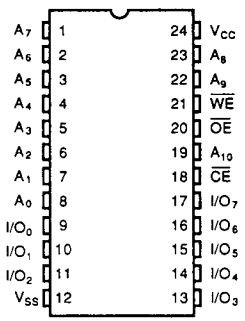
- **Fast Read Access Times**
  - **— 100ns, 150ns, 200ns, 250ns**
- **Low CMOS Power Consumption**
  - **— 30mA active (max.)**
  - **— 100µA standby (max.)**
- **5 Volt-only Operation**
  - **— Including Write**
- **Industrial Temperature Range Available (XLE28C16B)**
- **Fast Nonvolatile Write Cycle**
  - **— Internally Latched Data and Address**
  - **— 120ns Byte-load Cycle**
  - **— 5ms Nonvolatile Write Cycle**
- **On-chip Inadvertent Write Protection**
- **Unlimited Read Cycle Endurance**
- **10,000 Rewrites per Byte**
- **10 Year Secure Data Retention**
- **$\overline{\text{DATA}}$ Polling To Minimize Write Cycle Times**
- **Reliable Floating Gate CMOS Technology**
- **16 Byte Page Mode**

PIN CONFIGURATION

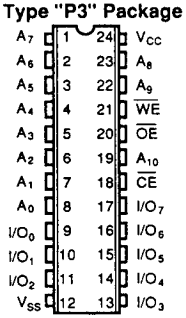
24 Pin PDIP
Type "P" Package



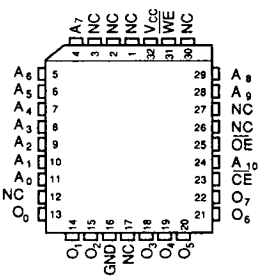
24 Pin CERDIP
Type "C" Package



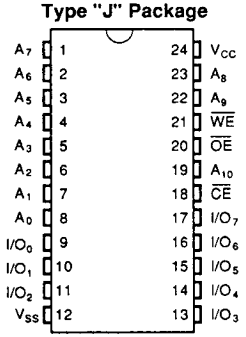
24 Pin Skinny DIP
Type "P3" Package



32 Pin PLCC
Type"D" Package



Small Outline
Type "J" Package



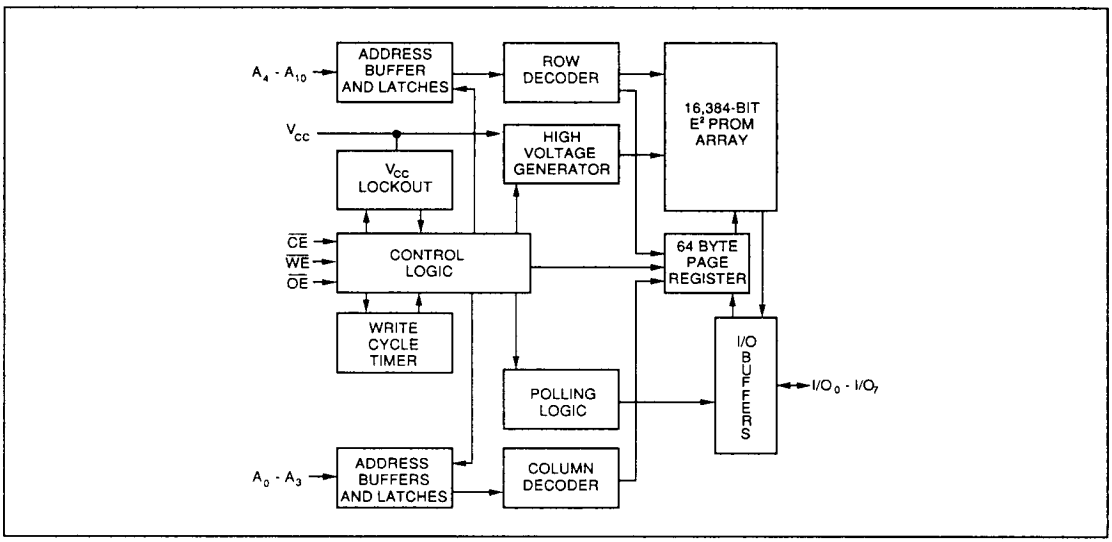
PIN NAMES

A_0-A_{10}	Address Inputs
I/O_0-I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Power and Signal Ground
NC	No Connect

OVERVIEW

The XL28C16B is a full-featured, 2K x 8 bit CMOS E²PROM (Electrically Erasable Programmable Read Only Memory). Operationally, it is compatible with industry standard 16K bit E²PROM devices, and it offers improved speed and power efficiency. Read access times are as low as 100ns; standby current, less than 100µA. The device is fully functional with a single 5V power supply, and the XL28C16B is manufactured with EXEL's 1.5µ CMOS E²PROM process.

BLOCK DIAGRAM



The sophisticated architecture of this device provides complete and automatic control of the nonvolatile write cycle eliminating the need for external timers, latches, high voltage generators and inadvertent write protection circuitry. It fits into a standard SRAM socket and responds to typical SRAM write commands.

The XL28C16B features V_{CC} lockout, power-on reset and noise protected $\overline{WE}$, to inhibit inadvertent writes.

The XL28C16B is compatible with industrial standard 2K x 8 E^2PROMS — its pinouts and operating modes conform to established standards. This compatibility extends to higher and lower density EXEL E^2PROMS as well.

APPLICATIONS

The XL28C16B provides secure and reliable data storage thoughout your system's lifetime, both during periods of power on and power off. It may be written to through standard microprocessor protocols as if it were a Static RAM, yet it retains its data in the absence of system power for at least 10 years after the data is written. This flexibility has resulted in a wide variety of digital system applications.

The nonvolatile storage in the XL28C16B replaces dip switches as a means of storing configuration data. It delivers firmware for booting up systems, and for operating industrial and process controllers, traffic controllers, robotics and telemetry, measuring instruments and appliance controls. It retains phone numbers and messages in facsimile machines. The XL28C16B is ideal in applications that are self-adapting such as video games and systems that require automatic re-calibration, as well as those that are subject to power failures.

ENDURANCE and DATA RETENTION

The XL28C16B is designed for applications requiring up to 10,000 data changes per E^2PROM byte ensuring a guaranteed endurance of 20 million data changes per device. It provides 10 years of secure data retention, with or without power applied after the data is written.

DEVICE OPERATION

Three control pins ($\overline{CE}$, $\overline{OE}$ and $\overline{WE}$) select all standard user-operating modes for the XL28C16B. Chip erase (typically executed during test procedures) requires a higher supply voltage on one input pin. This conforms with existing E^2PROM standards.

Read Mode
Data is read from the XL28C16B by bringing both $\overline{CE}$ and $\overline{OE}$ LOW while keeping $\overline{WE}$ HIGH. With the read mode selected, address lines can be changed at any time, in any order to read data at various locations in the E^2PROM array. Read access time is measured from the time when the final controlling line ($\overline{CE}$ or $\overline{OE}$) goes LOW, or the time when the address is established.

The device can be read an unlimited number of times, because the stored charge that defines the bit state is not affected by a read cycle. (See Figure 2.)

Write Mode
The XL28C16B uses a two-step process to store new data. Byte-load cycles fill latches in a volatile page buffer. A subsequent nonvolatile write cycle transfers new entries in the page-buffer to the E^2PROM array.

The XL28C16B contains 128 16-byte pages. Address lines A_4-A_{10} identify the page: lines A_0-A_3 identify the byte within the page. All bytes written within one write cycle must be on the same page (A_4-A_{10} must remain unchanged). Any number of the 16 bytes in the page can be written or re-written, in any order; the last data written is retained.

Either $\overline{WE}$ or $\overline{CE}$ can be used to trigger the byte-load cycle. The address is latched into internal address latches upon the last falling edge of $\overline{WE}$ or $\overline{CE}$. A byte-load timer is started on the subsequent rising edge of the controlling line. The timer provides a 75µS window for initiating the next byte-load cycle. Byte-loading can continue indefinitely if each new load cycle is started within the timeout period. Please note that all write cycles require that $\overline{OE}$ is held HIGH.

When the timer times out, additional byte-load cycles are inhibited and data is automatically transferred from the page buffer to the E^2PROM array during the internal nonvolatile write cycle. Byte flags, set during the byte-load cycles, ensure that high voltage is applied only to newly written bytes. By avoiding the unnecessary cycling of bytes, the endurance of the array is extended. The nonvolatile write cycle is immune to any concurrent control pin activity.

A write-latch is set on the first byte-load of each write cycle. Output pins remain in a high impedance state except during a byte-load (when they contain new input data) or during a $\overline{DATA}$ polling read cycle. When the nonvolatile cycle is completed, the operating mode is again determined by the control pins ($\overline{CE}$, $\overline{OE}$ and $\overline{WE}$). (See Figures 3, 4 and 6.)

Output Disable Mode
If, while in the read mode, $\overline{OE}$ is brought HIGH, the device remains in the read mode, but with the outputs disabled. (I/O pins are in a high impedance state.)

Standby Mode
Whenever $\overline{CE}$ is brought HIGH, the device is set into its standby mode, placing the I/O pins in a high impedance state. Standby power dissipation is less than 100µA with CMOS level inputs. While $\overline{CE}$ remains HIGH, all other input pins are disabled, insulating the device from activity on the system busses.

Chip Erase
The chip erase mode allows the user to erase the entire E^2PROM array with a single command. The method requires the application of high voltage (V_H) on the $\overline{OE}$ pin, with $\overline{CE}$ at a logical "0." Chip erase is initiated by a standard byte write command while holding data on the I/O inputs high. A byte containing all "1's" is automatically written to all locations in the E^2PROM array. (Refer to the Mode Selection chart.)

MONITORING DEVICE STATUS

Because the internal nonvolatile write cycle is completely managed by the XL28C16B, a status indicator has been incorporated to provide for the system to monitor the READY/$\overline{BUSY}$ status of the device. This is accomplished through a system software routine which simply re-reads the XL28C16B until it determines a simple logical condition.

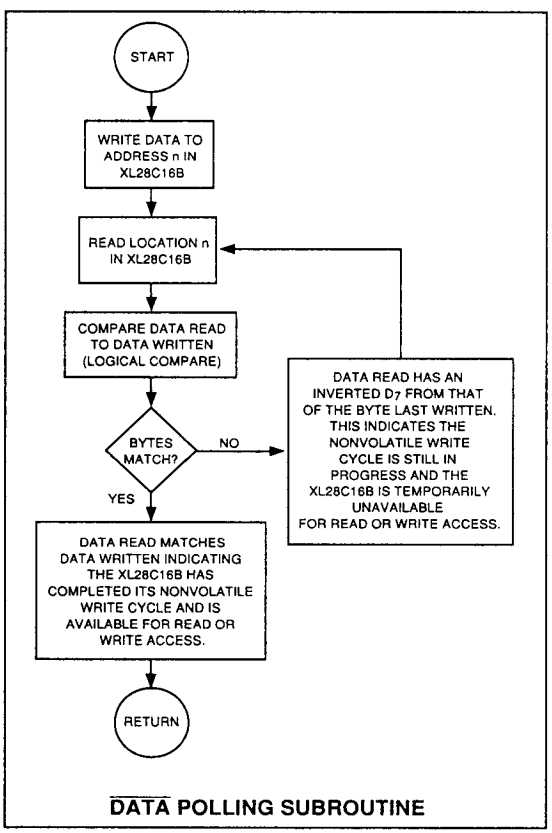
MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
V_{IH}	X	X	Standby	HIGH Z	Standby
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
V_{IL}	V_{IH}	⌐‾⌐	Byte Write ($\overline{WE}$ Controlled)	D_{IN}	Active
⌐‾⌐	V_{IH}	V_{IL}	Byte Write ($\overline{CE}$ Controlled)	D_{IN}	Active
V_{IL}	V_H	V_{IL}	Chip Erase*	Data In=V_{IH}	Active
X	V_{IL}	X	Write Inhibit	—	—

*Contact EXEL for details

$\overline{\text{DATA}}$ Polling

The XL28C16B provides a feature named $\overline{\text{DATA}}$ polling which enables the host system to determine the status of the device through the use of the system busses. No additional hardware is required. Any attempt to read the part while the XL28C16B is busy executing its nonvolatile write cycle will be interpreted as a $\overline{\text{DATA}}$ polling read. This is performed by exercising the control pins in the same sequence as for a normal read. $\overline{\text{DATA}}$ polling cycles have no effect on the byte-load timer, contents of the data buffer or nonvolatile cycle timing.



$\overline{\text{DATA}}$ POLLING SUBROUTINE

$\overline{\text{DATA}}$ polling is a simple software technique used to determine the status of the XL28C16B. It is executed as a normal read cycle where the target byte location is the same as that of the byte last written to the XL28C16B. During the 5ms (max.) period that the device requires to complete its nonvolatile write cycle, the I/O buffers are set in a high impedance state with the exception of I/O_7. I/O_7 is set to output the **complement** of the value of the MSB of the last byte written to the XL28C16B when a read command is asserted.

The procedure is quite simple. The system reads the location last written to in the XL28C16B and executes a compare operation between the data thus retrieved and the original data byte written. If the compare fails, the XL28C16B is still busy with its nonvolatile write cycle. If the compare passes, the nonvolatile write cycle is complete and the device is available for read or write accesses.

This procedure is commonly used to determine the actual nonvolatile write cycle completion timing eliminating the need to await the 5ms (max.) period specified and enabling accelerated device loading operations. (See Figure 5.)

WRITE PROTECT MECHANISMS

The XL28C16B features several integrated mechanisms to protect it from inadvertent writes that might occur during system power supply transitions or periods of system noise. In addition to the user-controlled protection mechanisms, the following specialized circuits are built in.

$\overline{\text{OE}}$ Write Inhibit

If $\overline{\text{OE}}$ is brought LOW before the $\overline{\text{CE}}$ and $\overline{\text{WE}}$ write command sequence, the internal nonvolatile write cycle will not occur. See the Mode Selection Table on page 3.

Noise Protection

Write pulses of less than 10ns duration on the $\overline{\text{WE}}$ pin will not initiate nonvolatile write cycles.

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Soldering Temperature (less than 10 seconds) ..... 300°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pin* ..... -0.6V to +7.0V
Voltage on $\overline{OE}$ Pin* ..... -0.6V to +15V
ESD Rating 2000V
DC Output Current 5mA
*With respect to ground

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Although this product includes specific circuitry to protect it from electrostatic discharge, conventional precautions should be taken to protect it from any voltages higher than the rated maxima.

DC CHARACTERISTICS

T_A = 0°C to +70°C for the XLS28C16B or -40°C to +85°C for the XLE28C16B, V_{CC} = 5V±10%

Symbol	Parameter	Test Conditions	Min.	Max.	Units
I_{CC}	V_{CC} Current-Active (TTL)	$\overline{CE}$ = $\overline{OE}$ = V_{IL} WE = V_{IH} I/O's = open A_0-A_{12} = toggling f = 5 MHz		30	mA
I_{SB}	V_{CC} Current-Standby (TTL)	$\overline{CE}$ = V_{IH} $\overline{OE}$ = V_{IL} I/O's = open A_0-A_{12} = V_{CC}		2	mA
I_{SBC}	V_{CC} Current-Standby (CMOS)	$\overline{CE}$ >= V_{CC}-0.2 $\overline{OE}$ = V_{IL} I/O's = open A_0-A_{12} >= V_{CC}-0.2		100	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}	-10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC} $\overline{CE}$ = V_{IH}	-10	10	µA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}+ 0.5	V
V_{OL}	Output Low Voltage	I_{OL}= 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400µA I_{OH} = -10µA	2.4 V_{CC}-0.1		V V
V_H	High Voltage for Chip Erase		11.4	12.6	V

CAPACITANCE

T_A= +25°C, f = 1.0 MHz

Symbol	Test	Test Conditions	Max.	Units
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V	10	pF
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF

AC OPERATING CHARACTERISTICS

READ CYCLE (See Figure 2)

T_A = 0°C to +70°C for the XLS28C16B or -40°C to +85°C for the XLE28C16B, V_{CC} = 5V±10%

Symbol	Parameter	XL28C16B-100 Limits		XL28C16B-150 Limits		XL28C16B-200 Limits		XL28C16B-250 Limits		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	100		150		200		250		ns
t_{AA}	Address Access Time		100		150		200		250	ns
t_{CE}	Chip Enable Access Time		100		150		200		250	ns
t_{OE}	Output Enable Access Time		70		80		90		100	ns
t_{LZ}	Chip Enable to Output in Low Z	0		0		0		0		ns
t_{HZ}	Chip Disable to Output in High Z	0	50	0	50	0	50	0	60	ns
t_{OLZ}	Output Enable to Output in Low Z	0		0		0		0		ns
t_{OHZ}	Output Disable to Output in High Z	0	35	0	50	0	50	0	60	ns
t_{OH}	Output Hold from Address Change	15		15		15		15		ns

WRITE CYCLE (See Figures 3, 4, 5 and 6)

T_A = 0°C to +70°C for the XLS28C16B or -40°C to +85°C for the XLE28C16B, V_{CC} = 5V±10%

Symbol	Parameter	Min.	Max.	Units
t_{WC}	Write Cycle Time		5	ms
t_{BLC}	Byte Load Cycle	.120	100	µs
t_{AS}	Address Setup Time	0		ns
t_{AH}	Address Hold Time	35		ns
t_{CS}	Write Setup Time	0		ns
t_{CH}	Write Hold Time	0		ns
t_{CW}	Chip Enable Pulse Width	50		ns
t_{OES}	Output Enable Setup Time	5		ns
t_{OEH}	Output Enable Hold Time	5		ns
*t_{WP}	Write Enable Pulse Width	70		ns
t_{WPH}	Write Pulse Width High	50		ns
t_{DS}	Data Setup Time	30		ns
t_{DH}	Data Hold Time	0		ns
t_{DV}	Data Valid Time		1	µs
t_{INIT}	Power-up Initialization Period		20	ms

* Note: A write pulse of less than 10ns will not initiate a write cycle.

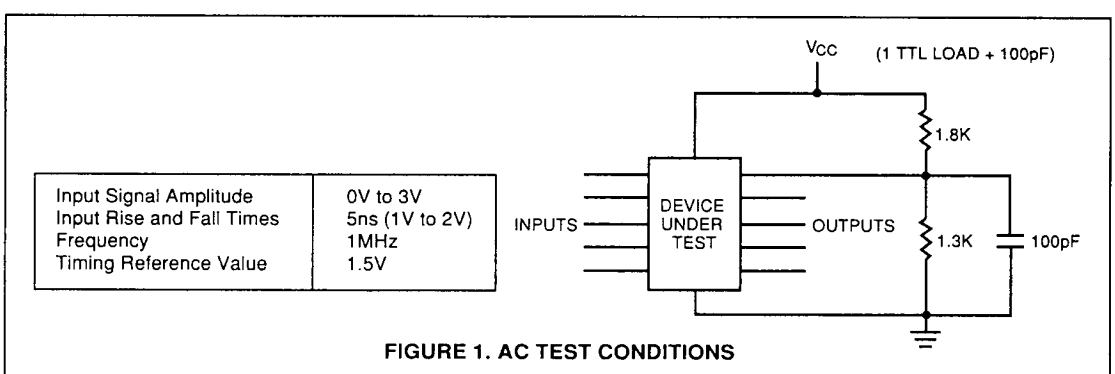


FIGURE 1. AC TEST CONDITIONS

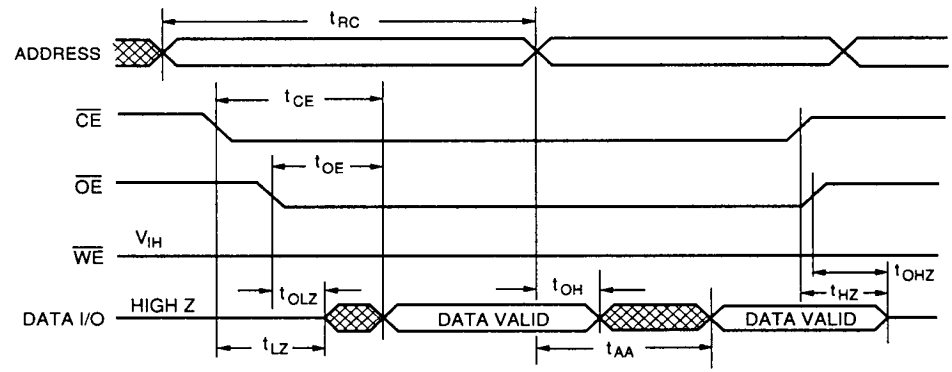


FIGURE 2. READ CYCLE TIMING

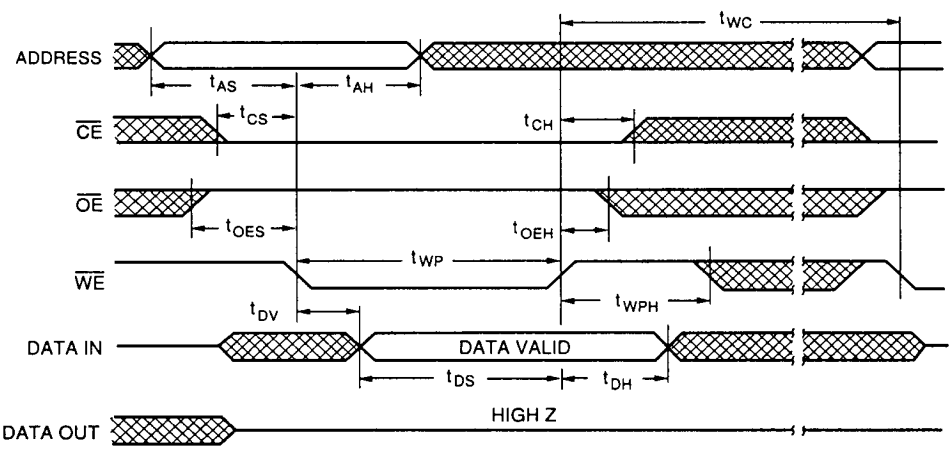


FIGURE 3. $\overline{WE}$ CONTROLLED WRITE CYCLE TIMING

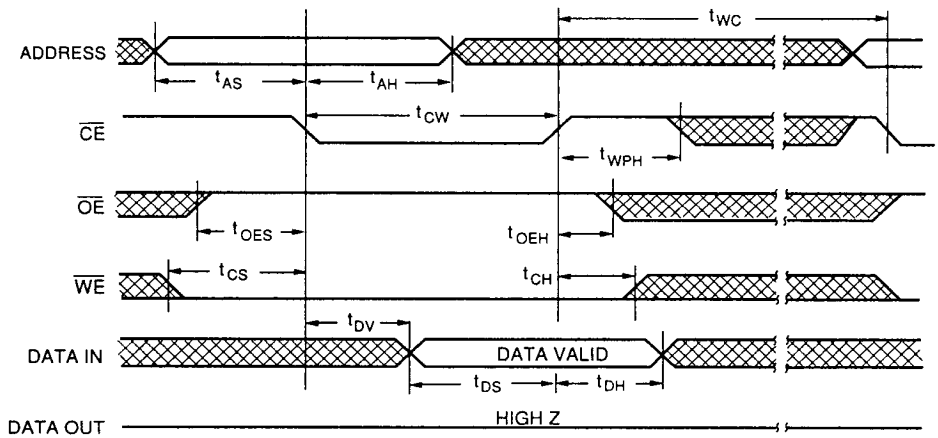
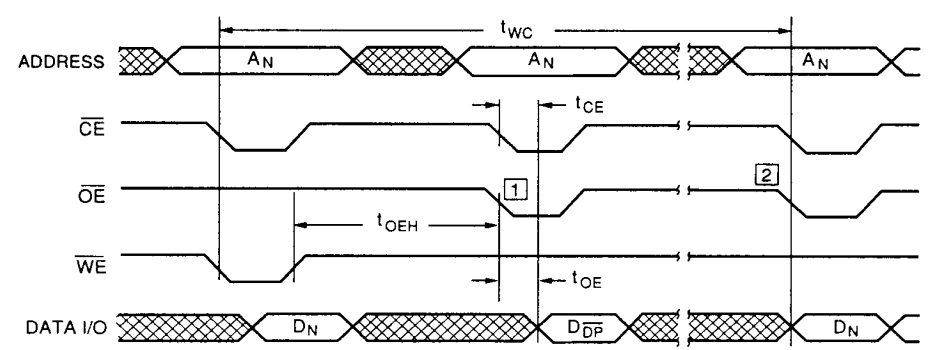


FIGURE 4. $\overline{CE}$ CONTROLLED WRITE CYCLE TIMING



1. This initiates a read cycle yielding $D_{\overline{DP}}$ (inverted MSB) at the output buffer indicating the device is still busy with the nonvolatile write cycle.

2. This initiates a read cycle yielding the data which was written to the XL28C16B indicating that the nonvolatile write cycle is complete and that the device is available for subsequent commands.

FIGURE 5. $\overline{DATA}$ POLLING TIMING

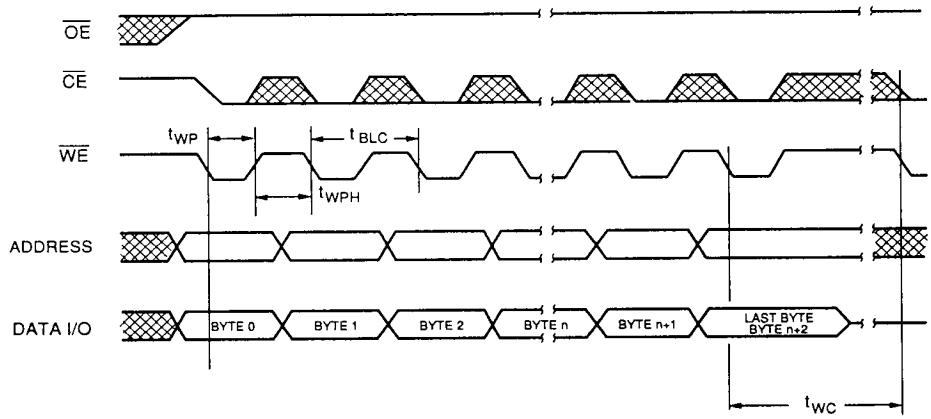


FIGURE 6. PAGE MODE WRITE CYCLE TIMING