RICOH

Microelectronic Specification

RP2X04

THERMAL HEAD DRIVER WITH LATCH RESET AND ENABLE

■ GENERAL DESCRIPTION

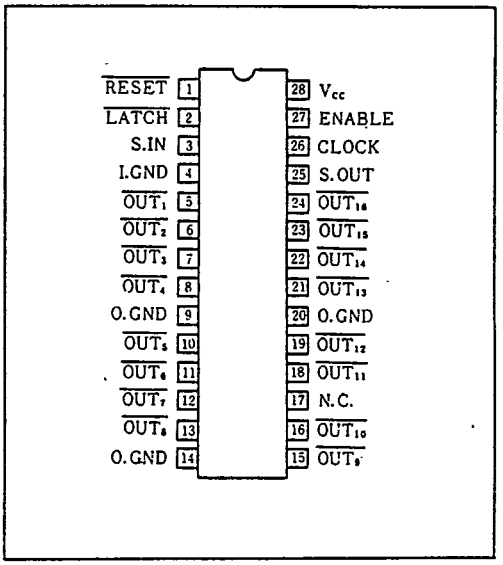
The RP2X04 is a thermal head and LED driving IC with 16-bit S/P shift register. It is provided with serial input function and parallel output function with high breakdown voltage.

The RP2X04 has such functions as RESET, LATCH and ENABLE, and is able to operate clear, hold, inhibit, etc, of parallel output data.

As it has a common clock terminal and a serial output terminal, the cascade connection, too, is possible, resulting in diversity in use, extensibility in function and easiness in increasing bit.

The RP2X04 operates from a 5V single power supply as in the case of TTL, and its inputs and outputs are compatible with TTL.

■ PIN CONFIGURATION (Top view)



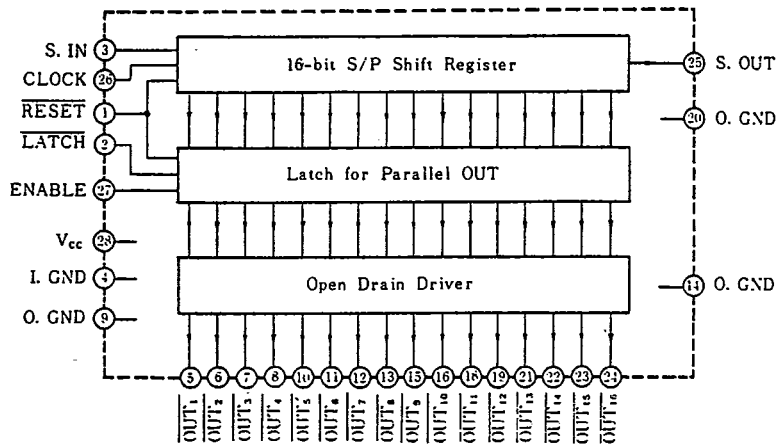
■ FEATURES

- Thermal head driver with 16-bit S/P shift register
- RESET, LATCH and ENABLE functions of the parallel output data
- High breakdown voltage ····· Drain breakdown voltage : 20.5V (Max)
- Large output current ····· Sink current : 60mA/Pin
- High operating frequency ····· 3MHz (Max)
- Low power dissipation ····· 30mW (Max)
  (NOTE: This value does not include power dissipation of Open Drain Tr.)
- 28-pin plastic DIL package
- Nch. Si gate MOS construction

■ APPLICATIONS

The RP2X04 in itself is what was developed for the purpose of driving the thermal head, but it can be used also for driving small power lamps such as LED, etc., and in addition, for driving the data series-parallel converter. It has, therefore, wide range of application fields including peripheral equipment of microcomputer, various equipment, etc.

■ BLOCK DIAGRAM



NOTE: The GND for open drain transistors is provided separately from that (I. GND) for the logic circuit because it should allow large current to flow.

■ ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

Symbol	Parameters	Measuring Conditions	Rated Values	Unit
V_{TE}	Pin Voltage	GND=0V	−0.5~7	V
V_{OT}	Open Drain Breakup (NOTE)	GND=0V	21.0	V
I_D	Drain Current		80	mA
P_d	Maximum Power Dissipation		600	mW
T_{opr}	Operating Ambient Temperature		0~70	℃
T_{stg}	Storage Ambient Temperature		−40~125	℃

NOTE : Open Drain Breakdown Voltage means voltage that can be applied to the parallel output terminal.

■ RECOMMENDED OPERATING CONDITIONS (Unless Specified : Ta=0~70℃)

Symbol	Parameters	Rating Value			Unit
		Min	Typ	Max	
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V
f_{CK}	Clock Frequency	DC	1.0	3.0	MHz
V_{OT}	Open Drain Breakup			20.5	V
I_D	Drain Current			60	mA/pin

■ ELECTRICAL CHARACTERISTICS

● DC ELECTRICAL CHARACTERISTICS (Unless Specified : Ta=0~70℃, V_{CC}=5V±10%)

Symbol	Parameters	Measuring Conditions	Specified Value			Unit	Remarks
			Min	Typ	Max		
V_{IL}	"L" Input Voltage		−0.5		0.8	V	
V_{IH}	"H" Input Voltage		2.0		V_{CC}+0.5	V	
V_{OL1}	"L" Output Voltage	I_{OL}=1.6mA			0.4	V	pin 25
V_{OH}	"H" Output Voltage	I_{OH}=−100μA	2.4			V	
V_{OL2}	"L" Output Voltage	0.1V<V_{OL}<0.5V	0.1		0.5	V	pin 5~8
V_{OT}	Open Drain Breakdown Voltage	I_{OZ}<100μA			20.5	V	pin 10~13
I_D	Drain Current	0.1V<V_{OL}<0.5V			60	mA	pin 15, 16, 18, 19
I_{OLK}	Output Leak Current	V_{OT}=20.5V			±100	μA	pin 21~24
I_{ILK}	Input Leak Current	0≦V_I≦V_{CC}			± 10	μA	
I_{IL}	Input Current	0≦V_I≦V_{CC}			−100	μA	
I_{CC}	V_{CC} Power Supply Current	0≦V_I≦V_{CC}			5.4	mA	f_{CK} ≦100k times/sec.

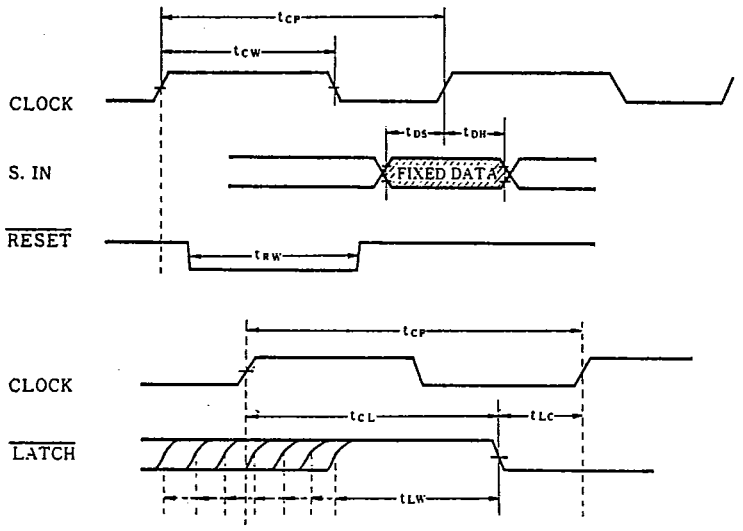
● AC OPERATING CONDITIONS (Unless Specified : Ta=0~70℃, V_{CC}=5V±10%)

Symbol	Parameters	Measuring Conditions	Specified Value			Unit	Remarks
			Min	Typ	Max		
t_{CP}	Clock Cycle		330	1000	DC	ns	
t_{CW}	Clock Pulse Width		100	600	t_{CP}-150	ns	
t_{DS}	Data Set-up Time		60			ns	
t_{DH}	Data Hold Time		35			ns	
t_{RW}	Reset Pulse Width		200			ns	
t_{LW}	Latch Pulse Width		230			ns	
t_{CL}	Clock—Latch Time		300			ns	
t_{LC}	Latch—Clock Time		−15			ns	

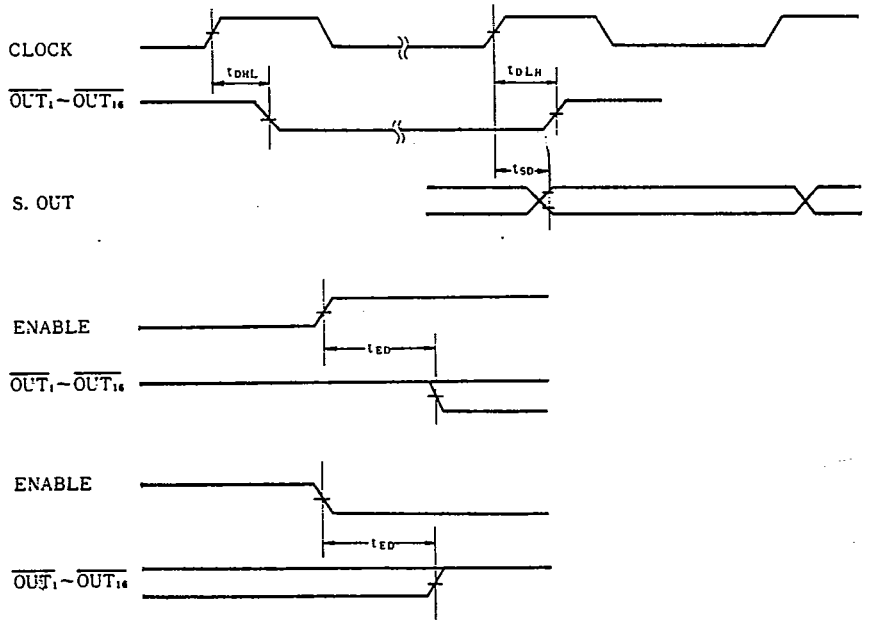
● AC ELECTRICAL CHARACTERISTICS (Unless specified : Ta=0~70℃, V_{CC}=5V±10%)

Symbol	Parameters	Measuring Conditions	Specified Value			Unit	Remarks
			Min	Typ	Max		
t_{DHL}	Turn-on Delay Time	V_{OL}=0.5V no load			10	μs	
t_{DLH}	Turn-off Delay Time	V_{OH}=6V no load			10	μs	
t_{SD}	Series Output Data Delay Time	C_L=25pF	40		250	ns	
t_{ED}	Enable Signal Delay Time				10	μs	

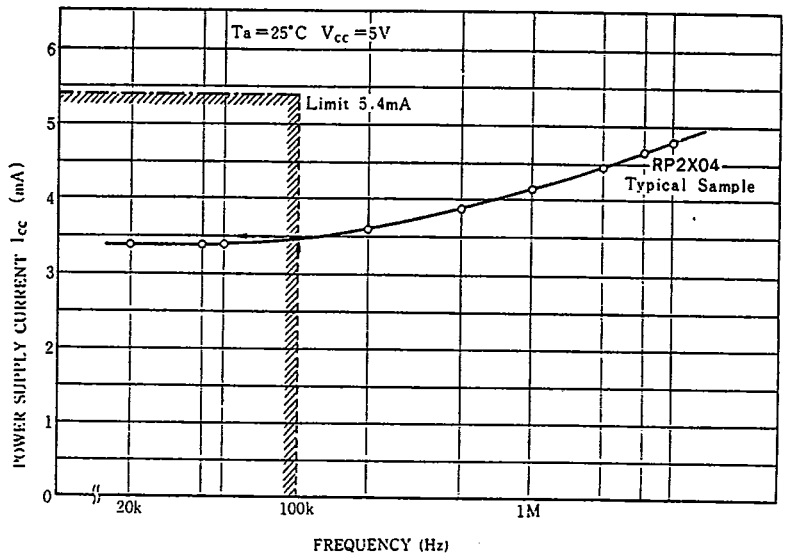
■ INPUT DATA TIMING DIAGRAM



■ TIMING DIAGRAM



■ DEPENDENCY OF I_{cc} OPERATING FREQUENCY



■ EXPLANATION ON PIN FUNCTIONS

Pin Name	Pin Number	I/O	Functions
$\overline{\text{RESET}}$	1	I	Shift Register and Latch data are reset (LOW) by making this pin at LOW by means of Reset input. It is connected internally to V_{cc} through Pull-up resistor.
$\overline{\text{LATCH}}$	2	I	Latch command input for the parallel output data. The parallel output is latched by making this pin at LOW. It is connected internally to V_{cc} through Pull-up resistor.
S.IN	3	I	Serial input of 16-bit S/P Shift register
I.GND	4	I	INPUT GND GND of Logic Circuits
$\overline{\text{OUT}}_{1\sim16}$	5, 6, 7, 8, 10, 11 12, 13, 15, 16, 18, 19 21, 22, 23, 24	O	Open Drain Giant Transistor Parallel Output. (Each pin can be applied with high voltage of 20.5V at maximum and large current of 60mA/pin at maximum.)
S.OUT	25	O	Serial data output
CLOCK	26	I	Clock Input
ENABLE	27	I	When this pin is High, the parallel output is possible. It is internally pulled up to V_{cc}.
V_{cc}	28	I	+5V Power Supply
O.GND	9, 14, 20	I	GND (0V) for the parallel output driver

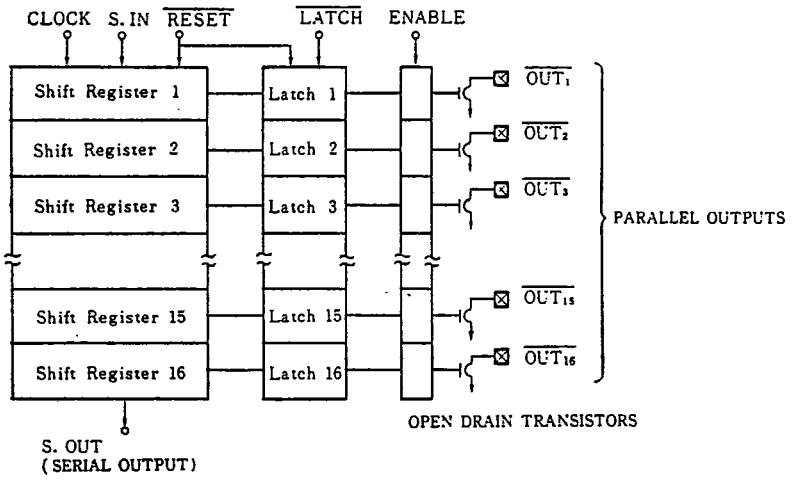
NOTE: The GND for open drain transistors is provided reparately from that (I GND) for the logic circuit because large current flows in it.

■ EXPLANATION ON INTERNAL FUNCTION

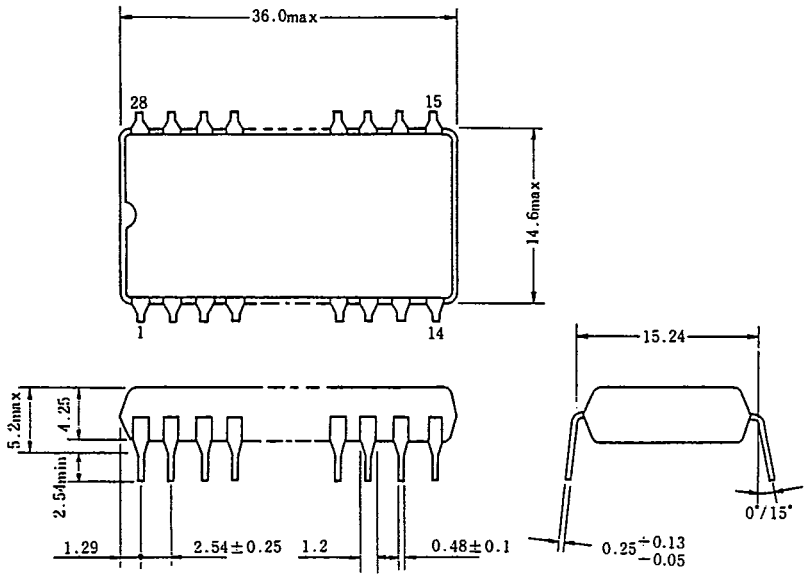
The RP2X04 consists of the 16-bit shift register with S/P conversion function and the open drain driver unit for parallel output.

The data that was put in through S.IN terminal is 16-bit shifted, and then put out from S.OUT in synchronization with rise-up of CLOCK.

When the ENABLE terminal and the $\overline{\text{LATCH}}$ terminal are at HIGH level, output is put out in parallel, too. In case of holding the parallel output data independently of CLOCK, all that is necessary is to make the $\overline{\text{LATCH}}$ terminal to the LOW level. For resetting each bit, the $\overline{\text{RESET}}$ terminal is made at the LOW level. In this case, the open drain driver is in the state of OFF. When the ENABLE terminal is at the LOW level, all the open drain driver terminals get in the state of OFF, while the information in the shift register is kept as it is.



■ 28-PIN PLASTIC DIL PACKAGE (EXTERNAL VIEW)(Unit : mm)



T-51-15