

Microelectronic Specification

RF5H01 / RP5H01

64-bit CMOS PROM WITH 6/7-bit BINARY COUNTER

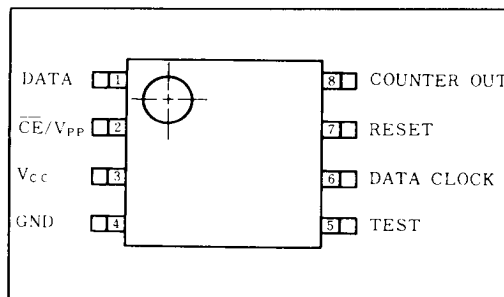
■ GENERAL DESCRIPTION

RF5H01/RP5H01 is a PROM with 64×1 bit organization (+ dummy 8 bits), employing 2 layer silicon gate CMOS processing technology.

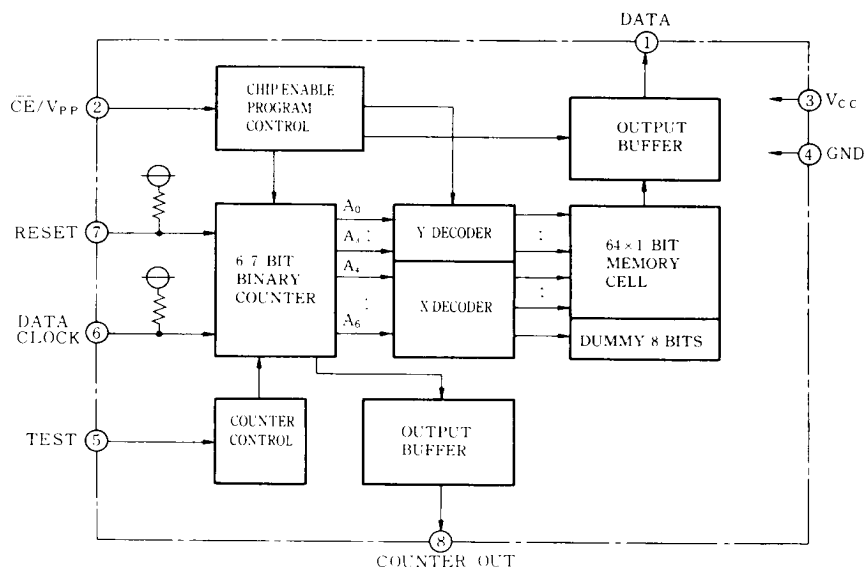
■ FEATURES

- 64×1 bit organization (+ dummy 8 bits)
- Low power dissipation
 - Active 55mW (max)
 - Standby $550\mu\text{W}$ (max)
- Access time $1\mu\text{s}$ (max)
- Single power supply $5\text{V} \pm 10\%$
- Serial outputs
- Inputs and outputs TTL level
- 3 state (Tri-state) outputs

■ PIN CONFIGURATION (Top view)



■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Symbol	Parameters	Conditions	Limits	Unit
V_{CC}	V_{CC} Supply Voltage	With respect to GND	-0.3 ~ 7	V
V_{PP}	V_{PP} Supply Voltage		-0.3 ~ 22	V
V_I	Input Voltage		-0.3 ~ 7	V
V_O	Output Voltage		-0.3 ~ 7	V
P_d	Maximum Power Dissipation	$T_a = 25^\circ\text{C}$	0.3	W
T_{OPR}	Operating Temperature Range		-20 ~ 70	$^\circ\text{C}$
T_{STR}	Storage Temperature		-40 ~ 125	$^\circ\text{C}$

■ RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim 70^\circ\text{C}$)

Symbol	Parameters	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.0		$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage	-0.1		0.8	V

■ ELECTRICAL CHARACTERISTICS

● READ OPERATION D.C. CHARACTERISTICS ($T_a = -20 \sim 70^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$)

Symbol	Parameters		Test Conditions	Limits			Unit
				Min	Typ	Max	
I_{CC1}	Standby V_{CC} Supply Current		CE, $V_{PP} = V_{CC} + 0.3V$ DATA CLOCK, RESET = V_{IL} or Open TEST = GND or $V_{CC} \pm 0.3V$			100	μA
I_{CC2}	Operating V_{CC} Supply Current		$I_{OUT} = 0\text{mA}$			10	mA
V_{OH}	Output High Voltage		$I_{OH} = -400\mu\text{A}$	2.4			V
V_{OL}	Output Low Voltage		$I_{OL} = 2.1\text{mA}$			0.45	V
V_{IH}	Input High Voltage	Except TEST		2.0		$V_{CC} + 0.3$	V
		TEST		4.0		$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage	Except TEST		0.1		0.8	V
		TEST		-0.1		1.0	V
I_{LI}	Input Leakage Current	RESET, DATA CLOCK	$V_I = 0V, V_{CC} = 5.5V$	-180		-20	μA
		TEST, CE/ V_{PP}	$V_I = 0V \sim V_{CC}$	-10		10	μA
I_{LO}	Output Leakage Current		$V_O = 0V \sim V_{CC}$	-10		10	μA

● READ OPERATION, A.C. CHARACTERISTICS ($T_a = -20 \sim 70^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$)

Symbol	Parameters	Test Conditions		Limits			Unit
				Min	Typ	Max	
t _{ACC}	Clock to Output Delay	CE, V _{PP} = V _{II}	Load = 1TTL + 100pF			1	μs
t _{CE}	CE to Output Delay					1	μs
t _{DF}	CE High to Output Float			0		200	ns
t _{RW}	Reset pulse width			2			μs
t _{CW}	Clock pulse width		2			μs	

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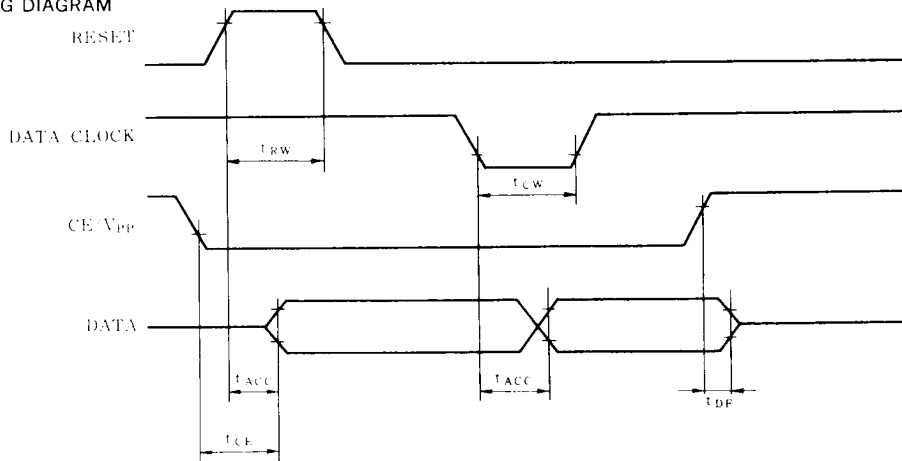
● D.C. PROGRAMMING CHARACTERISTICS $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$

Symbol	Parameters		Test Conditions	Limits			Unit
				Min	Typ	Max	
I_{PP}	V_{PP} Supply Current		$\overline{\text{CE}}/V_{PP} = V_{IMP}$			5	mA
I_{CC}	V_{CC} Supply Current					0.5	mA
V_{IH}	Input High Voltage	Except TEST		2.0		$V_{CC} + 0.3$	V
		TEST		4.0		$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage	Except TEST		-0.1		0.8	V
		TEST		-0.1		1.0	V
V_{IMP}	Program pulse Input High Voltage			20.5	21.0	21.5	V
V_{ILP}	Program pulse Input Low Voltage			2.0	V_{CC}	6.0	V
I_{II}	Input leakage Current	RESET, DATA, CLOCK	$V_I = 0\text{V}$, $V_{CC} = 5.25\text{V}$	-170		-20	μA
		TEST	$V_I = 0\text{V} \sim V_{CC}$	-10		10	μA

● PROGRAMMING CHARACTERISTICS $(T_a = 25^\circ\text{C} \pm 5^\circ\text{C}, V_{CC} = 5\text{V} \pm 5\%)$

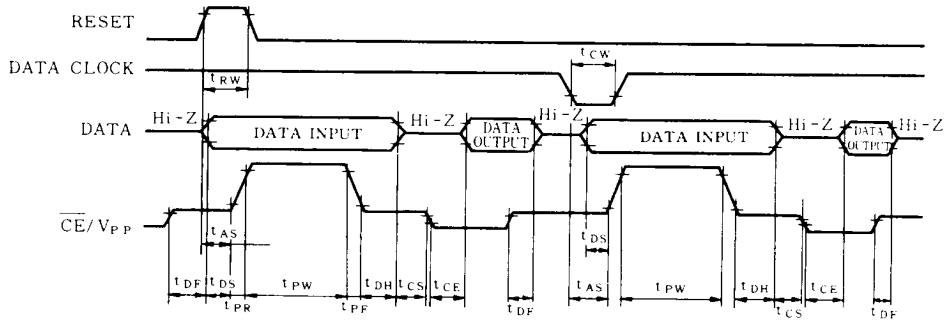
Symbol	Parameters	Limits			Unit
		Min	Typ	Max	
t_{AS}	Address Set-up Time	2			μs
t_{CS}	$\overline{\text{CE}}$ Set-up Time	2			μs
t_{DS}	Data Set-up Time	2			μs
t_{DH}	Data Hold Time	2			μs
t_{DF}	$\overline{\text{CE}}$ to Output Float	0		200	ns
t_{CF}	$\overline{\text{CE}}$ to Output Delay			1	μs
t_{PW}	Program pulse width	45	50	55	ms
t_{PR}	V_{PP} Pulse rise time	0.5		100	μs
t_{PF}	V_{PP} Pulse fall time	0.5		100	μs
t_{RW}	Reset pulse width	2			μs
t_{CW}	Clock pulse width	2			μs

■ TIMING DIAGRAM



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● PROGRAM MODE



■ OPERATING MODES

Pins	Data	Counter output	CE/V _{PP}	V _{CC}	GND
Mode	1	8	2	3	4
Read	Data Output	Clock/A5 Output	V _{IL}	V _{CC}	GND
Standby	High impedance	High impedance	V _{IH}	V _{CC}	GND
Program	Data Input	High impedance	V _{IOP}	V _{CC}	GND

	Counter operation mode
TEST (5) = GND	6 bits
TEST (5) = V _{CC}	7 bits

■ EXPLANATION ON OPERATION

● READ MODE

RF5H01/RP5H01 is a serial address type PROM with 6-bit/7-bit counter. The first bit can be read out by adding reset pulse after $\overline{\text{CE}}/\text{V}_{\text{PP}} = \text{V}_{\text{IL}}$. The 2nd bit~the 64th bit can be sequentially read out by adding data clock pulse. The output data is valid after a delay of t_{ACC} from reset rise up or data clock fall down, in the state of $\overline{\text{CE}}/\text{V}_{\text{PP}} = \text{V}_{\text{IL}}$.

In the state of TEST=GND, the counter operates as a 6-bit counter. It returns to the reset condition (address 000000), if it is added with 64-time data clock pulses after the reset pulse is applied.

The counter output pin is for operation test of the built-in counter. It puts out the highest output (A5) of the 6-bit counter.

● STANDBY MODE

RF5H01/RP5H01 is provided with power down function that is controlled by CE input. If TTL high level is given to the chip enable input ($\overline{\text{CE}}$), the device comes to be the Standby Mode, and the output is in the state of high impedance.

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● PROGRAM MODE

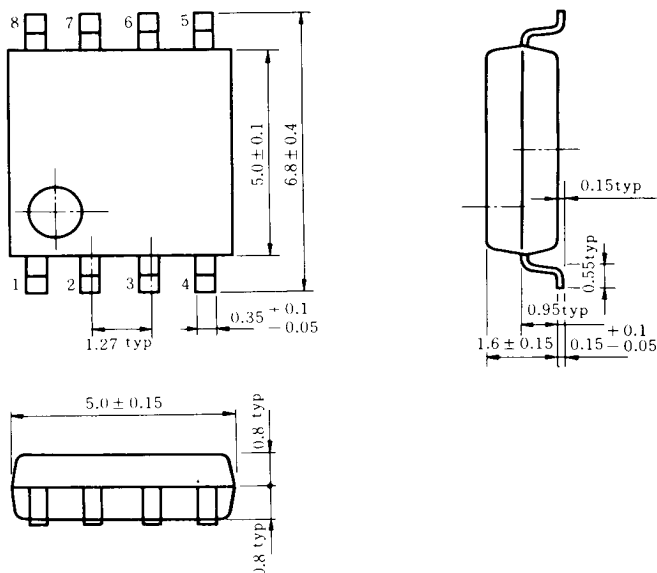
Initially, all bits of RF5H01/RP5H01 are in the "1" state. Data is introduced by selectively programming "0" into the desired bit locations.

The program is operated by setting up $\overline{CE}/V_{PP} = V_{IH}$, and adding the reset pulse, and then applying the 50mS 21V program pulse. The data are verified by making $\overline{CE}/V_{PP} = V_{IL}$. The 2nd bit~the 64th bit are programmed by progressing the addresses in sequence by means of adding the data clock pulse.

● DUMMY BITS

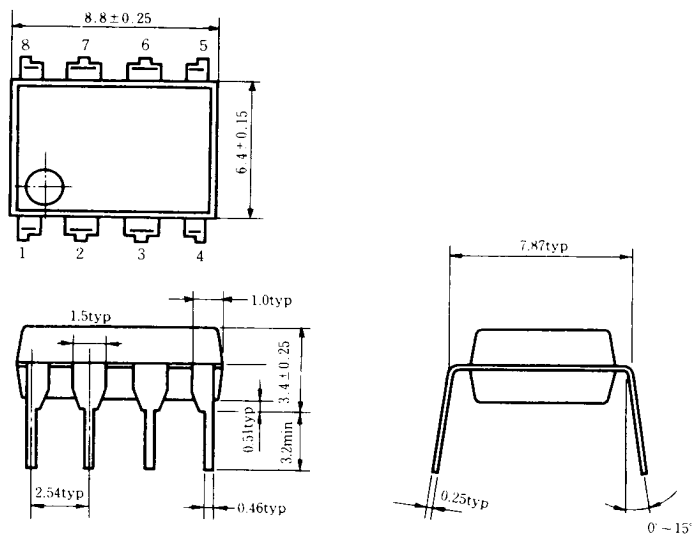
RF5H01/RP5H01 is a one-time PROM. For this reason, it is provided with a dummy bit of 8 bits for test programming. The dummy bit is located after the practical use 64th bit. The address is 8 bits of 1000000~1000111. The built-in counter operates as a 7-bit counter when "Test" (5 pins) is set at V_{CC} level, enabling to select the dummy bit. In the case of the "Test" being GND level, the counter operates as the 6-bit counter, being unable to select the dummy bit. In the 7-bit counter, when the clock pulse is added in sequence, the address progresses from 0000000 to 1111111, and then returns to 0000000.

■ 8-PIN PLASTIC FLAT PACKAGE (EXTERNAL VIEW) (UNIT : mm)



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■ 8-PIN PLASTIC DIL PACKAGE (EXTERNAL VIEW) (UNIT : mm)



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