Data Sheet
June 1995

AT&T Microelectronics

ATT22C498 16-Bit Interface RAMDAC *PrecisionDAC*™ Technology

Features

- Analog clock doubler
- 16-bit pixel port, usable as an 8-bit port
- 170/135/110 MHz speed grades:
  — 170 MHz 2:1 multiplex 8-bit pseudocolor
  — 73 MHz true-color operation
- 16M, 64K, 256 on-screen colors
- Eleven software-selectable color modes:
  — 24-bit true color, packed data format
  — 24-, 16-bit true color
  — 8-bit pseudocolor
- Pixel-by-pixel mode switching
- On-chip analog clock doubler (mode 2)
  — 85 MHz input, 170 MHz pixel output
  — 16 bit wide 2:1 multiplex
  — Selectable analog or digital doubler
- VGA-accessible control register
- Device and manufacturer ID registers
- Low power dissipation, 0.8 W @ 110 MHz typical
- *PrecisionDAC* technology and on-chip voltage reference provide typical DAC output current accuracy of ±3%
- On-chip output comparators for monitor detection
- ISO 9001 certified
- Programmable 8- or 6-bit DACs
- 256 x 24/18 color RAM
- 44-pin PLCC package

Applications

- True-color desktop motherboards
- True-color add-in card
- Screen resolutions:
  — 1600 x 1280, 8 bits per pixel, 60 Hz
  — 1280 x 1024, 16 bits per pixel, 60 Hz
  — 1024 x 768, 24 bits per pixel, 72 Hz
  — 800 x 600, 24 bits per pixel, 85 Hz

Application Differences
(From the ATT20C491/490)

The ATT22C498 is AT&T's third-generation device addressing the 16-bit pixel port market. The enhancement added to the ATT22C498 beyond the previous two generations is an analog clock doubler.

The ATT22C498 utilizes the low-cost 44-pin PLCC package common to other RAMDACs. The signal footprint of 490/491/492/493 44-pin RAMDACs has been updated to support the additional eight pixel inputs as well as provide better noise immunity. Pins 2, 5, 19, 20, 21, 30, and 41—44 have been changed. This includes the true control pin, SYNC function, and overlays that were offered in previous 44-pin RAMDACs, but have been eliminated in the ATT22C498 to reduce power consumption and provide eight additional pixel pins.

Description

The ATT22C498 CMOS RAMDAC supports 24- and 16-bit true-color bypass along with 8-bit pseudocolor applications. A 16-bit pixel bus interface allows higher color resolution at higher screen resolution in a 44-pin PLCC. The ATT22C498 provides the next level of performance over the ATT20C490/491/492/493 RAMDACs.

The ATT22C498 formats and displays data at up to 220 Mbytes/s, making it an ideal device for display systems with 2 Mbyte frame buffers.

Software can uniquely identify each of AT&T's 49X family of devices. Easy identification of the RAMDAC allows the video BIOS to determine if a requested mode is available on the hardware being used.

Table of Contents

Contents

Page

Description (continued)

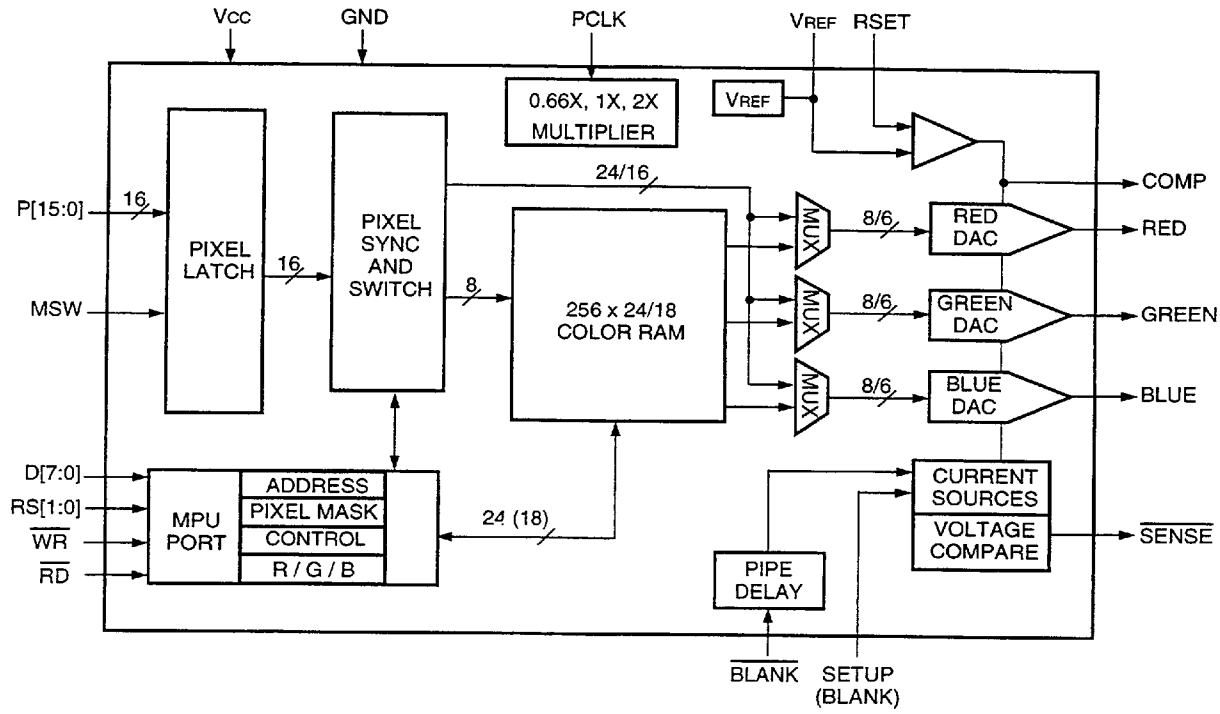


Figure 1. Block Diagram

Pin Information

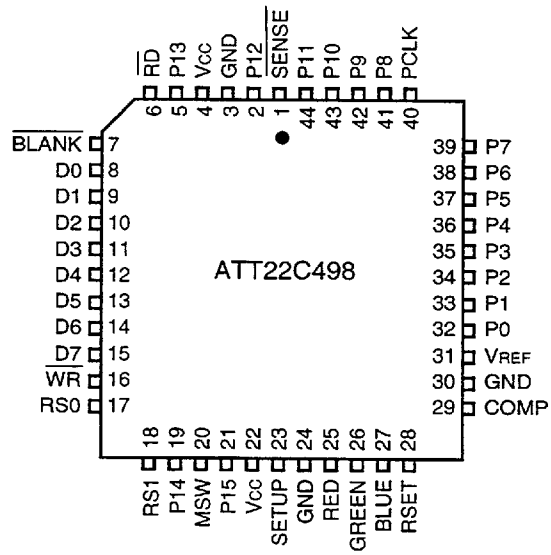


Figure 2. 44-Pin PLCC Diagram (Top View)

Pin Information (continued)

Table 1. Pin Descriptions

ATT22C498 Pin #	Symbol	Type	Name/Function
1	$\overline{\text{SENSE}}$	O	**$\overline{\text{SENSE}}$ (Active-Low).** TTL compatible. Monitor detection signal. $\overline{\text{SENSE}}$ is a logic 0 if one or more of the red, green, or blue outputs have exceeded an internal voltage level.
2, 5, 19, 21, 32—39, 41—44	P[15:0]	I	**Pixel Inputs.** TTL compatible. These pins are latched on the rising edge of PCLK. Pixels are presented to the DACs as color data in true-color modes and are used as addresses in pseudocolor mode to look-up color data in the color RAM. Unused inputs should be connected to GND.
3, 24, 30	GND	—	**Ground.** Connect these pins to circuit ground.
4, 22	Vcc	—	**Power.** Connect these pins to +5 V.
6	$\overline{\text{RD}}$	I	**Read (Active-Low).** TTL compatible. When $\overline{\text{RD}}$ is low, data transfers from the selected internal register to the data bus. RS[1:0] are latched on the falling edge of $\overline{\text{RD}}$.
7	$\overline{\text{BLANK}}$	I	**$\overline{\text{BLANK}}$ (Active-Low).** TTL compatible. $\overline{\text{BLANK}}$ is latched on the rising edge of PCLK. When $\overline{\text{BLANK}}$ is low, the 1.44 mA current source on the analog outputs will be turned off. The DACs are turned off. The RAMDAC and overlay memory can be updated during blanking.
8—15	D[7:0]	I/O	**Data Bus.** TTL compatible. Data is transferred between the data bus and the internal registers under control of the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signals. In an MPU write operation, D[7:0] is latched on the rising edge of $\overline{\text{WR}}$. To read data D[7:0] from the device, $\overline{\text{RD}}$ must be active. The rising edge of the $\overline{\text{RD}}$ signal indicates the end of a read cycle. Following the read cycle, the data bus will go to a high-impedance state. **Note:** For 6-bit operation, color data is contained in the lower 6 bits of the data bus. D0 is the LSB, and D5 is the MSB. When the MPU writes color data, D6 and D7 are ignored. During MPU read cycles, D6 and D7 are a logic 0.
16	$\overline{\text{WR}}$	I	**Write (Active-Low).** TTL compatible. $\overline{\text{WR}}$ controls the data transfer from the data bus to the selected internal register. D[7:0] data is latched at the rising edge of $\overline{\text{WR}}$, and RS[1:0] data is latched at the falling edge of $\overline{\text{WR}}$.
17, 18	RS[1:0]	I	**Register Select.** TTL compatible. These inputs are sampled on the falling edge of the $\overline{\text{RD}}$ or $\overline{\text{WR}}$ to determine which one of the internal registers is to be accessed. See the Control Register 0 (CR0) section under Register Descriptions.
20	MSW	I	**Mode Switch.** This input changes the RAMDAC mode. The RAMDAC interprets the incoming data on a pixel-by-pixel basis based on the mode. Ground this pin if not used.
23	SETUP	I	**Pedestal Setup.** TTL compatible. A logic high will cause a blanking pedestal of 1.44 mA on an RS-343A output.
25 26 27	RED GREEN BLUE	O	**Color Signals.** These pins are analog outputs. These high-impedance current sources are capable of driving a double-terminated 75 Ω coaxial cable.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

ATT22C498 Pin #	Symbol	Type	Name/Function
28	RSET	I	**Reference Resistor.** An external resistor (RSET) is connected between the RSET pin and GND to control the magnitude of the full-scale current. Refer to DAC Gain section under Functional Description.
29	COMP	—	**Compensation Pin.** Bypass this pin with an external 0.1 µF capacitor to Vcc.
31	VREF	I	**Voltage Reference.** If an external voltage is used, this is the input. This node is disabled internally during powerdown.
40	PCLK	I	**Pixel Clock.** TTL compatible. The rising edge of the pixel clock latches the pixel address and BLANK and SYNC inputs.

Register Descriptions

Internal Register Set

Table 2. Standard Registers

RS1	RS0	Register Name	Addressed by MPU
0	0	WMA	Address register; look-up table write mode
0	1	LUT	Look-up table register; sends data to pixel color RAM
1	0	RMR	Pixel read mask register
1	1	RMA	Address register; look-up table read mode

Table 3. Indirect Registers

RS1	RS0	Register Name	Addressed by MPU
1	0	CR0	Control register 0
1	0	MIR	Manufacturer's identification register
1	0	DIR	Device identification register
1	0	RTEST	Red signature analysis register
1	0	GTEST	Green signature analysis register
1	0	BTEST	Blue signature analysis register

Note: Indirect registers CR0, MIR, DIR, RTEST, GTEST, and BTEST are accessed by multiple reads of the RMR (see Figure 3).

Tables 2 and 3 list the internal register set of the ATT22C498. This device is designed to support enhanced features in a VGA compatible architecture. A typical VGA system only supports RS0 and RS1 register select signals. With only two register select lines, access to four registers is provided. In order to provide enhanced features, additional register locations are required and need to be accessible in the VGA register space.

To provide the additional registers, an indirect access method has been added. This method provides access to a control register (CR0), a manufacturer's identification register (MIR), a device identification register (DIR), and test registers.

Register Descriptions (continued)

Look-Up Table (LUT) Write Mode Address Register (WMA)

The LUT write mode address register holds an 8-bit value that is used as an index when writing into the LUT data register. This register points to one of the 256 LUT locations. Each of the LUT locations is 24 bits wide (8 bits red, 8 bits green, and 8 bits blue). To write all 24 bits of a LUT location, three successive writes are made to the same address. After the sequence of three writes is completed, the 24-bit value is transferred to the LUT's RAM.

This register is only used while writing to the LUT. After this register is set to the desired index, MPU data can be written to the LUT data register. The WMA register is autoincrementing. When three writes to the LUT data registers are complete, the LUT data is written to the LUT and the WMA register increments by 1.

Table 4. Standard Register Set

The LUT and RMR registers apply only in pseudocolor modes.

Reg. Name	Reg. Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WMA	R/W	A7	A6	A5	A4	A3	A2	A1	A0
LUT	R/W	D7	D6	D5	D4	D3	D2	D1	D0
RMR	R/W	M7	M6	M5	M4	M3	M2	M1	M0
RMA	R/W	A7	A6	A5	A4	A3	A2	A1	A0

LUT Read Mode Address Register (RMA)

The LUT read mode address register holds an 8-bit value that is used as an index when reading from the LUT data register. To read all 24 bits of a LUT location, three successive reads are made to the same address.

Because this register is autoincrementing, when written to, the RMA reads the LUT into the LUT data register and then increments. When the three reads from the LUT data register are complete, the device transfers the new LUT data at the RMA address into the LUT data register and increments again.

LUT Data Register

The LUT data register is a data port through which reads and writes are made to the LUT. The LUT write mode address or read mode address registers are used to specify which LUT location is to be accessed. This register is an 8-bit port located in a 24-bit location. Three accesses are needed to read or write the LUT data register. Because both the LUT write mode address and LUT read mode address registers are autoincrementing, accesses to this port should be made three at a time to avoid leaving a partial read or write to the LUT data register. A partially written data register is not transferred to the LUT. The blue value must be written before the LUT is updated.

Pixel Read Mask Register (RMR)

The contents of the pixel read mask register (RMR) can be accessed by the MPU at any time and are not initialized on powerup. The RMR bits are logic ANDed with the 8-bit pixels in pseudocolor mode. In true-color modes, pixels are not modified by the RMR. A logic 1 stored in a data bit of the read mask register leaves the corresponding bit in the pixel unchanged. A logic 0 in the read mask register sets the pixel bit to 0. Bit D0 of the pixel read mask register corresponds to pixel bit P0.

Indirect Registers

The following six registers are indirectly accessed. See the Functional Description section.

Table 5. Accessing the RMR Enables Indirect Access of CR0, MIR, and DIR

RMR READ #	Register Name	Register Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
5	CR0	Read/Write	CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
6	MIR	Read Only	1	0	0	0	0	1	0	0
7	DIR	Read Only	1	0	0	1	1	0	0	0

Register Descriptions (continued)

Indirect Registers (continued)

Table 6. Accessing the RMR Enables Indirect Access to RTEST, GTEST, and BTEST

RMR READ #	Register Name	Register Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
8	RTEST	Read/Write	R7	R6	R5	R4	R3	R2	R1	R0
9	GTEST	Read	G7	G6	G5	G4	G3	G2	G1	G0
10	BTEST	Read	B7	B6	B5	B4	B3	B2	B1	B0

Control Register 0 (CR0)

The control register is written to or read by the MPU and is not initialized at powerup. Table 7 defines the bits of the control register. CR0 bits [7:4] determine the color mode as shown in Table 10.

Setting bit 3 to a 1 places the RAMDAC in powerdown mode. In the powerdown state, the device retains the information in the color look-up table. Access to the color look-up table is disabled during sleep. The internal registers can be written while the device is sleeping. The analog doubler is not affected by CR0[3]. The analog doubler is powered on in mode 2 and powered off in all other modes.

Table 7. Control Register 0

Bit	Name/Description
CR0[7:4]	**Color Mode.** These bits are used to control the color modes (see Table 10).
CR0[3]	**Powerdown.** Setting this bit to logic 1 powers the device down. In the powerdown mode, the device retains the information in the color look-up table. Access to the color look-up table is disabled during powerdown. The internal registers can be read/written while the device is powered down.
CR0[2]	**MSW Override and Mode 2 Doubler Type Select.** For all modes except mode 2 (CR0[7:4] = 0010), this bit controls on-the-fly format change. Logic 0: Enable MSW pin and C control bit. Logic 1: Disable MSW pin and C control bit. Setting this bit to logic 1 disables the MSW and C (mode 1) inputs and forces the data to be interpreted in the primary format for the given mode. For mode 2 (CR0[7:4] = 0010). This bit, in combination with CR0[2], defines the doubler operation (see CR0[0] and below for definition).
CR0[1]	**8/6-bit Select.** Logic 0: 6-bit data to the DAC. Logic 1: 8-bit data to the DAC. A logic 1 specifies 8 bits per DAC operation (16M possible colors). A logic 0 specifies 6 bits per DAC operation (256K possible colors).
CR0[0]	**Mode 2 Doubler Type Select.** This bit, in conjunction with CR0[2], defines the doubler operation in mode 2. When CR0[7:4] is not equal to 0010, this bit has no effect on the device operation (see below for programming options).

CR0[7:4]	CR0[3]	CR0[2]	CR0[1]	CR0[0]	Doubler Operation
0010*	X	0	X	0	Analog doubler with PCLK between 11.25 MHz and 22.5 MHz.
	X	0	X	1	Analog doubler with PCLK between 22.50 MHz and 45.0 MHz.
	X	1	X	0	Analog doubler with PCLK input above 45 MHz.
	0	1	X	1	Digital doubler.
	1	1	X	1	Digital doubler powered down.

* When CR0[7:4] is set to 0010 to select mode 2, the analog doubler will be powered on.

Register Descriptions (continued)

Manufacturer Identification Register (MIR)

This 8-bit register contains an 8-bit value to identify the manufacturer of the RAMDAC. The MIR is read by reading the RMR six times without accessing any other RAMDAC register. The first four reads will return the contents of the RMR; the fifth read will return the CR0 contents; the sixth read will return the MIR contents; and the seventh read will return the DIR contents. The ATT22C498 returns the value 84 hex on the sixth read.

Device Identification Register (DIR)

This 8-bit register contains an 8-bit value to identify the type of RAMDAC. The DIR is read by reading the RMR seven times without accessing any other RAMDAC register. The ATT22C498 returns the value 98 hex. To differentiate the ATT21C498 and the ATT22C498, and to determine if the analog doubler is present, we have added a simple test. Set the RAMDAC video mode to Ah (CR0[7:4] = Ah), and then read CR0. (Ah is not a valid video mode, it is only used for this test.) If the data returned from CR0 is 00h, the device is an ATT22C498. If the data returned from CR0 is what was written, AXh, the device is an ATT21C498.

Test Registers

The red, green, and blue test registers will analyze red, green, or blue signatures by using linear feedback shift registers (LFSRs). During signature analysis, the R, G, B data is sampled and compressed at the pixel clock frequency. The signature is accumulated based on the initial seed value. A new signature value is produced every pixel clock. When writing a seed value to the test register, the red, green, and blue test registers are all seeded with the same value.

Reading the RMR register eight, nine, and ten times will produce the red, green, and blue signatures. The first value read is the red signature, followed by the green and blue signatures. The test register may be read or written only during the blanking interval. During active video, the signatures are being accumulated. When $\overline{\text{BLANK}}$ is low, the signature analysis registers (SARs) are frozen. When $\overline{\text{BLANK}}$ rises, signatures accumulate to whatever value is in the SARs.

Functional Description

Accessing Indirect Registers

Access to the indirect registers is outlined in Table 9 and Figure 3. The indirect registers are CR0, MIR, DIR, RTEST, GTEST, and BTEST. To read CR0, read the RMR five times. The fifth read results in the contents of CR0. To write CR0, read the RMR four times. This sets an internal flag allowing access to control register 0. The next write will be directed to control register 0. The MIR, DIR, and test registers are accessed in a similar manner as shown in Figure 3. The sixth read of the RMR results in the MIR (read only). The seventh read of the RMR results in the DIR (read only). The eighth, ninth, and tenth reads of the RMR result in the red, green, and blue signature analysis registers. Any I/O operation, except an RMR read, will reset the state machine to state 0. (See Table 8.)

Table 8. I/O Operations that Reset the State Machine to State 0

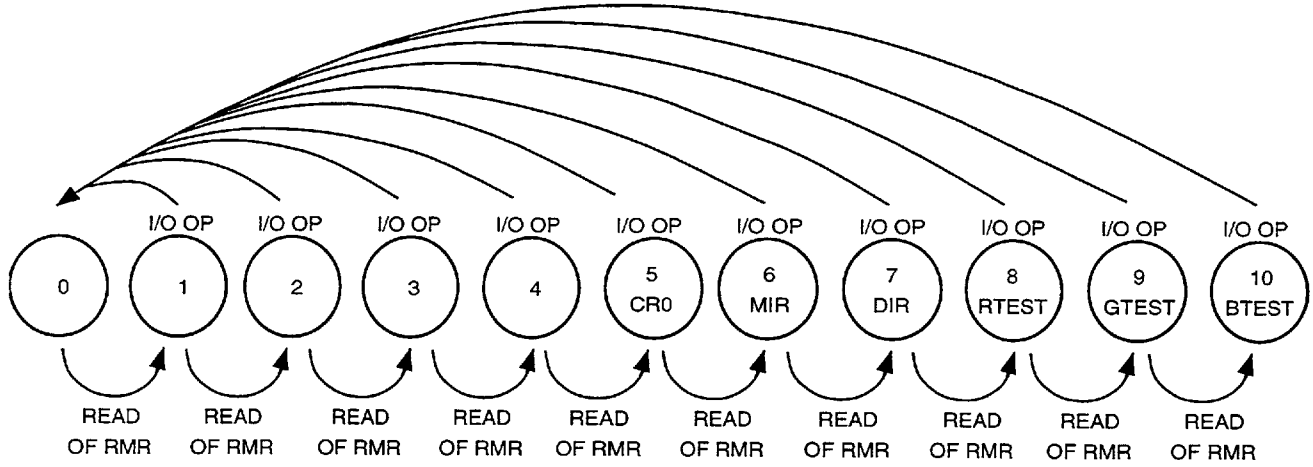
$\overline{\text{RD}}$	$\overline{\text{WR}}$	RS1	RS0
√	√	0	0
√	√	0	1
—	√	1	0
√	√	1	1

Table 9. State Table Showing Access to CR0, MIR, DIR, and Test Registers

State	State Entry Conditions	State Activity
0	Any I/O write	Normal I/O access
1	Read of RMR while in state 0	Normal I/O access
2	Read of RMR while in state 1	Normal I/O access
3	Read of RMR while in state 2	Normal I/O access
4	Read of RMR while in state 3	Normal I/O access
5	Read or write of RMR while in state 4	I/O access to CR0
6	Read of RMR while in state 5	Returns manufacturer identification, 84 hex
7	Read of RMR while in state 6	Returns device identification number, 98 hex
8	Read of RMR while in state 7	Returns RTEST signature analysis register
9	Read of RMR while in state 8	Returns GTEST signature analysis register
10	Read of RMR while in state 9	Returns BTEST signature analysis register

Functional Description (continued)

Accessing Indirect Registers (continued)



Note: I/O OP is any write to 3C6, 3C7, 3C8, or 3C9.

Figure 3. State Diagram Illustrating Access to Indirect Registers

Color Modes

The ATT22C498 provides eleven different color modes that are selectable by programming the MPU control register bits CR0[7:4] (see Table 10). Most modes have a primary and a secondary display mode. The choice of the two modes is controlled by the mode switch input (MSW) or the control bit in mode 1. When the MSW pin is logic 0, the RAMDAC interprets the incoming pixel data to be the primary mode format. When the MSW pin is logic 1, the RAMDAC interprets the incoming pixel data to be the secondary or alternate mode format (see Figures 4—7).

In true-color modes with multiple clocks per pixel, a counter will provide the internal load pulse that latches the data into a 16- or 24-bit pixel. An active $\overline{\text{BLANK}}$ low signal clears the counter. True-color modes bypass the look-up table and are not gamma corrected. $\overline{\text{BLANK}}$ going high will signal that the first pixel information is available on P[15:0].

Mode 0

Primary mode is 8-bit pseudo; secondary mode is mode 3 (see Figure 4). This mode displays data formatted in 8-bit pseudocolor. The primary or secondary mode operation is determined by the mode switch input. Mode 0 is selected by setting control register CR0 bits [7:4] to 0000. In both data formats, the P[15:0] inputs are latched on the rising edge of the pixel clock. Mode 0 ignores the P[15:8] inputs.

Mode 1

Primary mode is 15-bit true color; secondary mode is mode 0 (see Figure 5). This mode displays data formatted for 15-bit per pixel true color (5-5-5). The mode switch is determined by the C bit (P15), not by the MSW pin. The MSW input has no effect on mode 1 and can be either high or low. When C = 0, the pixel data is interpreted as 15-bit true color. When C = 1, the pixel data is interpreted as mode 0, 8-bit pseudo-color. This mode is selected by setting control register CR0 bits [7:4] to 0001.

Mode 2

Primary mode is 8-bit pseudocolor with 2:1 multi-plexing using an internal analog clock doubler (there is no secondary mode for mode 2). This mode accepts two 8-bit pseudocolor pixels on each clock. The MSW input has no effect on mode 2 and may be either high or low. This mode is selected by setting control register CR0 bits [7:4] to 0010. The internal clock doubler outputs the pixels at twice the PCLK frequency. This allows the RAMDAC to output 8-bit pseudocolor pixels at 135 MHz with 67.5 MHz data rates. This mode reduces EMI problems when displaying 1280 x 1024 resolutions. Control register 0, bit 0 must be selected for this mode.

Functional Description (continued)

Color Modes (continued)

Mode 3

Primary mode is 16-bit true color; secondary mode is mode 0. This mode formats data in either 16-bit per pixel true color or 8-bit per pixel pseudocolor. The primary or secondary mode operation is determined by the mode switch input. This mode is selected by setting control register CR1 bits [7:4] to 0011.

Mode 4

Primary mode is 8-bit pseudocolor; secondary mode is mode 5. This mode accepts data formatted as 8-bit pseudocolor latched 4-bits at a time. Latching one pixel's worth of data during two pixel clocks allows mode switching to 24-bit true color (mode 5) without changing pixel clock frequencies (see Figure 6). The primary or secondary mode operation is determined by the mode switch input. This mode is selected by setting control register CR0 bits [7:4] to 0100.

Mode 5

Primary mode is 24-bit true color; secondary mode is mode 6. This mode accepts a 24-bit pixel formatted as two 16-bit words latched by two pixel clocks. The primary or secondary mode operation is determined by the mode switch input. This mode is selected by setting control register CR0 bits [7:4] to 0101.

Mode 6

Primary mode is 16-bit true color (5-6-5); secondary mode is mode 5. The 16-bit pixel is latched in 2 bytes with two PCLKs. Latching 1 byte per clock allows mode switching to 24-bit true color (mode 5) without changing pixel clock frequencies (see Figure 7). The primary or secondary mode operation is determined by the mode switch input. This mode is selected by setting control register CR0 bits [7:4] to 0110. BLANK going high will signal that the first pixel information is available on P[15:0]. The rising edge of PCLK that captures BLANK going high also captures the LSBs of the pixel information. The LSBs are latched first, followed by the MSBs. The LSBs and MSBs follow in succession until BLANK goes low. The LSBs of the DACs are set to logic 0.

Mode 7

Primary mode is 24-bit true color (8-8-8); there is no secondary mode. The 24-bit pixel is latched in 3 bytes with three PCLKs. The MSW input has no effect on mode 7 and may be either high or low. This mode is selected by setting the control register CR0 bits [7:5] to 0111. The pixel information is collected over three rising edges of the pixel clock. BLANK going high will signal that the first pixel information is available on P[15:0]. The rising edge of PCLK that captures BLANK going high also captures the blue information of the first pixel. The blue pixel is latched first followed by the green and red. Blue, green, and red follow in succession until BLANK goes low.

Mode 8

Primary mode is 8-bit pseudocolor; secondary mode is mode 6. This mode accepts data formatted as 8-bit pseudocolor latched by two pixel clocks as 4-bit nibbles. Latching two nibbles allows mode switching to 16-bit true color (mode 6) without changing pixel clock frequencies. The primary or secondary mode operation is determined by the mode switch input. This mode is selected by setting control register CR0 bits [7:4] to 1000.

Mode 9

Primary mode is 8-bit pseudocolor; secondary mode is mode 5. Provides one 8-bit pseudocolor pixel per two clock cycles. Eight bits are taken from the eight LSBs of the pixel port on the first cycle. The second cycle is used as a dummy cycle for timing purposes. Latching the 16-bit pixel inputs twice allows mode switching to 24-bit true color (mode 5) without changing pixel clock frequency. The primary or secondary mode operation is determined by the mode switch input. Mode 9 is selected by setting control register CR0 bits [7:4] to 1001. In both data formats, the P[15:0] inputs are latched on the rising edge of the pixel clock. Mode 9 ignores the P[15:8] inputs.

Modes 10—13

Modes 10—13 are reserved. Setting CR0[7:4] with these values may cause the RAMDAC to malfunction. These values are reserved.

Mode 14

Mode 14 is a packed 24-bit mode that displays two 24-bit pixels for every three PCLKs. The output pixel rate will be two-thirds the PCLK rate.

Mode 15

Mode 15 is reserved. Setting CR0[7:4] to 0$F may cause the RAMDAC to malfunction.

Functional Description (continued)

Color Modes (continued)

Table 10. Color Modes

The following table details the eleven display formatting modes of the ATT22C498. These modes are set by bits CR[7:4] of the control register. Pixel data inputs are only latched on the rising edge of PCLK.

Primary Mode #*	Sec. Mode #†	CR0 [7:4]	Primary Mode Description	PCLK	Pixel Data Input 0—7 (0 1 2 3 4 5 6 7)	Pixel Data Input 8—15 (8 9 10 11 12 13 14 15)
0	3	0000	8-bit	↑	P0 P1 P2 P3 P4 P5 P6 P7	X X X X X X X X
1	NA	0001	15-bit + C CR0[2] = 1 CR0[2] = 0 CR0[2] = 0	↑	 B3 B4 B5 B6 B7 G3 G4 G5 B3 B4 B5 B6 B7 G3 G4 G5 P0 P1 P2 P3 P4 P5 P6 P7	 G6 G7 R3 R4 R5 R6 R7 **C = X** G6 G7 R3 R4 R5 R6 R7 **C = 0** X X X X X X X **C = 1**
2	NA	0010	8-bit 2 pixels	↑	P0 P1 P2 P3 P4 P5 P6 P7	P0 P1 P2 P3 P4 P5 P6 P7
3	0	0011	16-bit 5/6/5	↑	B3 B4 B5 B6 B7 G2 G3 G4	G5 G6 G7 R3 R4 R5 R6 R7
4	5	0100	8-bit 2 clocks	↑ ↑	P0 P1 P2 P3 X X X X P4 P5 P6 P7 X X X X	X X X X X X X X X X X X X X X X
5	6	0101	24-bit 2 clocks	↑ ↑	B0 B1 B2 B3 B4 B5 B6 B7 R0 R1 R2 R3 R4 R5 R6 R7	G0 G1 G2 G3 G4 G5 G6 G7 X X X X X X X X
6	5	0110	16-bit 5/6/5 2 clocks	↑ ↑	B3 B4 B5 B6 B7 G2 G3 G4 G5 G6 G7 R3 R4 R5 R6 R7	X X X X X X X X X X X X X X X X
7	NA	0111	24-bit 3 clocks	↑ ↑ ↑	B0 B1 B2 B3 B4 B5 B6 B7 G0 G1 G2 G3 G4 G5 G6 G7 R0 R1 R2 R3 R4 R5 R6 R7	X X X X X X X X X X X X X X X X X X X X X X X X
8	6	1000	8-bit 2 clocks	↑ ↑	P0 P1 P2 P3 X X X X P4 P5 P6 P7 X X X X	X X X X X X X X X X X X X X X X
9	5	1001	8-bit 2 clocks	↑ ↑	P0 P1 P2 P3 P4 P5 P6 P7 X X X X X X X X	X X X X X X X X X X X X X X X X
10—13	—	—	—	—	reserved	reserved
14	NA	1110	24-bit True-Color (Packed)	↑ ↑ ↑	B0 B1 B2 B3 B4 B5 B6 B7 R0 R1 R2 R3 R4 R5 R6 R7 G0 G1 G2 G3 G4 G5 G6 G7	G0 G1 G2 G3 G4 G5 G6 G7 B0 B1 B2 B3 B4 B5 B6 B7 R0 R1 R2 R3 R4 R5 R6 R7
15	—	—	—	—	reserved	reserved

* For primary mode, MSW = 0 or CR0[2] = 1.
† For secondary mode, MSW = 1 and CR0[2] = 0.

Note: MSW override will also cause the C field to be ignored and pixels to be interpreted in the primary mode.

Functional Description (continued)

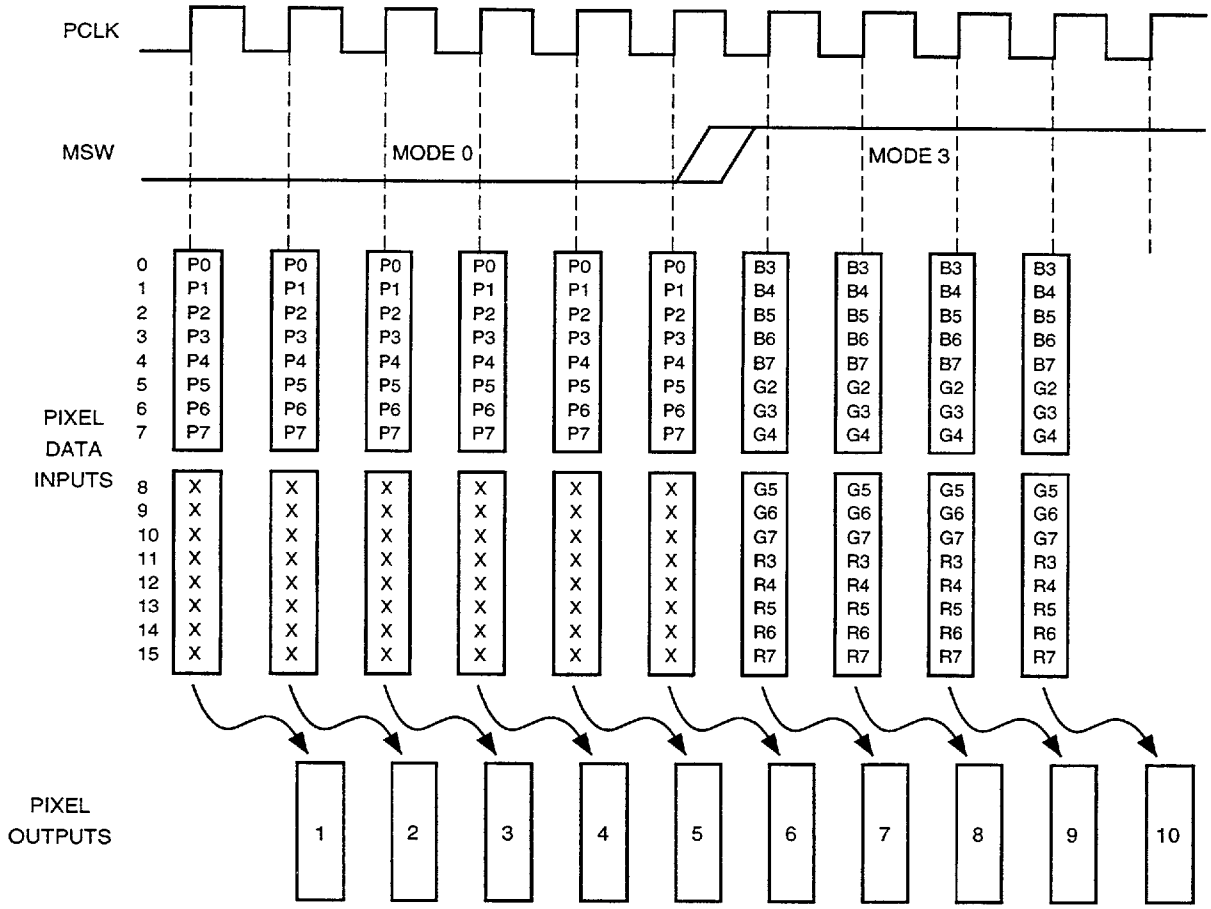
Color Modes (continued)

Table 11. Color Mode Speed

	170 MHz Max		135 MHz Max		110 MHz Max		
Primary Mode #	Max PCLK	Pixel Rate (MHz)	Max PCLK	Pixel Rate (MHz)	Max PCLK	Pixel Rate (MHz)	Pipeline (CLKS)
0	110	110	110	110	80	80	6
1	110	110	110	110	80	80	6
2	85	170	67.5	135	55	110	6
3	110	110	110	110	80	80	6
4	110	55	110	55	80	40	7
5	110	55	110	55	80	40	7
6	110	55	110	55	80	40	7
7	110	36	110	36	80	26	8
8	110	55	110	55	80	40	7
9	110	55	110	55	80	40	7
10—13	—	—	—	—	—	—	—
14	110	73	110	73	80	53	NA
15	—	—	—	—	—	—	—

Functional Description (continued)

Color Modes (continued)



Note: Pipeline delay not shown for clarity.

Figure 4. On-the-Fly Mode Switch from 8 Bits Per Pixel to 16 Bits Per Pixel (Mode 0 Changing to Mode 3)

Functional Description (continued)

Color Modes (continued)

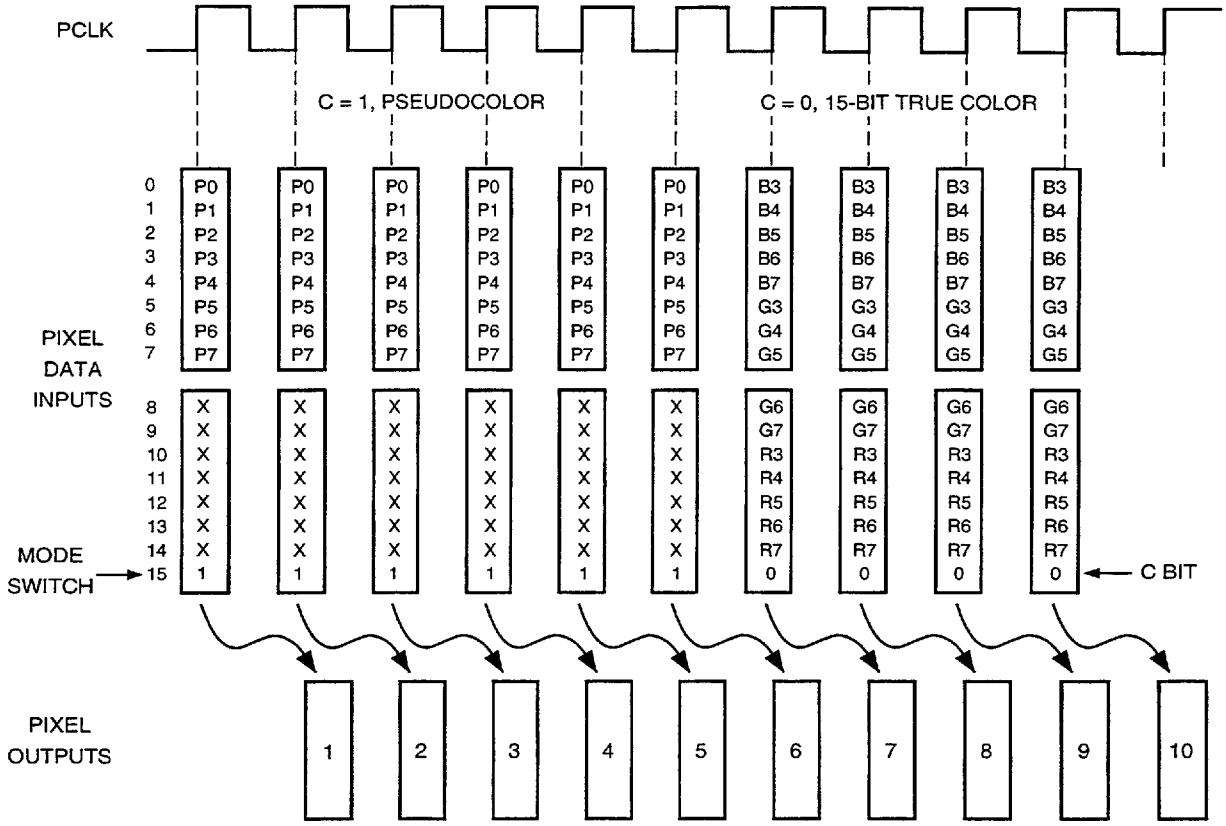
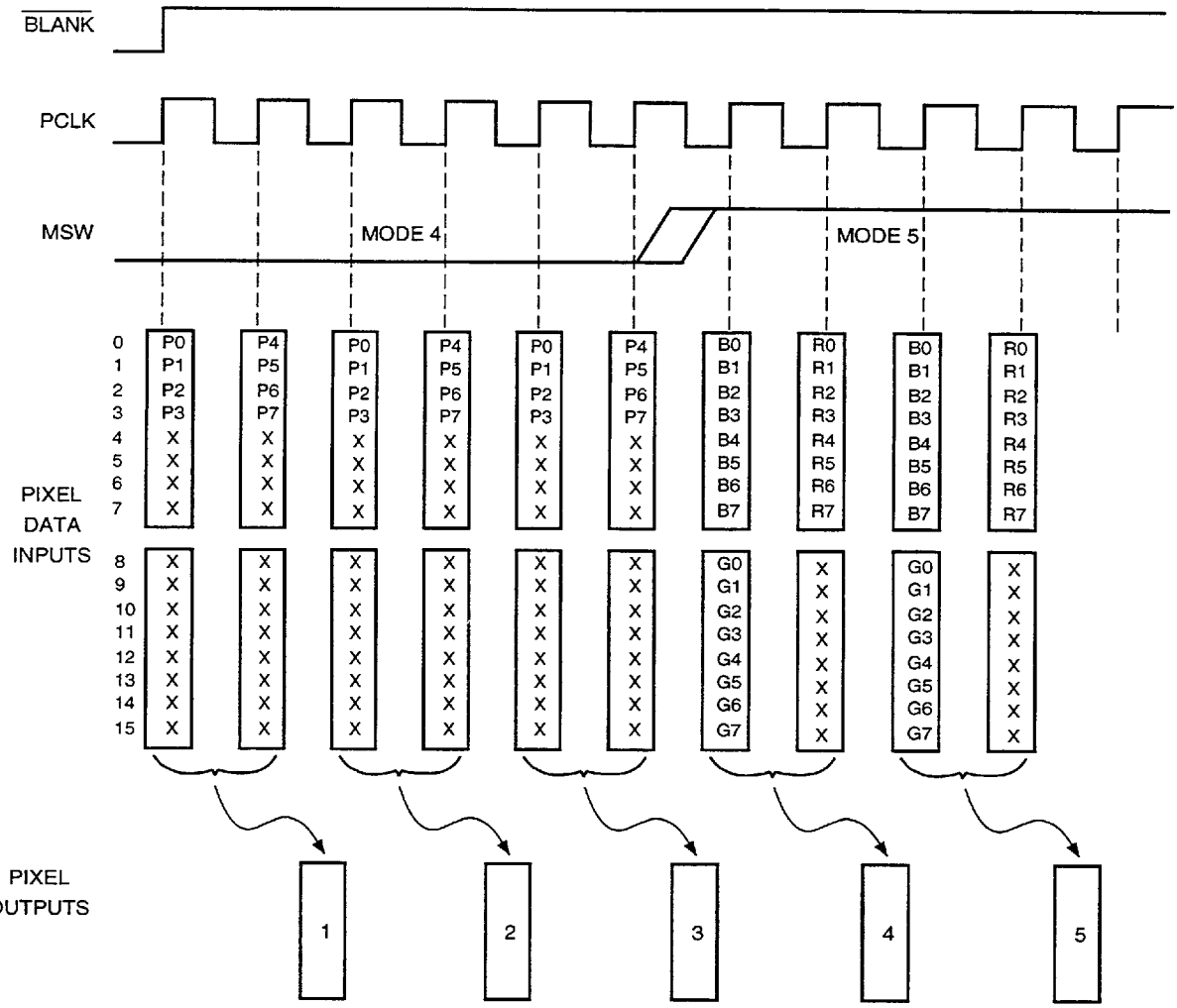


Figure 5. On-the-Fly Mode Switch from 8 Bits Per Pixel to 15 Bits Per Pixel (Mode 1, C = 1 Changing to C = 0)

Functional Description (continued)

Color Modes (continued)

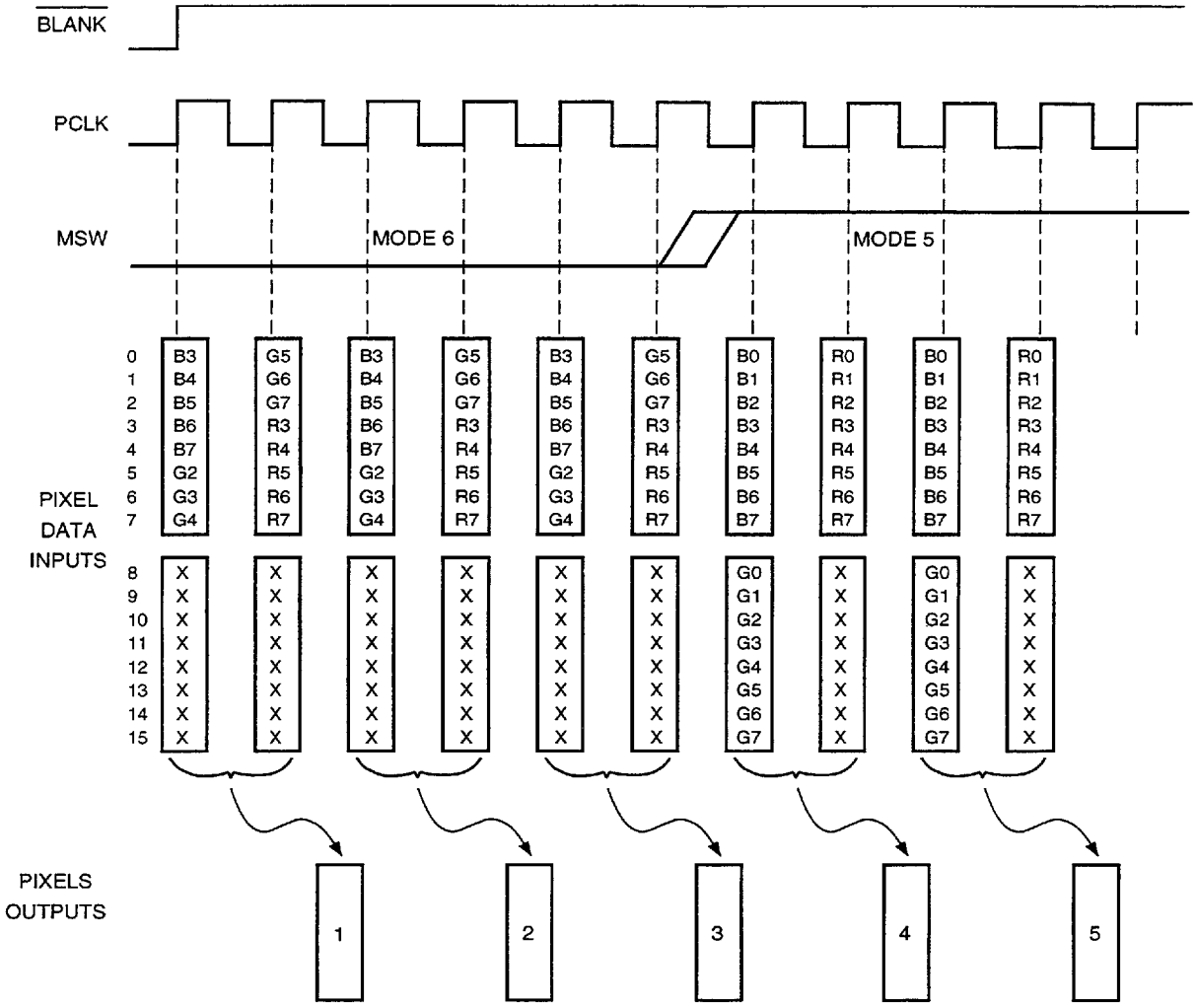


Note: Pipeline delay not shown for clarity.

Figure 6. On-the-Fly Mode Switch from 8 Bits Per Pixel to 24 Bits Per Pixel (Mode 4 Changing to Mode 5)

Functional Description (continued)

Color Modes (continued)



Note: Pipeline delay not shown for clarity.

Figure 7. On-the-Fly Mode Switch from 16 Bits Per Pixel to 24 Bits Per Pixel (Mode 6 Changing to Mode 5)

Functional Description (continued)

MPU Interface

The ATT22C498 supports a standard MPU interface, allowing the MPU direct access to the WMA, RAMDAC color RAM, RMR, or RMA. As outlined in Tables 2 and 3, the RS[1:0] select inputs indicate whether the MPU is accessing the address register WMA, RAMDAC color RAM, RMR, or RMA. To eliminate the requirement for external address multiplexers, the 8-bit address register is used to address the RAMDAC RAM. WMA[0] and RMA[0] corresponds to D0 and is the least significant bit.

Writing the RAMDAC

The MPU writes the address register (WMA) with the address of the RAMDAC color RAM location to be modified. Using RS[1:0] to select the RAMDAC color RAM (LUT), the MPU completes three continuous write cycles (6 or 8 bits each of red, green, and blue). Following the blue write cycle, the 3 bytes of color information are concatenated into an 18- or 24-bit word and written to the location specified by the address register. The address register advances to the next location which the MPU can modify by simply writing another sequence of red, green, and blue data. A block of color values in successive locations can be written to by writing the start address and performing continuous R, G, and B write cycles until the entire block has been written.

Reading the RAMDAC

The MPU loads the address register (RMA) with the address of the RAMDAC color RAM location to be read. The contents of the RAMDAC color RAM at the specified address are copied into the RGB register, and the address register advances to the next RAM location. Using RS[1:0] to select the RAMDAC color RAM (LUT), the MPU completes three continuous read cycles (6 or 8 bits each of red, green, and blue). After the blue read cycle, the contents of the RAMDAC color RAM at the address specified by the address register are copied into the RGB registers, and the address register advances to the next address. A block of color values in successive locations can be read by writing the start address and performing continuous R, G, and B read cycles until the entire block has been read.

Additional Information

Following a blue read or write cycle to color RAM location 0xFF, the address register resets to 0x00.

Operation of the MPU interface occurs asynchronously to the pixel clock. Internal logic synchronizes data transfers between the RAMDAC color RAM and the R, G, B color subregister. The transfers occur between MPU accesses. As a result, the $\overline{WR}$ and $\overline{RD}$ signals must maintain a logic high for several clock cycles. See Table 20 ac Characteristics $\overline{RD}$ and $\overline{WR}$ high times for further information. To eliminate sparkling on the CRT screen during MPU access to the RAMDAC RAMs, internal logic maintains the previous output color data on the analog outputs while the transfer between look-up table RAMs and the RGB registers occurs.

To monitor the red, green, and blue read/write cycles, the address register has two additional bits (ADa, ADb) that count modulo three, as shown in Table 12. They are reset to 0 when the MPU writes to the address register (WMA or RMA), and they are not reset to 0 when the MPU reads the address register. The MPU does not have access to these bits.

The WMA and RMA address registers increment following a blue read or write cycle, and they are accessible to the MPU and are used to address RAMDAC RAM locations (LUT). The MPU can read the address register at any time without modifying its contents or the existing read/write mode. Note that the pixel clock must be active for MPU accesses to the RAMDAC RAM (LUT).

Table 12. Modulo Counter Operation

AD[b:a]	Addressed by MPU
00	Red color RAM byte
01	Green color RAM byte
10	Blue color RAM byte

Functional Description (continued)

8-/6-Bit Color Resolution

The 8-/6-bit in the control register (CR0[1]) determines whether the MPU port reads and writes 8 bits or 6 bits of color data to the color look-up table RAM. In 6-bit mode, color data is on the lower 6 bits of the data bus, with D0 being the LSB and D5, the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be logic 0. Note that in the 6-bit mode, the full-scale output current will be about 1.5% lower than when in the 8-bit mode. This is a result of the two LSBs of each 8-bit DAC always being a logic 0 in the 6-bit mode. In the 8-bit color mode, bit D0 is the color data LSB and bit D7 is the MSB.

Powerdown

CR0[3] controls the powerdown. The device operates normally while the bit is a logic 0. A logic 1 will turn off power to the RAM and the DACs. The RAM still retains the data but cannot be read or written while powered down. The internal registers can be written or read while the RAMDAC is asleep. The power on/off state of the analog clock doubler is not changed by CR0[3]. To power off the analog doubler, program the mode to something other than mode 2.

$\overline{\text{SENSE}}$ Output

$\overline{\text{SENSE}}$ is a logic 0 if one or more of the red, green, or blue outputs have exceeded the internal voltage reference level of 340 mV (see Figure 8). This output is used to determine the presence of a CRT monitor, and via diagnostic code, the difference between a loaded or unloaded RGB line can be discerned. The 340 mV reference has a ±70 mV tolerance.

DAC Gain

The device gain from the voltage reference to the DAC output current is shown below. To set the full-scale white current on the DACs while using an internal or external voltage reference, use the formula below.

V_{REF} is the voltage reference in volts, and K is the gain constant. RSET is the resistor connected between the RSET pin and ground.

I_{OUT} (mA) = [V_{REF} (V) * 1,000 * K] / RSET (Ω)

In this case, a voltage reference of 1.235 V with RSET = 147 Ω and a K factor of 3.17 results in I_{OUT} = 26.63 mA. A 6-bit DAC with no blank results in a K factor of 2.1 and I_{OUT} = 17.64 mA.

The recommended RSET for RS-343A compatibility applications (doubly terminated 75 Ω) is 147 Ω. The recommended RSET for *PS/2** applications (50 Ω) is 182 Ω.

* *PS/2* is a registered trademark of International Business Machines Corporation.

Table 13. Gain Factor (K) and I_{OUT} Current

BLANK	K (8-Bit)	K (6-Bit)
Yes	2.28	2.26
No	2.12	2.1

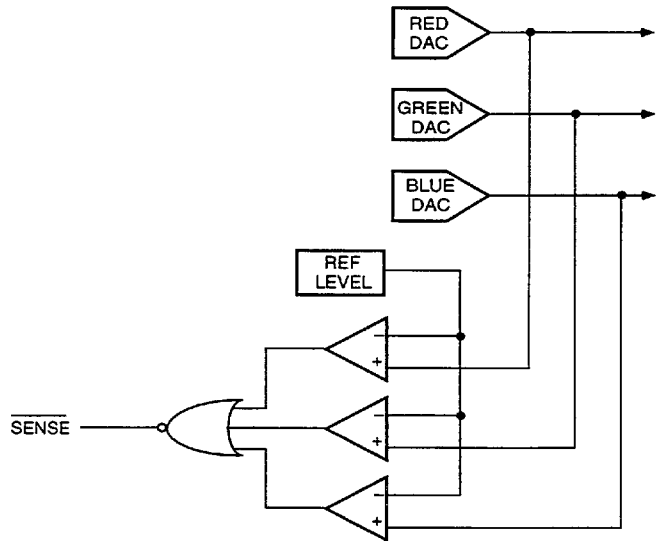


Figure 8. DAC Output Comparison Circuitry

Functional Description (continued)

DAC Gain (continued)

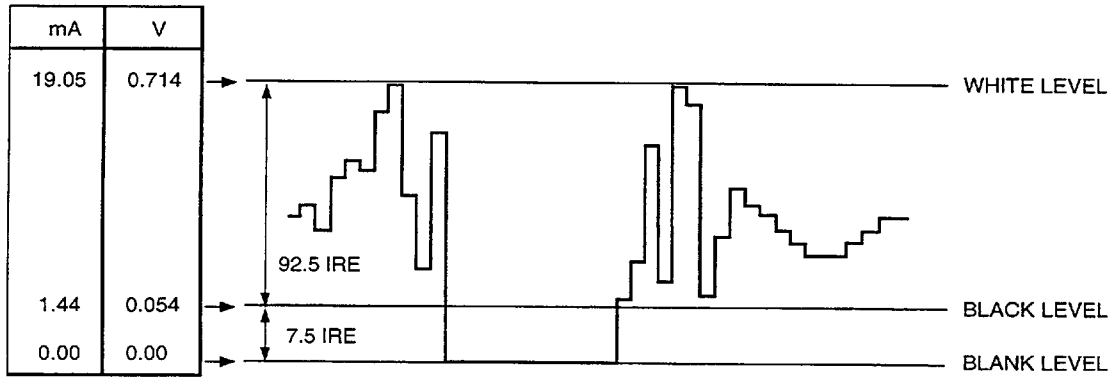


Figure 9. RS-343A Composite Video Output Waveforms

Table 14. RS-343A Video Output Truth Table (Blank Offset Current to Equal 7.5 IRE)

DAC Input Data	$\overline{\text{BLANK}}$	Output Level	I_{OUT} (mA)
$FF	1	WHITE	19.05
data	1	DATA	data + 1.44
$00	1	BLACK	1.44
$XX	0	$\overline{\text{BLANK}}$	0

Note: 75 Ω doubly terminated load, SETUP = 7.5 IRE. V_{REF} = internal, RSET = 147 Ω.

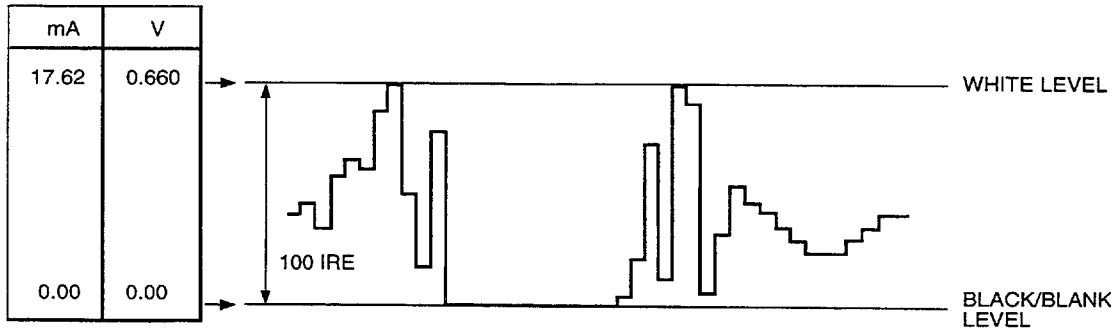


Figure 10. RS-343A Composite Video Output Waveforms (No Blank Pedestal)

Table 15. RS-343A Video Output Truth Table (No Blank Offset Current)

DAC Input Data	$\overline{\text{BLANK}}$	Output Level	I_{OUT} (mA)
$FF	1	WHITE	17.62
data	1	DATA	data
$00	1	BLACK	0
$XX	0	$\overline{\text{BLANK}}$	0

Note: 75 Ω doubly terminated load, SETUP = 0 IRE. V_{REF} = internal, RSET = 147 Ω.

Functional Description (continued)

DAC Gain (continued)

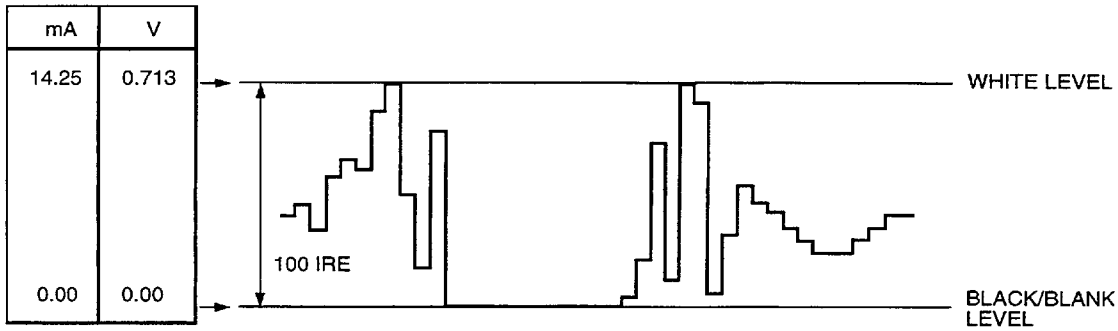


Figure 11. *PS/2* Composite Video Output Waveforms

Table 16. *PS/2* Video Output Truth Table (No Blank Offset Current)

DAC Input Data	$\overline{\text{BLANK}}$	Output Level	I_{OUT} (mA)
$FF	1	WHITE	14.25
data	1	DATA	data
$00	1	BLACK	0
$XX	0	$\overline{\text{BLANK}}$	0

Note: 75 Ω doubly terminated load, SETUP = 7.5 IRE. V_{REF} = internal, RSET = 182 Ω.

Application Information

Board Layout

Careful configuration and placement of supply planes, components, and signal traces ensure a low-noise board. This also helps ensure proper functionality and low signal emissions in restricted frequency bands as mandated by regulatory agencies.

A four-layer PC board with separate power and ground planes will likely result in a board with quieter signals and supplies.

The ATT22C498 should be placed close to the video output connector and between the video output connector and the edge card connector. This will keep the high-speed DAC output traces short and minimize the amount of circuitry between the RAMDAC and the supply pins on the edge card connector.

AT&T *PrecisionDAC* Technology

Now that AT&T is a major force in the RAMDAC market, we are taking the lead in defining the new level of product quality.

The voltage reference for a RAMDAC sets the output current level of the DACs. Originally, the voltage reference was an external component. The accuracy of this external component was important to ensure total system accuracy and, therefore, accurate output currents. Because RAMDACs now incorporate the voltage reference, the accuracy of the voltage reference is secondary in importance to the output current accuracy.

The brightness of a display is influenced by all of the errors that can affect the output current. Typically, they are the full-scale error, voltage reference error, RSET resistance error, and the Termination resistance error.

Calculation of the output current variations with traditional RAMDACs and voltage references is as follows:

1.00 Desired Current	x	±5% Full-scale Error (1.05)	x	±5% VREF Error (1.05)	x	±1% RSET Error (1.01)	x	±1% RTERM Error (1.01)	=	±12.4% Total Error (1.124)

Calculation using AT&T's RAMDACs with precision-trimmed output currents is as follows:

1.00 Desired Current	x	±3% Full-scale Error (1.03)	x	±1% RSET Error (1.01)	x	±1% RTERM Error (1.01)	=	±5.1% Total Error (1.051)

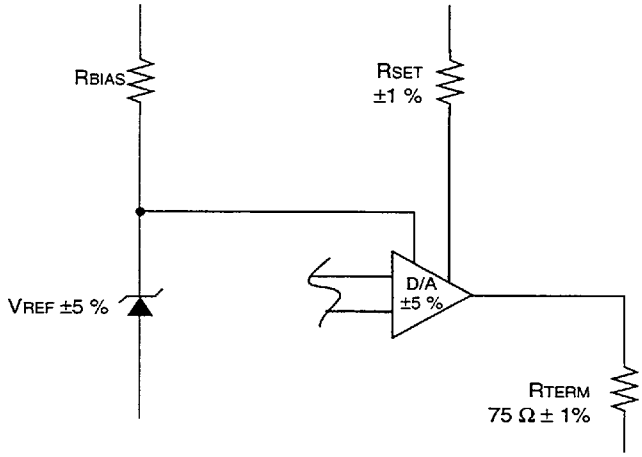


Figure 12. Traditional RAMDAC Output Current Variation

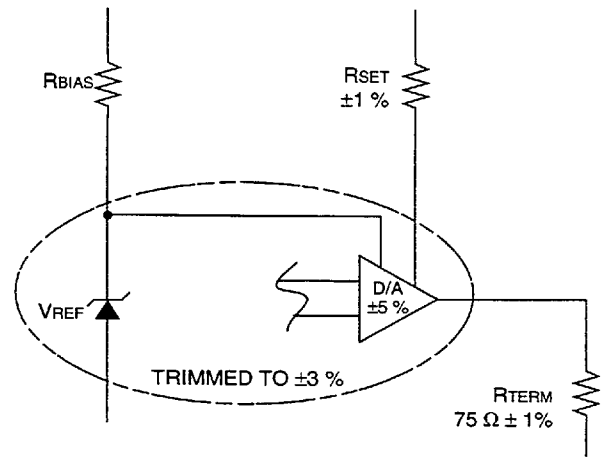


Figure 13. AT&T RAMDAC Output Current Variation

Application Information (continued)

Power Distribution

Separate the power plane into digital and analog areas. Place all digital components over the digital plane and all analog components over the analog plane. The analog components include the RAMDAC, reference circuitry, comparators, mixed-signal chips, and any passive support components for analog circuits.

The analog and digital power plane should be connected with at least one ferrite bead across the separation as illustrated in Figure 14. This bead provides resistance to high-frequency currents. Select a ferrite bead with an impedance curve suitable for your design. The power and ground traces or vias to the RAMDAC should be at least 50 mil wide. This is especially important on the ATT22C498 because the device has only two Vcc pins.

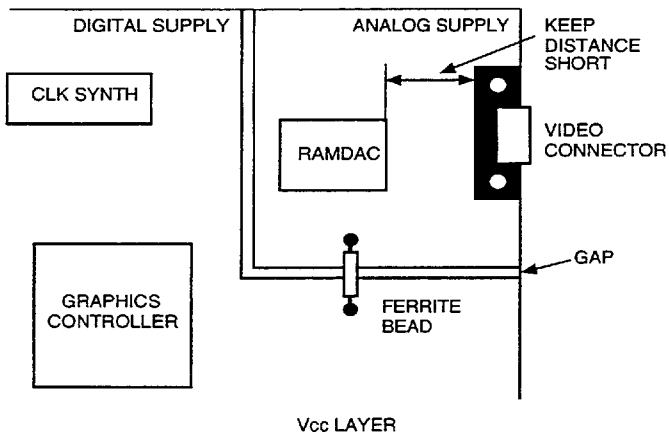


Figure 14. Digital and Analog Supply Plane Split

Decoupling Capacitors

All decoupling capacitors should be located within 0.25 in. of the device to be decoupled. Chip capacitors are recommended, but radial and axial leads will work. Keep lead lengths as short as possible to reduce inductance and EMI. For leaded capacitors, use devices with a self-resonance above the highest pixel clock frequency.

For the ATT22C498, decouple Vcc pin groupings to ground with a 0.1 µF capacitor. For higher-frequency pixel clocks (>110 MHz), use a 0.001 µF capacitor in parallel with the 0.1 µF capacitor to shunt the higher-frequency noise to ground. Power supply noise should be less than 200 mV for a good design. About 10% of any noise below 1 MHz will be coupled onto the DAC outputs. As illustrated in Figure 16, the COMP pin should also be decoupled with a 0.1 µF capacitor. For designs showing ghosting or smearing, add a parallel COMP capacitance of 2.2 µF.

Digital Signals

The digital inputs should not travel over the analog power plane if possible. The RAMDAC should be located over the analog plane close to the digital/analog supply separation. The RAMDAC may also be placed over the supply separation so the digital pixel inputs are over the digital supply plane. The digital inputs, especially the P[15:0] high-speed inputs, should be isolated from the analog outputs. Placing the digital inputs over the digital supply reduces coupling into the analog supply plane. High-speed signals (both analog and digital) should not be routed under the RAMDAC.

Avoid high slew rate edges since they can contribute to undershoot, overshoot, ringing, EMI, and noise feedthrough. Edges can be slowed down by using series termination (33 Ω to 150 Ω). Edge noise will result if the digital signal propagates from an impedance mismatch while the signal arises. The reflection noise is particularly troublesome in the TTL threshold region. For a 2 ns edge, the trace length must be less than 4 in.

The clock signal trace should be as short as possible and should not run parallel to any high-speed signals. To ensure a quality clock signal without high-frequency noise components, decouple the supply pins on the clock driver. If necessary, transmission line techniques should be used on the clock by providing controlled-impedance striplines and parallel termination. The 2x clock doubler in the ATT22C498 will help to reduce signal quality problems and EMI radiations by reducing the frequency of the clock signal to the device.

Application Information (continued)

Analog Signals

The load resistor should be as close as possible to the DAC outputs. The resistor should equal the destination termination which is usually a 75 Ω monitor. Unused analog outputs should be connected to ground. The DAC output traces should be as short as possible to minimize any impedance mismatch in the trace or video connector. Match the impedance of the R, G, B traces with the termination (75 Ω). The width of the traces will be determined by the distance from the ground plane and the dielectric constant of the PC board material. Try to keep the R, G, B traces at least 20 mil to 50 mil wide. Series ferrite beads can be added to the analog video signal to reduce high-frequency signals coupled onto the DAC outputs or reflected from the monitor.

To reduce the interaction of the analog video return current with board components, a separate video ground return trace can be added to the ground plane or signal layer. This trace connects directly to the ground of the edge card connector (see Figure 15). Using a separate video ground return path ensures that the RAMDAC ground is not corrupted with video return current.

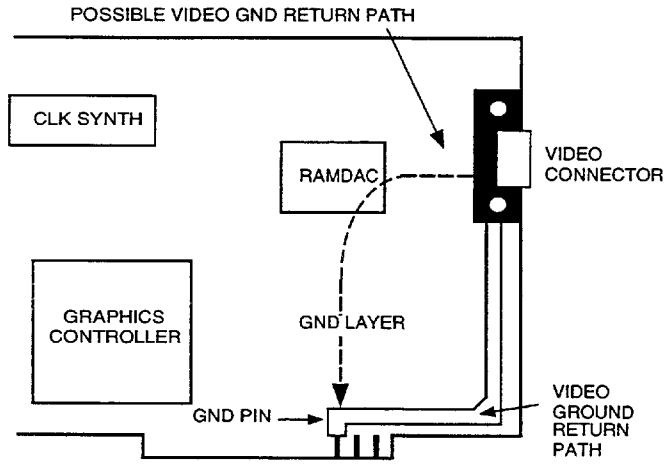


Figure 15. Video Ground Return Current Path

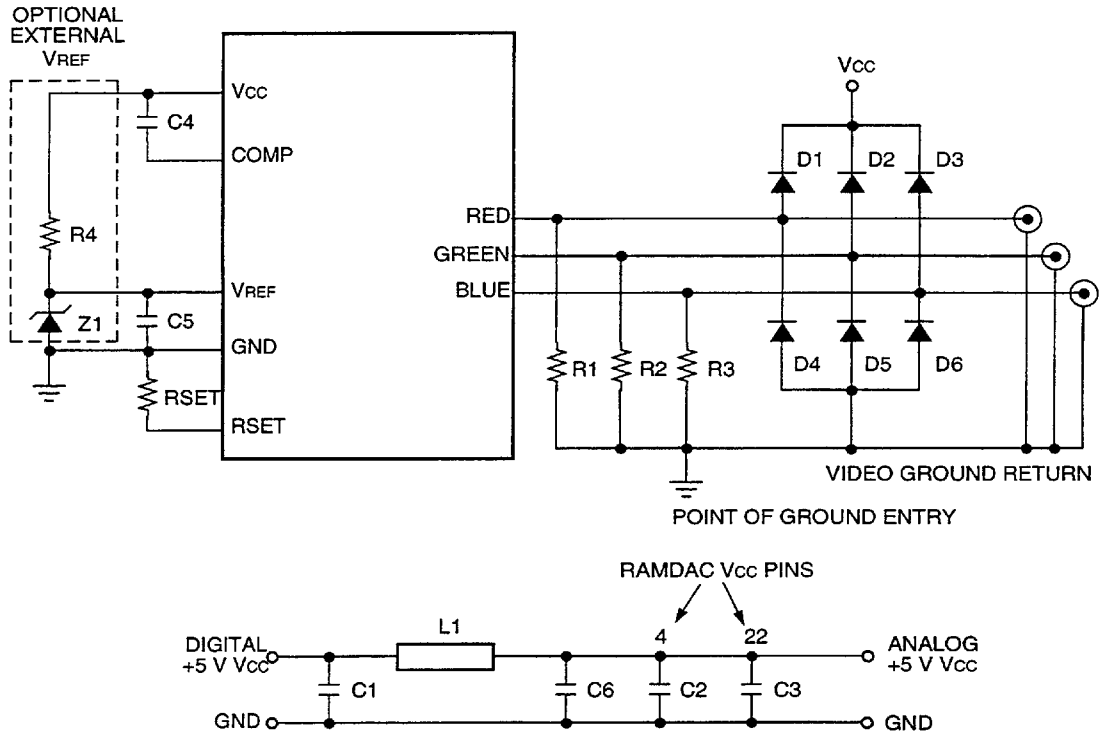
DAC Outputs

The ATT22C498 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching ac-coupled monitors.

The diode protection circuit shown in Figure 16 can prevent latch-up under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 are low-capacitance, fast-switching diodes.

Application Information (continued)

DAC Outputs (continued)



Note: Use of an external VREF for nonstandard operation will reduce accuracy provided with *PrecisionDAC* technology.

Figure 16. External and Internal Voltage Reference Typical Connection Diagram

Table 17. External and Internal Voltage Reference Parts List

Location	Description
C1—C5	0.1 µF ceramic capacitor
C6	10 µF capacitor
L1	Ferrite bead
R1—R3	75 Ω, 1% metal film resistor
RSET	147 Ω, 1% metal film resistor
D1—D6	Fast-switching diodes
R4*	Resistor
Z1*	Voltage reference

* Optional for external VREF.

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Typ	Max	Unit
V_{CC} (measured to GND)	—	—	—	7.0	V
Voltage on Any Digital Pin	—	GND – 0.5	—	V_{CC} + 0.5	V
Analog Output Short Circuit: Duration to Any Power Supply or Common	ISC	—	Indefinite	—	—
Ambient Operating Temperature	T_A	–55	—	125	°C
Storage Temperature	T_{stg}	–65	—	150	°C
Junction Temperature	T_J	—	—	150	°C
Vapor Phase Soldering (60 s)	TV_{SOL}	—	—	220	°C

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply	V_{CC}	4.75	5.00	5.25	V
Ambient Operating Temperature	T_A	0	—	70	°C
Output Load	R_L	—	37.5	—	Ω
Reference Voltage	V_{REF}	Internal			V

Electrical Characteristics

Table 18. dc Characteristics 1

Test conditions generate RS-343A video signals unless otherwise specified. The recommended operating condition for generating test signals is RSET = 147 Ω, and internal V_{REF}. The parameters below are applicable over full voltage and temperature ranges as shown in the Recommended Operating Conditions table.

Parameter	Symbol	Min	Typ	Max	Unit
Digital Inputs:					
Input Voltage:					
Low	V_{IL}	GND – 0.5	—	0.8	V
High	V_{IH}	2.0	—	V_{CC} + 0.5	V
Input Current:					
Low (V_{IN} = 0.4 V)	I_{IL}	—	—	–1	µA
High (V_{IN} = 2.4 V)	I_{IH}	—	—	1	µA
Capacitance (f = 1 MHz, V_{IN} = 2.4 V)	Cin	—	—	7	pF
Digital Outputs:					
Output Voltage:					
Low (I_{OL} = 3.2 mA)	V_{OL}	—	—	0.4	V
High (I_{OH} = –4 mA)	V_{OH}	2.4	—	—	V
3-State Current	I_{OZ}	—	—	50	µA
Capacitance	C_{DOUT}	—	—	7	pF

Electrical Characteristics (continued)

Table 19. dc Characteristics 2

Test conditions generate RS-343A video signals unless otherwise specified. The recommended operating condition for generating test signals is RSET = 147 Ω, and internal V_{REF}. The parameters below are applicable over full voltage and temperature ranges as shown in the Recommended Operating Conditions table.

Parameter	Symbol	Min	Typ	Max	Unit
Resolution (each DAC):	—	8	8	8	bits
Accuracy (each DAC):					
Integral Linearity Error:	IL				
Each DAC, 6-bit Mode	—	—	—	±1/4	LSB
Each DAC, 8-bit Mode	—	—	—	±1	LSB
Differential Linearity Error:	DL				
Each DAC, 6-bit Mode	—	—	—	±1/4	LSB
Each DAC, 8-bit Mode	—	—	—	±1	LSB
Gain Error	—	—	±3	±5	%
Monotonicity	—	—	Guaranteed	—	Scale
Coding	—	—	—	—	Binary
Analog Outputs:					
Gray Scale Current Range	Igray	—	—	20	mA
Output Current:					
White Level Relative to Black	Iwb	16.74	17.62	18.50	mA
Black Level Relative to Blank:	Ibb				
With Pedestal	—	0.95	1.44	1.90	mA
Without Pedestal	—	0	5	50	µA
Blank Level	Iblank	0	5	50	µA
LSB Size:	Ilsb				
6-bit	—	—	279.68	—	µA
8-bit	—	—	69.1	—	µA
DAC to DAC Matching	—	—	2	5	%
Output Compliance	V_{OC}	–0.5	—	1.5	V
Output Impedance	RA_{OUT}	—	10	—	kΩ
Output Capacitance (f = 1 MHz, I_{OUT} = 0 mA)	CA_{OUT}	—	—	30	pF
Internal Reference Output	V_{REF}	—	1.235	—	V
SENSE Trip Level	V_{SEN}	270	340	410	mV
Power Supply Rejection Ratio:	PSRR	—	—	0.5	%/% ΔVcc
(COMP = 0.1 µF, f = 1 kHz)	—	—	—	–6	dB

Electrical Characteristics (continued)

Table 20. ac Characteristics

The recommended operating condition for generating test signals is RSET = 147 Ω, and internal V_{REF}. TTL-level input values are 0 V to 3 V, with input rise/fall times ≤3 ns, measured from 10% to 90% points. Timing reference points are 50% for both inputs and outputs. Analog output load ≤10 pF, SENSE , D[7:0] output load ≤50 pF. The parameters below are applicable over full voltage and temperature ranges as shown in the Recommended Operating Conditions table.

		170 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Internal 2x Clock Rate (reference only)	fmax	—	—	170	MHz
PCLK Rate, 2x Clock Enabled	f2x	0	—	85	MHz
PCLK Rate, 2x Clock Disabled	fmax	—	—	110	MHz
PCLK Cycle Time	1	9.09	—	—	ns
PCLK Pulse Width High or Low	2	4	—	—	ns
PCLK Duty Cycle, 2x Clock (digital)	2xdc	45	—	55	%
PCLK Duty Cycle, 2x Clock (analog)	2xdc	30	—	70	%
DAC Performance:					
Analog Output Delay	3	—	—	30	ns
Analog Output Rise/Fall Time	4	—	2	—	ns
Analog Output Setting Time	—	—	13	—	ns
Clock and Data Feedthrough	—	—	–30	—	dB
Glitch Energy	—	—	75	—	pV-s
SENSE Output Delay	—	—	1	—	µs
DAC to DAC Crosstalk	—	—	–23	—	dB
Analog Output Skew	—	—	—	2	ns
Pixel and Control Timing:					
P[15:0], MSW, BLANK Setup	5	2	—	—	ns
P[15:0], MSW, BLANK Hold	6	2	—	—	ns
Microprocessor Port:					
RS[1:0] Setup Time	7	10	—	—	ns
RS[1:0] Hold Time	8	10	—	—	ns
RD Asserted to D[7:0] Driven	9	5	—	—	ns
RD Asserted to D[7:0] Valid	10	—	—	40	ns
RD Negated to D[7:0] 3-Stated	11	—	—	20	ns
Read D[7:0] Hold Time	12	5	—	—	ns
Write D[7:0] Setup Time	13	10	—	—	ns
Write D[7:0] Hold Time	14	10	—	—	ns
RD , WR Pulse Width Low	15	50	—	—	ns
RD , WR Pulse Width High, CR0[0] = 0	16	6	—	—	PCLK
Supply Current and Pipeline Delay:					
Pipeline Delay:*	Pipe				
Vcc Supply Current	Icc	—	225	250	mA
Sleep Current (PCLK = 35 MHz)	Islp	—	5	—	mA

* Pipeline delay is fixed for each mode (see Table 11 for pipeline delay for each mode).

Electrical Characteristics (continued)

Table 20. ac Characteristics (continued)

The recommended operating condition for generating test signals is RSET = 147 Ω, and internal V_{REF}. TTL-level input values are 0 V to 3 V, with input rise/fall times ≤3 ns, measured from 10% to 90% points. Timing reference points are 50% for both inputs and outputs. Analog output load ≤10 pF, SENSE , D[7:0] output load ≤50 pF. The parameters below are applicable over full voltage and temperature ranges as shown in the Recommended Operating Conditions table.

		135 MHz Devices			110 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Internal 2x Clock Rate (reference only)	fmax	—	—	135	—	—	110	MHz
PCLK Rate, 2x Clock Enabled	f2x	0	—	67.5	0	—	55	MHz
PCLK Rate, 2x Clock Disabled	fmax	—	—	110	—	—	80	MHz
PCLK Cycle Time	1	9.09	—	—	12.5	—	—	ns
PCLK Pulse Width High or Low	2	4	—	—	5.4	—	—	ns
PCLK Duty Cycle, 2x Clock (digital)	2xdc	45	—	55	45	—	55	%
PCLK Duty Cycle, 2x Clock (analog)	2xdc	30	—	70	30	—	70	%
DAC Performance:								
Analog Output Delay	3	—	—	30	—	—	30	ns
Analog Output Rise/Fall Time	4	—	3	—	—	3	—	ns
Analog Output Setting Time	—	—	13	—	—	13	—	ns
Clock and Data Feedthrough	—	—	–30	—	—	–30	—	dB
Glitch Energy	—	—	75	—	—	75	—	pV-s
SENSE Output Delay	—	—	1	—	—	1	—	µs
DAC to DAC Crosstalk	—	—	–23	—	—	–23	—	dB
Analog Output Skew	—	—	—	2	—	—	2	ns
Pixel and Control Timing:								
P[15:0], MSW, BLANK Setup	5	2	—	—	3	—	—	ns
P[15:0], MSW, BLANK Hold	6	2	—	—	3	—	—	ns
Microprocessor Port:								
RS[1:0] Setup Time	7	10	—	—	10	—	—	ns
RS[1:0] Hold Time	8	10	—	—	10	—	—	ns
RD Asserted to D[7:0] Driven	9	5	—	—	5	—	—	ns
RD Asserted to D[7:0] Valid	10	—	—	40	—	—	40	ns
RD Negated to D[7:0] 3-Stated	11	—	—	20	—	—	20	ns
Read D[7:0] Hold Time	12	5	—	—	5	—	—	ns
Write D[7:0] Setup Time	13	10	—	—	10	—	—	ns
Write D[7:0] Hold Time	14	10	—	—	10	—	—	ns
RD , WR Pulse Width Low	15	50	—	—	50	—	—	ns
RD , WR Pulse Width High, CR0[0] = 0	16	6	—	—	6	—	—	PCLK
Supply Current and Pipeline Delay:								
Pipeline Delay:*	Pipe							
Vcc Supply Current	Icc	—	195	220	—	170	195	mA
Sleep Current (PCLK = 35 MHz)	Islp	—	5	—	—	5	—	mA

* Pipeline delay is fixed for each mode (see Table 11 for pipeline delay for each mode).

Timing Characteristics

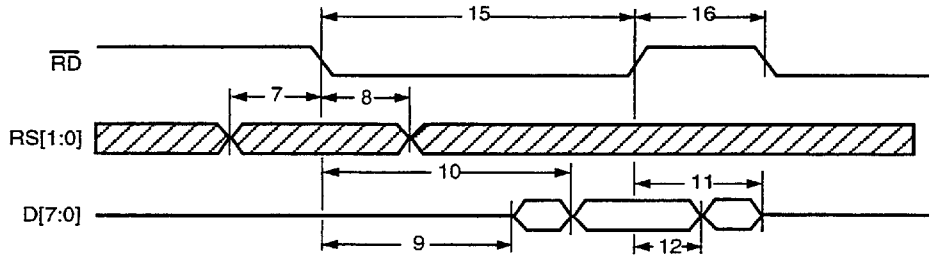


Figure 17. Basic Read Cycle Timing

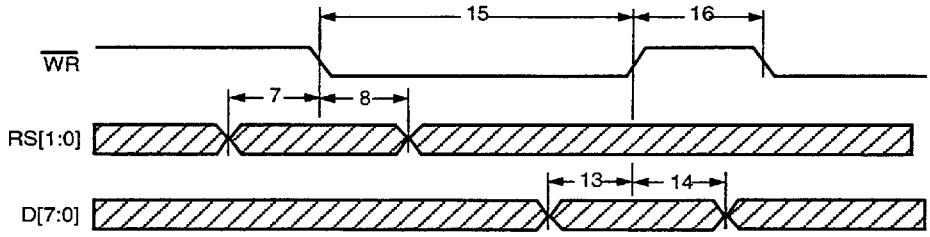


Figure 18. Basic Write Cycle Timing

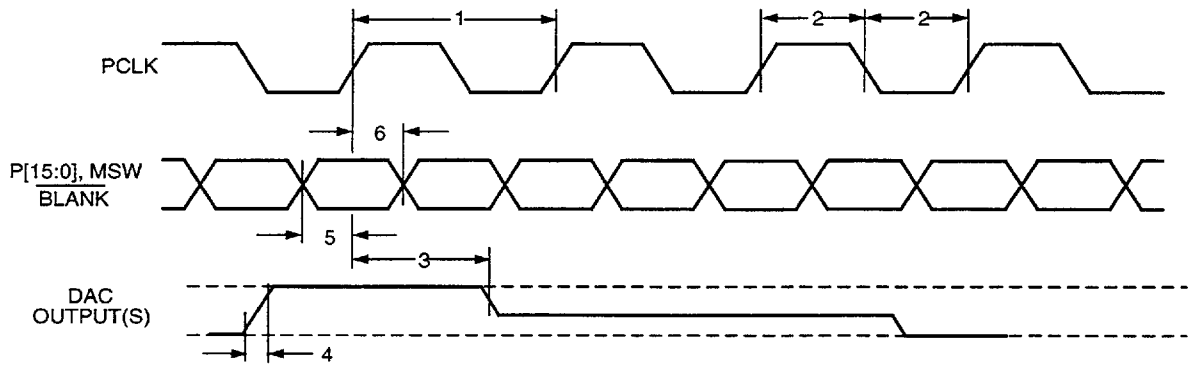
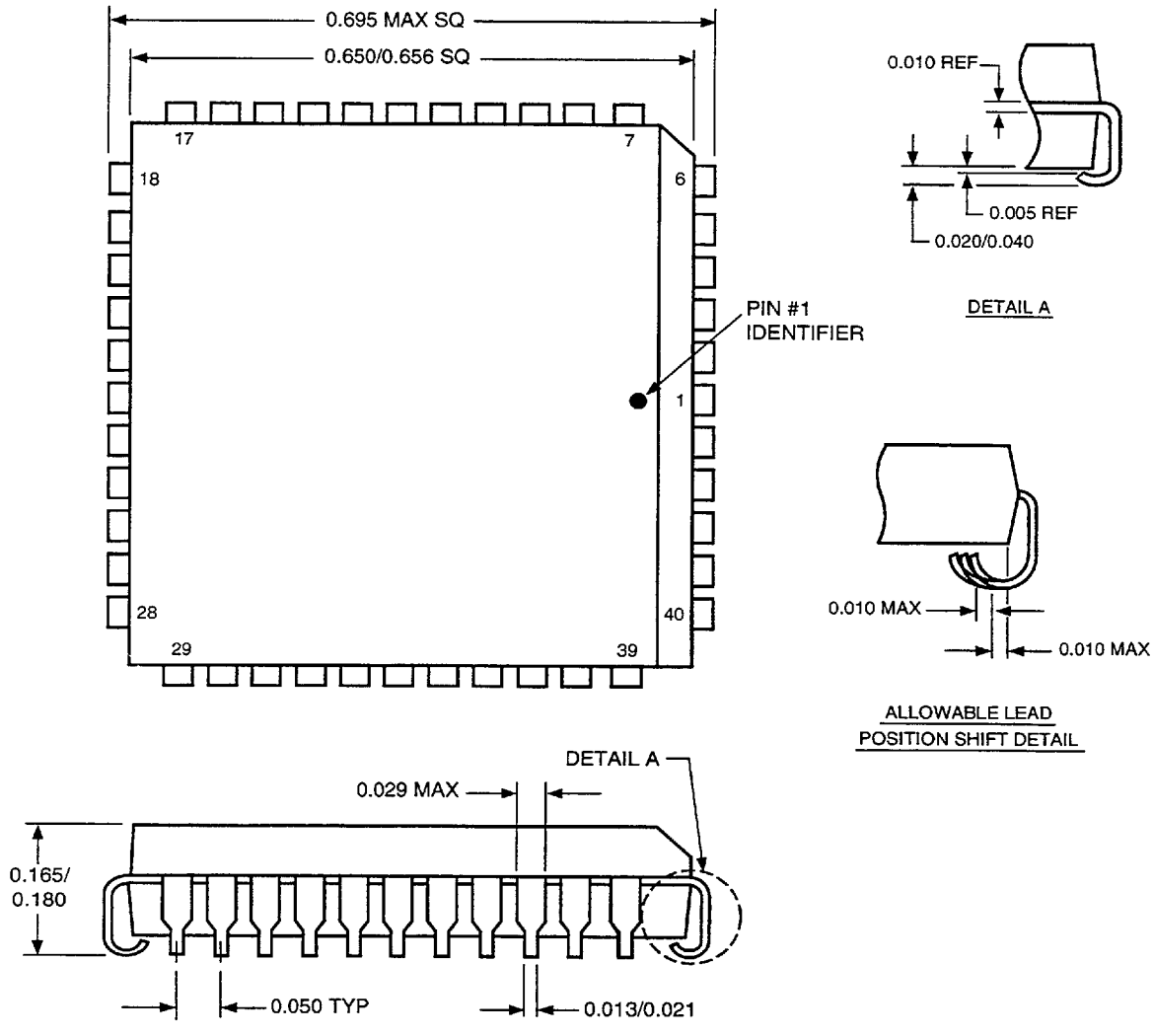


Figure 19. Pixel Input and Video Output Timing

Outline Diagram

44-Pin PLCC Package

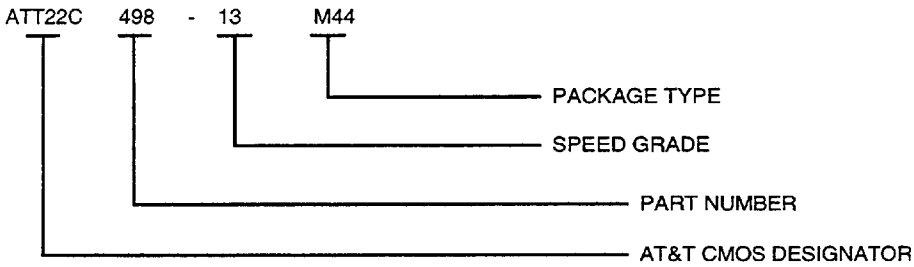
Dimensions are inches.



Ordering Information

Device	Speed	Temperature
ATT22C498-17M44	170 MHz	0 °C to 70 °C
ATT22C498-13M44	135 MHz	0 °C to 70 °C
ATT22C498-11M44	110 MHz	0 °C to 70 °C

Note: M44 is the package designator for the 44-pin PLCC.



For additional information, contact your AT&T Account Manager or the following:
U.S.A.: AT&T Microelectronics, 555 Union Boulevard, Room 21Q-133BA, Allentown, PA 18103
1-800-372-2447, FAX 610-712-4106 (In CANADA: **1-800-553-2448**, FAX 610-712-4106)
ASIA PACIFIC: AT&T Microelectronics Asia/Pacific, 14 Science Park Drive, #03-02A/04 The Maxwell, Singapore 0511
Tel. (65) 778-8833, FAX (65) 777-7495
JAPAN: AT&T Microelectronics, AT&T Japan Ltd., 7-18, Higashi-Gotanda 2-chome, Shinagawa-ku, Tokyo 141, Japan
Tel. (81) 3-5421-1600, FAX (81) 3-5421-1700
For data requests in Europe:
AT&T DATALINE: **Tel. (44) 1734 324 299**, FAX (44) 1734 328 148
For technical inquiries in Europe:
CENTRAL EUROPE: **(49) 89 95086 0** (Munich), NORTHERN EUROPE: **(44) 1344 487 111** (Bracknell UK),
FRANCE: **(33) 1 47 67 47 67** (Paris), SOUTHERN EUROPE: **(39) 2 6601 1800** (Milan) or **(34) 1 807 1700** (Madrid)

June 1995
DS94-104ASSP

AT&T Microelectronics

47003