Data Sheet
March 1992

AT&T Microelectronics

ATT7C186

High-Speed CMOS SRAM 64 Kbits (8K x 8), Flash Clear

Features

- High-speed read-access time — 12 ns maximum access time
- High-speed flash clear
- Automatic powerdown during long cycles
- Advanced CMOS technology
- Industry-standard pinout
- Data retention at 2 V for battery backup operation
- Plug-compatible with IDT7165
- Low-power operation
  — Active: 750 mW typical at 25 ns
  — Standby: 500 µW typical
- Package styles available:
  — 28-pin, plastic DIP
  — 28-pin, plastic SOJ (J-lead)

Description

The ATT7C186 device is a high-performance, low-power, CMOS static RAM organized as 8,192 words by 8 bits per word with the 8-bit data input/output on shared I/O pins. The device is offered in the industry-standard 8K x 8 SRAM pinout with a flash-clear function implemented on pin 1, which is normally a no connect.

The ATT7C186 device is available in four speeds with maximum access times from 12 ns to 25 ns. Operation is from a single 5 V power supply. Power consumption is 750 mW (typical) at 25 ns. Dissipation drops to 75 mW (typical) when the memory is in automatic powerdown mode. To speed switching and reduce ground bounce, noise-controlling *3-V** output circuitry is incorporated. This limits V_{OH} swings, while still maintaining full TTL compatibility.

Two standby modes are available. Automatic powerdown during long cycles reduces power consumption when memory is put into powerdown mode by deselecting CE2, or during read or write accesses that are longer than the minimum access time.

In addition, data can be retained in inactive storage with a supply voltage as low as 2 V. The ATT7C186 typically consumes only 30 µW at 3 V, thereby allowing effective battery backup operation.

**3-V* is a trademark of Logic Devices, Inc.

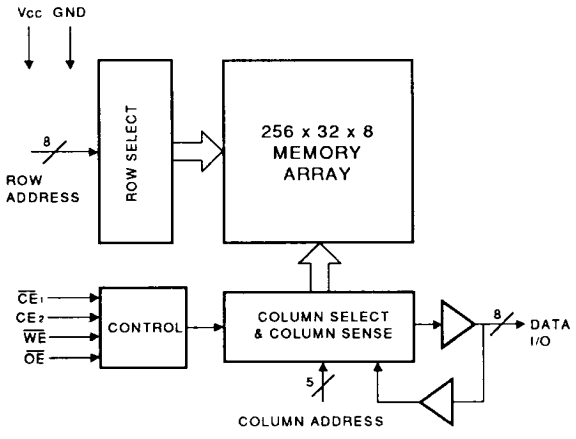

Figure 1. Block Diagram

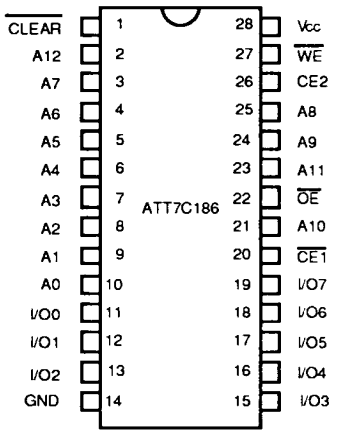

Figure 2. Pin Diagram

Table 1. Pin Descriptions

Pin	Name/Function
A0—A12	Address
I/O0—I/O7	Data Input/Output
$\overline{\text{CLEAR}}$	Clear Address Tag
$\overline{\text{CE 1}}$ and CE2	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
GND	Ground
Vcc	Power

Functional Description

The ATT7C186 device provides asynchronous (unclocked) operation with matching access and cycle times. Two chip enables and a 3-state I/O bus with a separate output-enable control simplify the connection of several chips for increased storage capacity. Memory locations are specified on address pins A0 through A12 with the functions as defined in Table 2.

During $\overline{\text{CLEAR}}$, the state of the I/O pins remains completely defined by the $\overline{\text{WE}}$, $\overline{\text{CE1}}$, CE2, and $\overline{\text{OE}}$ control inputs. Data-in has the same polarity as data-out. Latch-up and static discharge protection are provided on-chip. The ATT7C186 can withstand an injection of up to 200 mA on any pin without damage.

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{stg}	–65	150	°C
Operating Ambient Temperature	T_A	–55	125	°C
Supply Voltage with Respect to Ground	V_{CC}	–0.5	7.0	V
Input Signal with Respect to Ground	—	–3.0	7.0	V
Signal Applied to High-impedance Output	—	–3.0	7.0	V
Output Current into Low Outputs	—	—	25	mA
Latch-up Current	—	>200	—	mA

Recommended Operating Conditions

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation	0 °C to 70 °C	4.5 V ≤ Vcc ≤ 5.5 V
Data Retention	0 °C to 70 °C	2.0 V ≤ Vcc ≤ 5.5 V

Truth Table

Table 2. Truth Table

$\overline{CE1}$	$\overline{CE2}$	$\overline{WE}$	$\overline{OE}$	$\overline{CLEAR}$	Inputs/Outputs	Mode	Power
X	X	X	X	L	—	Clear A11 bits to low	Active
H	H	X	X	H	High Z	Deselect	Active*
X	L	X	X	H	High Z	Powerdown	Standby (I_{CC2} and I_{CC3})
L	H	H	H	H	High Z	Output Disabled	Active*
L	H	H	L	H	Data Out	Read	Active
L	H	L	X	H	Data In	Write	Active

*$I_{CC} \cong I_{CC1}$ at fb followed by powerdown after tICHICL has elapsed.

Electrical Characteristics

Table 3. General Electrical Characteristics

Over all Recommended Operating Conditions

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage:						
High	V_{OH}	I_{OH} = –4.0 mA, Vcc = 4.5 V	2.4	—	—	V
Low	V_{OL}	I_{OL} = 8.0 mA	—	—	0.4	V
Input Voltage:						
High	V_{IH}	—	2.2	—	Vcc + 0.3	V
Low[1]	V_{IL}	—	–3.0	—	0.8	V
Input Current	I_{IX}	Ground ≤ V_I ≤ Vcc	–10	—	10	µA
Output Leakage Current	I_{OZ}	Ground ≤ Vo ≤ Vcc, $\overline{CE}$ = Vcc	–10	—	10	µA
Output Short Current	I_{OS}	Vo = Ground, Vcc = Max[2]	—	—	–350	mA
Vcc Current:						
Inactive[3]	I_{CC2}	—	—	15	30	mA
Standby[4]	I_{CC3}	—	—	100	500	µA
DR Mode	I_{CC4}	Vcc = 3.0 V[5]	—	10	250	µA
Capacitance:						
Input	C_I	T_A = 25 °C, Vcc = 5.0 V	—	—	5	pF
Output	C_O	Test frequency = 1 MHz[6]	—	—	7	pF

1. This device provides hard clamping of transient undershoot. Input levels below ground are clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V, subject only to power dissipation and bond-wire fusing constraints.
2. Duration of the output short-circuit should not exceed 30 s.
3. Tested with outputs open and all address and data inputs changing at the maximum write-cycle rate. The device is continuously disabled, i.e., $\overline{CE1}$ ≥ V_{IH} or CE2 ≤ V_{IL}.
4. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE1}$ = Vcc, CE2 = ground. Input levels are within 0.2 V of Vcc or ground.
5. Data retention operation requires that Vcc never drops below 2.0 V. $\overline{CE1}$ must be ≥ Vcc – 0.2 V. For the ATT7C186, all other inputs meet V_{IN} < 0.2 V or V_{IN} ≥ Vcc – 0.2 V to ensure full powerdown.
6. This parameter is not 100% tested.

Table 4. Electrical Characteristics by Speed

Parameter	Symbol	Test Conditions	Speed (ns)				Unit
			25	20	15	12	
Max Vcc Current, Active	I_{CC1}	*	120	140	185	225	mA

* Tested with outputs open and all address and data inputs changing at the maximum write-cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE1}$, CE2, and $\overline{WE}$ ≤ V_{IL}. Input pulse levels are 0 V to 3.0 V. Max Icc shown applies over the active operating temperature range.

Timing Characteristics

Table 5. Read Cycle[1, 2, 3, 4]

Over all Recommended Operating Conditions; all measurements in ns. Test conditions assume input transition times of <3 ns, reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V (see Figure 10), and output loading for specified I_{OL} and I_{OH} +30 pF (see Figure 9A).

Symbol	Parameter	Speed (ns)							
		25		20		15		12	
		Min	Max	Min	Max	Min	Max	Min	Max
tADXADX, tCE1LCE1H	Read-cycle Time	25	—	20	—	15	—	12	—
tADXDOV	Address Change to Output Valid[5, 6]	—	25	—	20	—	15	—	12
tADXDOX	Address Change to Output Change	3	—	3	—	3	—	3	—
tCE1LDOV	$\overline{CE1}$ Low to Output Valid[5, 7]	—	12	—	10	—	8	—	6
tCE2HDOV	CE2 High to Output Valid[5, 7]	—	25	—	20	—	15	—	12
tCE1LDOZ, tCE2HDOZ	Chip Enable Active to Output Low-Z[8, 9]	3	—	3	—	3	—	3	—
tCE2LDOZ, tCE1HDOZ	Chip Enable Inactive to Output High-Z[8, 9]	—	10	—	8	—	8	—	5
tOELDOV	Output Enable Low to Output Valid	—	12	—	10	—	8	—	6
tOELDOZ	Output Enable Low to Output Low-Z[8, 9]	0	—	0	—	0	—	0	—
tOEHDOZ	Output Enable High to Output High-Z[8, 9]	—	10	—	8	—	5	—	5
tADXICH, tCE2HICH	Input Transition to Powerup[10, 11]	0	—	0	—	0	—	0	—
tICHICL, tCE2LICL	Powerup to Powerdown[10, 11]	—	25	—	20	—	20	—	20

1. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t ADXWEH (Table 6) is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.
2. All address timings are referenced from the last valid address line to the first transitioning address line.
3. $\overline{CE1}$, CE2, or $\overline{WE}$ must be inactive during address transitions.
4. This product is a very high-speed device, and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the Vcc and ground planes directly up to the contactor fingers. A 0.01 µF high-frequency capacitor is also required between Vcc and ground. To avoid signal reflections, proper terminations must be used.
5. $\overline{WE}$ is high for the read cycle.
6. During this state, the chip is continuously selected ($\overline{CE1}$ low, CE2 high).
7. All address lines are valid prior to or coincident with the later of $\overline{CE1}$ or CE2 transition to active.
8. At any given temperature and voltage condition, output-disable time is less than output-enable time for any given device.
9. Transition is measured ±200 mV from steady-state voltage with specified loading in Figure 9B. This parameter is sampled and not 100% tested.
10. This parameter is not 100% tested.
11. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions: (1) falling edge of CE2, (2) falling edge of $\overline{WE}$ ($\overline{CE1}$ and CE2 active), (3) transition on any address line ($\overline{CE1}$ and CE2 active), or (4) transition on any data line ($\overline{CE1}$, CE2, and $\overline{WE}$ active). The device automatically powers down from I_{CC1} to I_{CC2} after tICHICL has elapsed from any of the powerup triggers. Power dissipation is dependent only on cycle rate, not on chip-select pulse width.

Timing Characteristics (continued)

Table 6. Write Cycle[1, 2, 3, 4] (See Figures 5, 6, and 8).

Over all Recommended Operating Conditions; all measurements in ns. Test conditions assume input transition times of <3 ns, reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V (see Figure 10), and output loading for specified I_{OL} and I_{OH} +30 pF (see Figure 9A).

Symbol	Parameter	Speed (ns)							
		25		20		15		12	
		Min	Max	Min	Max	Min	Max	Min	Max
tADXADX	Write-cycle Time	20		20	—	15	—	12	—
tCE2HCE2L, tCE1LCE1H	Chip Enable Active to End of Write	15	—	15	—	12	—	10	—
tADXWEX, tADXWEL	Address Change to Beginning of Write	0	—	0	—	0	—	0	—
tADXWEH tADXCEH	Address Change to End of Write	15	—	15	—	12	—	10	—
tWEHADX, tCEHADX	End of Write to Address Change	0	—	0	—	0	—	0	—
tWELWEH, tWELCEH	Write Enable Low to End of Write	15	—	15	—	12	—	10	—
tDIVCEH, tDIVWEH	Data Invalid to Chip Enable High	10	—	10	—	7	—	6	—
tWEHDIX, tCEHDIX	End of Write to Data Change	0	—	0	—	0	—	0	—
tWEHDOZ	Write Enable High to Output Low-Z[5, 6]	0	—	0	—	0	—	0	—
tWELDOZ	Write Enable Low to Output High-Z[5, 6]	7	—	7	—	5	—	4	—
tCE2HICH, tCE1LICH	Chip Enable Active to Powerup[7, 8]	0	—	0	—	0	—	0	—
tWEHICL tCEHICL	Write Enable High to Powerdown[7, 8]	0	—	0	—	0	—	0	—
tCEHVCL	Chip Enable Inactive to Data Retention[7]	0	—	0	—	0	—	0	—

1. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, tADXWEH is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.
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5. At any given temperature and voltage condition, output-disable time is less than output-enable time for any given device.
6. Transition is measured ±200 mV from steady-state voltage with specified loading in Figure 9B. This parameter is sampled and not 100% tested.
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8. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions: (1) falling edge of CE2, (2) falling edge of $\overline{WE}$ ($\overline{CE1}$ and CE2 active), (3) transition on any address line ($\overline{CE1}$ and CE2 active), or (4) transition on any data line ($\overline{CE1}$, CE2, and $\overline{WE}$ active). The device automatically powers down from I_{CC1} to I_{CC2} after tICHICL has elapsed from any of the powerup triggers. Power dissipation is dependent only on cycle rate, not on chip-select pulse width.

Timing Characteristics (continued)

Table 7. $\overline{\text{CLEAR}}$ Cycle

Over all Recommended Operating Conditions; all measurements in ns. Test conditions assume input transition times of <3 ns, reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V (see Figure 10), and output loading for specified I_{OL} and I_{OH} +30 pF (see Figure 9A).

Symbol	Parameter	Speed (ns)							
		25		20		15		12	
		Min	Max	Min	Max	Min	Max	Min	Max
tCLCL	Clear Cycle Time	55	—	45	—	35	—	30	—
tCLCH	$\overline{\text{CLEAR}}$ Pulse Width	15	—	15	—	12	—	12	—
tCLWEX	$\overline{\text{CLEAR}}$ Low to Inputs Don't Care	0	—	0	—	0	—	0	—
tCLICL	$\overline{\text{CLEAR}}$ Low to Powerdown	—	55	—	45	—	35	—	30
tCLICH	$\overline{\text{CLEAR}}$ Low to Powerup	0	—	0	—	0	—	0	—

Notes:
Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, tADXWEH (Table 6) is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

All address timings are referenced from the last valid address line to the first transitioning address line.

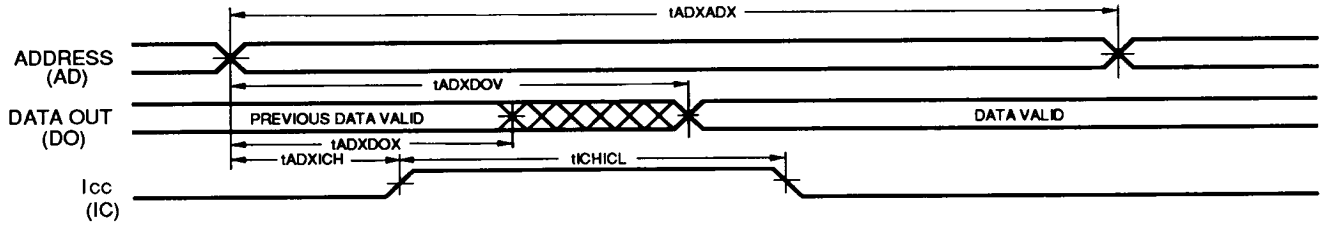
$\overline{\text{CE1}}$, CE2, or $\overline{\text{WE}}$ must be inactive during address transitions.

This product is a very high-speed device, and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the Vcc and ground planes directly up to the contactor fingers. A 0.01 µF high-frequency capacitor is also required between Vcc and ground. To avoid signal reflections, proper terminations must be used.

The flash-clear cycle is edge-triggered on the falling edge of $\overline{\text{CLEAR}}$ and lasts for tCLICL. During this time, the $\overline{\text{WE}}$ control input is internally disabled regardless of the state of $\overline{\text{CLEAR}}$ during tCLICL. Multiple $\overline{\text{CLEAR}}$ pulses during tCLICL are locked out. A new flash-clear cycle is only initiated on the first falling $\overline{\text{CLEAR}}$ edge after completion of the previous clear cycle. To ensure a complete clear of the entire memory array on powerup, the falling $\overline{\text{CLEAR}}$ edge should only be issued after Vcc has reached its normal operating voltage.

Timing Characteristics (continued)

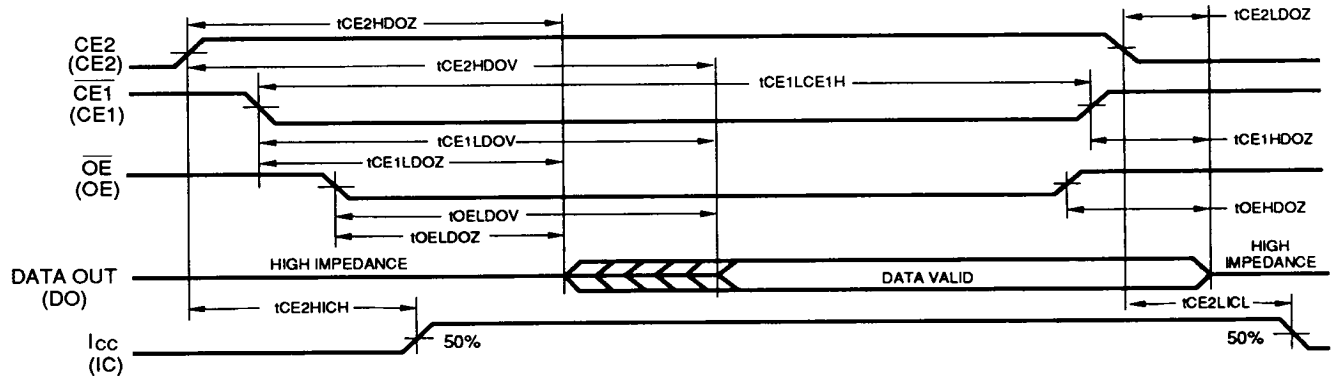
Timing Diagrams



Notes:
$\overline{WE}$ is high for the read cycle.

The chip is continuously selected ($\overline{CE1}$ low, CE2 high).

Figure 3. Read Cycle — Address-Controlled

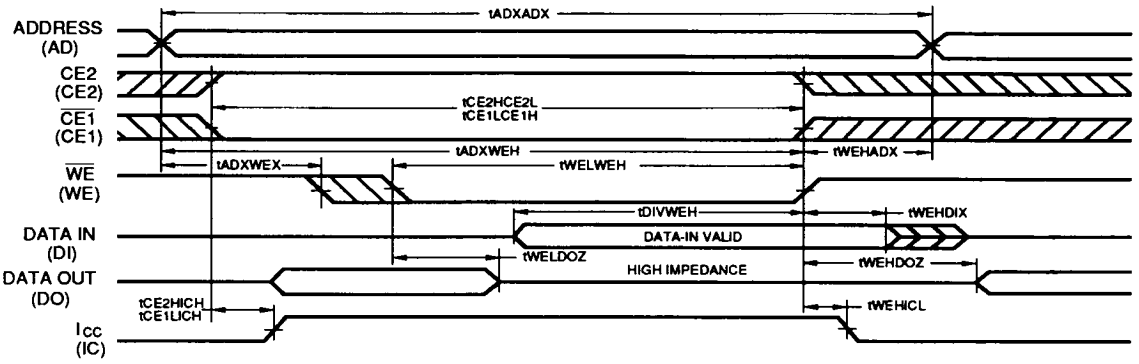


Notes:
$\overline{WE}$ is high for the read cycle.

All address lines are valid prior to or coincident with the later of $\overline{CE1}$ and CE2 transition to active.

Figure 4. Read Cycle — $\overline{CE}$ / $\overline{OE}$ -Controlled

Timing Characteristics (continued)



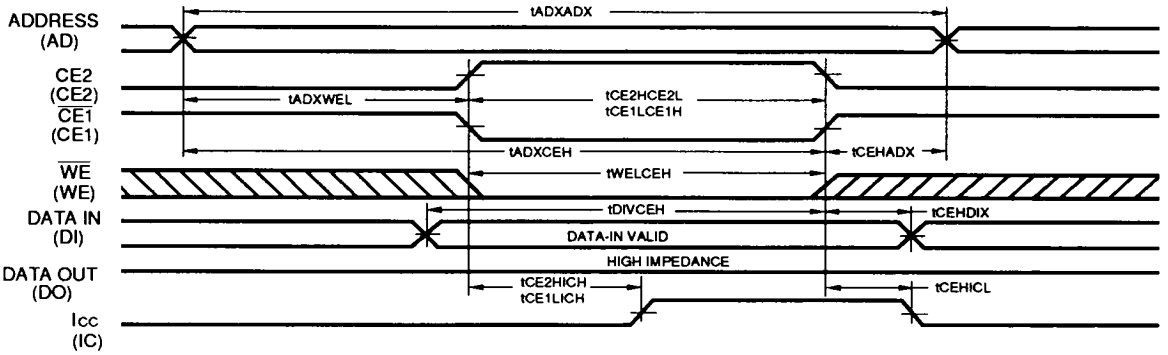
Notes:
The internal write cycle of the memory is defined by the overlap of $\overline{CE1}$ and CE2 active and $\overline{WE}$ low. All three signals must be active to initiate a write. Any signal can terminate a write by going inactive. The address, data, and control input setup and hold times should be referred to the signal that becomes active last or becomes inactive first.

If $\overline{WE}$ goes low before or concurrent with the later of $\overline{CE1}$ or CE2 going active, the output remains in a high-impedance state.

If $\overline{CE1}$ and CE2 go inactive before or concurrent with $\overline{WE}$ going high, the output remains in a high-impedance state.

Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions: (1) falling edge of CE2, (2) falling edge of $\overline{WE}$ ($\overline{CE1}$ and CE2 active), (3) transition on any address line ($\overline{CE1}$ and CE2 active), or (4) transition on any data line ($\overline{CE1}$, CE2, and $\overline{WE}$ active). The device automatically powers down from I_{CC1} to I_{CC2} after tICHICL has elapsed from any of the powerup triggers. Power dissipation is dependent only on cycle rate, not on chip-select pulse width.

Figure 5. Write Cycle — $\overline{WE}$ -Controlled



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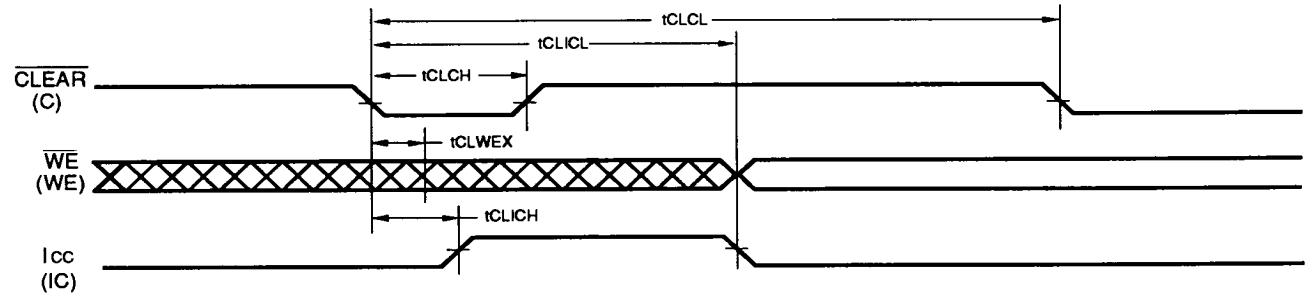
If $\overline{WE}$ goes low before or concurrent with the later of $\overline{CE1}$ or CE2 going active, the output remains in a high-impedance state.

If $\overline{CE1}$ and CE2 go inactive before or concurrent with $\overline{WE}$ going high, the output remains in a high-impedance state.

Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions: (1) falling edge of CE2, (2) falling edge of $\overline{WE}$ ($\overline{CE1}$ and CE2 active), (3) transition on any address line ($\overline{CE1}$ and CE2 active), or (4) transition on any data line ($\overline{CE1}$, CE2, and $\overline{WE}$ active). The device automatically powers down from I_{CC1} to I_{CC2} after tICHICL has elapsed from any of the powerup triggers. Power dissipation is dependent only on cycle rate, not on chip-select pulse width.

Figure 6. Write Cycle — $\overline{CE}$ -Controlled

Timing Characteristics (continued)



Note: The flash-clear cycle is edge-triggered on the falling edge of $\overline{\text{CLEAR}}$ and lasts for tCLICL. During this time, the $\overline{\text{WE}}$ control input is internally disabled regardless of the state of $\overline{\text{CLEAR}}$ during tCLICL. Multiple $\overline{\text{CLEAR}}$ pulses during tCLICL are locked out. A new flash-clear cycle is only initiated on the first falling $\overline{\text{CLEAR}}$ edge after completion of the previous clear cycle. To ensure a complete clear of the entire memory array on powerup, the falling $\overline{\text{CLEAR}}$ edge should only be issued after Vcc has reached its normal operating voltage.

Figure 7. $\overline{\text{CLEAR}}$ Timing

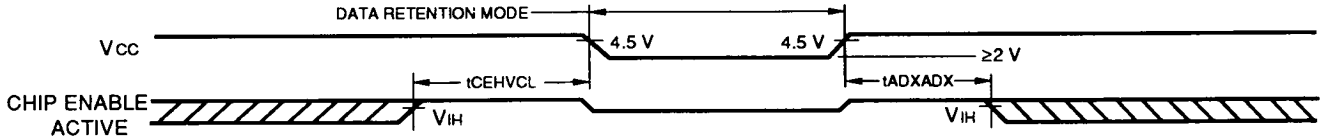


Figure 8. Data Retention

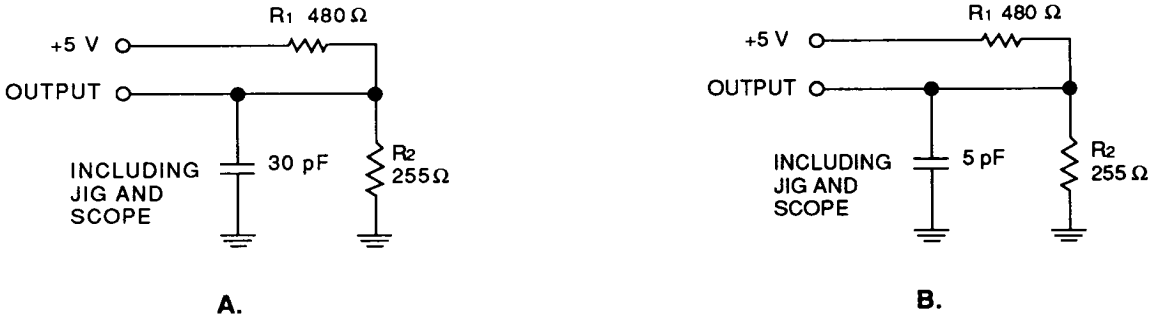


Figure 9. Test Loads

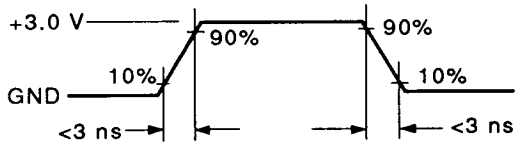
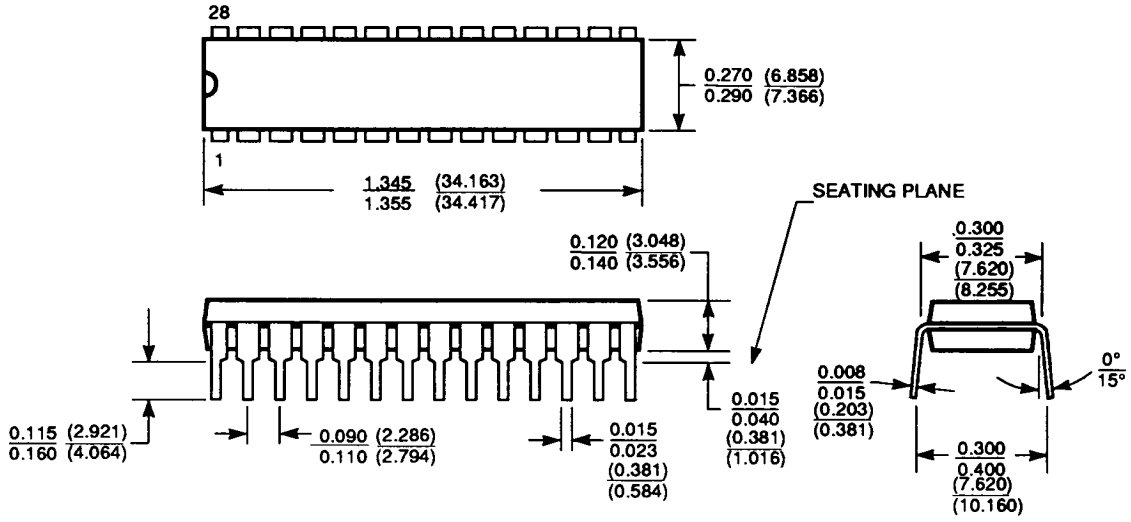


Figure 10. Transition Times

Outline Diagrams

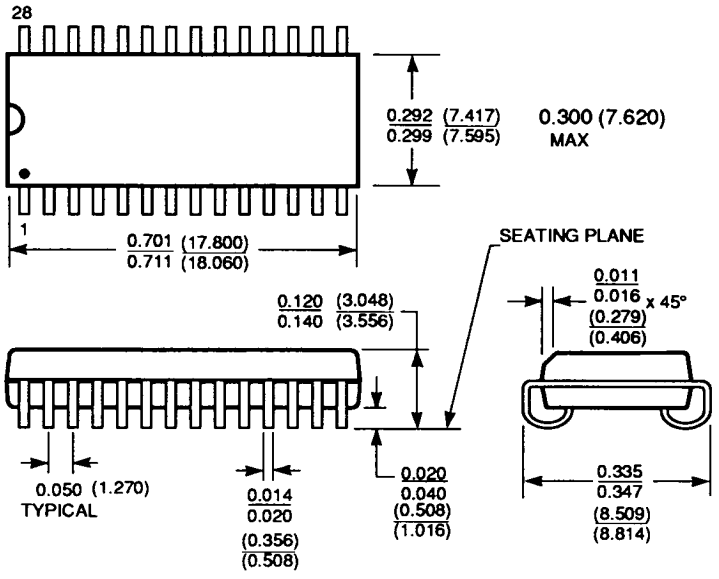
28-Pin, Plastic DIP

Dimensions are in inches and (millimeters).

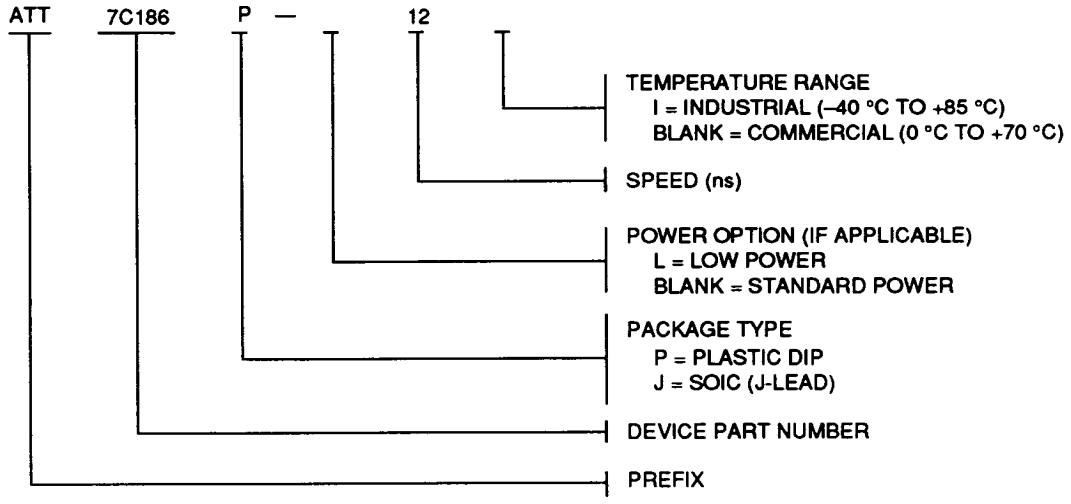


28-Pin, Plastic SOJ

Dimensions are in inches and (millimeters).



Ordering Information



Operating Range 0 °C to 70 °C

Package Style	Performance Speed			
	25 ns	20 ns	15 ns	12 ns
28-Pin, Plastic DIP	ATT7C186P–25	ATT7C186P–20	ATT7C186P–15	ATT7C186P–12
28-Pin, Plastic SOJ	ATT7C186J–25	ATT7C186J–20	ATT7C186J–15	ATT7C186J–12

For additional information, contact your AT&T Account Manager or the following:
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