Advance Data Sheet

AT&T

ATT91C010 Low-Power REACH1 Device

Features

- Fully-integrated single-chip read channel
- 5 V only all CMOS design
- Low-power operation: 225 mW max read mode/255 mW max write mode
- Standby mode power = 25 mW
- Data rates up to 30 Mbit/s
- Internal embedded servo demodulator
- On-chip pulse detector & AGC circuitry
- Fully integrated multizone constant density recording support
- On-chip DAC for PLL center frequency control
- Fast-acquisition zero-phase start PLL
- On-chip write precompensation circuitry
- µP Programmable via serial interface
- Available in both 44-pin PLCC package and EIAJ PQFP package

Description

The ATT91C010 all CMOS Read Channel Device (REACH1) has been designed specifically for low-power, small form factor Winchester rigid disk drives. The REACH1 consists of an automatic gain control (AGC) circuit, peak detector, pulse detector, embedded servo demodulator, write precompensation circuit, and data synchronizer. An on-chip current mode, DAC, permits accurate tuning of the data PLL's center frequency to facilitate the use of constant density recording techniques used to increase disk platter capacity.

The REACH1 is fabricated in AT&T's advanced .9 µm, mixed analog/digital CMOS process. In operation, the device dissipates less than 225 mW (read mode) or 255 mW (write mode) from a single 5 V supply. In powerdown standby mode, the power consumption decreases to under 25 mW.

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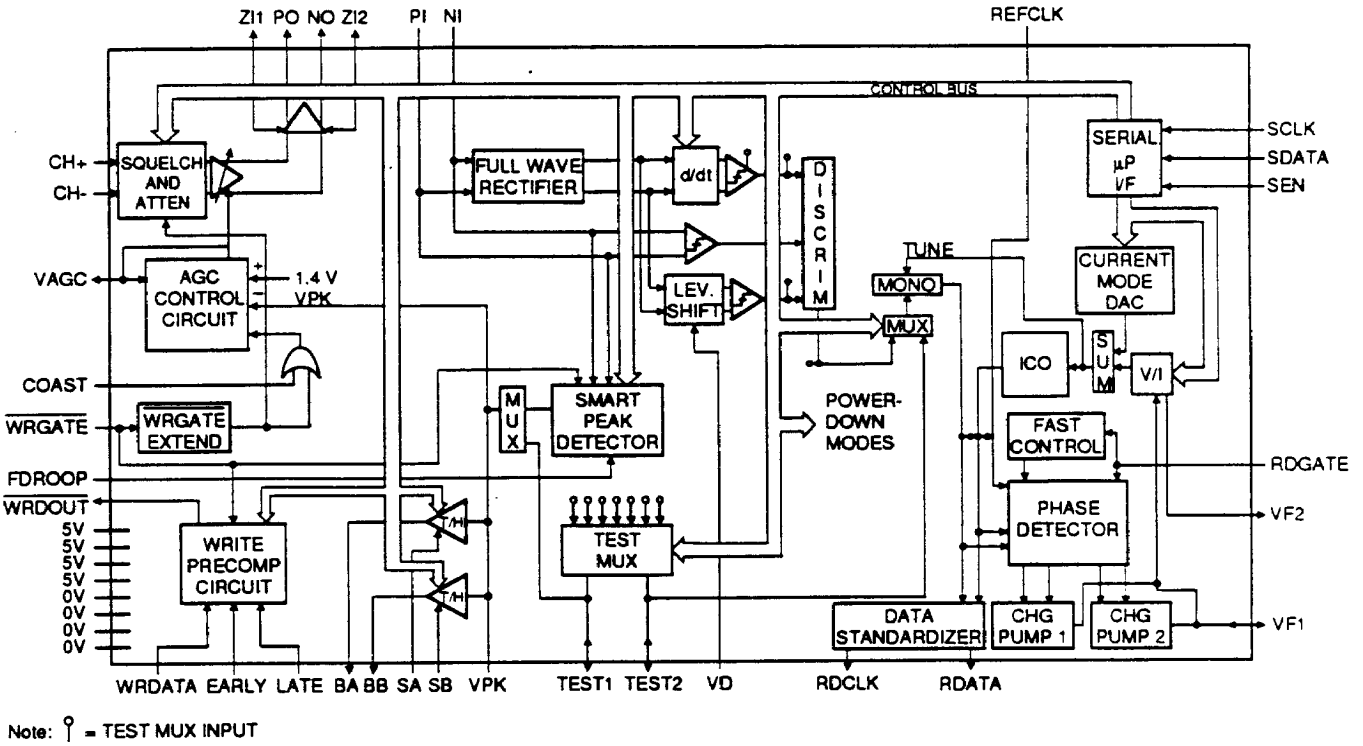


Figure 1. REACH1 Block Diagram

Pin Descriptions

Digital Signals

Table 1. Pin Descriptions

Pin	Symbol	Type	Name/Function
36,42	SA, SB	I	**Sample Bursts A, B.** Used to control track and hold cells for servo bursts A & B. A high level allows tracking of the respective burst. A low level will hold the sampled voltages.
41	RDGATE	I	**Read Gate.** Used to select the PLL reference clock and start the synchronization sequence. A high level selects the read data from the drive as the synchronization signal. A low level selects the crystal reference clock as the synchronization signal. When RDGATE is asserted, a zero-phase start of the PLL is initiated. The AGC loop exits the coast mode, and the PLL enters the fast acquisition mode for the first 16 data transitions, then automatically enters the slow acquisition mode.
34	$\overline{\text{WRGATE}}$	I	**Write Gate.** This input, when low, will cause the AGC gain to be held constant, the pulse detector circuitry to hold the last detected peak voltage, and the AGC amplifier input impedance to be reduced. When high, this input will cause the write precompensation circuitry to be powered down.
2	RDATA	O	**Read Data.** Encoded read data output synchronized with RDCLK.
1	RDCLK	O	**Read Clock.** During read data time, this output will run at 1.5 times the data rate.
40	REFCLK	I	**Reference Clock.** Crystal derived reference clock equal to the write clock frequency for the associated zone.
8	COAST	I	**Coast.** This input controls manual activation of the AGC coast mode. Coast mode is also entered when via $\overline{\text{WRGATE}}$ is active. When COAST is high, coast mode is entered, the voltage on VAGC is not updated and the variable gain amplifier will yield a constant gain. This signal has an internal pull-up.
4	SCLK	I	**Serial Clock.** This input is the clock generated by the microprocessor to shift serial data into the device.
3	SDATA	I	**Serial Data.** This input is the serial data from the microprocessor.
5	SEN	I	**Shift Enable.** This signal allows serial data to be shifted into the internal shift register.
43	FDROOP	I	**Fast Droop.** This input, when high, will cause the peak detector to enter a fast droop mode to allow the peak detector output to quickly adjust to very low signal levels. This mode is generally used during servo burst time.
37, 38	TEST1,2	I/O	**Test I/O.** Selected internal digital signals are output on these pins in Test Mode. In addition, these signals can become inputs and may be driven externally to force the injection of test waveforms into the device.
10	WRDATA	I	**Write Data Input.** This input is connected to the uncompensated write data pulse output of an external EN/DEC. A positive pulse indicates data.
9	EARLY	I	**Precompensate Early.** This input, when active-high, will cause the incoming write data to be advanced from 1 ns to 8 ns relative to the uncompensated data when it is output on the $\overline{\text{WRDOUT}}$ pin.
33	LATE	I	**Precompensate Late.** This input, when active-high, will cause the incoming write data to be delayed from 1 ns to 8 ns relative to the uncompensated data when it is output on the $\overline{\text{WRDOUT}}$ pin.
35	$\overline{\text{WRDOUT}}$	O	**Write Data Output.** This output is the precompensated WRDATA data pulses. Note that an inversion will occur from WRDATA to $\overline{\text{WRDOUT}}$.

Pin Descriptions (continued)

Analog Signals

Table 2. Pin Descriptions

Pin	Symbol	Type	Name/Function
22, 23	CH–, CH+	I	**Channel –,+.** Differential input signal from the read preamplifier.
28, 25	PO, NO	O	**Positive, Negative Out.** Differential output of the AGC circuit. These signals may be conditioned by an external filter prior to connection to the pulse position detection circuitry.
30, 31	PI, NI	I	**Positive, Negative In.** Differential inputs for filtered signal PO,NO.
14	VAGC	I/O	**Automatic Gain Control.** An external AGC capacitor may be connected between this point and ground. When the AGC charge pump is in coast mode, the AGC loop can be controlled by applying a voltage to this pin.
18, 17	BA, BB	O	**Burst A, B.** Sampled servo signals for the A and B bursts are output on these pins.
20	VD	I	**Discrimination Voltage.** This input is used to set the voltage level for the comparator that arms the discriminator logic in the pulse detector. An external resistor divider network connected between ground and the VPK output can be used to drive this input to make the hysteresis level equal to a percentage of the peak voltage detected.
21	VPK	O	**Peak Voltage.** The voltage level present on this input is the peak level detected on incoming data which is internally fed back to the AGC circuitry and pulse detector.
16	VF1	O	**Control Voltage for ICO.** This is the output of the charge pump. This output combined with VF2 should be attached to an external loop filter.
15	VF2	O	**Control Voltage for ICO.** This pin is connected to the loop filter as described in the VF1 pin description.
26, 27	ZI1,2	I/O	**Impedance In.** Connections for the external impedance for the output transconductance amplifier. The impedance can be a single resistor or a more complicated network for equalization.
29	GNDA	—	**Analog Ground.**
24	ANA +5	—	**Analog 5 V.**
11, 19,	NC	—	**No Connection.**
12	PLLGND	—	**PLL Ground.**
32, 39	DRVGND	—	**Ground for Output Drivers.**
44	DRV+5	—	**5 V Connection for Output Drivers.**
13	PLL+5	—	**PLL 5 V.**
7	DGND	—	**Digital Ground.**
6	DIG +5	—	**Digital +5 V.**

Pin Descriptions (continued)

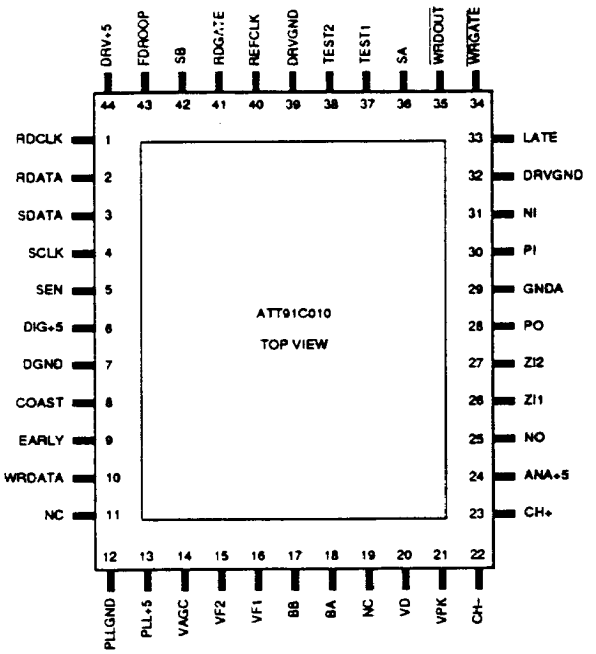


Figure 2. 44-Pin EIAJ PQFP Pin Diagram

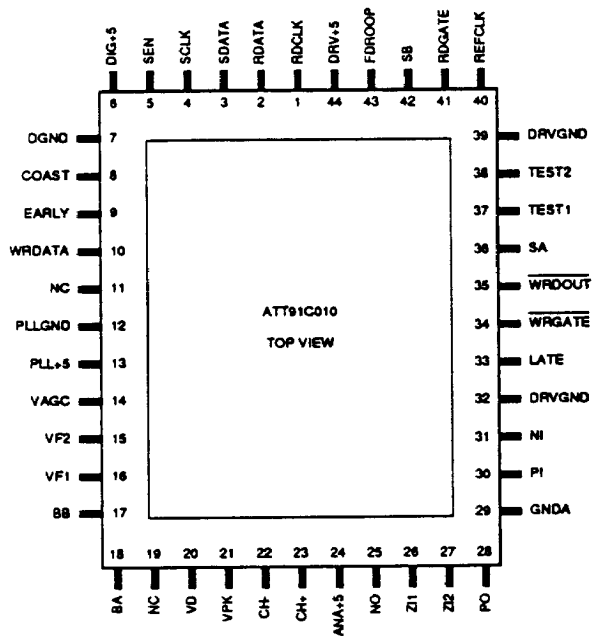


Figure 3. 44-Pin PLCC Pin Diagram

Functional Description

Automatic Gain Control

The AGC circuit consists of a variable gain amplifier, a charge pump, and a transconductance output stage. The variable gain amplifier provides linear gain amplification in two fully differential stages. The output of the variable gain amplifier goes to a transconductance output stage.

The input to the variable gain amplifier has an additional 10 dB attenuator which can be switched into the signal path under microprocessor control to allow higher than normal input voltage levels. When the WRGATE input signal is asserted, the input impedance of the VGA automatically lowers and squelches the input signal. The input impedance is kept low and the input remains squelched for an additional 1.5 µs (nominal) after WRGATE is released to allow the input signal from the external preamplifier to settle.

The differential transconductance output transforms the input voltages into differential currents through the use of an external impedance network. The output current can be converted directly to an external voltage through resistive loads to the positive supply, or they can be driven into an external passive equalizer filter.

The AGC operates to keep the peak voltage, VPK, from the pulse detector equal to an internally generated reference voltage. This is accomplished by sensing the difference in these two voltages and integrating the result onto an external loop filter connected to the VAGC pin. The resultant voltage controls the gain of the AGC. The time required to acquire the correct gain is proportional to the value of the capacitor connected to the VAGC pin.

When the COAST or $\overline{\text{WRGATE}}$ inputs are asserted, the AGC circuit enters coast mode. In this mode, the AGC control voltage into the variable gain amplifier is held constant. This permits the AGC loop to coast past periods of embedded servo information, periods of no data, or periods during disk write operations. When coast mode is activated by $\overline{\text{WRGATE}}$ going active, it will not terminate until the 1.5 µs timeout following $\overline{\text{WRGATE}}$ going inactive has expired.

Pulse Position Detector

The pulse position detector produces digital pulses aligned with the zero slope points of the analog input signal appearing on differential inputs PI and NI. The differentiator gain is set by means of the serial interface and is determined by the coarse center frequency value of the internal DAC. The gain can be further adjusted to correspond to the data rate being read from the media with additional control bits from the serial interface.

The discriminator is made READY when the sign of the input signal (before the rectifier) changes. If the discriminator has been made READY, it will be ARMED when the rectified input signal exceeds the discrimination level. A pulse is generated by the differentiator for the zero slope point in the rectified input signal. Once the discriminator is ARMED, it will allow this pulse to pass. After the pulse passes, the discriminator will be NOT READY and NOT ARMED and will have to be made READY and ARMED again before it will allow another pulse to pass.

The discrimination level is controlled by external input pin VD. Connection of the peak voltage output on the VPK pin directly to the discrimination voltage input VD will result in a discrimination voltage equal to 100% of the peak voltage. For discrimination levels less than 100%, an external resistor divider network should be used.

Smart Peak Detector

The peak detector output is fed back to the AGC charge pump circuitry and to the servo demodulator block. The output of the peak detector tracks the peak magnitude of the input signal with minimum droop between peaks.

The peak detector implementation is master-slave. The master has a droop rate set by an internal RC combination and generates an internal signal corresponding to the output of a traditional peak detector. The output of the smart peak detector comes from the slave whose output is only allowed to droop when the master is charging. This implementation results in minimum droop during periods of no data or few data transitions while allowing fast response to actual changes in peak signal levels.

Functional Description (continued)

Under normal conditions of data read, the droop rate of the master cell is controlled to allow a limited amount of droop during the longest permissible string of zeroes in the input signal. When the input signal magnitude drops suddenly to zero, the master cell doesn't charge at all and no droop current is routed to the slave cell. When this occurs, a data rate dependent time-out begins. When the time-out expires, a substantial droop current is provided to the slave cell.

The fast droop mode is manually controlled via input pin FDROOP. Fast droop mode is typically used to enable fast droop during servo burst time. The droop rates and time-outs in fast droop mode are nominally three times the values when the peak detector is not in fast droop mode.

Write Precompensation

The write precompensation circuitry reproduces the write data pulse with programmable advance (EARLY) or delay (LATE) times with respect to the nominal WRDOUT output. The amount of advance or delay time is independently programmable from 1 ns to 8 ns using register 3 of the serial input. The write precompensation circuitry will be automatically powered off when WRGATE is deasserted.

Servo Demodulator

The servo demodulator consists of two track and hold circuits. The track and hold circuits provide a variable gain which is controlled by bits from the serial input block. Within the track and hold circuits, an RC low pass filter is employed to reduce the effects of noise on the peak voltages detected. The track and hold low pass filter has a data rate dependent corner frequency.

The servo demodulator is configured to track and hold servo voltages under the control of externally generated strobes SA and SB. The sampled analog voltages are held and output on pins BA and BB.

Since the amplitude of the signals appearing during the A and B bursts can vary widely, the peak detector should be placed in a fast droop mode. This can be accomplished during the servo sample time by driving the FDROOP input active high.

Data Synchronizer

The data synchronizer consists of a current controlled oscillator, harmonic/non-harmonic phase detector, charge pump, precision tunable monostable, and data standardizer to delineate accurate cell boundaries of the encoded data presented from the pulse position detector. An on chip current mode, DAC, is used to set the ICO center frequency as a function of the nominal frequency of a particular zone.

Training mode is entered upon deassertion of RDGATE. After entering training mode, the harmonic phase detector is deactivated, and the non-harmonic phase detector is used to lock the PLL to the frequency of the REFCLK input.

During training mode, any frequency difference between the REFCLK input and the ICO output frequency causes the voltage on VF1 to be slewed monotonically in the correct direction until the frequency difference is eliminated. The REFCLK input and the center frequency of the PLL should be set to a frequency consistent with the particular zone frequency about to be read off the media.

The first data transition following the assertion of RDGATE ends training mode and initiates a zero phase start. For zero phase start, the ICO is halted until the next rising edge of the data from the pulse position detector is received. At this time, the ICO is restarted in sync with the data edge.

The data PLL has the ability to provide both a high-gain mode for fast data acquisition and a low-gain mode for data tracking after data synchronization is achieved. On the assertion of RDGATE, the PLL automatically enters the high-gain mode by employing a large magnitude charge pump connected in parallel with the small magnitude charge pump. The large magnitude charge pump provides 8 times as much charging current as the small magnitude charge pump. The high-gain mode remains in effect for 16 data transitions after the assertion of RDGATE. After 16 data transitions, the large magnitude charge pump is deactivated and low-gain data tracking mode is entered.

The dynamics of the PLL are determined by an external loop filter connected between pins VF1 and VF2. This filter can vary from a simple RC network to more complicated arrangements that permit particular damping factors, settling times, and acquisition times to be selected.

Functional Description (continued)

Table 3. Register Summary

	D7	D6	D5	D4	D3	D2	D1	D0
REG 0	0	0	DAC5	DAC4	DAC3	DAC2	DAC1	DAC0
REG 1	0	1	PRENA	SG1	SG0	ATT	PDN1	PDN0
REG 2	1	0	DIFF1	DIFF0	TST3	TST2	TST1	TST0
REG 3	1	1	EARLY2	EARLY1	EARLY0	LATE2	LATE1	LATE0

Serial Interface

The serial interface provides a means for an external processor to set and modify certain modes and functions within the device. Data is input to the device via a three-pin interface composed of SCLK, SDATA, and SEN which correspond to the serial shift clock, the serial data, and the shift enable functions.

All clocking of data occurs on the rising edge of SCLK. The polarity of SCLK is not significant and the quiescent state of SCLK (when no data is being shifted in) can be either high or low. Data will only be clocked into the device when SEN is active. The logical AND of SEN and the rising edge of SCLK is used as the internal shift register clock into the device.

Data is input to the device in 8-bit shifts with the first two bits (D7, D6) specifying one of four, 6-bit registers. For all data transfers, D7 is the first bit shifted into the device. The remaining 6 bits in each register correspond to a particular control (see Table 3).

Device Operation

RDGATE and $\overline{\text{WRGATE}}$ State Control

The following conditions are set up by the states of the RDGATE and $\overline{\text{WRGATE}}$ input pins:

1. Disk Read
   RDGATE = logic high
   $\overline{\text{WRGATE}}$ = logic high

   Characteristics:
   - Coast mode is off.
   - Fast data PLL acquire mode is on for first 16 data transitions.
   - Front-end input impedance is set at normal levels.
   - Write precompensation circuitry is powered down.

2. Idle
   RDGATE = logic low
   $\overline{\text{WRGATE}}$ = logic high

   Characteristics:
   - Coast mode is off.
   - Fast data PLL acquire mode is off.
   - Front-end input impedance is set at normal levels.
   - REFCLK used as PLL reference in non-harmonic mode write precompensation circuitry is powered down.
   - Write precompensation circuitry is powered down.

3. Disk Write
   RDGATE = logic low
   $\overline{\text{WRGATE}}$ = logic low

   Characteristics:
   - Coast mode is on.
   - Fast data PLL acquire mode is off.
   - Front-end input impedance is reduced.
   - REFCLK used as PLL reference in non-harmonic mode.

4. Reserved
   RDGATE = logic high
   $\overline{\text{WRGATE}}$ = logic low

Operating and Powerdown Modes

The operating and powerdown modes are enabled through the serial interface. The four available modes are:

1. Normal operation.
2. Same as 1 but RDCLK and RDATA output pins are forced to a logic low whenever the RDGATE input is deasserted.
3. Servo Tracking. Shut down data PLL and differentiator. RCLK and RDATA outputs forced to logic low. This permits the drive to stay on track while partially reducing power used by the device.
4. Complete powerdown of entire device.

Functional Description (continued)

Test Modes

The serial input block has 4 bits to select one of the 16 test states. These modes are used in chip test, but the parametrics are not guaranteed in operation:

Table 4. Test Mode Descriptions

Mode	Function
0	Programs the REACH1 for normal operating mode. In this mode, the TEST1 and TEST2 I/O pins are forced to a logic low.
1	Allows testing of the internal pulse detector by providing the outputs of both the differentiator and discriminator.
2	Allows testing of the harmonic phase detector by providing the output of the VCO (the ICO frequency/2) and the data synchronizer's monostable.
3	Allows testing of the data synchronizer precision monostable by providing the output of the discriminator (the input to the monostable) and the output of the monostable.
4	Allows an analog voltage to be MUXed in to replace the output of the peak detector at the inputs of the servo demodulator and the AGC charge pump circuits. A digital signal is also MUXed in to replace the output of the discrimination logic at the input of the data synchronizer monostable.
5	Identical to Test Mode 4 with the exception that the data synchronizer PLL is forced into the high-gain mode.
6	Identical to Test Mode 0 (normal operating mode) with the exception that the data synchronizer PLL is forced into the low-gain mode.
7	Identical to Test Mode 0 (normal operating mode) with the exception that the powerdown enable bits (PDN1 and PDN0) in Register 1 are redefined to select window centering offset. Powerdown operation is not possible in this mode.
8	Allows testing of the programmable current mode DAC. The data synchronizer will not operate properly in this mode. This mode also causes the inputs to the peak detector to be reversed to allow the input offsets to the pulse detector to be accurately measured.
9	Allows testing of the voltage to current converter in the data synchronizer. The data synchronizer will not operate properly in this mode.
10	A normal operating mode used in test to allow a **try before you buy** functionality test for window centering before trimming. This mode causes the powerdown enable bits (PDN1 and PDN0) in Register 2 to be redefined to control the window center trim. A digital signal is also MUXed in to replace the discriminator output as the input to the data synchronizer's monostable.
11	Identical to Test Mode 0 (normal operating mode) with the exception that current mode DAC runs at 125% of the programmed value for high-speed operation.
12	Identical to Test Mode 7 (normal operating mode with margining enabled) with the exception that an analog signal is MUXed in to replace the discriminator output as the input to the data synchronizer's monostable. This allows the measurement of window shift percentages. The VGA input is also squelched to allow measurement of the servo interface offsets.
13	Identical to Test Mode 7 (an operating mode with margining enabled) with the exception that the data synchronizer's monostable output is available and the REFCLK is internally MUXed out to the RDCLK pin when RDGATE is low.
14	Identical to Test Mode 0 (an operating mode) with the exception that the data synchronizer's monostable output is available.
15	Identical to Test Mode 13 (an operating mode) with the exception that margining is not enabled.

Functional Description (continued)

Window Margining

When window margining is enabled, small additional charge pumps are turned on when data pulses are present to offset the window from its normal position. The margining circuitry can be programmed by means of the serial interface to shift the window +3%, −3%, +6% or −6%. Window margining is included to provide data recovery and test capability.

Register Description

Register 0

Table 5. Register 0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	DAC5	DAC4	DAC3	DAC2	DAC1	DAC0

DAC5—0

These bits set the nominal center frequency of the oscillator in the data synchronizer. They also determine the coarse frequency which affects the PLL open loop gain, the droop rate of the peak detector, the nominal gain of the differentiator, and the time constant of the low-pass filter in the track and hold cells. The center and coarse frequencies corresponding to the setting of the DAC5—0 bits are given in Table 5.

These bits will provide for continuous frequency operation between 10 MHz and 60 MHz, although only 30 Mbit/s maximum (45 MHz symbol rate with RLL 1,7 data encoding) operation is supported at this time. The coarse center frequency number from the table is used to define a ratio called a which is equal to:

$$\alpha = \frac{\text{coarse center frequency programmed}}{39\ \text{MHz}}$$

α is used to generate a series of PLL gains, T/H time constants, and differentiator gains which are a function of the setting of DAC5—0. Refer to the individual ac specifications for this dependency.

Power-on reset will force the DAC5—0 bits in this register to 001111, which corresponds to a 16.87 MHz center frequency.

Functional Description (continued)

Table 6. Center Frequency Control Bits

DAC5—0	Center Frequency	Coarse C.F.
000000	10.00 MHz	11.96 MHz
000001	10.46 MHz	11.96 MHz
000010	10.92 MHz	11.96 MHz
000011	11.37 MHz	11.96 MHz
000100	11.83 MHz	11.96 MHz
000101	12.29 MHz	11.96 MHz
000110	12.75 MHz	11.96 MHz
000111	13.21 MHz	11.96 MHz
001000	13.66 MHz	11.96 MHz
001001	14.12 MHz	11.96 MHz
001010	14.58 MHz	17.12 MHz
001011	15.04 MHz	17.12 MHz
001100	15.50 MHz	17.12 MHz
001101	15.95 MHz	17.12 MHz
001110	16.41 MHz	17.12 MHz
001111	16.87 MHz	17.12 MHz
010000	17.33 MHz	17.12 MHz
010001	18.02 MHz	17.12 MHz
010010	18.70 MHz	17.12 MHz
010011	19.39 MHz	17.12 MHz
010100	20.08 MHz	17.12 MHz
010101	20.76 MHz	24.49 MHz
010110	21.45 MHz	24.49 MHz
010111	22.14 MHz	24.49 MHz
011000	22.82 MHz	24.49 MHz
011001	23.51 MHz	24.49 MHz
011010	24.20 MHz	24.49 MHz
011011	24.89 MHz	24.49 MHz
011100	25.57 MHz	24.49 MHz
011101	26.26 MHz	24.49 MHz
011110	26.95 MHz	24.49 MHz
011111	27.63 MHz	24.49 MHz

DAC5—0	Center Frequency	Coarse C.F.
100000	28.32 MHz	24.49 MHz
100001	29.24 MHz	24.49 MHz
100010	30.15 MHz	35.05 MHz
100011	31.07 MHz	35.05 MHz
100100	31.98 MHz	35.05 MHz
100101	32.90 MHz	35.05 MHz
100110	33.82 MHz	35.05 MHz
100111	34.73 MHz	35.05 MHz
101000	35.65 MHz	35.05 MHz
101001	36.56 MHz	35.05 MHz
101010	37.48 MHz	35.05 MHz
101011	38.40 MHz	35.05 MHz
101100	39.31 MHz	35.05 MHz
101101	40.23 MHz	35.05 MHz
101110	41.14 MHz	35.05 MHz
101111	42.06 MHz	35.05 MHz
110000	42.98 MHz	50.16 MHz
110001	44.13 MHz	50.16 MHz
110010	45.27 MHz	50.16 MHz
110011	46.41 MHz	50.16 MHz
110100	47.56 MHz	50.16 MHz
110101	48.71 MHz	50.16 MHz
110110	49.85 MHz	50.16 MHz
110111	51.00 MHz	50.16 MHz
111000	52.14 MHz	50.16 MHz
111001	53.29 MHz	50.16 MHz
111010	54.43 MHz	50.16 MHz
111011	55.58 MHz	50.16 MHz
111100	56.72 MHz	50.16 MHz
111101	57.89 MHz	50.16 MHz
111110	59.01 MHz	50.16 MHz
111111	60.16 MHz	50.16 MHz

Functional Description (continued)

Register 1

Table 7. Register 1

D7	D6	D5	D4	D3	D2	D1	D0
0	1	PRENA	SGI	SG0	ATT	PDN1	PDN2

PRENA

This bit, when set to a logic 1, will enable the write precompensation logic to advance or delay the write data. When set to a logic 0, the write precompensation logic is disabled.

SG1—0

These two bits set the servo demodulator gain as per Table 7.

Table 8. SG1—0

SG1	SG0	GAIN
1	1	2.0
1	0	2.5
0	1	3.2
0	0	4.0

PDN1, 0

The function of these two bits is dependent on the state of the TST3—0 bits. When the chip is not in Test Mode 7, 10, 12, 13, or 15, these bits define one of the four powerdown modes according to Table 8.

Table 9 PDN1—0 Mode Description

PDN1	PDN0	Mode Description
0	0	Normal operation.
0	1	Normal operation but force RCLK and RDATA outputs low during deassertion of $\overline{\text{RDGATE}}$.
1	0	Track Mode. Shut Down the data PLL and the differentiator and force RCLK and RDATA to a logic low.
1	1	Complete powerdown of entire device.

When the chip is programmed for Test Mode 7, 12, 13, or 15, these bits define the amount of window margining (window center offset) available for data recovery:

Table 10. PDN1—0 Window Offset

PDN1	PDN0	Window Offset
0	0	+6% (late)
0	1	+3% (late)
1	0	–3% (early)
1	1	–6% (early)

ATT

When set equal to 1, this bit will cause an additional 10 dB attenuator to be switched in before the input to the VGA at the CH+, CH– input pins to permit handling of large amplitude input signals. When set equal to 0, the attenuator is switched out.

Power-on reset will force this register to the value 000011, which will place the device in a complete powerdown mode.

Register 2

Table 11. Register 2

D7	D6	D5	D4	D3	D2	D1	D0
1	0	DIFF1	DIFF0	TST3	TST2	TST1	TST0

DIFF 1, 0

These two bits permit the gain of the differentiator to be fined tuned around the nominal value used for a given PLL center frequency according to Table 8.

Table 12. DIFF 1, 0

Gain Adjustment	DIFF1	DIFF0
No Adjustment	0	0
+3 dB	0	1
–3 dB	1	0
No Adjustment	1	1

Functional Description (continued)

TST3—0

These four bits define one of 16 test modes. In each case, the TEST1 and TEST2 pins function as per Table 13. The bits in this register are set to 0 by power-on reset. Refer to Table 4 for Test Mode definitions.

Table 13. TST3—0

		TEST1 Pin		TEST2 Pin	
TST3—0	Test Mode	I/O	Description	I/O	Description
0000	0	O	forced low	O	forced low
0001	1	O	differentiator's comparator output	O	discriminator's comparator output
0010	2	O	divided ICO output	O	monostable output
0011	3	O	discrimination logic output (monostable input)	O	monostable output
0100	4	I	analog input source for peak detector	I	digital input source for monostable
0101	5	I	analog input source for peak detector	I	digital input source for monostable
0110	6	O	forced low	O	forced low
0111	7	O	forced low	O	forced low
1000	8	O	current mode DAC output	O	forced low
1001	9	O	V to I converter current out	O	forced low
1010	10	O	force low	I	digital input source for monostable
1011	11	O	force low	O	forced low
1100	12	O	force low	I	digital input source for monostable
1101	13	O	monostable output	O	forced low
1110	14	O	monostable output	O	forced low
1111	15	O	monostable output	O	forced low

Functional Description (continued)

Register 3

Table 14. Register 3

D7	D6	D5	D4	D3	D2	D1	D0
1	1	EARLY2	EARLY1	EARLY0	LATE2	LATE1	LATE0

EARLY2—0

These three bits define one of eight settings which will advance the write data relative to uncompensated write data according to Table 14.

LATE2—0

These three bits define one of eight settings which will delay the write data relative to uncompensated write data according to Table 14.

Table 15. EARLY/LATE2—0

LATE2 EARLY2	LATE1 EARLY1	LATE0 EARLY0	Advance or Delay (ns)
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Value	Units
Storage Temperature	–65 to +120	°C
Junction Temperature	120	°C
Supply Voltage	6.5	V

Electrical Characteristics

Specifications in Table 15 refer to the device as a whole.

Table 16. General Specifications

Parameter	Conditions	Min	Nom	Max	Unit
Supply dc Voltage	—	4.75	5	5.25	V
Supply Noise	—	TBD	—	—	—
Ambient Temperature	—	0	—	70	°C
V_{IH}	—	2.0	—	—	V
V_{IL}	—	—	—	0.8	V
V_{OH}	Sourcing 1 mA	0.6	—	—	V
V_{OL}	Sinking 1 mA	—	—	0.4	V
Rise and Fall Times	At rated load. 10% to 90%	—	—	5	ns
Digital Input Leakage Current	Except for COAST, which is a 50 µA pull-up	–1	—	1	µA
Capacitive Load on Outputs	—	—	—	15	pF
Input Capacitance	—	—	—	4	pF
Power Dissipation	Read mode, 4T Pattern, 5 V supply, 39 MHz REFCLK rate, PDN1, 0 = 00	—	—	230	mW
Power Dissipation	Write mode, 4T Pattern, 5 V supply, 39 MHz REFCLK rate, PDN1, 0 = 00	—	—	255	mW
Power Dissipation	Write mode, 4T Pattern, 5 V supply, 39 MHz REFCLK rate, PDN1, 0 = 01	—	—	225	mW
Power Dissipation	Track mode, 4T Pattern, 5 V supply, PDN1, 0 = 10	—	—	110	mW
Power Dissipation	Powerdown mode, 5 V supply, PDN1, 0 = 11			25	mW
Startup Time from Powerdown Mode	*	—	—	100	µs
Startup Time from Track Mode	*	—	—	100	µs

* Specified values (TBD) of AGC cap and PLL cap external components.

Electrical Characteristics (continued)

AGC Specifications

Table 17. dc AGC Specifications

Parameter	Conditions	Min	Nom	Max	Unit
Input Offset	—	–8	0	8	mV
Differential Input Impedance	$\overline{\text{WRGATE}}$ high	0.8 x 4	4	1.2 x 4	kΩ
Differential Input Impedance	$\overline{\text{WRGATE}}$ low	200	—	400	Ω
Gain	ATT = 0*	18	—	36	dB
Gain	ATT = 1*	8	—	26	dB
Input Signal Level	ATT = 0*	—	—	225	mV p-p
Input Signal Level	ATT = 1*	—	—	700	mV p-p
Output Signal Level	For rated THD*	—	—	2	V p-p
THD	8 MHz input frequency*	—	1	2	%
Peak Detector Gain	From PI, NI to VPK	0.9	1	1.1	p/(p-p)
AGC Reference Voltage	Developed on VPK in closed loop	0.96 x 1.4	1.4	1.04 x 1.4	V
VAGC Leakage	During COAST	–50	—	50	nA
Control Transimpedance	—	0.85 x 15	15	1.15 x 15	kΩ
RZI	Magnitude of resistive part of external impedance across ZI1 and ZI2	500	—	—	Ω
CZI	Magnitude capacitive loading on ZI1 and ZI2	—	—	2	pF

* 300 Ω loads from PO, NO to V_{DD}; 500 Ω ZI.

Table 18. ac AGC Specifications

Parameter	Conditions	Min	Nom	Max	Unit
–3 dB BW	3 pF total external load on PO and on NO	40	45	—	MHz
Reflected Input Noise	Max VGA Gain	—	—	18	nV/rt-Hz
Gain Decay Time	50% drop in level of 4T signal, DAC bits set for 39 MHz center frequency, (TBD) value for CAGC: to 85%	—	—	10	µs
Gain Decay Time	50% drop in level of 4T signal, DAC bits set for 39 MHz center frequency, (TBD) value for CAGC: to 95%	—	—	14	µs
Gain Attack Time	$\overline{\text{WRGATE}}$ deasserted, initial gain setting 2x correct value, 4T signal, DAC bits set for 39 MHz center frequency, (TBD) value for CAGC: to 115%	—	—	10	µs
Gain Attack Time	$\overline{\text{WRGATE}}$ deasserted, initial gain setting 2x correct value, 4T signal, DAC bits set for 39 MHz center frequency, (TBD) value for CAGC: to 105%	—	—	14	µs
Extended $\overline{\text{WRGATE}}$	Internal $\overline{\text{WRGATE}}$ asserted after $\overline{\text{WRGATE}}$ input released	1		2	µs

Electrical Characteristics (continued)

Embedded Servo Interface Specifications

Table 19. dc Servo Interface Specifications

Parameter	Conditions	Min	Nom	Max	Unit
T&H Gain Error	—	-2	—	2	%
T&H Offset	Tracking	-10	—	10	mV
T&H Offset	Hold Pedestal	-10	—	10	mV
T&H Differential Offset	Tracking Offset + Hold Pedestal	-15	—	15	mV
Analog Output Buffer Drive (BA, BB, VPK)	Current	-150	—	150	µA
Analog Output Buffer Drive (BA, BB, VPK)	Capacitance	—	—	20	pF

Table 20. ac Servo Interface Specifications

Parameter	Conditions	Min	Nom	Max	Unit
Peak Detector Acquisition Time	To 90%; <12 pF load on VPK; 3T pattern	—	—	250 + 80/α	ns
Peak Detector Droop Time	Time for 90% droop; <12 pF load on VPK; 3T pattern; Amplitude drop to 65%; FDROOP = LOW	100 + 650/α	—	200 + 1000/α	ns
Peak Detector Droop Time	Time for 90% droop; <12 pF load on VPK; 3T pattern; Amplitude drop to 65%; FDROOP = HIGH	100 + 195/α	—	200 + 300/α	ns
T&H BW	Track Mode	-25%	alpha x TBD	25%	MHz
T&H Droop Rate	—	-25	—	25	V/s
Differential T&H Droop Rate	—	-5	—	5	V/s
Analog Output Buffer Bandwidth	12 pF load	2	—	6	MHz

Note: $\alpha = \frac{\text{coarse center frequency programmed}}{39\ \text{MHz}}$

Electrical Characteristics (continued)

Pulse Detector Specifications

Table 21. dc Pulse Detector Specifications

Parameter	Conditions	Min	Nom	Max	Unit
Input Offset	—	–10	—	10	mV
Input Impedance	—	—	4	—	kΩ
Discrimination Level	% of VPK voltage required to trip discrimination comparator. DC input: PI – NI = 0.6 V	96	—	104	%

Table 22. ac Pulse Detector Specifications

Parameter	Conditions	Min	Nom	Max	Unit
Generated Jitter 1 Sigma	Sinusoidal input 1 V to 1.5 V p-p at 1/4 nominal center frequency	—	—	$100/\sqrt{\alpha}$	ps
Pattern Dependant Generated Jitter	1 V to 1.5 V p-p signal consisting of repeating pattern: (6 0s) + (>5 2T)	—	—	$200/\sqrt{\alpha}$	ps
Pulse Pairing, Nominal Differentiator Gain Setting	Sinusoidal input 1 V to 1.5 V p-p at 1/4 nominal center frequency	—	—	$600/\sqrt{\alpha}$	ps
Pulse Pairing, High Differentiator Gain Setting	Sinusoidal input 1 V to 1.5 V p-p at 1/4 nominal center frequency	—	—	$500/\sqrt{\alpha}$	ps
Pulse Pairing, Low Differentiator Gain Setting	Not supported	—	—	—	ps
Delay Mismatch	Between discriminator comparator and differentiator comparator	15	10	0	ns

Note: $\alpha = \frac{\text{coarse center frequency programmed}}{39\ \text{MHz}}$

Electrical Characteristics (continued)

Data Synchronizer

Table 23. ac Data Synchronizer Specifications

Parameter	Conditions	Min	Nom	Max	Unit
Zero-phase Start Error (initial)	Phase error of 1—5 RDATA output rising edges from final settled phase; 3T pattern*	–2	—	2	ns
Zero-phase Start Error	Phase error of 6—30 RDATA output rising edges from final settled phase; 3T pattern*	–1.5	—	1.5	ns
Zero Phase Start Error	Phase error of 30—final RDATA output rising edges from final settled phase; 3T pattern*	–1	—	1	ns
Oscillation Frequency Range	Around specified center frequency	±10	—	—	%
PLL Open Loop Gain: $K_O \times I_p$	Low-gain mode	0.8 x α x 4.3	—	1.2 x α x 4.3	k-rad/ (Ω x s)
PLL Open Loop Gain: $K_O \times I_p$	High-gain mode	0.8 x α x 39	—	1.2 x alpha x 39	k-rad/ (Ω x s)
Generated Jitter 1 Sigma	3T Pattern*	—	—	$200/\sqrt{\alpha}$	ps
Generated Jitter1 Sigma	Valid (1, 7) or (2, 7) coded data*	—	—	$300/\sqrt{\alpha}$	ps
Window Centering Error	—	—	—	$0.3 + 0.5/\alpha$	ns
Window Closure	3T Pattern, measured at BER = 0.26%*	—	—	$6 \times 180/\sqrt{\alpha}$	ns
Delay Error	—	—	—	$1 + 0.77/\alpha$	ns
RDCLK Duty Cycle	Measured at the 2.5 V level	40	—	60	%
t_R, t_F Rise and Fall Time for RDCLK and RDATA	CL = 15 pF; 0.5 V level to 4.5 V level	—	—	5	ns
REFCLK Duty Cycle	Measured at the 1.5 V level	30	50	70	%
REFCLK Frequency	—	10	—	45	MHz

* Specified (TBD) loop filter.

Note: $\alpha = \frac{\text{coarse center frequency programmed}}{39\ \text{MHz}}$

Electrical Characteristics (continued)

AC Write Precompensation

Table 24. ac Write Precompensation Specifications

Parameter	Conditions	Min	Nom	Max	Unit
Powerup Time	From activation of WRGATE to fully operational.	—	—	150	ns
Early or Late Setup Time	—	10	—	—	ns
Early or Late Hold Time	—	5	—	—	ns
Precompensation Error	—	−10% − 0.1	—	10% + 0.1	ns
WRDOUT Pulse Widths	Active-low	15	—	30	ns
WRDOUT Falling-edge Jitter	With respect to WRDATA rising edges	—	—	±300	ps

Timing Characteristics

Read Data Output Specifications

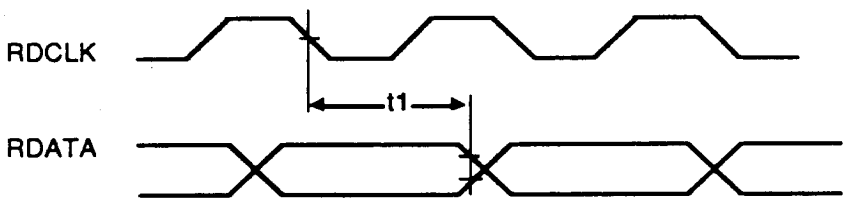


Figure 4. Read Data Output Timing Diagram

Table 25. Read Data Output Timing

Symbol	Parameter	Min	Nom	Max	Units
t1	RDATA Hold Time, CL = 10 pF, 2.0 V level of RDCLK to 0.8 V or 2.0 V level of RDATA	0	—	5	ns

Timing Characteristics (continued)

Write Precompensation Specifications

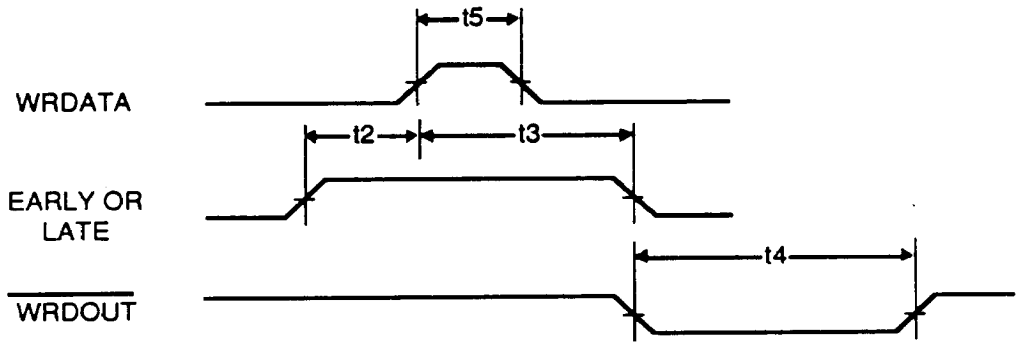


Figure 5. Write Precompensation Timing Diagram

Table 26. Write Precompensation Timing

Symbol	Parameter	Min	Nom	Max	Units
t2	2.0 V Level of WRDATA to 0.8 VLevel of EARLY or LATE Setup Time	10	—	—	ns
t3	2.0 V Level of WRDATA to 0.8 V Level of EARLY or LATE Hold Time	5	—	—	ns
t4	2.0 V Level of $\overline{\text{WRDOUT}}$ Pulse Width	15	—	30	ns
t5	2.0 V Level of WRDATA Pulse Width	10			ns

Serial Input Specifications

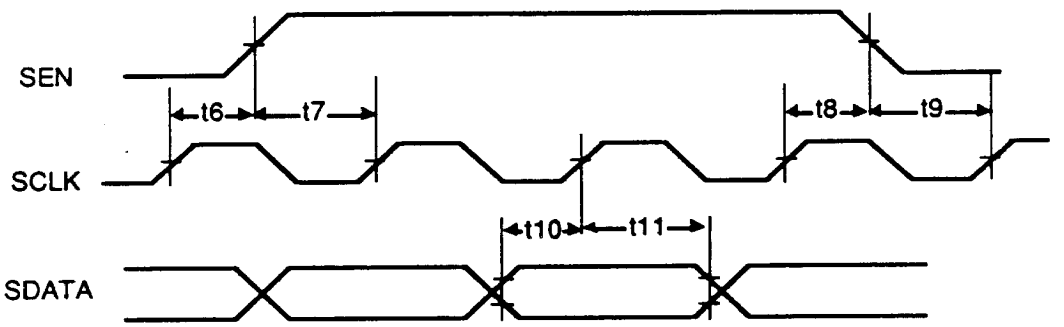


Figure 6. Serial Input Timing Diagram

Table 27. Serial Input Timing

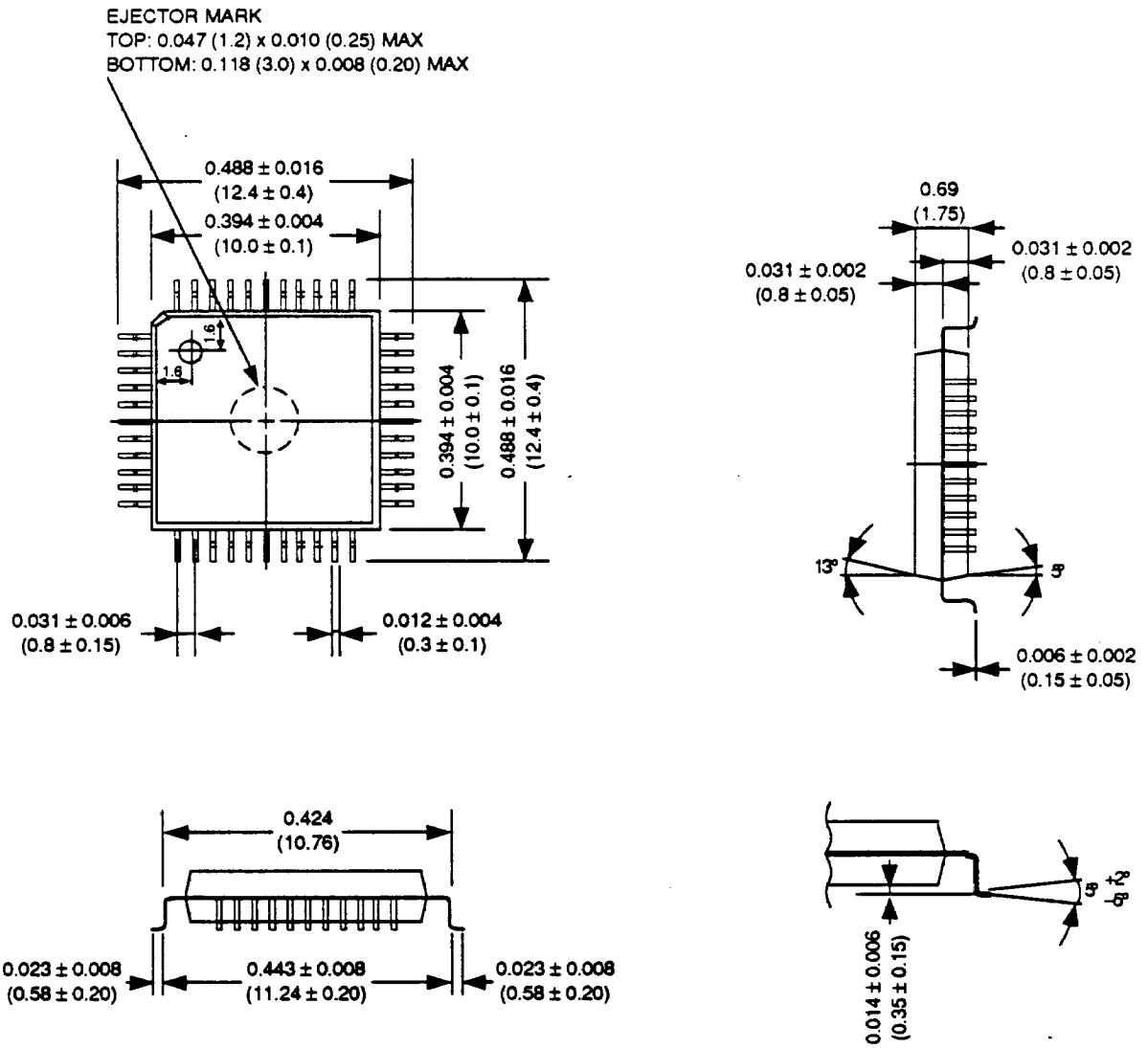
Symbol	Parameter	Min	Nom	Max	Units
t6	2.0 V Level of SCLK to 0.8 V Level of SEN	10	—	—	ns
t7	2.0 V Level of SEN to 2.0 V Level of SCLK	10	—	—	ns
t8	2.0 V Level of SCLK to 0.8 V Level of SEN	10	—	—	ns
t9	0.8 V Level of SEN to 2.0 V Level of SCLK	10	—	—	ns
t10	2.0 V or 0.8 V Level of SDATA to 0.8 V Level of SCLK	10	—	—	ns
t11	2.0 V Level of SCLK to 2.0 V or 0.8 V Level of SDATA	0	—	—	ns

Outline Diagrams

44-pin EIAJ PQFP

Dimensions are in inches and (millimeters).

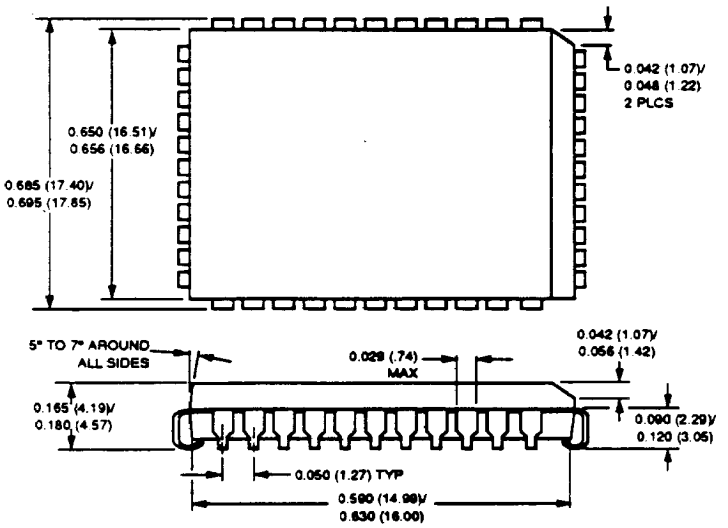
Note: These dimensions refer to the package supplied by Shinko. AT&T will be providing this package in the near future. The dimensions for the AT&T package may differ from those shown below.



Outline Diagrams (continued)

44-pin PLCC

Dimensions are in inches and (millimeters).



Ordering Information

Part	Part Number
44-pin PLCC	ATT91C010-30M44
44-pin EIAJ PQFP	ATT91C010-30J44

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