RPT-82/RPT-83

FEATURES

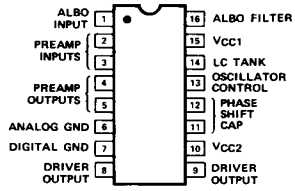
- **Automatic ALBO Function**
- **Clock-Shutdown Circuit (RPT-83)**
- **Low-Power Operation (100mW)**
- **Pin Compatible with XR-C277**

GENERAL DESCRIPTION

The RPT-82/83 are integrated circuits that perform the active functions required for regenerative PCM repeaters. They can operate from less than 100kHz to greater than 3MHz. In PCM systems, information is transmitted by the presence or absence of bipolar pulses in specified time slots. The RPT-82/83 repeaters automatically adjust gain to optimize signal levels, determine if a pulse is present or not, and retransmit the reconstructed pulses.

The difference between the RPT-82 and the RPT-83 is that the RPT-83 contains a **clock-shutdown circuit**. This shutdown circuit senses the incoming signal level and disables the clock drive if the incoming signal is below the level where accurate reconstruction is possible. This prevents noise or cross-talk from appearing as a valid signal that would be retransmitted.

PIN CONNECTIONS & ORDERING INFORMATION

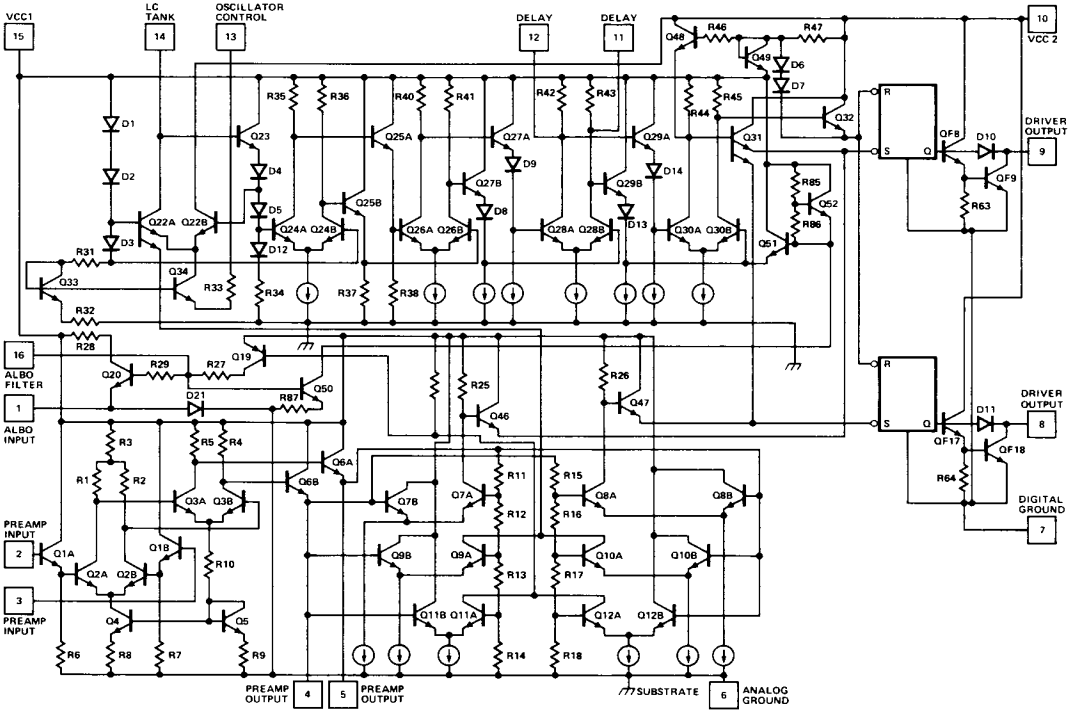


16-PIN HERMETIC DIP (Q-Suffix)

16-PIN SO (S-Suffix)

HERMETIC DIP	SO
RPT82FQ	RPT82FS
RPT83FQ	RPT83FS

RPT-83 SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Pin 10 to Pin 7 or 6 ..... ±16.0V, –0.2V
Pin 15 to Pin 7 or 6 ..... 8.0V, –0.2V
Maximum Voltage at Pins 8 or 9 ..... 30V, –0.2V
Maximum Voltage at Pins 2, 3, 4, 5, 11, 12, 14 ..... V_{CC2}
Maximum Sinking Current at Pin 8 or 9 ..... 300mA
Operating Temperature Range ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Lead Solding Temperature ..... 300°C

Junction Temperature ..... 150°C

PACKAGE TYPE	Θ_{jA} (Note 1)	Θ_{jC}	UNITS
16-Pin Hermetic DIP (Q)	100	16	°C/W
16-Pin SO (S)	111	35	°C/W

NOTES:
1. Θ_{jA} is specified for worst case mounting conditions, i.e., Θ_{jA} is specified for device in socket for CerDIP package; Θ_{jA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS

at $V_{CC1} = 4.4V$, $V_{CC2} = 6.8V$, $-40°C \le T_A \le +85°C$, unless otherwise noted. $V_{PIN\ 6} = V_{PIN\ 7} = V_{PIN\ 13} = GND$.

PARAMETER	SYMBOL	CONDITIONS	RPT-82/RPT-83 MIN	TYP	MAX	UNITS
SUPPLY						
Supply Current	I_{CC1}	$T_A = +25°C$ (Note 1)	5.0	8.5	9.5	mA
Supply Current	I_{CC2}	$T_A = +25°C$ (Note 1)	1.0	2.5	3.5	mA
Total Supply Current	$I_{CC1} + I_{CC2}$	$T_A = +25°C$ (Note 1)	6	11	13	mA
PREAMPLIFIER						
Preamplifier Open-Loop Gain $\frac{\Delta V_{PIN\ 5}}{\Delta V_{PIN\ 2}}$	A_o	Measure $\Delta V_{Pin\ 2}$ necessary to change pins from 1.9V to 3.2V	44	48	51	dB
Preamplifier Bandwidth	B_W	3dB Points (Note 2)	3	5	–	MHz
Preamplifier Input Impedance	Z_{IN}		–	600	–	kΩ
Preamplifier Input Offset Voltage	V_{OS}	$V_{PIN\ 2} - V_{PIN\ 3}$ (Note 1)	–	1	15	mV
Preamplifier Output Impedance	Z_{OUT}	(Note 2)	–	80	150	Ω
Preamplifier Output High	V_{OHA}	$V_{PIN\ 4}$ with $V_{PIN\ 2} = 2.5V$, $V_{PIN\ 3} = 2.7V$, $T_A = +25°C$	3.35	3.45	3.75	V
Preamplifier Output Low	V_{OLA}	$V_{PIN\ 4}$ with $V_{PIN\ 2} = 2.5V$, $V_{PIN\ 3} = 2.3V$, $T_A = +25°C$	1.0	1.4	1.45	V
Preamplier Input Bias Current	I_B	$I_{PIN\ 2}$ or $I_{PIN\ 3}$ (Note 1)	–	1	4	µA
Preamplifier Input Offset Current	I_{OS}	$I_{PIN\ 2} - I_{PIN\ 3}$ (Note 1)	–	0.05	2	µA
OUTPUT DRIVE						
Output Voltage Swing	V_{OP}	$V_{PIN\ 8\ High} - V_{PIN\ 8\ Low}$, $V_{PIN\ 9\ High} - V_{PIN\ 9\ Low}$	–	6	–	V
Output Voltage, Low	V_{OL}	$T_A = +25°C$, $I_{LOAD} = 15mA$	0.5	0.8	1.1	V
Differential Output Voltage, Low	V_{OLD}	$T_A = +25°C$, $I_{LOAD} = 15mA$	–	0.02	0.15	V
Output Leakage Current	I_{OH}	$V_{PIN\ 14} = 4.9V$, $V_{PIN\ 8} = V_{PIN\ 9} = 20V$, (Note 1) $T_A = +25°C$	–	0.05	50	µA
Output Pulse Rise-Time	T_{OS}	(Note 2)	–	30	50	ns
Output Pulse Fall-Time	T_{OF}	(Note 2)	–	10	60	ns
Output Pulse Width	P_W	At f = 1.544MHz	–	324	–	ns
Pulse-Width Differential	P_{WD}	(Note 2)	–	3	12	ns
Bipolar Violations at Maximum Density	BV_1 MAX		–	0	–	–
Bipolar Violations with Quasi-Random Input Pattern	BV_R MAX		–	0	–	–
CLOCK CIRCUIT						
Tank Emitter-Follower Base Current	I_{TB}	$I_{PIN\ 14}$, $VP_{IN\ 14} = 4.9V$ (Note 1)	–	4	15	µA
Tank Input Impedance	Z_{INT}	Measured from pin 14 to pin 15	–	300	–	kΩ
Oscillator Bias Current	I_{OSC}	$V_{PIN\ 14} = 3.9V$ ($I_{OSC} - I_{TB}$) (Note 1)	10	30	50	µA
Oscillator Injection Current	I_{INJ}	Set $V_{PIN\ 4} - V_{PIN\ 5} \pm 1.4V$, $V_{PIN\ 14} = 3.9V$ ($I_{INJ} - I_{OSC}$)	60	160	190	µA
Delay Circuit Resistor	R_d	Measured from pin 11 or pin 12 to pin 15, $T_A = +25°C$	3.2	4.0	4.8	kΩ

ELECTRICAL CHARACTERISTICS at $V_{CC1} = 4.4V$, $V_{CC2} = 6.8V$, $-40°C \leq T_A \leq +85°C$, unless otherwise noted. $V_{PIN\,6} = V_{PIN\,7} = V_{PIN\,13} = GND$. *Continued*

PARAMETER	SYMBOL	CONDITIONS	RPT-82/RPT-83 MIN	TYP	MAX	UNITS
MISCELLANEOUS						
ALBO Threshold	V_{TA}	Differential voltage, measured between pins 4 and 5, required to activate the Peak Detector. $T_A = +25°C$	1.35	1.5	1.65	V
Clock Threshold	V_{TC}	Differential voltage, measured between pins 4 and 5, required to activate the Data Detector $T_A = +25°C$	0.85	1.0	1.2	V
Data Threshold	V_{TL}	Differential voltage, measured between pins 4 and 5, required to activate the Data Detector $T_A = +25°C$	0.65	0.75	0.85	V
Clock Threshold as % of ALBO Voltage	$V_{TC\%}$	$T_A = +25°C$	67	73	78	%
Data Threshold as % of ALBO Voltage	$V_{TL\%}$	$T_A = +25°C$	46	54	58	%
ALBO ON Voltage	V_{O16}	Measured at pin 16, $[V_{p4} - V_{p5}]$ = ALBO Threshold	1.0	1.7	2.5	V
ALBO OFF Voltage	V_{F16}	Measured at pin 16 and pin 1 $T_A = +25°C$	–	–	75	mV
Minimum ALBO Diode Resistance	R_D MIN		–	8	–	Ω
Maximum ALBO Diode Impedance	R_D MAX	f = 1.544MHz	–	30	–	kΩ
ALBO Gain Range	A_m	(Note 3)	36	48	–	dB

NOTES:
1. $V_{PIN}2 = 2.5V$; adjust $V_{PIN\,3}$ until $V_{PIN\,4} = V_{PIN\,5}$.
2. Sample tested.
3. Guaranteed by design.

4

FUNCTIONAL DESCRIPTION

Bipolar-pulse transmission, the transmission of alternately positive and negative pulses, is used on repeater lines to remove the DC component present in unipolar PCM pulse trains. This also places the principal energy components in the 0–1.544MHz band, as opposed to the 0–3.088MHz band for unipolar pulse trains. The absence of a DC component in bipolar pulse trains permits the repeater to be transformer-coupled to the repeater line and helps prevent time-shifting of the regenerator firing levels with variations in input pulse density (see Figure 1).

ENERGY SPECTRA OF BIPOLAR AND UNIPOLAR PULSE TRAINS

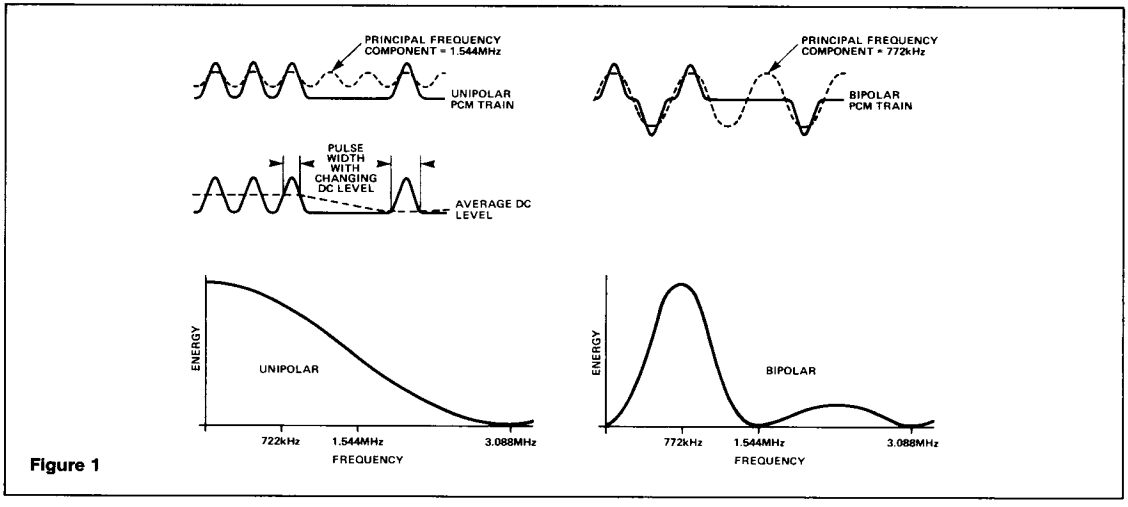


Figure 1

FUNCTIONAL BLOCK DIAGRAM

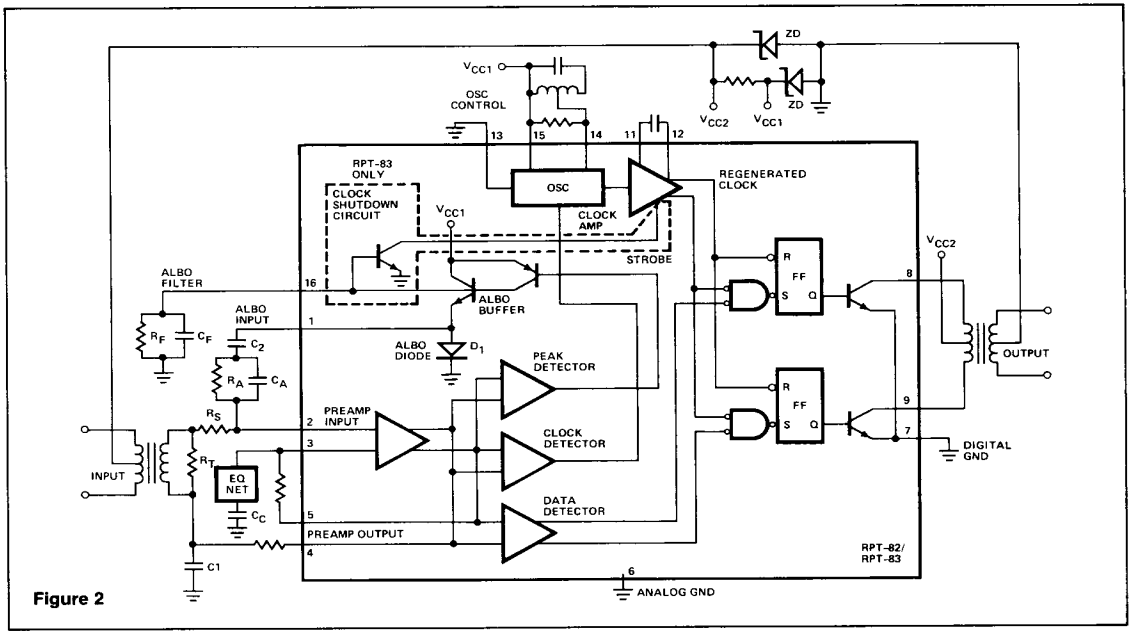


Figure 2

The bipolar-PCM pulse train is transformer-coupled into the preamplifier as shown in the functional block diagram (Figure 2). The secondary of the input transformer is loaded with the proper terminating resistor, R_T, to match the line impedance. One side of the transformer secondary is AC-coupled to ground by capacitor C1; the other side of the secondary winding is in series with resistance R_S. Resistor R_S and the RC network R_AC_A are AC-coupled to the ALBO input by capacitor C2. The impedance of the ALBO (Automatic Line Build-Out) input to ground is governed by the amount of current through the ALBO diode. R_S, in series with R_AC_A, provides signal attenuation proportional to the current flowing through the ALBO diode. When minimum current flows through the ALBO diode, C2 is effectively isolated from ground and the input signal attentuation is minimal. The ALBO diode range of 8Ω to 30kΩ provides compensation for line losses of approximately 5dB to 41dB.

The preamplifier stage amplifies the input signal and applies it to the three comparators labeled **data detector, clock detector,** and **peak detector,** respectively. Each comparator provides an output whenever the signal exceeds the trip point on both positive and negative pulses. Each comparator trips at a different threshold. The data detector is set to trip at the 54% point; the clock detector trips at the 73% point; and the peak detector trips at peak amplitude. Thresholds and waveforms are shown in Figure 3.

Current pulses from the peak detector are integrated by the capacitor in the ALBO filter. This causes a relatively constant current to flow through the emitter follower and D1. In the RPT-83, a low voltage at the ALBO filter enables the clock-shutdown circuit when there is no input signal. The clock-shutdown circuit turns off the clock amplifier so that neither the regenerated clock, nor the strobe outputs, are sent to the flip-flops. This prevents the RPT-83 from sending noise or cross-talk out as valid-appearing data pulses when the incoming data level is too low.

The clock detector output locks the oscillator to the input frequency. The following amplifier stages shape the oscillator

THRESHOLDS AND WAVEFORMS

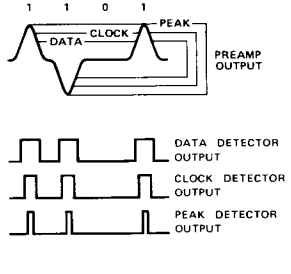


Figure 3

output and shift it in time. The phase-shift capacitor is selected to provide additional phase-shift so that the strobe pulses will occur at the center of the incoming pulses. This provides optimum timing for determining if a "1" or a "0" is present. A 0-to-30pF capacitor (10pF is typical at 1.544MHz) will optimize the performance of the complete repeater.

The delayed regenerated clock and the data-detector outputs drive the input flip-flops and output transistors. The output transistors are coupled to the transmission line through an output transformer.

DETAILED DESCRIPTION

PREAMPLIFIER

The preamplifier performs two basic functions. The first is to raise the level of the incoming signal to the correct level to trip the comparators. The second is to provide frequency/gain compensation to enhance the signal-to-noise ratio of the incoming signal. The preamp is designed to be operated in a near open-loop condition. A limited amount of feedback is used to control the frequency response. The gain-phase relationship of the preamp (see Figures 4 and 5) implies that the feedback network must have 40dB attenuation or more at 20MHz and above to ensure stability.

ALBO

To enable the preamp to operate open-loop with a wide range of signal levels, the ALBO diode is connected between the preamp input and ground. Since the ALBO-diode conductance is directly proportional to the ALBO-diode current, and the ALBO diode is driven by the peak detector, any signal in excess of that required to trip the peak detector will be shunted to ground through the ALBO diode. This automatic-gain-control function maintains the signal at the optimum level to operate the clock and data detectors.

The combination of R_S and R_A, in parallel with both C_A and the series impedance of the ALBO diode, perform the following two functions: 1) the automatic-gain-control function previously described, and 2) the frequency/phase compensation for transmission-line losses.

FREQUENCY/PHASE COMPENSATION

Frequency/phase compensation is desirable for three reasons:

1. If the bandwidth is wider than necessary, noise and cross-talk outside of the signal-frequency band will appear at the threshold detectors. Out-of-band signals increase the probability that an incorrect logic decision will be made. These incorrect logic decisions will increase the bit error rate.
2. Nonlinear phase-shifts in the transmission line may cause the signal to be distorted to the extent that bit errors occur. Phase compensation in the repeater can partly correct for this problem.
3. Large phase-shifts in the preamplifier at high frequencies can cause instability if not compensated for by the feedback network. (See Figures 4 and 5).

CLOCK DETECTOR

The clock detector drives the clock-tank circuit with a pulse each time that the incoming signal is greater than 73% of the average peak signal.

PEAK DETECTOR

The peak detector drives the ALBO buffer and ALBO diode at the peak of the amplified "1" bits. Whenever the preamp AC-signal-output exceeds about 1.5V peak-to-peak, the ALBO buffer becomes forward biased and drives current into both the ALBO diode and the ALBO filter. This closed-loop AGC action maintains the preamp input signal at about 5mVp-p.

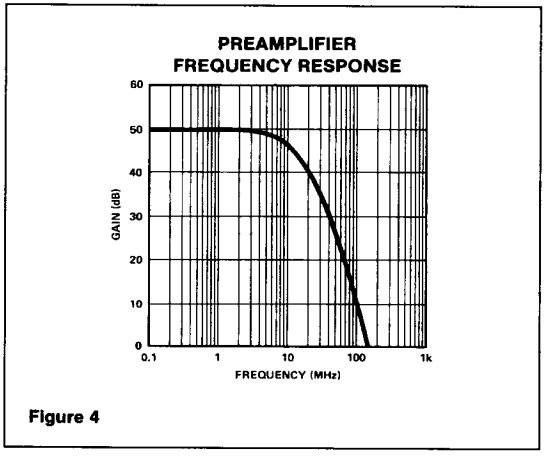


Figure 4

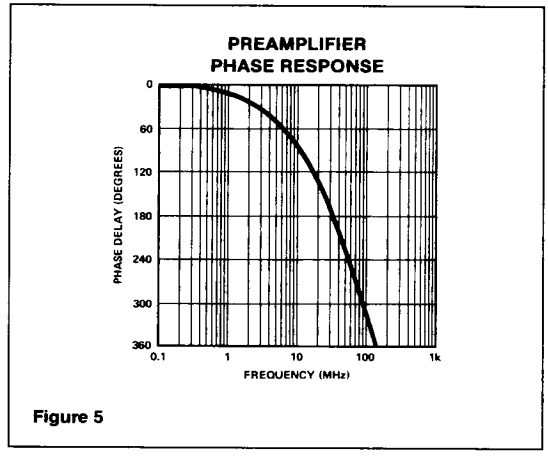


Figure 5

RPT-82/83 IN TYPICAL 1.544MHz T1 REPEATER SYSTEM

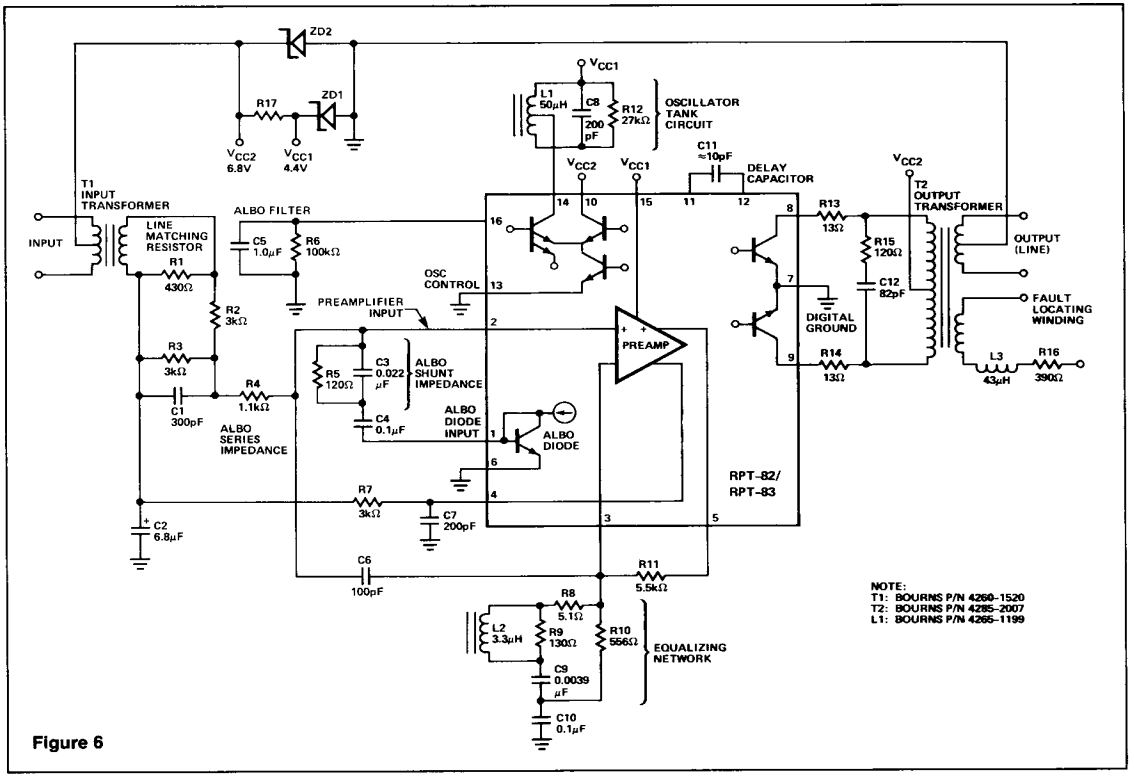


Figure 6

APPLICATION

In a typical T1, 1.544MHz repeater system (see Figure 6), the repeater is placed in series with a twisted-pair transmission line at distances of up to approximately 6000 feet. The power is supplied by a constant current of 60mA that is sent common-mode down the transmission line. This constant current is separated from the signal by input transformer T1 and output transformer T2, and is converted to voltages V_{CC1} and V_{CC2} by zener diodes Z_{D1} and Z_{D2}. The signal is coupled into the input network by T1. One end of T1 is held at AC ground by C2; and the other end is terminated by the line-matching resistor R1. The line-matching resistor is followed with a resistive attenuator consisting of R2 and R3, and the ALBO series impedance R4. The two resistors, R2 and R3, isolate the changing ALBO-diode impedance from the transmission line such that the transmission line is always correctly terminated. Resistor R4, in series with the shunt ALBO-diode impedance, determines the amount of attenuation provided at any given ALBO-diode current. Capacitor C1 provides a shunt path to ground for signals that are above the signal frequency.

When the ALBO-diode impedance is high, the ALBO series and shunt impedances have very little effect, so the unattenuated signal is applied to the preamp input with only C1 affecting the frequency response. When the ALBO-diode input impedance is reduced by higher signal levels, more of the input signal is shunted to ground through the ALBO shunt impedance.

The ALBO shunt impedance, C3 and R5, changes the input attenuation vs. frequency such that the system has more high frequency response at low signal levels, and less high frequency response at high signal levels. This change in bandwidth with signal level is intended to partially compensate for the increased high-frequency losses that occur in long transmission lines.

The bias feedback components between pin 4 and pin 2, consisting of C7, R7, and C2, operate as a DC self-biasing network. This C-R-C network prevents AC feedback and allows the preamp to establish a balanced input-and-output DC bias of 2.5 to 2.6 volts. Resistor R11 provides the DC path for biasing between pins 5 and 3.

Resistor R11 and capacitor C6 provide an AC feedback path. Resistors R10 and R11 act as an AC voltage divider that is shunted by the variable impedance of the resonant circuit comprised of L2 and C9. This frequency-selective feedback path, between pin 5 and pin 3, increases preamp gain at approximately 900kHz which further improves the system signal-to-noise ratio. The beneficial effect of the frequency-selective network is shown in Figure 7. The lower trace is a typical input signal (all 1's in this example) and the upper trace is the preamp output.

Figures 8 and 9 show the appearance of different preamp inputs measured at pin 5. Figure 8 is typical of an all 1's signal pattern with very little cross-talk or noise. Figure 9 shows a normal pattern of random 1's and 0's.

Due to the automatic-gain-control action of the ALBO circuitry, the peak amplitude is held constant for line losses of approximately 5dB to greater than 36dB. These signals are superimposed on a DC level of approximately 2.5V.

The preamp output drives the clock detector (reference Figures 2 and 6) which drives the clock-tank circuitry (L1, C8, and R12). The signal at pin 14, a sine wave of 0.2 to 1.0Vp-p (depending upon the percentage of 1-bits), drives the clock amplifier. The phase-shift capacitor, C11, provides the additional phase shift so that this integrated and phase-shifted signal (Figure 10) will strobe the output flip-flops at the optimum time to determine if a 1-bit is present. If a 1-bit is present, outputs from the data detector and the strobe cause the flip-flops to drive alternate output transistors. This signal is coupled through the output transformer into the next section of transmission line (see Figure 11, all 1's; and Figure 12, a random 1-0 pattern).

Figure 13 is a scope photograph of the signals as observed at several locations in the system. All traces are DC coupled and referenced to zero volts at the bottom graticule line. All signals, except the output, are displayed at 1-volt-per-division. The output is shown at 2-volts-per-division. The signal is all 1's. The phase relationships are typical for this type of repeater.

The signals shown are:

1. The preamp output at pin 5.
2. The clock-tank at pin 14.
3. The phase-shifted clock at pin 11.
4. The output signal at pin 8.

R13, 14, 15, and C12 control ringing and overshoot in the output waveform.

The fault-locating winding with L3 and R16 is used in long-line systems to determine which repeater, in a large series of repeaters, has become defective.

The RPT-82 and RPT-83 can be used in a variety of systems over a wide range of frequencies. The low-frequency response is limited by the difficulty in maintaining useable Q in the clock-tank circuit and by transformer-coupling losses. At high frequencies, the major limitation is the output-pulse rise-and-fall time.

The preamp is a high-gain, wide-bandwidth linear amplifier. Analog circuits do not have the noise rejection that is common with most digital circuits. To obtain best performance, certain precautions should be observed.

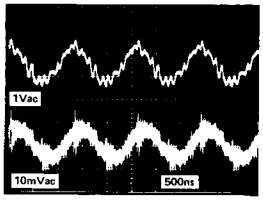


Figure 7

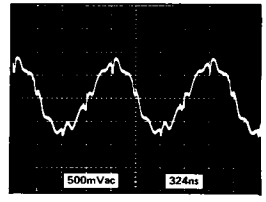


Figure 8

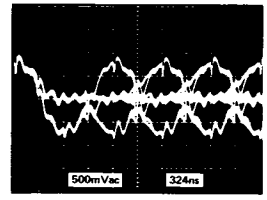


Figure 9

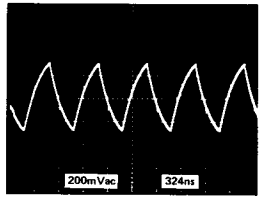


Figure 10

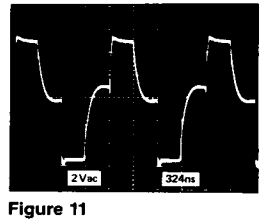


Figure 11

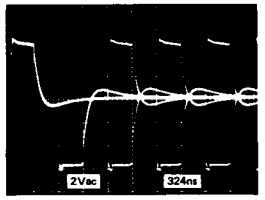


Figure 12

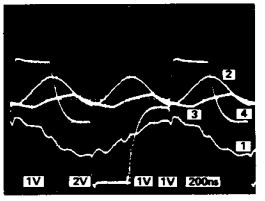


Figure 13

Circuit layout techniques used for R.F. amplifiers should be followed. Use of double-sided boards with all unused circuit-board area made into a ground plane is highly recommended. Keep input and output leads as far apart as possible, and signal runs as short as possible. Locate the attenuator network and the ALBO series impedance R4 as close to pin 2 as possible.

Power supply voltages V_{CC1} and V_{CC2} should be bypassed near pins 10 and 15. A bypass capacitor between the V_{CC2} connection on T_2 and pin 7 is also recommended.