AT&T Microelectronics

ATTL7582 Tip Ring Access Switch

Features

- Direct pin-for-pin replacement for ATTL7542
- Small size/surface-mount packaging
- Monolithic IC reliability
- No impulse noise generation
- No zero cross switching required
- Make-before-break, break-before-make operation
- Clean, bounce-free switching
- Low, matched ON-resistance
- Built-in current limiting, thermal shutdown, and SLIC protection
- 5 V only operation, very low power consumption
- Battery monitor, all off state upon loss of battery
- No EMI
- Latched logic level inputs, no drive circuitry
- Only one external protector required

Applications

- Central office
- DLC
- PBX
- DAML
- FOC/FITL

Description

The ATTL7582 Tip Ring Access Switch is a monolithic solid-state device that provides the switching functionality of a 2 form C switch. The ATTL7582 is a direct pin-for-pin replacement for the ATTL7542.

The ATTL7582 is designed to provide power ringing access to tip and ring in Central Office, Digital Loop Carrier, Private Branch Exchange, Digitally Added Main Line and Fiber Optic Coax/Fiber in the Loop analog line card applications. An additional pair of solid-state contacts provide access to the telephone loop for line test access or message waiting in the PBX application.

The ATTL7582 has four states: the idle talk state (line break switches closed, ringing and loop access switches open), the power ringing state (ringing access switches closed, line break and loop access switches open), loop access state (loop access switches closed, line break and ringing access switches open) and an "all off" state.

The ATTL7582 offers break-before-make or make-before-break switching, with simple logic level input control. Because of the solid-state construction, no impulse noise is generated when switching during ring cadence or ring trip, thus eliminating the need for external "zero cross" switching circuitry. State control is via logic level inputs so no additional driver circuitry is required.

The line break switch is a linear switch that has exceptionally low ON-resistance and an excellent ON-resistance matching characteristic. The ringing access switch has a breakdown voltage rating >480 V which is sufficiently high, with proper protection, to prevent breakdown in the presence of a transient fault condition (i.e., passing the transient on to the ringing generator).

Incorporated into the ATTL7582Axx is a diode bridge/SCR clamping circuit, current-limiting circuitry and a thermal shutdown mechanism to provide protection to the SLIC device and subsequent circuitry during fault conditions (see Figure 1). Positive and negative lightning is reduced by the current limiting circuitry and steered to ground via diodes and the integrated SCR. Power cross is also reduced by the current limiting and thermal shutdown circuits.

Description

The ATTL7582Bxx version provides only an integrated diode bridge along with current limiting and thermal shutdown as shown in Figure 2. This will cause positive faults to be directed to ground and negative faults to battery. In either polarity, faults are reduced by the current limit and/or thermal shutdown mechanisms.

To protect the ATTL7582 from an overvoltage fault condition, use of a secondary protector is required. The secondary protector must limit the voltage seen at the Tip/Ring terminals to prevent the breakdown voltage of the switches from being exceeded. To minimize stress on the solid-state contacts, use of a foldback or crowbar type secondary protector is recommended. With proper choice of secondary protection, a line card using the ATTL7582 will meet all relevant CCITT, LSSGR, FCC, or *UL* protection requirements.

The ATTL7582 operates off of a +5V supply only. This gives the device extremely low idle and active power dissipation and allows use with virtually any range of battery voltage. This makes the ATTL7582 especially appropriate for remote power applications such as DAML or FOC/FITL or other TA/TR 909 applications where power dissipation is particularly critical.

A battery voltage is also used by the ATTL7582, only as a reference for the integrated protection circuit. The ATTL7582 will enter an "all off" state upon loss of battery.

The ATTL7582 device is packaged in a 16-pin, plastic DIP package (ATTL7582AE/BE) and a 16-pin, plastic SOG package (ATTL7582AAE/BAE). The ATTL7582AAE/BAE are pin compatible with the ATTL7542AAE/BAE.

Pin Information

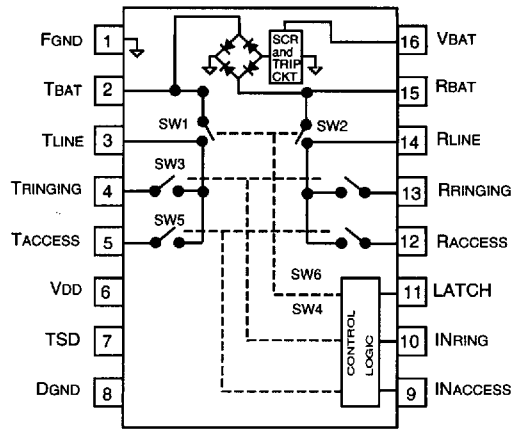


Figure 1. 16-Pin, Plastic SOG (A Version)

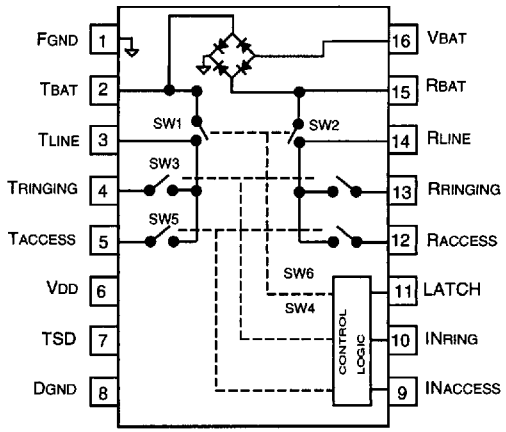


Figure 2. 16-Pin, Plastic DIP (B Version)

Pin Information

Table 1. Pin Descriptions

DIP	SOG	Symbol	Description	DIP	SOG	Symbol	Description
1	1	FGnd	Fault ground.	16	16	VBAT	Battery voltage. Used as a reference for protection circuit.
2	2	TBAT	Connect to TIP on SLIC side.	15	15	RBAT	Connect to RING on SLIC side.
3	3	TLINE	Connect to TIP on line side.	14	14	RLINE	Connect to RING on line side.
4	4	TRINGING	Connect to return ground for ringing generator.	13	13	RRINGING	Connect to ringing generator.
5	5	TACCESS	Test access.	12	12	RACCESS	Test access.
6	6	VDD	+5 V supply.	11	11	LATCH	Data latch control, active-high, transparent low.
7	7	TSD	Temperature shutdown pin. Can be used as a logic level input or output. See Truth Table and Switching section of this data sheet for input pin description. As an output, will read +5 V when device is in its operational mode and 0 V in the thermal shutdown mode. To disable the thermal shutdown mechanism, tie this pin to +5 V (**NOT** Recommended).	10	10	INRINGING	Logic level input switch control.
8	8	DGnd	Digital ground.	9	9	INACCESS	Logic level input switch control.

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods of time can adversely affect device reliability.

Table 2. Absolute Maximum Ratings Parameters

Parameter	Min	Max	Units
Operating Temperature Range	–40	110	°C
Storage Temperature Range	–40	150	°C
Relative Humidity Range	5	95	%
Pin Soldering Temperature (t = 10 s max)	—	260	C
+5 V Power Supply	—	7	V
Battery Supply	—	–85	V
Logic Input Voltage	—	7	V
Input-to-Output Isolation	—	330	V
Pole-to-Pole Isolation	—	330	V

Electrical Characteristics

T_A = –40 °C to +85 °C, unless otherwise specified.

Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluations. Typical values are for information purposes only and are not part of the testing requirements.

Power Supply Specifications

Supply	Min	Typ	Max	Unit
V_{DD}	+4.5	+5	+5.5	V
V_{BAT}*	–19	—	–72	V

* V_{BAT} is used only as a reference for internal protection circuitry.
If V_{BAT} rises above –10 V, the device will enter an all off state and will remain in the all off state until the battery voltage drops below –15 V.

Table 3. Break Switch, 1 and 2

Parameter	Test Condition	Measure	Min	Typ	Max	Unit
Off-state Leakage Current:						
+25 °C	Vswitch (differential) = –320 V to Gnd Vswitch (differential) = –60 V to +260 V	Iswitch	—	—	1	µA
+85 °C	Vswitch (differential) = –330 V to Gnd Vswitch (differential) = –60 V to +270 V	Iswitch	—	—	1	µA
–40 °C	Vswitch (differential) = –310 V to Gnd Vswitch (differential) = –60 V to +250 V	Iswitch	—	—	1	µA
ON-resistance (SW1, SW2):						
+25 °C	T_{LINE} = ±10 mA, ±40 mA, T_{BAT} = –2 V	Δ Von	—	—	19.5	Ω
+85 °C	T_{LINE} = ±10 mA, ±40 mA, T_{BAT} = –2 V	Δ Von	—	—	28	Ω
–40 °C	T_{LINE} = ±10 mA, ±40 mA, T_{BAT} = –2 V	Δ Von	—	—	14.5	Ω
ON-resistance Match	Per ON-resistance Test Condition of SW1, SW2	Magnitude R_{ON} SW1—R_{ON} SW2	—	0.2	—	Ω
dc Current Limit:	Vswitch (on) = ±10 V	Iswitch				
+85 °C			80	—	—	mA
–40 °C			—	—	250	mA
Dynamic Current Limit: (t = <0.5 µs)	Break switches in ON state, Ringing access switches OFF, Apply ± 1000 V at 10/1000 µs pulse, Appropriate secondary protection in place.	Iswitch		2.5		A
Isolation:						
+25 °C	Vswitch (both poles) = ±320 V Logic Inputs = Gnd	Iswitch	—	—	1	µA
+85 °C	Vswitch (both poles) = ±330 V Logic Inputs = Gnd	Iswitch	—	—	1	µA
–40 °C	Vswitch (both poles) = ±310 V Logic Inputs = Gnd	Iswitch	—	—	1	µA
dv/dt Sensitivity*	—	—	—	200	—	V/µs

* Applied voltage is 100 Vpp square wave at 100 Hz.

Electrical Characteristics (continued)

Table 4. Ring Return Switch, 3

Parameter	Test Condition	Measure	Min	Typ	Max	Unit
Off-state Leakage Current, (SW3):						
+25 °C	Vswitch (differential) = –320 V to Gnd V Vswitch (differential) = –60 V to +260 V	Iswitch	—	—	1	µA
+85 °C	Vswitch (differential) = –330 V to Gnd Vswitch (differential) = –60 V to +270 V	Iswitch	—	—	1	µA
–40 °C	Vswitch (differential) = –310 V to Gnd Vswitch (differential) = –60 V to +250 V	Iswitch	—	—	1	µA
dc Current Limit	Vswitch (on) = ±10 V	Iswitch	—	200	—	mA
Dynamic Current Limit: (t = <0.5 µs)	Break switches in ON state, Ringing access switches OFF, Apply ± 1000 V at 10/1000 µs pulse, Appropriate secondary protection in place.	Iswitch		2.5		A
ON-resistance	Iswitch (on) = ±0 mA, ±10 mA	Δ V_{on}	—		100	Ω
Isolation:						
+25 °C	Vswitch (both poles) = ±320 V Logic Inputs = Gnd	Iswitch	—	—	1	µA
+85 °C	Vswitch (both poles) = ±330 V Logic Inputs = Gnd	Iswitch	—	—	1	µA
–40 °C	Vswitch (both poles) = ±310 V Logic Inputs = Gnd	Iswitch	—	—	1	µA
dv/dt Sensitivity*	—	—	—	200	—	V/µs

* Applied voltage is 100 Vpp square wave at 100 Hz.

Electrical Characteristics (continued)

Table 5. Ringing Access Switch, 4

Parameter	Test Condition	Measure	Min	Typ	Max	Unit
Off-state Leakage Current, (SW3):						
+25 °C	Vswitch (differential) = −255 V to +210 V Vswitch (differential) = +255 V to −210 V	Iswitch	—	—	1	µA
+85 °C	Vswitch (differential) = −270 V to +210 V Vswitch (differential) = +270 V to −210 V	Iswitch	—	—	1	µA
−40 °C	Vswitch (differential) = −245 V to +210 V Vswitch (differential) = +245 V to −210 V	Iswitch	—	—	1	µA
ON Voltage	Iswitch (on) = ±1 mA	—	—	—	3	V
Surge Current	—	—	—	—	2	A
Release Current	—	—	100	—	500	µA
ON-resistance	Iswitch (on) = ±70 mA, ±80 mA	Δ Von	—		10	Ω
Isolation:						
+25 °C	Vswitch (both poles) = ±320 V Logic Inputs = Gnd	Iswitch	—	—	1	µA
+85 °C	Vswitch (both poles) = ±330 V Logic Inputs = Gnd	Iswitch	—	—	1	µA
−40 °C	Vswitch (both poles) = ±310 V Logic Inputs = Gnd	Iswitch	—	—	1	µA
dv/dt Sensitivity*	—	—	—	200	—	V/µs

* Applied voltage is 100 Vpp square wave at 100 Hz.

Electrical Characteristics (continued)

Table 6. Loop Access Switches, 5 and 6

Parameter	Test Condition	Measure	Min	Typ	Max	Unit
Off-state Leakage Current, (SW3):						
+25 °C	Vswitch (differential) = –255 V to +210 V Vswitch (differential) = +255 V to –210 V	Iswitch	—	—	1	µA
+85 °C	Vswitch (differential) = –270 V to +210 V Vswitch (differential) = +270 V to –210 V	Iswitch	—	—	1	µA
–40 °C	Vswitch (differential) = –245 V to +210 V Vswitch (differential) = +245 V to –210 V	Iswitch	—	—	1	µA
dc Current Limit:	Vswitch (on) = ±10 V	Iswitch				
+85 °C			80	—	—	mA
–40 °C			—	—	250	mA
Dynamic Current Limit: (t = <0.5 µs)	Break switches in ON state, Ringing access switches OFF, Apply ± 1000 V at 10/1000 µs pulse, Appropriate secondary protection in place.	Iswitch		2.5		A
ON-resistance:						
+25 °C	Iswitch (on) = ±10 mA, ±40 mA	Δ Von	—	—	45	Ω
+85 °C	Iswitch (on) = ±10 mA, ±40 mA	Δ Von	—	—	65	Ω
–40 °C	Iswitch (on) = ±10 mA, ±40 mA	Δ Von	—	—	33	Ω
ON Resistance Match	Per ON-resistance test condition of SW5, SW6	Magnitude RON SW5, RON SW6	—	—	TBD	Ω
Isolation:						
+25 °C	Vswitch (both poles) = ±320 V Logic Inputs = Gnd	Iswitch	—	—	1	µA
+85 °C	Vswitch (both poles) = ±330 V Logic Inputs = Gnd	Iswitch	—	—	1	µA
–40 °C	Vswitch (both poles) = ±310 V Logic Inputs = Gnd	Iswitch	—	—	1	µA
dv/dt Sensitivity*	—	—	—	200	—	V/µs

* Applied voltage is 100 Vpp square wave at 100 Hz.

Electrical Characteristics (continued)

Table 7. Additional Electrical Characteristics

Parameter	Test Condition	Measure	Min	Typ	Max	Unit
Digital Input Characteristics:	—	—	—	—	1.5	V
Input Low Voltage						
Input High Voltage	—	—	3.5	—	—	V
Input Leakage Current (High)	V_{DD} = 5.5 V, V_{BAT} = –75 V, Vlogicin = 5 V	Ilogicin	—	—	1	µA
Input Leakage Current (Low)	V_{DD} = 5.5 V, V_{BAT} = –75 V, Vlogicin = 0 V	Ilogicin	—	—	1	µA
Power Requirements:						
Power Dissipation	V_{DD} = 5 V, V_{BAT} = –48 V,					
	Idle/Talk State or All Off State	I_{DD}, I_{BAT}	—	3	5	mW
	Ringing State or Access State	I_{DD}	—	6	10	mW
V_{DD} Current	V_{DD} = 5 V,					
	Idle/Talk State or All Off State	I_{DD}	—	560	900	µA
	Ringing State or Access State	I_{DD}	—	0.750	1.9	mA
V_{BAT} Current	V_{BAT} = –48 V,					
	Idle/Talk State or All Off State	I_{BAT}	—	4	10	µA
	Ringing State or Access State	I_{BAT}	—	4	10	µA
Temperature Shutdown Requirements:*						
Shutdown Activation Temperature	—	—	110	125	150	°C
Shutdown Circuit Hysteresis	—	—	10	—	25	°C

* Temperature shutdown flag (TSD) will be high during normal operation and low during temperature shutdown state.

Zero Cross Current Turn Off

The ring access switch (SW4) is designed to turn off on the next zero current crossing after application of the appropriate logic input control. This switch requires a current zero cross to turn off. Switch 4, once on, will remain in the on state (regardless of logic input) until a current zero cross. Therefore, to ensure proper operation of switch 4, this switch should be connected, via proper impedance, to the ringing generator or some other ac source. Do not attempt to switch pure dc with switch 4.

For a detailed explanation of the operation of switch 4 please refer to *An Introduction to ATTL758X Series of Line Card Access Switches* Application Note.

Switching Behavior

When switching from the power ringing state to the idle/talk state, via simple logic level input control, the ATTL7582 is able to provide control with respect to the timing when the ringing access contacts are released relative to the state of the line break contacts.

Make-before-break operation occurs when the line break switch contacts are closed (or made) before the ringing access switch contact is opened (or broken). Break-before-make operation occurs when the ringing access contact is opened (broke) before the line break switch contacts are closed (made).

Using the logic level input pins INring and INaccess, either make-before-break or break-before-make operation of the ATTL7582 is easily achieved. The logic sequences for either mode of operation are given below. See Truth Table for explanation of logic states. The switching behavior of the ATTL7582 is presented in greater detail in the *Switching Behavior of the ATTL758X Series of Line Card Access Switches* Application Note.

Table 8. Make-Before-Break Operation

Access	Input	TSD	State	Timing	Break Switches 1 & 2	Ring Return Switch 3	Ring Access Switch 4	Line Access Switch 5 & 6
0 V	5 V	Float	Power Ringing	—	Open	Closed	Closed	Open
0 V	0 V	Float	Make-before-break	SW4 waiting for next zero current crossing to turn off maximum time—one half of ringing. In this transition state, current that is limited to the dc break switch current-limit value will be sourced from the ring node of the SLIC.	Closed	Open	Closed	Open
0 V	0 V	Float	Idle/Talk	Zero cross current has occurred.	Closed	Open	Open	Open

Switching Behavior (continued)

Table 9. Break-Before-Make Operation

Access	Input	TSD	State	Timing	Break Switches 1&2	Ring Return Switch 3	Ring Access Switch 4	Line Access Switch 5 & 6
0 V	5 V	Float	Power Ringing	—	Open	Closed	Closed	Open
5 V	5 V	Float	All Off	Hold this State for ≤25 ms. SW4 waiting for zero current to turn off.	Open	Open	Closed	Open
5 V	5 V	Float	All Off	Zero current has occurred, SW4 has closed	Open	Open	Open	Open
0 V	0 V	Float	Idle/Talk	Release Break Switches	Closed	Open	Open	Open

Note that break-before-make operation can also be achieved using TSD as an input. In lines 2 & 3 of Table 9, instead of using the logic input pins to force the "all off" state, force TSD to ground. This will override the logic inputs and also force the all off state. Hold this state for 25 ms. During this 25 ms all off state, toggle the inputs from the 10 (ringing state) to 00 (idle/talk state). After 25 ms, release TSD to return switch control to the input pins which will set the idle talk state.

When using the ATTL7582 in this mode, forcing TSD to ground will override the INPUT pins and force an all off state. Setting TSD to +5 will allow switch control via the logic INPUT pins. However, setting TSD to +5V will also disable the thermal shutdown mechanism. This is not recommended. Therefore, to allow switch control via the logic INPUT pins, allow TSD to float.

Thus when using TSD as an input, the two recommended states are 0 (overrides logic input pins and forces all off state) and float (allows switch control via logic input pins and thermal shutdown mechanism is active). The may require use of an open collector buffer.

Also note that TSD operation in ATTL7582 is different than TSD operation of the ATTL7581, where application of +5 V does not disable the thermal shutdown mechanism.

Power Supplies

Both the +5 V and battery supply are brought onto the ATTL7582. The ATTL7582 requires only the +5 V supply for switch operation; that is, state control is powered exclusively off of the +5 V supply. Because of this, the ATTL7582 offers extremely low power dissipation, both in the idle and active states.

The battery voltage is not used for switch state control. The battery is used as a reference voltage by the integrated secondary protection circuit. When the voltage at Tbat or Rbat drops 2 to 4 volts below the battery, the integrated SCR will trigger, thus preventing fault induced overvoltage situations at the Tbat/ Rbat nodes.

Loss of Battery Voltage

As an additional protection feature, the ATTL7582 monitors the battery voltage. Upon loss of battery voltage, the ATTL7582 will automatically enter an "all off" state and remain in that state until the battery voltage is restored. The ATTL7582 is designed such that the device will enter the "all off" state if the battery rises above –10 V and will remain off until the battery drops below –15 V.

Monitoring the battery for the automatic shutdown feature will draw a small current from the battery, typically 4 μA. This will add slightly to the overall power dissipation of the device.

Impulse Noise

Using the ATTL7582 will minimize and possibly eliminate the contribution to the overall system impulse noise that is associated with ringing access switches. Because of this characteristic of the ATTL7582, it may not be necessary to incorporate a zero-cross switching scheme. This ultimately depends upon the characteristics of the individual system and is best evaluated at the board level.

A more detailed explanation of this characteristic is found in the *Impulse Noise and the ATTL758X Series Line Card Access Switches* Application Note in this chapter.

Protection

Integrated SLIC Protection

Diode Bridge/SCR

In the ATTL7582Axx version, protection to the SLIC device or other subsequent circuitry is provided by a combination of current-limited break switches, a diode bridge/SCR clamping circuit, and a thermal shutdown mechanism. In the ATTL7582Bxx version, protection to the SLIC device or other subsequent circuitry is provided by a combination of current-limited break switches, a diode bridge, and a thermal shutdown mechanism.

Protection (continued)

Integrated SLIC Protection (continued)

Diode Bridge/SCR (continued)

In both versions, during a positive lightning event, fault current is directed to ground via steering diodes in the diode bridge. Voltage is clamped to a diode drop above ground. In the A version, negative lightning causes the SCR to conduct when the voltage goes two to four volts more negative than the battery. Fault currents are then directed to ground via the SCR and steering diodes in the diode bridge.

Note that for the SCR, to foldback or crowbar, the ON voltage (see Table 10) of the SCR must less negative than the battery reference voltage. If the battery voltage is less negative than the SCR ON voltage, the SCR will conduct fault currents to ground, however it will not crowbar.

In the B version, negative lightning is directed to battery via steering diodes in the diode bridge.

For power cross and power induction faults, in both versions, the positive cycle of the fault is clamped a diode drop above ground and fault currents steered to ground. In the A version, the negative cycle will cause the SCR to trigger when the voltage exceeds the battery reference voltage by two to four volts. When the SCR triggers, fault current is steered to ground. In the B version the negative cycle of the power cross is steered to battery.

Current Limiting

During a lightning event, the current that is passed through the break switches and presented to the integrated protection circuit and subsequent circuitry is limited by the dynamic current-limit response of the break switches (assuming idle/talk state). When the voltage seen at the Tline/Rline nodes is properly clamped by an external secondary protector, upon application of a 1000 V 10X1000 pulse (LSSGR lightning) the current seen at the Tbat/Rbat nodes will be typically a pulse of magnitude 2.5 A and duration less than 0.5 µs.

During a power cross event, the current that is passed through the break switches and presented to the integrated protection circuit and subsequent circuitry is limited by the dc current limit response of the break switches (assuming idle/talk state). The dc current limit is specified over temperature between 100 mA and 250 mA.

Note that the current limit circuitry has a negative temperature coefficient. Thus, if the device is subjected to an extended power cross the value of current seen at Tbat/Rbat will decrease as the device heats due to the fault current. If sufficient heating occurs, the temperature shutdown mechanism will activate and the device will enter an all off mode.

Temperature Shutdown Mechanism

When the device temperature reaches a minimum of 110 °C, the thermal shutdown mechanism will activate and force the device into an all off state, regardless of the logic input pins. Pin TSD when used as an output will read 0 V when the device is in the thermal shutdown mode and +V_{DD} during normal operation.

During a lightning event, due to the relatively short duration, the thermal shutdown will not typically activate.

During an extended power cross, the device temperature will rise and cause the device to enter the thermal shutdown mode. This forces an all off mode, and the current seen at Tbat/Rbat drops to zero. Once in the thermal shutdown mode, the device will cool and exit the thermal shutdown mode thus returning to the state it was in prior to thermal shutdown. Current, limited to the dc current limit value, will again begin to flow and device heating begins again. This cycle of entering and exiting thermal shutdown will last as long as the power-cross fault is present.

If the magnitude of power is great enough, the external secondary protector could trigger, thereby shunting all current to ground.

In the ATTL7582, the thermal shutdown mechanism can be disabled by forcing the TSD pin to +V_{DD}. This functionality differs from the ATTL7581, whose thermal shutdown mechanism cannot be disabled.

Protection (continued)

Integrated SLIC Protection (continued)

External Secondary Protector

With the above integrated protection features only one over voltage secondary protection device on the loop side of the ATTL7582 is required. The purpose of this device is to limit fault voltages seen by the ATTL7582 so as not to exceed the breakdown voltage or input-output isolation rating of the device. To minimize stress on the ATTL7582 use of a foldback or "crowbar" type device is recommended. A detailed explanation and design equations on the choice of the external secondary protection device are given in the *An Introduction to ATTL758x Series of Line Card Access Switches* Application Note. Basic design equations governing the choice of external secondary protector are given below:

- $|V_{BATmax}| + |V_{breakovermax}| < |V_{breakdownmin(break)}|$
- $|V_{ringingpeakmax}| + |V_{BATmax}| + |V_{breakovermax}| < |V_{breakdownmin(ring)}|$
- $|V_{ringingbreakmax}| + |V_{BATmax}| < |V_{breakovermin}|$

where:

V_{BATmax} — Maximum magnitude of battery voltage

$V_{breakovermax}$ — Maximum magnitude breakover voltage of external secondary protector

$V_{breakovermin}$ — Minimum magnitude breakover voltage of external secondary protector

$V_{breakdownmin(break)}$ — Minimum magnitude breakdown voltage of ATTL7582 break switch

$V_{breakdownmin(ring)}$ — Minimum magnitude breakdown voltage of ATTL7582 ring access switch

$V_{ringingpeakmax}$ — Maximum magnitude peak voltage of ringing signal

Series current-limiting fused resistors or PTCs should be chosen so as not to exceed the current rating of the external secondary protector, see manufacturer's data sheet for requirements.

Table 10. Electrical Specifications, Protection Circuitry

Parameters Related to Diodes (in Diode Bridge)						
Parameter	**Test Condition**	**Measure**	**Min**	**Typ**	**Max**	**Unit**
Voltage Drop @Continuous Current (50/60 Hz)	Apply ±dc current limit of break switches	Forward Voltage	—	—	3	V
Voltage Drop @ Surge Current	Apply ±dynamic current limit of break switches	Forward Voltage	—	5	—	V
Parameters Related to Protection SCR						
Surge Current	—	—	—	—	*	A
Trigger Current	—	—	50	—	—	mA
Hold Current	—	—	†	—	‡	mA
Gate Trigger Voltage	Trigger current	—	$V_{BAT} - 4$	—	$V_{BAT} - 2$	V
Reverse Leakage Current	V_{BAT}	—	—	—	1.0	µA
ON State Voltage§	0.5 A, t = 0.5 µs 2.0 A, t = 0.5 µs	Von —	— —	–3 –5	— —	V V

* Twice ± dynamic current limit of break switches.
† Trigger current.
‡ dc current-limit break switches.
§ In some instances, the typical ON state voltage can range as low as –25 V.

Typical Performance Characteristics

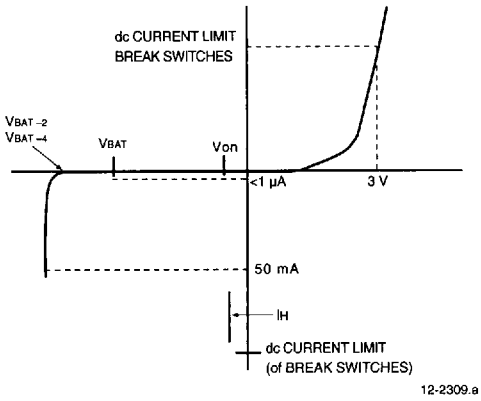


Figure 3. Protection Circuit A Version

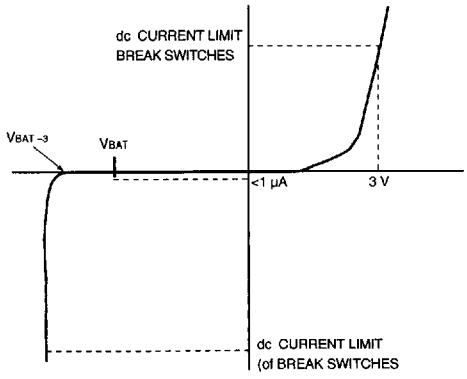


Figure 4. Protection Circuit B Version

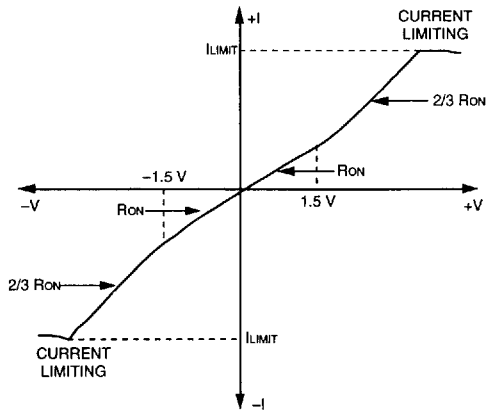


Figure 5. Switch 1—3

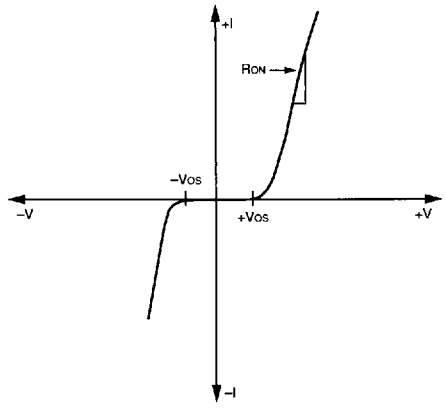


Figure 6. Switch 4

Application

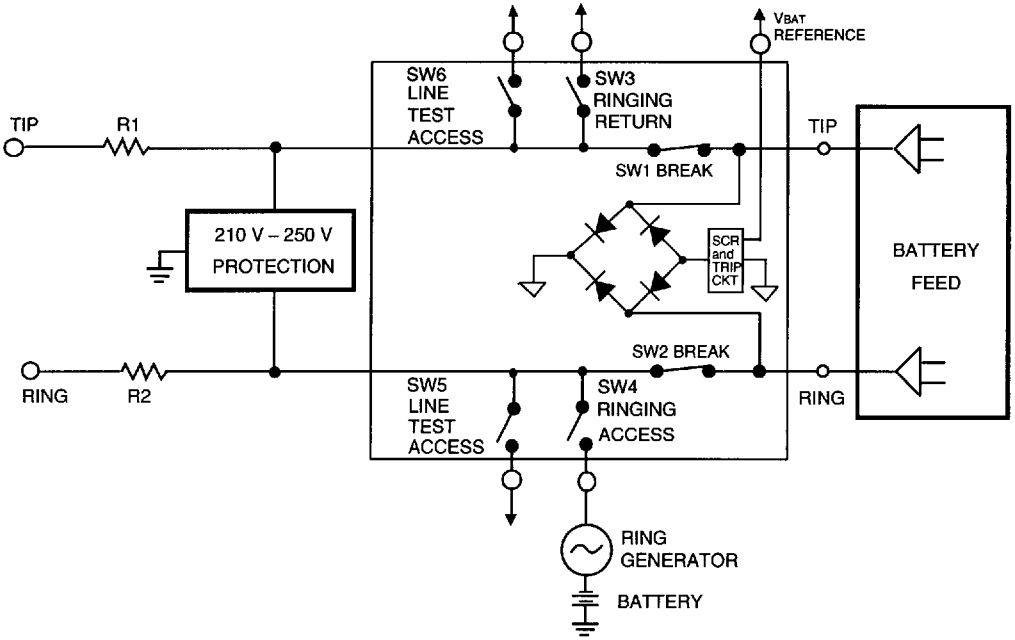


Figure 7. Typical TRAS Application, Idle or Talk State Shown

Table 11. Truth Table

Input	Access	TSD	Tip Break Switch	Ring Break Switch	Ringing Return Switch	Ring Switch	Tip Access Switch	Ring Access Switch
0 V	0 V	5 V/Float[5]	On	On	Off	Off	Off	Off[1]
5 V	0 V	5 V/Float[5]	Off	Off	On	On	Off	Off[2]
0 V	5 V	5 V/Float[5]	Off	Off	Off	Off	On	On[3]
5 V	5 V	5 V/Float[5]	Off	Off	Off	Off	Off	Off[4]
Don't Care	Don't Care	0 V[6]	Off	Off	Off	Off	Off	Off[4]

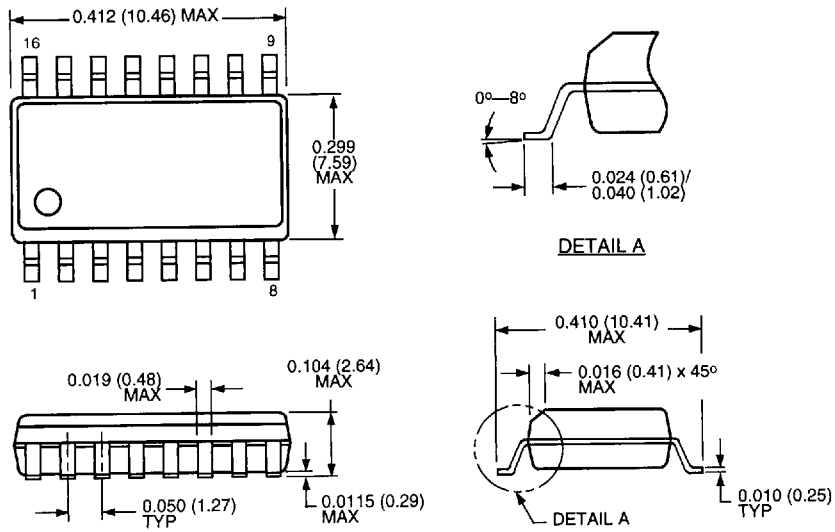
1. Idle/Talk state.
2. Power ringing state.
3. Test out message waiting state.
4. All OFF state.
5. If TSD = 5 V, the thermal shutdown mechanism is disabled.
   If TSD is floating, the thermal shutdown mechanism is active.
6. Forcing TSD to ground overrides the logic input pins and forces an all off state.

A parallel in/parallel out data latch is integrated into the ATTL7582. Operation of the data latch is controlled by the logic level input pin LATCH. The data input to the latch is the INPUT pin of the ATTL7582, and the output of the data latch is an internal node used for state control. When the LATCH control pin is at logic 0, the data latch is transparent and data control signals flow directly from INPUT, through the data latch to state control. Any changes in INPUT will be reflected in the state of the switches. When the LATCH control pin is at logic 1, the data latch is active — the ATTL7582 will no longer react to changes at the INPUT control pin. The state of the switches is now latched; that is, the state of the switches will remain as they were when the LATCH input transitioned from logic 0 to logic 1. The switches will not respond to changes in INPUT as long as LATCH is held high. Also note that the TSD input is not tied to the data latch. TSD is not affected by the LATCH input. TSD input will override state control via INPUT and LATCH.

Outline Drawings

Dimensions are in inches and (millimeters).

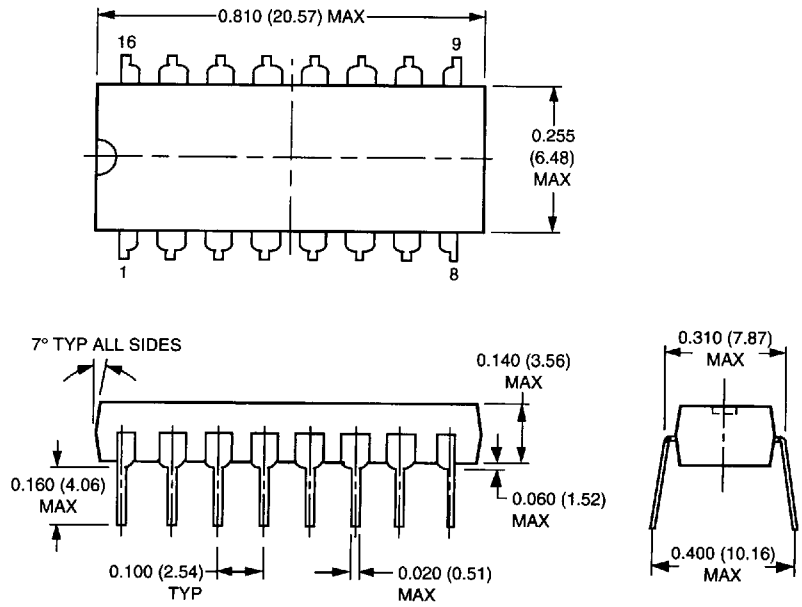
16-Pin, Plastic SOG (ATTL7582AAE/BAE)



Outline Drawings (continued)

Dimensions are in inches and (millimeters).

16-Pin, Plastic DIP (ATTL7582AE/BE)



Packaging and Ordering Information

Throughout this section the following abbreviations are used:

DIP — Dual in-line package; SOG — Small-outline gull wing; SOJ — Small-outline J-lead; SONB — Small-outline narrow body; PLCC — Plastic leaded chip carrier.

Device Code	Package Type	Temperature
ATTL7551AP	44-Pin PLCC	–40 °C to +85 °C
ATTL7551AF	24-Pin DIP	–40 °C to +85 °C
ATTL7554AP	44-Pin PLCC	–40 °C to +85 °C
ATTL7556AAU	32-Pin PLCC	–40 °C to +85 °C
ATTL7557AAU		
ATTL7561AP	44-Pin PLCC	–40 °C to +85 °C
ATTL7564AP		
ATTL7581AC/BC	16-Pin DIP	–40 °C to +85 °C
ATTL7581AAE/BAE	16-Pin Plastic SOG	–40 °C to +85 °C
ATTL7582AE/BE	16-Pin Plastic DIP	–40 °C to +85 °C
ATTL7582AAE/BAE	16-Pin Plastic SOG	–40 °C to +85 °C
ATTL7583AF/BF	24-Pin Plastic DIP (600 mil)	–40 °C to +85 °C
ATTL7583ACG/BCG	24-Pin Plastic DIP (300 mil)	–40 °C to +85 °C
ATTL7583AAJ/BAJ	28-Pin Plastic SOG	–40 °C to +85 °C
ATTL7590AAF	14-Pin	–40 °C to +85 °C
ATTL7591AB	8-Pin, DIP	–40 °C to +85 °C
ATTL7591AS	8-Pin, SONB	–40 °C to +85 °C
LB1011AB	8-Pin, DIP	–20 °C to +70 °C
LB1013AD	18-Pin, DIP	–25 °C to +85 °C
LB1060AB	8-Pin, DIP	–40 °C to +65 °C
LB1201AB	8-Pin, DIP	–40 °C to +85 °C
LB1201AS	8-Pin, SONB	–40 °C to +85 °C
LB1208AAJ	28-pin SOG	–40 °C to +85 °C
LB1276AP	44-Pin PLCC	–40 °C to +85 °C
LB1276AF	24-Pin DIP	–40 °C to +85 °C
LB1356AF	24-Pin DIP	–40 °C to +85 °C
LH1263AR	20-Pin Plastic DIP	–40 °C to +85 °C
LH1571AB	8-pin Plastic DIP	–40 °C to +85 °C
LH1571AAC	8-pin SOG	–40 °C to +85 °C
T - 7503 - - - EL	20-Pin, SOJ	–40 °C to +85 °C
T - 7503 - - 1EC	20-Pin, SOJ	0 °C to 70 °C
T - 7504 - - - PL	28-Pin, DIP	–40 °C to +85 °C
T - 7504 - - - ML	28-Pin, PLCC	–40 °C to +85 °C
T - 5504 - - - PL	28-Pin, DIP	–40 °C to +85 °C
T - 5504 - - - ML	28-Pin, PLCC	–40 °C to +85 °C
T - 7513B - - EE	20-Pin, SOJ	–40 °C to +85 °C
T - 7513B - - PE	20-Pin, DIP	–40 °C to +85 °C
T - 7517A - - EE	16-Pin, DIP	–40 °C to +85 °C
T - 7517A - - PE	16-Pin, SOJ	–40 °C to +85 °C
T - 7548 - - - ME2	28-Pin, PLCC	0 °C to 85 °C
T - 7570 - - - ML2	28-Pin, PLCC	–40 °C to +85 °C