

ATTL8570A SLIC

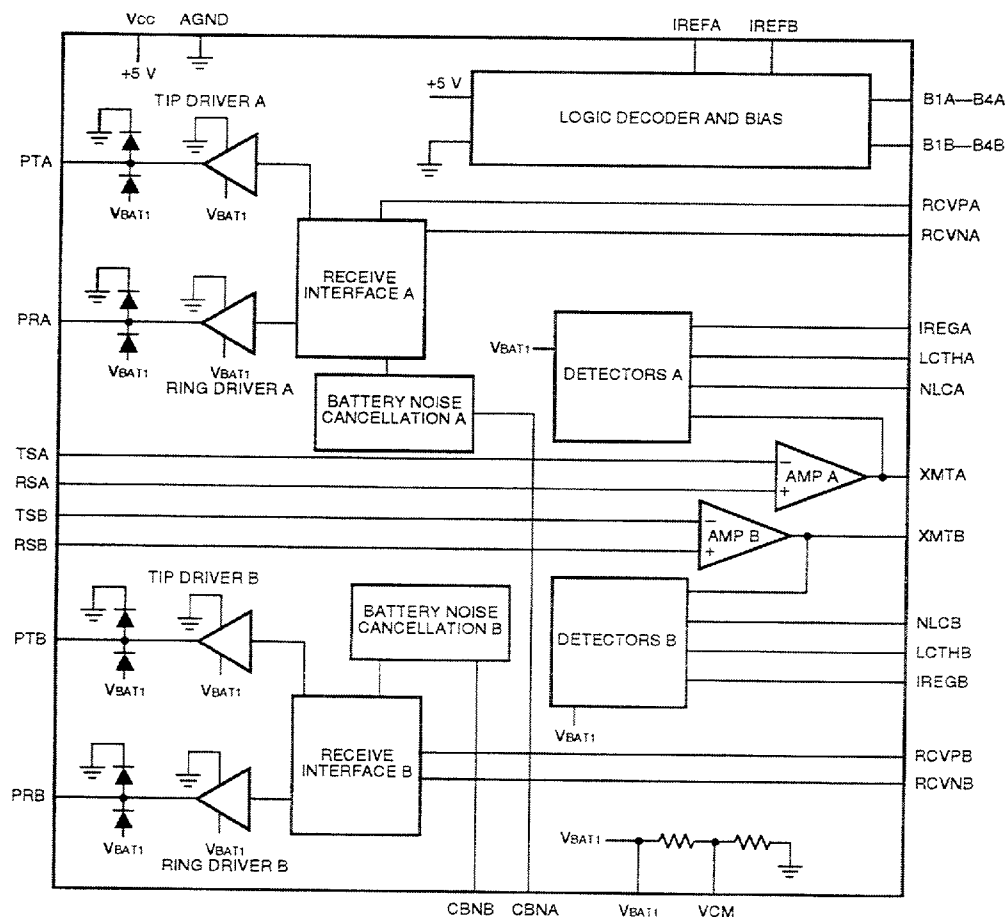
Features

- Per channel power-down
- Low active power (150 mW typical per channel)
- Battery noise cancellation
- Loop closure detector

Introduction

The ATTL8570A is a dual electronic Subscriber Loop Interface Circuit and is designed to be used with the ATTL8571A. It interfaces the low-voltage circuits on a line card to the Tip and Ring of two subscriber loops. The ATTL8570A does not supply dc current to the subscriber loops; external resistors are used for this purpose. This device is available in a 44-pin PLCC package.

Description



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Figure 1. Functional Diagram

Pin Descriptions

Pin	Symbol	Type	Name/Function
1	B4A	I	State Control Input (Chan A). B1A – B4A determine the state of Channel A of the SLIC. See Input State Coding Table.
2	B1B	I	State Control Input (Chan B). B1B – B4B determine the state of Channel B of the SLIC. See Input State Coding Table.
3	B2B	I	State Control Input (Chan B). B1B – B4B determine the state of Channel B of the SLIC. See Input State Coding Table.
4	B3B	I	State Control Input (Chan B). B1B – B4B determine the state of Channel B of the SLIC. See Input State Coding Table.
5	B4B	I	State Control Input (Chan B). B1B – B4B determine the state of Channel B of the SLIC. See Input State Coding Table.
6	NLCB	O	Not Loop–Closure (Chan B). This logic output indicates an off–hook condition on channel B when it is low.
7	LCTHB	I	Loop Closure Threshold (Chan B). Scaled voltage of VREG for the loop closure comparator.
8	IREGB	I	VREG Reference Current (Chan B). This current input is equal to $VREG / (RLCTH1 + RLCTH2)$.
9	NC	—	No Connection. Must leave open on PWB.
10	NC	—	No Connection. Must leave open on PWB.
11	Vcc	—	+5 V Analog dc Supply.
12	IREFB	O	Reference Current Output (Chan B). 40 μ A reference current output to the ATT8571A.
13	RCVPB	I	Receive Signal Input + (Chan B). The differential voltage from PTB to PRB is 25.8 times the differential voltage applied between RCVPB and RCVNB.
14	RCVNB	I	Receive Signal Input – (Chan B). The differential voltage from PTB to PRB is 25.8 times the differential voltage applied between RCVPB and RCVNB.
15	RSB	I	RING Sense (Chan B). Positive input of Channel B transmit op amp. Connect one high–value resistor between RSB and the RING of loop B and another high–value resistor between RSB and AGND.
16	TSB	I	TIP Sense (Chan B). Negative input of Channel B transmit op amp. Connect one high–value resistor between TSB and the TIP of loop B and another high–value resistor between TSB and XMTB.
17	XMTB	O	Transmit Signal Output (Chan B). Channel B transmit amplifier output.
18	PRB	O	Protected RING (Chan B). Output of RING Drive Amplifier B. Connect a resistor and capacitor in series between PRB and the RING of loop B.
19	PTB	O	Protected TIP (Chan B). Output of TIP Drive Amplifier B. Connect a resistor and capacitor in series between PTB and the TIP of loop B.
20	CBNB	I	Battery Noise Capacitor (Chan B). Connect a 0.1 μ F capacitor from CBNB to VREG of Channel B. This capacitor couples noise from VREG to the battery noise cancellation circuit which eliminates battery noise on the TIP/RING of Channel B.

Pin Description (continued)

Pin	Symbol	Type	Name/Function
21	CBNA	I	Battery Noise Capacitor (Chan A). Connect a 0.1 μ F capacitor from CBNA to VREG of Channel A. This capacitor couples noise from VREG to the battery noise cancellation circuit which eliminates battery noise on the TIP/RING of Channel A.
22	VBAT1	—	Office Battery Supply. Negative Office Battery Supply.
23	VCC	—	+5 V Analog dc Supply.
24	AGND	—	Analog Signal Ground.
25	VCM	I/O	Common Mode Reference Voltage. Connect a 0.1 μ F capacitor from VCM to AGND. This capacitor filters noise on VBAT1 from appearing longitudinally on the TIP/RING of both channels. Nominal voltage at VCM is VBAT1/2.
26	NC	—	No Connection. Can be used as a feed through on PWB.
27	PTA	O	Protected TIP (Chan A). Output of TIP Drive Amplifier A. Connect a resistor and capacitor in series between PTA and the TIP of loop A.
28	PRA	O	Protected RING (Chan A). Output of RING Drive Amplifier A. Connect a resistor and capacitor in series between PRA and the RING of loop A.
29	XMTA	O	Transmit Signal Output (Chan A). Channel A transmit amplifier output.
30	TSA	I	TIP Sense (Chan A). Negative input of Channel A transmit op amp. Connect one high-value resistor between TSA and the TIP of loop A and another high-value resistor between TSA and XMTA.
31	RSA	I	RING Sense (Chan A). Positive input of Channel A transmit op amp. Connect one high-value resistor between RSA and the RING of loop A and another high-value resistor between RSA and AGND.
32	RCVNA	I	Receive Signal Input – (Chan A). The differential voltage from PTA to PRA is 25.8 times the differential voltage applied between RCVPA and RCVNA.
33	RCVPA	I	Receive Signal Input + (Chan A). The differential voltage from PTA to PRA is 25.8 times the differential voltage applied between RCVPA and RCVNA.
34	IREFA	O	Reference Current Output (Chan A). 40 μ A reference current output to the ATTL8571A.
35	AGND	—	Analog Signal Ground.
36	NC	—	No Connection. Must leave open on PWB.
37	NC	—	No Connection. Must leave open on PWB.
38	IREGA	I	VREG Reference Current (Chan A). This current input is equal to VREG/ (RLCTH1+RLCTH2).
39	LCTHA	I	Loop Closure Threshold (Chan A). Scaled voltage of VREG for the loop closure comparator.
40	NLCA	O	Not Loop-Closure (Chan A). This logic output indicates an off-hook condition on channel A when it is low.
41	B1A	I	State Control Input (Chan A). B1A – B4A determine the state of Channel A of the SLIC. See Input State Coding Table.
42	B2A	I	State Control Input (Chan A). B1A – B4A determine the state of Channel A of the SLIC. See Input State Coding Table.
43	B3A	I	State Control Input (Chan A). B1A – B4A determine the state of Channel A of the SLIC. See Input State Coding Table.
44	NC	—	No Connection. Can be used as a feedthrough on PWB.

Absolute Maximum Ratings

TA = 25 °C

Stresses exceeding the values listed under maximum ratings may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this data sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Parameter	Value	Unit
Vcc Supply Voltage	7.0	V
VBAT1 Supply Voltage	-60	V
Logic Input Voltage	-0.5 to 7.0	V
Analog Input Voltage	-7.0 to 7.0	V
Operating Temperature Range	-40 to 125	°C
Storage Temperature Range	-40 to 125	°C
Relative Humidity Range	5 to 95	%

Note: The IC can be damaged unless all ground connections are applied before, and removed after, all other connections. Furthermore, when powering the device, the user must guarantee that no external potential creates a voltage on any pin of the device that exceeds the device ratings. Some of the known examples of conditions that cause such potentials during powerup are 1) an inductor connected to Tip and Ring can force an overvoltage on VBAT1 through external components if the VBAT1 connection chatters, 2) inductances in the VBAT1 lead could resonate with the VBAT1 filter capacitor to cause destructive overvoltages.

Recommended Operating Voltages & Conditions

Parameter	Min	Typ	Max	Unit
Ambient Temperature	-40	—	85	°C
Vcc Supply Voltage	4.75	5.00	5.25	V
VBAT1 Supply Voltage	-43	-48	-57	V

Input State Coding

Combined Input State Coding (for both ATTL8570A & ATTL8571A)

No.	B0*	B1	B2	B3	B4	Combined State
1	1	1	1	1	1	High Battery Talk State
2	0	1	1	1	1	Low Battery Talk State
3	0	0	0	1	0	Ringing State
4	0	1	0	0	0	Sleep State
5	0	0	1	1	0	Forward Disconnect State
6	1	0	0	1	1	On-hook Transmission State

*For reference only, not used by ATTL8570A.

Input State Coding (for ATTL8570A only):

No.	B1	B2	B3	B4	State
1	1	1	1	1	Normal Powerup Talk State
2	0	0	1	0	Ringing State
3	1	0	0	0	Sleep State
4	0	1	1	0	Forward Disconnect State
5	0	0	1	1	Normal Powerup Talk State

Definition of States:

- Normal Powerup Talk State (States 1 & 5)
 - Normal talk state.
 - AT & AR are powered up.
 - NLC indicates logic high if the loop is open.
- Ringing State (State 2)
 - Receive Transmission Path (AT, AR, & Receive Interface) power down to conserve power.
- Sleep State (State 3)
 - Receive Transmission Path (AT, AR, & Receive Interface) power down to conserve power.
 - AX Amplifier & Loop Closure Detector are active; NLC indicates logic high if loop is open.
- Forward Disconnect State (State 4)
 - Receive & Transmit Transmission Path Power Down.
 - Output of AX Amplifier forced to ground.

Electrical Characteristics

In general, minimum and maximum values are testing requirements. However, some parameters may not be tested in production because they are guaranteed by design and device characterization. Typical values reflect the design center or nominal value of the parameter; they are for information only and are not a requirement. Minimum and maximum values apply across the entire temperature range (-40°C to $+85^{\circ}\text{C}$). Typical is defined as 25°C . $V_{CC} = +5.0\text{ V}$, $V_{BAT1} = -48\text{ V}$. Positive currents flow into the device.

Power Supply

Parameter	Min	Typ	Max	Unit
Power Supply – Talk State (Both Channels), No Loop Current:				
I_{CC}	—	12.0	16.0	mA
I_{BAT1} ($V_{BAT1} = -48\text{ V}$)	—	-5.0	-6.0	mA
Power Dissipation	—	300	370	mW
Power Supply – Low-power Scan State (Both Channels), No Loop Current:				
I_{CC}	—	12.0	16.0	mA
I_{BAT1} ($V_{BAT1} = -48\text{ V}$)	—	-2.5	-3.0	mA
Power Dissipation	—	180	225	mW
Power Supply Rejection – Talk State: (500 Hz – 3 kHz, 100 mVrms ripple):				
V_{CC}	35	—	—	dB
V_{BAT1}	35	—	—	dB

Transmission Characteristics

Transmit direction is TIP/RING to 4-Wire. Receive direction is 4-Wire to TIP/RING.

Parameter	Min	Typ	Max	Unit
Longitudinal to Metallic Balance – IEEE std 4551 200 Hz – 4 kHz	40	—	—	dB
Metallic to Longitudinal Balance 200 Hz – 4 kHz	30	—	—	dB
RFI Rejection 0.5 Vrms, 50 Ω source, 30% AM Mod 1 kHz 500 kHz – 100 MHz	—	—	-45	dB
ac Termination Impedance	—	600	—	Ω
Total Harmonic Distortion – 200 Hz to 4 kHz	—	—	0.3	%
TIP/RING Signal Level (reference to 600 Ω)	—	—	3.14	dBm
Transmit Gain Accuracy, f = 1 kHz (TIP/RING to XMT)	0.245	0.250	0.255	—
Receive + Gain Accuracy, f = 1 kHz (RCVP to PT/PR)	24.5	25.8	27.1	—
Receive – Gain Accuracy, f = 1 kHz (RCVN to PT/PR)	-24.5	-25.8	-27.1	—
Gain vs. Frequency (Transmit & Receive): (600 Ω termination; reference 1 kHz)				
200 Hz – 300 Hz	-1.00	0	0.05	dB
300 Hz – 3.4 kHz	-0.3	0	0.05	dB
3.4 kHz – 20 kHz	-3.0	-0.1	2.00	dB
3.4 kHz – 266 kHz	—	—	2.00	dB
Gain vs. Level (Transmit & Receive): (reference 0 dBV) -50 dB to +3 dB	-0.05	0	0.05	dB
Return Loss: 2				
200 Hz – 500 Hz	15	—	—	dB
500 Hz – 25 00 Hz	20	—	—	dB
2500 Hz – 3400 Hz	15	—	—	dB
TIP/RING Idle-Channel Noise: 2				
Psophometric	—	—	-77	dBmp
C-message	—	—	13	dBmC
3 kHz flat	—	—	20	dBm
Transmit Idle-Channel Noise: 2				
Psophometric	—	—	-77	dBmp0
C-message	—	—	13	dBmC0
3 kHz flat	—	—	20	dBm0
Transhybrid Loss: 2				
200 Hz – 500 Hz	15	—	—	dB
500 Hz – 2500 Hz	20	—	—	dB
2500 Hz – 3400 Hz	15	—	—	dB

Notes: Guaranteed performance assumes RTFx & RRFx matched to 0.2% and (R1/R2) & (R3/R4) matched to 0.2%.

Measured with the ATTL8571A connected per Figure 2. Transmission characteristics are specified assuming a 600 Ω resistive termination. External resistors RT1, RT2, RT3, RHB, RX 1% tolerance; all external capacitors 20% tolerance.

Transmission Characteristics (continued)

Analog Signal Pins

Parameter	Min	Typ	Max	Unit
PTA, PTB, PRA, and PRB:				
Surge Current (from external source)				
continuous	—	—	±50	mAdc
1 ms pulse (50 repetitions)	—	—	±500	mA
30 ms pulse (60 repetitions)	—	—	±250	mA
10 µs pulse (10 repetitions)	—	—	±1.3	A
Output Drive Current	—	—	—	mA
Output Voltage Swing:	—	—	—	—
maximum	—	—	AGND	V
minimum (7 mA Load)	—	—	—	V _{p-p}
Output Short-Circuit Current	—	—	±50	mA
Output Impedance (60 Hz – 3.4 kHz)	—	—	5	Ω
Output Load Resistance (dc or ac)	—	—	—	kΩ
Output Load Capacitance	—	—	50	pF
XMTA and XMTB:				
Output Drive Current	±3	—	—	mA
Output Voltage Swing (3 mA Load):				
maximum	V _{BAT}	—	V _{DDA}	V
minimum	V _{BAT} +10	—	+2.5	V
Output Short-circuit Current	—	—	±30	mA
Output Impedance (60 Hz– 3.4 kHz)	—	—	10	Ω
Output Load dc Resistance	20	—	—	kΩ
Output Load ac Impedance	2	—	—	kΩ
Output Load Capacitance	—	—	50	pF
RCVPA, RCVNA, RCVPB, and RCVNB:				
Input Voltage Range	–1.75	—	2.25	V
Input Bias Current	—	—	±1	µA
Input Impedance	20	—	—	MΩ
TSA, TSB, RSA, and RSB:				
Surge Current (from external source)	—	—	±25	mAdc
Input Voltage Range	V _{BAT} +3	—	AGND	V
Input Bias Current	—	—	±1	µA
Differential Input Impedance	50	—	—	kΩ
Common-mode Input Impedance	50	—	—	MΩ
External Capacitance (67 kΩ source impedance)	—	—	10	pF

Loop Closure Detector

Parameter	Min	Typ	Max	Unit
Loop Resistance Threshold*	—	1700	—	Ω

* Detector threshold is independent of battery voltages, and can be programmed with two external resistors, RLCTH1 & RLCTH2. In kΩ, RLCTH1=150(RLOOP+80)/(RLOOP+480), RLCTH2=600–RLCTH1.

Transmission Characteristics (continued)**Logic Inputs & Outputs (B1A–B4A, B1B–B4B, NLC)**

Parameter	Min	Typ	Max	Unit
High-level Input Voltage	2.5	—	V _{CC}	V
Low-level Input Voltage	0	—	0.8	V
Input Bias Current (V _{IH} = 2.5 V)	—	—	330	μA
Input Bias Current (V _{IL} = 0.8 V)	—	—	500	μA
High-level Output Voltage (I _{out} = –100 μA)	V _{CC} – 1.5	—	V _{CC}	V
Low-level Output Voltage (I _{out} = 1 μA)	0	—	0.4	V

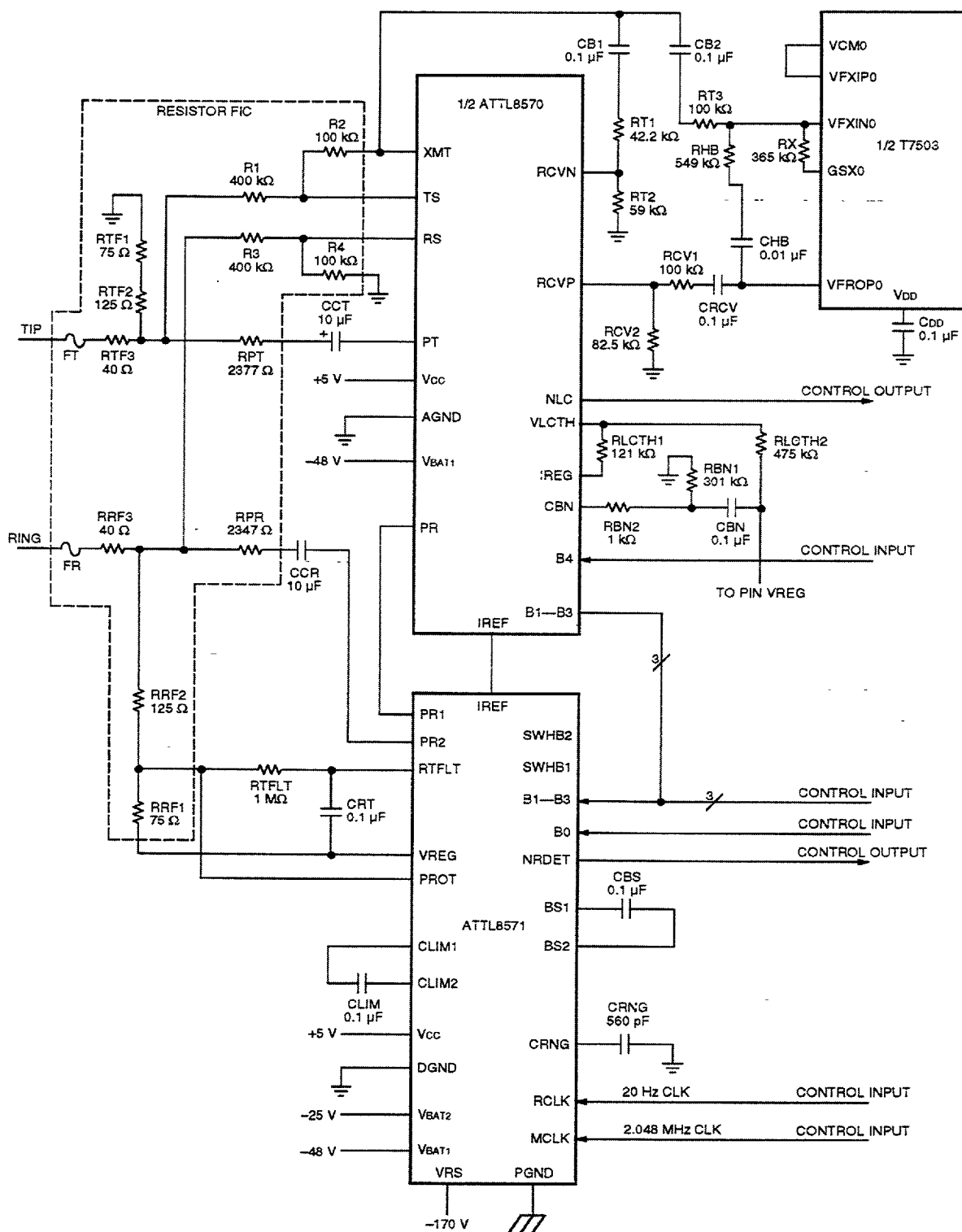
- *Logic inputs have 10 kΩ internal pull-up resistors to V_{CC}.

External Component List

The quantity assumes 2 channels per board.

Component Name	Quant.	Value	Tol.	Comments
Resistor FIC	2			Thick Film FIC, MMC or CTS
CCT	2	10 μ F Min, 50 VWdc, Aluminum Electrolytic Through Hole		
CCR	2	10 μ F Min, 50 VWdc, Non-polarized Aluminum Electrolytic Through Hole		
CLIM	2	0.1 μ F, 100 VWdc, Ceramic SMT	10%	
CCC	1	0.1 μ F, 10 VWdc, Ceramic SMT	20%	One cap per two channels
CDD	1	0.1 μ F, 10 VWdc, Ceramic SMT	20%	One cap per two channels
CBAT1	1	0.1 μ F, 100 VWdc, Ceramic SMT	20%	One cap per two channels
CBAT2	1	0.1 μ F, 100 VWdc, Ceramic SMT	20%	One cap per two channels
CRNG	2	560 pF, 200 VWdc, Ceramic SMT	10%	
CRT	2	0.1 μ F, 10 VWdc, Ceramic SMT	5%	
CBS	2	0.1 μ F, 100 VWdc, Ceramic SMT	20%	
CBN	2	0.1 μ F, 200 VWdc, Ceramic SMT	10%	
CRCV	2	0.1 μ F, 10 VWdc, Ceramic SMT	20%	
CB1	2	0.1 μ F, 100 VWdc, Ceramic SMT	20%	
CB2	2	0.1 μ F, 100 VWdc, Ceramic SMT	20%	
CHB	2	0.01 μ F, 10 VWdc, Ceramic SMT	20%	
RT1	2	42.2 k Ω Metal Film, 0.125 W, 100 V	1%	
RT2	2	59 k Ω Metal Film, 0.05 W, 10 V	1%	
RT3	2	100 k Ω Metal Film, 0.125 W, 100 V	1%	
RX	2	365 k Ω Metal Film, 0.05 W, 10 V	1%	
RHB	2	549 k Ω Metal Film, 0.05 W, 10 V	1%	
RCV1	2	100 k Ω Metal Film, 0.05 W, 10 V	1%	
RCV2	2	82.5 k Ω Metal Film, 0.05 W, 10 V	1%	
RLCTH1	2	121 k Ω Metal Film, 0.05 W, 50 V	1%	
RLCTH2	2	475 k Ω Metal Film, 0.125 W, 200 V	1%	
RTFLT	2	1 M Ω Metal Film, 0.05 W, 20 V	1%	
RBN1	2	301 k Ω Metal Film, 0.05 W, 50 V	1%	
RBN2	2	1 k Ω Metal Film, 0.05 W, 10 V	5%	

Applications



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Figure 2. Typical 600 Ω Loop Start Dual-Battery Application Circuit With ATTL8571A & T7503

The schematic diagram illustrates the circuit for the ATT8571, which includes a 1/2 ATT8570 and an ATT8571 IC. The 1/2 ATT8570 is configured with various resistors (R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R35, R36, R37, R38, R39, R40, R41, R42, R43, R44, R45, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56, R57, R58, R59, R60, R61, R62, R63, R64, R65, R66, R67, R68, R69, R70, R71, R72, R73, R74, R75, R76, R77, R78, R79, R80, R81, R82, R83, R84, R85, R86, R87, R88, R89, R90, R91, R92, R93, R94, R95, R96, R97, R98, R99, R100) and capacitors (C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68, C69, C70, C71, C72, C73, C74, C75, C76, C77, C78, C79, C80, C81, C82, C83, C84, C85, C86, C87, C88, C89, C90, C91, C92, C93, C94, C95, C96, C97, C98, C99, C100) to interface with the TIP, RING, and various control signals. The ATT8571 is configured with various resistors (R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R35, R36, R37, R38, R39, R40, R41, R42, R43, R44, R45, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56, R57, R58, R59, R60, R61, R62, R63, R64, R65, R66, R67, R68, R69, R70, R71, R72, R73, R74, R75, R76, R77, R78, R79, R80, R81, R82, R83, R84, R85, R86, R87, R88, R89, R90, R91, R92, R93, R94, R95, R96, R97, R98, R99, R100) and capacitors (C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68, C69, C70, C71, C72, C73, C74, C75, C76, C77, C78, C79, C80, C81, C82, C83, C84, C85, C86, C87, C88, C89, C90, C91, C92, C93, C94, C95, C96, C97, C98, C99, C100) to interface with the VCC, DGND, and various control signals. The circuit also includes a 1/2 T7503 and a 1/2 T7503.

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