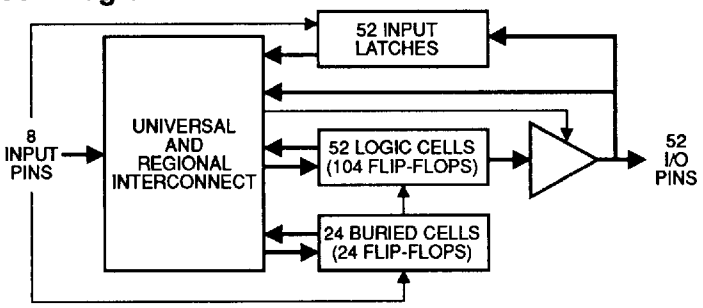
High Density UV Erasable Programmable Logic Device

Features

- **Advanced Programmable Logic Device - High Gate Utilization**
- **Flexible Interconnect Architecture - Universal Routing**
- **Flexible Logic Cells - 128 Flip-Flops and 52 Latches**
- **Multiple Flip-Flop Types - Synchronous or Asynchronous Registers**
- **High Speed - 50 MHz Operation**
- **Complete Third Party Software Support**
  - **No Placement, Routing or Layout Software Required**
- **Proven and Reliable High Speed CMOS EPROM Process**
  - **2000 V ESD Protection**
  - **200 mA Latchup Immunity**
- **Reprogrammable - Tested 100% for Programmability**
- **Commercial, Industrial and Military Temperature Grades**

Block Diagram



Description

The Atmel V5000 is an easy to use, high density programmable logic device. Its simple, regular architecture translates into increased utilization and high performance.

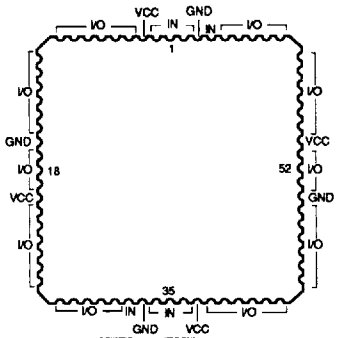
The ATV5000 has one programmable combinatorial logic array. This guarantees easy interconnection of and uniform performance from all nodes. "Sum terms", which are easy to use groupings of AND-OR gates, provide combinatorial logic blocks. Sum terms can be wire-OR'd together to integrate larger logic blocks. To expand the levels of logic, buried sum terms feed back into the logic array. The 52 I/O pins can each be driven by a register or a sum term. Each I/O pin has an individually enabled input latch.

All 128 registers are configurable as D- or T-types without using extra logic gates. Individual sum terms, asynchronous presets, resets and clocks give each flip-flop added flexibility. A direct "clock from pin" option guarantees synchronization and fast clock to output performance.

Standard, off-the-shelf third-party software tools and programmers support the ATV5000. This minimizes start-up investment and improves product support.

Chip Carrier Pin Configuration

Pin Name	Function
IN	Logic and Clock Inputs
Pins 2,32,36,66	Input/Register Clocks 1-4
Pins 1,34,35,68	Input/Latch Clocks 1-4
I/O	Bidirectional Buffers
VCC	+5 V Supply



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V[1]
Voltage on Input Pins with Respect to Ground During Programming	-2.0 V to +14.0 V[1]
Programming Voltage with Respect to Ground	-2.0 V to +14.0 V[1]
Integrated UV Erase Dose	7258 W·sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC}+0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

Functional Logic Diagram Description

There are 52 identical input/ouput logic cells and 24 identical buried logic cells in the ATV5000. Each I/O cell has two flip-flops, up to three sum terms, individual clock, reset, and preset terms per flip-flop, and one output enable term. Independent of output configuration, all flip-flops are always usable, and have at least four product term inputs each.

Each I/O pin (52 total) signal or its latched version drives the logic array. There is one latch clock per quadrant.

The ATV5000 has four identical quadrants (see Figure 2). The universal bus routes true and false signals from each of the 52 I/O pins to all four quadrants. Regional buses route each quadrant's flip-flop Q and $\overline{Q}$ locally. The eight input-only pins are available in all four regional buses.

Each logic cell has a number of "regional" and "universal" product terms (see Figure 1). The I/O logic cells contain three sum terms, two flip-flops, and an I/O buffer.

The buried logic cells each contain one flip-flop. In addition, in each buried logic cell the sum term can drive the regional bus. This allows for logic expansion.

Serial register preload and observability simplify testing. All registers automatically clear at power up.

Quadrant Functional Logic Diagram ATV5000

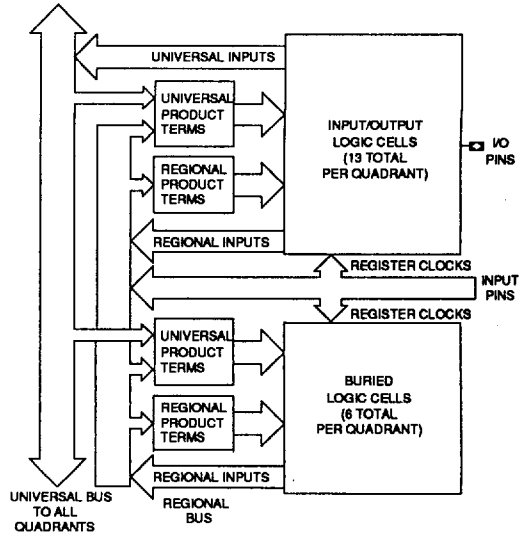


Figure 1

D.C. and A.C. Operating Range

		ATV5000-25	ATV5000/L-30	ATV5000/L-35
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%	5 V ± 10%

ATV5000 Block Diagram

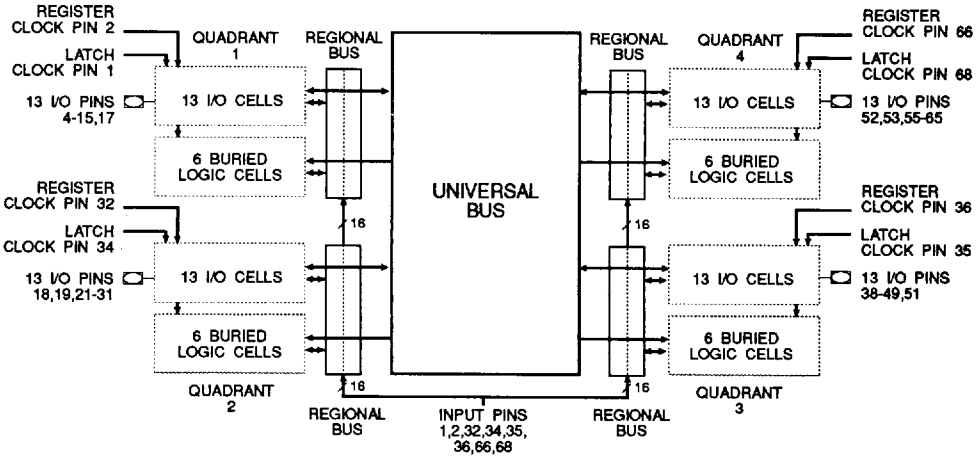


Figure 2

Quadrant Logic Diagram and Description

The ATV5000 has: four identical quadrants, 52 identical input/output logic cells, and 24 identical buried logic cells. The universal bus routes true and false signals from each of the 52 I/O pins to all four quadrants. Regional buses route each quadrant's flip-flop Q and $\overline{Q}$ locally. The eight input-only pins are available in every regional bus.

Each logic cell has a number of "regional" and "universal" product terms (see Figure 3). The I/O logic cells (Figures 7, 8, 9) contain three sum terms, two flip-flops, and an I/O buffer. Sum term B has five product terms - two universal and three regional. Sum terms A and C each have four product terms - one universal and three regional. Flip-flop Q1 has global asynchronous preset, reset, and clock product terms. Flip-flop Q2 has universal asynchronous reset and clock terms and a regional asynchronous preset term. There is one universal product term for the I/O pin output enable.

The buried logic cells (Figure 4) each contain one flip-flop. The sum term has one universal product term and four regional product terms for a total of five. The flip-flop has universal asynchronous preset, reset, and clock terms. In addition, in each buried logic cell the sum term can be fed back into the regional bus instead of the flip-flop. This allows for logic expansion.

Regional product terms have as inputs all quadrant flip-flop outputs (or buried flip-flop inputs) and the eight dedicated input pins. Universal product terms have the same inputs plus the 52 I/O pins and their complements.

Quadrant Clock Pin Assignments

Quadrant Number	Register Clock Pin	Latch Clock Pin
1	2	1
2	32	34
3	36	35
4	66	68

Quadrant Structure

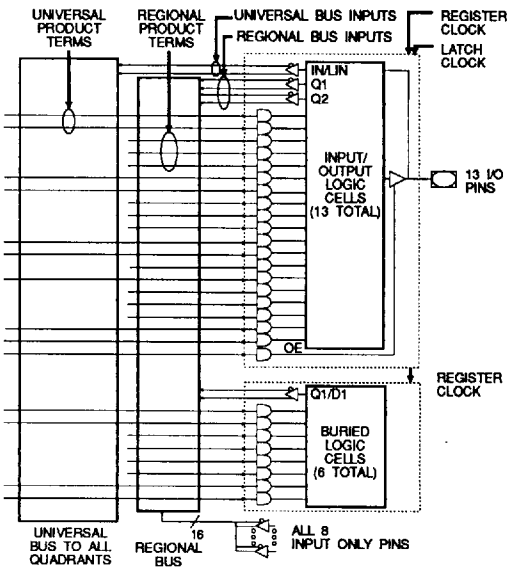


Figure 3

Logic Cell Options

The ATV5000 logic cells contain most of the chip's logic options. The standard logic cell contains two flip-flops, three sum terms and three array inputs. The three sum terms can be combined to provide sum term options of four, five, nine, or 13 product terms. A combinatorial signal or the output of Q1 can be sent to the I/O cell.

The ATV5000 retains the ATV2500's ability to bury both registers in the I/O cell and still output a combinatorial signal (see Figure 8). A new feature, unique to the ATV5000, is the ability to output Q1 and feedback the combinatorial term directly (see Figure 7). This high speed logic expansion term increases the devices flexibility and gate utilization.

Buried Logic Cells

Each quadrant has six buried logic cells (see Figure 4). Each cell contains one sum term with five product terms, a flip-flop, and individual preset, clear, and clock terms. A configuration bit selects either the Q output or the D input for feedback into the regional bus.

Buried Logic Cells

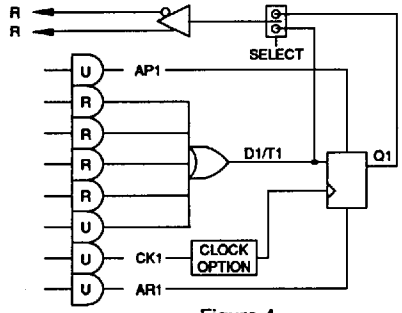


Figure 4

Clock Option

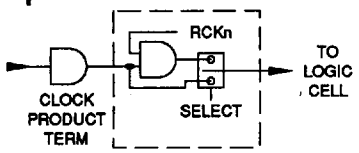


Figure 5

I/O Pin Logic

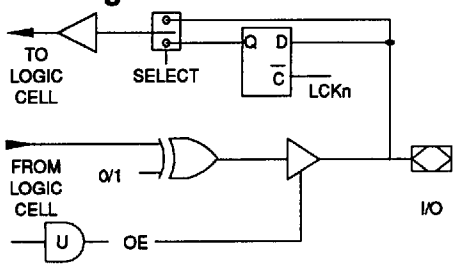


Figure 6

Logic Cell with Buried Sum Term and Register to I/O Cell

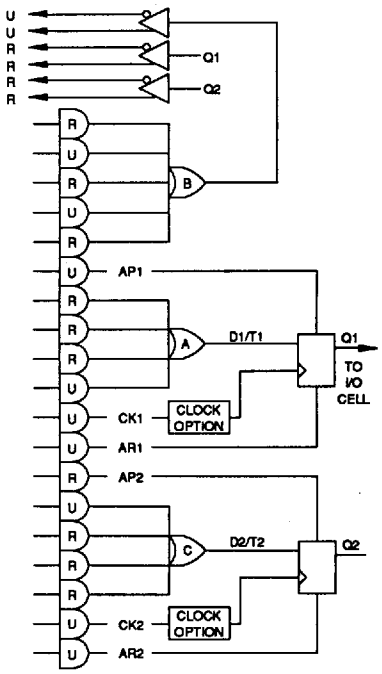


Figure 7

Flip-Flop Clock Options

Each register may be connected to its regional clock to provide fast clock-to-output timing (see Figure 5). In this "synchronous" mode, the clock is one of four input pins, a unique clock pin for each chip quadrant. One product term defines each flip-flop's clock in the "asynchronous" mode.

In the "synchronous" mode, the regional clock is ANDed with the product term. This provides the fast timing of a synchronous clock with the local control of the product term.

I/O Pin Latches

Each I/O pin of the ATV5000 has an input latch which can be individually enabled or disabled (see Figure 6). Each chip quadrant has a unique latch clock. When the latch is inactive, pin input flows directly into the array. When activated, the latch is flow-through when the clock signal is low, and data is captured on the clock's rising edge.

Flip-Flop Types

Each flip-flop in the ATV5000 may be configured as either a T- or D-type flip-flop. A T-type flip-flop can also easily be configured into a JK or SR flip-flop.

Logic Cell, Two Buried Registers, Combinatorial to I/O Cell

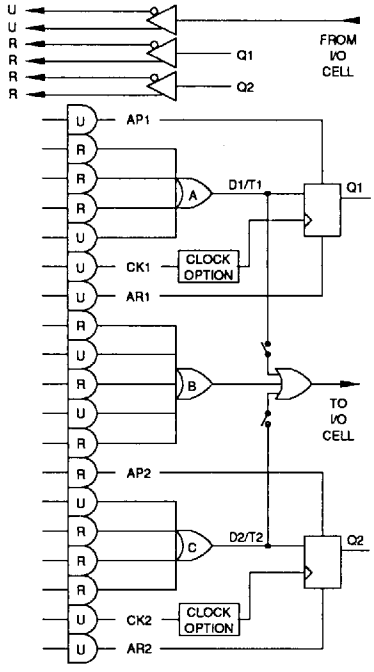


Figure 8

Logic Cell with Combinable Sum Terms, Register to I/O Cell

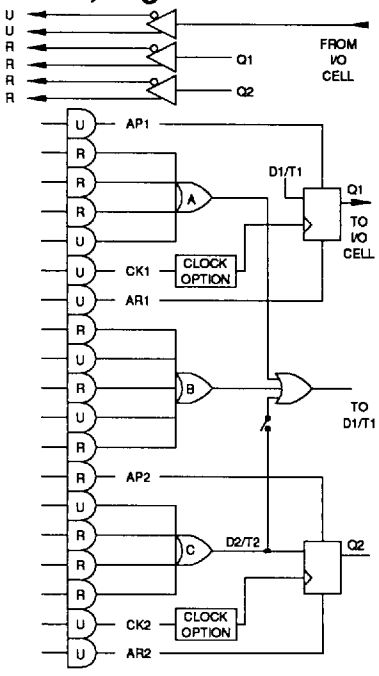


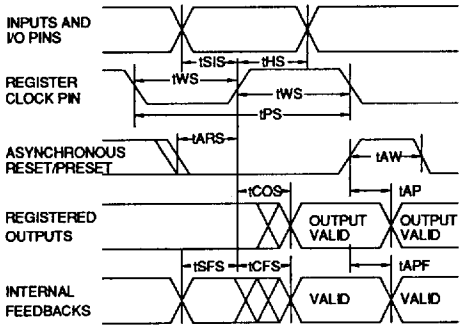
Figure 9

D.C. Characteristics

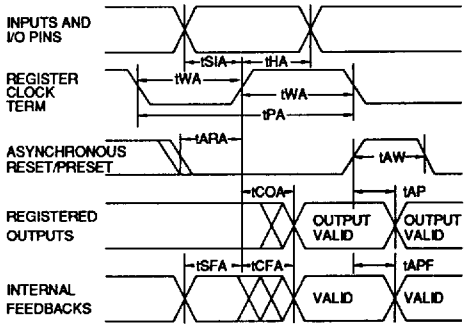
Symbol	Parameter	Condition		Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+1 V				10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC}+0.1 V				10	µA
I_{CC}	Power Supply Current ATV5000	V_{CC} = MAX, V_{IN} = GND or V_{CC} Outputs Open	Com.		200	350	mA
			Ind.,Mil.		200	400	mA
I_{CC}	Power Supply Current ATV5000L	V_{CC} = MAX, V_{IN} = GND or V_{CC} Outputs Open	Com.		32	40	mA
			Ind.,Mil.		32	50	mA
I_{CC2}	Clocked Power Supply Current, ATV5000L Only	f = 1 MHz, V_{CC} = MAX Outputs Open	Com.		30	50	mA
			Ind.,Mil.		30	60	mA
I_{OS} (1)	Output Short Circuit Current	V_{OUT} = 0.5 V				-90	mA
V_{IL}	Input Low Voltage			-0.6		0.8	V
V_{IH}	Input High Voltage			2.0		V_{CC}+0.75	V
V_{OL}	Output Low Voltage	V_{IN} = V_{IH} or V_{IL}, I_{OL} = 8 mA Com,Ind; 6 mA Mil.				0.5	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA		V_{CC}-0.3			V
		I_{OH} = -4.0 mA		2.4			V

Note: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 seconds.

A.C. Waveforms [1] Input Pin Clock



A.C. Waveforms [1] Product Term Clock



Notes: 1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

Register A.C. Characteristics, Input Pin Clock

		ATV5000-25		ATV5000/L-30		ATV5000/L-35		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Units
t_{COS}	Clock to Output		15		20		25	ns
t_{CFS}	Clock to Feedback	0	9	0	12	0	15	ns
t_{SIS}	Input Setup Time[1]	16		17		20		ns
t_{SFS}	Feedback Setup Time[1]	11		13		15		ns
t_{HS}	Hold Time	0		0		0		ns
t_{WS}	Clock Width	10		12		15		ns
t_{PS}	Clock Period	20		25		30		ns
F_{MAXS}	Maximum Frequency (1/t_{PS})		50		40		33	MHz
t_{ARS}	Asynchronous Reset/Preset Recovery Time	20		25		30		ns

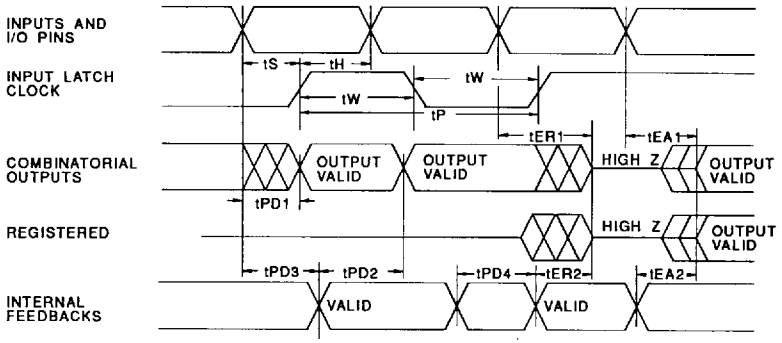
Note: 1. Add 3 ns for Universal Product Terms.

Register A.C. Characteristics, Product Term Clock

		ATV5000-25		ATV5000/L-30		ATV5000/L-35		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Units
t_{COA}	Clock to Output		25		30		35	ns
t_{CFA}	Clock to Feedback	7	20	10	25	12	27	ns
t_{SIA}	Input Setup Time[1]	10		12		15		ns
t_{SFA}	Feedback Setup Time[1]	5		8		13		ns
t_{HA}	Hold Time	8		10		12		ns
t_{WA}	Clock Width	12		15		15		ns
t_{PA}	Clock Period	25		33		40		ns
F_{MAXA}	Maximum Frequency (1/t_{PA})		40		30		25	MHz
t_{ARA}	Asynchronous Reset/Preset Recovery Time	15		20		25		ns

Note: 1. Add 3 ns for Universal Product Terms.

A.C. Waveforms [1]



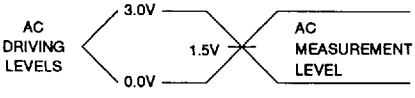
Notes: 1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

A.C. Characteristics

Symbol	Parameter	ATV5000-25 Min	ATV5000-25 Max	ATV5000/L-30 Min	ATV5000/L-30 Max	ATV5000/L-35 Min	ATV5000/L-35 Max	Units
t_{PD1}	Input to Non-Registered Output[1]		25		30		35	ns
t_{PD2}	Feedback to Non-Registered Output[1]		20		25		30	ns
t_{PD3}	Input to Non-Registered Feedback[1]		20		25		30	ns
t_{PD4}	Feedback to Non-Registered Feedback[1]		15		18		22	ns
t_{EA1}	Input to Output Enable		30		35		40	ns
t_{ER1}	Input to Output Disable		30		35		40	ns
t_{EA2}	Feedback to Output Enable		25		30		35	ns
t_{ER2}	Feedback to Output Disable		25		30		35	ns
t_S	Input Latch Setup Time	5		6		7		ns
t_H	Input Latch Hold Time	5		5		5		ns
t_W	Clock Width	10		12		12		ns
t_P	Clock Period	20		25		30		ns
F_{MAX}	Maximum Frequency ($1/t_P$)		50		40		33	MHz
t_{AW}	Asynchronous Reset/Preset Width	15		20		20		ns
t_{AP}	Asynchronous Reset/ Preset to Registered Output		30		35		40	ns
t_{APF}	Asynchronous Reset/ Preset to Registered Feedback		25		30		35	ns

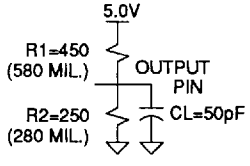
Note: 1. Add 3 ns for Universal Product Terms.

Input Test Waveforms and Measurement Levels



t_R, t_F < 5 ns (10% to 90%)

Output Test Load



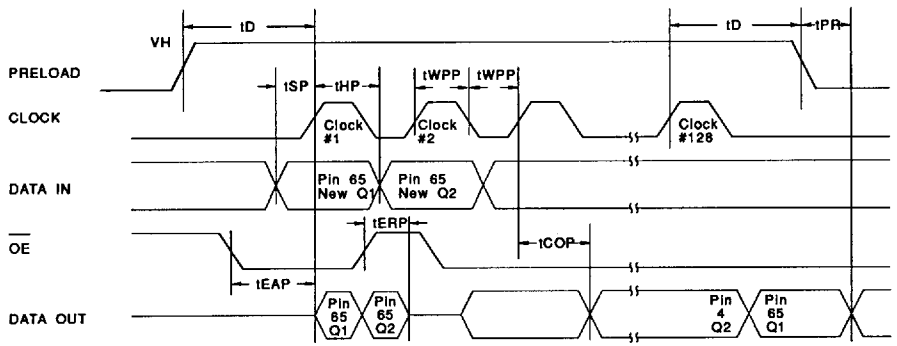
Preload and Observability of Registers

The ATV5000's registers include circuity to load and unload them serially. This feature simplifies testing. Any state can be forced into the registers to control test sequencing, and all registers may be observed, independent of being buried. A V_{IH} level on the Data In pin will force the appropriate register high; a V_{IL} will force it low, independent of the polarity or other configuration bit settings.

The preload/observe state is entered by placing an 11-V to 14-V signal on pin 68 on the JLCC. When the clock (pin 1) is pulsed high, data (pin 2) is clocked serially through all registers in the device, as in the following table. All register contents are also clocked out of the device on Pin 65 in FIFO fashion. If observability only is required, data out should be connected back to data in. If preload only is required, OE (pin 66) can be held high and data out (pin 65) will remain high impedance.

Any user contemplating the use of register preload/obervability is encouraged to contact Atmel's PLD applications department.

Note: All register clock terms or pins must be low prior to entering the preload/observe state, and low prior to leaving the preload/observe state. Pin 1 must be low prior to entering the preload/observe state.



tD_{MIN} = 100 ns
tSP_{MIN} = 50 ns
tHP_{MIN} = 50 ns
$tWPP_{MIN}$ = 100 ns
tPR_{MIN} = 1000 ns
$tERP_{MAX}$ = 100 ns
$tEAP_{MAX}$ = 100 ns
$tCOP_{MAX}$ = 100 ns

Preload / Observe Register Scan Order

Quadrant	Pin																			
Quadrant 1	Pin	4				5			6			•••			15			17		
	D_{IN}	→ Q2	→ Q1	→ B23	→ Q2	→ Q1	→ Q2	→ Q1	•••	B18	→ Q2	→ Q1	→ Q2	→ Q1	→ (Quadrant 2)					
Quadrant 2	Pin	18			19			21			22		•••			31				
(Quadrant 1)→		Q2	→ Q1	→ Q2	→ Q1	→ B17	→ Q2	→ Q1	→ Q2	→ Q1	•••	B12	→ Q2	→ Q1	→ (Quadrant 3)					
Quadrant 3	Pin	38			39			40			•••			49			51			
(Quadrant 2)→		Q2	→ Q1	→ B11	→ Q2	→ Q1	→ Q2	→ Q1	•••	B6	→ Q2	→ Q1	→ Q2	→ Q1	→ (Quadrant 4)					
Quadrant 4	Pin	52			53			55			56		•••			65				
(Quadrant 3)→		Q2	→ Q1	→ Q2	→ Q1	→ B5	→ Q2	→ Q1	→ Q2	→ Q1	•••	B0	→ Q2	→ Q1	→ D_{OUT}					

Power Up Reset

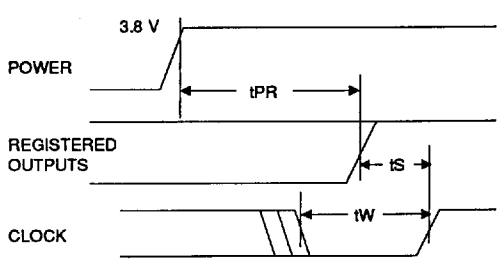
The registers in the ATV5000 are designed to reset during power up. At a point delayed slightly from V_{CC} crossing 3.8 V, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1) The V_{CC} rise must be monotonic,

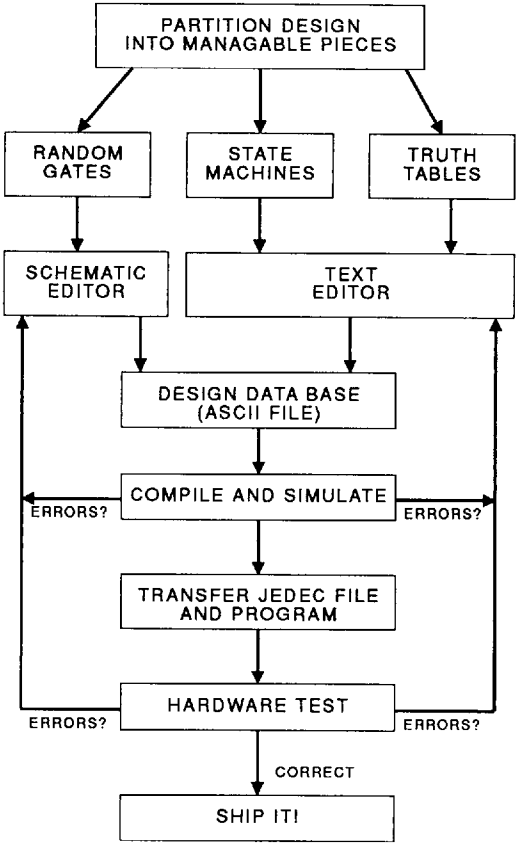
2) After reset occurs, all input and feedback setup times must be met before driving the clock term high, and

3) The signals from which the clock is derived must remain stable during t_{PR}.



Parameter	Description	Min	Typ	Max	Units
t_{PR}	Power-Up Reset Time		600	1000	ns

Design Flow Diagram



Using The ATV5000

The ATV5000's simple, regular architecture means that only simple logic compilers are required to configure the device. No layout or route and place are required. These software tools are readily available from companies such as Data I/O Corporation (Abel™), Logical Devices (Cupl™), and ISDATA (LOGiC™).

The first step in designing a device as complex as the ATV5000 is to partition your design into manageable blocks. These blocks are then allocated proportionally to each of the four quadrants of the ATV5000. Random gates can be described either with boolean equations (a behavioral description) or with a schematic editor. Truth table logic and state machines are best described behaviorially and entered with a text editor. The design is then combined into one ASCII file, which is then submitted to the logic compiler. Compilation, logic reduction, simulation, JEDEC file creation and documentation are then completed by all of the popular compilers.

Assignment of signals to pins or buried nodes as well as selecting the various options of the ATV5000 (such as register clocks and input latches) can be done manually in the design data base file, or an automatic fitter may be used.

A logic fitter assigns pins and nodes to make best use of the features in the ATV5000, and frees the designer from being required to learn all of the features of a complex device such as the ATV5000. For further information on fitters for the ATV5000, contact Atmel's PLD applications department.

After correcting any syntax and logic errors discovered by the compiler, the JEDEC file is ready to download to an PLD programmer. These are available from a number of manufacturers. Programmed devices are usually first tested in the programmer with your supplied test vectors. The next step is check out your "custom chip" in the target system. When this hardware debug step is complete, your system is ready to go— all in a matter of hours.

Abel™, Cupl™ and LOGiC™ may be trademarks of others.

Operating Modes

	68-Lead LCC Pin								
Mode	1	2	36	34	68	66	Vcc (3,20,37,54)	I/O's	I/O Pin 65
"PLD"	X (1)	X	X	X	X	X	5V	I/O	I/O
Program	V_{PP}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	6V	ADD/D_{IN}	ADD
PGM Verify	V_{PP}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	X	6V	ADD/D_{OUT}	ADD
PGM Inhibit	V_{PP}	V_{IH}	V_{IH}	V_{IH}	V_{IH}	X	6V	High Z	High Z
Preload/Observe	⎍	D_{IN}	X	X	V_H (2)	$\overline{OE}$	5V	High Z	D_{OUT}

Notes: 1. X can be V_{IL} or V_{IH}.
2. V_H = 11.0 V to 14.0 V

ATV5000 PLCC/PGA Pin Assignments

PLCC Pin	PGA Pin	Name	PLCC Pin	PGA Pin	Name	PLCC Pin	PGA Pin	Name	PLCC Pin	PGA Pin	Name
1	B6	IN	18	F2	I/O	35	K6	IN	52	F10	I/O
2	A6	IN	19	F1	I/O	36	L6	IN	53	F11	I/O
3	B5	VCC	20	G2	VCC	37	K7	VCC	54	E10	VCC
4	A5	I/O	21	G1	I/O	38	L7	I/O	55	E11	I/O
5	B4	I/O	22	H2	I/O	39	K8	I/O	56	D10	I/O
6	A4	I/O	23	H1	I/O	40	L8	I/O	57	D11	I/O
7	B3	I/O	24	J2	I/O	41	K9	I/O	58	C10	I/O
8	A3	I/O	25	J1	I/O	42	L9	I/O	59	C11	I/O
9	A2	I/O	26	K1	I/O	43	L10	I/O	60	B11	I/O
10	B2	I/O	27	K2	I/O	44	K10	I/O	61	B10	I/O
11	B1	I/O	28	L2	I/O	45	K11	I/O	62	A10	I/O
12	C2	I/O	29	K3	I/O	46	J10	I/O	63	B9	I/O
13	C1	I/O	30	L3	I/O	47	J11	I/O	64	A9	I/O
14	D2	I/O	31	K4	I/O	48	H10	I/O	65	B8	I/O
15	D1	I/O	32	L4	IN	49	H11	I/O	66	A8	IN
16	E2	GND	33	K5	GND	50	G10	GND	67	B7	GND
17	E1	I/O	34	L5	IN	51	G11	I/O	68	A7	IN

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	6	8	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATV5000 fuse patterns. Once programmed, all outputs appear programmed during verify. The security fuse should be programmed last (after verifying all other programmed bits), as its effect is immediate.

The security fuse also inhibits preload and observability.

Erasure Characteristics

The entire memory array of an ATV5000 is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 $W \cdot sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable PLD which will be subjected to continuous fluorescent indoor lighting or sunlight.

Ordering Information

t_{PD} (ns)	t_{COS} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
25	15	50	ATV5000-25JC ATV5000-25KC ATV5000-25UC	68J 68KW 68UW	Commercial (0°C to 70°C)
			ATV5000-25KI ATV5000-25UI	68KW 68UW	Industrial (-40°C to 85°C)
			ATV5000-25KM ATV5000-25UM	68KW 68UW	Military (-55°C to 125°C)
30	20	40	ATV5000-30JC ATV5000-30KC ATV5000-30UC	68J 68KW 68UW	Commercial (0°C to 70°C)
			ATV5000-30KI ATV5000-30UI	68KW 68UW	Industrial (-40°C to 85°C)
			ATV5000-30KM ATV5000-30UM	68KW 68UW	Military (-55°C to 125°C)
			ATV5000-30KM/883 ATV5000-30UM/883	68KW 68UW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
35	25	33	ATV5000-35JC ATV5000-35KC ATV5000-35UC	68J 68KW 68UW	Commercial (0°C to 70°C)
			ATV5000-35KI ATV5000-35UI	68KW 68UW	Industrial (-40°C to 85°C)
			ATV5000-35KM ATV5000-35UM	68KW 68UW	Military (-55°C to 125°C)
			ATV5000-35KM/883 ATV5000-35UM/883	68KW 68UW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

t_{PD} (ns)	t_{COS} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
30	20	40	ATV5000L-30JC ATV5000L-30KC ATV5000L-30UC	68J 68KW 68UW	Commercial (0°C to 70°C)
35	25	33	ATV5000L-35JC ATV5000L-35KC ATV5000L-35UC	68J 68KW 68UW	Commercial (0°C to 70°C)
			ATV5000L-35KI ATV5000L-35UI	68KW 68UW	Industrial (-40°C to 85°C)
			ATV5000L-35KM ATV5000L-35UM	68KW 68UW	Military (-55°C to 125°C)
			ATV5000L-35KM/883 ATV5000L-35UM/883	68KW 68UW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
68J	68 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
68KW	68 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
68UW	68 Pin, Windowed, Ceramic Pin Grid Array (PGA)