Rockwell

RS701/RS702
Gallium Arsenide
16-Bit Mux/Demux Chip Set

Features

- Serial data rates up to 3 Gbits/sec
- 16-bit wide ECL-compatible parallel data I/O
- Advanced HBT GaAs process yields high margins and very fast edge rates
- High speed differential serial data I/O and clock inputs (optionally single-ended)
- Fully differential internal logic minimizes skew and jitter
- Built-in phase comparator on RS701 Mux
- Low power dissipation: RS701 Mux - 1.5 W (typ.), RS702 Demux - 1.3 W (typ.)
- Standard power supplies: V_{EE} = -5.2 V, V_{CCP} = +5.0 V, V_{TT} = -2.0 V
- Choice of commercial (0 to 70 °C) or industrial (-40 to +85 °C) temperature ranges
- Package: high performance 52-pin plastic quad flatpack (PQFP)

Applications

- Fiber optic communication systems (OC-48)
- Data and video transmission
- Computers
- Digital signal processing
- Pin electronics for automated test equipment
- SONET testers

Functional Description

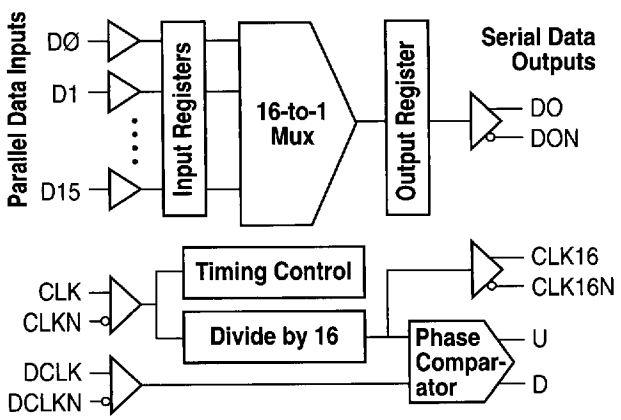
The RS701 Mux and RS702 Demux are parallel-to-serial and serial-to-parallel digital data conversion ICs capable of serial rates up to 3 Gbits/sec. Fabricated using Rockwell's advanced AlGaAs/GaAs HBT (heterojunction bipolar transistor) process, these devices provide high speed coupled with low power dissipation. All internal logic is differential to minimize signal skew and jitter. High speed data and clock signals are also differential, but may be used single-ended. To ease system design, both devices use industry standard power supplies and ECL-compatible I/Os for parallel data. These devices are ideal for applications including fiber optic communications, data transmission, test equipment, and instrumentation.

RS701 Multiplexer

The RS701 contains a 16-to-1 mux, a phase comparator, and a timing circuit which generates a divide-by-16 clock from the high speed clock input. The 16-to-1 mux accepts 16 parallel single-ended ECL compatible inputs (DØ through D15) and serializes them bitwise into data stream present at output DO/DON.

All internal timing is referenced to the falling edge of the true input of the high speed clock, CLK/CLKN, which is divided by 16 in the timing circuit and provided as output CLK16. The setup and hold time of the parallel inputs (DØ-D15) are specified with respect to the falling edge of CLK16, so that CLK16 can be used to clock the data source of DØ-D15.

Figure 1: RS701 Multiplexer Logic Diagram



The RS701's internal phase comparator monitors the relationship between the internally generated divide-by-16 clock and an externally supplied low speed reference clock input DCLK/DCLKN. Phase differences detected between these two clock signals in the phase comparator will generate an up or down output (U, D) for phase lock applications. Using the U and D signals, the phase

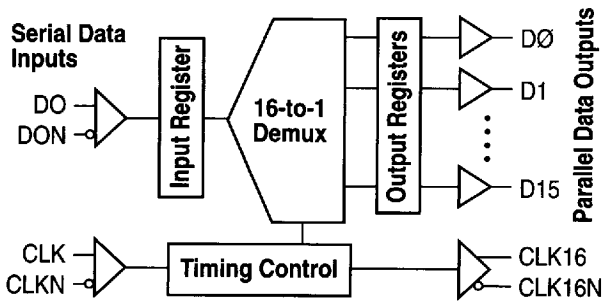
comparator can be used as part of an external phase-locked loop (PLL) to perform a clock multiplication function.

In applications that can provide a high speed system clock and do not require the phase comparator, the DCLK input should be connected to V_{TT} through a 50 ohm resistor. The U and D outputs can be left unconnected.

RS702 Demultiplexer

The RS702 contains a 1-to-16 demux and timing circuitry to generate a divide-by-16 clock from the high speed clock input CLK/CLKN. The demultiplexer accepts serial data through inputs DI/DIN and deserializes it into 16 parallel single-ended ECL compatible outputs present at DØ-D15. All internal timing of the RS702 is referenced to the falling edge of the true input of the high speed clock, CLK/CLKN. This clock is divided by 16 and provided as output CLK16. The timing of the parallel data outputs (DØ-D15) are synchronized with respect to the falling edge of CLK16, so that CLK16 can be used to clock the destination of DØ-D15.

Figure 2: RS702 Demultiplexer Logic Diagram



RS701 Phase Detector

The RS701's phase detector compares the internally generated divide-by-16 clock (ICLK) and the DCLK input. If both signals are in phase, the U and D outputs will both be low. If the rising edge of ICLK precedes DCLK, a series of pulses with a width proportional to the phase difference will be present at the U output. Conversely, if the rising edge of DCLK precedes ICLK, a series of pulses with widths proportional to the phase difference will be present at the D output. In each case, the other output (U or D) will remain low. The phase detector ignores phase differences for falling edges.

The phase detector circuit is useful for applications that implement clock multiplication for the RS701. DCLK can be used as the system reference clock at the parallel data rate. An external voltage controlled oscillator (VCO) at 16 times the frequency of the reference clock can be used as the CLK input for the RS701. The phase detector outputs (U and D) can then be used by an external integrator to generate an output that controls the VCO so the high speed clock is phase-locked to the reference clock.

Figure 3: RS701 Phase Detector Logic Diagram

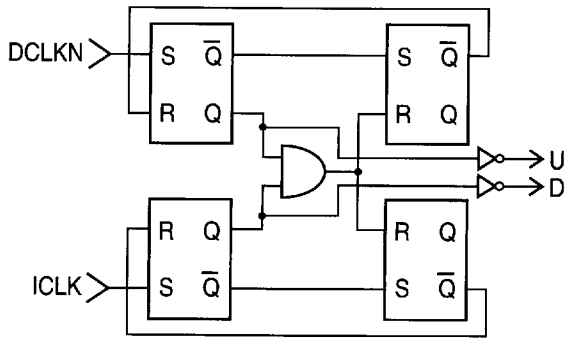
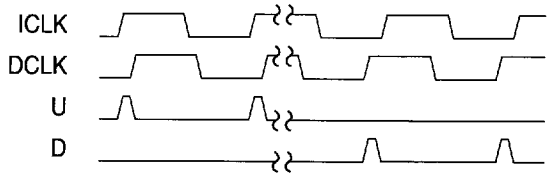


Figure 4: RS701 Phase Detector Waveforms



GaAs HBT Fabrication Process

Fabrication of the RS701 and RS702 is accomplished using a proprietary AlGaAs/GaAs HBT (heterojunction bipolar transistor) process developed at Rockwell over a five year period. Using this process, a variety of circuits, including prescalers, gain blocks, and digital-to-analog converters have been successfully fabricated with high yields. The performance of some of these devices have exceeded frequencies of 10 GHz, with HBT's typically exhibiting f_T and f_{MAX} between 50 and 60 GHz.

The process features high noise margins, low input capacitance, ultrahigh speed, relatively low power, and high output drive current. Three layers of metal are used for signal routing and power distribution.

AC Characteristics, RS701 Multiplexer (over recommended operating conditions)

Parameter	Description	Min	Nom	Max	Units
t_{CLK} [1]	Clock Period	330	400	—	ps
t_D [1]	CLK16, DCLK period (t_{CLK} x 16)	5 3	6 4	—	ns
t_{SU}	Data setup time (write after CLK16 falling edge)	2 0	—	—	ns
t_H	Data hold time (write after CLK16 falling edge)	0.5	—	—	ns
t_{DC}	CLK16 duty cycle	40	—	60	%
t_r, t_f	DCLK rise and fall times (10% - 90%)	—	—	1.5	ns
t_r, t_f	DØ - D15 rise and fall times (10% - 90%)	—	—	2.0	ns
t_r, t_f	CLK16 rise and fall times (10% - 90%)	—	0.5	0.8	ns
t_r, t_f	DO, DON rise and fall times (20% - 80%)	—	120	140	ps

NOTES
[1] All parameters are based on t_{CLK} If a different t_{CLK} period is specified, all other parameters will change as well

RS701 Multiplexer Waveforms

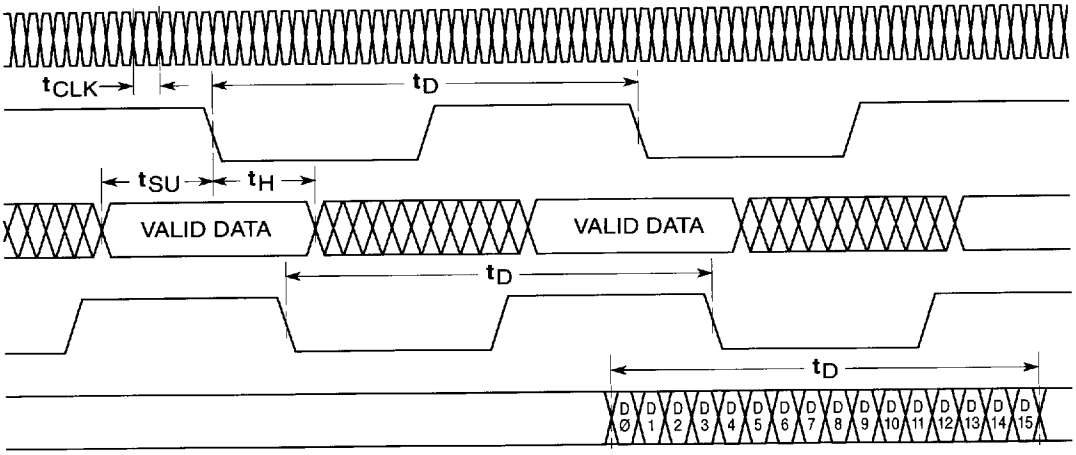
CLK, CLKN
High speed clock input

CLK16
Divide by 16 parallel data clock output

DØ-D15
Parallel data inputs

DCLK
Divide by 16 parallel data clock input

DO, DON
High speed serial data output

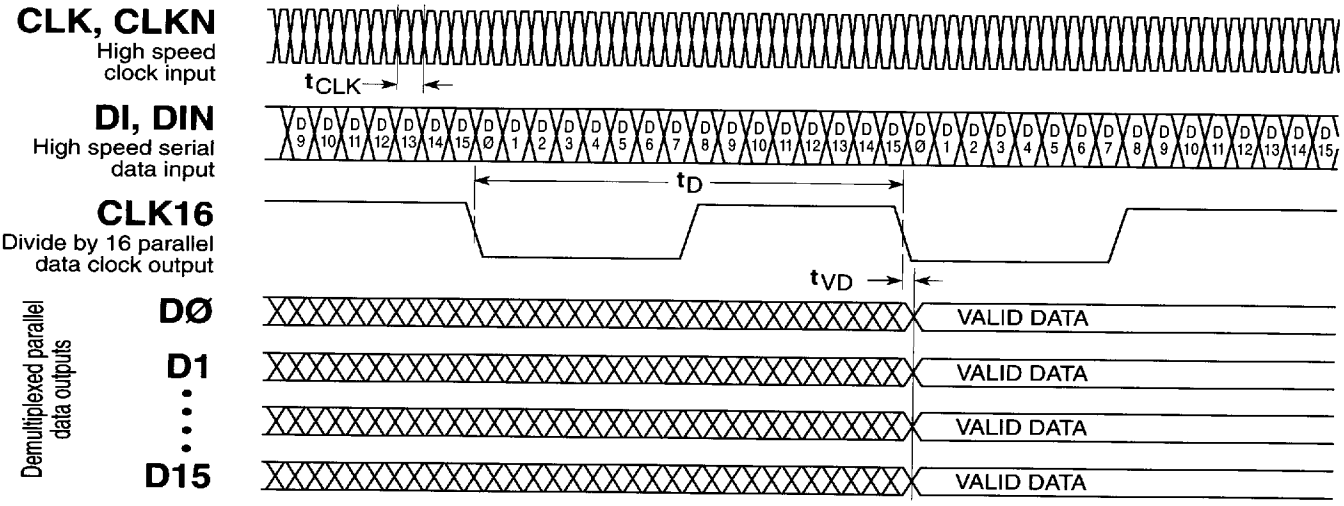


AC Characteristics, RS702 Demultiplexer (over recommended operating conditions)

Parameter	Description	Min	Nom	Max	Units
t_{CLK} [1]	Clock Period	330	400	—	ps
t_D	CLK16, DCLK period (t_{CLK} x 16)	5.3	6.4	—	ns
t_{VD}	CLK16 falling edge output to valid data	1.0	—	3.0	ns
phase margin	Serial data phase margin with respect to high speed clock Phase Margin = $\left(1 - \frac{t_{SU} + t_H}{t_{CLK}}\right)$ X 360° [3]	225 [2]	—	—	degrees

NOTES
[1] All parameters are based on t_{CLK} If a different t_{CLK} period is specified, all other parameters will change as well.
[2] At t_{CLK} = 400 ps
[3] t_{SU} and t_H are setup and hold times for the serial data input registers

RS702 Demultiplexer Waveforms



Absolute Maximum Ratings [1]

Power Supply Voltage (V_{CC}) ..... GND
Power Supply Voltage (V_{CCP}) ..... V_{CC} to +6.0 V
Power Supply Voltage (V_{EE}) ..... V_{CC} to -6.0 V
Input Voltage Applied (V_{ECLIN}) ..... -2.5 to 0.5 V
High Speed Input Voltage Applied (V_{HSIN}) ..... V_{EE} - 0.7 to V_{CC} + 0.7 V
DC Output Current (I_{OUT}, output high) ..... -50 mA
Case Temperature Under Bias (T_C) ..... -55 to 125 °C
Storage Temperature (T_{STG}) ..... -65 to 150 °C

NOTES.
[1] Stresses listed above may be applied to devices one at a time without causing damage. Functionality is not guaranteed at or above the values listed and exposure to these values for extended periods may affect device reliability.
[2] V_{TT} must be applied before any input signal voltage is applied

Recommended Operating Conditions

Power Supply Voltage (V_{CC}) ..... GND
Power Supply Voltage (V_{TT}) ..... -2.0 V ±5%
Power Supply Voltage (V_{CCP}) ..... 5.0 V ±5%
Power Supply Voltage (V_{EE}) ..... -5.2 V ±5%
Operating Temperature Range, Commercial (**T**) ..... [1] 0 to 70 °C
Operating Temperature Range, Industrial (**T**) ..... [1] -45 to 85 °C

NOTE
1) Temperature specifications are case.

DC Characteristics, ECL Inputs and Outputs

(over recommended operating conditions, V_{CC} = GND, outputs terminated with 50 Ω to -2.0 V)

Parameter	Description	Min	Nom	Max	Units	Conditions
V_{OH}	Output high voltage [1]	-1100	—	-700	mV	V_{IN} = V_{IH} (max) or V_{IL} (min)
V_{OL}	Output low voltage [1]	V_{TT}	—	-1750	mV	V_{IN} = V_{IH} (max) or V_{IL} (min)
V_{IH}	Input high voltage	-1600	—	-1200	mV	Guaranteed high for all inputs [2]
V_{IL}	Input low voltage	-2400	—	-2000	mV	Guaranteed low for all inputs [2]
V_{IHR}	Input high voltage, RESET	—	-1200	—	mV	—
V_{ILR}	Input low voltage, RESET	—	-1400	—	mV	—
ΔV_{ECLOUT}	Output voltage swing	0.85	—	—	V	Output load 50 Ω to V_{TT}
ΔV_{ECLIN}	Input voltage swing	0.20	0.40	1.2	V	AC coupled

NOTES
1) ECL output pairs must be terminated identically.
2) V_{IH} and V_{IL} for all ECL inputs except RESET (see V_{ILR} and V_{IHR})

Specifications for High Speed Inputs and Outputs

(over recommended operating conditions, V_{CC} = GND, outputs terminated with 50 Ω to -2.0 V)

Parameter	Description	Min	Nom	Max	Units	Conditions
ΔV_{HSOUT}	Output voltage swing	0.7	0.9	—	V	Output load 50 Ω to -2 0 V
ΔV_{HSIN}	Input voltage swing	0.6	0 7	1.2	V	AC coupled
T_R, T_F	Input voltage rise/fall time	—	0 2	1.5	ns	Same for all data rates

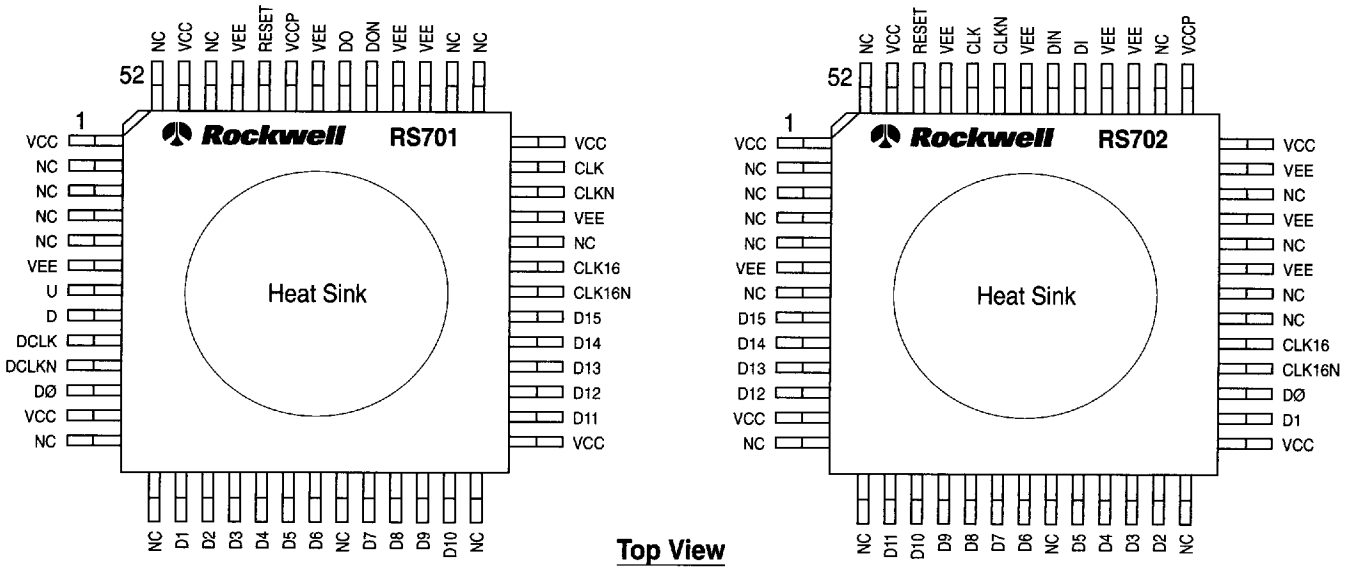
NOTE High speed inputs are designed for AC coupling In applications where high speed input are driven single-ended, a capacitor should be connected between the unused input and V_{TT}

Power Dissipation (over recommended operating conditions, V_{CC} = GND, outputs open)

Parameter	Description	**RS701** (max)	**RS702** (max)	Units
I_{EE}	V_{EE} supply current	290	240	mA
I_{CCP}	V_{CCP} supply current	30	40	mA
P_D	Power dissipation	1 7	1.4	W

NOTE. If all output signals of the RS701/RS702 are connected to V_{TT} through a 50 ohm resistor, then each output will draw 20 mA from the V_{TT} supply The power dissipated across the resistor will be 20 mW

RS701/RS702 Pin Configurations for 52-Pin PQFP



Top View

RS701 Pin Description for 52-Pin PQFP

Pin #	Name	I/O	Description
38	CLK	I	High speed clock input, true
37	CLKN	I	High speed clock input, complement
9	DCLK	I	Data clock input, true, ECL
10	DCLKN	I	Data clock input, complement, ECL
34	CLK16	O	Clock divide-by-16, true, ECL
33	CLK16N	O	Clock divide-by-16, complement, ECL
11,15-20, 22-25, 28-32	DØ-D15	I	Parallel data inputs, ECL
45	DO	O	High speed serial data output, true
44	DON	O	High speed serial data output, complement
7	U	O	Up frequency phase comparator output, ECL
8	D	O	Down frequency phase comparator output, ECL
1,12,27, 39,51	V_{CC}	—	Most positive supply voltage connection
6,36,42, 43,46,49	V_{EE}	—	SCFL negative supply voltage connection
47	V_{CCP}	—	+5V with respect to V_{CC}
2-5,13,14, 21,26,35, 40,41,50, 52	NC	—	No connection, leave open
48	Reset	I	ECL input. Leave open if not used.[1]

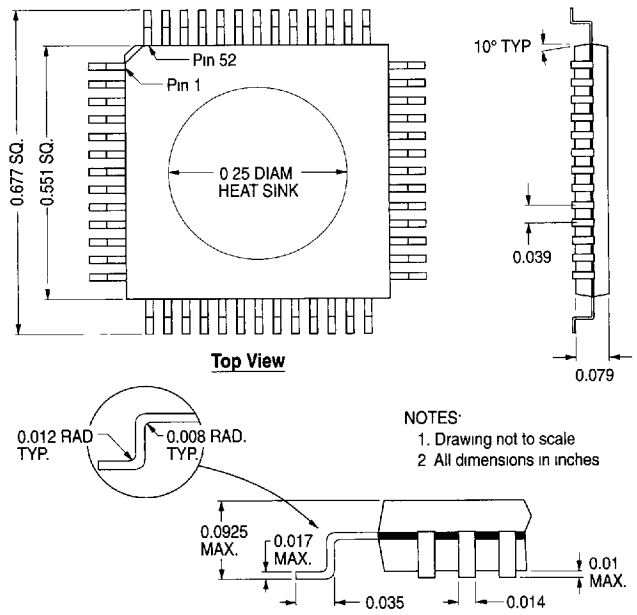
NOTE: 1) Reset pin has different V_{IH} and V_{IL} levels than other ECL inputs See *DC Characteristics, ECL Inputs and Outputs.*

RS702 Pin Description for 52-Pin PQFP

Pin #	Name	I/O	Description
48	CLK	I	High speed clock input, true
47	CLKN	I	High speed clock input, complement
44	DI	I	High speed serial data input, true
45	DIN	I	High speed serial data input, complement
31	CLK16	O	Clock divide-by-16, true, ECL
30	CLK16N	O	Clock divide-by-16, complement, ECL
8-11,15-20, 22-25,28,29	DØ-D15	O	Parallel data outputs, ECL
1,12,27, 39,51	V_{CC}	—	Most positive supply voltage connection
6,34,36,38, 42,43,46, 49	V_{EE}	—	SCFL negative supply voltage connection
40	V_{CCP}	—	+5V with respect to V_{CC}
2-5,7,13, 14,21,26, 32,33,35, 37,41,52	NC	—	No connection, leave open
50	Reset	—	ECL input. Leave open if not used.[1]

NOTE: 1) Reset pin has different V_{IH} and V_{IL} levels than other ECL inputs See *DC Characteristics, ECL Inputs and Outputs.*

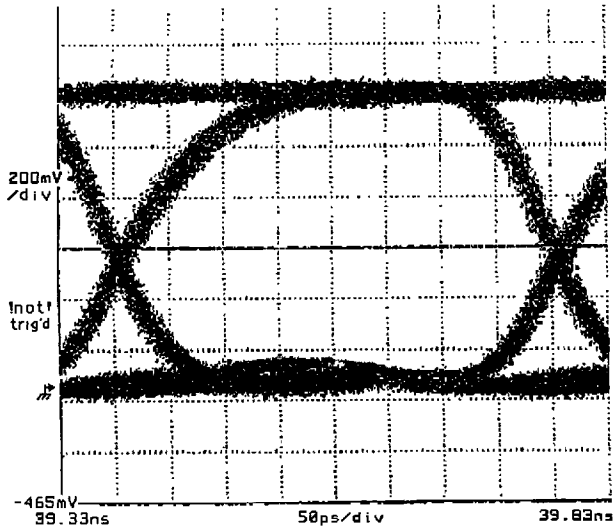
52-Pin PQFP Package Dimensions



Packaging

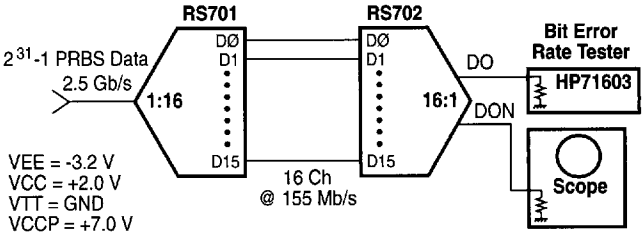
The RS701 and RS702 are packaged in a high performance 52-pin plastic quad flat pack. The 52-pin PQFP features an integral heat spreader and excellent electrical characteristics in a molded plastic package design.

Data Eye Diagram From Serial Output (DO/DON) of RS701 in PQFP Package



Amplitude: 200 mV/div
Time Scale: 50 ps/div
Data Rate: 2.5 Gbits/sec

Data Eye Measurement Setup



Ordering Information

Rockwell's RS701/RS702 are available with different operating temperature ranges. The order number is formed by using a combination of the device type, package type, and temperature of operation.

RS701-P-I

DEVICE TYPE:
RS701 = 3 Gbits/sec 16-bit Multiplexer
RS702 = 3 Gbits/sec 16-bit Demultiplexer

OPERATING TEMPERATURE RANGE:
C = Commercial (0 to 70 °C)
I = Industrial (-40 to +85 °C)

PACKAGE TYPE:
P = 52-pin Plastic Quad Flatpack

Rockwell Gallium Arsenide Standard Products and ASICs

RS701/RS702 ..... 2.5 Gbits/Sec, 16-bit Mux/Demux Chipset
RI61008 ..... 1.2 GSPS, 10-bit Digital-to-Analog Converter (DAC)
LI300 ..... Lightning Series, 300 Gate, 5 GHz Gate Array
LI1000 ..... Lightning Series, 1000 Gate, 5 GHz Gate Array
CC30K ..... Cyclone Series, 30,000 Raw Gates, 1 GHz Gate Array
CC60K ..... Cyclone Series, 60,000 Raw Gates, 1 GHz Gate Array
CC100K ..... Cyclone Series, 100,000 Raw Gates, 1 GHz Gate Array

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