ATW2800S Series

## Single Output, Hybrid - High Reliability DC/DC Converter

## DESCRIPTION

The ATW2800S Series of DC/DC converters feature high power density and an extended temperature range for use in military and industrial applications. Designed to MIL-STD-704 input requirements, these devices have nominal 28 V DC inputs with $+5,+12 \mathrm{~V}$ and +15 V single outputs. The circuit design incorporates a pulse width modulated push-pull topology operating in the feed-forward mode at a nominal switching frequency of 270 KHz . Input to output isolation is achieved through the use of transformers in the forward and feedback circuits.

The advanced feedback design provides fast loop response for superior line and load transient characteristics and offers greater reliability and radiation tolerance than devices incorporating optical feedback circuits.

Three standard temperature grades are offered. Refer to Part Number section. They are provided in a flanged package for more severe enviroments.

Manufactured in a facility fully qualified to MIL-PRF38534, these converters are available in four screening grades to satisfy a wide range of requirements. The CH grade is fully compliant to the requirements of MIL-PRF-38534 for class H . The HB grade is processed and screened to the class H requirement, but may not necessarily meet all of the other MIL-PRF-38534 requirements, e.g., element evaluation and Periodic Inspection (P.I.) not required. Both grades are tested to meet the complete group " A " test specification over the full military temperature range without output power deration. Two grades with more limited screening are also available for use in less demanding applications. Variations in electrical, mechanical and screening can be accommodated. Contact Lambda Advanced Analog for special requirements.

## FEATURES

- 19 To 40 Volt Input Range ( $28 \mathrm{~V}_{\text {DC }}$ Nominal)
- 30 Watts Output Power
- Indefinite Short Circuit and Overload Protection
- 22.8 W/in ${ }^{3}$ Power Density
- Fast Loop Response For Superior Transient Characteristics
- Operating Temperature Range From $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ Available
- Popular Industry Standard Pin-Out

■ Resistance Seam Welded Case For Superior Long Term Hermeticity

- Efficiencies Up to 83\%
- Shutdown From External Signal

■ Military Screening

- 250,000 Hour MTBF at $85^{\circ} \mathrm{C}$

■ MIL-PRF-38534 Compliant Versions Available

ABSOLUTE MAXIMUM RATINGS

Input Voltage
Soldering Temperature
Case Temperature
-0.5 V to 50 V
$300^{\circ} \mathrm{C}$ for 10 seconds
Operating- $55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$
Storage $-65^{\circ} \mathrm{C}$ to $+135^{\circ} \mathrm{C}$

TABLE I. Electrical Performance Characteristics

| Test | Symbol | Conditions$\begin{gathered} -55^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{C}} \leq+125^{\circ} \mathrm{C} \\ \mathrm{~V}_{\text {IN }}=28 \mathrm{~V} \mathrm{dc} \pm 5 \%, \mathrm{C}_{\mathrm{L}}=0 \text { unless } \\ \text { otherwise specified } \end{gathered}$ | Group A subgroups | Device types | Limits |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  | Min | Max |  |
| Output voltage | $\mathrm{V}_{\text {OUT }}$ | $\mathrm{I}_{\text {OUT }}=0$ | 1 | All | 4.95 | 5.05 | V |
|  |  |  | 2,3 |  | 4.90 | 5.10 |  |
| Output current 1 / | $\mathrm{I}_{\text {OUT }}$ | $\mathrm{V}_{\text {IN }}=19,28$, and 40 V dc | 1,2,3 | All | 0.0 | 6000 | mA |
| Output ripple voltage $2 /$ | $\mathrm{V}_{\text {RIP }}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=19,28 \text {, and } 40 \mathrm{~V} \mathrm{dc} \\ & \text { B.W. }=\text { dc to } 2 \mathrm{MHz} \end{aligned}$ | 1,2,3 | All |  | 50 | mV p-p |
| Output power $\underline{1 / 3}$ | $\mathrm{P}_{\text {OUT }}$ | $\mathrm{V}_{\text {IN }}=19,28$, and 40 V dc | 1,2,3 | All | 30 |  | W |
| Line regulation 4/ | $\mathrm{VR}_{\text {LINE }}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=19,28, \text { and } 40 \mathrm{~V} \mathrm{dc} \\ & \mathrm{I}_{\text {OUT }}=0,3000, \text { and } 6000 \mathrm{~mA} \end{aligned}$ | 1 | All |  | 5 | mV |
|  |  |  | 2,3 |  |  | 20 |  |
| Load regulation 4/ | $\mathrm{VR}_{\text {LOAD }}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=19,28 \text {, and } 40 \mathrm{~V} \mathrm{dc} \\ & \mathrm{I}_{\mathrm{OUT}}=0,3000 \text {, and } 6000 \mathrm{~mA} \end{aligned}$ | 1,2,3 | All |  | 30 | mV |
| Input current | $\mathrm{I}_{\text {IN }}$ | $\mathrm{I}_{\text {OUT }}=0$, inhibit $(\operatorname{pin} 2)$ tied to input return (pin 10) | 1,2,3 | All |  | 18 | mA |
|  |  | $\mathrm{I}_{\text {Out }}=0$, inhibit $(\operatorname{pin} 2)=$ open |  |  |  | 40 |  |
| Input ripple current 2/ | $\mathrm{I}_{\text {RIP }}$ | $\begin{aligned} & \mathrm{I}_{\text {Out }}=6000 \mathrm{~mA} \\ & \text { B.W. }=\text { dc to } 2 \mathrm{MHz} \end{aligned}$ | 1,2,3 | All |  | 20 | mA p-p |
| Efficiency | $\mathrm{E}_{\mathrm{FF}}$ | $\begin{aligned} & \mathrm{I}_{\text {OUT }}=6000 \mathrm{~mA}, \\ & \mathrm{~T}_{\mathrm{C}}=+25^{\circ} \mathrm{C} \end{aligned}$ | 1 | All | 78 |  | \% |
| Isolation | ISO | Input to output or any pin to case (except pin 7) at $500 \mathrm{~V} \mathrm{dc}, \mathrm{T}_{\mathrm{C}}$ $=+25^{\circ} \mathrm{C}$ | 1 | All | 100 |  | $\mathrm{M} \Omega$ |
| Capacitive load 5/ 6/ | $\mathrm{C}_{\mathrm{L}}$ | No effect on dc performance, $\mathrm{T}_{\mathrm{C}}=+25^{\circ} \mathrm{C}$ | 4 | All |  | 500 | $\mu \mathrm{F}$ |
| Power dissipation load fault | $\mathrm{P}_{\mathrm{D}}$ | Overload, $\mathrm{T}_{\mathrm{C}}=+25^{\circ} \mathrm{C} \quad$ 7/ | 1 | All |  | 12 | W |
|  |  | Short circuit, $\mathrm{T}_{\mathrm{C}}=+25^{\circ} \mathrm{C}$ |  |  |  | 9 |  |

See footnotes at end of table.

TABLE I. Electrical Performance Characteristics - Continued.

| Test | Symbol | Conditions$\begin{gathered} -55^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{C}} \leq+125^{\circ} \mathrm{C} \\ \mathrm{~V}_{\text {IN }}=28 \mathrm{~V} \mathrm{dc} \pm 5 \%, \mathrm{C}_{\mathrm{L}}=0 \text { unless } \\ \text { otherwise specified } \end{gathered}$ | Group A <br> Subgroups | Device Type | Limits |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  | Min | Max |  |
| Switching frequency | $\mathrm{F}_{\mathrm{S}}$ | $\mathrm{I}_{\text {OUT }}=6000 \mathrm{~mA}$ | 4,5,6 | 01 | 250 | 300 | kHz |
|  |  |  |  | 02 | 250 | 270 |  |
|  |  |  |  | 03 | 275 | 300 |  |
| Output response to step transient load changes 8/ | $\mathrm{VO}_{\text {TLOAD }}$ | 4000 mA to/from 6000 mA | 4,5,6 | All | -500 | +500 | mV pk |
|  |  | 500 mA to/from 2500 mA | 4,5,6 | All | -500 | +500 |  |
| Recovery time step transient load changes $\underline{8 / 9 /}$ | $\mathrm{TT}_{\text {LOAD }}$ | 4000 mA to/from 6000 mA | 4 | All |  | 100 | $\mu \mathrm{s}$ |
|  |  |  | 5,6 |  |  | 200 |  |
|  |  | 500 mA to/from 2500 mA | 4 | All |  | 100 |  |
|  |  |  | 5,6 |  |  | 200 |  |
| Turn on overshoot | VTonos | $\mathrm{I}_{\text {Out }}=0$ and 6000 mA | 4,5,6 | All |  | 500 | mV pk |
| Turn on delay $\underline{10}$ | $\mathrm{Ton}_{\mathrm{D}}$ | $\mathrm{I}_{\text {Out }}=0$ and 6000 mA | 4,5,6 | All |  | 12 | ms |
| Load fault recovery 6/ 10/ | $\mathrm{Tr}_{\text {LF }}$ |  | 4,5,6 | All |  | 12 | ms |

## Notes:

1/ Parameter guaranteed by line and load regulation tests.
2/ Bandwidth guaranteed by design. Tested for 20 KHz to 2 MHz .
3/ Above $+125^{\circ} \mathrm{C}$ case, derate output power linearly to 0 at $+135^{\circ} \mathrm{C}$.
4/ Output voltage measured at load with remote sense leads connected across load.
5/ Capacitive load may be any value from 0 to the maximum limit without compromising dc performance. A capacitive load in excess of the maximum limit will not disturb loop stability but may interfere with the operation of the load fault detection circuitry, appearing as a short circuit during turn on.
6/ Parameter shall be tested as part of design characterization and after design or process changes. Thereafter parameters shall be guaranteed to the limits specified in Table I.
7/ An overload is that condition with a load in excess of the rated load but less than that necessary to trigger the short circuit protection and is the condition of maximum power dissipation.
8/ Load step transition time between 2 and 10 microseconds.
$\underline{9} /$ Recovery time is measured from the initiation of the transient to where $\mathrm{V}_{\text {Out }}$ has returned to within $\pm 1$ percent of $\mathrm{V}_{\text {Out }}$ at 50 percent load.
10/Turn on delay time measurement is for either a step application of power at the input or the removal of a ground signal from the inhibit pin (pin 2) while power is applied to the input.

## ABSOLUTE MAXIMUM RATINGS

Input Voltage
Soldering Temperature
Case Temperature
-0.5 V to 50 V
$300^{\circ} \mathrm{C}$ for 10 seconds
Operating- $55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$
Storage $-65^{\circ} \mathrm{C}$ to $+135^{\circ} \mathrm{C}$

TABLE II. Electrical Performance Characteristics

| Test | Symbol | Conditions$\begin{gathered} -55^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{C}} \leq+125^{\circ} \mathrm{C} \\ \mathrm{~V}_{\text {IN }}=28 \mathrm{~V} \mathrm{dc} \pm 5 \%, \mathrm{C}_{\mathrm{L}}=0 \text { unless } \\ \text { otherwise specified } \end{gathered}$ | Group A subgroups | Device types | Limits |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  | Min | Max |  |
| Output voltage | $\mathrm{V}_{\text {Out }}$ | $\mathrm{I}_{\text {OUT }}=0$ | 1 | All | 4.95 | 5.05 | V |
|  |  |  | 2,3 |  | 4.90 | 5.10 |  |
| Output current 1 / | $\mathrm{I}_{\text {Out }}$ | $\mathrm{V}_{\text {IN }}=19,28$, and 40 V dc | 1,2,3 | All | 0.0 | 6000 | mA |
| Output ripple voltage 2/ | $\mathrm{V}_{\text {RIP }}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=19,28, \text { and } 40 \mathrm{~V} \mathrm{dc} \\ & \text { B.W. }=\text { dc to } 2 \mathrm{MHz} \end{aligned}$ | 1,2,3 | All |  | 50 | mV p-p |
| Output power 1/ $\underline{3} /$ | Pout | $\mathrm{V}_{\text {IN }}=19,28$, and 40 V dc | 1,2,3 | All | 30 |  | W |
| Line regulation 4/ | $\mathrm{VR}_{\text {LINE }}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=19,28, \text { and } 40 \mathrm{~V} \mathrm{dc} \\ & \mathrm{I}_{\mathrm{OUT}}=0,3000 \text {, and } 6000 \mathrm{~mA} \end{aligned}$ | 1 | All |  | 5 | mV |
|  |  |  | 2,3 |  |  | 20 |  |
| Load regulation 4/ | $\mathrm{VR}_{\text {LOAD }}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=19,28, \text { and } 40 \mathrm{~V} \mathrm{dc} \\ & \mathrm{I}_{\mathrm{OUT}}=0,3000 \text {, and } 6000 \mathrm{~mA} \end{aligned}$ | 1,2,3 | All |  | 30 | mV |
| Input current | $\mathrm{I}_{\text {IN }}$ | $\mathrm{I}_{\text {out }}=0$, inhibit $($ pin 2$)$ tied to input return (pin 10) | 1,2,3 | All |  | 18 | mA |
|  |  | $\mathrm{I}_{\text {OUT }}=0$, inhibit $(\operatorname{pin} 2)=$ open |  |  |  | 40 |  |
| Input ripple current $\underline{2 /}$ | $\mathrm{I}_{\text {RIP }}$ | $\begin{aligned} & \mathrm{I}_{\text {out }}=6000 \mathrm{~mA} \\ & \text { B.W. }=\text { dc to } 2 \mathrm{MHz} \end{aligned}$ | 1,2,3 | All |  | 20 | mA p-p |
| Efficiency | $\mathrm{E}_{\mathrm{FF}}$ | $\mathrm{I}_{\text {OuT }}=6000 \mathrm{~mA}, \mathrm{~T}_{\mathrm{C}}=+25^{\circ} \mathrm{C}$ | 1 | All | 78 |  | \% |
| Isolation | ISO | Input to output or any pin to case (except pin 7) at $500 \mathrm{~V} \mathrm{dc}, \mathrm{T}_{\mathrm{C}}$ $=+25^{\circ} \mathrm{C}$ | 1 | All | 100 |  | $\mathrm{M} \Omega$ |
| Capacitive load 5/ 6/ | $\mathrm{C}_{\mathrm{L}}$ | No effect on dc performance, $\mathrm{T}_{\mathrm{C}}=+25^{\circ} \mathrm{C}$ | 4 | All |  | 500 | $\mu \mathrm{F}$ |
| Power dissipation load fault | $\mathrm{P}_{\mathrm{D}}$ | Overload, $\mathrm{T}_{\mathrm{C}}=+25^{\circ} \mathrm{C} \quad$ 7/ | 1 | All |  | 12 | W |
|  |  | Short circuit, $\mathrm{T}_{\mathrm{C}}=+25^{\circ} \mathrm{C}$ |  |  |  | 9 |  |

See footnotes at end of table.

TABLE II. Electrical Performance Characteristics - Continued.

| Test | Symbol | Conditions$\begin{gathered} -55^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{C}} \leq+125^{\circ} \mathrm{C} \\ \mathrm{~V}_{\text {IN }}=28 \mathrm{~V} \mathrm{dc} \pm 5 \%, \mathrm{C}_{\mathrm{L}}=0 \text { unless } \\ \text { otherwise specified } \end{gathered}$ | Group A Subgroups | Device Type | Limits |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  | Min | Max |  |
| Switching frequency | $\mathrm{F}_{\text {S }}$ | $\mathrm{I}_{\text {OUT }}=6000 \mathrm{~mA}$ | 4,5,6 | 01 | 250 | 300 | kHz |
|  |  |  |  | 02 | 250 | 270 |  |
|  |  |  |  | 03 | 275 | 300 |  |
| Output response to step transient load changes $\underline{8 /}$ | $\mathrm{VO}_{\text {TLOAD }}$ | 4000 mA to/from 6000 mA | 4,5,6 | All | -500 | +500 | mV pk |
|  |  | 500 mA to/from 2500 mA | 4,5,6 | All | -500 | +500 |  |
| Recovery time step transient load changes $\underline{8 /}$ /9/ | TT ${ }_{\text {LOAD }}$ | 4000 mA to/from 6000 mA | 4 | All |  | 100 | $\mu \mathrm{s}$ |
|  |  |  | 5,6 |  |  | 200 |  |
|  |  | 500 mA to/from 2500 mA | 4 | All |  | 100 |  |
|  |  |  | 5,6 |  |  | 200 |  |
| Turn on overshoot | VTonos | $\mathrm{I}_{\text {OuT }}=0$ and 6000 mA | 4,5,6 | All |  | 500 | mV pk |
| Turn on delay $\underline{10}$ | $\mathrm{Ton}_{\mathrm{D}}$ | $\mathrm{I}_{\text {Out }}=0$ and 6000 mA | 4,5,6 | All |  | 12 | ms |
| Load fault recovery 6/ 10/ | $\mathrm{Tr}_{\text {LF }}$ |  | 4,5,6 | All |  | 12 | ms |
| Weight |  | Flange |  |  |  | 75 | grams |

## Notes:

1/ Parameter guaranteed by line and load regulation tests.
2/ Bandwidth guaranteed by design. Tested for 20 KHz to 2 MHz .
3/ Above $+125^{\circ} \mathrm{C}$ case, derate output power linearly to 0 at $+135^{\circ} \mathrm{C}$.
4/ Output voltage measured at load with remote sense leads connected across load.
$\underline{5} /$ Capacitive load may be any value from 0 to the maximum limit without compromising dc performance. A capacitive load in excess of the maximum limit will not disturb loop stability but may interfere with the operation of the load fault detection circuitry, appearing as a short circuit during turn on.
6/ Parameter shall be tested as part of design characterization and after design or process changes. Thereafter parameters shall be guaranteed to the limits specified in Table II.
7/ An overload is that condition with a load in excess of the rated load but less than that necessary to trigger the short circuit protection and is the condition of maximum power dissipation.
8/ Load step transition time between 2 and 10 microseconds.
$\underline{9 /}$ Recovery time is measured from the initiation of the transient to where $\mathrm{V}_{\text {out }}$ has returned to within $\pm 1$ percent of $\mathrm{V}_{\text {out }}$ at 50 percent load.
10/ Turn on delay time measurement is for either a step application of power at the input or the removal of a ground signal from the inhibit pin (pin 2 ) while power is applied to the input.

## ABSOLUTE MAXIMUM RATINGS

Input Voltage
Soldering Temperature
Case Temperature
-0.5 V to 50 V
$300^{\circ} \mathrm{C}$ for 10 seconds
Operating- $55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$
Storage $-65^{\circ} \mathrm{C}$ to $+135^{\circ} \mathrm{C}$

TABLE III. Electrical Performance Characteristics

| Test | Symbol | Conditions$\begin{gathered} -55^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{C}} \leq+125^{\circ} \mathrm{C} \\ \mathrm{~V}_{\text {IN }}=28 \mathrm{~V} \mathrm{dc} \pm 5 \%, \mathrm{C}_{\mathrm{L}}=0 \text { unless } \\ \text { otherwise specified } \end{gathered}$ | Group A subgroups | Device types | Limits |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  | Min | Max |  |
| Output voltage | $\mathrm{V}_{\text {Out }}$ | $\mathrm{I}_{\text {OUT }}=0$ | 1 | All | 14.85 | 15.15 | V |
|  |  |  | 2,3 |  | 14.70 | 15.30 |  |
| Output current $\underline{1 /}$ | $\mathrm{I}_{\text {OUT }}$ | $\mathrm{V}_{\text {IN }}=17,28$, and 40 V dc | 1,2,3 | All | 0.0 | 1333 | mA |
| Output ripple voltage 2/ | $\mathrm{V}_{\text {RIP }}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=17,28, \text { and } 40 \mathrm{~V} \text { dc } \\ & \text { B.W. }=\text { dc to } 2 \mathrm{MHz} \end{aligned}$ | 1,2,3 | All |  | 60 | mV p-p |
| Output power $\underline{1 /} \underline{3}$ | Pout | $\mathrm{V}_{\text {IN }}=17,28$, and 40 V dc | 1,2,3 | All | 20 |  | W |
| Line regulation | $\mathrm{VR}_{\text {LINE }}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=17,28, \text { and } 40 \mathrm{~V} \mathrm{dc} \\ & \mathrm{I}_{\mathrm{OUT}}=0, .677, \text { and } 1333 \mathrm{~mA} \end{aligned}$ | 1 | All |  | 35 | mV |
|  |  |  | 2,3 |  |  | 75 |  |
| Load regulation | $\mathrm{VR}_{\text {LOAD }}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=17,28, \text { and } 40 \mathrm{~V} \mathrm{dc} \\ & \mathrm{I}_{\mathrm{OUT}}=0, .677, \text { and } 1333 \mathrm{~mA} \end{aligned}$ | 1,2,3 | All |  | 150 | mV |
| Input current | $\mathrm{I}_{\text {IN }}$ | $\mathrm{I}_{\text {OUT }}=0$, inhibit $(\operatorname{pin} 2)$ tied to input return (pin 10) | 1,2,3 | All |  | 18 | mA |
|  |  | $\begin{aligned} & \text { Iout }=0, \\ & \text { inhibit }(\operatorname{pin} 2)=\text { open } \end{aligned}$ |  |  |  | 35 |  |
| Input ripple current $\underline{2 /}$ | $\mathrm{I}_{\text {RIP }}$ | $\begin{aligned} & \mathrm{I}_{\text {out }}=1333 \mathrm{~mA} \\ & \text { B.W. }=\text { dc to } 2 \mathrm{MHz} \end{aligned}$ | 1,2,3 | All |  | 50 | mA p-p |
| Efficiency | $\mathrm{E}_{\text {FF }}$ | $\mathrm{I}_{\text {Out }}=1333 \mathrm{~mA}, \mathrm{~T}_{\mathrm{C}}=+25^{\circ} \mathrm{C}$ | 1 | All | 80 |  | \% |
| Isolation | ISO | Input to output or any pin to case (except pin 8) at $500 \mathrm{~V} \mathrm{dc}, \mathrm{T}_{\mathrm{C}}=$ $+25^{\circ} \mathrm{C}$ | 1 | All | 100 |  | $\mathrm{M} \Omega$ |
| Capacitive load 4/ 5/ | $\mathrm{C}_{\mathrm{L}}$ | No effect on dc performance, $\mathrm{T}_{\mathrm{C}}=$ $+25^{\circ} \mathrm{C}$ | 4 | All |  | 200 | $\mu \mathrm{F}$ |
| Power dissipation load fault | $\mathrm{P}_{\mathrm{D}}$ | Overload, $\mathrm{T}_{\mathrm{C}}=+25^{\circ} \mathrm{C} \quad \underline{6 /}$ | 1 | All |  | 6 | W |
|  |  | Short circuit, $\mathrm{T}_{\mathrm{C}}=+25^{\circ} \mathrm{C}$ |  |  |  | 6 |  |

See footnotes at end of table.

TABLE III. Electrical Performance Characteristics - Continued.

| Test | Symbol | Conditions$\begin{gathered} -55^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{C}} \leq+125^{\circ} \mathrm{C} \\ \mathrm{~V}_{\text {IN }}=28 \mathrm{~V} \mathrm{dc} \pm 5 \%, \mathrm{C}_{\mathrm{L}}=0 \text { unless } \\ \text { otherwise specified } \end{gathered}$ | Group A subgroups | Device types | Limits |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  | Min | Max |  |
| Switching frequency | $\mathrm{F}_{\text {S }}$ | $\mathrm{I}_{\text {OUT }}=1333 \mathrm{~mA}$ | 4,5,6 | 01 | 225 | 275 | kHz |
|  |  |  |  | 02 | 225 | 245 |  |
|  |  |  |  | 03 | 250 | 275 |  |
| Output response to step transient load changes 7/ | $\mathrm{VO}_{\text {tLoad }}$ | 50 percent load to/from 100 percent load | 4 | All | -300 | +300 | mV pk |
|  |  |  | 5,6 |  | -450 | +450 |  |
|  |  | No load to/from 50 percent load | 4 | All | -500 | +500 |  |
|  |  |  | 5,6 |  | -750 | +750 |  |
| Recovery time step transient load changes $\underline{7 /} \underline{8 /}$ | $\mathrm{TT}_{\text {LOAD }}$ | 50 percent load to/from 100 percent load | 4 | All |  | 70 | $\mu \mathrm{s}$ |
|  |  |  | 5,6 |  |  | 100 |  |
|  |  | No load to 50 percent load | 4,5,6 | All |  | 1500 |  |
|  |  | 50 percent load to no load | 4,5,6 | All |  | 5 | ms |
| Output response to transient step line changes $\underline{5} / \underline{9} /$ | $\mathrm{VO}_{\text {TLine }}$ | Input step 17 to 40 V dc | 4,5,6 | All |  | 500 | mV pk |
|  |  | Input step 40 to 17 V dc | 4,5,6 | All |  | -1500 |  |
| Recovery time transient line changes $\underline{5} / \underline{8} / \underline{9} /$ | TT ${ }_{\text {LINE }}$ | Input step 17 to 40 V dc | 4,5,6 | All |  | 800 | ms |
|  |  | Input step 40 to 17 V dc | 4,5,6 | All |  | 800 |  |
| Turn on overshoot | $\mathrm{VTon}_{\text {OS }}$ | $\mathrm{I}_{\text {Out }}=0$ and 1333 mA | 4,5,6 | All |  | 600 | mV pk |
| Turn on delay $\underline{10 /}$ | $\mathrm{Ton}_{\text {D }}$ | $\mathrm{I}_{\text {Out }}=0$ and 1333 mA | 4,5,6 | All |  | 10 | ms |
| Load fault recovery 5/ | $\mathrm{Tr}_{\text {LF }}$ |  | 4,5,6 | All |  | 10 | ms |
| Weight |  | Flange |  |  |  | 75 | grams |

## Notes:

1/ Parameter guaranteed by line and load regulation tests.
2/ Bandwidth guaranteed by design. Tested for 20 KHz to 2 MHz .
3/ For operation at 16 V dc input, derate output power by 33 percent.
$\underline{4} /$ Capacitive load may be any value from 0 to the maximum limit without compromising dc performance. A capacitive load in excess of the maximum limit will not disturb loop stability but may interfere with the operation of the load fault detection circuitry, appearing as a short circuit during turn on.
5/ Parameter shall be tested as part of design characterization and after design or process changes. Thereafter parameters shall be guaranteed to the limits specified in Table III.
6/ An overload is that condition with a load in excess of the rated load but less than that necessary to trigger the short circuit protection and is the condition of maximum power dissipation.
7/ Load step transition time between 2 and 10 microseconds.
8/ Recovery time is measured from the initiation of the transient to where $\mathrm{V}_{\text {out }}$ has returned to within $\pm 1$ percent of $\mathrm{V}_{\text {out }}$ at 50 percent load.
$\underline{9}$ / Input step transition time between 2 and 10 microseconds.
10/ Turn on delay time measurement is for either a step application of power at the input or the removal of a ground signal from the inhibit pin (pin 2) while power is applied to the input.

## BLOCK DIAGRAM



Available Screening Levels and Process Variations for ATW 2800 S Series

| Requirement | MIL-STD-883 method | No Suffix | ES Suffix | HB Suffix | CH Suffix |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Temperature Range |  | $-55^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | $-55^{\circ} \mathrm{C}$ to $+115^{\circ} \mathrm{C}$ | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| Element Evaluation |  |  |  |  | MIL-PRF-38534 |
| Internal Visual | 2017 | - | $\checkmark$ | $\checkmark$ | $\checkmark$ |
| Temperature Cycle | 1010, Cond C |  | Cond A | $\checkmark$ | $\checkmark$ |
| Constant Acceleration | 2001, Cond A |  | 500 g | 5,000g | 5,000g |
| Burn-in | 1015 |  | 96hrs @ $105^{\circ} \mathrm{C}$ | 160hrs @ $125^{\circ} \mathrm{C}$ | 160hrs @ $125^{\circ} \mathrm{C}$ |
| Final Electrical (Group A) | Specification | $25^{\circ} \mathrm{C}$ | $25^{\circ} \mathrm{C}$ | $-55,+25,+125^{\circ} \mathrm{C}$ | $-55,+25,+125^{\circ} \mathrm{C}$ |
| Seal, Fine \& Gross | 1014 |  | $\checkmark$ | $\checkmark$ | $\checkmark$ |
| External Visual | 2009 | - | $\checkmark$ | $\checkmark$ | $\checkmark$ |

- per Commercial Standards


## PART NUMBER

Model $\square$ ATW 28xx S / x-xxx

Input Voltage $\qquad$

Output Voltage $\qquad$
Single Output $\qquad$
Synchronization Option
Omit for standard
MSTR - Master
SLV - Slave
Temperature Range
Omit for $-55^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ (Industrial)
ES $-55^{\circ} \mathrm{C}$ to $+105^{\circ} \mathrm{C}$ (Environmental)
$\mathrm{HB}-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ (Military Screening)
$\mathrm{CH}-55^{1} / 2 \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ (DESC Compliant)

$2 \mu \mathrm{~s} / \mathrm{div}$
Figure 1 Output Ripple Voltage VIN $=28 \mathrm{VDC}$, Full Load

$2 \mathrm{~ms} /$ div
Figure 3 Turn-on Response @Full Load

$100 \mu \mathrm{~s} /$ div
Figure 5 Load Step Response Load Step 0 to 6.0 Adc (No Load to Full Load)

$2 \mu \mathrm{~s} / \mathrm{div}$
Figure 2 Input Ripple Voltage
VIN $=28 \mathrm{Vdc}$, Full Load

$100 \mu \mathrm{~s} / \mathrm{div}$
Figure 4 Turn-on Response, @Full Load

$2 \mathrm{~ms} / \mathrm{div}$
Figure 6 Load Step Response Load Step 3.0 to 0 Adc (Full Load to No Load)


Figure 7 Load Step Response
Load Step 3.0 Adc to 6.0 Adc
(Half Load to Full Load)

$100 \mu \mathrm{~s} / \mathrm{div}$
Figure 9 Line Step Response
A: Output @ 100 mV V/div, Full Load
B: Input step @ 19 Vdc to 40 Vdc



Figure 8 Load Step Response
Load Step 6.0 Adc to 3.0 Adc
(Full Load to Half Load)

$100 \mu \mathrm{~s} / \mathrm{div}$
Figure 10 Line Step Response
A: Output @ $100 \mathrm{mV} / \mathrm{div}$, Full Load
B: Input Step 40 Vdc to 19 Vdc

Flgure 11 Audio Rejection


Figure 12 Audio Rejection with AFC461 EMI Filter

## MECHANICAL OUTLINE



## PIN DESIGNATION

Pin 1 Positive input
Pin 2 Inhibit input
Pin 3 Neg. remote sense*
Pin 4 Output common
Pin 5 Positive output

Pin 10 Input common
Pin 9 N/C
Pin 8 N/C**
Pin 7 Case ground
Pin 6 Pos. remote sense*
*ATW2805S only. ATW2812S, ATW2815S have N/C.
**Or synchronization option.

## APPLICATION INFORMATION

## Inhibit Function

Connecting the inhibit input (Pin 2) to input common (Pin 10) will cause the converter to shut down. It is recommended that the inhibit pin be driven by an open collector device capable of sinking at least $400 \mu \mathrm{~A}$ of current. The open circuit voltage of the inhibit input is $11.5 \pm 1 \mathrm{VDC}$.

## EMI Filter

An optional EMI filter (AFC461) will reduce the input ripple current to levels below the limits imposed by MIL-STD-461 CEO3.

## Remote Sense (ATW2805S only)

Better than $0.1 \%$ line and load regulation (case temperature constant) are typical when the remote sense leads are used. If the remote sense leads are left unconnected, then the output voltage (measured at pins 4 and 5 ) will rise approximately 5.4 VDC .
If the remote sense leads are shorted together, the output voltage may rise above 10 VdC depending on load, posibly damaging both the converter and load.

## Device Synchronization

Whenever multiple DC/DC converters are utilized in a single system, significant low frequency noise may be generated due to slight differences in the switching frequencies of the converters (beat frequency noise). Because of the low frequency nature of this noise (typically less than 10 KHz ), it is difficult to filter out and may interfere with proper operation of sensitive systems (communications, radar or telemetry). Lambda Advanced Analog offers an option which provides synchronization of multiple AHE/ATW type converters, thus eliminating this type of noise.

## STANDARDIZED MILITARY DRAWING

 CROSS REFERENCE| Standardized <br> military drawing <br> PIN | Vendor <br> CAGE <br> number | Vendor <br> similar <br> PIN |
| :--- | :---: | :--- |
| $5962-9157904 \mathrm{HZX}$ | 52467 | ATW2805S/CH |
| $5962-9157905 \mathrm{HZX}$ | 52467 | ATW2805S/CH-SLV |
| $5962-9157906 \mathrm{HZX}$ | 52467 | ATW2805S/CH-MSTR |
| $5962-921101 \mathrm{HZX}$ | 52467 | ATW2812S/CH |
| $5962-921102 \mathrm{HZX}$ | 52467 | ATW2812S/CH-SLV |
| $5962-921103 \mathrm{HZX}$ | 52467 | ATW2812S/CH-MSTR |
| $5962-9159904 \mathrm{HZX}$ | 52467 | ATW2815S/CH |
| $5962-9159905 \mathrm{HZX}$ | 52467 | ATW2815S/CH-SLV |
| $5962-9159906 \mathrm{HZX}$ | 52467 | ATW2815S/CH-MSTR |

To take advantage of this capability, the system designer must assign one of the converters as the master. Then, by definition, the remaining converters become slaves and will operate at the masters' switching frequency. The user should be aware that the synchronization system is failsafe; that is, the slaves will continue operating should the master frequency be interrupted for any reason. The layout must be such that the synchronization output (pin 8) of the master device is connected to the synchronization input (pin 8) of each slave device. It is advisable to keep this run short to minimize the possibility of radiating the 250 KHz switching frequency.
The appropriate parts must be ordered to utilize this feature. After selecting the converters required for the system, a 'MSTR' suffix is added for the master converter part number and a 'SLV' suffix is added for slave part number. See Part Number section.


Typical Synchronization Connection Diagram

ATW2805S EFFICIENCY


## NOTES

