

Multi-Phase DC/DC Controller for CPU Core Power Supply

General Description

The RT9237A is a multi-phase buck DC/DC controller integrated with all control functions for high performance processor VRM. The RT9237A drives 2, 3 or 4 buck switching stages operating in interleaved phase set automatically. The multi-phase architecture provides high output current while maintaining low power dissipation on power devices and low stress on input and output capacitors. The high equivalent operating frequency also reduces the component dimension and the output voltage ripple in load transient.

RT9237A regulates both easily set voltage and current loops. Precise current sharing for power stage is achieved by differential input current sense and processing circuit. The settings of current sense, droop tuning and over current protection are independent to compensation circuit of voltage loop. The feature greatly facilitates the flexibility of CPU power supply design and tuning.

The RT9237A uses a 5-bit DAC of 1.1V to 1.85V (25mV/step) output with load current droop compensation to meet the strict VRM transient requirement. The IC monitors the V_{CORE} voltage for PGOOD and over voltage protection. Soft start, over current protection and programmable under voltage lockout are also provided to assure the safety of microprocessor and power system.

Applications

- Power Supply for Server and Workstation
- Power Supply for High Current Microprocessor

Ordering Information

RT9237A□□

Package Type
S : SOP-28

Operating Temperature Range
C: Commercial Standard

Features

- Multi-Phase Power Conversion with Automatic Phase Selection
- VRM 9.0 DAC Output with Active Droop Compensation for Fast Load Transient
- Precise Channel Current Sharing with Differential Sense Input
- Hiccup Mode Over Current Protection
- Programmable Under Voltage Lockout and Soft Start
- High Ripple Frequency, (Channel Frequency 100kHz) Times Channel Number

Pin Configurations

Part Number	Pin Configurations
RT9237ACS (Plastic SOP-28)	<p>TOP VIEW</p> <p> VID4 [1] [28] VDD VID3 [2] [27] PGOOD VID2 [3] [26] PWM4 VID1 [4] [25] ISP4 VID0 [5] [24] ISP1 COMP [6] [23] PWM1 FB [7] [22] PWM2 ADJ [8] [21] ISP2 GND [9] [20] ISP3 VSEN [10] [19] PWM3 IRMP [11] [18] ISN1 DVD [12] [17] ISN2 IMAX [13] [16] ISN3 SS [14] [15] ISN4 </p>

Absolute Maximum Ratings

- Supply Voltage 7V
- Input, Output or I/O Voltage GND-0.3V ~ VDD+0.3V
- Ambient Temperature Range 0°C ~ 70°C
- Operating Junction Temperature Range 0°C ~ 125°C
- Storage Temperature Range -65°C ~ 150°C
- Power Dissipation, P_D @ $T_A = 25^\circ\text{C}$
 SOP-28 0.625W
- Package Thermal Resistance
 SOP-28, θ_{JA} 60°C /W
- Lead Temperature (Soldering, 10 sec.) 260°C

Electrical Characteristics

($V_{DD} = 5V$, $GND = 0V$, $T_A = 25^\circ\text{C}$, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
V_{DD} Supply Current						
Nominal Supply Current	I_{DD}	PWM 1,2,3,4 Open	--	5	12	mA
Power-On Reset						
V _{DD} Rising Threshold			4.2	4.35	4.6	V
V _{DD} Falling Threshold			--	3.85	--	V
Hysteresis			0.2	0.6	--	V
V _{DVD} Rising Trip Threshold			1.19	1.25	1.31	V
Oscillator						
Frequency		For each phase	85	100	115	kHz
Ramp Amplitude	ΔV_{OSC}	$R_{IRMP} = 112k\Omega$	--	1	--	V
Ramp Valley			1.0	1.3	--	V
Maximum On Time of Each Channel			70	75	80	%
IRMP Pin Voltage		$R_{IRMP} = 50k\Omega$	0.95	1	1.05	V
Reference and DAC						
DACOUT Voltage Accuracy			-1.0	--	+1.0	%
DAC (VID0-VID4) Input Low Voltage			--	--	0.8	V
DAC (VID0-VID4) Input High Voltage			2.0	--	--	V
DAC (VID0-VID4) Bias Current			20	28	36	μA
PWM Controller Error Amplifier						
DC Gain			--	85	--	DB
Bandwidth			--	10	--	MHz
Slew Rate		$C_L = 10pF$	--	5	--	V/ μS

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Current Sense GM Amplifier						
ISP 1,2,3,4 Full Scale Source Current			50	--	--	μA
ISP 1,2,3,4 Current for OCP			80	90	--	μA
Protection						
IMAX Voltage		$R_{\text{IMAX}} = 15\text{k}$	0.55	0.6	0.65	V
SS Current		$V_{\text{SS}} = 1\text{V}$	8	13	18	μA
Over-Voltage Trip (VSEN/DACOUT)			118	122	126	%
Power Good						
Upper Threshold (VSEN/DACOUT)		VSEN Rising	106	110	114	%
Lower Threshold (VSEN/DACOUT)		VSEN Rising	86	92	94	%

Function Block Diagram

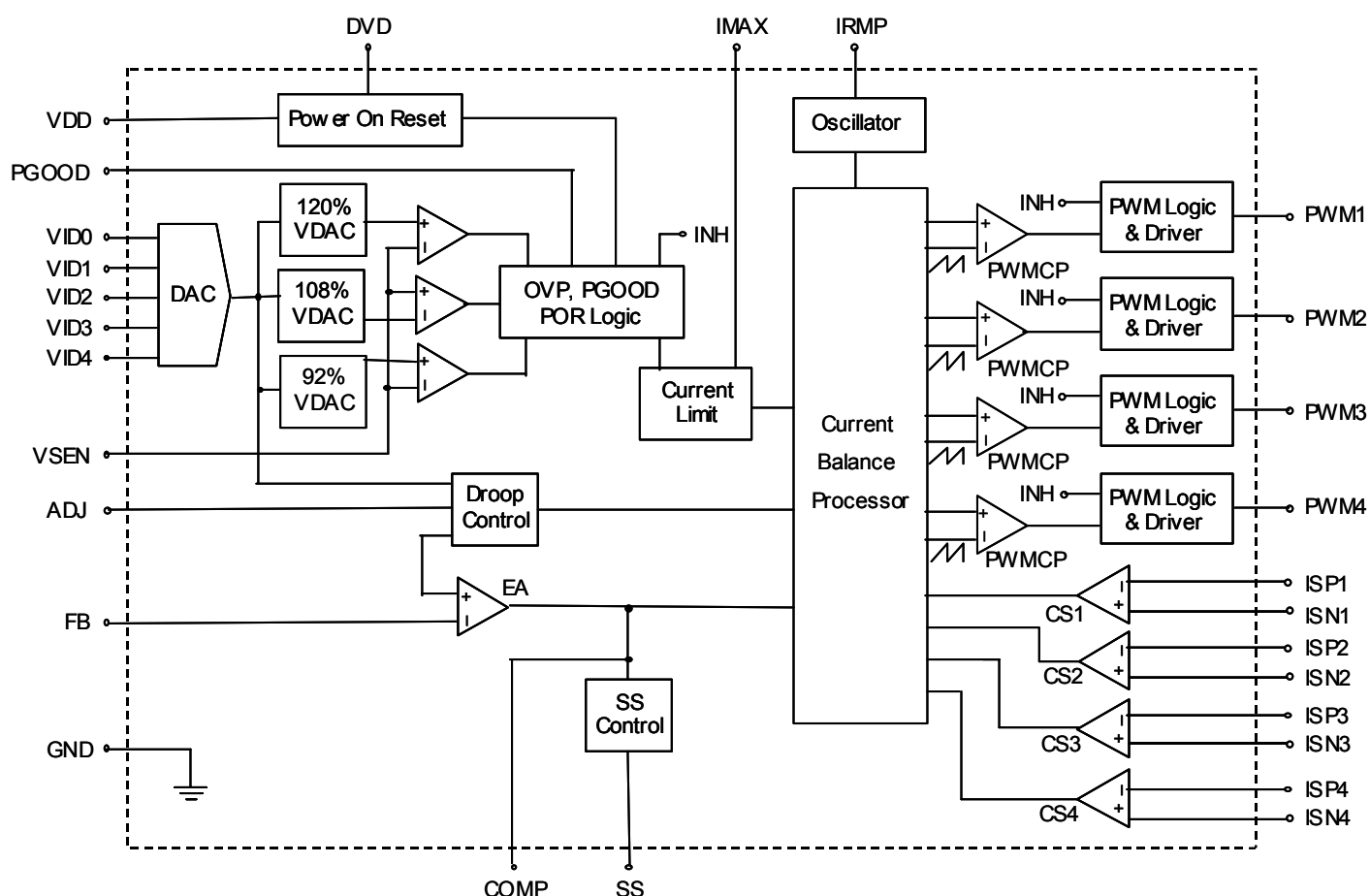
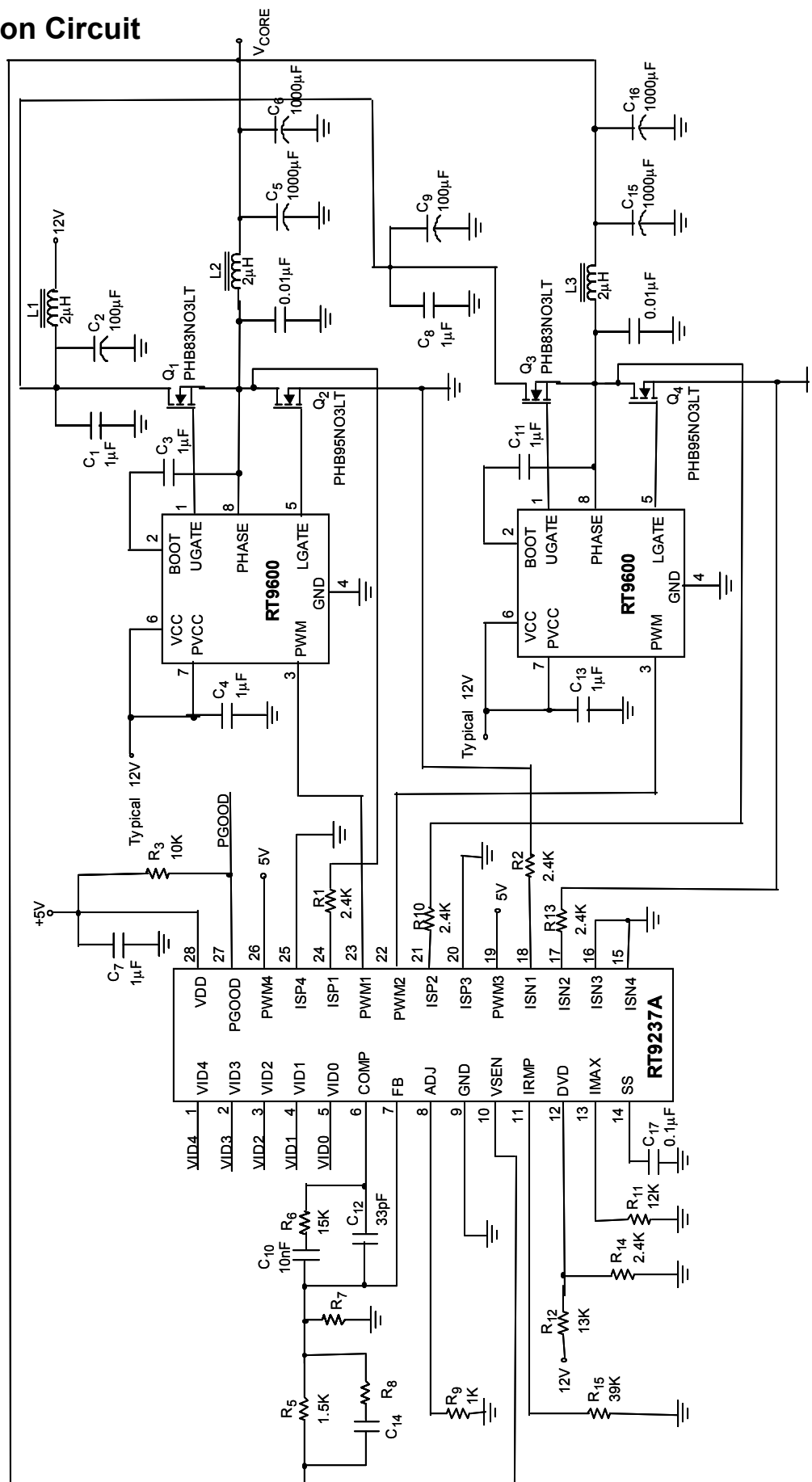


Table 1 Output Voltage Program

Pin Name					Nominal Output Voltage DACOUT
VID4	VID3	VID2	VID1	VID0	
1	1	1	1	1	Off
1	1	1	1	0	1.100V
1	1	1	0	1	1.125V
1	1	1	0	0	1.150V
1	1	0	1	1	1.175V
1	1	0	1	0	1.200V
1	1	0	0	1	1.225V
1	1	0	0	0	1.250V
1	0	1	1	1	1.275V
1	0	1	1	0	1.300V
1	0	1	0	1	1.325V
1	0	1	0	0	1.350V
1	0	0	1	1	1.375V
1	0	0	1	0	1.400V
1	0	0	0	1	1.425V
1	0	0	0	0	1.450V
0	1	1	1	1	1.475V
0	1	1	1	0	1.500V
0	1	1	0	1	1.525V
0	1	1	0	0	1.550V
0	1	0	1	1	1.575V
0	1	0	1	0	1.600V
0	1	0	0	1	1.625V
0	1	0	0	0	1.650V
0	0	1	1	1	1.675V
0	0	1	1	0	1.700V
0	0	1	0	1	1.725V
0	0	1	0	0	1.750V
0	0	0	1	1	1.775V
0	0	0	1	0	1.800V
0	0	0	0	1	1.825V
0	0	0	0	0	1.850V

Note: (1) 0:Connected to GND (2) 1:Open

Typical Application Circuit



Functional Pin Description

VID4, VID3, VID2, VID1 and VID0 (Pin1,2,3,4,5)

DAC voltage identification inputs for VRM9.0. These pins are TTL-compatible and internally pulled to VDD if left open.

COMP (Pin 6)

Output of the error amplifier and input of the PWM comparator.

FB (Pin 7)

Inverting input of the internal error amplifier.

ADJ (Pin 8)

Current sense output for active droop adjust. Connect a resistor from this pin to GND to set the amount of load droop.

GND (Pin 9)

Ground for the IC.

VSEN (Pin 10)

Power good and over voltage monitor input. Connect to the microprocessor-CORE voltage.

IRMP (Pin 11)

PWM ramp amplitude set by external resistor. Ramp amplitude = $1V \times (112K\Omega / R[IRMP])$

DVD (Pin 12)

Programmable power UVLO detection input. Trip threshold = 1.25V at V(DVD) rising

IMAX (Pin 13)

Over current protection amplitude set.

SS (Pin 14)

Connect this SS pin to GND with a capacitor to set the start time interval. Pull this pin below 1V(ramp valley of saw-tooth wave in pulse width modulator) to shutdown the converter output.

ISEN1 (Pin 18), ISEN2 (Pin 17), ISEN3 (Pin 16) and ISEN4 (Pin 15)

Current sense inputs from the individual converter channel's sense component GND nodes.

ISP1 (Pin 24), ISEN2 (Pin 21), ISEN3 (Pin 20) and ISEN4 (Pin 25)

Current sense inputs for individual converter channels. Tie this pin to the component sense node.

PWM1 (Pin 23), PWM2 (Pin 22), PWM3 (Pin 19) and PWM4 (Pin 26)

PWM outputs for each driven channel. Connect these pins to the PWM input of the MOSFET driver. For systems which use 3 channels, connect PWM4 high. Two channel systems connect PWM3 and PWM4 high.

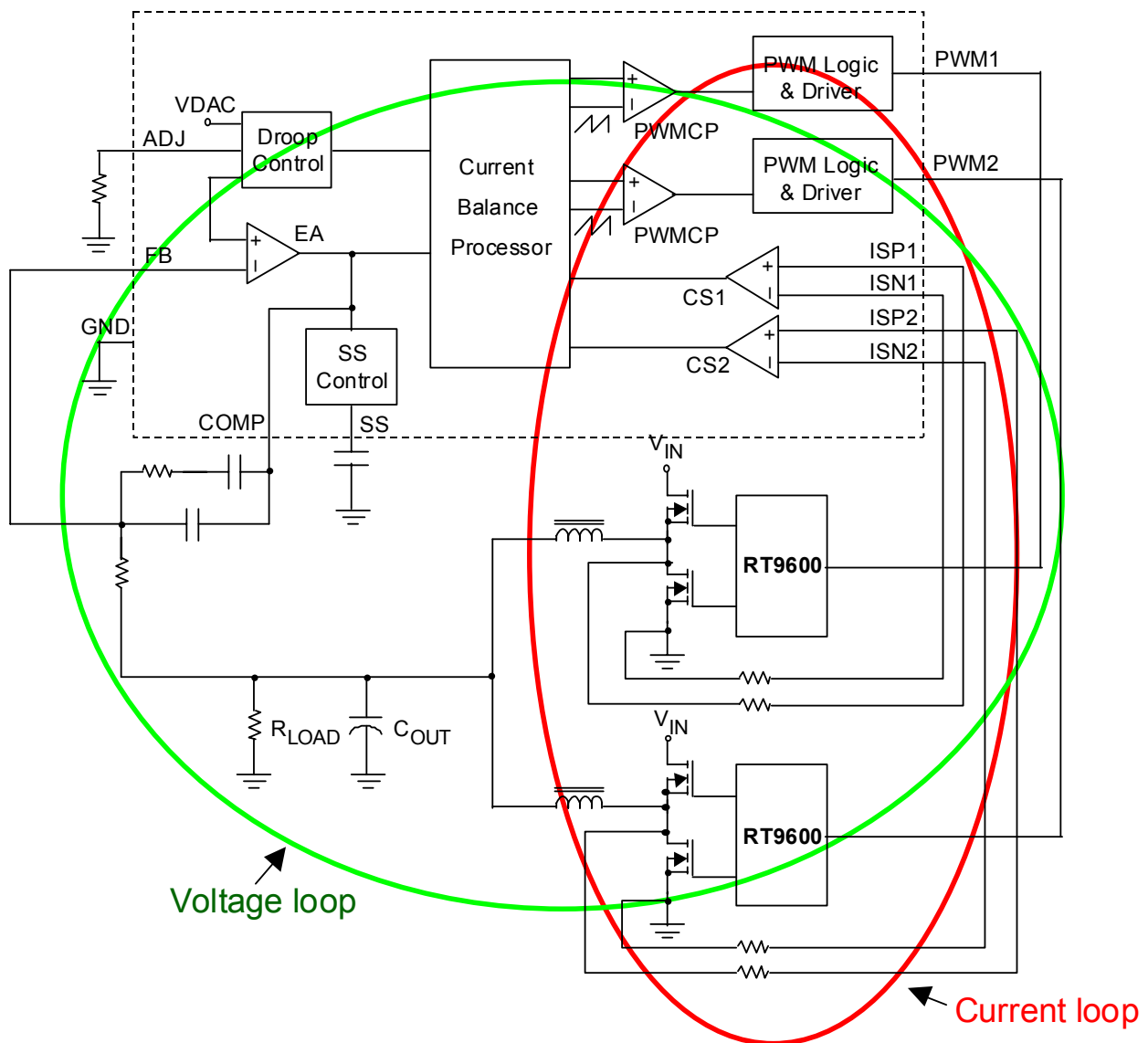
PGOOD (Pin 27)

Power good open-drain output.

VDD (Pin 28)

IC power supply. Connect this pin to a 5V supply.

Simplified Block Diagram Control Loops for a Two Phase Converter



Operation

RT9237A is a multi-phase DC/DC controller that precisely regulates CPU core voltage and balances the current of different power channels. The converter consists of RT9237A and its companion MOSFET driver provide high quality CPU power and all protection function to meet the requirement of modern VRM.

Voltage control

The reference of V_{CORE} is provided by a 5-bit DAC of VRM9.0 specification. Control loop consists of error amplifier, multi-phase pulse width modulator, driver and power components. Like conventional voltage mode PWM controller, the output voltage is locked at the V_{REF} of error amplifier and the error signal is used as the control signal VC of pulse width modulator. The PWM signals of different channels are generated by comparison of EA output and split-phase saw-tooth wave. Power stage transforms V_{IN} to output by PWM signal on-time ratio.

Current balance

RT9237A senses the current of low side MOSFET in each synchronous rectifier when it is conducting for channel current balance and droop tuning. The differential sensing GM amplifier converts the voltage on the sense component (can be a sense resistor or the $R_{DS(ON)}$ of the low side MOSFET) to current signal into internal balance circuit. The current balance circuit sums and averages the current signals then produces the balancing signals injected to pulse width modulator. If the current of some power channel is greater than average, the balancing signal reduces the output pulse width to keep the balance.

Load Droop

The sensed power channel current signals regulate the reference of DAC to form a output voltage droop proportional to the load current. The droop or so call "active voltage positioning" can reduce the output voltage ripple at load transient and the LC filter size.

Fault detection

The chip detects V_{CORE} for over voltage and power good detection. The "hiccup mode" operation of over current protection is adopted to reduce the short circuit current. The in-rush current at the start up is suppressed by the soft start circuit through clamping the pulse width and output voltage.

Application Circuit setting

Phase setting and converter start up

RT9237A interface with companion MOSFET driver (like RT9600 or HIP660X series) for correct converter initialization. The tri-phase PWM output (high, low, high impedance) pins sense the interface voltage at IC POR acts (both VDD and DVD trip). The channel is enabled if the pin voltage is 1.2V less than VDD. Please tie the PWM output to VDD and the current sense pins to GND or left float if the channel is unused. For 2-channel application, connect PWM3 and PWM4 high. 3-channel application connect PWM4 high.

Current sensing setting

RT9237A senses the current of low side MOSFET in each synchronous rectifier when it is conducting for channel current balance and droop tuning. The differential sensing GM amplifier converts the voltage on the sense component (can be a sense resistor or the $R_{DS(ON)}$ of the low side MOSFET) to current signal into internal circuit (see Fig.1).

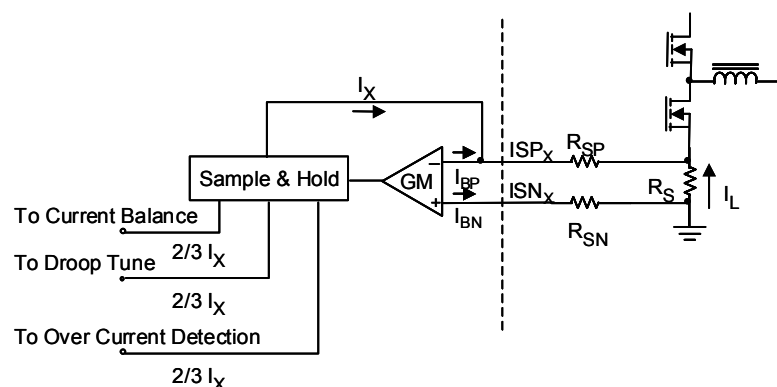


Fig.1 Current Sense Circuit

The sensing circuit gets $I_X = \frac{I_L \times R_S}{R_{SP}}$ by local feedback. $R_{SP} = R_{SN}$ to cancel the voltage drop caused by GM amplifier input bias current. I_X is sampled and held just before low side MOSFET turns off (See Fig.2).

Therefore,

$$I_{X(S/H)} = \frac{I_{L(S/H)} \times R_S}{R_{SP}}, \quad I_{L(S/H)} = I_{L(AVG)} - \frac{V_O}{L} \times \frac{T_{OFF}}{2},$$

$$T_{OFF} = \left(\frac{V_{IN} - V_O}{V_{IN}} \right) \times 10\mu S, \text{ for operating frequency} = 100kHz$$

$$I_{X(S/H)} = \left[I_{L(AVG)} - \frac{V_O - \left(\frac{V_{IN} - V_O}{V_{IN}} \right) \times 10\mu S}{2L} \right] \times \frac{R_S}{R_{SP}}$$

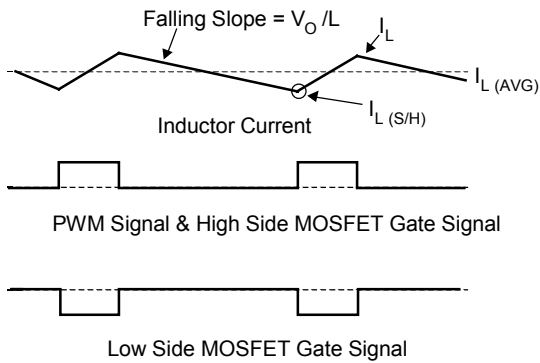


Fig. 2 Inductor Current and PWM Signal

Droop Tuning

The S/H current signals from power channels are injected to ADJ pin to create droop voltage.

$$V_{ADJ} = R_{ADJ} \times \frac{2}{3} \sum I_X$$

The DAC output voltage decreases by V_{ADJ} to form the V_{CORE} load droop (see Fig.3).

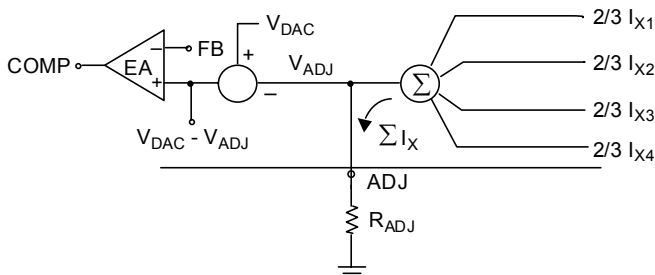


Fig. 3 Droop Tune Circuit

Protection and SS function

For OVP, the RT9237A detects the V_{CORE} by V_{SEN} pin. Eliminate the parasitic delay and noise influence on the PCB path for fast and accurate detection. The trip point of OVP is 120% of normal output level. The PWM outputs are pulled low to turn on the low side MOSFET and turn off the high side MOSFET of the synchronous rectifier at OVP. The OVP latch can only be reset by VDD or DVD restart power on reset sequence. The PGOOD detection trip point of V_{CORE} is $\pm 8\%$ out of the normal level. The PGOOD open drain output pulls low when V_{OCRE} exceeds the range.

Soft start circuit generates a ramp voltage by charging external capacitor with 10uA current after IC POR acts. The PWM pulse width and V_{CORE} are clamped by the rising ramp to reduce the in-rush current and protect the power devices.

Over current protection trip point is set by the resistor R_{IMAX} connected to IMAX pin. OCP is triggered if one channel S/H current signal $I_X > \frac{3}{2} \times \frac{0.6}{R_{IMAX}}$. Controller forces PWM output latched at high impedance to turn off both high and low side MOSFET in the power stage and initial the hiccup mode protection. The SS pin voltage is pulled low with a 10uA current after it is less than 90% VDD. The converter restarts after SS pin voltage $< 0.2V$. Three times of OCP disable the converter and only release the latch by POR acts (see Fig.4).

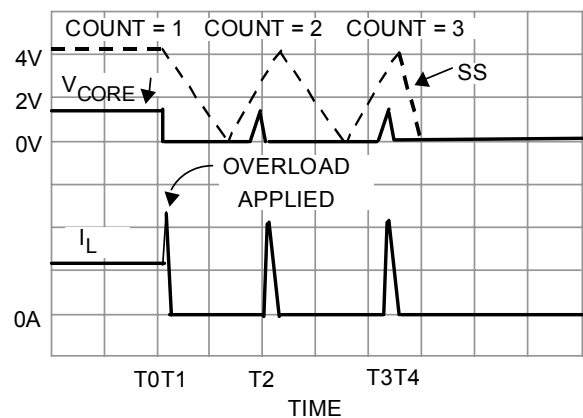
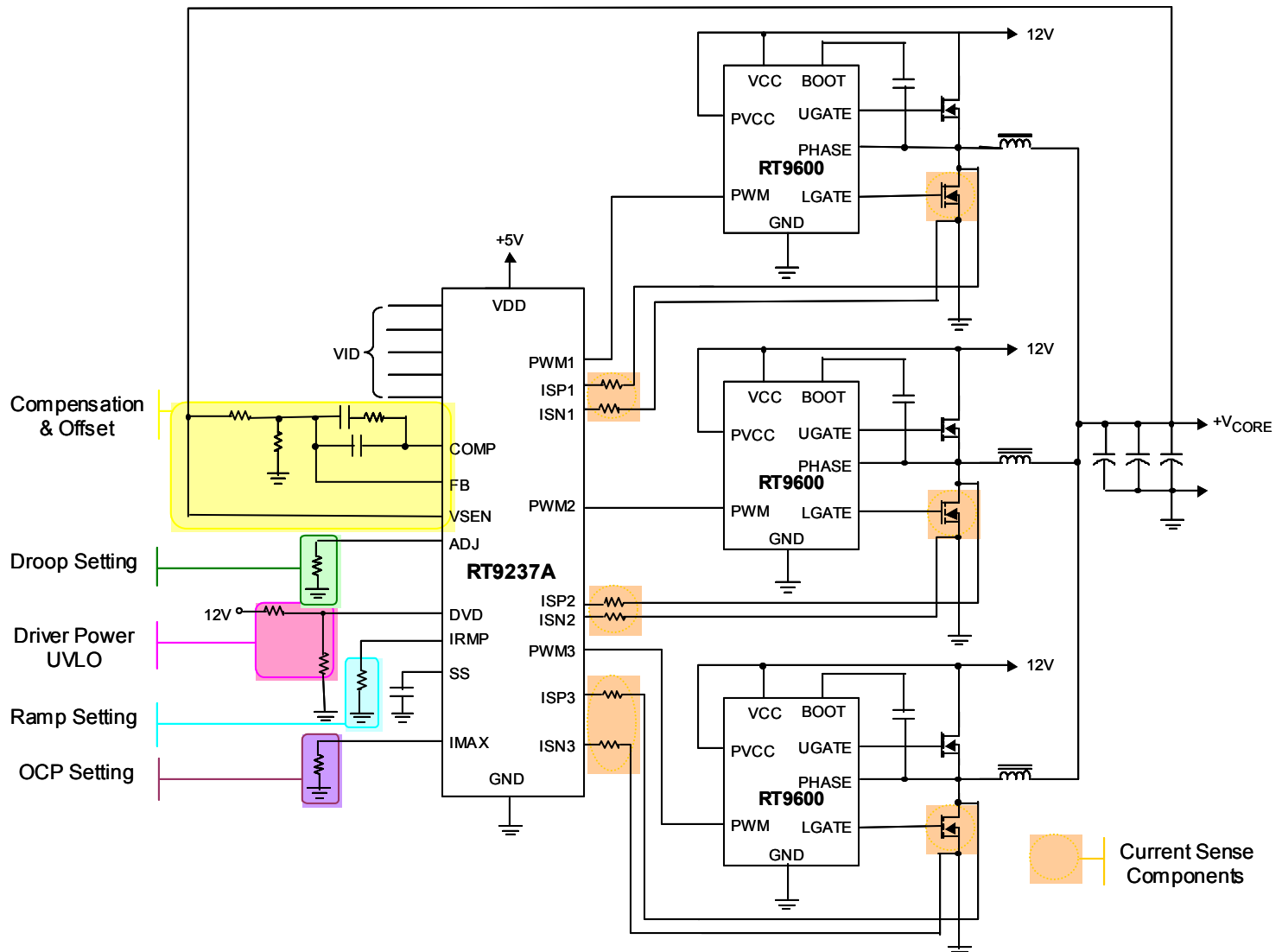


Fig. 4

3-Phase Converter and Components Function Grouping



Design Procedure Suggestion

Voltage Loop setting

- Output filter pole and zero (Inductor, output capacitor value & ESR)
- Error amplifier compensation & saw-tooth wave amplitude (compensation network & IRMP pin resistor)

Current loop setting

- GM amplifier S/H current (current sense component R_{on} , ISP_x & ISN_x pin external resistor value, keep ISP_x current $< 50\mu A$ at full load condition)
- Over current protection trip point (IMAX pin resistor, keep ISP_x current $< 80\mu A$ at OCP condition)

VRM load line setting

- Droop amplitude (ADJ pin resistor)
- No load offset (additional resistor in compensation network)

Power sequence & SS

DVD pin external resistor and SS pin capacitor

PCB layout

- Kelvin sense for current sense GM amplifier input
- Refer to layout guide for other item

Design Example

Three phase converter $V_{CORE} = 1.5V$, $V_{IN} = 12V$, full load current = 60Amp, droop voltage at full load = 120mV, OCP trip point for each power stage = 30Amp (at Sample/Hold), low side MOSFET $R_{DS(ON)} = 6m\Omega$ at room temperature, $L = 2\mu H$, $C_{OUT} = 9000\mu F$, capacitor ESR = $2m\Omega$.

1. Compensation setting

a. Modulator Gain, Pole and Zero

Modulator Gain = $\frac{V_{IN}}{V_{RAMP}}$, saw-tooth wave
 amplitude $V_{RAMP} = 1V \times \frac{112k\Omega}{R_{IMP}}$, choose $R_{IMP} = 78K$, $V_{RAMP} = 1.4V$, modulator Gain = 8.6 = 18.7dB, LC filter pole = $\frac{1}{2\pi\sqrt{LC}} = 1.2kHz$,
 ESR zero = $\frac{1}{2} \pi C_{RESR} = 8.8kHz$

b. EA compensation network

Use type 2 compensation scheme (see Fig. 5),

$$F_Z = \frac{1}{2\pi R_2 C_1}, \quad F_P = \frac{1}{2\pi R_2 \left(\frac{C_1 \times C_2}{C_1 + C_2} \right)}$$

mid-band gain = $\frac{R_2}{R_1}$. Choose $R_1 = 2.4K\Omega$, $R_2 = 24K\Omega$, $C_1 = 6.6nF$, $C_2 = 33pF$, get $F_Z = 1KHz$,

$F_P = 200KHz$, mid-band Gain=10=20dB,

modulator asymptotic Bode plot of EA

compensation and PWM loop Gain Bode

shown as Fig. 6.

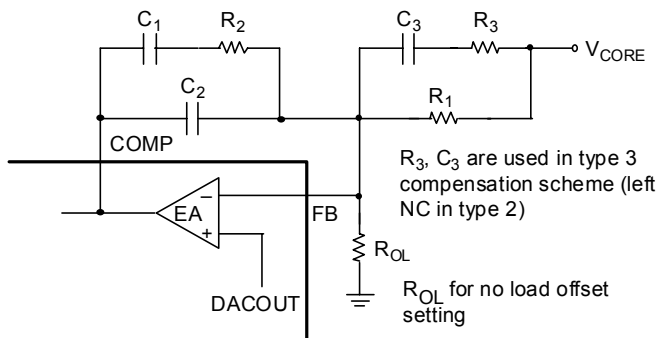


Fig. 5 EA Compensation Network

Asymptotic Bode Plot of PWM Loop Gain

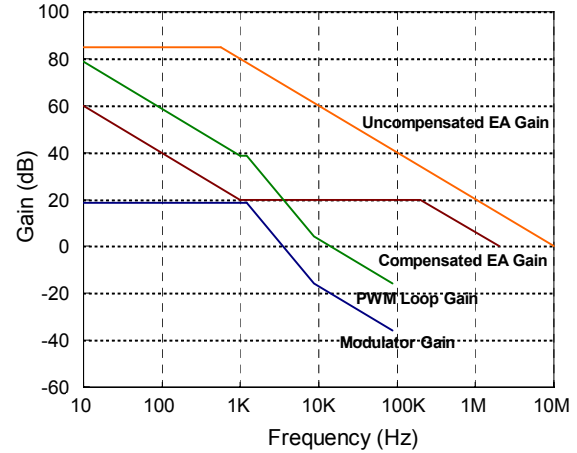


Fig. 6 Asymptotic Bode Plot of PWM Loop Gain

2. Droop setting

Full load current of each power channel = 60A/3 = 20Amp, the ripple current = $\Delta I_L =$

$$10\mu S \times \frac{1.5V}{2\mu H} \times \left(1 - \frac{1.5V}{12V} \right) = 6.56A$$

, load current at S/H = $20A - \frac{\Delta I_L}{2} = 16.72A$, GM

Amp S/H $I_{X(MAX)} = \frac{R_{DS(ON)} \times 16.72A}{R_{SP}}$, suggested I_X

at full = $40\mu A \sim 50\mu A$, choose $R_{SP} = R_{SN} = 2.4K\Omega$,

$I_{X(MAX)} = 41.8\mu A$, required Droop = 120mV =

$$41.8\mu A \times 3 \times 2/3 \times R_{ADJ}, \quad R_{ADJ} = 1.44K\Omega.$$

Take the temperature rising for consideration, if

MOSFET working temperature=70°C and the

temperature coefficient = 5000ppm/°C, the

$$R_{DS(ON)}(70^\circ C) = 6m\Omega \times \{1 + (70^\circ C - 27^\circ C) \times 5000ppm/^\circ C\} = 7.3m\Omega, \quad R_{ADJ}(70^\circ C) = R_{ADJ}(27^\circ C) \times \{R_{DS(ON)}(27^\circ C)/R_{DS(ON)}(70^\circ C)\} = 1.19K\Omega$$

3. Over Current Protection setting

OCP trip point current = 30A (at Sample/Hold),

$$I_X = \frac{R_{DS(ON)} \times 30A}{R_{SP}} = \frac{3}{2} \times \frac{0.6V}{R_{IMAX}}, \quad R_{IMAX} = 13.6K\Omega$$

Take the temperature rising for consideration,

$$R_{IMAX}(70^\circ C) = R_{IMAX}(27^\circ C) \times$$

$$\{R_{DS(ON)}(27^\circ C)/R_{DS(ON)}(70^\circ C)\} = 11.2K\Omega$$

4. SS capacitor

$C_{SS} = 0.1\mu F$ is the suitable value for most application.

Layout Guide

Layout Guide

Place the high-power switching components first, and separate them from sensitive nodes.

1. **Most critical path: the current sense circuit is the most sensitive part of the converter. The current sense resistors tied to ISP1,2,3,4 and ISN1,2,3,4 should be located not more than 0.5 inch from the IC and away from the noise switching nodes. The PCB trace of sense nodes should be parallel and as short as possible. Kelvin connection of the sense component (additional sense resistor or MOSFET $R_{DS(ON)}$) ensures the accurate stable current sensing.**

No Kelvin sense, no guarantee for stable operation!

2. Switching ripple current path:
 - a. Input capacitor to high side MOSFET
 - b. Low side MOSFET to output capacitor
 - c. The return path of input and output capacitor
 - d. Separate the power and signal GND
 - e. The switching nodes (the connection node of high/low side MOSFET and inductor) is the most noisy points. Keep them away from sensitive small-signal node.
 - f. Reduce parasitic R, L by minimum length, enough copper thickness and avoiding of via.
3. MOSFET driver should be close to MOSFET
4. The compensation, bypass and other function setting components should be near the IC and away from the noisy power path.

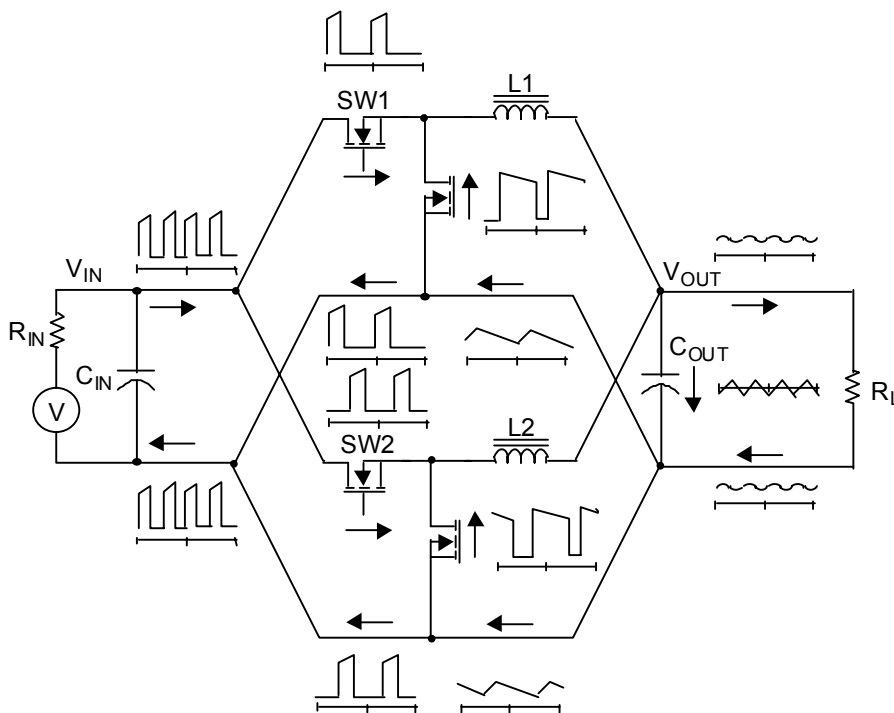


Fig.7 Power Stage Ripple Current Path

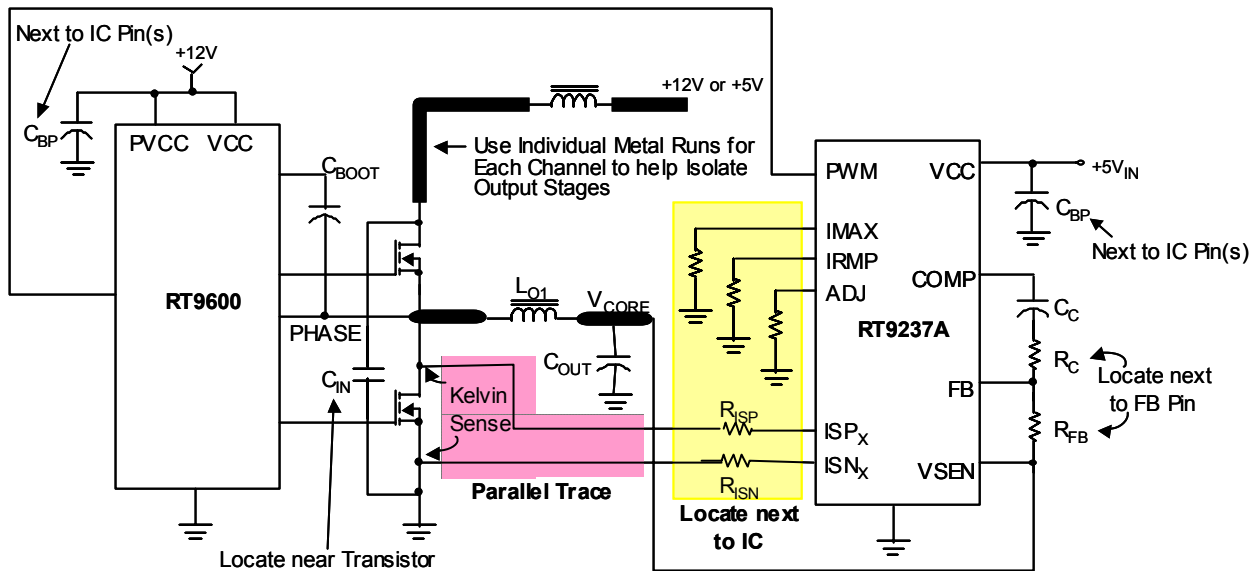
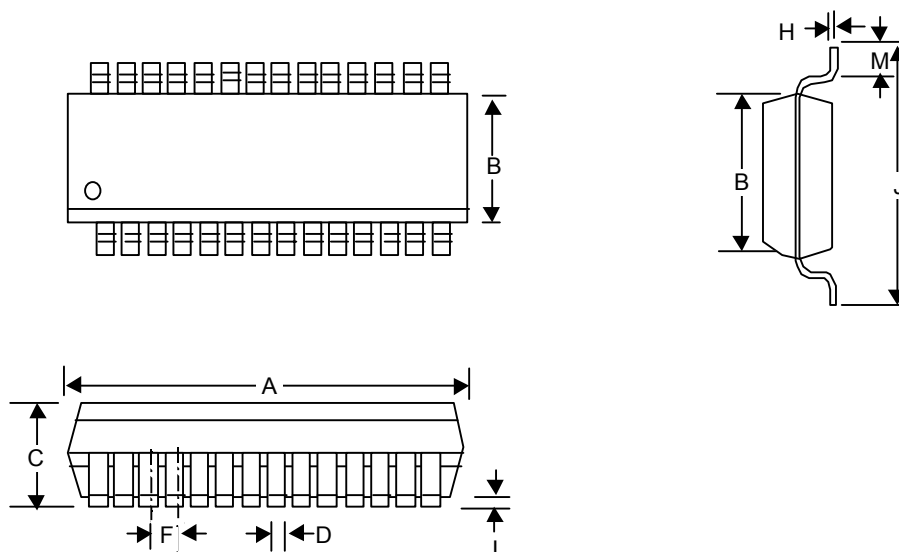


Fig.8 Layout Consideration

Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	17.704	18.110	0.697	0.713
B	7.391	7.595	0.291	0.299
C	2.362	2.642	0.093	0.104
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.229	0.330	0.009	0.013
I	0.102	0.305	0.004	0.012
J	10.008	10.643	0.394	0.419
M	0.381	1.270	0.015	0.050

28-Lead SOP Plastic Package

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