Integrated Circuit Systems, Inc.

AV9107S-04

CPU Frequency Generator

General Description

The **AV9107S-04** offers a tiny footprint solution for generating two simultaneous clocks. The 2XCPUCLK can vary between 2 and 120 MHz, with up to 16 selectable preprogrammed frequencies stored in internal ROM (frequency range depends on design option). The other clock, CPUCLK, is a divide-by-2 output and is skew-controlled within 1ns.

The device has advanced features which include on-chip loop filters, tristate outputs, and power-down capability. A minimum of external components - two decoupling capacitors and an optional ferrite bead - are all that are required for jitter-free operation. Custom masked versions, with customized frequencies and features, are available in 6-8 weeks for a small NRE.

Features

Patented on-chip Phase-Locked Loop with VCO for clock generation

- Provides 2 synthesized clocks
- Generates frequencies from 2 to 120 MHz
  2 to 32 MHz input reference frequency (depending on option)
- On-chip loop filter
- Up to 16 frequencies stored internally
- Low power CMOS technology
- Single +3.3 or +5 volt power supply
- Runs up to 80 MHz @ 3.3V
- 14-DIP or SOIC package

Applications

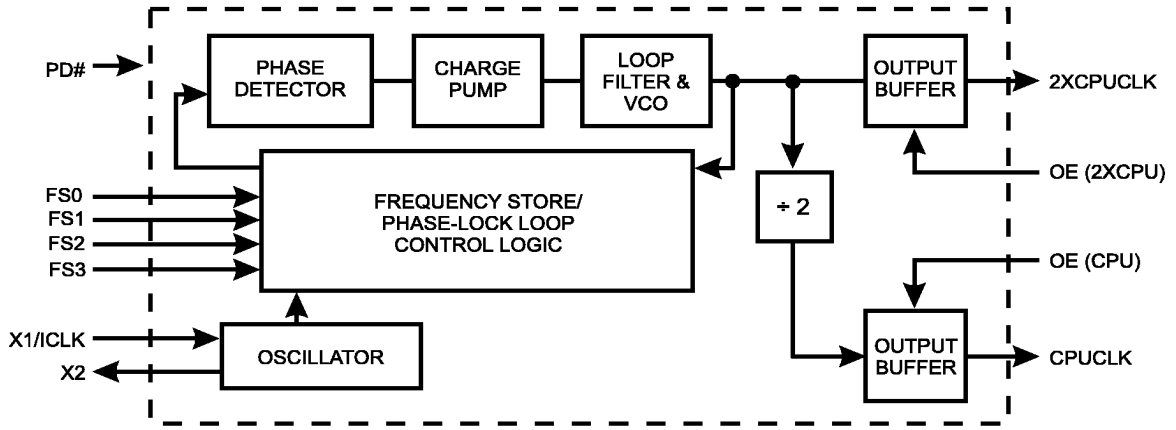
Graphics: The **AV9107S-04** is the easiest to use, lowest cost, and smallest footprint frequency generator for graphics appli-cations. It can generate up to 16 different frequencies, including all frequencies necessary for VGA standards.

Computer: The **AV9107S-04** is the ideal solution for replacing high speed oscillators and for reducing clock speeds to save power in computers. The device provides smooth, glitch-free frequency transitions so that the CPU can continue to operate during slow down or speed up. The rate of frequency change makes the **AV9107S-04** compatible with all 386DX, 386SX, 486DX, 486DX2, and 486SX devices.

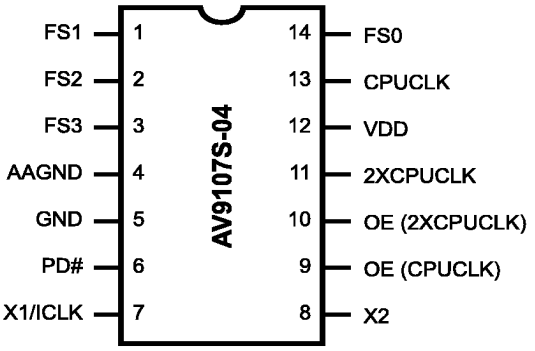
Disk Drives: Smaller than a single crystal or an oscillator, the tiny SOIC package can be used for any general purpose fre-quency generation in disk drives. The most popular application is for Constant Density Recording, where its low jitter output clock provides the necessary frequencies for reading and re-cording. Another popular application is for slowing the disk drive CPU to save power.

High Speed Systems: The **AV9107S-04** can be used as a proximity oscillator - using a low frequency (down to 2 MHz) input to generate a high frequency clock (up to 120 MHz) near the device requiring the high frequency (depending on option). This avoids the need to route high speed traces over a long distance.

Block Diagram



Pin Configuration



14-Pin DIP, SOIC

Functionality

(using a 14.318 MHz input)

FS3	FS2	FS1	FS0	2XCPUCLK	CPUCLK
0	0	0	0	80 MHz	40 MHz
0	0	0	1	66.66 MHz	33.33 MHz
0	0	1	0	50 MHz	25 MHz
0	0	1	1	40 MHz	20 MHz
0	1	0	0	100 MHz*	50 MHz*
0	1	0	1	33.33 MHz	16.67 MHz
0	1	1	0	32 MHz	16MHz
0	1	1	1	25 MHz	12.5 MHz
1	0	0	0	64 MHz	32 MHz
1	0	0	1	2X INPUT	INPUT
1	0	1	0	3X INPUT	1.5X INPUT
1	0	1	1	8X INPUT*	4X INPUT*
1	1	0	0	.5X INPUT	.25X INPUT
1	1	0	1	.25X INPUT	.125X INPUT
1	1	1	0	120 MHz*	60 MHz*
1	1	1	1	Note 1	Note 1

*5V V_{DD} only.

Note 1: This frequency select (1111) will operate at 130 MHz (2XCPUCLK) and 65 MHz (CPUCLK) only for $V_{DD} \geq 5.0V$. It is not guaranteed for 4.5V or any condition less than 5.0V.

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	FS1	Input	Frequency Select 1 (see decoding table). Pull-up.
2	FS2	Input	Frequency Select 2 (see decoding table). Pull-up.
3	FS3	Input	Frequency Select 3 (see decoding table). Pull-up.
4	AGND	-	Analog Ground.
5	GND	-	Digital Ground.
6	PD#	Input	Power-down. Shuts off entire chip when low. Pull-up.
7	X1/ICLK	Input	Crystal Input or Input Clock frequency. Typically 14.318 MHz system clock.
8	X2	Output	Crystal Output (No Connect when clock used.).
9	OE (CPUCLK)	Input	Output Enable. Tristates CPUCLK when low. Pull-up.
10	OE (2XCPUCLK)	Input	Output Enable. Tristates 2XCPUCLK when low. Pull-up.
11	2XCPUCLK	Output	2X CPU Clock Output (see decoding table, Note 2 below).
12	VDD	-	Digital power supply.
13	CPUCLK	Output	CPU Clock Output (see decoding table, Note 2 below).
14	FS0	Input	Frequency Select 0 (see decoding table). Pull-up.

Note 2: The CPUCLK and 2XCPUCLK outputs are skew controlled to within 1.0ns max.

Frequency Accuracy and Calculation

The accuracy of the frequencies produced by the **AV9107S-04** depends on the input frequency and the desired actual output frequency. The formula for calculating the exact frequency is as follows:

$$\text{Output Frequency} = \text{Input Frequency} \times \frac{A}{B}$$

where A=2, 3, 4 ... 128, and
B=2, 3, 4 ... 32.

For example, to calculate the actual output frequency for a video monitor expecting a 44.900 MHz clock and using a 14.318 MHz input clock, the closest A/B ratio is 69/22, which gives an output of 44.906 MHz (within 0.02% of the target frequency). Generally, the **AV9107S-04** can produce frequen-cies within 0.1% of the desired output.

Allowable Input and Output Frequencies for Possible Options

The input frequency should be between 2 and 32 MHz and the A/B ratio should not exceed 24. The output should fall in the range of 2-120 MHz.

Output Enable

The Output Enable feature tristates the specified output clock pins. This places the selected output pins in a high impedance state to allow for system level diagnostic testing.

Power-Down

The power-down pin shuts off the PLL and entire chip to save current when this pin is pulled low. A few milliseconds are required to reach full functioning speed from a power-down state.

Absolute Maximum Ratings

AVDD, VDD referenced to GND 7V
Operating temperature under bias. . . . . 0°C to +70°C
Storage temperature . . . . . -65°C to +150°C
Voltage on I/O pins referenced to GND. . . . . GND -0.5V to VDD +0.5V
Power dissipation . . . . . 0.5 Watts

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 5V

V_{DD}=5.0V±10%

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DC Characteristics						
Input Low Voltage	V_{IL}		-	-	0.8	V
Input High Voltage	V_{IH}		2.0	-	-	V
Input Low Current	I_{IL}	V_{IN}=0V (Pull-up input)	-16.0	-6.0	-	µA
Input High Current	I_{IH}	V_{IN}=V_{DD}	-2.0	-	2.0	µA
Output Low Voltage[1]	V_{OL}	I_{OL}=10mA	-	0.15	0.40	V
Output High Voltage[1]	V_{OH}	I_{OH}=-30mA	2.4	3.25	-	V
Output Low Current[1]	I_{OL}	V_{OL}=0.8V	22.0	35.0	-	mA
Output High Current[1]	I_{OH}	V_{OH}=2.0V	-	-50.0	-35.0	mA
Supply Current	I_{DD1}	No load, 2XCPU=120 Mhz	-	33.0	55.0	mA
Supply Current	I_{DD2}	No load, 2XCPU=66 Mhz	-	24.0	42.0	mA
Supply Current; Power-down	I_{DD} $(PD\ low)_1$	No load, 0000 (includes pull-up currents)	-	45.0	100.0	µA
Supply Current; Power-down	I_{DD} $(PD\ low)_2$	No load, 1111	-	16.0	40.0	µA
Pull-up Resistor[1]	R_{pu}		-	380.0	700.0	k ohms
AC Characteristics						
Rise Time[1]	T_r	15pF load, 0.8 to 2.0V	-	0.60	1.40	ns
Fall Time[1]	T_f	15pF load, 2.0 to 0.8V	-	0.40	1.00	ns
Rise Time[1]	T_r	15pF load, 20% to 80%	-	2.0	3.5	ns
Fall Time[1]	Tf	15pF load, 80 to 20%	-	1.0	2.5	ns
Jitter, One Sigma[1]	T_{jls1}	f_{CPU} > 20 MHz	-	30	100	ps
Jitter, One Sigma[1]	T_{jls2}	24 ≥ f_{CPU} ≥ 20 MHz	-	50	100	ps
Jitter, One Sigma[1]	T_{jls3}	fCPU < 4 MHz	-	-	0.3	%
Jitter, One Sigma[1]	T_{jls4}	f2XCPU > 40 MHz	-	100	200	ps
Jitter, One Sigma[1]	T_{jls5}	7 ≥ f_{2XCPU} ≥ 40 MHz	-	80	200	ps
Jitter, One Sigma[1]	T_{jls6}	f2XCPU < 7 MHz	-	-	0.3	%
Jitter, Absolute[1]	T_{jab1}	f_{CPU} > 20 MHz	-	120	250	ps
Jitter, Absolute[1]	T_{jab2}	4 ≥ f_{CPU} ≥ 20 MHz	-	400	1200	ps
Jitter, Absolute[1]	T_{jab3}	fCPU < 4 MHz	-	-	1.0	%
Jitter, Absolute[1]	T_{jab4}	f2XCPU > 40 MHz	-	250	350	ps
Jitter, Absolute[1]	T_{jab5}	7 ≥ f_{2XCPU} ≥ 40 MHz	-	300	750	ps
Jitter, Absolute[1]	T_{jab6}	f2XCPU < 7 MHz	-	-	1.0	%
Duty Cycle[1]	D_{t1}	15pF load, @ V_{OUT}=50%	43	50	53	%
Duty Cycle[1]	D_{t2}	15pF load, @ V_{OUT}=1.4V	47	52	57	%
Input Frequency[1]	F_i		11.0	14.3	19.0	MHz
Output Frequency[1]	F_o		2.0	-	120.0	MHz
Power-up Time[1]	T_{pu}		-	7.58	18.0	ms
Transition Time[1]	T_{ft}	8 to 66.6 MHz	-	6.0	13.0	ms
Skew Window[1]	T_{sk}	2XCPUCLK to CPUCLK @ 1.4V	-	-	1.0	ns

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Characteristics at 3.3V

V_{DD}=3.3V±10%

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	$0.20V_{DD}$	V
Input High Voltage	V_{IH}		$0.7V_{DD}$	-	-	V
Input Low Current	I_{IL}	V_{IN}=0V (Pull-up input)	-7.0	-2.5	-	µA
Input High Current	I_{IH}	$V_{IN}=V_{DD}$	-2.0	-	2.0	µA
Output Low Voltage[1]	V_{OL}	I_{OL}=6mA	-	$0.05V_{DD}$	$0.1V_{DD}$	V
Output High Voltage[1]	V_{OH}	I_{OH}=-5mA	$0.85V_{DD}$	$0.92V_{DD}$	-	V
Output Low Current[1]	I_{OL}	$V_{OL}=0.2V_{DD}$	15.0	22.0	-	mA
Output High Current[1]	I_{OH}	$V_{OL}=0.7V_{DD}$	-	-17.0	-10.0	mA
Supply Current	I_{DD}	No load, 2XCPU=80 Mhz	-	15.0	30.0	mA
Supply Current; Power-down	I_{DD} (PD low)$_1$	No load, 0000 (Includes pull-up currents)	-	15.0	40.0	µA
Supply Current; Power-down	I_{DD} (PD low)$_2$	No load, 1111	-	5.0	12.0	µA
Pull-up Resistor[1]	R_{pu}		-	550.0	900.0	k ohms
AC Characteristics						
Rise Time[1]	T_r	15pF load, 20% to 80%	-	2.2	3.5	ns
Fall Time[1]	T_f	15pF load, 80% to 20%	-	1.2	2.5	ns
Jitter, One Sigma[1]	T_{jls1}	f_{CPU} > 20 MHz	-	30	100	ps
Jitter, One Sigma[1]	T_{jls2}	4 ≤ f_{CPU} ≤ 20 MHz	-	35	100	ps
Jitter, One Sigma[1]	T_{jls3}	fCPU < 4 MHz	-	-	0.3	%
Jitter, One Sigma[1]	T_{jls4}	f2XCPU > 40 MHz	-	170	300	ps
Jitter, One Sigma[1]	T_{jls5}	7 ≤ f_{2XCPU}≤ 40 MHz	-	170	350	ps
Jitter, One Sigma[1]	T_{jls6}	f2XCPU < 7 MHz	-	-	0.3	%
Jitter, Absolute[1]	T_{jab1}	f_{CPU} > 20 MHz	-	140	250	ps
Jitter, Absolute[1]	T_{jab2}	4 ≥ f_{CPU} ≥ 20 MHz	-	200	700	ps
Jitter, Absolute[1]	T_{jab3}	fCPU < 4 MHz	-	-	1.0	%
Jitter, Absolute[1]	T_{jab4}	f2XCPU > 40 MHz	-	300	500	ps
Jitter, Absolute[1]	T_{jab5}	7 ≤ f_{2XCPU} ≤ 40 MHz	-	300	900	ps
Jitter, Absolute[1]	T_{jab6}	f2XCPU < 7 MHz	-	-	1.0	%
Duty Cycle[1]	D_{t1}	15pF load, 50%	42	50	52	%
Duty Cycle[1]	D_{t2}	15pF load, 1.4V	38	47	52	%
Input Frequency[1]	F_i		13.3	14.3	15.3	MHz
Output Frequency[1]	F_o		2.0	-	80.0	MHz
Power-up Time[1]	T_{pu}		-	7.58	18.0	ms
Transition Time[1]	T_{ft}	8 to 66.6 Mhz	-	6.0	13.0	ms
Skew Window[1]	T_{sk}	2XCPUCLK to CPUCLK @ 1.4V	-	-	1.0	ns

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

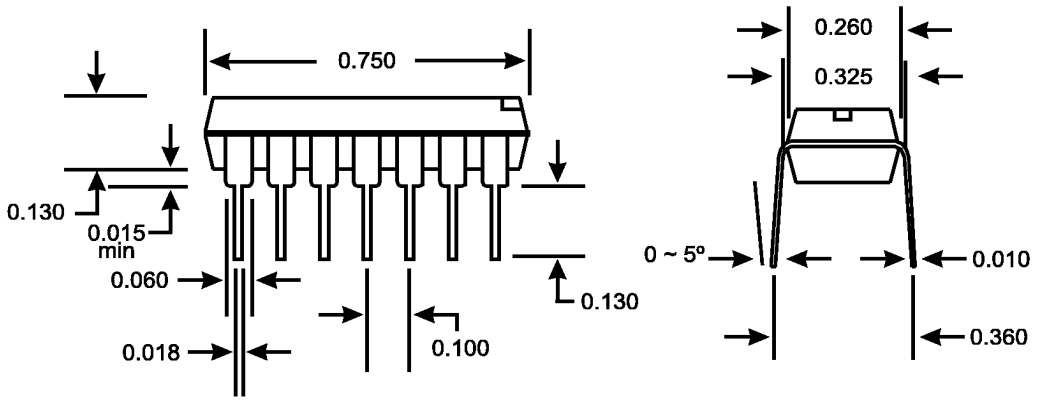
Actual Output Frequencies for AV9107S-04

(using a 14.318 MHz input)

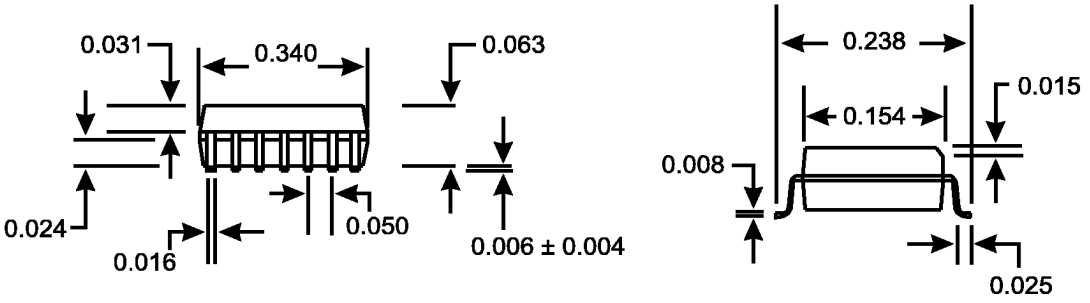
FS3	FS2	FS1	FS0	2XCPUCLK	CPUCLK
0	0	0	0	80.02 Mhz	40.01 MHz
0	0	0	1	66.66 Mhz	33.31 MHz
0	0	1	0	50.11 Mhz	25.06 MHz
0	0	1	1	40.01 Mhz	20.00 MHz
0	1	0	0	100.23 Mhz*	50.11 MHz*
0	1	0	1	33.31 Mhz	16.66 MHz
0	1	1	0	32.01 Mhz	16.00MHz
1	1	1	1	25.06 Mhz	12.47 MHz
1	0	0	0	64.02 Mhz	32.01 MHz
1	0	0	1	2X INPUT	1X INPUT
1	0	1	0	3X INPUT	1.5X INPUT
1	0	1	1	8X INPUT	4X INPUT
1	1	0	0	.5X INPUT	.25X INPUT
1	1	0	1	.25X INPUT	.125X INPUT
1	1	1	0	120.00 Mhz*	60.00 MHz*
1	1	1	1	129.96 Mhz**	64.98 MHz**

* 5V V_{DD} only.

** This frequency select (1111) will operate at 130 MHz (2XCPUCLK) and 65 MHz (CPUCLK) only for $V_{DD} \geq 5.0V$. It is not guaranteed for 4.5V or any condition less than 5.0V.



14-Pin DIP Package



14-Pin SOIC Package

Ordering Information

AV9107S-04CN14 or AV9107S-04CS14

Example:

XXX XXXX-PPP M X#W

Lead Count & Package Width
Lead Count=1, 2 or 3 digits
W=.3" SOIC or .6" DIP; None=Standard Width

Package Type
N=DIP
S=SOIC

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device