Low Cost 16 Pin Frequency Generator

Features

- Compatible with 286, 386, and 486 CPUs
- Generates up to 6 output clocks for CPU plus peripherals
- Up to 100 MHz
- All loop filter components internal
- Skew controlled 2X and 1X CPU clocks
- 3V and 5V versions
- 16 pin PDIP or 150 mil wide SOIC
- Power down options

Applications

Computer Motherboards: The AV9154 replaces crystals and oscillators, saving board space, component cost, part count, and inventory costs. It produces a switchable CPU clock, and up to four fixed clocks to drive floppy disk, communications, super I/O, bus, and/or keyboard devices. The small package and 3V operation is perfect for handheld computers.

Disk Drives: The low profile, narrow SOIC package makes this a popular device for replacing expensive surface mount oscillators in space-critical disk drives.

General Description

The AV9154 is a low cost frequency generator designed for general purpose PC and disk drive applications. Its CPU clocks provide all necessary frequencies for 286, 386 and 486 systems, including support for the latest speeds of processors. The standard devices use a 14.318 MHz crystal to generate the CPU and peripheral clocks for integrated desktop and notebook motherboards.

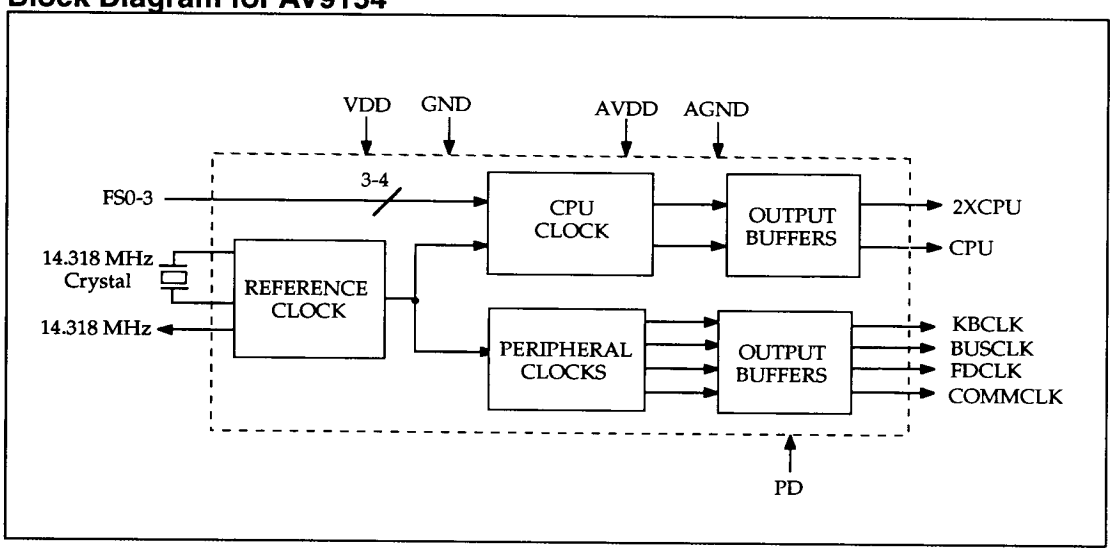
The CPU clock offers the unique feature of smooth, glitch-free transitions from one frequency to the next, making this the ideal device to use whenever slowing the CPU speed. The AV9154 makes a gradual transition between frequencies, so that it obeys the Intel cycle to cycle timing specification for 486 systems.

The simultaneous 2X and 1X CPU clocks offer controlled skew to within 1.0ns (max) of each other.

ICS has been shipping Motherboard Frequency Generators since April 1990, and is the leader in the area of multiple output clocks on a single chip. The AV9154 uses the same technology as ICS's highly successful AV9107 and AV9155 products. ICS offers a broad family of frequency generators for motherboards, graphics and other applications, including cost effective versions with only one or two output clocks. Consult ICS for all of your clock generation needs.

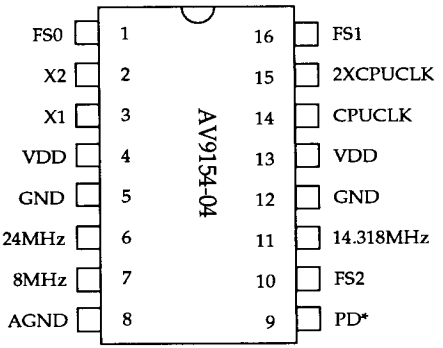
D

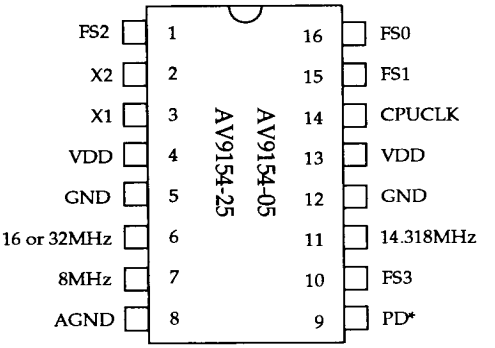
Block Diagram for AV9154

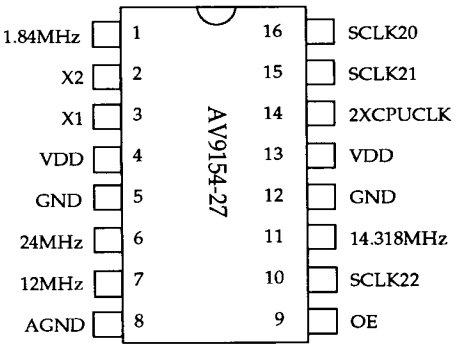


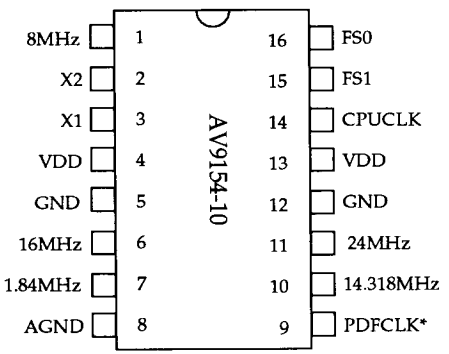
Pentium™ is a trademark of Intel Corporation

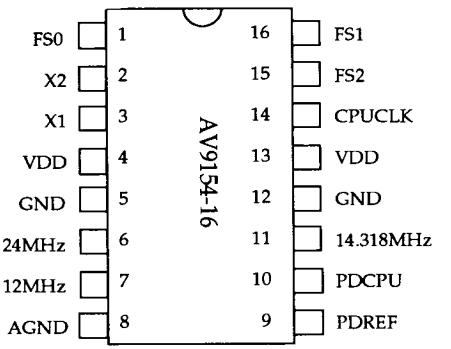
Pin Configurations











* Active low

Pin Description for AV9154-04, -05, -10, -16, -25, -27

Pin Name	Pin Type	Description	Pin # -04	-05	-10	-16	-25	-27
VDD	P	Digital Power (+3.3V or +5V)	4	4	4	4	4	4
VDD	P	Digital Power (+3.3V or +5V)	13	13	13	13	13	13
GND	P	Digital GROUND	5	5	5	5	5	5
GND	P	Digital GROUND	12	12	12	12	12	12
AGND	P	ANALOG GROUND	8	8	8	8	8	8
FS0	I	FREQUENCY SELECT 0 for CPUCLK	1	16	16	1	16	16
FS1	I	FREQUENCY SELECT 1 for CPUCLK	16	15	15	16	15	15
FS2	I	FREQUENCY SELECT 2 for CPUCLK	10	1	-	15	1	10
FS3	I	FREQUENCY SELECT 3 for CPUCLK	-	10	-	-	10	-
PDREF	I	POWER DOWN REFERENCE Clock (14.318 MHz) (Active High)	-	-	-	9	-	-
PDCPU	I	POWER DOWN CPU Clock (Active High)	-	-	-	10	-	-
PD*	I	POWER DOWN All (Active Low)	9	9	-	-	9	-
PDFCLK*	I	POWER DOWN FIXED CLOCK (1.84, 8, 16, 24)	-	-	9	-	-	-
X1	I	CRYSTAL IN	3	3	3	3	3	3
X2	O	CRYSTAL OUT	2	2	2	2	2	2
32MHz	O	32 MHz clock output	-	-	-	-	6	-
24MHz	O	24 MHz clock output	6	-	11	6	-	6
16MHz	O	16 MHz clock output	-	6	6	-	-	-
12MHz	O	12 MHz clock output	-	-	-	7	-	7
8MHz	O	8 MHz clock output	7	7	1	-	7	-
1.84MHz	O	1.84 MHz clock output	-	-	7	-	-	1
14.318MHz	O	14.318 MHz reference clock output	11	11	10	11	11	11
CPUCLK	O	CPU CLOCK output determined by status of FS0 - FS3	14	14	14	14	14	-
2XCPUCLK	O	2X CPU CLOCK output	15	-	-	-	-	14

*Active Low

D

Clock Tables in MHz
(All parts shown will operate at 3V)

FS(3:0)	-04		-05	-10	-16	-25	-27
	2XCPU	CPU	CPUCLK	CPUCLK	CPUCLK	CPUCLK	CPUCLK
0	100*	50*	2	PDCPU	16	2	75
1	80*	40*	8	40	20	8	32
2	66.6*	33.3*	16	50	25	16	60
3	50	25	20	66.6*	33.3	20	40
4	40	20	25	-	40	25	50
5	32	16	33.3*	-	50	33.3*	66.66
6	24	12	40*	-	66.6*	40*	80
7	16	8	50*	-	80*	50*	52
8	-	-	4	-	-	4	-
9	-	-	16	-	-	16	-
A	-	-	32	-	-	32	-
B	-	-	40	-	-	40	-
C	-	-	50	-	-	50	-
D	-	-	66.6*	-	-	66.6*	-
E	-	-	80*	-	-	80*	-
F	-	-	100*	-	-	100*	-
Floppy	24		-	24	24	-	24
Bus	-		16	16	-	32	-
Kybd	8		8	8	12	8	12
Comm	-		-	1.84	-	-	1.84
Refclk	14.318		14.318	14.318	14.318	14.318	14.318
3V	up to 50 MHz		up to 50 MHz	up to 50 MHz	up to 50 MHz	up to 50 MHz	up to 50 MHz

Smooth Transitions

Smooth Transitions

* These selections will only operate at 5V

Actual Output Frequencies
(using 14.318 MHz input. All frequencies in MHz)

FS(3:0)	-04		-05	-10	-16	-25	-27	
	2XCPU	CPU	CPUCLK	CPUCLK	CPUCLK	CPUCLK	2XCPUCLK	
0	100.23*	50.11*	2.15	PDCPU	16.11	2.15	75.17	Smooth Transitions
1	80.18*	40.09*	8.18	40.09	20.05	8.18	31.94	
2	66.48*	33.24*	16.11	50.11	25.06	16.11	60.136	
3	50.11	25.06	20.05	66.48*	33.41	20.05	40.09	
4	40.09	20.05	25.06	-	40.09	25.06	50.11	
5	32.22	16.11	33.24*	-	50.11	33.24*	66.48	
6	24.23	12.12	40.09*	-	66.48*	40.09*	80.18	
7	15.75	7.88	50.11*	-	80.18*	50.11*	51.90	
8	-	-	4.30	-	-	4.30	-	Smooth Transitions
9	-	-	16.11	-	-	16.11	-	
A	-	-	32.22	-	-	32.22	-	
B	-	-	40.09	-	-	40.09	-	
C	-	-	50.11	-	-	50.11	-	
D	-	-	66.48*	-	-	66.48*	-	
E	-	-	80.18*	-	-	80.18*	-	
F	-	-	100.23*	-	-	100.23*	-	
Floppy	24.00		-	24.00	24.00	-	24	
Bus	-		16.00	16.00	-	32.01	-	
Kybd	8.00		8.00	8.00	12.00	8.00	12	
Comm	-		-	1.846	-	-	1.846	
Refclk	14.318		14.318	14.318	14.318	14.318	14.318	

* These selections will only operate at 5V

Absolute Maximum Ratings

VDD referenced to GND..... 7V
Operating temperature under bias..... 0°C to +70°C
Storage temperature..... -40°C to +150°C
Voltage on I/O pins referenced to GND..... GND -0.5V to VDD +0.5V
Power dissipation..... 0.5 Watts

Note: Stresses above those listed under Absolute Maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may affect devices reliability.

Electrical Characterisitcs at 5V

(V_{DD} = +5V± 10%, T_A = 0°C to 70°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
DC Characteristics						
V_{IL}	Input Low Voltage			0.8	V	V_{DD} = 5V
V_{IH}	Input High Voltage	2.0			V	V_{DD} = 5V
I_{IL}	Input Low Current			-5	µA	V_{IN} = 0V
I_{IH}	Input High Current			5	µA	V_{IN} = V_{DD}
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4mA
V_{OH}	Output High Voltage	V_{DD}-.4V			V	I_{OH} = -1mA,V_{DD}=5.0V
V_{OH}	Output High Voltage	V_{DD}-.8V			V	I_{OH} = -4mA,V_{DD}=5.0V
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -8mA
I_{DD}	Supply Current		25	40	mA	[1]No load
F_D	Output Frequency Change over Supply and Temperature		0.002	0.01	%	With respect to typical frequency
I_{SC}	Short circuit current	25	40		mA	Each output clock
C_i	Input Capacitance			10	pF	Except X1, X2
C_L	Load Capacitance		20		pF	Pins X1, X2
I_{DDSTBY}	Supply Current, power down		30		µA	
AC Characteristics						
t_{ICr}	Input Clock Rise Time			20	ns	
t_{ICf}	Input Clock Fall Time			20	ns	
t_r	Output Rise time, 0.8 to 2.0V	-	1	2	ns	15 pf load
t_r	Rise time, 20% to 80% V_{DD}	-	2	4	ns	15 pf load
t_f	Output Fall time, 2.0 to 0.8V	-	1	2	ns	15 pf load
t_f	Fall time, 80% to 20% V_{DD}	-	2	4	ns	15 pf load
d_t	Duty cycle	40/60	48/52	60/40	%	15 pf load
d_t	Duty cycle, reference clocks	40/60	43/57	60/40	%	15 pf load
t_{jis}	Jitter, one sigma		0.8	2.5	%	As compared with
t_{jab}	Jitter, absolute		2	5	%	clock period
t_{jab}	Jitter, absolute			700	ps	16-100 MHz clocks
f_i	Input Frequency		14.318		MHz	
T_{sk}	Clock skew between CPU and 2XCPU outputs		0.5	1.0	ns	AV9154-04
t_{ft}	Frequency Transition time		15	20	ms	From 8 to 100 MHz

Notes:
1. All clocks on AV9154-05 running at highest possible frequencies. Power supply current can change substantially with different mask configurations. Consult ICS.

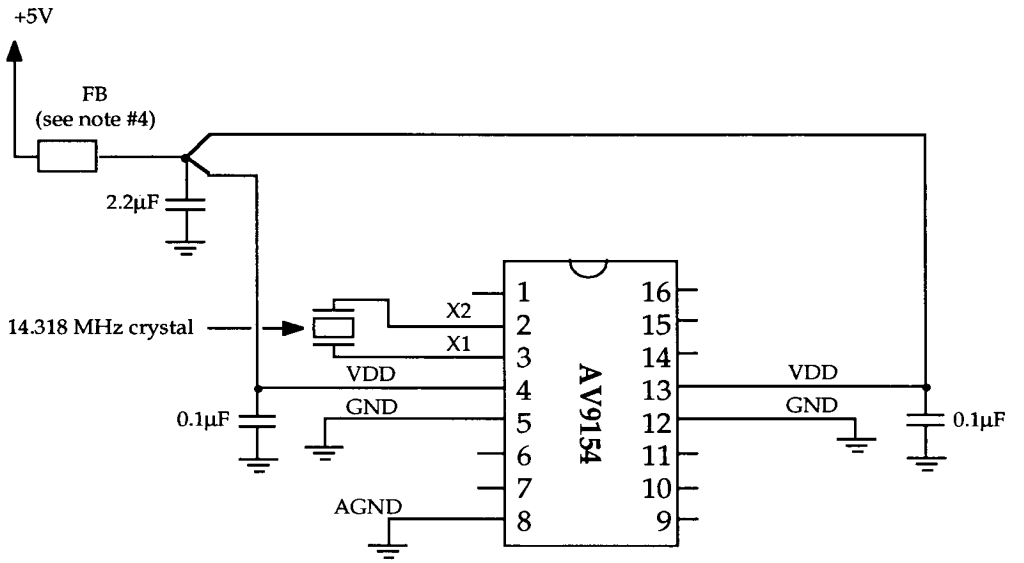
Electrical Characteristics at 3.3V

(Operating V_{DD} = +2.7V to +3.7V, T_A = 0°C to 70°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
DC Characteristics						
V_{IL}	Input Low Voltage	-	-	$0.15V_{DD}$	V	
V_{IH}	Input High Voltage	$0.7V_{DD}$	-	-	V	
I_{IL}	Input Low Current	-5	-	5	µA	V_{IN} = 0V
I_{IH}	Input High Current	-5	-	5	µA	V_{IN} = V_{DD}
V_{OL}	Output Low Voltage	-	-	0.1	V	I_{OL} = 8mA
V_{OH}	Output High Voltage	V_{DD}-.1V	-	-	V	I_{OH} = -4mA
I_{DD}	Supply Current	-	15		mA	Note 1
F_d	Output Frequency Change over Supply and Temperature	-	0.002	0.01	%	With respect to typical frequency
C_i	Input Capacitance			10	pF	Except X1, X2
C_L	Load Capacitance		20		pF	Pins X1, X2
$I_{DDSTDBY}$	Supply Current, Standby		15		µA	When powered down
I_{sc}	Short Circuit Current		30		mA	
AC Characteristics						
t_w	Enable pulse width	20	-	-	ns	
t_{su}	Setup time data to enable	20	-	-	ns	
$ICLK_r$	Input Clock Rise time	-	-	20	ns	
$ICLK_f$	Input Clock Fall time	-	-	20	ns	
t_{hd}	Hold time data to enable	10	-	-	ns	
t_r	Rise time	-	-	4	ns	15 pf load
t_f	Fall time	-	-	4	ns	15 pf load
d_t	Duty cycle	40	48/52	60	%	15 pf load
T_{jis}	Jitter, 1 sigma		±0.5	±2	%	All frequencies
T_{jabs}	Jitter, absolute		±3	±5	%	All frequencies
t_{ft}	Frequency Transition time			20	ms	From 2 to 25 MHz
t_{pu}	Power up time		15		ms	From off to 50 MHz
f_o	Output Frequency	2		50	MHz	
f_i	Input Frequency	2	14.318	32	MHz	

Note 1: AV9154 with no load, with 14.318 MHz crystal input, and CLK1 running at 40 MHz. Power supply current varies with frequency. Consult ICS for actual current at different frequencies.

AV9154
Recommended External Circuit



Notes:

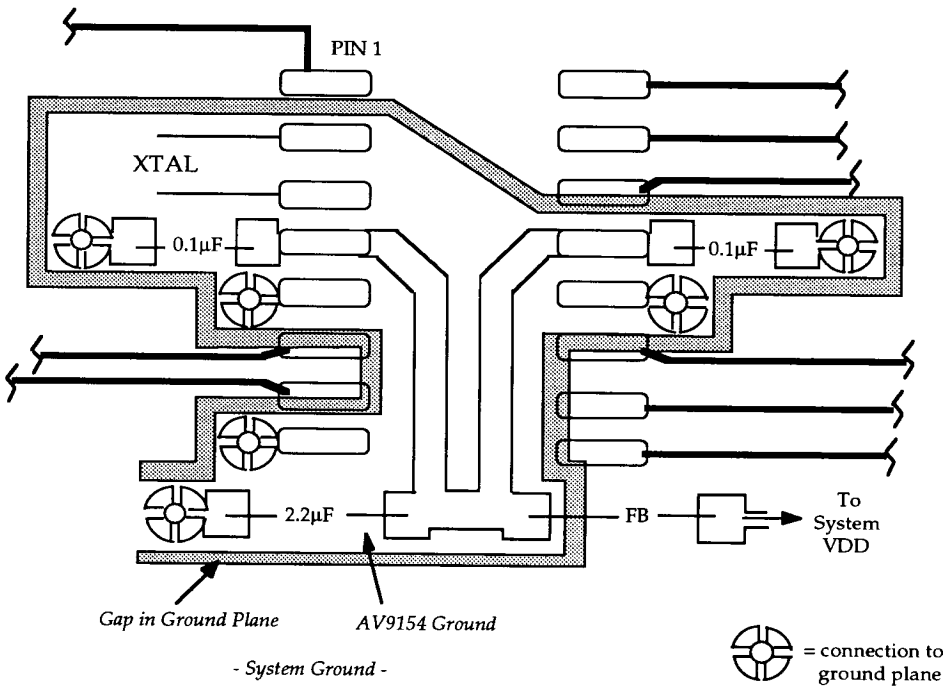
1. Avasem recommends the use of an isolated ground plane for the AV9154. All grounds shown on this drawing should be connected to this ground plane. This ground plane should be connected to the system ground plane at a single point. Please refer to AV9154 Board Layout diagram.

2. A single power supply connection for all VDD lines at the 2.2 µF decoupling capacitor is recommended to reduce interaction of analog and digital circuits. The 0.1 µF decoupling capacitors should be located as close to each VDD pin as possible.

3. A 33 Ω series termination resistor should be used on any clock output which drives more than one load or drives a long trace (more than about 2 inches), especially when using high frequencies (>50 MHz). This termination resistor is put in series with the clock output line close to the clock output. It helps improve jitter perfomance and reduce EMI by damping standing waves caused by impedance mismatches in the output clock circuit trace.

4. The ferrite bead does not enhance the performance of the AV9154, but will reduce EMI radiation from the VDD line.

AV9154 Recommended Board Layout



This is the recommended layout for the AV9154 to maximize clock performance. Shown are the power and ground connections, the ground plane, and the input/output traces.

Use of the isolated ground plane and power connection, as shown, will prevent stray high frequency ground and system noise from propagating through the device. When compared to using the system ground and power planes, this technique will minimize output clock jitter. The isolated ground plane should be connected to the system ground plane at one point, near the 2.2µF decoupling cap. For lowest jitter performance, this isolated ground plane should be kept away from clock output pins and traces. Keeping the isolated ground plane area as small as possible will minimize EMI radiation. Use a sufficient gap between the isolated ground plane and system ground plane to prevent AC coupling. The ferrite bead in the VDD line optional, but will help reduce EMI.

The traces to distribute the output clocks should be over a system ground or power supply plane. The trace width should be about two times the thickness of the PC board between the trace and the underlying plane. These guidelines help minimize clock jitter and EMI radiation. The traces to distribute power should be as wide as possible.

Ordering Information

Part Number	Temperature Range	Package Type
AV9154-xxCN16	0°C to +70°C	16 lead Plastic DIP
AV9154-xxCS16	0°C to +70°C	16 lead 150 mil wide SOIC

Note: The dash number following AV9154, (denoted by xx above) must be included when ordering product, since it specifies the options being ordered.

Part Marking

ICS
AV9154-xxCx16
Date code/Lot code