

REALTEK SINGLE CHIP

5-PORT 10/100 MBPS SWITCH CONTROLLER

RTL8305SB

1. Features.....	2	7.2 Physical Layer Functional Overview	39
2. General Description	3	7.2.1 Auto-Negotiation for UTP	39
3. Block Diagram.....	4	7.2.2 10Base-T Transmit Function	39
4. Pin Assignments	5	7.2.3 10Base-T Receive Function	39
5. Pin Descriptions.....	7	7.2.4 Link Monitor.....	39
5.1 Media Connection Pins	7	7.2.5 100Base-TX Transmit Function.....	39
5.2 Configuration Pins	7	7.2.6 100Base-TX Receive Function	39
5.3 Port4 External MAC Interface Pins.....	8	7.2.7 100Base-FX	39
5.4 Miscellaneous Pins	13	7.2.8 100Base-FX Transmit Function.....	40
5.5 Per Port LED Pins	14	7.2.9 100Base-FX Receive Function	40
5.6 Power Pins.....	15	7.2.10 100Base-FX Far-End-Fault-Indication (FEFI) 40	
5.7 Reserved Pins.....	16	7.2.11 Reduced Fiber Interface	40
5.8 Serial EEPROM and SMI Pins.....	16	7.2.12 Power Saving Mode.....	40
5.9 Strapping Pins	17	7.2.13 Reg0.11 Power Down Mode	40
5.10 Port Status Strapping Pins	19	7.2.14 Crossover Detection and Auto Correction	41
6. Register Description.....	21	7.2.15 Polarity Detection and Correction.....	41
6.1 PHY0 to 4: PHY Register of Each Port.....	22	7.3 Advanced Functional Overview	42
6.1.1 Register0: Control Register	22	7.3.1 Reset	42
6.1.2 Register1: Status Register.....	23	7.3.2 Setup and Configuration	42
6.1.3 Register4: Auto-Negotiation Advertisement Register.....	23	7.3.3 Example of Serial EEPROM: 24LC02	43
6.1.4 Register5: Auto-Negotiation Link Partner Ability Register	24	7.3.4 24LC02 Device Operation	43
6.1.5 Register6: Auto-Negotiation Expansion Register	24	7.3.5 SMI	44
6.2 PHY0: EEPROM Register0	25	7.3.6 Head-Of-Line Blocking	44
6.2.1 Register16: EEPROM Byte0 and 1 Register	25	7.3.7 802.1Q Port Based VLAN	44
6.2.2 Register17: EEPROM Byte2 and 3 Register	25	7.3.8 QoS Function.....	46
6.2.3 Register18~20: EEPROM EthernetID Register.....	25	7.3.9 Insert/Remove VLAN Priority Tag.....	46
6.2.4 Register21: EEPROM Byte10 and 11 Register	26	7.3.10 Filtering/Forwarding Reserved Control Frame.....	47
6.2.5 Register22: EEPROM Byte12 and 13 Register	26	7.3.11 Broadcast Storm Control.....	47
6.3 PHY1: EEPROM Register1	27	7.3.12 Broadcast In/Out Drop	47
6.3.1 Register16~23: EEPROM (Byte 14~29) Register.....	27	7.3.13 Loop Detection	48
6.3.2 Register24~31: EEPROM VLAN(Byte 30~44) Register	27	7.3.14 MAC Loopback return to External	49
6.4 PHY2: Pin & EEPROM Register	28	7.3.15 Reg0.14 PHY Loopback return to Internal	50
6.4.1 Register16: Pin Register	28	7.3.16 LED	50
6.4.2 Register17: Pin & EEPROM Register for VLAN.....	29	7.3.17 2.5V Power Generation.....	52
6.5 PHY3: Port Control Register.....	30	7.3.18 Crystal/Oscillator	52
6.5.1 Register16: Port Control Register.....	30	8. Serial EEPROM Description.....	53
6.5.2 Register17: EEPROM (Byte 46) Register	31	9. Electrical Characteristics	57
6.5.3 Register18~20: EEPROM (Byte 47~52) Register.....	31	9.1 Absolute Maximum Ratings:.....	57
7. Functional Description	32	9.2 Operating Range:.....	57
7.1 Switch Core Functional Overview	32	9.3 DC Characteristics.....	57
7.1.1 Application	32	9.4 AC Characteristics.....	58
7.1.2 Port4	32	9.5 Digital Timing Characteristics.....	59
7.1.3 Port Status Configuration	36	9.6 Thermal Data.....	59
7.1.4 Enable Port	36	10. Application Information	60
7.1.5 Flow Control.....	37	10.1 UTP (10Base-T/100Base-TX) Application	60
7.1.6 Address Search, Learning and Aging	38	10.2 100Base-FX Application:.....	62
7.1.7 Address Direct Mapping Mode.....	38	11. System Application Diagram.....	63
7.1.8 Half Duplex Operation	38	12. Design and Layout Guide	64
7.1.9 Inter-Frame Gap	38	13. Mechanical Dimensions	65
7.1.10 Illegal Frame.....	38		

1. Features

- 5-port integrated switch controller with memory and transceiver for 10Base-T and 100Base-TX with
 - ◆ 5-port 10/100M UTP or
 - ◆ 4-port 10/100M UTP + 1-port MII/SNI
- Supports PHY mode MII /SNI for router applications and MAC mode MII for HomePNA or VDSL solutions
- All ports support 100Base-FX with optional flow control enable/disable and full/half duplex setting
- Non-blocking wire-speed reception and transmission and non-head-of-line-blocking forwarding
- Fully compliant with IEEE 802.3/802.3u auto-negotiation function
- Built-in high efficiency SRAM for packet buffer and 1K entry look-up table, and 16 entry CAM
- Supports broadcast storm filtering function
- Supports IEEE802.3x full duplex flow control and back pressure half duplex flow control
- Supports SMI (Serial Management Interface: MDC/MDIO) for programming and diagnostics
- Supports loop detection function with one LED to indicate the existence of loop
- Supports loopback function for diagnosis
- Flexible 802.1Q Port based VLAN. Up to 5 VLAN
 - ◆ Supports 802.1Q tag VLAN function
 - ◆ Supports ARP VLAN for broadcast packets
 - ◆ Supports Leaky VLAN for unicast packets
- Supports QoS function on each port:
 - ◆ QoS based on: (1) Port-based (2) VLAN tag (3) TCP/IP header's TOS/DS
 - ◆ Supports two level priority queues
 - ◆ Weighted round robin service
- Supports VLAN priority tag Insert/Remove function
- Optional 1536 or 1552 byte maximum packet length
- Supports reserved control frames (DID= 0180C2000003~0180C200000F) filtering function
- Flexible LED indicators for link, activity, speed, full/half duplex and collision
- LEDs blink upon reset for LED diagnostics
- Supports two Power Reduction methods:
 - ◆ Power saving mode by cable detection
 - ◆ Power down mode (by PHY register 0.11)
- Robust baseline wander correction for improved 100BASE-TX performance
- Optional Crossover Detection and Auto Correction function
- Physical layer port Polarity Detection and Correction function
- Optional EEPROM interface for configuration
- 25MHz crystal or OSC input. Single 3.3V power system like by translating of an external transistor
- 0.25 μ m, CMOS technology, 3.3V/2.5V with 3.3V input tolerant, 128 pin PQFP package

2. General Description

The RTL8305SB is a Fast Ethernet switch, which integrates memory, five MACs, and five physical layer transceivers for 10Base-T and 100Base-TX operation into a single chip. All ports support 100Base-FX, which share pins (TX+/-/RX+/-) with UTP ports and need no SD+/- pins, a development using Realtek proprietary technology. Due to the lack of auto-negotiation in 100Base-FX applications, the RTL8305SB can be forced into half or full duplex mode and can enable or disable flow control in fiber mode.

The five ports are separated into 3 groups (GroupX/GroupY/Port4) for flexible port configuration using strapping pins upon reset. The SetGroup pin is used to select port members in GroupX and GroupY. While the port members is determined, you can use mode selection pin (GxMode/Gymode/P4Mode[1:0]) to select operating interfaces such as 10/100Base-TX, 100Base-FX. Each group has 4 pins to select initial port status (ANEG/Force, 100/10, Full/Half, Enable/Disable Flow Control) upon reset. Upon reset, in addition to using strapping pins, the RTL8305SB also can be configured with an EEPROM or read/write operation by a CPU through the MDC/MDIO interface.

The fifth port (port 4) supports an external MAC interface, which can be set to PHY mode MII, PHY mode SNI, or MAC mode MII to work with a routing engine, HomePNA or VDSL transceiver. In order to accomplish diagnostics in complex network systems, the RTL8305SB also provides a loopback feature in each port for a variable CPU system.

The RTL8305SB contains a 1K entry address look-up table and supports a 16 entry CAM to avoid hash collisions and to maintain forwarding performance. The RTL8305SB supports IEEE 802.3x full duplex flow control and back- pressure half duplex flow control. The broadcast storm filtering function is provided to filter unusual broadcast storm issues and has an intelligent switch engine to prevent Head-Of-Line blocking problems.

The RTL8305SB supports 5 groups of VLANs which can be configured with port based VLAN and/or 802.1Q tag VLAN. ARP broadcast and Leaky VLAN are also supported for advanced applications.

The RTL8305SB supports several types of QoS functions with two level priority queues to improve multi-media or real-time networking applications. The QoS functions are based on: 1) Port based priority; 2) 802.1Q VLAN priority tag; 3) The TOS/DS (DiffServ) field of TCP/IP. In order to avoid the flow control function effecting the quality of high priority frames, the RTL8305SB supports an intelligent flow control for high priority frames by setting DisFCAutoOff to automatically turn off flow control for 1~2 seconds whenever the congestion port receives high priority frames. When the QoS function is enabled, a VLAN tag can be inserted or removed at the output port. The RTL8305SB will insert a VLAN priority-tag (VID=0x000) for untagged frames or remove the tag for all tagged frames.

Maximum packet length can be 1536 or 1552 bytes according to the initial configuration (strapping upon reset). The filtering function is supported for the 802.1D specified reserved group MAC addresses (01-80-C2-00-00-03 to 01-80-C2-00-00-0F).

The RTL8305SB provides flexible LED functions for diagnostics, which include: 1) Four combinations of link, activity, speed, duplex and collision which are designed for convenient LED displays, such as bi-color LEDs; 2) Reset blinking; 3) Blinking time selection. The RTL8305SB also provides a loop detection function and alarm, for network existence notification, with an output pin which can be designed as a visual LED or a status input pin for a CPU.

The RTL8305SB implements a power saving mode on a per port basis. One port automatically enters power saving mode 10 seconds after the cable is disconnected from it. The RTL8305SB also implements a power down mode on a per port basis. Users can set MII Reg.0.11 to force the corresponding port to enter the power down mode, which disables all transmit/receive functions, except SMI (MDC/MDIO management interface).

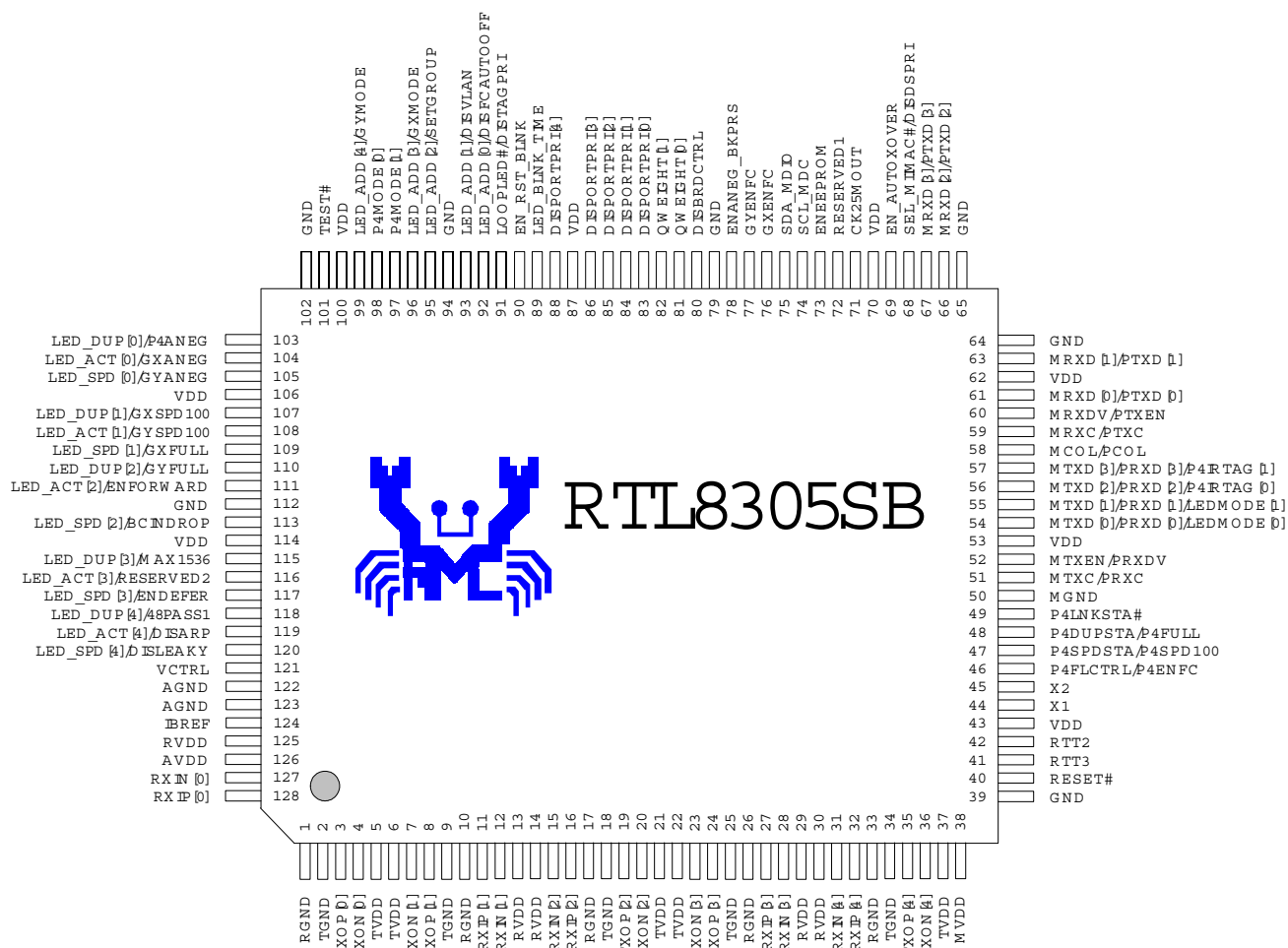
Each physical layer channel of the RTL8305SB consists of a 4B5B encoder/decoder, a Manchester encoder/decoder, a scrambler/descrambler, a transmit output driver, output wave shaping filters, a digital adaptive equalizer, a PLL circuit and a DC restoration circuit for clock/data recovery. Friendly crossover auto detection and correction functions are also supported for easy cable connection.

The integrated chip benefits from low power consumption, advanced functions with flexible configurations for 5-port SOHO switch, Home Gateway, xDSL/Cable router, and other IA applications.

The diagram illustrates the Ethernet MAC and PHY interface architecture. It shows the flow of data and control signals between various components:

- Global functions:** Receives control signals (ENBRDCTRL, ENANEG_BKPRS, RESET#) and provides outputs (X1, X2, CK25MOUT).
- Look-up Table:** Receives data from the MACs and provides output to the Packet Buffer.
- Packet Buffer:** Receives data from the Look-up Table and provides output to the MACs.
- MACs and Switch Engines:** Five MACs (MAC0 to MAC4) are shown, each with a corresponding Switch Engine. They are connected to the Look-up Table and Packet Buffer.
- PHYs:** Each MAC is connected to a PHY (10B based-T or 100B based-T PHY coeiver).
- Waveform Shaping:** Receives IBREF and provides output to the PHYs.
- Interface:** Receives TXC/RXC, TXEN/RXD, TXD/RXD, RXC/TXC, RXDV/TXEN, RXD/TXD, and COL signals. It is connected to the MACs and PHYs.
- LED controlle:** Receives SEL_MIIMAC, EN_RST_BLNK, LED_BLNK_TIME, LED_SPD[4:0], LED_ACT[4:0], LED_DUP[4:0], and LED_ADD[4:0] signals.
- Other signals:** P4MODE[1:0] is connected to the PHYs.

4. Pin Assignments



'I' stands for inputs; 'O' stands for outputs; 'A' stands for analog; 'D' stands for digital

NAME	PIN No.	TYPE	NAME	PIN No.	TYPE
RGND	1	AGND	GND	65	DGND
TGND	2	AGND	MRXD[2]/PTXD[2]	66	I
TXOP[0]	3	AO	MRXD[3]/PTXD[3]	67	I
TXON[0]	4	AO	SEL_MIIMAC#/DISDSPRI	68	I/O
TVDD	5	AVDD	EN_AUTOXOVER	69	I
TVDD	6	AVDD	VDD	70	DVDD
TXON[1]	7	AO	CK25MOUT	71	O
TXOP[1]	8	AO	RESERVED1	72	I/O
TGND	9	AGND	ENEEPROM	73	I
RGND	10	AGND	SCL_MDC	74	I/O
RXIP[1]	11	AI	SDA_MDIO	75	I/O
RXIN[1]	12	AI	GXENFC	76	I
RVDD	13	AVDD	GYENFC	77	I
RVDD	14	AVDD	ENANEG_BKPRS	78	I
RXIN[2]	15	AI	GND	79	DGND
RXIP[2]	16	AI	DISBRDCTRL	80	I
RGND	17	AGND	QWEIGHT[0]	81	I
TGND	18	AGND	QWEIGHT[1]	82	I
TXOP[2]	19	AO	DISPORTPRI[0]	83	I
TXON[2]	20	AO	DISPORTPRI[1]	84	I
TVDD	21	AVDD	DISPORTPRI[2]	85	I
TVDD	22	AVDD	DISPORTPRI[3]	86	I
TXON[3]	23	AO	VDD	87	DVDD
TXOP[3]	24	AO	DISPORTPRI[4]	88	I
TGND	25	AGND	LED_BLNK_TIME	89	I
RGND	26	AGND	EN_RST_BLNK	90	I
RXIP[3]	27	AI	LOOPLD#/DISTAGPRI	91	I/O
RXIN[3]	28	AI	LED_ADD[0]/DISFCAUTOOFF	92	I/O
RVDD	29	AVDD	LED_ADD[1]/DISVLAN	93	I/O
RVDD	30	AVDD	GND	94	DGND
RXIN[4]	31	AI	LED_ADD[2]/SETGROUP	95	I/O
RXIP[4]	32	AI	LED_ADD[3]/GXMODE	96	I/O
RGND	33	AGND	P4MODE[1]	97	I
TGND	34	AGND	P4MODE[0]	98	I
TXOP[4]	35	AO	LED_ADD[4]/GYMODE	99	I/O
TXON[4]	36	AO	VDD	100	DVDD
TVDD	37	AVDD	TEST#	101	I/O
MVDD	38	DVDD	GND	102	DGND
GND	39	DGND	LED_DUP[0]/P4ANEG	103	I/O
RESET#	40	I	LED_ACT[0]/GXANEG	104	I/O
RTT3	41	O	LED_SPD[0]/GYANEG	105	I/O
RTT2	42	O	VDD	106	DVDD
VDD	43	DVDD	LED_DUP[1]/GXSPD100	107	I/O
X1	44	I	LED_ACT[1]/GYSPD100	108	I/O
X2	45	O	LED_SPD[1]/GXFULL	109	I/O
P4FLCTRL/P4ENFC	46	I	LED_DUP[2]/GYFULL	110	I/O
P4SPDSTA/P4SPD100	47	I	LED_ACT[2]/ENFORWARD	111	I/O
P4DUPSTA/P4FULL	48	I	GND	112	GND
P4LNKSTA#	49	I	LED_SPD[2]/BCINDROP	113	I/O
MGND	50	DGND	VDD	114	DVDD
MTXC/PRXC	51	I/O	LED_DUP[3]/MAX1536	115	I/O
MTXEN/PRXDV	52	O	LED_ACT[3]/RESERVED2	116	I/O
VDD	53	DVDD	LED_SPD[3]/ENDEFER	117	I/O
MTXD[0]/PRXD[0]/LEDMODE[0]	54	I/O	LED_DUP[4]/48PASS1	118	I/O
MTXD[1]/PRXD[1]/LEDMODE[1]	55	I/O	LED_ACT[4]/DISARP	119	I/O
MTXD[2]/PRXD[2]/P4IRTAG[0]	56	I/O	LED_SPD[4]/DISLEAKY	120	I/O
MTXD[3]/PRXD[3]/P4IRTAG[1]	57	I/O	VCTRL	121	O
MCOL/PCOL	58	I/O	AGND	122	AGND
MRXC/PTXC	59	I/O	AGND	123	AGND
MRXDV/PTXEN	60	I	IBREF	124	A
MRXD[0]/PTXD[0]	61	I	RVDD	125	AVDD
VDD	62	DVDD	AVDD	126	AVDD
MRXD[1]/PTXD[1]	63	I	RXIN[0]	127	AI
GND	64	DGND	RXIP[0]	128	AI

5. Pin Descriptions

'I' stands for inputs; 'O' stands for outputs; 'A' stands for analog; 'D' stands for digital

Upon reset: defined as a short time after at the end of a hardware reset. **After reset:** defined as the time after the specified "Upon Reset" time.

5.1 Media Connection Pins

Pin Name	Pin No.	Type	Description	Default
RXIP[4:0] RXIN[4:0]	11,12,15, 16,27,28, 31,32 127,128	AI	Differential Receive Data Input: Shared by 100Base-TX, 10Base-T and 100Base-FX. UTP or FX depends on pin GxMode/GyMode/P4Mode[1:0]. Note: The 8305SB uses these pins for UTP and Fiber. The 8305S uses these pins for UTP only.	
TXOP[4:0] TXON[4:0]	3,4 7,8 19,20 23,24 35,36	AO	Differential Transmit Data Output: Shared by 100Base-TX, 10Base-T and 100Base-FX. UTP or FX depends on pin GxMode/GyMode/P4Mode[1:0]. Note: The 8305SB uses these pins for UTP and Fiber. The 8305S uses these pins for UTP only.	

5.2 Configuration Pins

Pin Name	Pin No.	Type	Description	Default
ENANEG_BKPRS	78	I	Enable Auto-Negotiation Back Pressure: This pin sets back pressure for auto-negotiation mode for all UTP ports. 1: Enable 0: Disable 8305SB=ENANEG_BKPRS, 8305S=ENBKPRS. This pin has the same function for both the RTL8305SB and RTL8305S. The RTL8305SB also supports Force mode (through P4ENFC/GxENFC/GyENFC), but this pin is used only for Auto-Negotiation mode. The pin name is changed to differentiate between "Enable back pressure for Auto-Negotiation mode" and "Enable backpressure for Force mode."	1
DISBRDCTRL	80	I	Disable Broadcast Storm Control: 1= Disable 0= Enable 8305SB=DISBRDCTRL, 8305S=ENBRDCTRL. The RTL8305SB will disable this function when pin DISBRDCTRL is left floating. However, the RTL8305S will enable this function when pin ENBRDCTRL is left floating.	1
LED_BLNK_TIME	89	I	LED Blink Time: This pin selects the blinking speed of the activity and collision LEDs. 1: On 43ms, then Off 43ms 0: On 120ms, then Off 120ms	1
EN_RST_BLNK	90	I	Enable Reset Blink: This pin enables the blinking of the LEDs upon reset for diagnosis purposes. 1: Enable reset LED blinking 0: Disable reset LED blinking 8305SB=EN_RST_BLNK, 8305S=DIS_RST_BLNK#. This pin has the same function for both the RTL8305SB and RTL8305S. The pin name has been changed for convenience.	1

5.3 Port4 External MAC Interface Pins

The external device should be 2.5V compatible, because the digital output of the RTL8305SB is 2.5V. The input or input/output pins listed below do not have internal pull-high resistors for connecting to external devices. External pull-high resistors are recommended for those floating input pins without internal pull-high resistor if reduced power consumption is desired.

In order to differentiate between MAC and PHY mode, the name of the pins change for PHY mode. For example: RTL8305SB=MRXD[0]/PTXD[0], RTL8305S=MRXD[0]/MTXD[0].

Tip: Connect the input of Port4 to the output of the external device.

Pin Name	Pin No.	Type	Description	Default
MRXD[3:0]/PTXD[3:0]	67,66,63,61	I	For MAC mode MII, these pins are MRXD[3:0], MII receive data nibble. For PHY mode MII, these pins are PTXD[3:0], MII transmit data nibble. For PHY mode SNI, PTXD[0] is serial transmit data. Because this pin can be connected to a 2.5V or 3.3V devices, these pins have no internal pull-high resistor. RTL8305SB = MRXD[3:0] / PTXD[3:0], RTL8305S = MRXD[3:0] / MTXD[3:0]. In order to differentiate between MAC and PHY modes, the RTL8305SB changes the pin name for PHY mode.	
MRXDV/PTXEN	60	I	For MAC mode MII, this pin represents MRXDV, MII receive data valid. For PHY mode MII, this pin represents PTXEN, MII transmit enable. For PHY mode SNI, this pin represents PTXEN, transmit enable. Because this pin can be connected to a 2.5V or 3.3V device, this pin has no internal pull-high resistor. RTL8305SB = MRXDV/PTXEN, RTL8305S = MRXDV/MTXEN. In order to differentiate between MAC and PHY mode, the RTL8305SB changes the pin name for PHY mode.	
MRXC/PTXC	59	I/O	For MAC mode MII, it is receive clock, MRXC (acts as input). For PHY mode MII/PHY mode SNI, it is transmit clock, PTXC (acts as output). Because this pin can be connected to a 2.5V or 3.3V device, this pin has no internal pull-high resistor. RTL8305SB = MRXC/PTXC, RTL8305S = MRXC/MTXC. In order to differentiate between MAC and PHY mode, the RTL8305SB changes the pin name for PHY mode.	
MCOL/PCOL	58	I/O	For MAC mode MII, this pin represents MCOL collision (acts as input) For PHY mode MII/PHY mode SNI, this pin represents PCOL collision (acts as output) Because this pin can be connected to a 2.5V or 3.3V device, this pin has no internal pull-high resistor. RTL8305SB = MCOL/PCOL, RTL8305S = MCOL. In order to differentiate between MAC and PHY mode, the RTL8305SB changes the pin name for PHY mode.	

Cont...

MTXD[3]/ PRXD[3]/ P4IRTag[1]	57	I/O	Output after reset: For MAC mode MII (P4Mode[1:0]=11), these pins are MTXD[3:0], MII transmit data of MAC . For PHY mode MII (P4Mode[1:0]=01), these pins are PRXD[3:0], MII receive data of PHY . For PHY mode SNI (P4Mode[1:0]=00), PRXD[0] is SNI serial receive data . Input upon reset: P4IRTag[1:0] Insert/Remove Priority Tag of Port4. 11: Do not insert/remove Tag from Output High and Low Queue of Port4. 10: Insert Tag from Output High and Low Queue of Port4. 01: Insert Tag from Output High Queue only of Port4. 00: Remove Tag from Output High and Low Queue of Port4. RTL8305SB = MTXD[3:2]/PRXD[3:2]/P4IRTag[1:0], RTL8305S = MTXD[3:2]/MRXD[3:2]. In order to differentiate between MAC and PHY mode, the RTL8305SB changes the pin name for PHY mode. For RTL8305SB: These pins are input pins used for strapping upon reset and used as output pins (output data) after reset. For RTL8305S: These pins are used as output pins (output data) after reset. These pins are used for Port4 only. Use serial EEPROM for other ports.	11
MTXD[2]/ PRXD[2]/ P4IRTag[0]	56			
MTXD[1]/PRXD[1]/ LEDMode[1]	55	I/O	Output after reset: For MAC mode MII (P4Mode[1:0]=11), these pins are MTXD[3:0], MII transmit data of MAC . For PHY mode MII (P4Mode[1:0]=01), these pins are PRXD[3:0], MII receive data of PHY . For PHY mode SNI (P4Mode[1:0]=00), PRXD[0] is SNI serial receive data . Input upon reset: LEDMode[1:0] Each port has four LED indicator pins. Each pin may has different indicator meaning set by pins LEDMode[1:0]. LEDMode[1:0]=11 : Speed + Link/Act + Duplex/Col + Link/Act/Spd. LEDMode[1:0]=10 : Speed + Act + Duplex/Col + Bi-color Link/Active. LEDMode[1:0]=01 : Speed + RxAct + TxAct + Link. LEDMode[1:0]=00 : Speed + Link/Act + Col + Duplex. All LED statuses are represented as active-low or high depending on input strapping, except Bi-color Link/Act in Bi-color LED mode, whose polarity depends on Spd status. Link/Act/Spd: Link, Activity, and Speed Indicator. On for link established. Blinking every 43ms when the corresponding port is transmitting or receiving in 100Mb/s. Blinking every 120ms when the port is transmitting or receiving in 10Mb/s. RTL8305SB = MTXD[1:0]/PRXD[1:0]/LEDMode[1:0], RTL8305S = MTXD[1:0]/MRXD[1:0]. In order to differentiate between MAC and PHY mode, the RTL8305SB changes the pin name for PHY mode. For RTL8305SB: These pins are input pins used for strapping upon reset and used as output pins (output data) after reset. For RTL8305S: These pins are used as output pins (output data) after reset.	11
MTXD[0]/PRXD[0]/ LEDMode[0]	54			

Cont...

MTXEN/PRXDV	52	O	For MAC mode MII, this pin represents MTXEN, MII transmit enable. For PHY mode MII, this pin represents PRXDV, MII received data valid. For PHY mode SNI, this pin represents PRXDV, received data valid. RTL8305SB = MTXEN/PRXDV, RTL8305S = MTXEN/MRXDV. In order to differentiate between MAC and PHY mode, the RTL8305SB changes the pin name for PHY mode.	1
MTXC/PRXC	51	I/O	For MAC mode MII, it is transmit clock, MTXC (acts as input). For PHY mode MII/PHY mode SNI, it is receive clock, PRXC (acts as output). Because this pin can be connected to a 2.5V or 3.3V device, this pin has no internal pull-high resistor. RTL8305SB = MTXC/PRXC, RTL8305S = MTXC/MRXC. In order to differentiate between MAC and PHY mode, the RTL8305SB changes the pin name for PHY mode.	
P4MODE[1:0]	97,98	I	Select Port 4 operating mode: 11: UTP / MAC mode MII 10: 100Base-FX mode 01: PHY mode MII 00: PHY mode SNI The RTL8305SB has 4 options and the RTL8305S has 3 options.	11
P4LNKSTA#	49	I	Port4 Link Status for MAC: When the PHY part of Port4 is not used, this pin determines the link status of the Port4 MAC in real-time. That is link status of real-time for MII MAC/MII PHY/SNI PHY only. This pin is low active. 1: No Link. 0: Link When P4MODE[1:0]=11 (UTP/MAC mode MII), this pin determines the link status of MAC mode MII only in real time. The link status of UTP mode is provided by the internal PHY in real time. If both UTP and MII port are linked OK, UTP has higher priority. When P4MODE[1:0]=10 (100Base-FX mode), this pin does nothing. The internal PHY will provide the link status to the MAC in real time. When P4MODE[1:0]=01 (PHY mode MII), this pin determines the link status of Port4 in real time. When P4MODE[1:0]=00 (PHY mode SNI), this pin determines the link status of Port4 in real time. This pin should be left floating in UTP or FX mode, and pulled down in the other three modes. In MAC mode MII/ PHY mode MII/ PHY mode SNI, configuration of this pin will not set the link status of the internal register. The link status depends on the external PHY or MAC.	1

Cont...

P4DUPSTA/ P4FULL	48	I	<p>Port4 Duplex Status: Port4 initial configuration pin for Duplex upon reset for PHY of UTP or FX mode and Duplex Status for MAC of other mode in real time after reset.</p> <p>1: Full duplex 0: Half duplex</p> <p>When P4MODE[1:0]=11 (UTP/MAC mode MII), this pin provides the initial duplex configuration for the PHY part upon reset (UTP) then determines the duplex status of MAC mode MII in real time after reset. The duplex status of the PHY part (UTP) is provided by the internal PHY in real time after reset.</p> <p>When P4MODE[1:0]=10 (100Base-FX mode), this pin provides the initial register configuration of duplex for PHY part upon reset (FX). The duplex status of the PHY part (FX) is provided by the internal PHY in real time after reset.</p> <p>When P4MODE[1:0]=01 (PHY mode MII), this pin determines the duplex status of Port4 in real time after reset.</p> <p>When P4MODE[1:0]=00 (PHY mode SNI), this pin determines the duplex status of Port4 in real time after reset.</p> <p>8305SB = P4DUPSTA/P4FULL, 8305S = P4DUPSTA#.</p> <p>In order to provide Full duplex as the default value for the PHY, this pin is changed as high active.</p> <p>In 100Base-Fx/ MAC mode MII/ PHY mode MII/ PHY mode SNI, the configuration of this pin after reset will not set the link status of the internal register. The link status depends on the external PHY or MAC.</p>	1
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P4SPDSTA/ P4SPD100	47	I	<p>Port4 Speed Status: Port4 initial configuration pin for Speed upon reset for PHY of UTP mode only and Speed Status for MAC of other mode in real time after reset.</p> <p>1: 100Mbps 0: 10Mbps</p> <p>When P4MODE[1:0]=11 (UTP/MAC mode MII), this pin provides the initial configuration of speed for the PHY part upon reset (UTP) then determines speed status of MAC mode MII in real time after reset. The speed status of the PHY part (UTP) is provided by the internal PHY in real time after reset.</p> <p>When P4MODE[1:0]=10 (100Base-FX mode), speed is dedicated to 100M. This pin does nothing and should be left floating.</p> <p>When P4MODE[1:0]=01 (PHY mode MII), this pin determines the duplex status of Port4 in real time after reset.</p> <p>When P4MODE[1:0]=00 (PHY mode SNI), speed is dedicated to 10MHz clock rate. This pin should be pulled down.</p> <p>For the application listed below, this pin should be left floating: For P4MODE[1:0]=10 (100Base-FX mode).</p> <p>For the application listed below, this pin should be pulled down: For PHY mode SNI, speed is dedicated to 10MHz clock rate.</p> <p>8305SB = P4SPDSTA/P4SPD100, 8305S = P4SPDSTA#.</p> <p>In order to provide 100M for the default value for PHY, this pin is changed as high active.</p>	1
P4FLCTRL/ P4EnFC	46	I	<p>Port4 Flow Control: Port4 initial configuration pin for Flow Control upon reset for PHY of UTP and FX mode and Flow Control Status for MAC of other mode in real time after reset.</p> <p>1=Enable Flow Control ability. 0=Disable Flow Control ability.</p> <p>When P4MODE[1:0]=11 (UTP/MAC mode MII), this pin provides the initial configuration of flow control for the PHY part upon reset (UTP) then determines the flow control status of MAC mode MII in real time after reset. The flow control status of PHY part (UTP) is provided by the internal PHY in real time after reset.</p> <p>When P4MODE[1:0]=10 (100Base-FX mode), this pin provides the initial configuration of flow control for the PHY part upon reset (FX).</p> <p>When P4MODE[1:0]=01 (PHY mode MII), this pin determines the duplex status of Port4 in real time after reset.</p> <p>When P4MODE[1:0]=00 (PHY mode SNI), flow control should be disabled. This pin should be pulled down.</p> <p>8305SB = P4FLCTRL/P4EnFC, 8305S = P4FLCTRL#.</p> <p>In order to enable flow control ability for the PHY, this pin is changed as high active.</p>	1

Cont...

SEL_MIIMAC#/ DisDSPri	68	I/O	<p>Output after reset = SEL_MIIMAC# used for LED: When P4MODE[1:0]=11, this pin indicates whether the UTP path or the MII MAC path is selected. Otherwise, this pin is of no use.</p> <p>The LED statuses are represented as active-low or high depending on input strapping. => If Input=1: Output 0= MII MAC port is selected. 1= UTP is selected. => If Input=0: Output 1= MII MAC port is selected. 0= UTP is selected.</p> <p>While P4MODE[1:0]=11, RTL8305S supports UTP/II MAC auto-detection function via the link status of Port4 UTP and the status of pin P4LNKSTA# and MAC mode MII. UTP has higher priority over the MAC mode MII.</p> <p>Input upon reset = DisDSPri. Disable Differentiated Service Priority. 1: Disable DS priority; 0: Enable DS priority 8305SB = SEL_MIIMAC#/DisDSPri, 8305S = SEL_MIIMAC#.</p>	1
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5.4 Miscellaneous Pins

Pin Name	Pin No.	Type	Description	Default
X1	44	I	25MHz crystal or oscillator clock input. The clock tolerance is +/-50ppm.	
X2	45	O	To crystal input, when using an oscillator, this pin should be floating.	
CK25MOUT	71	O	<p>25MHz clock output. The source of this output is clock from X1 and X2. This pin is used to support an extra 25M clock for the external device (for example: HomePNA PHY).</p> <p>The output voltage of the RTL8305SB is 2.5V. The output voltage of the RTL8305S is 3.3V.</p>	
RESET#	40	I	<p>Active low reset signal: To complete reset function, this pin must be asserted for at least 10ms. After reset, about 30ms is needed for the RTL8305SB to complete internal test functions and initialization.</p> <p>This pin is a Schmitt input.</p> <p>Because this pin can be connected to a 2.5V or 3.3V device, this pin has no internal pull-high resistor.</p>	
IBREF	124	A	Control transmit output waveform Vpp: This pin should be grounded through a 1.96KΩ resistor.	
VCtrl	121	O	<p>Voltage control to external regulator: This signal controls a power PNP transistor to generate the 2.5V power supply.</p> <p>8305SB = VCtrl, 8305S = TEST#.</p>	
RTT3	41	O	<p>Cap+ for future use: Reserve capacitors in layout for future use, but do not use those capacitors in the BOM.</p> <p>8305SB = RTT3, 8305S = TESTCLK.</p>	
RTT2	42	O	<p>Cap- for future use: Reserve capacitors in layout for future use, but do not use those capacitors in the BOM.</p> <p>8305SB = RTT2, 8305S = TESTDATA.</p>	
TEST#	101	I/O	Reserved pin for internal use. Should be left floating.	1

5.5 Per Port LED Pins

Each port has four LED indicator pins. Each pin may have different indicator meanings as set by pins LEDMode[1:0].

All LED statuses are represented as active-low or high depending on input strapping, except Bi-color Link/Act in Bi-color LED mode, whose polarity depends on Spd status.

Those pins which are dual function pins are output for LED or input for strapping. Below are LED descriptions only.

Pin Name	Pin No.	Type	Description	Default
LED_SPD[4:0]/...	120, 117, 113, 109, 105	I/O	Output after reset = used for 1st LED: LEDMode[1:0]=11 -> Speed (On=100, Off=10) LEDMode[1:0]=10 -> Speed (On=100, Off=10) LEDMode[1:0]=01 -> Speed (On=100, Off=10) LEDMode[1:0]=00 -> Speed (On=100, Off=10) Input upon reset = ... Refer below for each pin.	1111
LED_ACT[4:0]/...	119, 116, 111, 108, 104	I/O	Output after reset = used for 2nd LED: LEDMode[1:0]=11 -> Link/Act: (On=Link, Off=no Link, Flash=Tx or Rx activity) LEDMode[1:0]=10 -> Act: (Off=no activity, ON=Tx or Rx activity) LEDMode[1:0]=01 -> RxAct: (Off=no activity, ON=Rx activity) LEDMode[1:0]=00 -> Link/Act: (On=Link, Off=no Link, Flash=Tx or Rx activity) Input upon reset = ... Refer below for each pin.	1111
LED_DUP[4:0]/...	118, 115, 110, 107, 103	I/O	Output after reset = used for 3rd LED: LEDMode[1:0]=11 -> Duplex/Col: (On=Full, Off=Half with no collision, Flash=Collision) LEDMode[1:0]=10 -> Duplex/Col: (On=Full, Off=Half with no collision, Flash=Collision) LEDMode[1:0]=01 -> TxAct: (Off=no activity, ON=Tx activity) LEDMode[1:0]=00 -> Col: (Off=Half with no collision, ON=Collide) Input upon reset = ... Refer below for each pin.	1111
LED_ADD[4:0]/...	99,96, 95,93, 92	I/O	Output after reset = used for 4th LED: LEDMode[1:0]=11 -> Link/Act/Spd: On for link established. Blinking every 43ms when the corresponding port is transmitting or receiving in 100Mb/s. Blinking every 120ms when the port is transmitting or receiving in 10Mb/s. LEDMode[1:0]=10 -> Bi-color Link/Active: polarity depends on Spd status. See Figure2 and Table1. LEDMode[1:0]=01 -> Link: (On=Link, Off=no Link) LEDMode[1:0]=00 -> Duplex: (On=Full, Off=Half) Input upon reset = ... Refer below for each pin. 8305SB = LED_ADD[4:0]/..., 8305S = NC.	1111

5.6 Power Pins

Pin Name	Pin No.	Type	Description	Default
TVDD	5,6,21, 22,37	P	3.3V Analog Transmit Power	
RVDD	13,14 29,30	P	2.5V Analog Receive Power 8305SB = 2.5V, 8305S = 3.3V.	
AVDD	126	P	3.3V Analog Power 8305SB = 3.3V AVDD, 8305S = 3.3V RVDD.	
RVDD	125	P	2.5V Analog Receive Power 8305SB = 2.5V RVDD, 8305S = 3.3V AVDD.	
MVDD	38	P	2.5V Internal RAM Power 8305SB = 2.5V, 8305S = 3.3V.	
VDD	43,53 62,70 87,100 106,114	P	2.5V Digital Power 8305SB = 2.5V, 8305S = 3.3V.	
RGND	1,10,17, 26,33	P	Analog Ground	
TGND	2,9,18, 25,34	P	Analog Ground	
AGND	122 123	P	Analog GND Pin122 for 8305SB = AGND, 8305S = DGND.	
MGND	50	P	Internal RAM GND Pin50 for 8305SB = MGND, 8305S = GND.	
GND	39,64, 65,79 94,102 112	P	Digital GND Pin64 for 8305SB = GND, 8305S = MGND.	

5.7 Reserved Pins

Pin Name	Pin No.	Type	Description	Default
RESERVED1	72	I/O	Reserved: Reserved pin for internal use. Should be left floating.	1

5.8 Serial EEPROM and SMI Pins

The serial EEPROM and external device should be 2.5V compatible, as the output of the RTL8305SB is 2.5V.

If the external device output is 3.3V. There are 0.7V (3.3V–2.5V) on pull-high resistors which one side is a 3.3V external device and the other side is 2.5V VDD. There are 0.7V (3.3V–2.5V) on pull-high resistors which one side is 3.3V VDD and the other side is the 2.5V output of the RTL8305SB.

Pin Name	Pin No.	Type	Description	Default
EnEEPROM	73	I	Enable EEPROM: This pin sets the RTL8305SB to enable the loading of the serial EEPROM upon reset. 1: Enable 0: Disable 8305SB = EnEEPROM, 8305S = NC.	1
SCL_MDC	74	I/O	SCL or MDC: This pin is tri state when pin RESET#=0. When pin EnEEPROM=1, this pin becomes SCL (output) to load the serial EEPROM upon reset. Then this pin changes as MDC (input) after reset. In this case, this pin should be pulled-high (2.5V) by an external resistor. When pin EnEEPROM=0, this pin is MDC (input): 0 to 25MHz clock, sourced by an external device to sample MDIO. In this case, if, and only if, this pin is floating, it needs an external pull-high (2.5V) resistor. Because this pin can be connected to a 2.5V or 3.3V device, this pin has no internal pull-high resistor. 8305SB = SCL_MDC, 8305S = NC.	
SDA_MDIO	75	IO	SDA or MDIO: This pin is tri state when RESET#=0. When pin EnEEPROM=1, this pin becomes SDA (input/output) to load the serial EEPROM upon reset. Then this pin changes as MDIO (input/output) after reset. When pin EnEEPROM=0, this pin is MDIO (input/output). It should be pulled-high by an external resistor. Because this pin can be connected to a 2.5V or 3.3V device, this pin has no internal pull-high resistor. 8305SB = SDA_MDIO, 8305S = NC.	

5.9 Strapping Pins

Those pins which are dual function pins are output for LED or input for strapping. Below are strapping descriptions only.

Pin Name	Pin No.	Type	Description	Default
EN_AUTOXOVER	69	I	Enable Auto crossover function. 1: Enable auto crossover detection. 0: Disable auto crossover detection. MDI only.	1
QWeight[1] QWeight[0]	82 81	I	Weighted round robin ration of priority queue. The frame service rate of High-pri queue: Low-pri queue 11: 16:1 10: always high priority queue first 01: 8:1 00: 4:1 8305SB = QWeight[1:0], 8305S = NC.	11
DisPortPri[4] DisPortPri[3] DisPortPri[2] DisPortPri[1] DisPortPri[0]	88 86 85 84 83	I	Enable Port based priority QoS function. DisPortPri[4]: 1=Disable port 4 priority. 0=Enable port 4 priority. DisPortPri[3]: 1=Disable port 3 priority. 0=Enable port 3 priority. DisPortPri[2]: 1=Disable port 2 priority. 0=Enable port 2 priority. DisPortPri[1]: 1=Disable port 1 priority. 0=Enable port 1 priority. DisPortPri[0]: 1=Disable port 0 priority. 0=Enable port 0 priority. 8305SB = DisPortPri[4:0], 8305S = NC.	11111
LoopLED# /DisTagPri	91	I/O	Output after reset = LoopLED# used for LED: If the Loop detection function is enabled, this pin indicates whether Network loop is detected or not. Otherwise, this pin is of no use. The LED statuses are represented as active-low or high depending on input strapping. => If Input=1: Ouput 0= Network loop is detected. 1=No loop. => If Input=0: Ouput 1= Network loop is detected. 0= No loop. Input upon reset = Disable 802.1p VLAN Tag priority based QoS function. 1: Disable 0: Enable 8305SB = LoopLED#/DisTagPri, 8305S = EnP4LED. 8305SB moves the EnP4LED option into EEPROM.	1
LED_ADD[0]/ DisFCAutoOff	92	I/O	Output after reset = used for LED: Input upon reset = Disable Auto Turn Off function of Flow Control Ability. 1: Disable 0: Enable. Enable Auto turn off low priority queue's flow control ability 1~2 sec whenever the port received a VLAN-tag or TOS/DS high priority frame. The flow control ability will re-enabled when there is not received and high priority frame during 1~2 sec.	1
LED_ADD[1]/ DISVLAN	93	I/O	Output after reset = used for LED: Input upon reset = Disable VLAN function. 1: Disable VLAN 0: Enable VLAN According to the internal registers	1

Cont...

LED_ACT[2]/ EnForward	111	I/O	Output after reset = used for LED Input upon reset = Enable to forward 802.1D specified reserved group MAC addresses frame. 1: Forward reserved control frames, which DID=01-80-C2-00-00-03 to 01-80-C2-00-00-0F packets. 0: Filter reserved control packets, which DID=01-80-C2-00-00-03 to 01-80-C2-00-00-0F.	1
LED_SPD[2]/ BCInDrop	113	I/O	Output after reset = used for LED Input upon reset = Broadcast Input Drop. 1: Use Broadcast Input drop mechanism. 0: Use Broadcast Output drop mechanism.	1
LED_DUP[3]/ Max1536	115	I/O	Output after reset = used for LED Input upon reset = Maximum Frame Length 1536 Bytes 1: 1536 Bytes 0: 1552 Bytes	1
LED_DUP[4]/ 48pass1	118	I/O	Output after reset = used for LED Input upon reset = Back pressure Mode. 48pass1: 1: 48 pass 1: at most 48 consecutively collision to avoid repeater partition when buffer is full. 0: Continuously collide to avoid packet loss when buffer is full.	111
LED_SPD[3]/ EnDefer	117		EnDefer: 1: Enable Carrier Sense Deferring function for half duplex back pressure. 0: Disable Carrier Sense Deferring function for half duplex back pressure.	
LED_ACT[3]/ RESERVED2	116			
LED_ACT[4]/ DisARP	119	I/O	Output after reset = used for LED: Input upon reset = Disable ARP broadcast to all VLAN. 1: Disable to broadcast the ARP broadcast packet to all VLANs. 0: Enable to broadcast the ARP broadcast packet to all VLANs. ARP broadcast frame: DID is all F.	1
LED_SPD[4]/ DisLeaky	120	I/O	Output after reset = used for LED: Input upon reset = Disable Leaky VLAN. 1: Disable to forward unicast frames to other VLAN. 0: Enable to forward unicast frames to other VLAN. Broadcast and multicast frames adhere to the VLAN configuration.	1

5.10 Port Status Strapping Pins

Those pins which are dual function pins are output for LED or input for strapping. Below are strapping descriptions only.

Pin Name	Pin No.	Type	Description	Default
LED_ADD[2]/ SetGroup	95	I/O	Output after reset = used for LED: Input upon reset = Set group of port 1: 1: Port 0 is group X. Port 1, 2, and 3 are group Y 0: Port 0, and 1 are group X. Port 2, and 3 are group Y	1
LED_ADD[3]/ GxMode	96	I/O	Output after reset = used for LED: Input upon reset = Group X operating mode: 1: UTP mode 0: FX mode	1
LED_ADD[4]/ /GyMode	99	I/O	Output after reset = used for LED: Input upon reset = Group Y operating mode: 1: UTP mode 0: FX mode	1
LED_DUP[0]/ P4ANEG	103	I/O	Output after reset = used for LED: Input upon reset = Port4 Auto-Negotiation ability: 1: Enable auto-negotiation (NWAY mode) 0: Disable auto-negotiation (Force mode) Upon reset, this pin sets Reg.0.12 of Port4. Strap after reset for initial value of Port4 UTP mode only. This pin is not used for Port4 FX, MAC mode MII, PHY mode MII, and PHY mode SNI.	1
LED_ACT[0]/ GxANEG	104	I/O	Output after reset = used for LED: Input upon reset = GroupX Auto-Negotiation ability: 1: Enable auto-negotiation (NWAY mode) 0: Disable auto-negotiation (Force mode) Upon reset, this pin sets Reg.0. 12 of Group X. Strap after reset for initial value of UTP mode only. This pin is not used for FX.	1
LED_SPD[0]/ /GyANEG	105	I/O	Output after reset = used for LED: Input upon reset = GroupY Auto-Negotiation ability: 1: Enable auto-negotiation(NWAY mode) 0: Disable auto-negotiation (Force mode) Upon reset, this pin sets Reg.0. 12 of Group Y. Strap after reset for initial value of UTP mode only. This pin is not used for FX.	1
LED_DUP[1]/ /GxSpd100	107	I/O	Output after reset = used for LED: Input upon reset = GroupX 10Base-T/100Base-TX ability: GxSpd100=1, GxFull=1 => MII Reg0.13=1, 0.8=1, 4.8=1, 4.7=1, 4.6=1, 4.5=1 GxSpd100=1, GxFull=0 => MII Reg0.13=1, 0.8=0, 4.8=0, 4.7=1, 4.6=1, 4.5=1 GxSpd100=0, GxFull=1; => MII Reg0.13=0, 0.8=1, 4.8=0, 4.7=0, 4.6=1, 4.5=1 GxSpd100=0, GxFull=0; => MII Reg0.13=0, 0.8=0, 4.8=0, 4.7=0, 4.6=0, 4.5=1 Upon reset, this pin sets Reg.0.13. In addition, upon reset, this pin and GxFull also sets Reg.4.8/4.7/4.6/4.5. Strap after reset for initial value of Group X UTP mode only. This pin is not used for FX.	1

Cont...

LED_ACT[1]/ GySpd100	108	I/O	Output after reset = used for LED: Input upon reset = GroupY 10Base-T/100Base-TX ability: GySpd100=1, GyFull=1 => MII Reg0.13=1, 0.8=1, 4.8=1, 4.7=1, 4.6=1, 4.5=1 GySpd100=1, GyFull=0 => MII Reg0.13=1, 0.8=0, 4.8=0, 4.7=1, 4.6=1, 4.5=1 GySpd100=0, GyFull=1; => MII Reg0.13=0, 0.8=1, 4.8=0, 4.7=0, 4.6=1, 4.5=1 GySpd100=0, GyFull=0; => MII Reg0.13=0, 0.8=0, 4.8=0, 4.7=0, 4.6=0, 4.5=1 Upon reset, this pin sets Reg.0.13. In addition, upon reset, this pin and GyFull also sets Reg.4.8/4.7/4.6/4.5. Strap after reset for initial value of Group Y UTP mode only. This pin is not used for FX.	1
LED_SPD[1]/GxFu ll	109	I/O	Output after reset = used for LED: Input upon reset = GroupX Full Duplex ability: Upon reset, this pin sets the default value of Reg.0.8. In addition, on reset, this pin also sets Nway full-duplex ability on Reg.4.8 and Reg.4.6. Strap after reset for initial value of Group X UTP or FX mode. FX can be Force 100 Full or Force 100 Half.	1
LED_DUP[2]/GyFu ll	110	I/O	Output after reset = used for LED: Input upon reset = GroupY Full Duplex ability: Upon reset, this pin sets the default value of Reg.0.8. On reset, this pin also sets Nway full-duplex ability on Reg.4.8 and Reg.4.6. Strap after reset for initial value of Group Y UTP or FX mode. FX can be Force 100 Full or Force 100 Half.	1
GxEnFC	76	I	GroupX Enable Flow Control ability: 1: Enable Reg4.10 (NWAY Full duplex only), or “Enable Force Full pause ability of Force mode (UTP Force mode or FX mode)”, or “Enable Force Half Back Pressure ability of Force mode (UTP Force mode or FX mode)”. 0: Disable Reg4.10 (NWAY Full duplex only), or “Disable Force Full pause ability of Force mode (UTP Force mode or FX mode)”, or “Disable Force Half Back Pressure ability of Force mode (UTP Force mode or FX mode)”. Strap after reset for initial value of Group X “UTP NWAY Full”, or “UTP Force Full or Half mode”, or “FX Full or Half mode”. 8305SB = GxEnFC, 8305S = NWAYHALF#. For 8305SB, the function of NWAYHALF# is replaced by 3 pins: GxFull, GyFull, P4Full.	1
GyEnFC	77	I	GroupY Enable Flow Control ability: 1: Enable Reg4.10 (NWAY Full duplex only), or “Enable Force Full pause ability of Force mode (UTP Force mode or FX mode)”, or “Enable Force Half Back Pressure ability of Force mode (UTP Force mode or FX mode)”. 0: Disable Reg4.10 (NWAY Full duplex only), or “Disable Force Full pause ability of Force mode (UTP Force mode or FX mode)”, or “Disable Force Half Back Pressure ability of Force mode (UTP Force mode or FX mode)”. Strap after reset for initial value of Group Y “UTP NWAY Full”, or “UTP Force Full or Half mode”, or “FX Full or Half mode.” 8305SB = GyEnFC, 8305S = ENFCTRL. For 8305SB, the function of ENFCTRL is replaced by 3 pins: GxEnFC, GyEnFC, and P4EnFC.	1

6. Register Description

Hardware Reset: pin RESET# = 0 to 1. Reset all then load EEPROM and Pin registers with serial EEPROM and Pins strappings.

Soft Reset: Write bit15 of Reg16 of PHY3 as 1. Reset all except loading EEPROM and Pin Registers with serial EEPROM and Pins. After updating the EEPROM or Pin registers via SMI, the external device has to do soft reset in order to change the configuration.

Name	Soft Reset	PHY	Register	Register Description
Port0 PHY Reg	No	0	0	Control Register
			1	Status Register
			4	Auto-Negotiation Advertisement Register
			5	Auto-Negotiation Link Partner Ability Register
			6	Auto-Negotiation Expansion Registers
Port1 PHY Reg	No	1	0	Control Register
			1	Status Register
			4	Auto-Negotiation Advertisement Register
			5	Auto-Negotiation Link Partner Ability Register
			6	Auto-Negotiation Expansion Registers
Port2 PHY Reg	No	2	0	Control Register
			1	Status Register
			4	Auto-Negotiation Advertisement Register
			5	Auto-Negotiation Link Partner Ability Register
			6	Auto-Negotiation Expansion Registers
Port3 PHY Reg	No	3	0	Control Register
			1	Status Register
			4	Auto-Negotiation Advertisement Register
			5	Auto-Negotiation Link Partner Ability Register
			6	Auto-Negotiation Expansion Registers
Port4 PHY Reg	No	4	0	Control Register
			1	Status Register
			4	Auto-Negotiation Advertisement Register
			5	Auto-Negotiation Link Partner Ability Register
			6	Auto-Negotiation Expansion Registers
EEPROM Reg0	Need	0	16~22	Register for EEPROM
EEPROM Reg1	Need	1	16~31	Register for EEPROM
Pin Reg	Need	2	16	Register for some Pins
Pin & EEPROM Reg	Need	2	17	Register for some Pins and EEPROM
Port Control Reg	No	3	16	Register for Port Control
EEPROM Reg	Need	3	17~20	Register for EEPROM

RO: Read Only

RW: Read/Write

LL: Latch Low until clear

LH: Latch High until clear

SC: Self Clearing

6.1 PHY0 to 4: PHY Register of Each Port

6.1.1 Register0: Control Register

Reg.bit	Name	Description	Mode	Default
0.15	Reset	Reset: 1: PHY reset. This bit is self-clearing.	RW/SC	0
0.14	Loopback (digital loopback)	<p>Enable Loopback: This pin enables loopback from the MII TXD to the MII RXD and ignores all the activities on the cable media.</p> <p>1: Enable loopback 0: Normal operation</p> <p>This function is usable only when this PHY is 10Based-T full duplex or 100Base-T full duplex.</p> <p>The packet is forwarded from other PHY (could be 10Based-T, or 100TX, or 100FX, both full and half duplex) by switch core and will loopback to the switch core. It could be forwarded to the other port or dropped depending on the destination and source MAC address of the packet.</p>	RW	0
0.13	Spd_Sel	<p>Speed Select:</p> <p>1: 100Mbps 0: 10Mbps</p> <p>When Nway is enabled, this bit reflects the result of auto-negotiation. (Read only)</p> <p>When Nway is disabled, this bit can be set through SMI. (Read/Write)</p> <p>When 100FX mode is enabled, this bit =1. (Read only)</p>	RW	From pin
0.12	Auto Negotiation Enable	<p>1: Enable auto-negotiation process 0: Disable auto-negotiation process</p> <p>This bit can be set through SMI.(Read/Write)</p> <p>When 100FX mode is enabled, this bit =0.(Read only)</p> <p>100FX should be force mode. In order to avoid errors, the RTL8305SB will ignore the action to this bit when writing Reg0.12 as 1 in 100FX mode.</p>	RW	From pin
0.11	Power Down	<p>1: Power down. All functions will be disabled except SMI function and internal TXC to MAC. 0: Normal operation.</p>	RW	0
0.10	Isolate	<p>1: Electrically isolate the PHY from internal MII. The PHY is still able to response to MDC/MDIO. 0: Normal operation</p>	RW	0
0.9	Restart Auto Negotiation	<p>1: Restart Auto-Negotiation process. 0: Normal operation.</p>	RW/SC	0
0.8	Duplex Mode	<p>Duplex mode:</p> <p>1: Full duplex operation 0: Half duplex operation</p> <p>When Nway is enabled (Reg0.12=1), this bit reflects the result of auto-negotiation. (Read only)</p> <p>When Nway is disabled (Reg0.12=0, force mode of UTP or 100FX), this bit can be set through SMI*. (Read/Write)</p> <p>100FX should be force mode. In order to avoid errors, the RTL8305SB will ignore the action to this bit when writing Reg0.12 as 1 in 100FX mode.</p>	RW	From pin
0.[7:0]	Reserved		RO	0

6.1.2 Register1: Status Register

Reg.bit	Name	Description	Mode	Default
1.15	100Base_T4	0: No 100Base-T4 capability.	RO	0
1.14	100Base_TX_FD	1: 100Base-TX full duplex capable. 0: Not 100Base-TX full duplex capable.	RO	1
1.13	100Base_TX_HD	1: 100Base-TX half duplex capable. 0: Not 100Base-TX half duplex capable.	RO	1
1.12	10Base_T_FD	1: 10Base-TX full duplex capable. 0: Not 10Base-TX full duplex capable.	RO	1
1.11	10Base_T_HD	1: 10Base-TX half duplex capable. 0: Not 10Base-TX half duplex capable.	RO	1
1.[10:7]	Reserved		RO	0
1.6	MF Preamble Suppression	The RTL8305SB will accept management frames with preamble suppressed. The RTL8305SB accepts management frames without preamble. Minimum of 32 preamble bits are required for the first SMI read/write transaction after reset. One idle bit is required between any two management transactions as defined in IEEE802.3u specs.	RO	1
1.5	Auto-negotiate Complete	1: Auto-negotiation process completed. MII Reg.4,5 are valid if this bit is set. 0: Auto-negotiation process not completed.	RO	0
1.4	Remote Fault	1: Remote fault condition detected. 0: No remote fault. When in 100FX mode, this bit means in-band signal Far-End-Fault is detected.	RO/LH	0
1.3	Auto-Negotiation Ability	1: Nway auto-negotiation capable. (permanently: 1)	RO	1
1.2	Link Status	1: Link is established. If link had ever failed, this bit will be 0 until after reading this bit again. 0: Link is failed.	RO/LL	0
1.1	Jabber Detect	0: No Jabber detected. Note: this function is not necessary for single chip.	RO	0
1.0	Extended Capability	1: Extended register capable. (permanently: 1)	RO	1

6.1.3 Register4: Auto-Negotiation Advertisement Register

Reg.bit	Name	Description	Mode	Default
4.15	Next Page	1: Next Page enabled. 0: Next Page disabled. (Permanently: 0)	RO	0
4.14	Acknowledge	Permanently: 0	RO	0
4.13	Remote Fault	1: Advertises that RTL8305SB has detected a remote fault. 0: No remote fault detected.	RW	0
4.[12:11]	Reserved		RO	0
4.10	Pause	1: Advertises that RTL8305SB has flow control capability. 0: Without flow control capability.	RW	From pin
4.9	100Base-T4	Technology not supported. (Permanently =0)	RO	0
4.8	100Base-TX-FD	1: 100Base-TX full duplex capable. 0: Not 100Base-TX full duplex capable.	RW	From pin
4.7	100Base-TX	1: 100Base-TX half duplex capable. 0: Not 100Base-TX half duplex capable.	RW	From pin
4.6	10Base-T-FD	1: 10Base-TX full duplex capable. 0: Not 10Base-TX full duplex capable.	RW	From pin
4.5	10Base-T	1: 10Base-TX half duplex capable. 0: Not 10Base-TX half duplex capable.	RW	1
4.[4:0]	Selector Field	[00001]=IEEE802.3	RW	00001

6.1.4 Register5: Auto-Negotiation Link Partner Ability Register

Reg.bit	Name	Description	Mode	Default
5.15	Next Page	1: Link partner desires Next Page transfer. 0: Link partner does not desire Next Page transfer.	RO	0
5.14	Acknowledge	1: Link Partner acknowledges reception of FLP words. 0: Not acknowledged by Link Partner.	RO	0
5.13	Remote Fault	1: Remote Fault indicated by Link Partner. 0: No remote fault indicated by Link Partner.	RO	0
5.[12:11]	Reserved		RO	0
5.10	Pause	1: Flow control supported by Link Partner. 0: No flow control supported by Link Partner. <i>Note: this bit is read only when Reg0.12=1. This bit is read/write when Reg0.12=0 for future use.</i>	RW	0
5.9	100Base-T4	1: 100Base-T4 supported by Link Partner. 0: 100Base-T4 not supported by Link Partner.	RO	0
5.8	100Base-TX-FD	1: 100Base-TX full duplex supported by Link Partner. 0: 100Base-TX full duplex not supported by Link Partner. For 100FX mode, this bit is set when Reg.0.8=1 or **Full =1 after link established. When Nway disabled TX mode, this bit is set when Reg.0.13=1, and Reg.0.8=1 after link established.	RO	0
5.7	100Base-TX	1: 100Base-TX half duplex supported by Link Partner. 0: 100Base-TX half duplex not supported by Link Partner. For 100FX mode, this bit is set when Reg.0.8=0 or **Full = 0 after link established. When Nway disabled, this bit is set when Reg.0.13=1, and Reg.0.8=0 after link established.	RO	0
5.6	10Base-T-FD	1: 10Base-TX full duplex supported by Link Partner. 0: 10Base-TX full duplex not supported by Link Partner. When Nway disabled, this bit is set when Reg.0.13=0, and Reg.0.8=1 after link established.	RO	0
5.5	10Base-T	1: 10Base-TX half duplex supported by Link Partner. 0: 10Base-TX half duplex not supported by Link Partner. When Nway disabled, this bit is set when Reg.0.13=0, and Reg.0.8=0. after link established	RO	0
5.[4:0]	Selector Field	[00001]=IEEE802.3	RO	00001

6.1.5 Register6: Auto-Negotiation Expansion Register

Reg.bit	Name	Description	Mode	Default
6.[15:5]	Reserved		RO	0
6.4	Parallel Detection Fault	1: A fault has been detected via the Parallel Detection function. 0: A fault has not been detected via the Parallel Detection function.	RO	0
6.3	Link Partner Next Page Able	1: Link Partner is Next Page able. 0: Link Partner is not Next Page able. (permanently=0)	RO	0
6.2	Local Next Page Able	1: RTL8305SB is Next Page able. 0: RTL8305SB is not Next Page able.	RO	0
6.1	Page Received	1: A New Page has been received. 0: A New Page has not been received.	RO	0
6.0	Link Partner Auto-Negotiation Able	If Nway is enabled, this bit means: 1: Link Partner is Auto-Negotiation able. 0: Link Partner is not Auto-Negotiation able. In 100FX or Nway disabled, this bit always =1.	RO	0 (Nway) or 1 (Force)

6.2 PHY0: EEPROM Register0

6.2.1 Register16: EEPROM Byte0 and 1 Register

Reg.bit	Name	Description	Mode	Default
16.15	Internal		RW	1
16.14	DisLoop	Disable Loop Detection Function. 1: Disable Loop Detection function. 0: Enable Loop Detection function.	RW	1
16.13	Internal		RW	1
16.12	Internal		RW	1
16.11	EnP4LED	Enable Port4 LED. 1: Drive LED pins of port4. 0: Do not drive LED pins of port4 for special application. In UTP applications, this bit should be 1 to drive LEDs of port 4. This bit is reserved for original RTL8305S users only, and not used for general applications.	RW	1
16.10	Reserved		RO	1
16.9	Reserved		RO	1
16.8	Reserved		RO	1
16.7	Internal		RW	1
16.6	Internal		RW	1
16.5	Internal		RW	1
16.4	Internal		RW	1
16.3	Internal		RW	1
16.2	Internal		RW	1
16.1	Internal		RW	1
16.0	NoEEPROM	1: EEPROM does not exist. (pin EnEEPROM=0. Or pin EnEEPROM=1 but no EEPROM) 0: EEPROM exist.(pin EnEEPROM=1 and have EEPROM)	RO	

6.2.2 Register17: EEPROM Byte2 and 3 Register

Reg.bit	Name	Description	Mode	Default
17.15~17.10	Reserved		RO	1
17.9	Internal	Internal Use Only: Should be 1.	RW	1
17.8	Internal	Internal Use Only: Should be 1.	RW	1
17.7~17.4	Reserved		RO	1111
17.3~17.0	Internal	Internal Use Only: Should be 0000.	RW	0000

6.2.3 Register18~20: EEPROM EthernetID Register For Bytes 4, 5, 6, 7, 8, and 9

Reg.bit	Name	Description	Mode	Default
18	EthernetID	Device Ethernet MAC ID: Byte 4, 5 of EEPROM	RW	[7:0]=52 [15:8]=54
19	EthernetID	Device Ethernet MAC ID: Byte 6, 7 of EEPROM	RW	[7:0]=4c [15:8]=83
20	EthernetID	Device Ethernet MAC ID: Byte 8, 9 of EEPROM	RW	[7:0]= 05 [15:8]= b0

6.2.4 Register21: EEPROM Byte10 and 11 Register

Reg.bit	Name	Description	Mode	Default
21.15	Reserved		RO	1
21.14~21.12	P3VLANIndex[2] P3VLANIndex[1] P3VLANIndex[0]	Port 3 VLAN Index: P3VLANIndex[2:0]=0b011 means port 3 use the forth VLAN (VLAN D).	RW	011
21.11	Reserved		RO	1
21.10~21.8	P2VLANIndex[2] P2VLANIndex[1] P2VLANIndex[0]	Port 2 VLAN Index: P2VLANIndex[2:0]=0b010 means port 2 use the third VLAN (VLAN C).	RW	010
21.7	Reserved		RO	1
21.6~21.4	P1VLANIndex[2] P1VLANIndex[1] P1VLANIndex[0]	Port 1 VLAN Index: P1VLANIndex[2:0]=0b001 means port 1 use the second VLAN (VLAN B).	RW	001
21.3	Reserved		RO	1
21.2~ 21.0	P0VLANIndex[2] P0VLANIndex[1] P0VLANIndex[0]	Port 0 VLAN Index: P0VLANIndex[2:0] are use to assign the VLAN of port 0. For example, P0VLANIndex[2:0]=0b000 means port 0 use the first VLAN (VLAN A). P0VLANIndex[0] is bit0, P0VLANIndex[1] is bit1, P0VLANIndex[2] is bit2.	RW	000

6.2.5 Register22: EEPROM Byte12 and 13 Register

Reg.bit	Name	Description	Mode	Default
22.15 22.14	P3IRTag[1] P3IRTag[0]	Insert/Remove Priority Tag of Port3. 11: Do not insert/remove Tag from Output High and Low Queue of Port3 10: Insert Tag from Output High and Low Queue of Port3 01: Insert Tag from Output High Queue only of Port3 00: Remove Tag from Output High and Low Queue of Port3	RW	11
22.13 22.12	P2IRTag[1] P2IRTag[0]	Insert/Remove Priority Tag of Port2. 11: Do not insert/remove Tag from Output High and Low Queue of Port2 10: Insert Tag from Output High and Low Queue of Port2 01: Insert Tag from Output High Queue only of Port2 00: Remove Tag from Output High and Low Queue of Port2	RW	11
22.11 22.10	P1IRTag[1] P1IRTag[0]	Insert/Remove Priority Tag of Port1. 11: Do not insert/remove Tag from Output High and Low Queue of Port1 10: Insert Tag from Output High and Low Queue of Port1 01: Insert Tag from Output High Queue only of Port1 00: Remove Tag from Output High and Low Queue of Port1	RW	11
22.9 22.8	P0IRTag[1] P0IRTag[0]	Insert/Remove Priority Tag of Port0. 11: Do not insert/remove Tag from Output High and Low Queue of Port0 10: Insert Tag from Output High and Low Queue of Port0 01: Insert Tag from Output High Queue only of Port0 00: Remove Tag from Output High and Low Queue of Port0	RW	11
22.7 22.6	P4IRTag[1] P4IRTag[0]	Insert/Remove Priority Tag of Port4. 11: Do not insert/remove Tag from Output High and Low Queue of Port4 10: Insert Tag from Output High and Low Queue of Port4 01: Insert Tag from Output High Queue only of Port4 00: Remove Tag from Output High and Low Queue of Port4	RW	11
22.5~11.3	Reserved		RO	1
22.2~ 22.0	P4VLANIndex[2] P4VLANIndex[1] P4VLANIndex[0]	Port 4 VLAN Index. P4VLANIndex[2:0]=0b100 means port 4 use the fifth VLAN (VLAN E).	RW	100

6.3 PHY1: EEPROM Register1

6.3.1 Register16~23: EEPROM (Byte 14~29) Register

Reg.bit	Name	Description	Mode	Default
16	Internal	Internal use only	RW	
17	Internal	Internal use only	RW	
18	Internal	Internal use only	RW	
19	Internal	Internal use only	RW	
20	Internal	Internal use only	RW	
21	Internal	Internal use only	RW	
22	Internal	Internal use only	RW	
23	Internal	Internal use only	RW	

Note: There is no default value.

6.3.2 Register24~31: EEPROM VLAN (Byte 30~44) Register

Reg.bit	Name	Description	Mode	Default
24.15~24.12	Reserved		RO	1111
24.11~24.0	VIDA[11:0]	VLAN Identifier of VLAN A: Reg24.11=VIDA[11], Reg24.0=VIDA[0]. There is no default value.	RW	
25.7~25.5	Reserved		RO	111
25.4~25.0	MemberA[4:0]	Member Set of VLAN A: MemberA[4:0] determines the VLAN member of VLAN A. For example, MemberA[4:0]=10001 means port4 and port0 are the members of VLAN A. MemberA[4:0]=10010 means port4 and port1 are the members of VLAN A. MemberA[4:0]=11111 means all ports are members of VLAN A.	RW	10001
26.7~26.4	Reserved		RO	1111
26.3~26.0 25.15~25.8	VIDB[11:0]	VLAN Identifier of VLAN B: There is no default value.	RW	
26.15~26.11	Reserved		RO	111
26.12~26.8	MemberB[4:0]	Member Set of VLAN B: MemberB[4:0]=10010 means port4 and port1 are members of VLAN B.	RW	10010
27.15~27.12	Reserved		RO	1111
27.11~27.0	VIDC[11:0]	VLAN Identifier of VLAN C: There is no default value.	RW	
28.7~28.5	Reserved		RO	111
28.4~28.0	MemberC[4:0]	Member Set of VLAN C: MemberC[4:0]=10100 means port4 and port2 are members of VLAN C.	RW	10100
29.7~29.4	Reserved		RO	1111
29.3~29.0 28.15~28.8	VIDD[11:0]	VLAN Identifier of VLAN D: There is no default value.	RW	
29.15~29.13	Reserved		RO	111
29.12~29.8	MemberD[4:0]	Member Set of VLAN D: MemberD[4:0]=11000 means port4 and port3 are members of VLAN D.	RW	11000
30.15~30.12	Reserved		RO	1111
30.11~30.0	VIDE[11:0]	VLAN Identifier of VLAN E: There is no default value.	RW	
31.15~31.5	Reserved		RO	1111111111
31.4~31.0	MemberE[4:0]	Member Set of VLAN E: MemberE[4:0]=11111 means all ports are the members of VLAN E.	RW	11111

6.4 PHY2: Pin & EEPROM Register

6.4.1 Register16: Pin Register

The RTL8305SB will load the value from pins upon reset, but can be updated via SMI after reset. This register needs a soft reset.

Reg.bit	Name	Description	Mode	Default
16.15	Internal	Internal use only	RW	1
16.14	Internal	Internal use only	RW	1
16.13	Internal	Internal use only	RW	1
16.12	Internal	Internal use only	RW	1
16.11	Reserved	Internal use only	RW	1
16.10	Reserved	Internal use only	RW	1
16.9 16.8	Qweight[1] Qweight[0]	Weighted Round Robin Ratio of Priority Queue: The frame service rate of High-pri queue: Low-pri queue 11: 16:1 10: Always high priority queue first 01: 8:1 00: 4:1 Pin Register.	RW	11
16.7	DisFCAutoOff	Disable Auto Turn Off Function of Flow Control Ability: 1: Disable 0: Enable Enable Auto turn off low priority queue's flow control ability 1~2 sec whenever the port received a high priority frame. The flow control ability will re-enabled when there is not received and high priority frame during 1~2 sec. Pin Register.	RW	1
16.6	DisDSPri	Disable Differentiated Service Priority: 1: Disable DS priority 0: Enable DS priority Pin Register.	RW	1
16.5	DisTagPri	Disable 802.1p VLAN Tag Priority Based QoS Function: 1: Disable 0: Enable Pin Register.	RW	1
16.4	DisPortPri[4]	Disable Port Based Priority QoS Function for Port4: DisPortPri[4]: 1: Disable port 4 priority 0: Enable port 4 priority	RW	1
16.3	DisPortPri[3]	Disable Port Based Priority QoS Function for Port3: DisPortPri[3]: 1: Disable port 3 priority 0: Enable port 3 priority	RW	1
16.2	DisPortPri[2]	Disable Port Based Priority QoS Function for Port2: DisPortPri[2]: 1: Disable port 2 priority 0: Enable port 2 priority	RW	1
16.1	DisPortPri[1]	Disable Port Based Priority QoS Function for Port1: DisPortPri[1]: 1: Disable port 1 priority 0: Enable port 1 priority	RW	1
16.0	DisPortPri[0]	Disable Port Based Priority QoS Function for Port0: DisPortPri[0]: 1: Disable port 0 priority 0: Enable port 0 priority Pin Register.	RW	1

6.4.2 Register17: Pin & EEPROM Register for VLAN

Reg.bit	Name	Description	Mode	Default
17.15~17.6	Reserved		RW	1111 1111 11
17.5	DisVLAN	Disable VLAN: 1: Disable VLAN 0: Enable VLAN	RW	1
17.4	DisTagAware	Disable Tag Aware: 1: Disable the 802.1Q tagged-VID Aware function. The RTL8305SB will not check the tagged VID of received frame to do the VLAN classification. The RTL8305SB will always use Port Based VLAN mapping. 0: Enable the Member Set Filtering function of VLAN Ingress Rule. The RTL8305SB will check the tagged VID of received frame to do the VLAN classification. The RTL8305SB will use tagged-VID VLAN mapping for tagged frame and will use Port Based VLAN mapping for untagged and priority-tagged frame.	RW	1
17.3	DisMemFilter	Disable Member Set Filtering: 1: Disable the Member Set Filtering function of VLAN Ingress Rule. The RTL8305SB will not discard any frames associated with a VLAN for which that port is not in the member set. 0: Enable the Member Set Filtering function of VLAN Ingress Rule. The RTL8305SB will discard any frames associated with a VLAN for which that port is not in the member set.	RW	1
17.2	DisTagAdmitCtrl	Disable Tag Admit Control: Acceptable Frame Type: 1: Disable Tag Admit Control: Acceptable Frame Type is "Admit All". The RTL8305SB will receive all frames. 0: Enable Tag Admit Control: Acceptable Frame Type is "Admit All Tagged". The RTL8305SB will receive only the VLAN-tagged frame and drop all other untagged frames and priority tagged (VID=0) frame.	RW	1
17.1	DisLeaky	Disable Leaky VLAN: 1: Disable to forward unicast frames to other VLAN. 0: Enable to forward unicast frames to other VLAN. Broadcast and multicast frames adhere to the VLAN configuration.	RW	1
17.0	DisARP	Disable ARP Broadcast to all VLAN: 1: Disable to broadcast the ARP broadcast packet to all VLANs. 0: Enable to broadcast the ARP broadcast packet to all VLANs. ARP broadcast frame: DID is all F.	RW	1

6.5 PHY3: Port Control Register

6.5.1 Register16: Port Control Register

This register does not need a soft reset.

Reg.bit	Name	Description	Mode	Default
16.15	SoftReset	Soft Reset: 1: Soft reset. This bit is self-clearing.	RW/SC	0
16.14~16.10	Reserved		RO	1
16.9	DisP4LoopBack	Disable Port4 Loopback: 1: Disable port4 loopback function for normal application 0: Enable port4 loopback function for diagnostic application	RW	1
16.8	DisP3LoopBack	Disable Port3 Loopback: 1: Disable port3 loopback function for normal application 0: Enable port3 loopback function for diagnostic application	RW	1
16.7	DisP2LoopBack	Disable Port2 Loopback: 1: Disable port2 loopback function for normal application 0: Enable port2 loopback function for diagnostic application	RW	1
16.6	DisP1LoopBack	Disable Port1 Loopback: 1: Disable port1 loopback function for normal application 0: Enable port1 loopback function for diagnostic application	RW	1
16.5	DisP0LoopBack	Disable Port0 Loopback: 1: Disable port0 loopback function for normal application 0: Enable port0 loopback function for diagnostic application	RW	1
16.4	EnPort4	Enable Link of Port4: 1: Enable Port4's PHY (UTP or FX) to provide the Link status to MAC for normal operation 0: Disable Port4's PHY (UTP or FX) to provide the Link status to MAC. This port is linked fail for MAC, but PHY still work normally. The link status of MII MAC/MII PHY/SNI PHY is determined by P4LNKSTA pin.	RW	1
16.3	EnPort3	Enable Link of Port3: 1: Enable Port3's PHY (UTP or FX) to provide the Link status to MAC for normal operation. 0: Disable Port3's PHY (UTP or FX) to provide the Link status to MAC. This port is linked fail for MAC, but PHY still work normally.	RW	1
16.2	EnPort2	Enable Link of Port2: 1: Enable Port2's PHY (UTP or FX) to provide the Link status to MAC for normal operation. 0: Disable Port2's PHY (UTP or FX) to provide the Link status to MAC. This port is linked fail for MAC, but PHY still work normally.	RW	1
16.1	EnPort1	Enable Link of Port1: 1: Enable Port1's PHY (UTP or FX) to provide the Link status to MAC for normal operation. 0: Disable Port1's PHY (UTP or FX) to provide the Link status to MAC. This port is linked fail for MAC, but PHY still work normally.	RW	1
16.0	EnPort0	Enable Link of Port0: 1: Enable Port0's PHY (UTP or FX) to provide the Link status to MAC for normal operation. 0: Disable Port0's PHY (UTP or FX) to provide the Link status to MAC. This port is linked fail for MAC, but PHY still work normally.	RW	1

6.5.2 Register17: EEPROM (Byte 46) Register

Reg.bit	Name	Description	Mode	Default
17.15~17.7	Reserved		RO	1111 1111 1
17.6	Internal	Internal use only	RW	1
17.5~17.3	Internal	Internal use only	RW	
17.2~17.0	Internal	Internal use only	RW	

6.5.3 Register18~20: EEPROM (Byte 47~52) Register

Reg.bit	Name	Description	Mode	Default
18	Internal	Internal use only	RW	
19	Internal	Internal use only	RW	
20	Internal	Internal use only	RW	

7. Functional Description

7.1 Switch Core Functional Overview

7.1.1 Application

The RTL8305SB is a 5 port Fast Ethernet switch controller, which integrates embedded memory, five MAC, and five physical layer transceivers for 10Base-T and 100Base-TX into a single chip. All ports also support 100Base-FX, which shares pins with UTP (TX+/-/RX+/-) and needs no SD+/- pins (this is a Realtek patent technology).

The five ports are separated into 3 groups (GroupX/GroupY/Port4) for flexible port configuration using strapping pins upon reset. The SetGroup pin is used to select the port numbers for GroupX and GroupY (SetGroup=1: GroupX=Port0; GroupY=Ports 1, 2, and 3. SetGroup=0: GroupX=Ports 0 and 1; GroupY=Ports 2 and 3). The GxMode/GyMode/P4Mode[1:0] pins are used to select the operation mode. (UTP / FX for GroupX and GroupY. UTP / FX / PHY mode MII / PHY mode SNI / MAC mode MII for Port4)

Upon reset: defined as a short time after at the end of a hardware reset. **After reset:** defined as the time after the specified "Upon Reset" time.

7.1.2 Port4

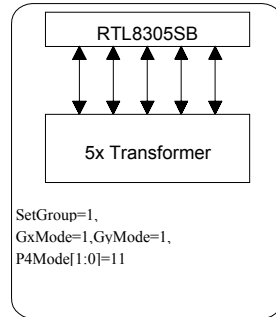
Operation mode of port4: Each port has two parts: MAC and PHY. In the UTP and FX mode, Port4 uses both the MAC and internal PHY parts like the other ports. In the other mode, Port4 uses only the MAC part, which provides an external interface to connect to the external MAC or PHY. Two pins are used for those operation mode configurations: P4MODE[1:0].

The fifth port (port 4) supports an external MAC interface which can be set to PHY mode MII, PHY mode SNI, or MAC mode MII to work with an external MAC of a routing engine, PHY of a HomePNA or other physical layer transceiver.

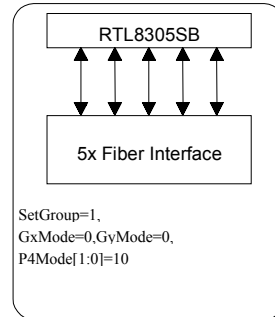
If the MAC part of Port4 connects with an external MAC, such as processor for a router application, it should act as a PHY. This is PHY mode MII or PHY mode SNI. In PHY mode MII or PHY mode SNI, Port4 uses the MAC part only, and provides an external MAC interface to connect MAC of external device. In order to connect both MACs, the MII of the switch MAC should be reversed into PHY mode.

If the MAC part of Port4 connects with an external PHY, such as a PHY for a HomePNA application, Port4 should act as MAC. This is MAC mode MII. In MAC mode MII, Port4 uses its MAC to connect external PHY and ignores the internal PHY part.

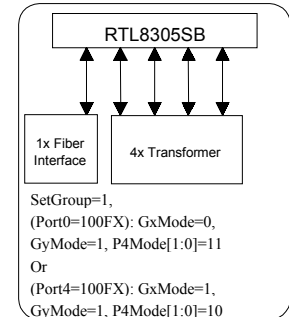
General System Application
 1. General switch application
 2. Router application:
 3. HomePNA application
 4. Other PHY application



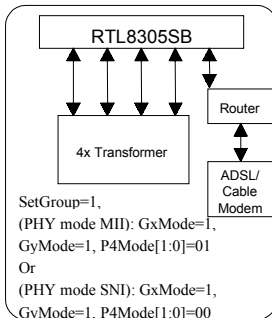
1.1 General switch application:
5 port 10/100 UTP



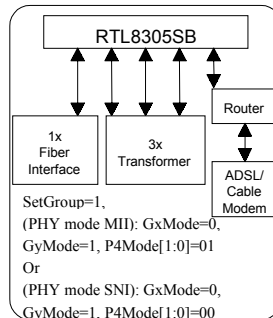
1.2 General switch application:
5 port 100 FX



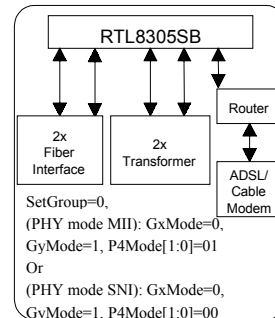
1.3 General switch application:
1 port 100 FX (Port0 or 4)
4 port 10/100 UTP



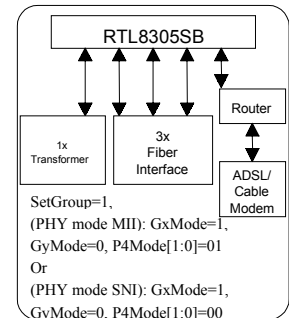
2.1: Router application:
4 port 10/100 UTP
1 port PHY mode MII or SNI (Port4)



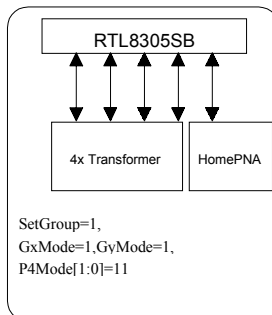
2.2: Router application:
1 port 100 FX (Port0)
3 port 10/100 UTP (Port1,2,3)
1 port PHY mode MII or SNI (Port4)



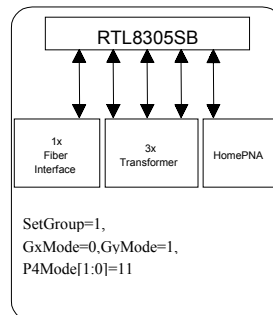
2.3: Router application:
2 port 100 FX (Port0, 1)
2 port 10/100 UTP (Port2,3)
1 port PHY mode MII or SNI (Port4)



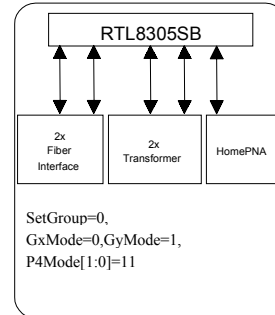
2.4: Router application:
1 port 10/100 UTP (Port0)
3 port 100 FX (Port1,2,3)
1 port PHY mode MII or SNI (Port4)



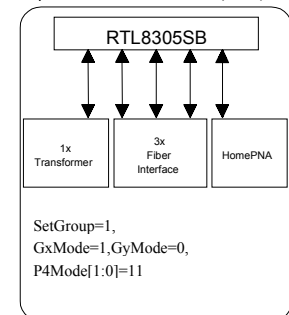
3.1: HomePNA application:
4 port 10/100 UTP
1 port MAC mode MII (Port4)



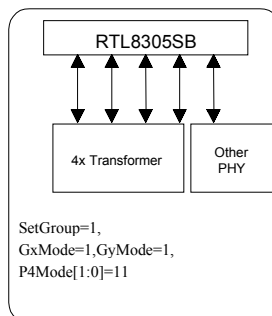
3.2: HomePNA application:
1 port 100 FX (Port0)
3 port 10/100 UTP (Port1,2,3)
1 port MAC mode MII (Port4)



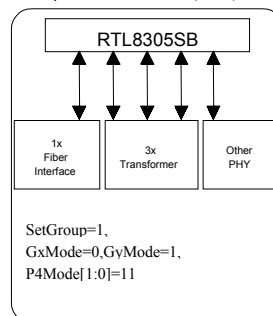
3.3: HomePNA application:
2 port 100 FX (Port0,1)
2 port 10/100 UTP (Port2,3)
1 port MAC mode MII (Port4)



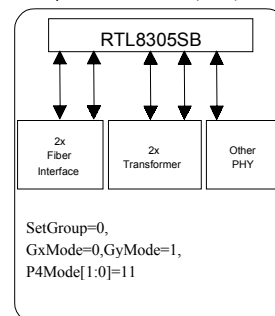
3.4: HomePNA application:
1 port 10/100 UTP (Port0)
3 port 100 FX (Port1,2,3)
1 port MAC mode MII (Port4)



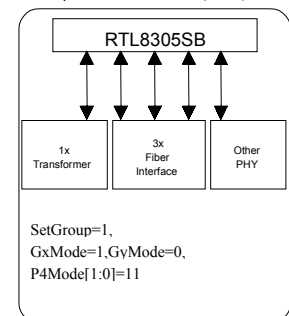
4.1: Other PHY application:
4 port 10/100 UTP
1 port MAC mode MII (Port4)



4.2: Other PHY application:
1 port 100 FX (Port0)
3 port 10/100 UTP (Port1,2,3)
1 port MAC mode MII (Port4)



4.3: Other PHY application:
2 port 100 FX (Port0,1)
2 port 10/100 UTP (Port2,3)
1 port MAC mode MII (Port4)



4.4: Other PHY application:
1 port 10/100 UTP (Port0)
3 port 100 FX (Port1,2,3)
1 port MAC mode MII (Port4)

External MAC interface: In order to act as PHY. When port4 is in PHY mode, some pins of the external MAC interface should be changed. For example, TXC are input pins for MAC but output pins for PHY. So the pin MTXC/PRXC is input for MAC mode and output for PHY mode. Please refer to below diagram to check the relationship between RTL8305SB and the external device. Hint: Connect input of RTL8305SB to output of external device. RTL8305SB has no RXER, TXER, and CRS pins for MII signaling. Because RTL8305SB does not support pin CRS, it is necessary to connect the MTXEN/PRXDV (output) of PHY mode to both CRS and RXDV (input) of the external device.

Note: In order to differentiate between MAC and PHY mode, the RTL8305SB change the pin name of PHY mode. For example: RTL8305SB=MRXD[0]/PTXD[0], RTL8305S=MRXD[0]/MTXD[0].

Port4 status pins: When P4MODE[1:0]=11, Port4 can be either UTP or MAC mode MII. Port4 will automatically detect the link status of UTP from internal PHY and link status MAC mode MII from both TXC of external PHY and P4LNKSTA#. If both UTP and MII port are linked OK, UTP has higher priority and RTL8305SB will ignore the signal of MII port.

In UTP and FX mode, the internal PHY will provide the port status (Link/Speed/Duplex/Full Flow Control ability) in real time. In order to provide the initial configuration of Port4's PHY (UTP or FX mode), four pins (P4ANEG, P4Full, P4Spd100, P4EnFC) are used to strap upon reset. **Upon reset:** defined as a short time after at the end of hardware reset. However, three of these pins are also used for Port4's MAC (the other three modes) in real time after reset (P4Spd100 -> P4SpdSta, P4Full -> P4DupSta, P4EnFC -> P4FLCTRL). **After reset:** defined as the time after upon reset. *Note: These 3 pin are changed as high active in order to provide dual function. For example: RTL8305SB=P4SpdSta/P4Spd100, RTL8305SB=P4SpdSta#.*

In the other three modes, four pins (P4LNKSTA#, P4SpdSta, P4DupSta, P4FLCTRL) are necessary in order to provides the port status to Port4's MAC in real time. That means that the external MAC or PHY should be forced to the same port status as Port4's MAC.

Related pins: When port4 is in UTP or FX mode, the LEDs of port4 are used to displays PHY status. When port4 is in other mode, the LEDs of port4 are used to displays MAC status.

Four parallel LEDs corresponding to port 4 can be three-stated (disable LED functions) for MII port application by setting ENP4LED in EEPROM as 0. In UTP application, this bit should be 1 to drive LEDs of port 4.

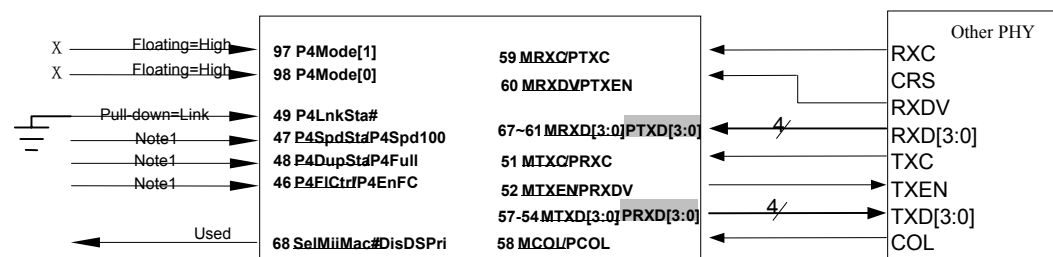
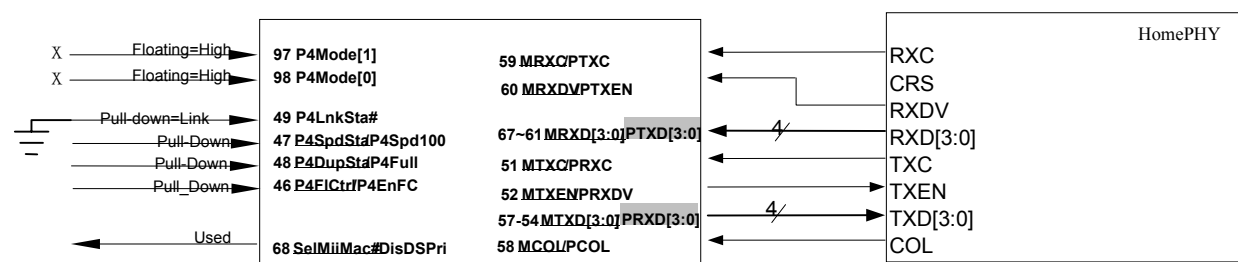
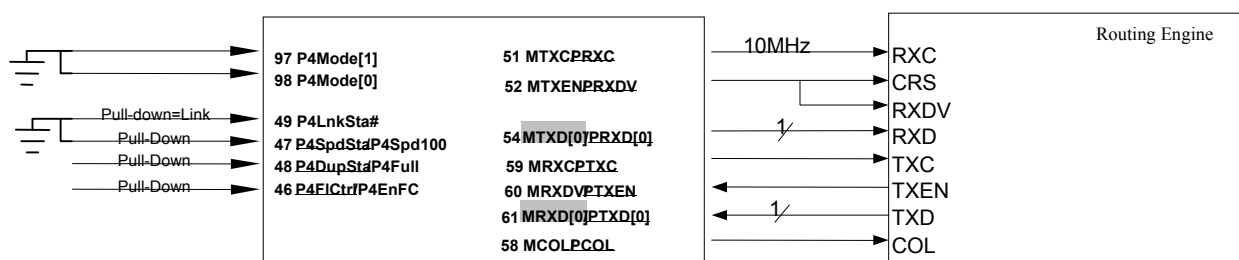
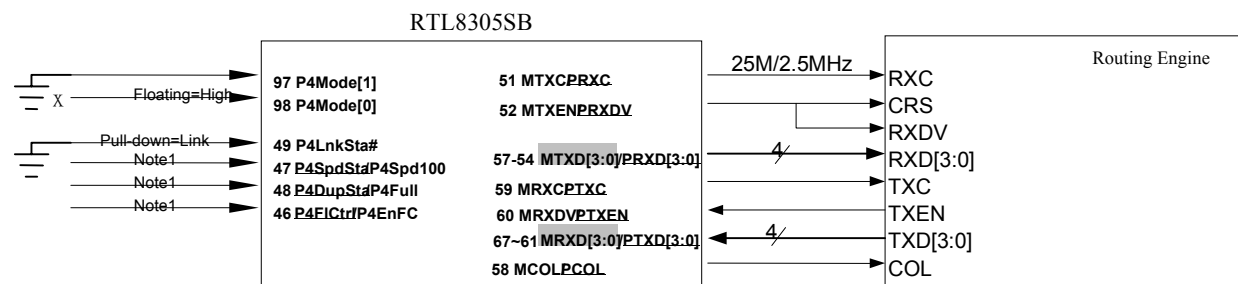
Pin **SEL_MIIMAC#** can be used to indicate MII MAC port active after reset for the sake of UTP/MII auto-detection.

One 25MHz clock output (pin CK25MOUT) can be used as a clock source of the underlying HomePNA/other PHY physical devices. *Note: the output voltage is 2.5V for RTL8305SB but is 3.3V for RTL8305S.*

PHY mode MII/PHY mode SNI: In routing application, RTL8305SB cooperates with a routing engine to communicate with WAN (Wide Area Network) through MII/SNI. In such application, P4LNKSTA# =0 and P4MODE[1] is pulled low upon reset. P4MODE[0] determines whether MII or SNI mode is selected.

In MII (nibble) mode (P4MODE[0]=1), P4SPDSTA=1 results in MII operating at 100Mbps with MTXC and MRXC runs at 25MHz; however, P4SPDSTA=0 leads to MII operating at 10Mbps with MTXC and MRXC runs at 2.5MHz.

In SNI (serial) mode (P4MODE[0]=0), P4SPDSTA takes no effect and should be pull-down. SNI mode operates at 10Mbps only, with MTXC and MRXC running at 10MHz. In SNI mode, RTL8305SB does not loopback RXDV signal as response to TXEN and does not support heart-beat function. (asserting COL signal for each complete of TXEN signal).



Note1: Floating or Pull-down, depend on application

Note2: Pin 46,47, and 48 are high active for RTL8305SB, but are low active for RTL8305S.

MAC mode MII: In HomePNA or other PHY applications, the RTL8305SB provides the MII interface to the underlying HomePNA or other physical devices so as to communicate with other types of LAN media. In such applications, the P4MODE[1:0] pins are floating upon reset and the RTL8305SB supports the UTP/MII auto-detection function. When both UTP and MII are active (link on), the UTP port has a higher priority over MII port.

In HomePNA applications, P4SPDSTA must be pulled down since HomePNA is half-duplex only. P4DUPSTA should be pulled down as well. P4LNKSTA# must be pulled down instead of being wired to the LINK LED pin of the HomePNA because of the unstable link state of HomePNA, a characteristic based on the HomePNA 1.0 standard. Because the HomePNA PHY physical layer is half duplex and can only detect the collision event during AID header interval (the time for transmit Ethernet preamble), the back pressure flow control algorithm is not suitable for the HomePNA network. So the P4FLCTRL pin should be pulled down.

For other PHY applications, P4SPDSTA, P4DUPSTA, and P4FLCTRL depend on application.

7.1.3 Port Status Configuration

The RTL8305SB supports flexible port status configuration for PHY by pin (GxANeg/GyANeg/P4ANeg, GxSpd100/GySpd100/P4Spd100, and GxFull/GyFull/P4Full) on a group basis upon reset or by internal registers (Reg0.12, Reg0.13, Reg0.8, and Reg4.5/4.6/4.7/4.8) via SMI on a per port basis after reset. Those pins are used to assign the initial value of MII register 0 and 4 (PHY registers) upon reset. The registers can be updated via SMI on a per port basis after reset. For example, the initial value of register 0.12 of port4 will be 0 when pin P4ANeg is 1 upon reset. *Note: The RTL8305S only supports UTP with Auto-Negotiation ability. Only one pin, NWAYHalf#, is supported for global configuration of all PHYs. And does not support these registers for configuration via SMI.*

All ports support 100Base-FX, which share pins with UTP (TX+/-/RX+/-) and need no SD+/- pins (Realtek patent). The 100Base-FX can be forced into half or full duplex mode with optional flow control ability. In order to operate correctly, both sides of the connection should set the same duplex and flow control ability. In 100Base-FX, only duplex and flow control ability can be set via strapped pins upon reset or via SMI after reset. Note that 100Base-FX does not support Auto-Negotiation according to IEEE 802.3u. Pins GxANeg/GyANeg/P4ANeg as well as GxSpd100/GySpd100/P4Spd100 are not used for 100Base-FX mode and can be left floating while in 100Base-FX mode. For example: port4 will be forced into full duplex 100Base-FX with flow control ability when P4Mode[1:0]=10, P4Full=1, P4EnFC=1 upon reset (regardless of P4Spd100 and P4ANeg).

When Auto-Negotiation ability is enabled in UTP mode, the RTL8305SB supports Auto-Negotiation and parallel detection for 10Base-T/100Base-TX to automatically determine line speed, duplex and flow control ability. The parallel detection process is used when the other side does not support auto-negotiation. For example: port0 is UTP with all abilities (default for normal switch application: GxMode=1, GxANeg=1, GxSpd100=1, GxFull=1, GxEnFC=1. The content of MII registers will be Reg0.12=1, Reg4.5=1, Reg4.6=1, Reg4.7=1, Reg4.8=1, and Reg4.10=1.) If the other side is auto-negotiation, 10Full with 802.3x flow control ability, port0 will enter the auto-negotiation process. The result should be 10Full with 802.3x flow control ability for both sides. If the other side is 10M without auto-negotiation, port0 will enter the parallel detection process. The result should be 10Half without 802.3x flow control ability for port0.

Note: Each port can operate at 10Mbps or 100Mbps with full-duplex or half-duplex mode independently to others when auto-negotiation process is on.

The port status for the PHY on a group basis can easily be set by pin configuration. For example, when group X is 100FX (GxMode=0), group X can be set as force mode half duplex by setting pin GxFull to 0. Group Y can also be set as UTP mode NWAY mode 10Full by setting pins GyMode=1, GyANeg=1, GySpd100=0, GyFull=1. Refer to the pin descriptions for details.

7.1.4 Enable Port

The RTL8305SB supports internal registers for individual ports for MAC to mask the current Link status from the PHY. For example: If register EnPort0=0, MAC of port0 will ignore Link status from the PHY and treat this port as no-link.

7.1.5 Flow Control

The RTL8305SB supports IEEE 802.3x full duplex flow control, Force mode Full duplex Flow Control, and optional half duplex back pressure.

IEEE 802.3x full duplex flow control: For UTP with auto-negotiation ability (GxANeg/GyANeg/P4Aneg is 1), the pause ability (Reg 4.10) of full duplex flow control is enabled by pin GxEnFC/GyEnFC/P4EnFC on a group basis upon reset or internal registers via SMI in per port basis after reset. For UTP with auto-negotiation ability, the IEEE 802.3x flow control's ability is auto-negotiated between the remote device and the RTL8305SB. If the result of the 802.3x pause ability auto-negotiation is enabled (Reg 4.10=1 and Reg5.10=1), the full duplex 802.3x flow control function is enabled. Otherwise, the full duplex 802.3x flow control function is disabled.

Force mode Full duplex Flow Control: For UTP without auto-negotiation ability (GxANeg/GyANeg/P4Aneg is 0) and 100Base-FX, the IEEE 802.3x flow control's ability can be forced to enabled at the RTL8305SB side by a pin GxEnFC/GyEnFC/P4EnFC in group basis upon reset or internal registers (Reg5.10) via SMI in per port basis after reset. For example, port 4 will be forced to 10Full UTP with forced mode full duplex flow control ability, regardless of the other side, when P4Mode[1:0]=10, P4Aneg=0, P4Spd100=0, P4Full=1, P4EnFC=1. Port 0 will be forced to 100Full FX with forced mode full duplex flow control ability, regardless of the other side when SetGroup=1, GxMode=0, GxFull=1, GxEnFC=1.

Regardless of IEEE 802.3x full duplex flow control or Force mode Full duplex Flow Control, when full duplex flow control is enabled, the RTL8305SB will only recognize the 802.3x flow control PAUSE ON/OFF frames with DA="0180C2000001", type="8808", OP-code="01", PAUSE Time = maximum to zero, and with good CRC.

If a PAUSE frame is received from any PAUSE flow control enabled port with DA=0180C2000001, the corresponding port of the RTL8305SB will stop its packet transmission until the PAUSE timer times out or another PAUSE frame with zero PAUSE time is received. The RTL8305SB will not forward any 802.3x PAUSE frames received from any port.

Half duplex back pressure: The RTL8305SB adopts optional half duplex back pressure design:

If pin EnDefer is 1, the RTL8305SB will send a preamble to defer the other station's transmission when there is no packet to send. Otherwise, if pin EnDefer is 0, the RTL8305SB will force a collision to the other station's transmission when the buffer is full.

If pin 48pass1 is 0, the RTL8305SB will collide with JAM always (Continuous collision). Otherwise, if pin 48pass1 is 1, the RTL8305SB will try to forward one packet successfully after 48 force collisions (48pass1), to avoid the connected repeater being partitioned due to excessive collision.

NWAY (has Auto-Negotiation ability) **mode:** For UTP with auto-negotiation ability, pin GxEnFC/GyEnFC/P4EnFC is used for Full duplex. But the result of auto-negotiation may be half duplex. So for UTP with auto-negotiation ability, the half duplex back pressure flow control is controlled by the EnANEG_BKPRS pin strap upon hardware reset.

Force mode: For UTP without auto-negotiation ability and 100Base-FX, the operation mode can be forced as half duplex. So the half duplex back pressure flow control can be forced enable at the RTL8305SB side by pin GxEnFC/GyEnFC/P4EnFC in group basis upon reset.

Note: For the RTL8305SB, the name of the EnBkPrs pin on the RTL8305S is replaced by EnANeg_BkPrs.

Note: For the RTL8305SB, the function of the ENFCTRL on the RTL8305S is replaced by 3 pins: GxEnFC, GyEnFC, P4EnFC.

7.1.6 Address Search, Learning and Aging

When a packet is received, the RTL8305SB will first use the least 10 bits of the destination MAC address to index the 1024-entry look-up table and at the same time will compare the destination MAC address with the contents of the 16-entry CAM. If the indexed entry is valid or the CAM comparison is match, this received packet will be forwarded to the corresponding destination port. Otherwise, the RTL8305SB will broadcast the packet. This is called 'search'.

The RTL8305SB then extracts the least 10 bits of source MAC address to index the 1024-entry look-up table. If this indexed entry is empty, it will record the source MAC address and update switching information. If this is an occupied entry with the same switching information, it will update the entry with new information. This is called 'learning'. If the indexed location has been occupied by different MAC address (hash collision), the new source MAC address will be recorded into the 16-entry CAM. The 16 entry CAM can reduce the address hash collision and will improve the switch network performance.

Address aging function is used to keep the contents of the address table correct in a dynamic network topology. The look-up engine will update time stamp information of an entry whenever the corresponding source MAC address appears. An entry will be invalid (aging out) if it's time stamp information is not refreshed by the address learning process during the aging time period. Aging time of the RTL8305SB is around 200 to 300 seconds.

7.1.7 Address Direct Mapping Mode

The RTL8305SB uses the least 10 bits of the MAC address to index the 1024-entry look-up table. For example: the index of MAC address "12 34 56 78 90 ab" will be 0ab.

7.1.8 Half Duplex Operation

In half duplex mode, the CSMA/CD media access method is the means by which two or more stations share a common transmission medium. To transmit, a station waits (defers) for a quiet period on the medium (that is, no other station is transmitting) and then sends the intended message in bit-serial form. If, after initiating a transmission, the message collides with that of another station, then each transmitting station intentionally transmits for an additional predefined period to ensure propagation of the collision throughout the system. The station remains silent for a random amount of time (backoff) before attempting to transmit again.

When a transmission attempt has terminated due to a collision, it is retried until it is successful. The scheduling of the retransmissions is determined by a controlled randomization process called "truncated binary exponential backoff". At the end of enforcing a collision (jamming), the switch delays before attempting to retransmit the frame. The delay is an integer multiple of slotTime (512 bit times). The number of slot times to delay before the n^{th} retransmission attempt is chosen as a uniformly distributed random integer r in the range:

$$0 \leq r < 2^k$$

where

$k = \min(n, \text{backoffLimit})$, The 802.3 defines the backoffLimit as 10.

7.1.9 Inter-Frame Gap

The Inter-Frame Gap is 9.6μs for 10Mbps Ethernet and 960ns for 100Mbps Fast Ethernet.

7.1.10 Illegal Frame

Illegal frames such as CRC error packets, runt packets (length < 64 bytes) and oversize packets (length > maximum length) will be discarded.

7.2 Physical Layer Functional Overview

7.2.1 Auto-Negotiation for UTP

The RTL8305SB obtains the states of duplex, speed and flow control ability through the auto-negotiation mechanism defined in IEEE802.3u specifications for each port in UTP mode. During auto-negotiation, each port advertises its ability to its link partner and compares ability with those received from its link partner. By default, the RTL8305SB advertises full capabilities (100Full, 100Half, 10Full, 10Half) together with flow control ability.

7.2.2 10Base-T Transmit Function

The output 10Base-T waveform is Manchester-encoded before it is driven into the network media. The internal filter shapes the driven signals to reduce EMI emission, eliminating the need for an external filter.

7.2.3 10Base-T Receive Function

The Manchester decoder converts the incoming serial stream to NRZ data when the squelch circuit detects the signal level is above squelch level.

7.2.4 Link Monitor

The 10Base-T link pulse detection circuit always monitors the RXIP/RXIN pins for the presence of valid link pulses. Auto-polarity is implemented to correct the detected reverse polarity of RXIP/RXIN signal pairs.

7.2.5 100Base-TX Transmit Function

The 100Base-TX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ/NRZI conversion, and MLT3 encoding. The 5-bit serial data stream after 4B/5B coding is then scrambled as defined by the TP-PMD Stream Cipher function to flatten the power spectrum energy such that EMI effects can be reduced significantly.

The scrambled seed is unique for each port based on PHY addresses. The bit stream after scrambler is driven into network media in the form of MLT-3 signaling. The multi-level signaling technology moves the power spectrum energy from high frequency to low frequency, which also benefits EMI emission.

7.2.6 100Base-TX Receive Function

The receive path includes a receiver composed of adaptive equalizer and DC restoration circuits to compensate for the incoming distortion MLT-3 signal, MLT-3 to NRZI, NRZI to NRZ converter to convert analog signal to digital bit-stream, and PLL circuit to clock data bit exactly with minimum bit error rate. De-scrambler, 5B/4B decoder and serial-to-parallel conversion circuits are followed. Finally, the converted parallel data is fed into the MAC.

7.2.7 100Base-FX

All ports support 100Base-FX, which shares pins with UTP (TX+/-/RX+/-) and need no SD+/- pins (Realtek patent). The 100Base-FX can be forced as half or full duplex with optional flow control ability. Hint: The 100Base-FX does not support Auto-Negotiation according to IEEE 802.3u. In order to operate correctly, both sides of the connection should set the same duplex and flow control ability. A scrambler is not needed in 100Base-FX. As compared to common 100Base-FX applications, the RTL8305SB lacks of a pair of differential SD (signal detect) signals to achieve link monitoring function (Realtek patent), which significantly reduces the pin count.

7.2.8 100Base-FX Transmit Function

In 100Base-FX transmit, di-bits of TXD are processed as 100Base-TX except without scrambler before NRZI stage. Instead of converting to MLT-3 signals as in 100Base-TX, serial data stream is driven out as NRZI PECL signals, which enter the fiber transceiver in differential-pairs form. The fiber transceiver should be available working in a 3.3V environment. Refer to fiber application section.

Parameter	Symbol	Min	Max	Unit
PECL Input High Voltage	Vih	Vdd-1.16	Vdd-0.88	V
PECL Input Low Voltage	Vil	Vdd-1.81	Vdd-1.47	V
PECL Output High Voltage	Voh	Vdd-1.02		V
PECL Output Low Voltage	Vol		Vdd-1.62	V

PECL DC characteristics

7.2.9 100Base-FX Receive Function

Signals are received through PECL receiver inputs from fiber transceiver, and directly passed to clock recovery circuit for data/clock recovery. Scrambler/de-scrambler is bypassed in 100Base-FX.

7.2.10 100Base-FX Far-End-Fault-Indication (FEFI)

MII Reg.1.4 (Remote Fault) is the FEFI bit for ports when 100FX is enabled, which indicates that a FEFI has been detected. FEFI is an alternative in-band signaling which is composed of 84 consecutive '1' followed by one '0'. From the view of the RTL8305SB, when this pattern has been detected three times, Reg.1.4 is set, which means the transmit path (Remote side's receive path) has problems. On the other hand, to send FEFI stream pattern, 1 condition need to be satisfied. The incoming signal failed in causing link OK will force the RTL8305SB to start sending this pattern, which in turn causes the remote side detecting Far-End-Fault. This means that the receive path has a problem from the view of the RTL8305SB. The FEFI mechanism is used only in 100Base-FX.

7.2.11 Reduced Fiber Interface

The RTL8305SB ignores the underlying SD signal of the fiber transceiver to complete link detection and connection. This is achieved by monitoring RD signals from the fiber transceiver and checking if any link integrity events are met. This significantly reduces pin-count, especially for high-port PHY devices. This is a Realtek patent-pending technology and available only with Realtek product solutions.

7.2.12 Power Saving Mode

The RTL8305SB implements power saving mode on per port base. A port automatically enters power saving mode 10 seconds after the cable is disconnected from it. Once a port enters power saving mode, it transmits normal link pulses only on its TXOP/TXON pins and continues to monitor the RXIP/RXIN pins to detect any incoming signals, which might be the 100Base-TX MLT-3 idle pattern, 10Base-T link pulses or Auto-Negotiation's FLP (fast link pulses). After it detects any incoming signals, it wakes up from the power saving mode and operates in the normal mode according to the result of connection.

7.2.13 Reg0.11 Power Down Mode

The RTL8305SB implements power down mode on a per port basis. Setting MII Reg.0.11 forces the corresponding port of the RTL8305SB to enter power down mode, which disables all transmit/receive functions, except SMI (MDC/MDIO management interface).

7.2.14 Crossover Detection and Auto Correction

During the link setup phase, the RTL8305SB checks if it receives active signals on every port to determine if connection can be established. In case the receiver data pin pair is connected to receiver pin pair of the peer device and vice versa, the RTL8305SB will automatically change its configuration to swap receiver data pins with transmitter data pins. In other words, the RTL8305SB can adapt automatically to a peer device's configuration. If a port is connected to a PC or NIC with MDI-X interface with a crossover cable, the RTL8305SB will reconfigure the port to provide the MDI-X interface to ensure proper connection. This will effectively replace the DIP switch commonly used for reconfiguring a port on a hub or switch.

By pulling-up EN_AUTOXOVER, the RTL8305SB can identify the type of connected cable to adjust its port as MDI or MDIX. When switching to MDI mode, the RTL8305SB uses TXOP/N as transmit pairs; when switching to MDIX mode, the RTL8305SB uses RXIP/N as transmit pairs. The same for receive pairs. This function is port-based implemented. Pulling-down EN_AUTOXOVER will disable this function and the RTL8305SB operates in MDI mode, in which TXOP/N represents transmit pairs and RXIP/N represents receive pairs.

According to the IEEE standard, the forced mode 100M ports with autoxover have link issues with NWAY (Auto-Negotiation) ports. It is recommended to *not* to use autoxover for forced 100M.

7.2.15 Polarity Detection and Correction

For better noise immunity and lower interference to ambient devices, the Ethernet electrical signal on a twisted pair cable is transmitted in differential forms. That is, the signal is transmitted on two wires for each direction with inverse polarities (+/-). If wiring on the connector is faulty or a faulty transformer is used, the two inputs to a transceiver may carry signals with opposite but incorrect polarities. As a direct consequence, the transceiver will not work properly.

When the RTL8305SB operates in 10Base-T mode, it automatically reverses the polarity of its two receiver input pins if it detects that the polarities of the incoming signals on the pins is incorrect. However, this feature is unnecessary when the RTL8305SB is operating in 100Base-TX mode.

7.3 Advanced Functional Overview

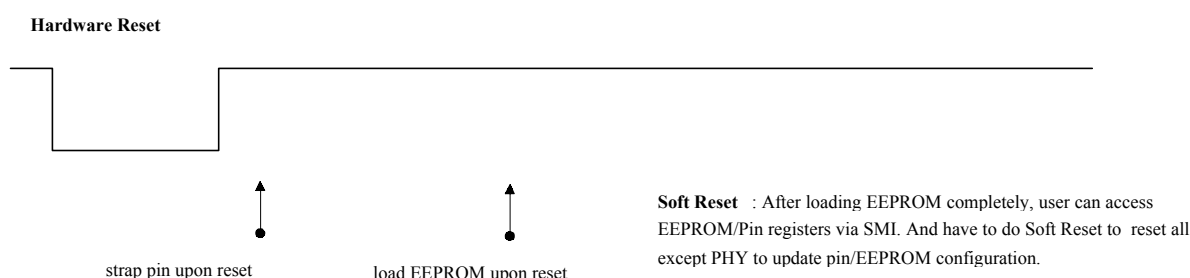
7.3.1 Reset

The whole or part of the RTL8305SB is initialized depending on the reset type. There are several ways to reset RTL8305SB: hardware reset for whole chip by pin RESET#, soft reset for all except PHY by register SoftReset, and PHY software reset for each PHY by register reset.

Hardware Reset: pin RESET# = 0 (asserted at least 1ms) to 1. The RTL8305SB will reset the whole chip then get initial value from pins and serial EEPROM.

Soft Reset: Write bit15 of Reg16 of PHY3 as 1. The RTL8305SB will reset all except PHY and will not load EEPROM and Pin Registers with serial EEPROM and Pins. The SoftReset, EEPROM and Pin registers are designed to provide a convenient way for users who want to use SMI to change the configuration. After changing the EEPROM or Pin registers via SMI, the external device has to perform a soft reset in order to update the configuration.

PHY software reset: Write bit15 of Reg0 of some PHY as 1. The RTL8305SB will then reset this PHY.



Some setting values for operation modes are latched from those corresponding mode pins at the end of hardware reset. Upon reset is defined as a short time after at the end of a hardware reset. Then other advanced configuration parameters may be latched from serial EEPROM if pin EnEEPROM=1.

7.3.2 Setup and Configuration

The RTL8305SB can be configured easily and flexibly by hardware pins upon reset, optional serial EEPROM upon reset, and internal registers (including PHY registers for each port and MAC register for global) via SMI (serial management interface: MDC/MDIO, also known as MII Management Interface). There are three ways to configure: 1) Only hardware pins for normal switch application; 2) Hardware pins and serial EEPROM for advanced switch application; 3) Hardware pins and internal registers via SMI for application with processor.

Four types of pins, which all have internal pull-high resistors, are used for configuration: 1) Input pins used for strapping only upon reset and are of no use after reset; 2) Input pins (P4DUPSTA/P4FULL, P4SPDSTA/P4SPD100, P4FLCTRL/P4EnFC) used for strapping upon reset and used as input pins after reset. For example, pin P4DUPSTA/P4FULL is used as P4FULL upon reset for PHY of Port 4 UTP/FX mode and used as P4DUPSTA for MAC of other mode after reset; 3) Input/Output pins (MTXD[3:2]/PRXD[3:2]/P4IRTag[1:0], MTXD[1:0]/PRXD[1:0]/LEDMode[1:0]) used for strapping upon reset and used as output pins after reset; 4) Input/Output pins (all LEDs) used for strapping upon reset and used as LED indicator pins after reset. The LED statuses are represented as active-low or high depending on input strapping, except Bi-color Link/Act in Bi-color LED mode, whose polarity depends on Spd status.

The Pins with default value=1 are internal pull-high and use I/O pad. So they can be left floating to choose input value as high but should not be connected to GND without a pull-down resistor.

The serial EEPROM, which shares two pins (SCL_MDC and SDA_MDIO) with SMI, is optional for advanced configuration. SCL_MDC and SDA_MDIO are tri-state during hardware reset (pin RESET#=0). The RTL8305SB will try to automatically find the serial EEPROM upon reset only if pin EnEEPROM is 1. Because the pin SDA_MDIO is pulled up by an external resistor. If and only if the NoEEPROM of serial EEPROM (bit 0 of the first byte) is 0, the RTL8305SB will load all contents of the serial EEPROM into internal registers. Otherwise, the RTL8305SB will use the default values for the internal.

Internal registers can still be accessed after reset via SMI (pin SCL_MDC and SDA_MDIO). Serial EEPROM signals and SMI signals should not exist in the same time. In order to use the SMI to change configuration flexibly, internal registers include content of some pins and all serial EEPROM: Pin register and EEPROM register. Those registers do not work in real time. Soft Reset is necessary after changing the EEPROM or Pin registers.

7.3.5 SMI

The SMI (Serial Management Interface) is also known as the MII Management Interface, which consists of two signals (MDIO and MDC), and allows external devices with SMI master mode (MDC is output) to control the state of the PHY and internal registers (SMI slave mode: MDC is input). MDC is an input clock for the RTL8305SB to latch MDIO on its rising edge. The clock can run from DC to 25MHz. MDIO is a bi-directional connection used to write data to, or read data from the RTL8305SB. The PHY address is from 0 to 4.

SMI Read/Write Cycles								
	Preamble (32 bits)	Start (2 bits)	OP Code (2 bits)	PHYAD (5 bits)	REGAD (5 bits)	Turn Around (2 bits)	Data (16 bits)	Idle
Read	1.....1	01	10	AAAAA	RRRRR	Z0	D.....D	Z*
Write	1.....1	01	01	AAAAA	RRRRR	10	D.....D	Z*

Z*: high-impedance. During idle time, MDIO state is determined by an external 1.5K Ω pull-up resistor.

The RTL8305SB supports Preamble Suppression, which allows the MAC to issue Read/Write Cycles without preamble bits. However, for the first cycle of MII management after power-on reset, a 32-bit preamble is needed.

To guarantee the first successful SMI transaction after power-on reset, external device should delay at least 1sec to issue the first SMI Read/Write Cycle relative to the rising edge of reset.

7.3.6 Head-Of-Line Blocking

The RTL8305SB incorporates an advanced mechanism to prevent Head-Of-Line blocking problem when flow control is disabled. When the flow control function is disabled, the RTL8305SB will first check the destination address of the incoming packet. If the destined port is congested, the RTL8305SB will discard this packet to avoid the blocking of the next packet, which is going to a non-congested port.

7.3.7 802.1Q Port Based VLAN

The RTL8305SB supports five VLAN groups: VLAN A, B, C, D, and E. Two association ingress rules are provided to map a frame to a given VLAN: port based and tagged-VID (VLAN Identifier).

Port based VLAN mapping is the simplest implicit mapping rule. A frame belongs to a VLAN is based on the index of the port which it came from. P0VLANIndex[2:0], P1VLANIndex[2:0], P2VLANIndex[2:0], P3VLANIndex[2:0], and P4VLANIndex[2:0] are used for each port as the distinguishing characteristic of a VLAN. Using the default value as an example, P0VLANIndex[2:0]=0b000 means port 0 belongs to VLAN A. P1VLANIndex[2:0]=0b001 means port 1 belongs to VLAN B. P2VLANIndex[2:0]=0b010 means port 2 belongs to VLAN C. P3VLANIndex[2:0]=0b011 means port 3 belongs to VLAN D. P4VLANIndex[2:0]=0b100 means port 4 belongs to VLAN E.

The 12-bit tagged-VID is the explicit indication of the frame's VLAN association. A total of 4094 values are possible. The value of all ones (0xFFF) is reserved and currently unused. The value of all zero (0x000) indicates a priority tag. A priority tagged frame is treated the same as an untagged frame. VIDA[11:0], VIDB[11:0], VIDC[11:0], VIDD[11:0], and VIDE[11:0] are used as the distinguishing characteristic for each VLAN. For example, VIDA[11:0]=0x001 means frame with tagged-VID=0x001 belongs to VLAN A. VIDB[11:0]=0x002 means frame with tagged-VID=0x002 belongs to VLAN B. VID filed have no default values in the register, users must assign them in the serial EEPROM or register via SMI for the Tagged-VID application.

Byte0~5	Byte6~11	Byte12~13	Byte14.7~14.5	Byte14.4	Byte14.3~15.0
DA	SA	81-00	User-Priority (0~3:Low-pri ; 4~7: High-pri)	CFI 0	VID

Table 1: 802.1Q VLAN tag frame format

For the egress rule, each VLAN has a Member Set field. Member set of a VLAN indicates which ports belong to this VLAN. Ports in the member set for a given VLAN can be expected to receive and transmit frames belonging to that VLAN; ports not in the member set should generally not be receiving and/or transmitting frames for that VLAN. For the RTL8305SB, the member set for a VLAN can be configured by serial EEPROM or register via SMI. Using the default value as an example, MemberA[4:0]=10001 means port 4 and 0 are members of VLAN A. MemberB[4:0]=10010 means port 4 and 1 are members of VLAN B. MemberC[4:0]=10100 means port 4 and 2 are members of VLAN C. MemberD[4:0]=11000 means port 4 and 3

are members of VLAN D. MemberE[4:0]=11111 means all ports are members of VLAN E.

When the serial EEPROM does not exist and pin DisVLAN=1, the RTL8305SB will disable the VLAN function. The SMI can be used to update the registers then do SoftReset to enable and change the VLAN.

When the serial EEPROM does not exist and pin DisVLAN=0, the RTL8305SB will use the default values for the internal register to provide a useful Port based VLAN mapping: P0VLANIndex[2:0]=0b000, P1VLANIndex[2:0]=0b001, P2VLANIndex[2:0]=0b010, P3VLANIndex[2:0]=0b011, and P4VLANIndex[2:0]=0b100; MemberA[4:0]=10001, MemberB[4:0]=10010, MemberC[4:0]=10100, MemberD[4:0]=11000, MemberE[4:0]=11111. Port 0 to 3 will be set at different VLAN and share the overlapping port 4. User can use SMI to update the register then do SoftReset to change the VLAN configuration.

	PortVLANIndex	Member A	Member B	Member C	Member D	Member E
Port 0	A	V				V
Port 1	B		V			V
Port 2	C			V		V
Port 3	D				V	V
Port 4	E	V	V	V	V	V

Table 2: 802.1Q VLAN default setup

When an EEPROM is used, the RTL8305SB will ignore the pin and will load the initial value of the internal registers with the EEPROM values.

When register DisVLAN=1, the RTL8305SB will disable the VLAN function. When register DisVLAN=0, RTL8305SB will use the values of internal register to determine the VLAN mapping.

If the 802.1Q tagged-VID Aware function is enabled (DisTagAware=0), the RTL8305SB will check the tagged VID of the received frame to do the VLAN classification. The RTL8305SB will use tagged-VID VLAN mapping for tagged frames and will use Port Based VLAN mapping for untagged and priority-tagged frames. For example, if a tagged frame with tagged-VID=0x001 is received from port1, it will be classified as VLAN A when VIDA[11:0]=0x001. If the tagged-VID Aware function is disabled, the RTL8305SB will always use Port Based VLAN mapping. For example, if a tagged frame with tagged-VID=0x001 is received from port1, it will be classified as VLAN B when P1VLANIndex[2:0]=0b001.

The Acceptable Frame Type of Ingress Process can be “Admit All” or “Admit All Tagged”. When DisTagAdmitCtrl=1, the Acceptable Frame Type of Ingress Process will be “Admit All” and the RTL8305SB will receive all frames. When DisTagAdmitCtrl=0, the Acceptable Frame Type of Ingress Process will be “Admit All Tagged”. The RTL8305SB will receive only the VLAN-tagged frame and drop all other untagged frames and priority tagged (VID=0) frames.

When DisMemFilter=1, the VLAN Ingress Member set filtering is disabled. The RTL8305SB will not discard any frames associated with a VLAN for which that port is not in the member set. If the VLAN Ingress Member set filtering is enabled by setting DisMemFilter=0, RTL8305SB will discard any frame associated with a VLAN for which that port is not in the member set. For example, RTL8305SB will drop the frame with tagged-VID=0x002 received from port0 when DisVLAN=0, DisTagAware=0, DisMemFilter=0, VIDB[11:0]=0x002, and MemberB[4:0]=0b10010 (Port4 and 1 belong to the member set of VLAN B).

Two options can be used for special application. ARP VLAN: If DisARP=0, ARP broadcast frames (the RTL8305SB only checks frames with DID=all F, Type=0806) will be broadcast to all VLAN. Otherwise, ARP broadcast frames, like other frames, can only be forwarded to the same VLAN. Leaky VLAN: If DisLeaky=0, unicast frames, not including broadcast and multicast frames, can traverse VLANs. Otherwise, unicast frames can only be forwarded to the same VLAN, like broadcast and multicast frames.

7.3.8 QoS Function

The RTL8305SB can recognize the QoS priority information of the incoming packets to give a different egress service priority. The RTL8305SB identifies the packets as high priority based on several types of QoS priority information that based on: 1) Port based priority; 2) 802.1p/Q VLAN priority tag; 3) TCP/IP's TOS/DiffServ (DS) priority field. These types of QoS are selected by hardware pins DisPortPri[4:0], DisTagPri and DisDSPri respectively upon reset or internal registers via SMI after reset.

There are 2 priority queues, a high-priority queue and a low-priority queue, supported by the RTL8305SB to buffer high and low priority frames. The queue service rate is based on the Weighted Round Robin algorithm, the packet based service weight ratio of high-priority queue and low-priority queue can be set as 4:1, 8:1, 16:1 or "Always high priority first" by hardware pins QWeight[1:0] upon reset or internal register via SMI after reset.

When Port based priority is applied, any packets received from the high priority port, which is set by DisPortPri[4:0], will be sent to the high priority queue of the destination port.

When 802.1p VLAN tag priority applied, the RTL8305SB can recognize the 802.1Q VLAN tag frames and extract the 3-bit User_Priority information from the VLAN tag. The RTL8305SB sets the threshold of User_Priority as 3. Therefore, VLAN tagged frames with User_Priority value = 4~7 will be treat as high priority frames, other User_Priority values (0~3) as low priority frames (follows 802.1p standard).

When TCP/IP's TOS/DiffServ(DS) based priority is applied, the RTL8305SB can recognize TCP/IP Differentiated Services Codepoint (DSCP) priority information from the DS-field defined on RFC2474. The DS field byte for the IPv4 is Type-of-Service (TOS) octet and for IPv6 is Traffic-Class octet. The recommended DiffServ Codepoint is defined in RFC2597 to classify the traffic into different service classes. The RTL8305SB can extract the codepoint value of DS-field from IPv4 and IPv6 packets, and identify the priority of the incoming IP packet follows the definition as bellow:

High priority: whose DS-field = (EF ,expected forwarding:) 101110;
 (AF, Assured Forwarding:) 001010; 010010; 011010; 100010
 (Network Control:) 110000 and 111000.

Low priority: whose DS-field = others values.

The VLAN tagged frame and 6-bit DS-field in IPv4 and IPv6 frame format are shown bellow:

6 bytes	6 byte	2 byte	3 bits	
DA	SA	81-00	User-Priority (0~3:Low-pri ; 4~7: High-pri)	----

Table 3: 802.1Q VLAN tag frame format

6 bytes	6 byte	4 byte	2 byte	4 bits	4 bit	6 bits	
DA	SA	802.1Q Tag (optional)	08-00	Version IPv4= 0100	IHL	TOS[0:5] = DS-field	----

6 bytes	6 byte	4 byte	2 byte	4 bits	6 bits	
DA	SA	802.1Q Tag (optional)	08-00	Version IPv6= 0110	Traffic Class [0:5] =DS-field	----

Table 4: IPv4/6 frame format

Note: IPv6 refer to rcf2460

The RTL8305SB can automatically turn off 802.3x flow control and Back pressure flow control for 1~2 sec whenever the port receives VLAN-tag or TOS/DS high priority frames, the flow control is re-enabled when no priority frame is received during a 1~2 sec duration. The hardware pin DisFCAutoOff upon reset or internal register via SMI after reset can enable this auto-turn off function.

7.3.9 Insert/Remove VLAN Priority Tag

When QoS function is enabled, a tag can be inserted or removed on a per output port basis. The RTL8305SB will insert VLAN priority-tag (VID=0x000) for untagged frames only, or remove a tag for all types tagged frames. Port 4 can use two strapping pins upon reset or internal registers via SMI after reset to set Insert/Remove function. Other ports can use a serial EEPROM upon reset or internal registers via SMI after reset to set this function. For example: When P0IRTag[1:0]=10, the RTL8305SB will insert priority tag for untagged frame from Output High Queue (user priority field=0b111, CFI=0, VID=0x000) of Port0 and Low Queue of Port0 (user priority field=0b000, CFI=0, VID=0x000). When P0IRTag[1:0]=01, the

RTL8305SB will insert priority tag only from Output High Queue of Port0 (user priority field=0b111, CFI=0, VID=0x000).

If the tag removed frame is less than 64 bytes, it should add PAD with a "0x20" pattern at the packet before CRC field to fit 64-byte min packet length of IEEE 802.3 spec. The RTL8305SB will recalculate the FCS if the frame had been changed.

7.3.10 Filtering/Forwarding Reserved Control Frame

The RTL8305SB supports the ability to forward or drop the frames of the 802.1D specified reserved group MAC addresses (control frames): 01-80-C2-00-00-03 to 01-80-C2-00-00-0F.

Address	Use	Action
01-80-C2-00-00-00	Bridge Group Address	Forward to all ports
01-80-C2-00-00-01	Pause Control Frame	Drop Frame
01-80-C2-00-00-02		Drop Frame
01-80-C2-00-00-03 to 01-80-C2-00-00-0F	Reserved	Forward to all ports
Any other multicast Address	-	Forward to all ports

Table 5: EnForward=1: same as RTL8305S

Address	Use	Action
01-80-C2-00-00-00	Bridge Group Address	Forward to all ports
01-80-C2-00-00-01	Pause Control Frame	Drop Frame
01-80-C2-00-00-02		Drop Frame
01-80-C2-00-00-03 to 01-80-C2-00-00-0F	Reserved	Drop Frame
Any other multicast Address	-	Forward to all ports

Table 6: EnForward=0

7.3.11 Broadcast Storm Control

According to the latched value of DISBRDCTRL pin upon reset, the RTL8305SB determines whether or not to proceed with broadcast storm control. Once enabled (DISBRDCTRL=0), after consecutive 64 broadcast (DID=FFFF-FFFF-FFFF) packets are received by one port, the incoming consecutive broadcast packets during around 800ms time window of this port will be discarded. Any non-broadcast packet can reset the time window and broadcast counter such that the scheme restarts. It is per port based. Note2: Trigger condition: consecutive 64 DID = FFFF-FFFF-FFFF packets. Release condition: receive non-broadcast packet on or after 800ms.

7.3.12 Broadcast In/Out Drop

If some destination ports are blocking and the buffer is full, broadcast frames should be dropped according to configuration. Input Drop: do not forward to any port and drop the frame directly. Output Drop: forward only to non-blocking ports (Broadcast becomes multicast).

1. Broadcast packet from Port0
2. Buffer of Port4 is full, others are not full

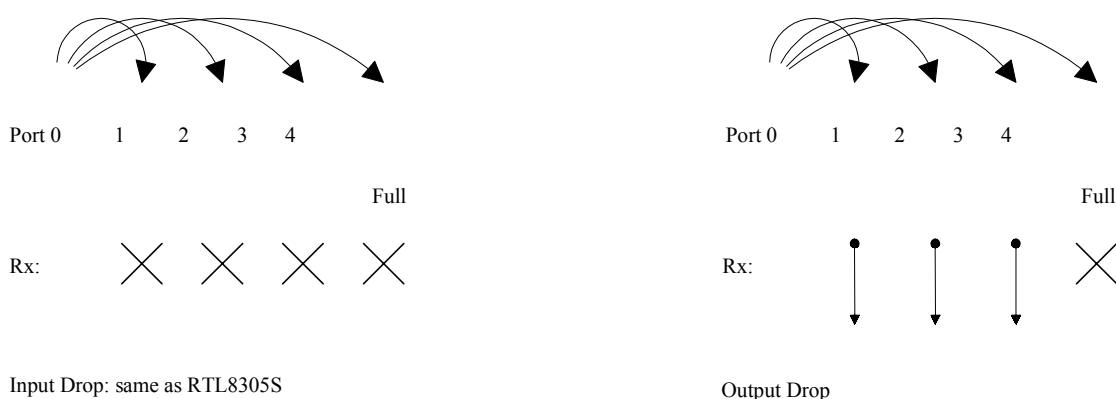


Figure 1: Input Drop v.s. Output Drop

7.3.13 Loop Detection

Loops should be avoided between switch applications. The simplest loop as shown below results in: 1) Unicast frame duplication; 2) Broadcast frame multiplication; 3) Address table nonconvergence. Frame may be transmitted from Switch1 to Switch2 via Link1, then return to Switch1 via Link2.

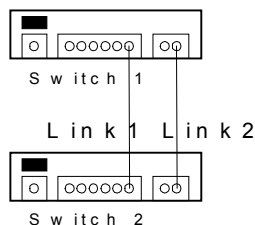


Figure 2: Example of Loop

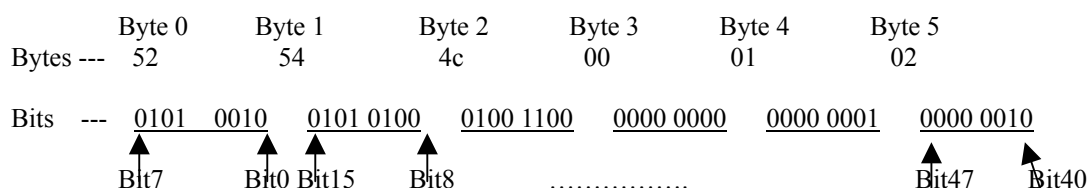
When the loop detection function is enabled by setting DisLoop=0 in EEPROM or an internal register, the RTL8305SB periodically sends out a broadcast 64-byte packet every 3~5 minutes and automatically detect whether if there is a network loop (or bridge loop) existence. The LoopLED# will be ON (active low or high) to indicate that a loop exists. The LED goes out by unplugging both of the RTL8305SB ports of the loop. The Loop frame length is 64 bytes and its format as shown below.

Table 7: Loop frame format

FFFF FFFF FFFF	SID	8899	0300	000...0000	CRC
----------------	-----	------	------	------------	-----

In order to achieve loop detection, each switch device needs different SID (Source MAC address Identifier) for detection. So that, the different EtherID is needed for each device when the loop detection function is enabled. If the EEPROM is not used, a unique EtherID via SMI should be assigned after reset and the default EtherID (0x5254 4c83 05b0) should not be used.

Ethernet MAC address byte (bit) ordering: For example, MAC address is 52 54 4c 00 01 02. According to 802.3, 0x52 is byte 0, 0x54 is byte 1, 0x02 is byte 5,



The order of bit transmission is low-order bit first. From bit0 to bit47:

0100 1010 0010 1010 0011 0010 0000 0000 1000 0000 0010 0000

7.3.14 MAC Loopback return to External

Each port supports loopback of the MAC (return to external device) function for diagnostic purposes. For example: If the internal register DisP4LoopBack=0, the RTL8305SB will “forward local and broadcast packets from the input of Port4 to output of Port4” and “drop unicast packets from the input of Port4”. The other port still can forward broadcast or unicast packets to port4. Example2: If the internal register DisP3LoopBack=0, the RTL8305SB will “forward local and broadcast packets from the input of Port3 to output of Port3” and “drop unicast packets from input of Port3”. The other port still can forward broadcast or unicast packets to port3.

This is especially useful for router applications to perform mass production tests. This function does nothing with PHY type (GxMode/GyMode/P4Mode[1:0]) and can be done on each mode. Below are two examples: In Example 1, the external device (CPU) is connected to MII or SNI interface of Port4. In Example 2, the external device (CPU) does not have an MII or SNI interface, so it can use the PCI interface to connect RTL8139 to the UTP of Port4.

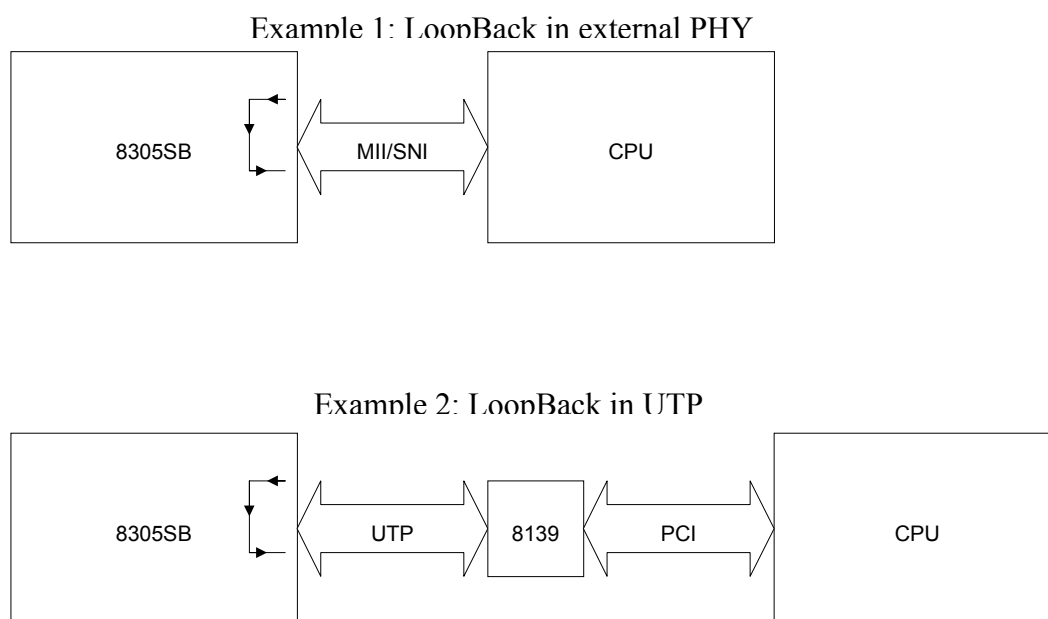


Figure 3: Port4 Loopback

7.3.15 Reg0.14 PHY Loopback return to Internal

The loopback mode of the PHY (return to internal MAC) can be enabled on a per port base by setting MII Reg.0.14 as 1. In Reg0.14 loopback mode, TXD of PHY is transferred directly to RXD of PHY with TXEN changed to CRS_DV and returns to MAC via internal MII. The data stream coming from the MAC will not egress to the physical medium and incoming data stream from the network medium will be blocked in this mode. The packets will be looped back in 10Mbps full duplex or 100Mbps at full duplex mode. This function is especially useful for diagnostic purposes. For example, a NIC can be used to send broadcast frame into port 0 of the RTL8305SB and set Port1 as Reg0.14 Loopback. The frame will be looped back to port 0, so the received packet count can be checked to verify that the switch device is good. In this example, port 0 can be 10M or 100M and full or half duplex.

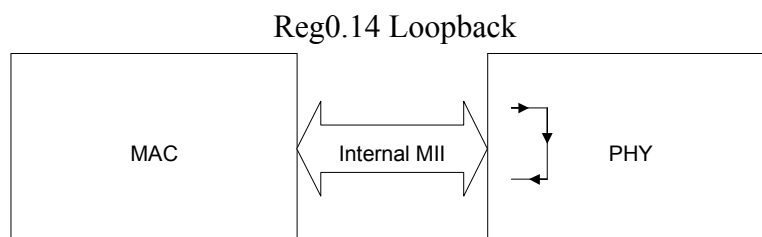


Figure 4: Reg0.14 Loopback

7.3.16 LED

The RTL8305SB supports four parallel LEDs for each port, and two special LEDs (SELMII MAC# and LOOPLED#). Each port has four LED indicator pins. Each pin may have different indicator meaning set by pins LEDMode[1:0], refer to the pin descriptions for details. Upon reset, the RTL8305SB supports diagnostics of chip reset and LED functions by blinking all LEDs once for 320ms. This function can be disabled by asserting EN_RST_LINK to 0. LED_BLINK_TIME determines LED blinking period for activity and collision, with 1 = 43ms and 0 = 120ms. The parallel LEDs corresponding to port 4 can be three-stated (disable LED functions) for MII port application by setting ENP4LED in EEPROM as 0. In UTP application, this bit should be 1 to drive LEDs of port 4.

All LED pins are dual function pins: input operation for configuration upon reset, and output operation for LED after reset. If the pin input is floating upon reset, the pin output is active low after reset. Otherwise, if the pin input is pulled down upon reset, the pin output is active high after reset. Exception: Bi-color Link/Act mode of pin LED_ADD[4:0] when LEDMode[1:0]=10. Below shows an example circuits for LEDs. The typical values for pull-down resistors are 10K Ω .

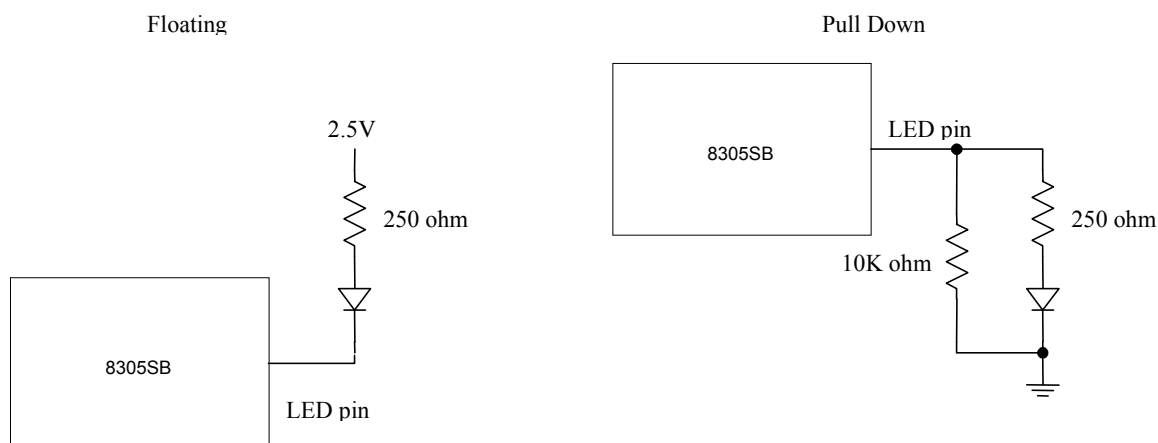


Figure 5: Floating and Pull-Down of LED pins

For two pin Bi-color LED mode (LEDMode[1:0]=10), Bi-color Link/Act (pin LED_ADD) and Spd (pin LED_SPD) can be used for one Bi-color LED package, which is a single LED package with two LEDs connected in parallel with opposite polarity. When LEDMode[1:0]=10, the active status of LED_ADD is opposite with LED_SPD, does nothing with input upon reset.

Indication	Bi-Color state	Spd:Input=Floating, Active Low. Bi-color Link/Act: the active status of LED_ADD is opposite with LED_SPD, does nothing with input upon reset.		Spd:Input=Pull-down, Active High. Bi-color Link/Act: the active status of LED_ADD is opposite with LED_SPD, does nothing with input upon reset.	
		Spd	Link/Act	Spd	Link/Act
No Link	Both Off	1	1	0	0
100M Link	Green On	0	1	1	0
10M Link	Yellow On	1	0	0	1
100M Act	Green Flash	0	Flash	1	Flash
10M Act	Yellow Flash	1	Flash	0	Flash

Table 8: Truth table of Spd and Bi-color Link/Act

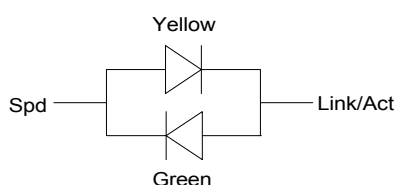


Figure 6: Two pin Bi-color LED for SPD floating or Pull-high

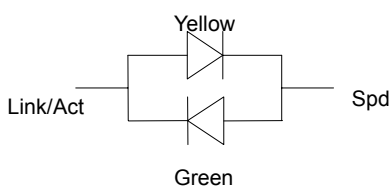


Figure 7: Two pin Bi-color LED for SPD Pull-down

7.3.17 2.5V Power Generation

The RTL8305SB can use a PNP transistor to generate 2.5V from a 3.3V power supply. This 2.5V is used for the digital core and analog receiver circuits. Do not use one PNP transistor for more than one RTL8305SB chip, even if the rating is enough: Use one transistor for each RTL8305SB chip.

Do not connect any inductor (bead) directly between the collector of PNP transistor and VDDAL. This will affect the stability of the 2.5V power significantly if the inductor (bead) exists.

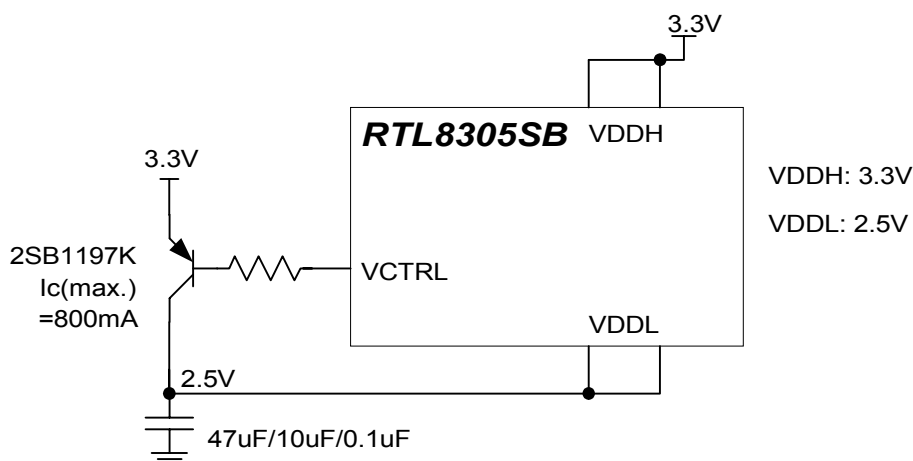


Figure 8: Use PNP Transistor to transform 3.3V into 2.5V

Parameter	Symbol	Limits	Unit
Collector-base voltage	VCBO	-40	V
Collector-emitter voltage	VCEO	-32	V
Emitter-base voltage	VEBO	-5	V
Collector current	IC	-0.8	A(DC)
Collector power dissipation	PC	0.2	W
Junction temperature	Tj	150	°C
Storage temperature	Tstg	-55~+150	°C

Table 9: Example of Power Transistor 2SB1197K

Absolute maximum ratings (Ta=25°C)

For more information, refer to <http://www.rohm.com>

7.3.18 Crystal/Oscillator

- The frequency is 25Mhz. The maximum Frequency Tolerance is +/- 100ppm. The maximum Jitter is 150 ps Peak to Peak.

8. Serial EEPROM Description

Unused Registers and bits are reserved for future or internal use, and should use the default value.

Name	Reg.bit	Description	Default
Internal	0.7	Internal use only	1
Internal	0.6	Internal use only	1
Internal	0.5	Internal use only	1
Internal	0.4	Internal use only	1
Internal	0.3	Internal use only	1
Internal	0.2	Internal use only	1
Internal	0.1	Internal use only	1
NoEEPROM	0.0	No EEPROM: 1: EEPROM does not exist. 0: EEPROM exist.	0
Internal	1.7	Internal use only	1
DisLoop	1.6	Disable Loop Detection Function: 1: Disable Loop Detection function. 0: Enable Loop Detection function.	1
Internal	1.5	Internal use only	1
Internal	1.4	Internal use only	1
EnP4LED	1.3	Enable Port4 LED: 1: Drive LED pins of port4. 0: Do not drive LED pins of port4 for special application. In UTP application, this bit should be 1 to drive the LEDs of port 4. Reserved for original RTL8305S user only. Not used for general applications.	1
Reserved	1.2		1
Reserved	1.1		1
Reserved	1.0		1
Reserved	2.7~2.4		1
Internal	2.3~2.0		1111
Reserved	3.7~3.2		1
Internal	3.1~3.0	Internal use only	11
EthernetID	4~9	Device Ethernet MAC ID (6 bytes). Example: for MAC ID = 52 54 4c 83 05 b0. Byte4 = 0x52 (Byte 1 of MAC ID). Byte5 = 0x54 (Byte 2 of MAC ID). Byte6 = 0x4c (Byte 3 of MAC ID). Byte7 = 0x83 (Byte 4 of MAC ID). Byte8 = 0x05 (Byte 5 of MAC ID). Byte9 = 0xb0 (Byte 6 of MAC ID).	0x52 0x54 0x4c 0x83 0x05 0xb0
Reserved	10.7		1
P1VLANIndex[2]	10.6	Port 1 VLAN Index: P1VLANIndex[2:0]=001 means port 1 uses the second VLAN (VLAN B).	001
P1VLANIndex[1]	10.5		
P1VLANIndex[0]	10.4		
Reserved	10.3		1
P0VLANIndex[2]	10.2	Port 0 VLAN Index: P0VLANIndex[2:0] are used to assign the VLAN of port 0. For example, P0VLANIndex[2:0]=000 means port 0 use the first VLAN (VLAN A). P0VLANIndex[0] is bit0, P0VLANIndex[1] is bit1, P0VLANIndex[2] is bit2.	000
P0VLANIndex[1]	10.1		
P0VLANIndex[0]	10.0		
Reserved	11.7		1
P3VLANIndex[2]	11.6	Port 3 VLAN Index: P3VLANIndex[2:0]=011 means port 3 use the forth VLAN (VLAN D).	011
P3VLANIndex[1]	11.5		
P3VLANIndex[0]	11.4		

Cont...

Reserved	11.3		1
P2VLANIndex[2]	11.2	Port 2 VLAN Index: P2VLANIndex[2:0]=010 means port 2 use the third VLAN (VLAN C).	010
P2VLANIndex[1]	11.1		
P2VLANIndex[0]	11.0		
Reserved	12.7 12.6 12.5 12.3		1111
P4VLANIndex[2]	12.2~12.0	Port 4 VLAN Index: P4VLANIndex[2:0]=100 means port 4 use the fifth VLAN (VLAN E).	100
P4VLANIndex[1]			
P4VLANIndex[0]			
P3IRTag[1]	13.7	Insert/Remove Priority Tag of Port3: 11: Do not insert/remove Tag from Output High and Low Queue of Port3. 10: Insert Tag from Output High and Low Queue of Port3. 01: Insert Tag from Output High Queue only of Port3. 00: Remove Tag from Output High and Low Queue of Port3.	11
P3IRTag[0]	13.6		
P2IRTag[1]	13.5	Insert/Remove Priority Tag of Port2: 11: Do not insert/remove Tag from Output High and Low Queue of Port2. 10: Insert Tag from Output High and Low Queue of Port2. 01: Insert Tag from Output High Queue only of Port2. 00: Remove Tag from Output High and Low Queue of Port2.	11
P2IRTag[0]	13.4		
P1IRTag[1]	13.3	Insert/Remove Priority Tag of Port1: 11: Do not insert/remove Tag from Output High and Low Queue of Port1. 10: Insert Tag from Output High and Low Queue of Port1. 01: Insert Tag from Output High Queue only of Port1. 00: Remove Tag from Output High and Low Queue of Port1.	11
P1IRTag[0]	13.2		
P0IRTag[1]	13.1	Insert/Remove Priority Tag of Port0: 11: Do not insert/remove Tag from Output High and Low Queue of Port0. 10: Insert Tag from Output High and Low Queue of Port0. 01: Insert Tag from Output High Queue only of Port0. 00: Remove Tag from Output High and Low Queue of Port0.	11
P0IRTag[0]	13.0		
Internal	14~17	Internal use only	0xff 0xff 0xff 0xff
Internal	18~21	Internal use only	0xff 0xff 0xff 0xff
Internal	22~25	Internal use only	0xff 0xff 0xff 0xff
Internal	26~29	Internal use only	0xff 0xff 0xff 0xff
VIDA[11:0]	31.3~30.0	VLAN Identifier of VLAN A: Reg31.3=VIDA[11], Reg30.0=VIDA[0].	0x001
Reserved	31.7~31.4		1111
Reserved	32.7~32.5		111

Cont...

MemberA[4:0]	32.4~32.0	Member Set of VLAN A: MemberA[4:0] determines the VLAN member of VLAN A. MemberA[4:0]=10001 means port4 and port0 are the members of VLAN A. MemberA[4:0]=10010 means port4 and port1 are the members of VLAN A. MemberA[4:0]=11111 means all ports are the members of VLAN A.	10001
VIDB[11:0]	34.3~33.0	VLAN Identifier of VLAN B:	0x002
Reserved	34.7~34.4		1111
Reserved	35.7~35.5		111
MemberB[4:0]	35.4~35.0	Member Set of VLAN B: MemberB[4:0]=10010 means port4 and port1 are the members of VLAN B.	10010
VIDC[11:0]	37.3~36.0	VLAN Identifier of VLAN C:	0x003
Reserved	37.7~37.4		1111
Reserved	38.7~38.5		111
MemberC[4:0]	38.4~38.0	Member Set of VLAN C: MemberC[4:0]=10100 means port4 and port2 are the members of VLAN C.	10100
VIDD[11:0]	40.3~39.0	VLAN Identifier of VLAN D:	0x004
Reserved	40.7~40.4		1111
Reserved	41.7~41.5		111
MemberD[4:0]	41.4~41.0	Member Set of VLAN D: MemberD[4:0]=11000 means port4 and port3 are the members of VLAN D.	11000
VIDE[11:0]	43.3~42.0	VLAN Identifier of VLAN E:	0x005
Reserved	43.7~43.4		1111
Reserved	44.7~44.5		111
MemberE[4:0]	44.4~44.0	Member Set of VLAN E: MemberE[4:0]=11111 means all ports are the members of VLAN E.	11111
Reserved	45.7~6		1
DisVLAN	45.5	Disable VLAN: 1: Disable VLAN 0: Enable VLAN This register has higher priority than pin.	1
DisTagAware	45.4	Disable Tag Aware: 1: Disable the 802.1Q tagged-VID Aware function. The RTL8305SB will not check the tagged VID of a received frame to do the VLAN classification. The RTL8305SB will always use Port Based VLAN mapping. 0: Enable the Member Set Filtering function of VLAN Ingress Rule. the RTL8305SB will check the tagged VID of received frame to do the VLAN classification. The RTL8305SB will use tagged-VID VLAN mapping for tagged frame and will use Port Based VLAN mapping for untagged and priority-tagged frame.	1

Cont...

DisMemFilter	45.3	Disable Member Set Filtering: 1: Disable the Member Set Filtering function of the VLAN Ingress Rule. The RTL8305SB will not discard any frames associated with a VLAN for which that port is not in the member set. 0: Enable the Member Set Filtering function of the VLAN Ingress Rule. The RTL8305SB will discard any frames associated with a VLAN for which that port is not in the member set.	1
DisTagAdmitCtrl	45.2	Disable Tag Admit Control: Covers acceptable frame type. 1: Disable Tag Admit Control: Acceptable Frame Type is “Admit All”. The RTL8305SB will receive all frames. 0: Enable Tag Admit Control: Acceptable Frame Type is “Admit All Tagged”. The RTL8305SB will receive only the VLAN-tagged frame and drop all other untagged frame and priority tagged (VID=0) frame.	1
DisLeaky	45.1	Disable Leaky VLAN: 1: Disable to forward unicast frames to other VLAN. 0: Enable to forward unicast frames to other VLAN. Broadcast and multicast frames adhere to the VLAN configuration. This register has higher priority than pin.	1
DisARP	45.0	Disable ARP broadcast to all VLAN: 1: Disable to broadcast the ARP broadcast packet to all VLANs. 0: Enable to broadcast the ARP broadcast packet to all VLANs. ARP broadcast frame: DID is all F. This register has higher priority than pin.	1
Reserved	46.7		1
Internal	46.6	Internal use only	1
Internal	46.5~3	Internal use only	000
Internal	46.2~0	Internal use only	100
Internal	47~52	Internal use only	0x52 0x54 0x4c 0x83 0x05 0xb1

9. Electrical Characteristics

9.1 Absolute Maximum Ratings:

WARNING: Absolute maximum ratings are limits beyond which may cause permanent damage to the device or affect device reliability. All voltages are specified reference to GND unless otherwise specified.

Parameter	Min	Max	Units
Storage Temperature	-55	+150	°C
Vcc Supply Referenced to GND	-0.5	+4.0	V
Digital Input Voltage	-0.5	VDD	V
DC Output Voltage	-0.5	VDD	V

9.2 Operating Range:

Parameter	Min	Max	Units
Ambient Operating Temperature(Ta)	0	+70	°C
3.3V Vcc Supply Voltage Range(VDDAH)	3.15	3.45	V
2.5V Vcc Supply Voltage Range (VDDAL,VDD)	2.375	2.625	V

9.3 DC Characteristics

Parameter	SYM	Conditions	Min	Typical	Max	Units
Power Supply Current for 2.5V	I _{cc}	10 Base-T, idle 10 Base-T, Peak continuous 100% utilization 100 Base-TX, idle 100 Base-TX, Peak continuous 100% utilization Power saving Power down				mA
Power Supply Current for 3.3V	I _{cc}	10 Base-T, idle 10 Base-T, Peak continuous 100% utilization 100 Base-TX, idle 100 Base-TX, Peak continuous 100% utilization Power saving Power down				mA
Total Power Consumption for all ports	PS	10 Base-T, idle 10 Base-T, Peak continuous 100% utilization 100 Base-TX, idle 100 Base-TX, Peak continuous 100% utilization Power saving Power down				mW
TTL Input High Voltage	V _{ih}		1.5			V
TTL Input Low Voltage	V _{il}				1.0	V
TTL Input Current	I _{in}		-10		10	uA
TTL Input Capacitance	C _{in}			3		pF
Output High Voltage	V _{oh}		2.25		2.75	V
Output Low voltage	V _{ol}		0		0.25	V

Parameter	SYM	Conditions	Min	Typical	Max	Units
Output Three state Leakage Current	I_{OZ}				10	μA
Transmitter, 100Base-TX (1:1 Transformer Ratio)						
TX+/- Output Current High	I_{OH}				20	mA
TX+/- Output Current Low	I_{OL}		0			μA
Transmitter, 10Base-T(1:1 Transformer Ratio)						
TX+/- Output Current High	I_{OH}				50	mA
TX+/- Output Current Low	I_{OL}		0			μA
Receiver, 100Base-TX						
RX+/- Common-mode input voltage				1.6		V
RX+/- Differential input resistance				20		k Ω
Receiver, 10BaseT						
Differential Input Resistance				20		k Ω
Input Squelch Threshold				340		mV

9.4 AC Characteristics

Parameter	SYM	Conditions	Min	Typical	Max	Units
Transmitter, 100Base-TX						
Differential Output Voltage, peak-to-peak	V_{OD}	50 Ω from each output to Vcc, Best-fit over 14 bit times				V
Differential Output Voltage Symmetry	V_{OS}	50 Ω from each output to Vcc, $ V_{p+} / V_{p-} $				%
Differential Output Overshoot	V_{OO}	Percent of V_{p+} or V_{p-}				%
Rise/Fall time	t_r, t_f	10-90% of V_{p+} or V_{p-}				ns
Rise/Fall time imbalance	$ t_r - t_f $					ps
Duty Cycle Distortion		Deviation from best-fit time-grid, 010101 ... Sequence				ps
Timing jitter		Idle pattern				ns
Transmitter, 10Base-T						
Differential Output Voltage, peak-to-peak	V_{OD}	50 Ω from each output to Vcc, all pattern				V
TP_IDL Silence Duration		Period of time from start of TP_IDL to link pulses or period of time between link pulses				ms
TD Short Circuit Fault Tolerance		Peak output current on TD short circuit for 10 seconds.				mA
TD Differential Output Impedance (return loss)		Return loss from 5MHz to 10MHz for reference resistance of 100 Ω .				dB
TD Common-Mode Output Voltage	Ecm	Terminate each end with 50 Ω resistive load.				mV
Transmitter Output Jitter						ns
RD Differential Output Impedance (return loss)		Return loss from 5MHz to 10MHz for reference resistance of 100 Ω .				dB
Harmonic Content		dB below fundamental, 20 cycles of all ones data				dB
Start-of-idle Pulse width		TP_IDL width				ns

9.5 Digital Timing Characteristics

Parameter	SYM	Conditions	Min	Typical	Max	Units
100Base-TX Transmit System Timing						
Active TX_EN Sampled to first bit of “J” on MDI output						Bits
Inactive TX_EN Sampled to first bit of “T” on MDI output						Bits
TX Propagation Delay	t _{TXpd}	From TXD[1:0] to TXOP/N				Bits
100Base-TX Receive System Timing						
First bit of “J” on MDI input to CRS_DV assert		From RXIP/N to CRS_DV		6	8	Bits
First bit of “T” on MDI input to CRS_DV de-assert		From RXIP/N to CRS_DV		16	18	Bits
RX Propagation Delay	t _{RXpd}	From RXIP/N to RXD[1:0]		15	17	Bits
10Base-T Transmit System Timing						
TX Propagation Delay	t _{TXpd}	From TXD[1:0] to TXOP/N		5	6	Bits
TXEN to MDI output		From TXEN assert to TXOP/N		5	6	Bits
10Base-T Receive System Timing						
Carrier Sense Turn-on delay	t _{CSOn}	Preamble on RXIP/N to CRS_DV asserted		12		Bits
Carrier Sense Turn-off Delay	t _{CSOff}	TP_IDL to CRS_DV de-asserted		8	9	Bits
RX Propagation Delay	t _{RXpd}	From RXIP/N to RXD[1:0]	9		12	Bits
LED timing						
LED On Time	t _{LEDOn}	While LED blinking	43		120	ms
LED Off Time	t _{LEDOff}	While LED blinking	43		120	ms
SMI timing						
MDC		MDC clock rate			25	MHz
MDIO Setup Time		Write cycle	10			ns
MDIO Hold Time		Write cycle			10	ns
MDIO output delay relative to rising edge of MDC		Read cycle			10	ns

9.6 Thermal Data

Parameter	SYM	Conditions	Min	Typical	Max	Units
Thermal resistance: junction to ambient, 0 ft/s airflow	θ _{ja}	4 layers PCB, ambient temperature 25°C				°C/W
Thermal resistance: junction to case, 0 ft/s airflow	θ _{jc}	4 layers PCB, ambient temperature 25°C				°C/W

10. Application Information

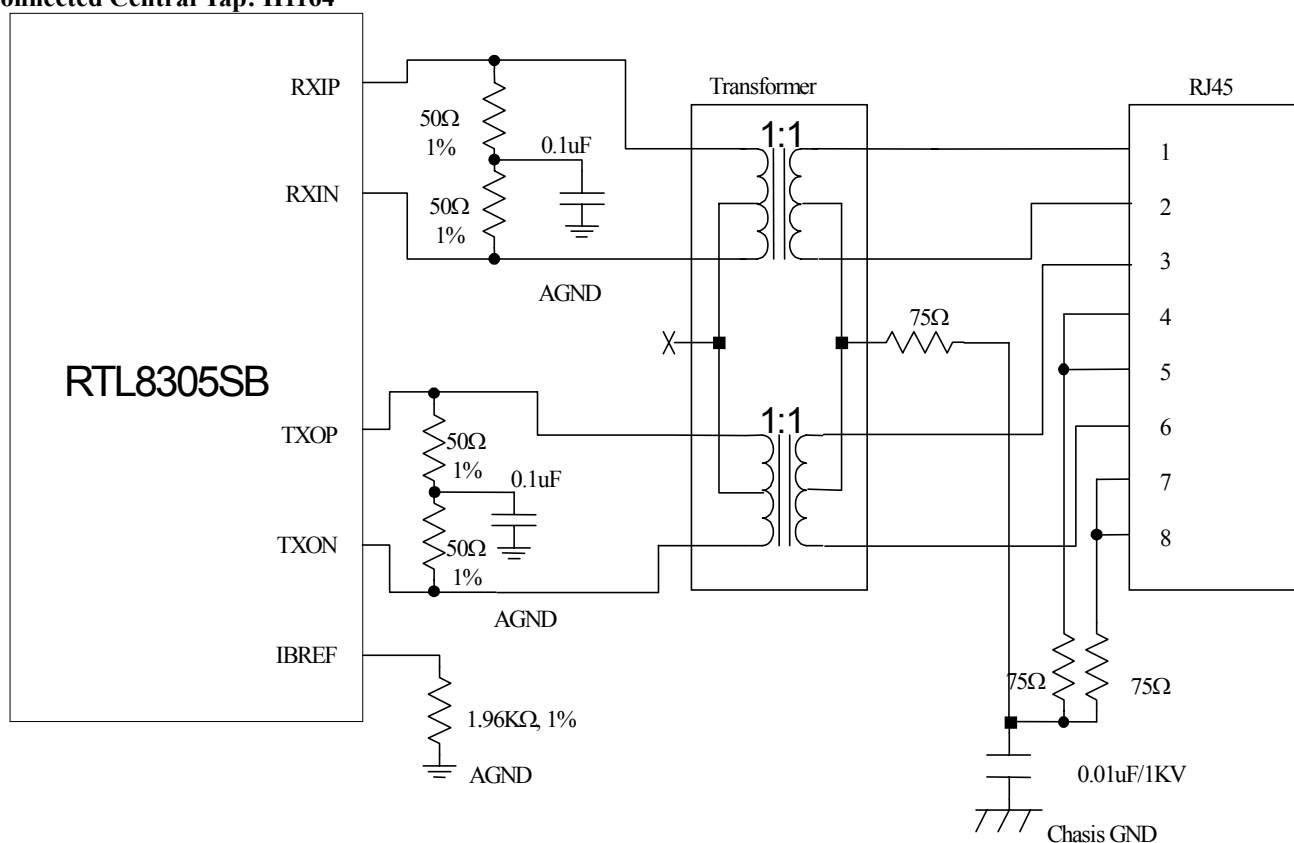
10.1 UTP (10Base-T/100Base-TX) Application

In reviewing this material, please be advised that the center-tap in primary side of the transformer should be left floating and can not be connected to ground through capacitors.

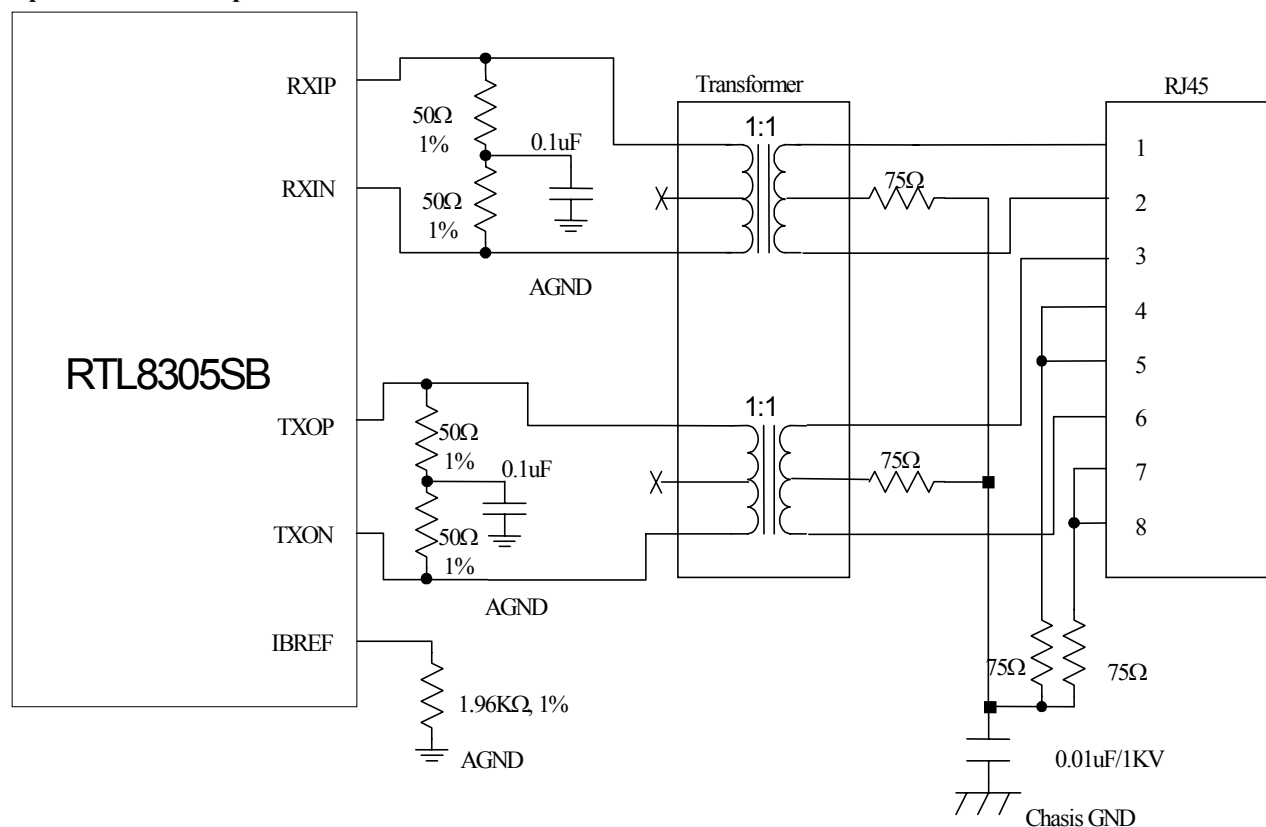
Vendor	Quad	Single
Pulse	H1164	H1102
Magnetic 1	ML164	ML102

Two types of transformers are generally used for the RTL8305SB. One is a Quad (4 port) transformer with one common pin on both sides for internal connected central tap. Another is a Single (1 port) transformer with two pins on both sides for a separate central tap.

Connected Central Tap: H1164



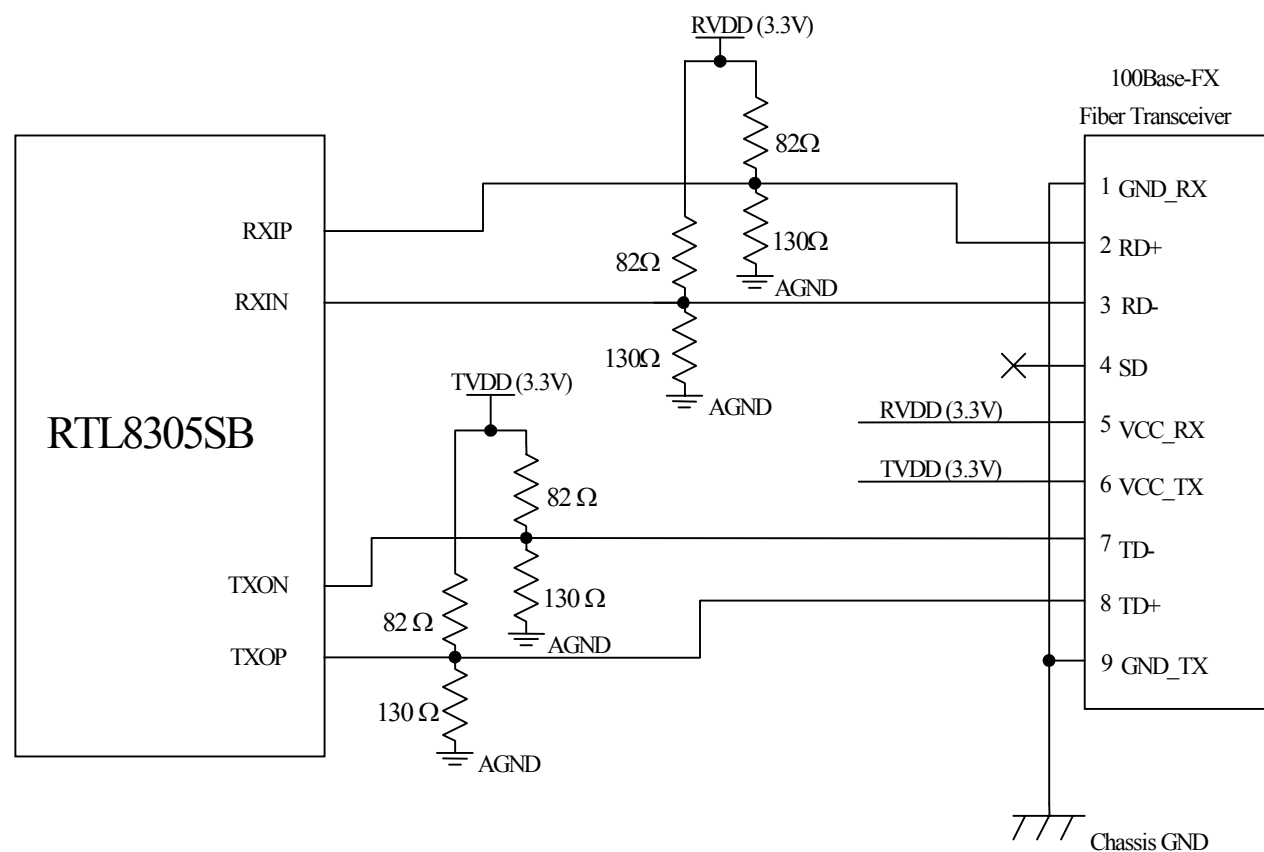
RTL8305SB UTP Application for Transformer with Connected Central Tap

Separate Central Tap: H1102


RTL8305SB UTP Application for Transformer with Separated Central Tap

10.2 100Base-FX Application:

The following is an example for DELTA OPT-155A2H1 (3.3V fiber transceiver, 1*9 SC Duplex FDDI Fast Ethernet Optical Transceiver Module)

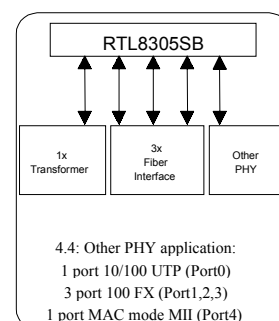
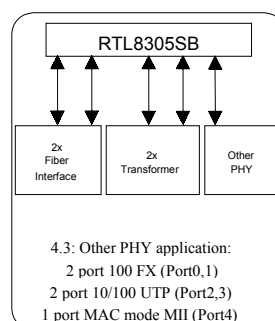
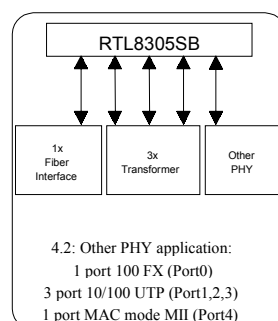
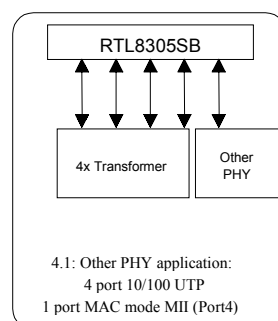
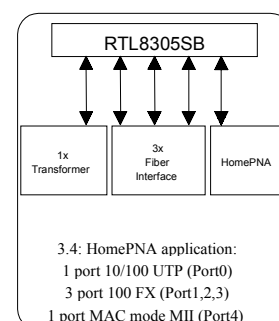
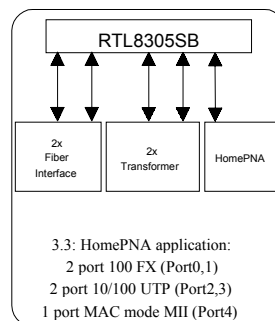
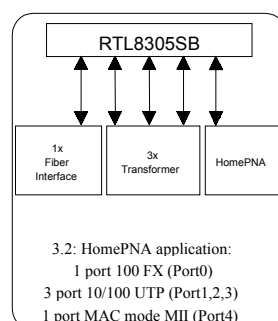
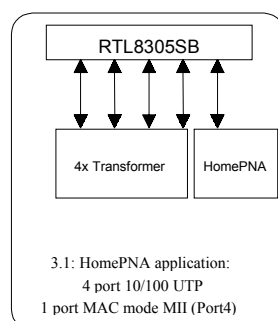
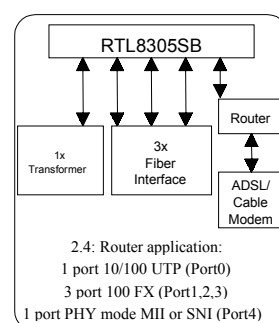
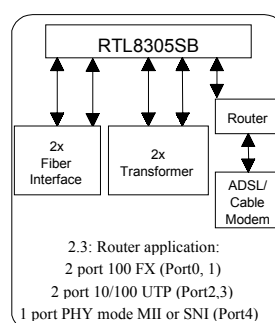
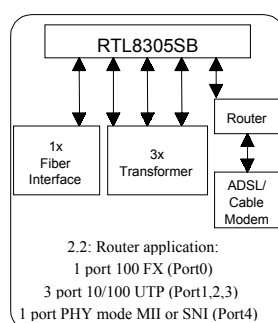
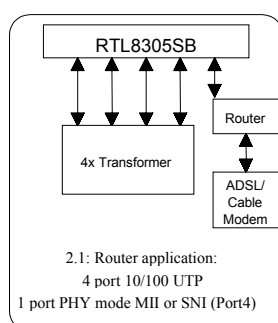
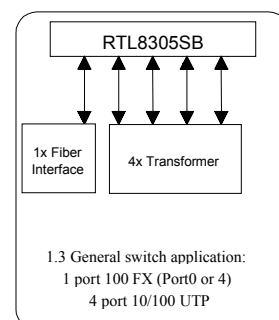
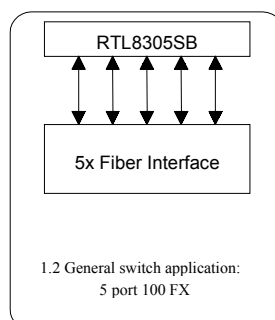
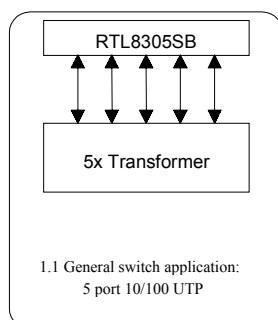


RTL8305SB 100Base-FX Application

11. System Application Diagram

General System Application

1. General switch application
2. Router application:
3. HomePNA application
4. Other PHY application



12. Design and Layout Guide

In order to achieve maximum performance using the RTL8305SB, good design attention is required throughout the design and layout process. The following are some suggestions on recommendations to implement a high performance system.

General Guidelines

- Provide a good power source, minimizing noise from switching power supply circuits (<50mV).
- Verify the qualities of critical components such as clock source and transformer to meet application requirements.
- Keep power and ground noise levels below 50mV.
- Use bulk capacitors (4.7 μ F-10 μ F) between the power and ground planes.
- Use 0.1 μ F de-coupling capacitors to reduce high-frequency noise on the power and ground planes.
- Keep de-coupling capacitors as close as possible to the RTL8305SB chip.

Differential Signal Layout Guidelines

- Keep differential pairs as close as possible and route both traces as identically as possible.
- Avoid vias and layer changes if possible.
- Keep transmit and receive pairs away from each other. Run orthogonal or separate by a ground plane.

Clock Circuit

- Surround the clock by ground trace to minimize the high-frequency emission, if possible.

2.5V Power

- Do not connect a bead directly between the collector of the PNP transistor and VDDAL. This will significantly affect the stability of the 2.5V power if such a bead is used.
- Use a bulk capacitor (4.7 μ F-10 μ F) between the collector of the PNP transistor and the ground plane.
- Do not use one PNP transistor for more than one RTL8305SB chip, even if the rating is enough. Use one transistor for each RTL8305SB chip.

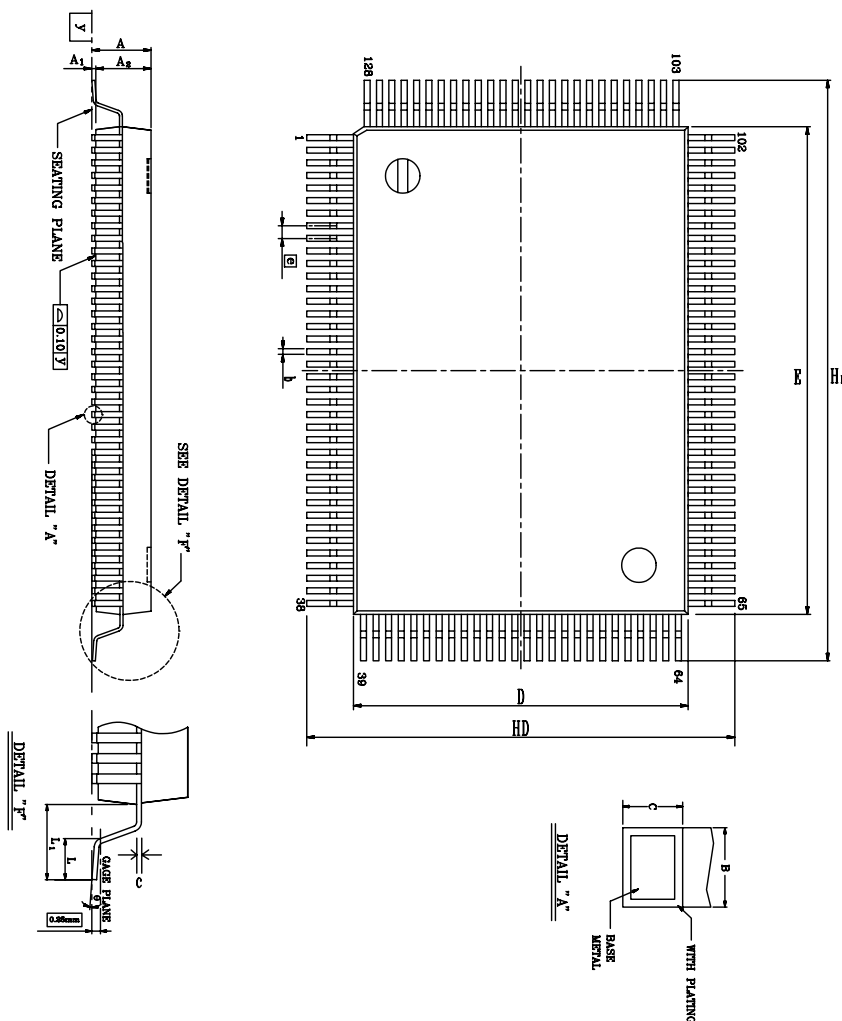
Power Planes

- Divide the power plane into 2.5V digital, and 3.3V analog.
- Use 0.1 μ F decoupling capacitors and bulk capacitors between each power plane and the ground plane.

Ground Planes

- Keep the system ground region as one continuous, unbroken plane that extends from the primary side of the transformer to the rest of the board.
- Place a moat (gap) between the system ground and chassis ground.
- Ensure the chassis ground area is voided at some point such that no ground loop exists on the chassis ground area.

13. Mechanical Dimensions



Symbol	Dimension in inch			Dimension in mm		
	Min	Typical	Max	Min	Typical	Max
A	-	-	0.134	-	-	3.40
A1	0.004	0.010	0.036	0.10	0.25	0.91
A2	0.102	0.112	0.122	2.60	2.85	3.10
b	0.005	0.009	0.013	0.12	0.22	0.32
c	0.002	0.006	0.010	0.05	0.15	0.25
D	0.541	0.551	0.561	13.75	14.00	14.25
E	0.778	0.787	0.797	19.75	20.00	20.25
e	0.010	0.020	0.030	0.25	0.5	0.75
HD	0.665	0.677	0.689	16.90	17.20	17.50
HE	0.902	0.913	0.925	22.90	23.20	23.50
L	0.027	0.035	0.043	0.68	0.88	1.08
L1	0.053	0.063	0.073	1.35	1.60	1.85
y	-	-	0.004	-	-	0.10
θ	0°	-	12°	0°	-	12°

1. Dimensions D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. should be based on final visual inspection spec.

TITLE: 128 QFP (14x20 mm) PACKAGE OUTLINE			
-CU L/F, FOOTPRINT 3.2 mm			
LEADFRAME MATERIAL:			
APPROVE		DOC. NO.	530-ASS-P004
		VERSION	1
		PAGE	OF
CHECK		DWG NO.	Q128 - 1
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