Integrated Circuit Systems, Inc.

Clock Synchronizer and Multiplier

General Description

The **AV9170** generates an output clock which is synchronized to a given continuous input clock with zero delay (±1ns). Using ICS's proprietary phase-locked loop (PLL) analog CMOS technology, the **AV9170** is useful for regenerating clocks in high speed systems where skew is a major concern. By the use of the two select pins, multiples or divisions of the input clock can be generated with zero delay (see Tables 2 and 3). The standard versions produce two outputs, where CLK2 is always a divide by two version of CLK1.

The **AV9170** is also useful to recover poor duty cycle clocks. A 50 MHz signal with a 20/80% duty cycle, for example, can be regenerated to the 48/52% typical of the part.

The **AV9170** allows the user to control the PLL feedback, making it possible, with an additional 74F240 octal buffer (or other such device that offers controlled skew outputs), to synchronize up to 8 output clocks with zero delay compared to the input (see Figure 1). Application notes for the **AV9170** are available. Please consult ICS.

Features

- On-chip Phase-Locked Loop for clocks synchronization
- Synchronizes frequencies up to 100 MHz (output)
- ±1ns skew (max) between input and output clocks
- Can recover poor duty cycle clocks
- CLK1 and CLK2 skew controlled to within ±1ns
- 5 volt only power supply
- Low power CMOS technology
- Small 8-pin DIP or SOIC package
- On chip loop filter
- **AV9170-01**, -04 for output clocks 20-100 MHz
- **AV9170-02**, -05 for output clocks 5-25 MHz

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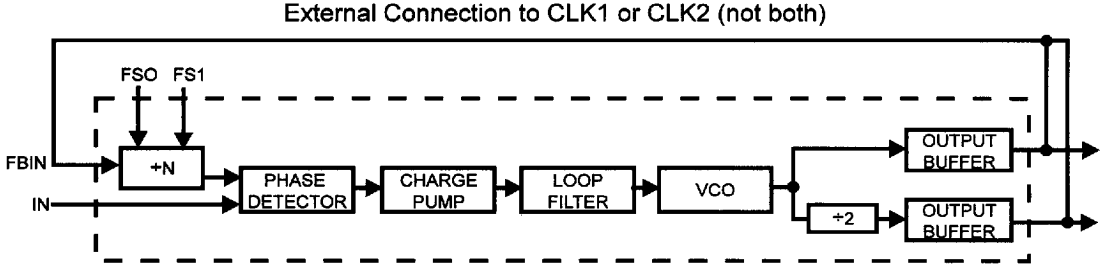
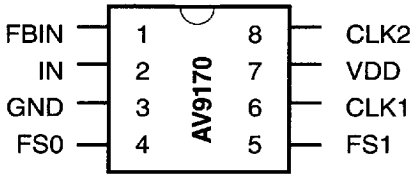
Block Diagram



Pin Configuration



8-Pin DIP or SOIC
K-3, K-6

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	FBIN	Input	FEEDBACK INPUT
2	IN	Input	INPUT for reference clock
3	GND	-	GROUND
4	FS0	Input	FREQUENCY SELECT 0
5	FS1	Input	FREQUENCY SELECT 1
6	CLK1	Output	CLOCK output 1 (See Tables 1, 2, 3, 6, 7 for values)
7	VDD	-	Power Supply (+5V)
8	CLK2	Output	CLOCK output 2 (See Tables 1, 2, 3, 6, 7 for values)

Using the AV9170

The **AV9170** has the following characteristics:

1. Rising edges at IN and FBIN are lined up. Falling edges are not synchronized.

2. The relationship between the frequencies at FBIN and IN is shown in Table 1.

Table 1

FS1	FS0	f_{FBIN}(-01, -02)	f_{FBIN}(-04, -05)
0	0	$2 \bullet f_{IN}$	$3 \bullet f_{IN}$
0	1	$4 \bullet f_{IN}$	$5 \bullet f_{IN}$
1	0	f_{IN}	$6 \bullet f_{IN}$
1	1	$8 \bullet f_{IN}$	$10 \bullet f_{IN}$

3. The frequency of CLK2 is half the CLK1 frequency.

4. The CLK1 frequency ranges are:

AV9170-01, -04 $\quad 20 < f_{CLK1} < 100$ MHz
AV9170-01, -05 $\quad 5 < f_{CLK1} < 25$ MHz

The **AV9170** will only operate correctly within these frequency ranges.

Eliminate High Speed Clock Routing Problems

The **AV9170** makes it possible to route lower speed clocks over long distances on the PC board and to place an **AV9170** next to the device requiring a higher speed clock. The multiplied output can then be used to produce a phase locked, higher speed output clock.

Compensate for Propagation Delays

Including an **AV9170** in a timing loop allows the use of PALs, gate arrays, etc., with loose timing specifications. The **AV9170** compensates for the delay through the PAL and synchronizes the output to the input reference clock.

Operating Frequency Range

The **AV9170** is offered in versions optimized for operation in two frequency ranges. The -01 and -04 cover high frequencies, 20 to 100 MHz. The -02 and -05 operate from 5 to 25 MHz. The **AV9170** can be supplied with custom multiplication factors and operating ranges. Consult ICS for details.

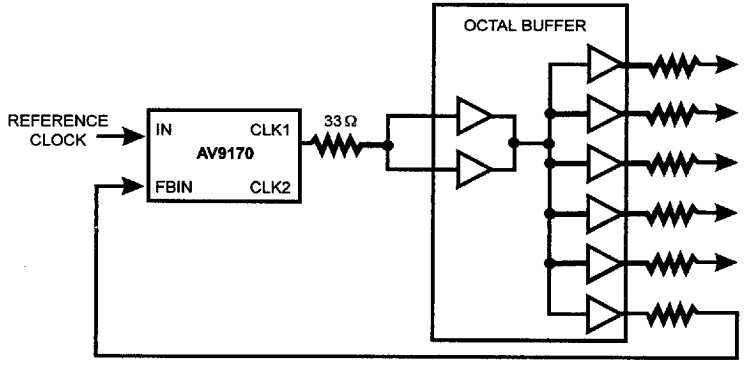


Figure 1: Application of AV9170 for Multiple Outputs

Using CLK2 Feedback

Connecting CLK2 to FBIN as shown in Figure 2 will cause all of the rising edges to be aligned (Figure 4)

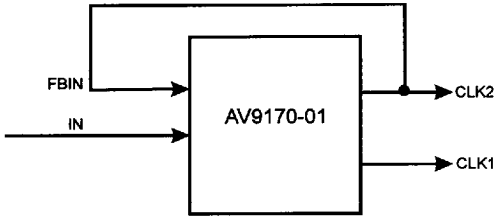


Figure 2

For CLK2 frequencies 10 - 50 MHz (-01)
For CLK2 frequencies 2.5 - 12.5 MHz (-02)

Using CLK1 Feedback

With CLK1 connected to FBIN as shown in Figure 3, the input and CLK1 output will be aligned on the rising edge, but CLK2 can be either rising or falling (Figure 5). Consult ICS if the CLK1 frequency is desired to be higher than 100 MHz.

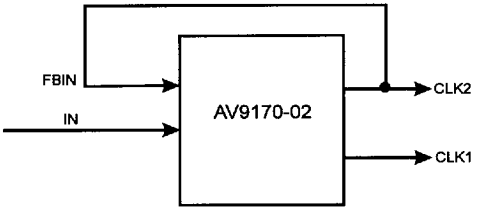


Figure 3

For CLK1 frequencies 20 - 100 MHz (-01)
For CLK1 frequencies 5 - 25 MHz (-02)

Table 2: Decoding Table for AV9170-01, -02 with CLK2 Feedback

FS1	FS0	CLK1	CLK2
0	0	INx4	INx2
0	1	INx8	INx4
1	0	INx2	IN
1	1	INx16	INx8

Table 3: Decoding Table for AV9170-01, -02 with CLK1 Feedback

FS1	FS0	CLK1	CLK2
0	0	INx2	IN
0	1	INx4	INx2
1	0	IN	IN+2
1	1	INx8	INx4

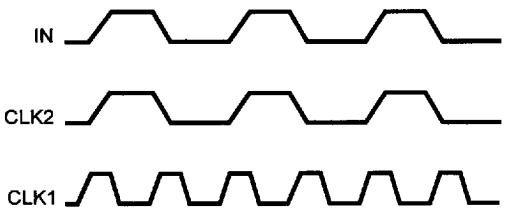


Figure 4: Input and Output Clock Waveforms with CLK2 Connected to FBIN

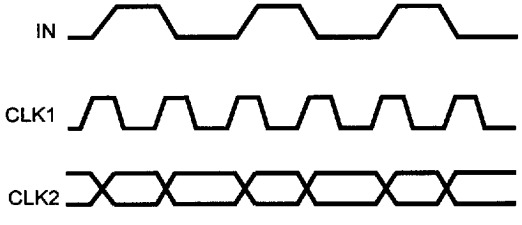


Figure 5: Input and Output Clock Waveforms with CLK1 Connected to FBIN

Using CLK2 Feedback

Connecting CLK2 to FBIN as shown in Figure 2 will cause all of the rising edges to be aligned (Figure 4)

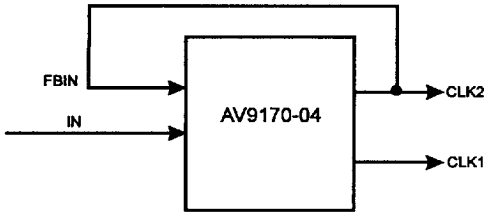


Figure 6

For CLK2 frequencies 10 - 50 MHz (-04)
For CLK2 frequencies 2.5 - 12.5 MHz (-05)

Using CLK1 Feedback

With CLK1 connected to FBIN as shown in Figure 3, the input and CLK1 output will be aligned on the rising edge, but CLK2 can be either rising or falling (Figure 5). Consult ICS if the CLK1 frequency is desired to be higher than 100 MHz.

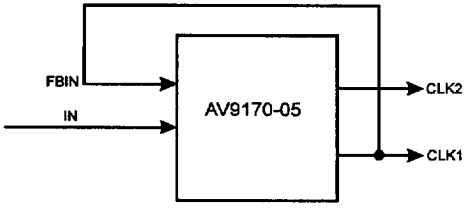


Figure 7

For CLK1 frequencies 20 - 100 MHz (-04)
For CLK1 frequencies 5 - 25 MHz (-05)

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Table 4: Decoding Table for AV9170-04, -05 with CLK2 Feedback

FS1	FS0	CLK1	CLK2
0	0	INx4	INx2
0	1	INx8	INx4
1	0	INx2	IN
1	1	INx16	INx8

Table 5: Decoding Table for AV9170-04, -05 with CLK1 Feedback

FS1	FS0	CLK1	CLK2
0	0	INx2	IN
0	1	INx4	INx2
1	0	IN	IN÷2
1	1	INx8	INx4

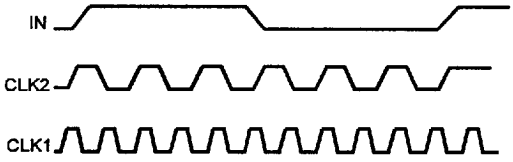


Figure 8: Input and Output Clock Waveforms with CLK2 Connected to FBIN

Figure 9: Input and Output Clock Waveforms with CLK1 Connected to FBIN

Absolute Maximum Ratings

VDD referenced to GND 7V
Operating temperature under bias ..... 0°C to +70°C
Storage temperature ..... -65°C to +150°C
Voltage on I/O pins referenced to GND..... GND -0.5V to VDD +0.5V
Power dissipation ..... 0.5 Watts

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics

V_{DD} = +5V±5%, T_A=0°C to 70°C (unless otherwise stated)

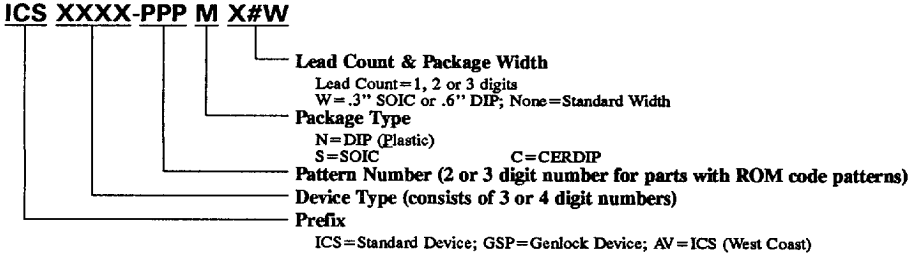
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DC/CHARACTERISTICS						
Input Low Voltage	V_{IL}	V_{DD} = 5V	-	-	0.8	V
Input High Voltage	V_{IH}	V_{DD} = 5V	2.0	-	-	V
Input Low Current	I_{IL}	V_{IN} = 0V	-5	-	5	µA
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5	-	5	µA
Output Low Voltage	V_{OL}	I_{OL} = 8mA	-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} =-1mA, V_{DD} = 5.0V	V_{DD}-.4V	-	-	V
Output High Voltage	V_{OH}	I_{OH} =-4mA, V_{DD} =5.0V	V_{DD}-.8V	-	-	V
Output High Voltage	V_{OH}	I_{OH} =-8mA	2.4	-	-	V
Supply Current	I_{DD}	Unloaded, 100 MHz	-	20	50	mA
AC/CHARACTERISTICS						
Input Clock Rise Time	$ICLK_r$		-	-	10	ns
Input Clock Fall Time	$ICLK_f$		-	-	10	ns
Output Rise time, 0.8 to 2.0V	t_r	15pF load	-	1	2	ns
Rise time, 20% to 80%V_{DD}	t_r	15pF load	-	2	4	ns
Output Fall time, 2.0 to 0.8V	t_f		-	1	2	ns
Fall time, 80% to 20% V_{DD}	t_f		-	2	48/52	ns
Output Duty Cycle, AV9170-01	d_t	15pF load. Note 2,3	40	48/52	60	%
Output Duty Cycle, AV9170-02	d_t	15pF load. Note 2,3	45	49/51	55	%
Jitter, 1 sigma	T_{1s}		-200	±120	300	ps
Jitter, absolute	T_{abs}	For CLK1 >10 MHz	-500	±250	500	ps
Jitter, absolute	T_{abs}	For CLK1 <10 MHz	-2%		2	%
Input Frequency	f_i	Note 1	1		67	MHz
Output Frequency CLK1	f_o	AV9170-01, - 04	20		100	MHz
Output Frequency CLK1	f_o	AV9170-01, - 05	5		25	MHz
FBIN to IN skew	t_{skew1}	Note 2,4. Input rise time <5ns	-1	0.4	1	ns
FBIN to IN skew	t_{skew1}	Note 2,4. Input rise time <10ns	-2	0.6	2	ns
CLK1 to CLK2 skew	t_{skew2}	Note 2,4	-1	0.4	1	ns

NOTES:
1. It may be possible to operate the AV9170 outside of these ranges. Consult ICS for your specific application.
2. All AC Specifications are measured with a 50Ω transmission line, load terminated with 50Ω to 1.4V.
3. Duty cycle measured at 1.4V.
4. Skew measured at 1.4V on rising edges.

Ordering Information

AV9170-xxCN8 (8 Lead Plastic DIP (300 mils)
AV9170-xxCS8 (8 Lead SOIC (150 mils)*
AV9170-xxCC8 (8 Lead CERDIP)

Example:



For the SOIC package, the AV9170-01 is marked ICS70-1 and the AV9170-02 is marked ICS70-2.

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