Integrated
Circuit
Systems, Inc.

AV9173

Video Genlock PLL

Features

- Phase-detector/VCO circuit block
- Ideal for genlock system
- Reference clock range 15 kHz to 1 MHz
- Output clock range 1.25 to 50 MHz
- On chip loop filter
- Single 5 volt power supply
- Low power CMOS technology
- Small 8 pin DIP or SOIC package

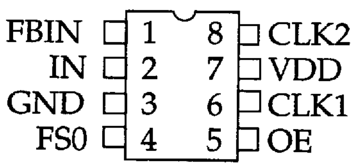
General Description

The AV9173 provides the analog circuit blocks required for implementing a video genlock dot (pixel) clock generator. It contains a phase detector, charge pump, loop filter, and voltage-controlled oscillator (VCO). By grouping these critical analog blocks into one IC and utilizing external digital functions, performance and design flexibility are optimized as are development time and system cost.

When used with an external clock divider, the AV9173 forms a Phase Locked Loop configured as a frequency synthesizer. The AV9173 is designed to accept video horizontal synchronization (h-sync) pulses and produce a video dot clock. A separated, negative-going sync input reference pulse is required at pin 2 (IN). The use of unstable video sources, such as a VCR output, is not recommended.

The AV9173 is also suited for other clock recovery applications in such areas as data communications.

Pin Configuration

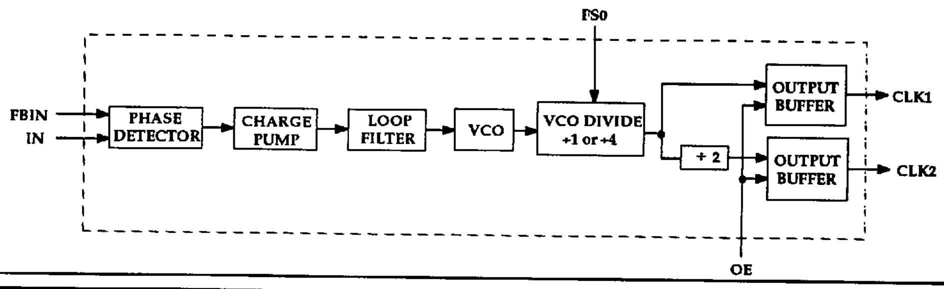


AV9173-01

Pin Description

Pin Name	Pin #	Type	Description
FBIN	1	Input	FEEDBACK INPUT
IN	2	Input	INPUT for reference sync pulse
GND	3	-	GROUND
FS0	4	Input	FREQUENCY SELECT 0 input
OE	5	Input	OUTPUT ENABLE
CLK1	6	Output	CLOCK output 1
VDD	7	-	Power supply (+5V)
CLK2	8	Output	CLOCK output 2

Block Diagram



Using the AV9173

Most video sources, such as video cameras, are asynchronous, free-running devices. To digitize video or synchronize one video source to another free-running reference video source, a video "genlock" (generator lock) circuit is required. The AV9173 integrates the analog blocks which make the task much easier.

In the complete video genlock circuit, the primary function of the AV9173 is to provide the analog circuitry required to generate the video dot clock within a PLL. This application is illustrated in Figure 1. The input reference signal for this circuit is the horizontal synchronization (h-sync) signal. If a composite video reference source is being used, the h-sync pulses must be separated from the composite signal. A video sync separator circuit, such as the National Semiconductor LM1881, can be used for this purpose.

The clock feedback divider shown in Figure 1 is a digital divider used within the PLL to multiply the reference frequency. Its divide ratio establishes how many video dot clock cycles occur per h-sync pulse. For example, if 880 pixel clocks are desired per h-sync pulse then the divider ratio is set to 880. Hence, together the h-sync frequency and external divider ratio establish the dot clock frequency:

$$f_{OUT} = f_{IN} \cdot N \quad \text{where N is external divide ratio}$$

Both AV9173 input pins IN and FBIN respond only to negative-going clock edges of the input signal. The h-sync signal must be constant frequency and stable (low clock jitter) for creation of a stable output clock.

The output hook-up of the AV9173 is dictated by the desired dot clock frequency. The primary consideration is the internal VCO which operates over a frequency range of 10 MHz to 50 MHz. Because of the selectable VCO output divider and the additional divider on output CLK2, four distinct output frequency ranges can be achieved. The following table lists these ranges and the corresponding device configuration.

FS0 State	Output Used	Frequency Range
0	CLK1	10 - 50 MHz
0	CLK2	5 - 25 MHz
1	CLK1	2.5 - 12.5 MHz
1	CLK2	1.25 - 6.25 MHz

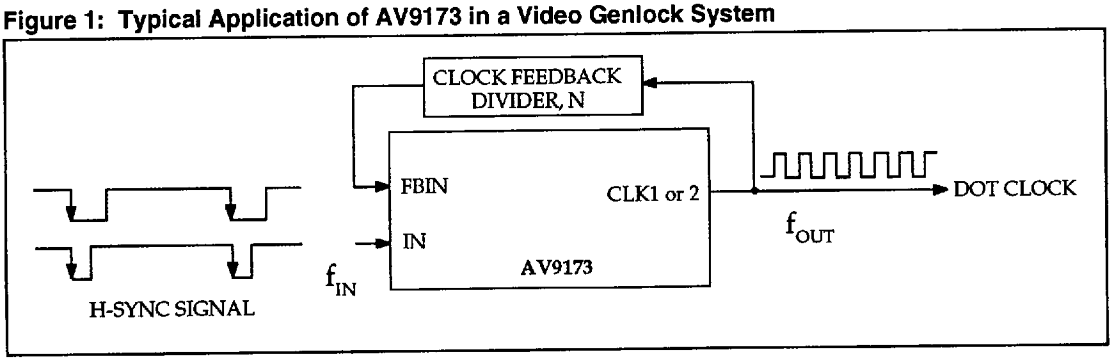
Note that both outputs, CLK1 and CLK2, are available during operation even though only one is fed back via the external clock divider.

Pin 5, OE, tri-states both CLK1 and CLK2 upon logic low input. This feature can be used to revert dot clock control to the system clock when not in genlock mode (hence, when in genlock mode the system dot clock must be tri-stated).

When unused, inputs FS0 and OE must be tied to either GND (logic low) or VDD (logic high).

For further discussion of VCO/PLL operation as it applies to the AV9173, please refer to the AV9170 application note. The AV9170 is a similar device with fixed feedback dividers for skew control applications.

Figure 1: Typical Application of AV9173 in a Video Genlock System



AV9173

Absolute Maximum Ratings

VDD referenced to GND..7V
Operating temperature under bias............0°C to +70°C
Storage temperature...............................-65°C to +150°C
Voltage on I/O pins referenced to GND...... GND -0.5V to VDD +0.5V
Power dissipation..0.5 Watts

Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the devices at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may affect the reliability of the device.

Electrical Characteristics

(V_{DD}= +5V± 5%, T_A = 0°C to 70°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
DC Characteristics						
V_{IL}	Input Low Voltage	-	-	0.8	V	V_{DD} = 5V
V_{IH}	Input High Voltage	2.0	-	-	V	V_{DD} = 5V
I_{IL}	Input Low Current	-5	-	-	µA	V_{IN} = 0V
I_{IH}	Input High Current	-5	-	5	µA	V_{IN} = V_{DD}
V_{OL}	Output Low Voltage	-	-	0.4	V	I_{OL} = 8mA
V_{OH}	Output High Voltage	V_{DD}-.4V	-	-	V	I_{OH} = -1mA,V_{DD}=5.0V
V_{OH}	Output High Voltage	V_{DD}-.8V	-	-	V	I_{OH} = -4mA,V_{DD}=5.0V
V_{OH}	Output High Voltage	2.4	-	-	V	I_{OH} = -8mA
I_{DD}	Supply Current	-	20	50	mA	Unloaded, 50MHz
AC Characteristics						
$ICLK_r$	Input Clock Rise Time	-	-	10	ns	Note 1
$ICLK_f$	Input Clock Fall Time	-	-	10	ns	Note 1
t_r	Output Rise time, 0.8 to 2.0V	-	1	2	ns	15 pf load
t_r	Rise time, 20% to 80% V_{DD}	-	2	4	ns	15 pf load
t_f	Output Fall time, 2.0 to 0.8V	-	1	2	ns	15 pf load
t_f	Fall time, 80% to 20% V_{DD}	-	2	4	ns	15 pf load
d_t	Output Duty cycle	40	48/52	60	%	15 pf load. Note 2
T_{1s}	Cycle-to-cycle jitter, 1 sigma		120	300	ps	
T_{abs}	Cycle-to-cycle Jitter, absolute	-500	±250	500	ps	
TL_{abs}	Line-to-line jitter, absolute		±4		ns	Note 3
f_i	Input Frequency, IN or FBIN	25		1000	kHz	Note 1
f_{VCO}	VCO clock speed	10		50	MHz	Note 1

NOTES:
1. It may be possible to operate the AV9173 outside of these ranges. Consult ICS for your specific application.
2. Duty cycle measured at 1.4V.
3. Input Reference Frequency = 15 kHz, Output Frequency = 25 MHz. Jitter measured between adjacent vertical pixels.

Ordering Information

Part Number	Part Marking	Temperature Range	Package Type
AV9173-01CC8	AV9173-01	0°C to +70°C	8 lead CERDIP
AV9173-01CN8	AV9173-01	0°C to +70°C	8 lead Plastic DIP (300 mils)
AV9173-01CS8	AV73-1	0°C to +70°C	8 lead SOIC (150 mils)

For the SOIC package, the AV9173-01 is marked AV73-1.